Specification

400G QSFP112 AOC

Active Optical Cable

T Q S - P 1 6 H 8 - X C Z x x

Length: xxM
1~50M

General Description

The TQS-P16H8-VAZ is a QSFP112 to QSFP112 active optical cable for short-range data communication and interconnect applications. Each AOC has 4 duplex channels with 425Gbit/s aggregate bandwidth. Each channel operates with PAM4 modulation scheme at 53.125G baud rate, and up to 60m using OM3 fiber or 100m using OM4 fiber.

Features and Benefits

- **QSFP112 Serial Optical Interface**
  - **4x100G PAM4 retimed 400GAUI-4 electrical interface**
  - **Active Optical Cable**
  - **4 channel VCSEL arrays and 4 channels PIN photo detector arrays**
  - **Maximum link length of 60m on OM3 or 100m on OM4**
- **QSFP112 MSA Compliant**
  - **Hot Pluggable QSFP112 form factor**
  - **Compliant to QSFP112_MSA_Specification_Rev2.1.1**
  - **Compliant with CMIS 5.2**
- **Support Protocol**
  - **Compliant with IEEE 802.3db**
  - **Compliant to IEEE 802.3ck**
- **Low Power Consumption**
  - **Less than 8W per cable end in temperature range of 0 to 70℃**

Applications

- **400GBASE-AOC 400G Ethernet**
- **Data center**

Absolute Maximum Ratings and Recommended Operating Conditions

- Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	Ts	-40	85	℃
Case Operating Temperature	Top	0	70	℃
Relative Humidity (non-condensation)	RH	15	85	%
Supply Voltage	Vcc	-0.5	3.6	V

➢ Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Operating Case Temperature	Top	0	70	°C
Relative Humidity (non-condensation)	RH	15	85	%
Power Supply Voltage	Vcc	3.135	3.465	V
Total Power Consumption per end[1]	Pc		8	W
Supply Current per end			2.55	A
Bit Rate	BR		425	Gbps
I2C Clock Frequency		0	400	kHz

Notes: Under condition of 3.465V operating supply voltage, and 70℃ case temperature.

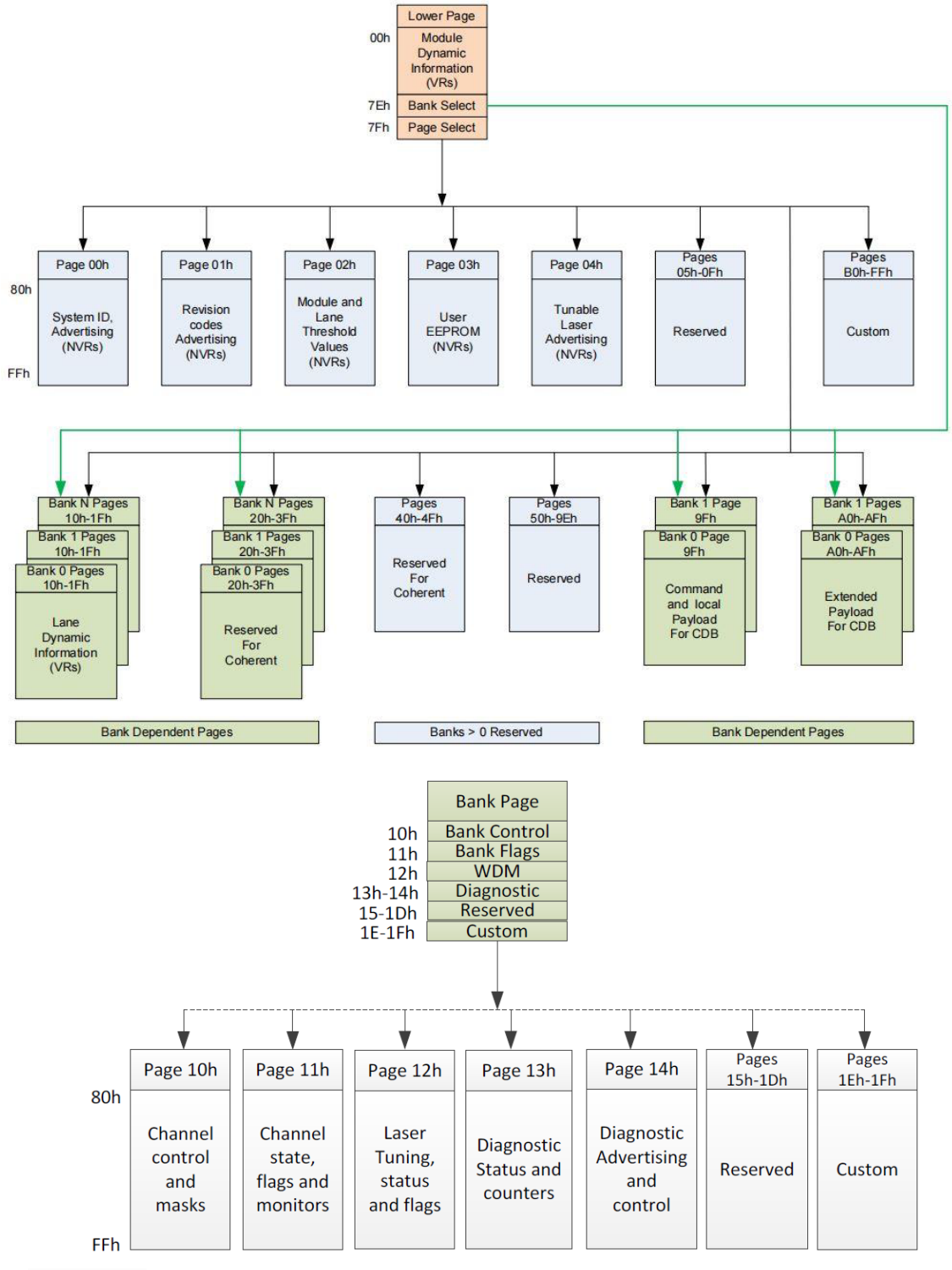
Electrical Characteristics

➢ Electrical Specifications

Parameters	Min	Typical	Max	Unit
Pre FEC Bit Error Ratio			2.4E-4	
Post FEC Bit Error Ratio			1E-12	
Transmitter (each Lane)				
Differential pk-pk Input Voltage tolerance	750			mV
Differential Termination Mismatch			10	%
Eye height	10			mV
Common-mode to differential-mode return loss	IEEE802.3ck Equation (120G-1)			dB
Vertical eye closure			12	dB
Effective return loss	7.3			dB
Transition Time	10			ps
Receiver (each Lane)				
Differential data output swing	300		900	mVpp
Differential termination mismatch			10	%
Eye height	15			mV
Vertical eye closure			12	dB
Common-mode to differential-mode return loss	IEEE802.3ck Equation (120G-1)			dB
Effective return loss	8.5			dB
Transition time	8.5			ps

User Interface

- Management Interface
- 2-Wire Serial Address: 1010000x（A0H）



CMIS Memory Map

Multiple Applications Support

The TQS-P16H8-VAZ supports CMIS 5.2 defined Application Advertising, Application Selection and Instantiation.

Address (Dec)	Application			
	AppSel Code	Name	Value (hex)	Description
85	NA	Module Type encoding	4	Optical Interfaces: AOC
86	0001b	HostInterfaceID	4B	HostInterfaceIDApp1:100GAUI-1-S C2M
87		MediaInterfaceID	3	MediaInterfaceIDApp1:BER 2.6E-4
88		HostLaneCount&MediaLaneCount	11	LaneCountApp1:TX & RX 4 lanes
89		HostLaneAssignmentOptions	F	HostLaneAssignmentOptionsApp1: lanes 1,2,3,4
01h-176		MediaLaneAssignmentOptions	F	Permissible first media lane number: lanes 1,2,3,4
90	0010b	HostInterfaceID	F	HostInterfaceIDApp2:200GAUI-4
91		MediaInterfaceID	3	MediaInterfaceIDApp2:BER 2.6E-4
92		HostLaneCount&MediaLaneCount	44	LaneCountApp2:TX & RX 4 lanes
93		HostLaneAssignmentOptions	1	Permissible first host lane number: lane 1
01h-177		MediaLaneAssignmentOptions	1	Permissible first media lane number: lane 1
94	0011b	HostInterfaceID	C	HostInterfaceIDApp3:100GAUI-4 C2M
95		MediaInterfaceID	2	MediaInterfaceIDApp3:BER 5E-5
96		HostLaneCount&MediaLaneCount	44	LaneCountApp3:TX & RX 4 lanes
97		HostLaneAssignmentOptions	1	Permissible first host lane number: lane 1
01h-178		MediaLaneAssignmentOptions	1	Permissible first media lane number: lane 1
98	0100b	HostInterfaceID	4F	HostInterfaceIDApp4:400GAUI-4-S C2M
99		MediaInterfaceID	3	MediaInterfaceIDApp4:BER 2.6E-4
100		HostLaneCount&MediaLaneCount	44	LaneCountApp4:TX & RX 4 lanes
101		HostLaneAssignmentOptions	1	HostLaneAssignmentOptionsApp4: begin lane 1
01h-179		MediaLaneAssignmentOptions	1	Permissible first media lane number: begin lane 1
102		HostInterfaceID	F	HostInterfaceIDApp5:
103		MediaInterfaceID	0	MediaInterfaceIDApp5
104		HostLaneCount&MediaLaneCount	0	LaneCountApp5
105		HostLaneAssignmentOptions	0	HostLaneAssignmentOptionsApp5

As shown in the table above，the TQS-P16H8-VAZ supports 4 applications, 400GBASE-AOC, 200GBASE-AOC , 100GBASE-AOC and 4x100GBASE-AOC

Application Selection and Instantiation

The host can select Applications by programming the AppSel value in Staged Set 0. AppSel=1 is the default Application populated in the Active Control Set at power-on or reset.
*Note that both sides of AOC need to be set to the same application.
TQS-P16H8-VAZ supports two methods of application selection and instantiation. The first method is implemented according to CMIS, and the second method is customized， which is simpler.

- **First mothod:**

The applications switching configuration sequence is as follows: read Application Descriptor Registers

and select the required Appsel. Write application configuration to DPConfigLane<i> in Stage Control Set 0, then write 1 to ApplyDPInitLane<i> to trigger Application Instantiation. The Active Set can be read from page11h.
For example, select AppDescriptor3:
Step 1: Write 0x30 in Page10h Byte145~Byte152(8 bytes)—Set AppselCode3
Step 2: Write 0xFF in Page10h Byte143—Set trigger register to run Application Instantiation.

- **Second mothod:**

Set the value of Page10h Byte240. This is a private definition.

Code Value	Bit Pattern	Host Electrical Interface	Media Interface
0	00000000b	100GAUI-1-S	4x100GBASE-AOC
1	00000001b	200GAUI-4	200GBASE-AOC
2	00000010b	100GAUI-4	100GBASE-AOC
3	00000011b	400GAUI-4-S	400GBASE-AOC

TX & RX Squelch

Default TX and RX auto-squelch is enabled. But TX and RX auto squelch disable, and force squelching function are not supported.

TX input equalization

Default TX adaptive equalization is enabled. But TX adaptive equalization disable, and fixed equalization adjust function are not supported.

RX output Equalization

RX output Equalization follows CMIS Table 6-7, with default 1dB, readable and writable

- **Rx Output Equalization code table**

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000b	0dB (No Equalization)	0dB (No Equalization)
1	0001b	1 dB	0.5 dB
2	0010b	2 dB	1.0 dB
3	0011b	3 dB	1.5 dB
4	0100b	4 dB	2.0 dB
5	0101b	5 dB	2.5 dB
6	0110b	6 dB	3.0 dB
7	0111b	7 dB	3.5 dB
8-11	1000b-1010b	Reserved	Reserved
11-15	1011b-1111b	Custom	Custom

RX output amplitude

RX output amplitude follows CMIS Table 6-8, Rx output amplitude is the difference peak-to-peak EYE high when Rx output equalization is set to 0dB. The default value of output amplitude is set to 2, with typical differential 600mVp-p

- **Rx Output Amplitude code table**

Code Value	Bit pattern	Output Amplitude
0	0000b	100-400 mV (P-P)
1	0001b	300-600 mV (P-P)
2	0010b	400-800 mV (P-P)
3	0011b	600-1200 mV (P-P)
4-14	0100b-1110b	**Reserved**
15	1111b	Custom

Loopback capabilities

Media side input loopback and Host side input loopback feature are supported, loopback control method refers to CMIS.

- **Rx Output Equalization code table**

Byte	Bits	Field Name	Field Description
13h:128	6	Simultaneous Host And Media Side loopbacks	0b: not supported
	5	Per Lane Media Side Loopbacks	1b: supported
	4	Per Lane Host Side Loopbacks	1b: supported
	3	Host Side Input Loopback	1b: supported
	2	Host Side Output Loopback	1b: supported
	1	Media Side Input Loopback	1b: supported
	0	Media Side Output Loopback	1b: supported

RX output amplitude

RX output amplitude follows CMIS Table 6-8, Rx output amplitude is the difference peak-to-peak EYE high when Rx output equalization is set to 0dB. The default value of output amplitude is set to 2, with typical differential 600mVp-p

- **Rx Output Amplitude code table**

Code Value	Bit pattern	Output Amplitude
0	0000b	100-400 mV (P-P)
1	0001b	300-600 mV (P-P)
2	0010b	400-800 mV (P-P)
3	0011b	600-1200 mV (P-P)
4-14	0100b-1110b	**Reserved**
15	1111b	Custom

Loopback capabilities

Media side input loopback and Host side input loopback feature are supported, loopback control method refers to CMIS.

- **Rx Output Equalization code table**

Byte	Bits	Field Name	Field Description
13h:128	6	Simultaneous Host And Media Side loopbacks	0b: not supported
	5	Per Lane Media Side Loopbacks	1b: supported
	4	Per Lane Host Side Loopbacks	1b: supported
	3	Host Side Input Loopback	1b: supported
	2	Host Side Output Loopback	1b: supported
	1	Media Side Input Loopback	1b: supported
	0	Media Side Output Loopback	1b: supported

Digital Diagnostic Monitor Accuracy

- The following characteristics are defined over recommended operating conditions

Parameter	Accuracy	Unit
Internally Measured AOC Temperature1	±3	℃
Internally Measured AOC Supply Voltage	±3	%
Measured Tx Bias Current	±10	%
Measured Tx Output Power2	±3	dB
Measured Rx Received Average Optical Power	±3	dB

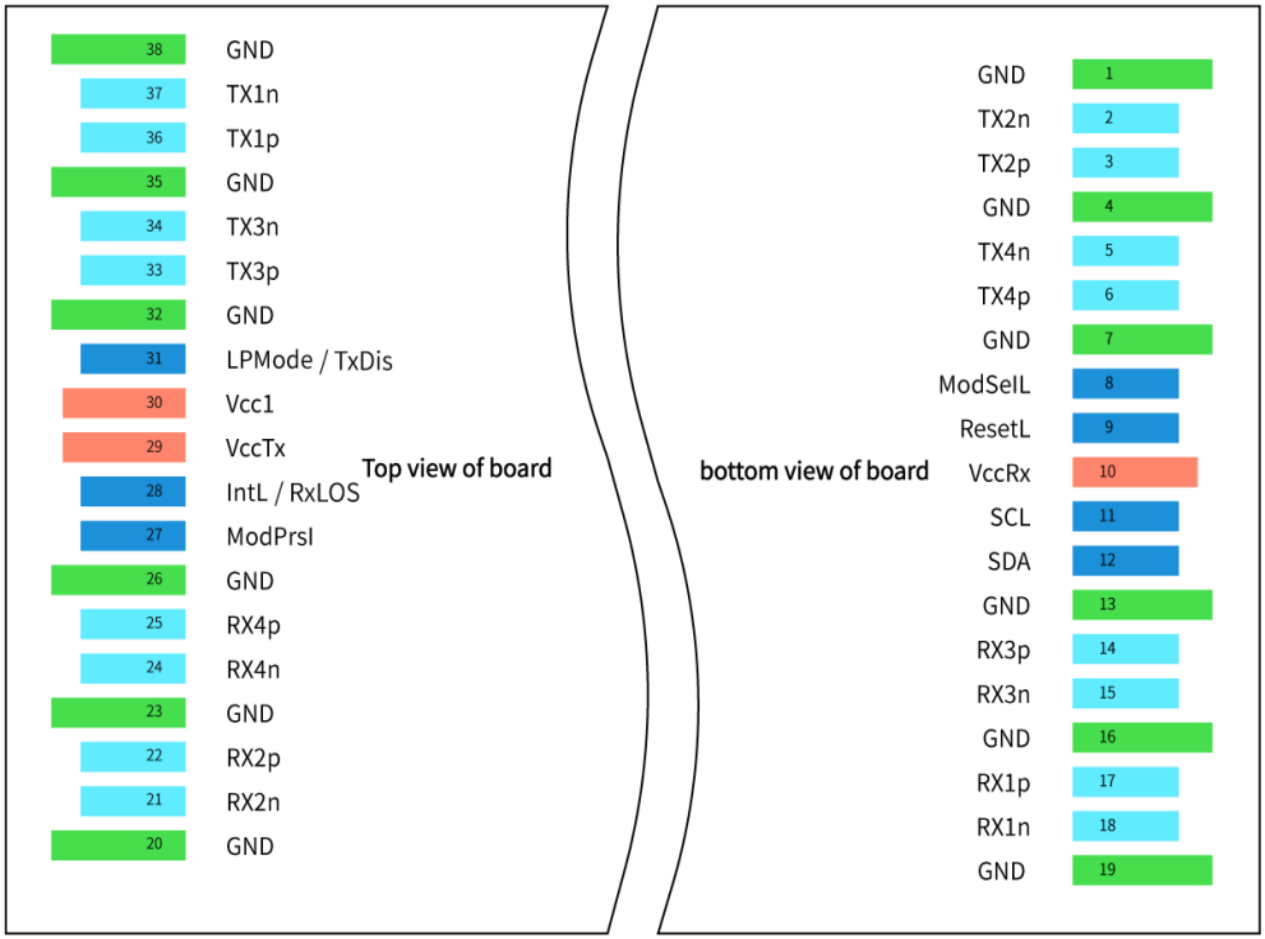
Notes:

1.Test point is the hotspot of the module.

2. DDM report stability shall be within 0.5 dB when temperature is stable. TX DDM must report -40 dBm when TX disable

Pin Assignment and Pin Description

➢ QSFP112 AOC Pad layout, and PIN Descriptions are as follows:



QSFP-DD AOC Electrical Pad Layout

➢ Pin Description

Pin	Name	Logic	Description	Power Seq	Notes
1	Ground		GND	1B	1
2	Tx2n	CML-I	Transmitter Inverted Data Input	3B	
3	Tx2p	CML-I	Transmitter Non-Inverted Data Input	3B	
4	Ground		GND	1B	1
5	Tx4n	CML-I	Transmitter Inverted Data Input	3B	
6	Tx4p	CML-I	Transmitter Non-Inverted Data Input	3B	
7	Ground		GND	1B	1
8	ModSelL	LVTTL-I	Module Select	3B	
9	ResetL	LVTTL-I	Module Reset	3B	
10	VccRx		+3.3V Power Supply Receiver	2B	2
11	SCL	LVCMOS-I/O	2-wire serial interface clock	3B	
12	SDA	LVCMOS-I/O	2-wire serial interface data	3B	
13	Ground		GND	1B	1
14	Rx3p	CML-O	Receiver Non-Inverted Data Output	3B	
15	Rx3n	CML-O	Receiver Inverted Data Output	3B	
16	Ground		GND	1B	1
17	Rx1p	CML-O	Receiver Non-Inverted Data Output	3B	
18	Rx1n	CML-O	Receiver Inverted Data Output	3B	
19	Ground		GND	1B	1
20	Ground		GND	1B	1
21	Rx2n	CML-O	Receiver Inverted Data Output	3B	
22	Rx2p	CML-O	Receiver Non-Inverted Data Output	3B	
23	Ground		GND	1B	1
24	Rx4n	CML-O	Receiver Inverted Data Output	3B	
25	Rx4p	CML-O	Receiver Non-Inverted Data Output	3B	
26	Ground		GND	1B	1

27	ModPrsL	LVTTL-O	Module Present	3B	
28	IntL	LVTTL-O	Interrupt	3B	
29	VccTx		+3.3V Power supply transmitter	2B	2
30	Vcc1		+3.3V Power supply	2B	2
31	LPMode	LVTTL-I	Low Power mode	3B	
32	Ground		GND	1B	1
33	Tx3p	CML-I	Transmitter Non-Inverted Data Input	3B	
34	Tx3n	CML-I	Transmitter Inverted Data Input	3B	
35	Ground		GND	1B	1
36	Tx1p	CML-I	Transmitter Non-Inverted Data Input	3B	
37	Tx1n	CML-I	Transmitter Inverted Data Input	3B	
38	Ground		GND	1B	1

Notes:

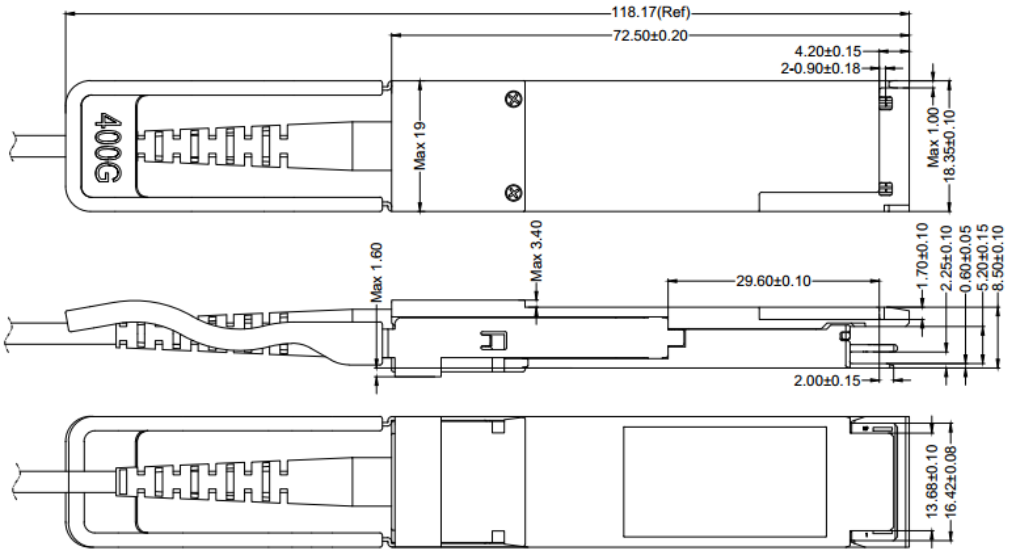
1. GND is the symbol for signal and supply (power) common for the QSFP112 module. All are common within the QSFP112 module and all voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2. Vcc Rx, Vcc1 and VccTx are the receiver and transmitter power supplies and shall be applied concurrently. VccRx, Vcc1 and VccTx may be internally connected within the QSFP112 module in any combination. The connector pins are each rated for a maximum current of 1.5A (max. current of 2.0 A is required for high module power of 15-20W)

Mechanical Dimensions

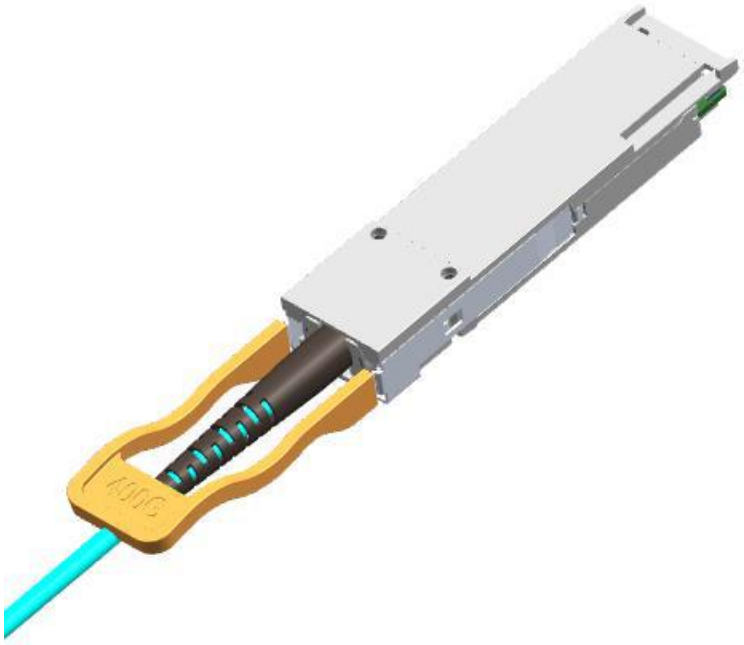
➢ Package dimensions

Below shows the package dimensions of the module. The module is designed to be complaint with QSFP112 MSA specification.



Pull-tab Color

Pull-tab color is Pantone 475U (Beige).



Contact Information

Formerica OptoElectronics Inc.
5F-11, No.38, Taiyuan St., Zhubei City,
Hsinchu County 30265, Taiwan
Tel: +886-3-5600286
Fax: +886-3-5600239

inquiry@formericaoe.com

www.formericaoe.com

Revision History

Date	Version	Description
03/12/2025	1.0	Initial release
07/11/2025	2.0	Modify the part number