User's Manual

S128 Microcontroller Group

User's Manual

Renesas Synergy™ Platform

Synergy Microcontrollers
S1 Series

The integrated module for Digital Addressable Lighting Interface (DALI) communications is designed for compliance to IEC 62386 version 2 (DALI 2) when used with suitable software and hardware.

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General Precautions

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Preface

1. About this Document

This manual describes the functions and electrical characteristics of the Renesas Synergy™ Microcontroller.

This manual is generally organized into an overview of the product, descriptions of the CPU, system control functions, peripheral functions, electrical characteristics, and usage notes. This manual describes the product specification of the microcontroller (MCU) superset. Depending on your product, some pins, registers, or functions might not exist. Address space that store unavailable registers are reserved.

2. Audience

This manual is written for system designers who are designing and programming applications using the Renesas Synergy Microcontroller. The user is expected to have basic knowledge of electrical circuits, logic circuits, and the MCU.

3. Renesas Publications

Renesas provides the following documents for the Renesas Synergy Microcontroller. Before using any of these documents, visit renesassynergy.com/docs for the most up-to-date version of the document.

Component	Document type	Description
Microcontrollers	Datasheet	Features, overview, and electrical characteristics of the MCU
	User's Manual: Microcontrollers	MCU specifications such as pin assignments, memory maps, peripheral functions, electrical characteristics, timing diagrams, and operation descriptions
	Application Notes	Technical notes, board design guidelines, and software migration information
	Technical Update (TU)	Preliminary reports on product specifications such as restriction and errata
Software	Datasheet	Functional descriptions and specific performance data for software modules that are included in Renesas Synergy Software Package (SSP)
	User's Manual: Software	API reference including SSP architecture and programming information
	Application Notes	Project files, guidelines for software programming, and application examples to develop embedded software applications
Tools & Kits, Solutions	User's Manual: Development Tools	User's manual and quick start guide for developing embedded software applications with Development Kit (DK), Starter Kit (SK), Promotion Kit (PK), Target Board Kit (TB), Product Examples (PE), and Application Examples (AE)
	User's Manual: Software	
	Quick Start Guide	
	Application Notes	Project files, guidelines for software programming, and application examples to develop embedded software applications

4. Numbering Notation

The following numbering notation is used throughout this manual:

Example	Description
011b	Binary number. For example, the binary equivalent of the number 3 is 011b.
1Fh	Hexadecimal number. For example, the hexadecimal equivalent of the number 31 is described 1Fh. In some cases, a hexadecimal number is shown with the prefix 0x, based on C/C++ formatting.
1234	Decimal number. Decimal numbers are generally shown without a suffix.

5. Typographic Notation

The following typographic notation is used throughout this manual:

Example	Description
ICU.NMICR.NMIMD	Periods separate a function module symbol (ICU), register symbol (NMICR), and bit field symbol (NMIMD)
ICU.NMICR	A period separates a function module symbol (ICU) and register symbol (NMICR)
NMICR.NMIMD	A period separates a register symbol (NMICR) and bit field symbol (NMIMD)
NFCLKSEL[1:0]	In a register bit name, the bit range enclosed in square brackets indicates the number of bits in the field at this location. In this example, NFCLKSEL[1:0] represents a 2-bit field at the specified location in the NMI Pin Interrupt Control Register (NMICR).

6. Unit Prefix

The following unit prefixes are sometimes misleading. Those unit prefixes are described throughout this manual with the following meaning:

Prefix	Description
b	Bit
B	Byte. This unit prefix is generally used for memory specification of the MCU and address space.
k	1000 = 10^3. k is also used to denote 1024 (2^{10}) but this unit prefix is used to denote 1000 (10^3) throughout this manual.
K	1024 = 2^{10}. This unit prefix is used to denote 1024 (2^{10}) not 1000 (10^3) throughout this manual.

7. Special Terms

The following terms have special meanings:

Term	Description
NC	Not connected pin. NC means the pin is not connected to the MCU.
Hi-Z	High impedance

8. Register Description

Each register description includes both a register diagram that shows the bit assignments and a register bit table that describes the content of each bit. The example of symbols used in these tables are described in the sections that follow. The following is an example of a register description and associated bit field definition.

X.X.X NMI Pin Interrupt Control Register (NMICR)

Address(es): ICU.NMICR 4000 6100h (1)

	b7	b6	b5	b4	b3	b2	b1	b0
	NFLTEN	—	NFCLKSEL[1:0]		—	—	—	NMIMD
Value after reset:	0	0	0	0	0	0	0	0

(2) (3)

(4) (5) (6)

Bit	Symbol	Bit name	Description	R/W
b0	NMIMD	NMI Detection Set	0: Falling edge 1: Rising edge.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5, b4	NFCLKSEL[1:0]	NMI Digital Filter Sampling Clock Select	b5 b4 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64.	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	NFLTEN	NMI Digital Filter Enable	0: Disable the digital filter 1: Enable the digital filter.	R/W

(1) Function module symbol, register symbol, and address assignment

Function module symbol, register symbol, and address assignment of this register are generally expressed. ICU.NMICR 4000 6100h means NMI Pin Interrupt Control Register (NMICR) of Interrupt Controller Unit (ICU) is assigned to address 4000 6100h.

(2) Bit number

This number indicates the bit number. These bits are shown in order from b31 to b0 for a 32-bit register, from b15 to b0 for a 16-bit register, and from b7 to b0 for an 8-bit register.

(3) Value after reset

This symbol or number indicates the value of each bit after a reset. The value is shown in binary unless specified otherwise.
0: Indicates that the value is 0 after a reset.
1: Indicates that the value is 1 after a reset.
x: Indicates that the value is undefined after a reset.

(4) Bit symbol

Bit symbol indicates the short name of the bit field. Reserved bit is expressed with a —.

(5) Bit name

Bit name indicates the full name of the bit field.

(6) R/W

The R/W column indicates access type: whether the bit field is read or write.
R/W: The bit field is read and write.
R/(W): The bit field is read and write. But writing to this bit field has some limitations. For details on the limitations, see the description or notes of respective registers.
R: The bit field is read-only. Writing to this bit field has no effect.
W: The bit field is write-only. The read value is undefined.

9. Abbreviations

Abbreviations used in this manual are shown in the following table:

Abbreviation	Description
AES	Advanced Encryption Standard
AHB	Advanced High-Performance Bus
AHB-AP	AHB Access Port
APB	Advanced Peripheral Bus
ARC	Alleged RC
ATB	Advanced Trace Bus
BCD	Binary Coded Decimal
BSDL	Boundary Scan Description Language
DES	Data Encryption Standard
DSA	Digital Signature Algorithm
ECC	Elliptic Curve Cryptography
ETB	Embedded Trace Buffer
ETM	Embedded Trace Macrocell
FLL	Frequency Locked Loop
FPU	Floating-Point Unit
GSM	Global System for Mobile communications
HMI	Human Machine Interface
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NVIC	Nested Vector Interrupt Controller
PC	Program Counter
PFS	Port Function Select
PLL	Phase Locked Loop
POR	Power-On Reset
PWM	Pulse Width Modulation
RSA	Rivest Shamir Adleman
SHA	Secure Hash Algorithm
S/H	Sample and Hold
SP	Stack Pointer
SWD	Serial Wire Debug
SW-DP	Serial Wire-Debug Port
TRNG	True Random Number Generator
UART	Universal Asynchronous Receiver/Transmitter

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Ultra low power 32-MHz Arm® Cortex®-M0+ core, up to 256-KB code flash memory, 24-KB SRAM, Digital Addressable Lighting Interface, Capacitive Touch Sensing Unit, 14-bit A/D Converter, 8-bit D/A Converter, security and safety features.

Features

■ Arm Cortex-M0+ Core
- Arm®v6-M architecture
- Maximum operating frequency: 32 MHz
- Arm® Memory Protection Unit (Arm MPU) with 8 regions
- Debug and Trace: DWT, BPU, CoreSight™ MTB-M0+
- CoreSight Debug Port: SW-DP

■ Memory
- Up to 256-KB code flash memory
- 4-KB data flash memory (100,000 erase/write cycles)
- Up to 24-KB SRAM
- Memory protection units
- 128-bit unique ID

■ Connectivity
- USB 2.0 Full-Speed (USBFS) module
  - On-chip transceiver with voltage regulator
  - Compliant with USB Battery Charging Specification 1.2
- Serial Communications Interface (SCI) × 3
  - UART
  - Simple IIC
  - Simple SPI
- Serial Peripheral Interface (SPI) × 2
- I^2C bus interface (IIC) × 2
- Controller Area Network (CAN) module
- Digital Addressable Lighting Interface (DALI)

■ Analog
- 14-bit A/D Converter (ADC14)
- 8-bit D/A Converter (DAC8) × 3
- High-Speed Analog Comparator (ACMPHS) × 3
- Low-Power Analog Comparator (ACMPLP) × 2
- Operational Amplifier (OPAMP) × 4
- Temperature Sensor (TSN)

■ Timers
- General PWM Timer 32-bit (GPT32)
- General PWM Timer 16-bit High Resolution (GPT16H) × 3
- General PWM Timer 16-bit (GPT16) × 3
- Low Power Asynchronous General-Purpose Timer (AGT) × 2
- Watchdog Timer (WDT)

■ Safety
- Error Correction Code (ECC) in SRAM
- SRAM parity error check
- Flash area protection
- ADC self-diagnosis function
- Clock Frequency Accuracy Measurement Circuit (CAC)
- Cyclic Redundancy Check (CRC) calculator
- Data Operation Circuit (DOC)
- Port Output Enable for GPT (POEG)
- Independent Watchdog Timer (IWDT)
- GPIO readback level detection
- Register write protection
- Main oscillator stop detection
- Illegal memory access

■ System and Power Management
- Low power modes
- Realtime clock (RTC)
- Event Link Controller (ELC)
- Data Transfer Controller (DTC)
- Key Interrupt Function (KINT)
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings

■ Security and Encryption
- AES128/256
- True Random Number Generator (TRNG)

■ Human Machine Interface (HMI)
- Capacitive Touch Sensing Unit (CTSU)

■ Multiple Clock Sources
- Main clock oscillator (MOSC)
  (1 to 20 MHz when VCC = 2.4 to 5.5 V)
  (1 to 8 MHz when VCC = 1.8 to 5.5 V)
  (1 to 4 MHz when VCC = 1.6 to 5.5 V)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO)
  (24, 32, 48, 64 MHz when VCC = 2.4 to 5.5 V)
  (24, 32, 48 MHz when VCC = 1.8 to 5.5 V)
  (24, 32 MHz when VCC = 1.6 to 5.5 V)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- IWDT-dedicated on-chip oscillator (15 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- Clock out support

■ General Purpose I/O Ports
- Up to 53 input/output pins
  - Up to 3 CMOS input
  - Up to 50 CMOS input/output
    - Up to 5V tolerant input/output
    - Up to 2 high current (20 mA)

■ Operating Voltage
- VCC: 1.6 to 5.5 V

■ Operating Temperature and Packages
- Ta = -40°C to +85°C
  - 36-pin LGA (4 mm × 4 mm, 0.5 mm pitch)
- Ta = -40°C to +105°C
  - 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)
  - 48-pin LQFP (7 mm × 7 mm, 0.5 mm pitch)
  - 32-pin LQFP (7 mm × 7 mm, 0.8 mm pitch)
  - 48-pin QFN (7 mm × 7 mm, 0.5 mm pitch)
  - 32-pin QFN (5 mm × 5 mm, 0.5 mm pitch)

1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU in this series incorporates an energy-efficient Arm Cortex®-M0+ 32-bit core that is particularly well suited for cost-sensitive and low-power applications, with the following features:

- Up to 256 KB code flash memory
- 24-KB SRAM
- Capacitive Touch Sensing Unit (CTSU)
- 14-bit A/D Converter (ADC14)
- 8-bit D/A Converter (DAC8)
- Security features.

1.1 Function Outline

Table 1.1 Arm core

Feature	Functional description
Arm Cortex-M0+ core	• Maximum operating frequency: up to 32 MHz • Arm Cortex-M0+ core: - Revision: r0p1-00rel0 - Armv6-M architecture profile - Single-cycle integer multiplier. • Arm Memory Protection Unit (Arm MPU) - Armv6 Protected Memory System Architecture - 8 protect regions. • SysTick timer - Driven by SYSTICCLK (LOCO) or ICLK.

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 256 KB of code flash memory. See section 42, Flash Memory.
Data flash memory	4 KB of data flash memory. See section 42, Flash Memory.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset. See section 6, Option-Setting Memory.
SRAM	On-chip high-speed SRAM with either parity bit or Error Correction Code (ECC). See section 41, SRAM.

Table 1.3 System (1 of 2)

Feature	Functional description
Operating mode	Two operating modes: • Single-chip mode • SCI boot mode. See section 3, Operating Modes.

Table 1.3 System (2 of 2)

Feature	Functional description
Resets	13 resets: • RES pin reset • Power-on reset • Independent watchdog timer reset • Watchdog timer reset • Voltage monitor 0 reset • Voltage monitor 1 reset • Voltage monitor 2 reset • SRAM parity error reset • SRAM ECC error reset • Bus master MPU error reset • Bus slave MPU error reset • CPU stack pointer error reset • Software reset. See section 5, Resets.
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) monitors the voltage level input to the VCC pin, and the detection level can be selected using a software program. See section 7, Low Voltage Detection (LVD).
Clock	• Main clock oscillator (MOSC) • Sub-clock oscillator (SOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • IWDT-dedicated on-chip oscillator • Clock out support. See section 8, Clock Generation Circuit.
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock to be used as a measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range. When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated. See section 9, Clock Frequency Accuracy Measurement Circuit (CAC).
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the NVIC/DTC module. The ICU also controls NMI interrupts. See section 12, Interrupt Controller Unit (ICU).
Key Interrupt Function (KINT)	A key interrupt can be generated by setting the Key Return Mode Register (KRM) and inputting a rising or falling edge to the key interrupt input pins. See section 18, Key Interrupt Function (KINT).
Low Power Mode	Power consumption can be reduced in multiple ways, such as by setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes. See section 10, Low Power Modes.
Register Write Protection	The register write protection function protects important registers from being overwritten because of software errors. See section 11, Register Write Protection.
Memory Protection Unit (MPU)	Four Memory Protection Units (MPUs) and a CPU stack pointer monitor function are provided for memory protection. See section 14, Memory Protection Unit (MPU).
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down-counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, a non-maskable interrupt or interrupt can be generated by an underflow. The refresh-permitted period can be set to refresh the counter and used as the condition for detecting when the system runs out of control. See section 24, Watchdog Timer (WDT).
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down-counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt/interrupt for a timer underflow. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail safe mechanism when the system runs out of control. The IWDT can be triggered automatically on a reset, underflow, refresh error, or by a refresh of the count value in the registers. See section 25, Independent Watchdog Timer (IWDT).

Table 1.4 Event Link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the interrupt requests generated by various peripheral modules as event signals to connect them to different modules, enabling direct interaction between the modules without CPU intervention. See section 16, Event Link Controller (ELC).

Table 1.5 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request. See section 15, Data Transfer Controller (DTC).

Table 1.6 Timers

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 32-bit timer with one channel and a 16-bit timer with six channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer. See section 20, General PWM Timer (GPT).
Port Output Enable for GPT (POEG)	Use the Port Output Enable for GPT (POEG) function to place the General PWM Timer (GPT) output pins in the output disable state. See section 19, Port Output Enable for GPT (POEG).
Low Power Asynchronous General Purpose Timer (AGT)	The Low Power Asynchronous General Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This 16-bit timer consists of a reload register and a down-counter. The reload register and the down-counter are allocated to the same address, and they can be accessed with the AGT register. See section 22, Low Power Asynchronous General Purpose Timer (AGT).
Realtime Clock (RTC)	The Realtime Clock (RTC) has two counting modes, calendar count mode and binary count mode, that are controlled by the register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar. See section 23, Realtime Clock (RTC).

Table 1.7 Communication interfaces (1 of 2)

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communication Interface (SCI) is configurable to five asynchronous and synchronous serial interfaces: • Asynchronous interfaces (UART and asynchronous communications interface adapter (ACIA)) • 8-bit clock synchronous interface • Simple IIC (master-only) • Simple SPI • Smart card interface. The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. SCI0 has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator. See section 27, Serial Communications Interface (SCI).
Digital Addressable Lighting Interface (DALI)	A Digital Addressable Lighting Interface (DALI) module is provided. DALI is an international open lighting control communication protocol that includes dimming control of electronic ballasts and LED lights from different manufacturers. The DALI interface module is designed to allow compliance with international standard IEC62386-101 Edition 1.0/2.0 (DALI 2), that includes software control. See section 28, Digital Addressable Lighting Interface (DALI).
I^2C bus interface (IIC)	The 2-channel I^2C bus interface (IIC) conforms with and provides a subset of the NXP I^2C (Inter-Integrated Circuit) bus interface functions. See section 29, I^2C Bus Interface (IIC).

Table 1.7 Communication interfaces (2 of 2)

Feature	Functional description
Serial Peripheral Interface (SPI)	Two independent Serial Peripheral Interface (SPI) channels are capable of high-speed, full-duplex synchronous serial communications with multiple processors and peripheral devices. See section 31, Serial Peripheral Interface (SPI).
Control Area Network (CAN) module	The Controller Area Network (CAN) module provides functionality to receive and transmit data using a message-based protocol between multiple slaves and masters in electromagnetically noisy applications. The CAN module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported. See section 30, Controller Area Network (CAN) Module.
USB 2.0 Full-Speed (USBFS) module	The USB 2.0 Full-Speed (USBFS) module is a USB controller that can operate as a device controller. The module supports full-speed and low-speed transfer as defined in the Universal Serial Bus Specification 2.0. The module has an internal USB transceiver and supports all of the transfer types defined in the Universal Serial Bus Specification 2.0. The USB has buffer memory for data transfer, providing a maximum of 5 pipes. Pipe 0 and pipe 4 to pipe 7 can be assigned any endpoint number based on the peripheral devices used for communication or based on the user system. The MCU supports Battery Charging Specification revision 1.2. Because the MCU can be powered at 5 V, the USB LDO regulator provides the internal USB transceiver power supply 3.3 V. See section 26, USB 2.0 Full-Speed Module (USBFS).

Table 1.8 Analog

Feature	Functional description
14-bit A/D Converter (ADC14)	A 14-bit successive approximation A/D converter is provided. Up to 21 analog input channels are selectable. Temperature sensor output and internal reference voltage are selectable for conversion. The A/D conversion accuracy is selectable from 12-bit and 14-bit conversion making it possible to optimize the tradeoff between speed and resolution in generating a digital value. See section 33, 14-Bit A/D Converter (ADC14).
8-bit D/A Converter (DAC8)	An 8-bit D/A converter (DAC8) is provided. See section 34, 8-Bit D/A Converter (DAC8).
Temperature Sensor (TSN)	The on-chip temperature sensor determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is linear. The output voltage is provided to the ADC14 for conversion and can be further used by the end application. See section 35, Temperature Sensor (TSN).
High-Speed Analog Comparator (ACMPHS)	The analog comparator compares a test voltage with a reference voltage and to provide a digital output based on the result of conversion. Both the test voltage and the reference voltage can be provided to the ACMPHS from internal sources (D/A converter output) and an external source. Such flexibility is useful in applications that require go/no-go comparisons to be performed between analog signals without necessarily requiring A/D conversion. See section 37, High-Speed Analog Comparator (ACMPHS).
Low-Power Analog Comparator (ACMPLP)	The analog comparator compares a reference input voltage and analog input voltage. The comparison result can be read by software and also be output externally. The reference input voltage can be selected from either an input to the CMPREFi (i = 0, 1) pin, an output from internal D/A converter, or from the internal reference voltage (Vref) generated internally in the MCU. The ACMPLP response speed can be set before starting an operation. Setting high-speed mode decreases the response delay time, but increases current consumption. Setting low-speed mode increases the response delay time, but decreases current consumption. See section 38, Low-Power Analog Comparator (ACMPLP).
Operational Amplifier (OPAMP)	The operational amplifier amplifies small analog input voltages and outputs the amplified voltages. A total of four differential operational amplifier units with two input pins and one output pin are provided. See section 36, Operational Amplifier (OPAMP).

Table 1.9 Human machine interfaces

Feature	Functional description
Capacitive Touch Sensing Unit (CTSU)	The Capacitive Touch Sensing Unit (CTSU) measures the electrostatic capacitance of the touch sensor. Changes in the electrostatic capacitance are determined by software, which enables the CTSU to detect whether a finger is in contact with the touch sensor. The electrode surface of the touch sensor is usually enclosed with an electrical insulator so that a finger does not come into direct contact with the electrode. See section 39, Capacitive Touch Sensing Unit (CTSU).

Table 1.10 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC) Calculator	The CRC calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC generation polynomials are available. The snoop function allows monitoring reads from and writes to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer. See section 32, Cyclic Redundancy Check (CRC) Calculator.
Data Operation Circuit (DOC)	The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. See section 40, Data Operation Circuit (DOC).

Table 1.11 Security

Feature	Functional description
AES	See section 43, AES Engine
True Random Number Generator (TRNG)	See section 44, True Random Number Generator (TRNG)

Table 1.12 I/O ports

Feature	Functional description
I/O ports	• I/O ports for the 64-pin LQFP, 64-pin QFN - I/O pins: 50 - Input pins: 3 - Pull-up resistors: 48 - N-ch open-drain outputs: 19 - 5-V tolerance: 5 • I/O ports for the 48-pin LQFP, 48-pin QFN - I/O pins: 34 - Input pins: 3 - Pull-up resistors: 32 - N-ch open-drain outputs: 14 - 5-V tolerance: 4 • I/O ports for the 36-pin LGA - I/O pins: 25 - Input pins: 3 - Pull-up resistors: 23 - N-ch open-drain outputs: 8 - 5-V tolerance: 1 • I/O ports for the 32-pin LQFP, 32-pin QFN - I/O pins: 21 - Input pins: 3 - Pull-up resistors: 19 - N-ch open-drain outputs: 8 - 5-V tolerance: 1

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset, some individual devices within the group have a subset of the features.

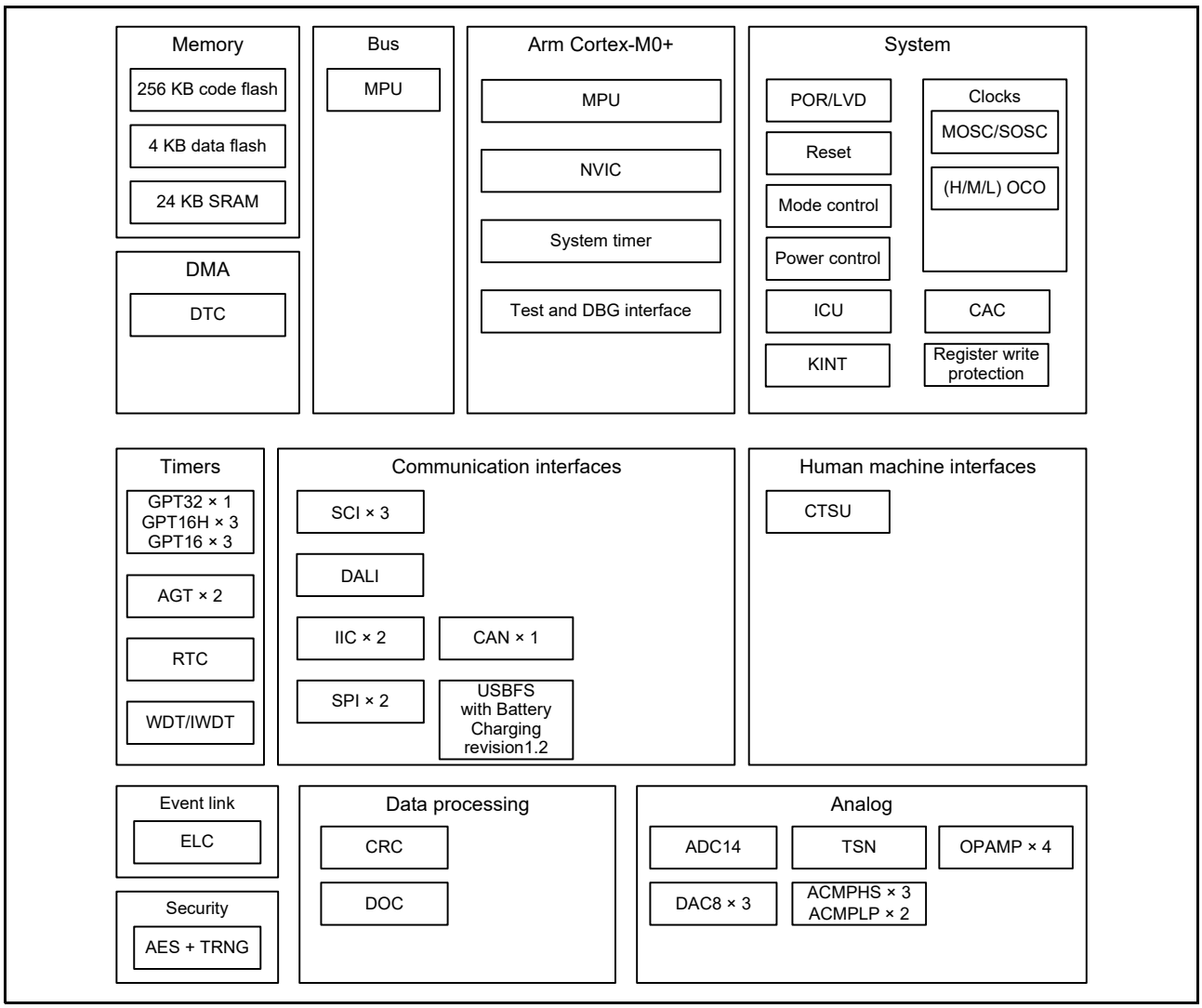


Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.13 shows a product list.

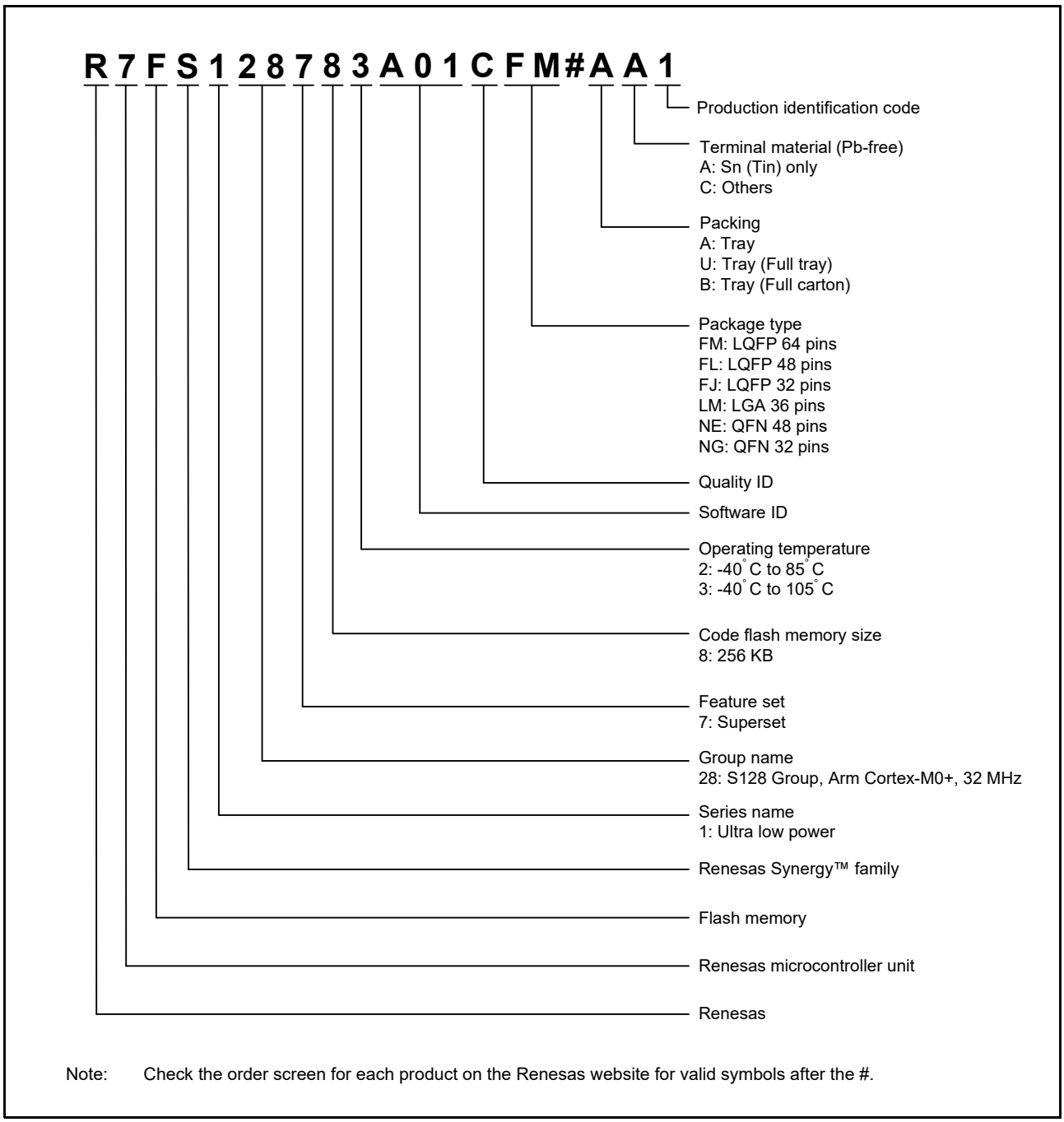


Figure 1.2 Part numbering scheme

Table 1.13 Product list

Product part number	Package code	Code flash	Data flash	SRAM	Operating temperature
R7FS128783A01CFM	PLQP0064KB-C	256 KB	4 KB	24 KB	-40 to +105°C
R7FS128783A01CFL	PLQP0048KB-B				-40 to +105°C
R7FS128783A01CNE	PWQN0048KB-A				-40 to +105°C
	PWQN0048KC-A				
R7FS128782A01CLM	PWLG0036KA-A				-40 to +85°C
R7FS128783A01CFJ	PLQP0032GB-A				-40 to +105°C
R7FS128783A01CNG	PWQN0032KB-A				-40 to +105°C
	PWQN0032KF-A				

1.4 Function Comparison

Table 1.14 Function comparison

Parts number		R7FS128783A01CFM	R7FS128783A01CFL R7FS128783A01CNE	R7FS128782A01CLM	R7FS128783A01CFJ R7FS128783A01CNG
Pin count		64	48	36	32
Package		LQFP	LQFP/QFN	LGA	LQFP/QFN
Code flash memory		256 KB			
Data flash memory		4 KB			
SRAM		24 KB			
	Parity	8 KB			
	ECC	16 KB			
System	CPU clock	32 MHz			
	ICU	Yes			
	KINT	8	5	4	4
Event control	ELC	Yes			
DMA	DTC	Yes			
Timers	GPT32	1			
	GPT16H	3	3	3	2
	GPT16	3	3	1	1
	AGT	2			
	RTC	Yes			
	WDT/IWDT	Yes			
Communication	SCI	3			
	DALI	Yes			
	IIC	2	2	1	1
	SPI	2	2	2	1
	CAN	Yes			
	USBFS	Yes			
Analog	ADC14	21	15	13	10
	DAC8	3			
	ACMPHS	3			
	ACMPLP	2			
	OPAMP	4	3	3	2
	TSN	Yes			
HMI	CTSU	28	21	12	9
Data processing	CRC	Yes			
	DOC	Yes			
Security		AES and TRNG			
I/O ports	I/O pins	50	34	25	21
	Input pins	3			
	Pull-up resistors	48	32	23	19
	N-ch open-drain outputs	19	14	8	8
	5-V tolerance	5	4	1	1

1.5 Pin Functions

Table 1.15 Pin functions (1 of 3)

Function	Signal	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1-μF capacitor. The capacitor should be placed close to the pin.
	VCL	I/O	Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCOUT	Output	
	CLKOUT	Output	Clock output pin
Operating mode control	MD	Input	Pins for setting the operating mode. The signal levels on these pins must not be changed during operation mode transition at the time of release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin
On-chip debug	SWDIO	I/O	Serial wire debug data input/output pin
	SWCLK	Input	Serial wire clock pin
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ7	Input	Maskable interrupt request pins
GPT	GTETRGA, GTETRGB	Input	External trigger input pin
	GTIOC0A to GTIOC6A, GTIOC0B to GTIOC6B	I/O	Input capture, output compare, or PWM output pin
	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W phase)
AGT	AGTEE0, AGTEE1	Input	External event input enable
	AGTIO0, AGTIO1	I/O	External event input and pulse output
	AGTO0, AGTO1	Output	Pulse output
	AGTOA0, AGTOA1	Output	Output compare match A output
	AGTOB0, AGTOB1	Output	Output compare match B output
RTC	RTCOUT	Output	Output pin for 1-Hz/64-Hz clock

Table 1.15 Pin functions (2 of 3)

Function	Signal	I/O	Description
SCI	SCK0, SCK1, SCK9	I/O	Input/output pins for the clock (clock synchronous mode)
	RXD0, RXD1, RXD9	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXD0, TXD1, TXD9	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTS0_RTS0, CTS1_RTS1, CTS9_RTS9	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low
	SCL0, SCL1, SCL9	I/O	Input/output pins for the IIC clock (simple IIC)
	SDA0, SDA1, SDA9	I/O	Input/output pins for the IIC data (simple IIC)
	SCK0, SCK1, SCK9	I/O	Input/output pins for the clock (simple SPI)
	MISO0, MISO1, MISO9	I/O	Input/output pins for slave transmission of data (simple SPI)
	MOSI0, MOSI1, MOSI9	I/O	Input/output pins for master transmission of data (simple SPI)
	SS0, SS1, SS9	Input	Chip-select input pins (simple SPI), active-low
DALI	DRX0	Input	Input pin for DALI received data
	DTX0	Output	Output pin for DALI transmitted data
IIC	SCL0, SCL1	I/O	Input/output pins for clock
	SDA0, SDA1	I/O	Input/output pins for data
SPI	RSPCKA, RSPCKB	I/O	Clock input/output pin
	MOSIA, MOSIB	I/O	Inputs or outputs data output from the master
	MISOA, MISOB	I/O	Inputs or outputs data output from the slave
	SSLA0, SSLB0	I/O	Input or output pin for slave selection
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	Output pin for slave selection
CAN	CRX0	Input	Receive data
	CTX0	Output	Transmit data
USBFS	VSS_USB	Input	Ground pins
	VCC_USB_LDO	Input	Power supply pin for USB LDO regulator
	VCC_USB	I/O	Input: Power supply pin for USB transceiver. Output: USB LDO regulator output pin. This pin should be connected to an external capacitor.
	USB_DP	I/O	D+ I/O pin of the USB on-chip transceiver. This pin should be connected to the D+ pin of the USB bus.
	USB_DM	I/O	D- I/O pin of the USB on-chip transceiver. This pin should be connected to the D- pin of the USB bus.
	USB_VBUS	Input	USB cable connection monitor pin. This pin should be connected to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USB module is operating as a device controller.
Analog power supply	AVCC0	Input	Analog block power supply pin
	AVSS0	Input	Analog block power supply ground pin
	VREFH0	Input	Reference power supply pin
	VREFL0	Input	Reference power supply ground pin

Table 1.15 Pin functions (3 of 3)

Function	Signal	I/O	Description
ADC14	AN000 to AN013, AN016 to AN022	Input	Input pins for the analog signals to be processed by the A/D converter
	ADTRG0	Input	Input pins for the external trigger signals that start the A/D conversion, active-low
DAC8	DA0 to DA2	Output	Output pins for the analog signals to be processed by the D/A converter
Comparator output	VCOUT	Output	Comparator output pin
ACMPHS	IVREF0 to IVREF2	Input	Reference voltage input pin
	IVCMP0 to IVCMP2	Input	Analog voltage input pin
ACMPLP	CMPREF0, CMPREF1	Input	Reference voltage input pins
	CMPIN0, CMPIN1	Input	Analog voltage input pins
OPAMP	AMP0+ to AMP3+	Input	Analog voltage input pins
	AMP0- to AMP3-	Input	Analog voltage input pins
	AMP0O to AMP3O	Output	Analog voltage output pins
CTSU	TS00 to TS22, TS25 to TS29	Input	Capacitive touch detection pins (touch pins)
	TSCAP	-	Secondary power supply pin for the touch driver
KINT	KR00 to KR07	Input	Key interrupt input pins
I/O ports	P000 to P004, P010 to P015	I/O	General-purpose input/output pins
	P100 to P113	I/O	General-purpose input/output pins
	P200	Input	General-purpose input pin
	P201, P204 to P206, P212, P213	I/O	General-purpose input/output pins
	P214, P215	Input	General-purpose input pins
	P300 to P304	I/O	General-purpose input/output pins
	P400 to P403, P407 to P411	I/O	General-purpose input/output pins
	P500 to P502	I/O	General-purpose input/output pins
	P914, P915	I/O	General-purpose input/output pins

1.6 Pin Assignments

Figure 1.3 to Figure 1.8 show the pin assignments.

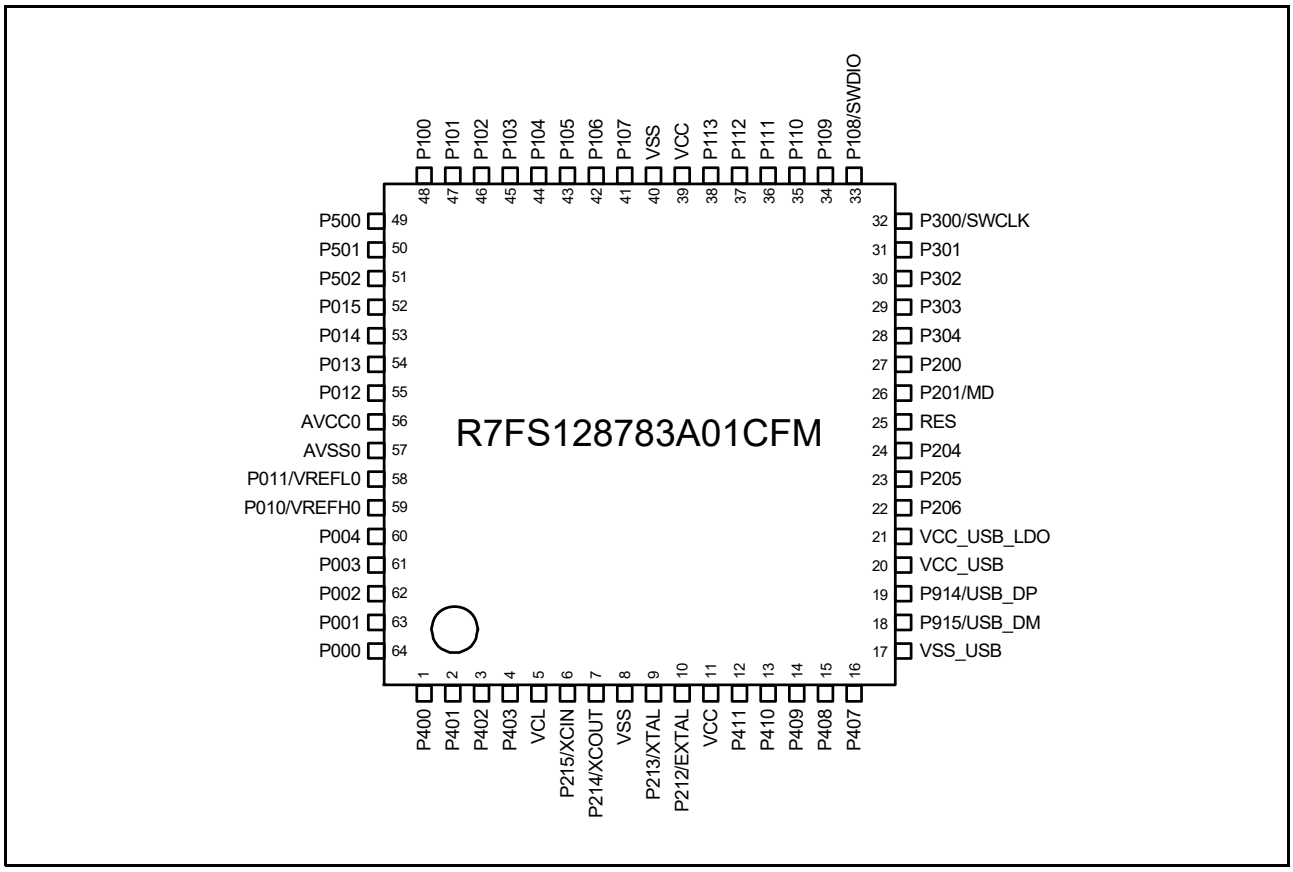


Figure 1.3 Pin assignment for LQFP 64-pin

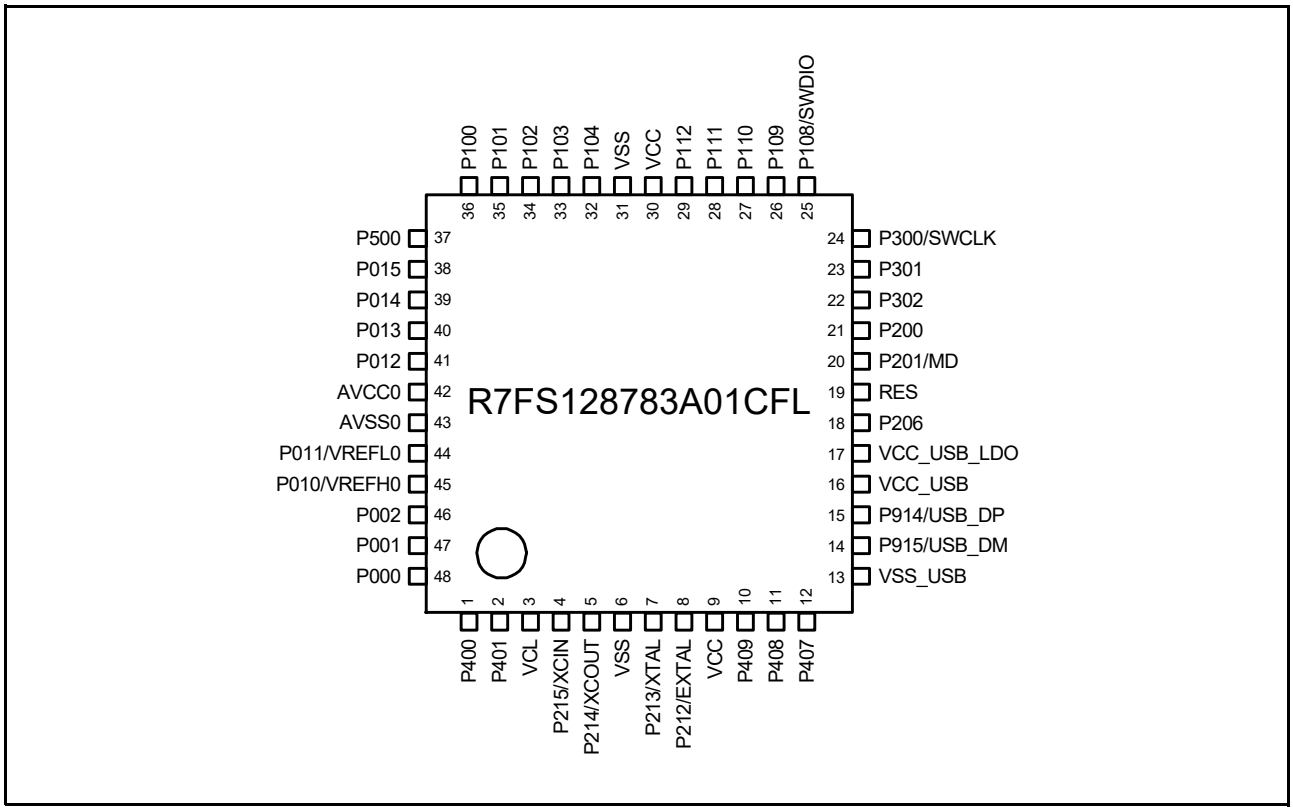
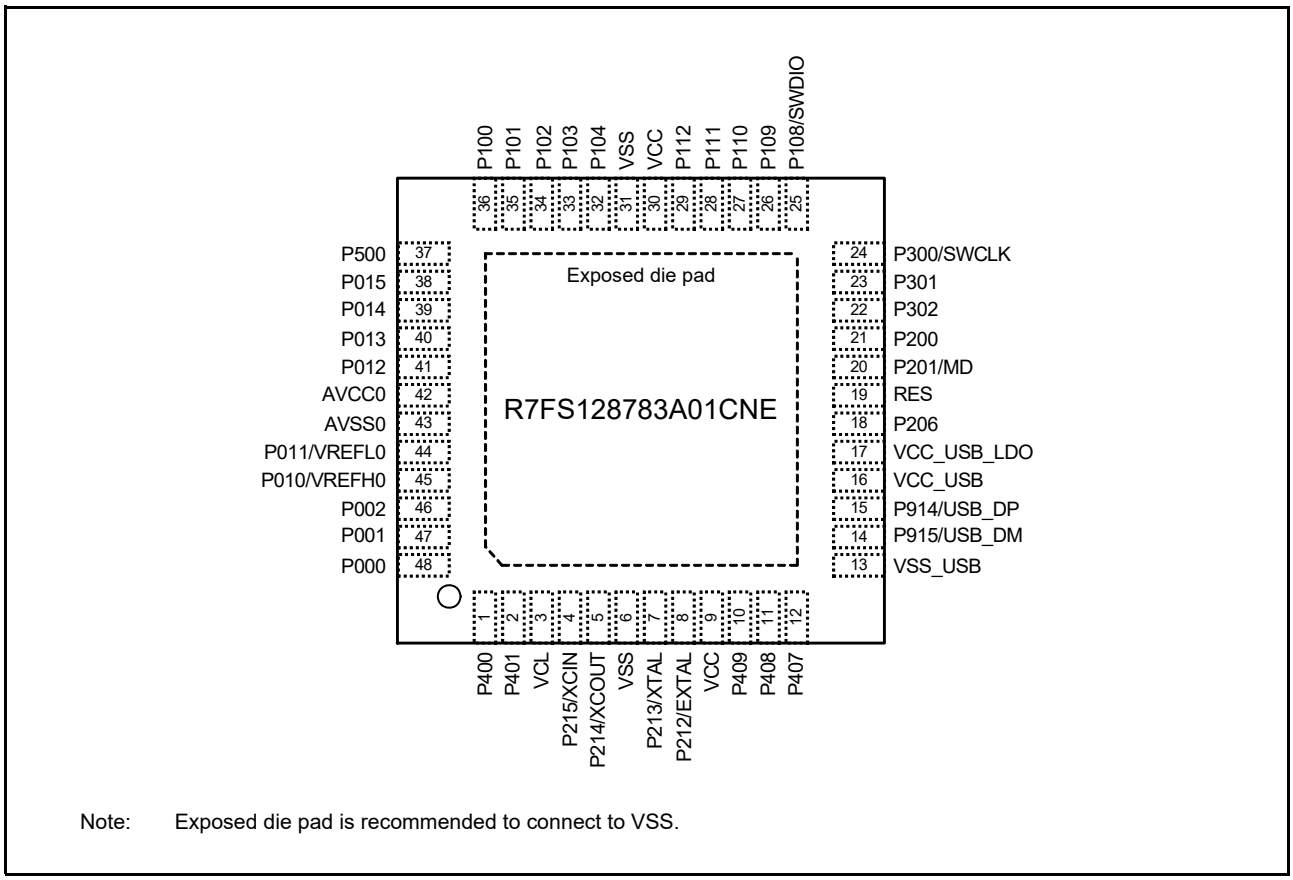


Figure 1.4 Pin assignment for LQFP 48-pin



Note: Exposed die pad is recommended to connect to VSS.

Figure 1.5 Pin assignment for QFN 48-pin

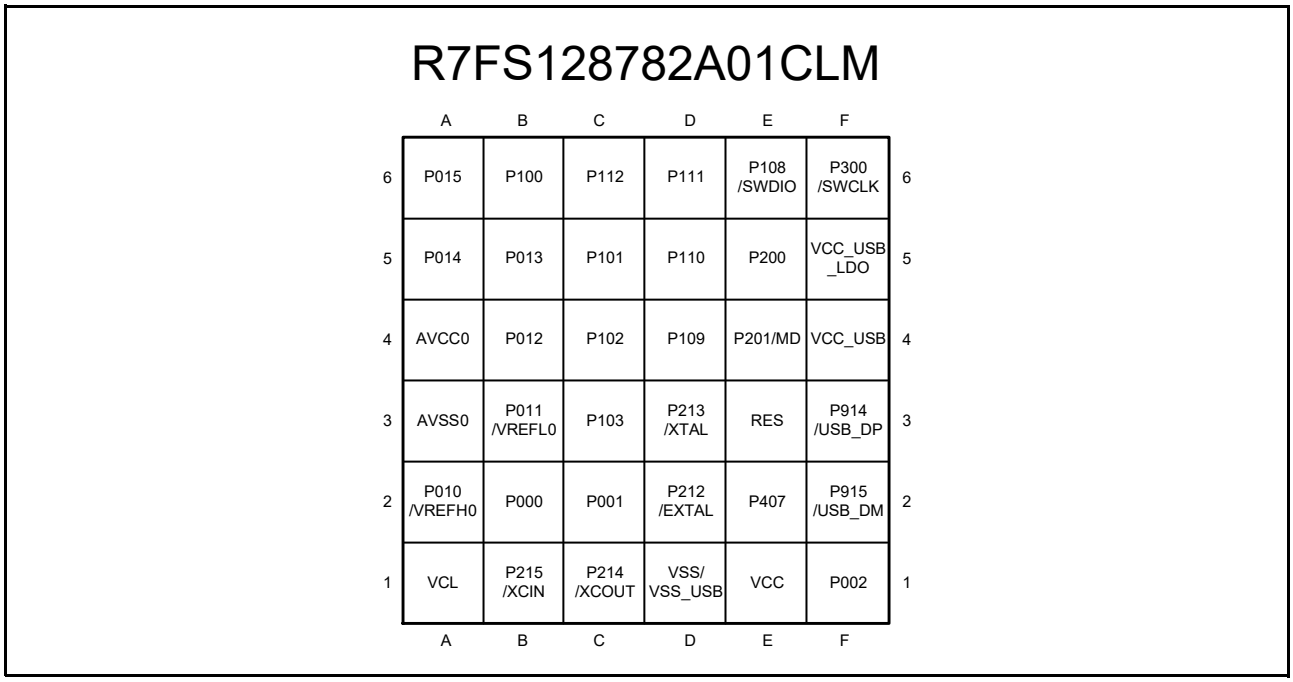


Figure 1.6 Pin assignment for LGA 36-pin (top view, pad side down)

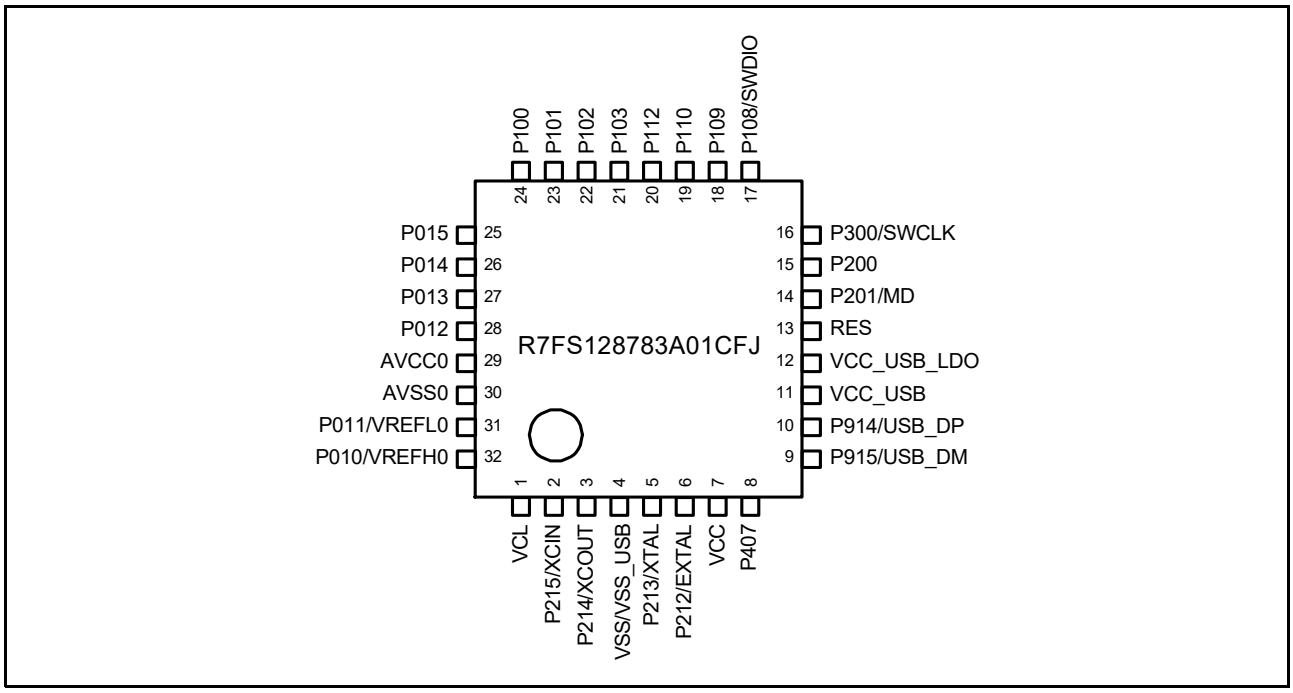
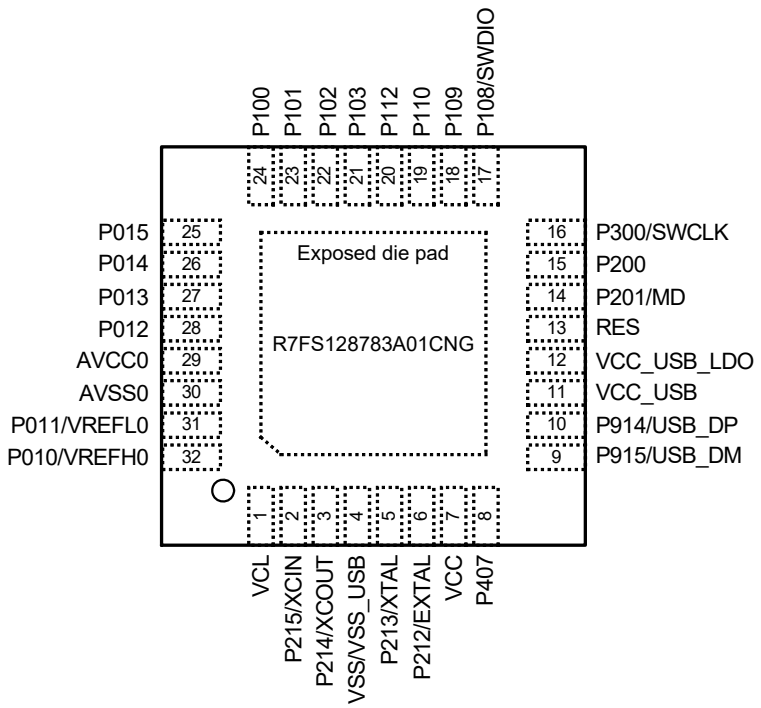


Figure 1.7 Pin assignment for LQFP 32-pin



Note: Exposed die pad is recommended to connect to VSS.

Figure 1.8 Pin assignment for QFN 32-pin

1.7 Pin Lists

Pin number								Timers				Communication Interfaces				Analogs				HMI	
LQFP64	LQFP48	QFN48	LGA36	LQFP32	QFN32	Power, System, Clock, Debug, CAC	I/O ports	AGT	GPT_OPS, POEG	GPT	RTC	USBFS,CAN, DALI	SCI	IIC	SPI	ADC14	DAC8	ACMPHS, ACMPLP	OPAMP	CTSU	Interrupt
1	1	1	-	-	-	CACREF_C	P400	AGTIO1_D		GTIOC6A_A			SCK0_B/SCK1_B	SCL0_A						TS20	IRQ0
2	2	2	-	-	-		P401		GTETRGA_B	GTIOC6B_A		CTX0_B	CTS0_RTS0_B/SS0_B/TXD1_B/MOSI1_B/SDA1_B	SDA0_A						TS19	IRQ5
3	-	-	-	-	-		P402			GTIOC3B_B		CRX0_B	RXD1_B/MISO1_B/SCL1_B							TS18	IRQ4
4	-	-	-	-	-		P403			GTIOC3A_B			CTS1_RTS1_B/SS1_B							TS17	
5	3	3	A1	1	1	VCL															
6	4	4	B1	2	2	XCIN	P215														
7	5	5	C1	3	3	XCOUT	P214														
8	6	6	D1	4	4	VSS															
9	7	7	D3	5	5	XTAL	P213		GTETRGA_D	GTIOC0A_D			TXD1_A/MOSI1_A/SDA1_A								IRQ2
10	8	8	D2	6	6	EXTAL	P212	AGTEE1	GTETRGB_D	GTIOC0B_D			RXD1_A/MISO1_A/SCL1_A								IRQ3
11	9	9	E1	7	7	VCC															
12	-	-	-	-	-		P411	AGTOA1	GTOVUP_B	GTIOC6A_B			TXD0_B/MOSI0_B/SDA0_B		MOSIA_B					TS07	IRQ4
13	-	-	-	-	-		P410	AGTOB1	GTOVLO_B	GTIOC6B_B			RXD0_B/MISO0_B/SCL0_B		MISOA_B					TS06	IRQ5
14	10	10	-	-	-		P409		GTOWUP_B	GTIOC5A_B			TXD0_E/MOSI0_E/SDA0_E/TXD9_A/MOSI9_A/SDA9_A							TS05	IRQ6
15	11	11	-	-	-		P408		GTOWLO_B	GTIOC5B_B			RXD9_A/MISO9_A/SCL9_A	SCL0_C						TS04	IRQ7
16	12	12	E2	8	8		P407	AGTIO0_C		GTIOC0A_E	RTCOUT	USB_VBUS	CTS0_RTS0_D/SS0_D	SDA0_B	SSLB3_A	ADTRG0_B				TS03	
17	13	13	D1	4	4	VSS_USB															
18	14	14	F2	9	9		P915					USB_DM									
19	15	15	F3	10	10		P914					USB_DP									
20	16	16	F4	11	11	VCC_USB															
21	17	17	F5	12	12	VCC_USB_LDO															
22	18	18	-	-	-		P206		GTIU_A				RXD0_D/MISO0_D/SCL0_D	SDA1_A	SSLB1_A					TS01	IRQ0
23	-	-	-	-	-	CLKOUT_A	P205	AGTO1	GTIV_A	GTIOC4A_B			TXD0_D/MOSI0_D/SDA0_D/CTS9_RTS9_A/SS9_A	SCL1_A	SSLB0_A					TSCAP_A	IRQ1
24	-	-	-	-	-	CACREF_A	P204	AGTIO1_A	GTIW_A	GTIOC4B_B			SCK0_D/SCK9_A	SCL0_B	RSPCKB_A					TS00	
25	19	19	E3	13	13	RES															
26	20	20	E4	14	14	MD	P201														
27	21	21	E5	15	15		P200														NMI
28	-	-	-	-	-		P304			GTIOC1A_B											
29	-	-	-	-	-		P303			GTIOC1B_B										TS02	
30	22	22	-	-	-		P302		GTOUUP_A	GTIOC4A_A					SSLB3_B					TS08	IRQ5
31	23	23	-	-	-		P301	AGTIO0_D	GTOULO_A	GTIOC4B_A			CTS9_RTS9_D/SS9_D		SSLB2_B					TS09	IRQ6
32	24	24	F6	16	16	SWCLK	P300		GTOUUP_C	GTIOC0A_A					SSLB1_B						
33	25	25	E6	17	17	SWDIO	P108		GTOULO_C	GTIOC0B_A			CTS9_RTS9_B/SS9_B		SSLB0_B						
34	26	26	D4	18	18	CLKOUT_B	P109		GTOVUP_A	GTIOC1A_A		CTX0_A	SCK1_E/TXD9_B/MOSI9_B/SDA9_B		MOSIB_B					TS10	

Pin number						Power, System, Clock, Debug, CAC	I/O ports	Timers				Communication Interfaces				Analogs				HMI	
LQFP64	LQFP48	QFN48	LGA36	LQFP32	QFN32			AGT	GPT_OPS, POEG	GPT	RTC	USBFS,CAN, DALI	SCI	IIC	SPI	ADC14	DAC8	ACMPHS, ACMPLP	OPAMP	CTSU	Interrupt
35	27	27	D5	19	19		P110		GTOVLO_A	GTIOC1B_A		CRX0_A	CTS0_RTS0_C/SS0_C/RXD9_B/MISO9_B/SCL9_B		MISOB_B			VCOUT		TS11	IRQ3
36	28	28	D6	-	-		P111	AGTOA0		GTIOC3A_A			SCK0_C/SCK9_B		RSPCKB_B					TS12	IRQ4
37	29	29	C6	20	20		P112	AGTOB0		GTIOC3B_A			TXD0_C/MOSI0_C/SDA0_C/SCK1_D		SSLB0_C					TSCAP_C	
38	-	-	-	-	-		P113			GTIOC2A_C											
39	30	30	-	-	-	VCC															
40	31	31	-	-	-	VSS															
41	-	-	-	-	-		P107			GTIOC0A_B											KR07
42	-	-	-	-	-		P106			GTIOC0B_B					SSLA3_A	AN016					KR06
43	-	-	-	-	-		P105		GTETRGA_C	GTIOC1A_C					SSLA2_A	AN017					KR05/IRQ0
44	32	32	-	-	-		P104		GTETRGB_B	GTIOC1B_C			RXD0_C/MISO0_C/SCL0_C		SSLA1_A	AN018				TS13	KR04/IRQ1
45	33	33	C3	21	21		P103		GTOWUP_A	GTIOC2A_A		CTX0_C	CTS0_RTS0_A/SS0_A		SSLA0_A	AN019		CMPREF1		TS14	KR03
46	34	34	C4	22	22		P102	AGTO0	GTOWLO_A	GTIOC2B_A		CRX0_C	SCK0_A		RSPCKA_A	AN020/ADTRG0_A		CMPIN1		TS15	KR02
47	35	35	C5	23	23		P101	AGTEE0	GTETRGB_A	GTIOC5A_A		DTX0	TXD0_A/MOSI0_A/SDA0_A/CTS1_RTS1_A/SS1_A	SDA1_B	MOSIA_A	AN021		CMPREF0		TS16	KR01/IRQ1
48	36	36	B6	24	24		P100	AGTIO0_A	GTETRGA_A	GTIOC5B_A		DRX0	RXD0_A/MISO0_A/SCL0_A/SCK1_A	SCL1_B	MISOA_A	AN022		CMPIN0		TS26	KR00/IRQ2
49	37	37	-	-	-		P500									AN013	DA1_B			TS27	
50	-	-	-	-	-		P501									AN012			AMP3+		
51	-	-	-	-	-		P502									AN011			AMP3-		
52	38	38	A6	25	25		P015									AN010	DA1_A	IVCMP1	AMP2+	TS28	IRQ7
53	39	39	A5	26	26		P014									AN009	DA0	IVREF1	AMP2-	TS29	
54	40	40	B5	27	27		P013									AN008		IVCMP0	AMP1+		
55	41	41	B4	28	28		P012									AN007		IVREF0	AMP1-		
56	42	42	A4	29	29	AVCC0															
57	43	43	A3	30	30	AVSS0															
58	44	44	B3	31	31	VREFL0	P011									AN006	DA2_A		AMP2O		
59	45	45	A2	32	32	VREFH0	P010									AN005			AMP1O		
60	-	-	-	-	-		P004									AN004	DA2_B			TS25	IRQ3
61	-	-	-	-	-		P003									AN003			AMP3O		
62	46	46	F1	-	-		P002									AN002			AMP0O		IRQ2
63	47	47	C2	-	-		P001									AN001		IVREF2	AMP0-	TS22	IRQ7
64	48	48	B2	-	-		P000									AN000		IVCMP2	AMP0+	TS21	IRQ6

Note: Several pin names have the added suffix of _A, _B, _C, _D and _E. The suffix can be ignored when assigning functionality.

2. CPU

The MCU is based on the Arm® Cortex®-M0+ core.

2.1 Overview

2.1.1 CPU

- Arm Cortex-M0+
  - Revision: r0p1-00rel0
  - ARMv6-M architecture profile
  - Single-cycle integer multiplier.
- Memory Protection Unit (MPU)
  - ARMv6 Protected Memory System Architecture
  - 8 protected regions.
- SysTick timer
  - Driven by SYSTICCLK (LOCO) or ICLK.

See reference 1. and 2. in section 2.9 for details.

2.1.2 Debug

- Arm CoreSight™ MTB-M0+
  - Revision: r0p1-00rel0
  - Buffer size: 1 KB of 8-KB MTB SRAM.
- Data Watchpoint Unit (DWT)
  - 2 comparators for watchpoints.
- Breakpoint Unit (BPU)
  - 4 instruction comparators.
- CoreSight Debug Access Port (DAP)
  - Serial Wire-Debug Port (SW-DP).
- Debug Register Module (DBGREG)
  - Reset control
  - Halt control.

See reference 1. and 2. in section 2.9 for details.

2.1.3 Operating Frequency

The operating frequencies for the MCU are as follows:

- CPU: maximum 32 MHz
- Serial Wire Debug (SWD) interface: maximum 12.5 MHz.

Figure 2.1 shows a block diagram of the Cortex-M0+ core.

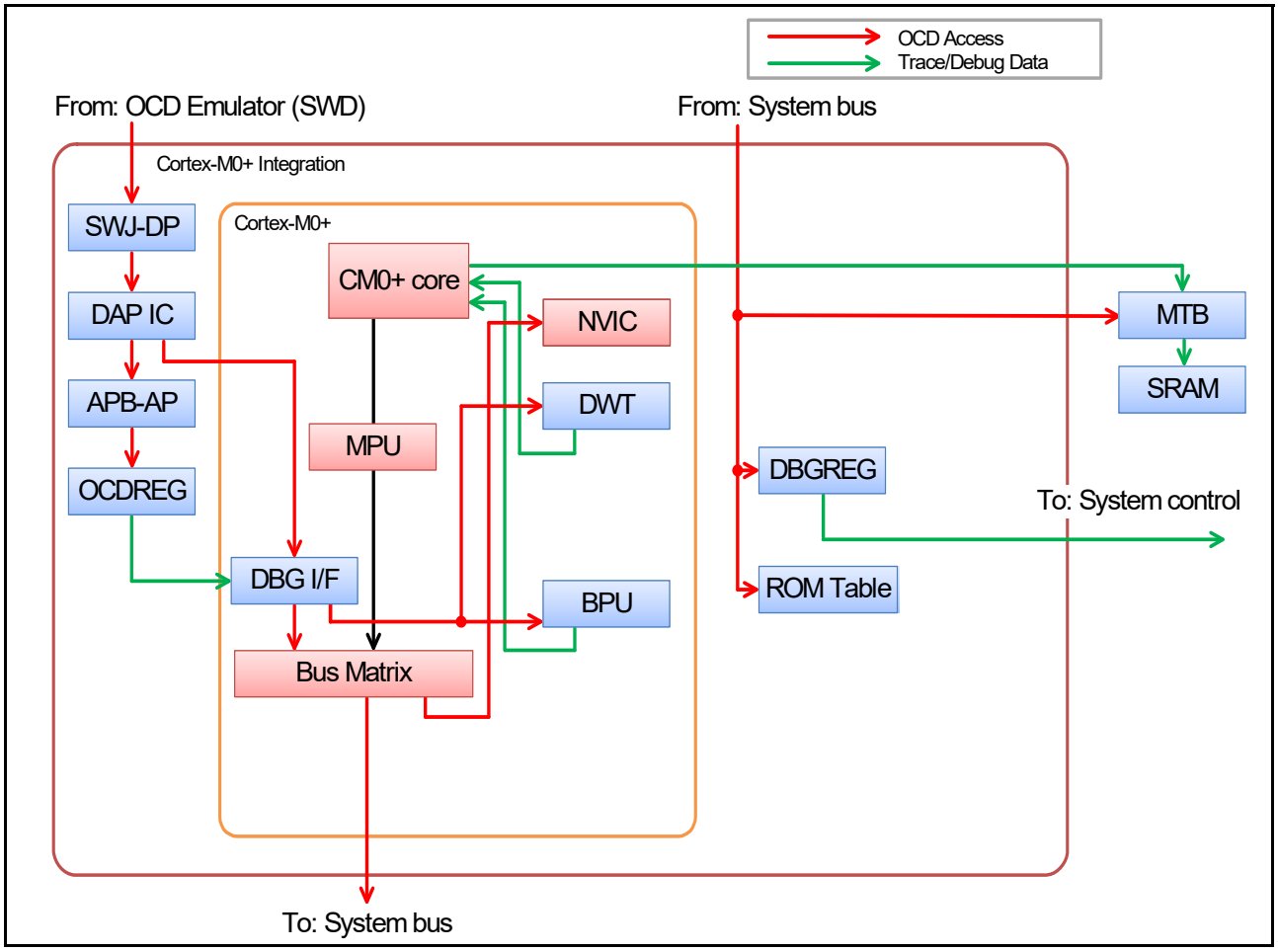


Figure 2.1 Cortex-M0+ block diagram

2.2 MCU Implementation Options

Table 2.1 shows the implementation options for the MCU and is based on the configurable options in reference 2.

Table 2.1 Implementation options (1 of 2)

Option	Implementation
Interrupts	External interrupts 32
Data endianness	Little-endian
SysTick timer	Present SYST_CALIB = 0x4000 0147 Bit[31] = 0 Reference clock provided Bit[30] = 1 TERMS value is inexact Bits[29:24] = 0x00 Reserved Bits[23:0] = 0x000147 TERM: (32768 × 10 ms) - 1 / 32.768 kHz = 326.66 decimal = 327 with skew = 0x00147
Number of watchpoint comparators	2
Number of breakpoint comparators	4
Halting debug support	Absent
Multiplier	Fast
Single-cycle I/O port	Absent

Table 2.1 Implementation options (2 of 2)

Option	Implementation
Wakeup interrupt controller	Not supported ICU can wake up CPU instead of WIC. See section 12, Interrupt Controller Unit (ICU) for details.
Vector Table Offset Register	Present
Unprivileged/Privileged support	Present
Memory Protection Unit	8 regions
Reset all registers	Absent
Instruction fetch width	Mostly 32-bit
MTB	Present
Debug Port	Serial wire
Sleep mode power-saving	Sleep mode and other low power modes are supported. See section 10, Low Power Modes for details. Note: SCB.SCR.SLEEPDEEP bit is ignored.
Memory features	No memory attribute is utilized in the MCU
Event input/output	Not implemented
System reset request output	The SYSRESETREQ bit in the Application Interrupt and Reset Control Register causes a CPU reset
Auxiliary fault inputs (AUXFAULT)	Not implemented

See reference 3. in section 2.9 for details.

2.3 Trace Interface

The MCU does not provide a dedicated trace output interface.

2.4 SWD Interface

Table 2.2 shows the SWD chip pins.

Table 2.2 SWD pins

Name	I/O	P/N	Width	Function	When not in use
SWCLK	Input	Pos.	1 bit	Serial Wire Data Clock Pin	Pull-up
SWDIO	I/O	Neg.	1 bit	Serial Wire Data I/O Pin	Pull-up

2.5 Debug Mode

2.5.1 Debug Mode Definition

In single chip mode, the debugger state of the connection is defined as OCD mode, the debugger state of the disconnection is defined as User mode. Table 2.3 shows the CPU debug modes and conditions.

Table 2.3 CPU debug mode and conditions

Conditions		Mode	
OCD connect	**SWD authentication**	**Debug mode**	**Debug authentication**
Not connected	—	User mode	Disabled
Connected	Failed	User mode	Disabled
Connected	Passed	OCD mode	Enabled

Note: OCD connect is determined by the CDBGPWRUPREQ bit output in the SWJ-DP register. The bit can only be written by the OCD. However, the level of the bit can be confirmed by reading the DBGSTR.CDBGPWRUPREQ bit.

Note: Debug Authentication is defined by the ARMv6-M architecture. Enabled means that both invasive and non-invasive CPU debugging are permitted. Disabled means that both are not permitted.

2.5.2 Debug Mode Effects

This section describes the effects of debug mode, which occur both internally and externally to the CPU.

2.5.2.1 Low power mode

All CoreSight debug components can store the register settings even when the CPU enters Software Standby mode or Snooze mode. However, AHB-AP cannot respond to On-Chip Debug (OCD) access in these low power modes. The OCD must wait for cancellation of the low power mode to access the CoreSight debug components. To request low power mode cancellation, the OCD can set the DBIRQ bit in the MCUCTRL register. For details, see section 2.6.6.3, MCU Control Register (MCUCTRL).

2.5.2.2 Reset

In OCD mode, some resets depend on the CPU status and the DBGSTOPCTR setting.

Table 2.4 Reset or interrupt and mode setting

Reset or interrupt name	Control in On-Chip Debug (OCD) mode	
	OCD break mode	OCD run mode
RES pin reset	Same as user mode	
Power-on reset	Same as user mode	
Independent watchdog timer reset or interrupt	Does not occur*1	Depends on DBGSTOPCTR setting*2
Watchdog timer reset or interrupt	Does not occur*1	Depends on DBGSTOPCTR setting*2
Voltage monitor 0 reset	Depends on DBGSTOPCTR setting*3	
Voltage monitor 1 reset or interrupt	Depends on DBGSTOPCTR setting*3	
Voltage monitor 2 reset or interrupt	Depends on DBGSTOPCTR setting*3	
SRAM parity error reset or interrupt	Depends on DBGSTOPCTR setting*3	
SRAM ECC error reset or interrupt	Depends on DBGSTOPCTR setting*3	
Bus master MPU error reset or interrupt	Same as user mode	
Bus slave MPU error reset or interrupt	Same as user mode	
CPU stack pointer error reset or interrupt	Same as user mode	
Software reset	Same as user mode	

Note: In OCD break mode, the CPU is halted. In OCD run mode, the CPU is in OCD mode and the CPU is not halted.
Note 1. The IWDT and WDT always stop in this mode.
Note 2. The IWDT and WDT operation depends on the DBGSTOPCTR setting.
Note 3. Reset or interrupt masking depends on the DBGSTOPCTR setting.

2.6 Programmers Model

2.6.1 Address Spaces

The MCU debug system has two CoreSight Access Ports (AP):

- AHB-AP, which is connected to the CPU bus matrix and has the same access to the system address space as the CPU
- APB-AP, which has a dedicated address space (OCD address space) and is connected to the OCD register.

Figure 2.2 shows the block diagram of the AP connection and address spaces.

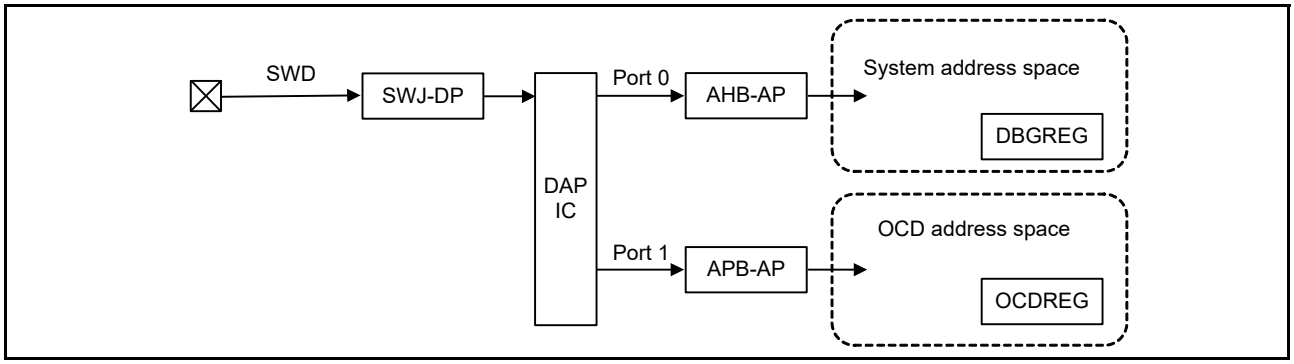


Figure 2.2 SWD authentication block diagram

For debugging purposes, there are two register modules, DBGREG and OCDREG. DBGREG is located in the system address space and can be accessed from the OCD emulator, the CPU, and other bus masters in the MCU. OCDREG is located in the OCD address space and can only be accessed from the OCD tool. The CPU and other bus masters cannot access the OCD registers.

2.6.2 Cortex-M0+ Peripheral Address Map

In the system address space, the Cortex-M0+ core has a Private Peripheral Bus (PPB) that can only be accessed from the CPU and OCD emulator. Table 2.5 shows the address map of the MCU.

Table 2.5 Cortex-M0+ peripheral address map

Component name	Start address	End address	Note
DWT	E000 1000h	E000 1FFFh	See reference 2.
BPU	E000 2000h	E000 2FFFh	See reference 2.
SCS	E000 E000h	E000 EEFFh	See reference 2.
ROM Table	E00F F000h	E00F FFFFh	See section 2.6.4, CoreSight ROM Table and reference 5.

2.6.3 External Debug Address Map

In the system address space, the Cortex-M0+ core has external debug components. These components can be accessed from the CPU and other bus masters through the system bus. Table 2.6 shows the address map of the Cortex-M0+ external debug components.

Table 2.6 External debug address map

Component name	Start address	End address	Note
MTB (SRAM area)	2000 4000h	2000 5FFFh	MTB uses 1 KB of 8 KB as trace buffer See reference 6.
MTB (SFR area)	4001 9000h	4001 9FFFh	See reference 6.
ROM Table	4001 A000h	4001 AFFFh	See reference 6.

2.6.4 CoreSight ROM Table

The MCU contains two CoreSight ROM Tables. One ROM Table is the root that contains a list of external debug components and a pointer to Arm components. The other ROM Table contains a list of Arm components.

2.6.4.1 ROM entries

Table 2.7 shows the first ROM Table that contains a pointer to the Arm system area and the user area component information. Table 2.8 shows the second ROM Table that contains Arm system area component information. See reference 5. and reference 6. for details.

Table 2.7 ROM Table 1

#	Address	Access size	R/W	Value	Target module pointer
0	4001 A000h	32 bits	R	A00E5003h	Arm® Cortex®-M0+ processor
1	4001 A004h	32 bits	R	FFFFF003h	MTB
2	4001 A008h	32 bits	R	00000000h	End of entries

Table 2.8 ROM Table 2

#	Address	Access size	R/W	Value	Target module pointer
0	E00F F000h	32 bits	R	FFF0F003h	SCS
1	E00F F004h	32 bits	R	FFF02003h	DWT
2	E00F F008h	32 bits	R	FFF03003h	BPU
3	E00F F00Ch	32 bits	R	00000000h	End of entries

2.6.4.2 CoreSight Component Registers

The CoreSight ROM Table lists the CoreSight component registers defined in the Arm CoreSight architecture. Table 2.9 shows the registers. See reference 5. for details on each register.

Table 2.9 CoreSight component registers in the CoreSight ROM Table

Name	Address	Access size	R/W	Initial value
DEVTYPE	E00F FFCCh	32 bits	R	00000001h
PID4	E00F FFD0h	32 bits	R	00000004h
PID5	E00F FFD4h	32 bits	R	00000000h
PID6	E00F FFD8h	32 bits	R	00000000h
PID7	E00F FFDCh	32 bits	R	00000000h
PID0	E00F FFE0h	32 bits	R	00000011h
PID1	E00F FFE4h	32 bits	R	00000030h
PID2	E00F FFE8h	32 bits	R	0000000Ah
PID3	E00F FFECh	32 bits	R	00000000h
CID0	E00F FFF0h	32 bits	R	0000000Dh
CID1	E00F FFF4h	32 bits	R	00000010h
CID2	E00F FFF8h	32 bits	R	00000005h
CID3	E00F FFFCh	32 bits	R	000000B1h

2.6.5 DBGREG Module

The DBGREG module controls the debug functionalities and is implemented as a CoreSight-compliant component. Table 2.10 lists the DBGREG registers other than the CoreSight component registers.

Table 2.10 Non-CoreSight DBGREG registers

Name		DAP port	Address	Access size	R/W
Debug Status Register	DBGSTR	Port 0	4001 B000h	32 bits	R
Debug Stop Control Register	DBGSTOPCTR	Port 0	4001 B010h	32 bits	R/W

2.6.5.1 Debug Status Register (DBGSTR)

Address(es): DBG.DBGSTR 4001 B000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	CDBGPWRUPACK	CDBGPWRUPREQ	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b27 to b0	—	Reserved	These bits are read as 0	R
b28	CDBGPWRUPREQ	Debug power-up request	0: OCD is not requesting debug power up 1: OCD is requesting debug power up.	R
b29	CDBGPWRUPACK	Debug power-up acknowledge	0: Debug power-up request is not acknowledged 1: Debug power-up request is acknowledged.	R
b31, b30	—	Reserved	These bits are read as 0	R

2.6.5.2 Debug Stop Control Register (DBGSTOPCR)

Address(es): DBG.DBGSTOPCR 4001 B010h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	DBGSTOP_RECCR	DBGSTOP_RPER	—	—	—	—	—	DBGSTOP_LVD[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DBGSTOP_WDT	DBGSTOP_IWDT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit	Symbol	Bit name	Description	R/W
b0	DBGSTOP_IWDT	Mask bit for IWDT reset/interrupt in the OCD run mode	In the OCD break mode, the reset/interrupt is masked and IWDT counter is stopped, regardless of this bit value. 0: Enable IWDT reset/interrupt 1: Mask IWDT reset/interrupt and stop IWDT count when CPU is in OCD break mode.	R/W
b1	DBGSTOP_WDT	Mask bit for WDT reset/interrupt in the OCD run mode	In the OCD break mode, the reset/interrupt is masked and WDT counter is stopped, regardless of this bit value. 0: Enable WDT reset/interrupt 1: Mask WDT reset/interrupt and stop WDT count when CPU is in OCD break mode.	R/W
b15 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit name	Description	R/W
b16	DBGSTOP_LVD[2:0]	Mask bit for LVD0 reset	0: Enable LVD0 reset 1: Mask LVD0 reset.	R/W
b17		Mask bit for LVD1 reset/interrupt	0: Enable LVD1 reset/interrupt 1: Mask LVD1 reset/interrupt.	R/W
b18		Mask bit for LVD2 reset/interrupt	0: Enable LVD2 reset/interrupt 1: Mask LVD2 reset/interrupt.	R/W
b23 to b19	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b24	DBGSTOP_RPER	Mask bit for SRAM parity error reset/interrupt	0: Enable SRAM parity error reset/interrupt 1: Mask SRAM parity error reset/interrupt.	R/W
b25	DBGSTOP_RECCR	Mask bit for SRAM ECC error reset/interrupt	0: Enable SRAM ECC error reset/interrupt 1: Mask SRAM ECC error reset/interrupt.	R/W
b31 to b26	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The Debug Stop Control Register (DBGSTOPCR) controls the functional stop in OCD mode. All bits in the register are regarded as 0 when the chip is not in OCD mode.

2.6.5.3 DBGREG CoreSight component registers

DBGREG provides the CoreSight component registers defined in the Arm® CoreSight™ architecture. Table 2.11 lists these registers. See reference 5. in section 2.9 for details on each register.

Table 2.11 DBGREG CoreSight component registers

Name	Address	Access size	R/W	Initial value
PID4	4001 BFD0h	32 bits	R	00000004h
PID5	4001 BFD4h	32 bits	R	00000000h
PID6	4001 BFD8h	32 bits	R	00000000h
PID7	4001 BFDCh	32 bits	R	00000000h
PID0	4001 BFE0h	32 bits	R	00000005h
PID1	4001 BFE4h	32 bits	R	00000030h
PID2	4001 BFE8h	32 bits	R	0000001Ah
PID3	4001 BFECh	32 bits	R	00000000h
CID0	4001 BFF0h	32 bits	R	0000000Dh
CID1	4001 BFF4h	32 bits	R	000000F0h
CID2	4001 BFF8h	32 bits	R	00000005h
CID3	4001 BFFCh	32 bits	R	000000B1h

2.6.6 OCDREG Module

The OCDREG module controls the On-Chip Debug (OCD) Emulator functionalities and is implemented as a CoreSight compliant component. Table 2.12 lists the OCDREG registers other than the CoreSight component registers.

Table 2.12 OCDREG registers

Name		DAP port	Address	Access size	R/W
ID Authentication Code Register 0	IAUTH0	Port 1	8000 0000h	32 bits	W
ID Authentication Code Register 1	IAUTH1	Port 1	8000 0100h	32 bits	W
ID Authentication Code Register 2	IAUTH2	Port 1	8000 0200h	32 bits	W
ID Authentication Code Register 3	IAUTH3	Port 1	8000 0300h	32 bits	W
MCU Status Register	MCUSTAT	Port 1	8000 0400h	32 bits	R
MCU Control Register	MCUCTRL	Port 1	8000 0410h	32 bits	R/W

Note: OCDREG is located in dedicated OCD address space. This address map is independent from the system address map.

2.6.6.1 ID Authentication Code Register (IAUTH0 to 3)

Four authentication registers are provided for writing the 128-bit key. These registers must be written in sequential order from IAUTH0 to IAUTH3. If the set of register writes is not compliant with this order, the result is unpredictable.

Only 32-bit writes are permitted. The initial value of the registers is all 1s. This means that SWD access is initially permitted when ID code in the OSIS register has the initial value. See section 2.8.2, Unlock ID Code.

Address(es): IAUTH0 8000 0000h

	b31																															b0
	IAUTH0: AID 31-0 bits																															
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Address(es): IAUTH1 8000 0100h

	b31																															b0
	IAUTH1: AID 63-32 bits																															
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Address(es): IAUTH2 8000 0200h

	b31																															b0
	IAUTH2: AID 95-64 bits																															
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Address(es): IAUTH3 8000 0300h

	b31																															b0
	IAUTH3: AID 127-96 bits																															
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

2.6.6.2 MCU Status Register (MCUSTAT)

Address(es): MCUSTAT 8000 0400h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	CPUSTOPCLK	CPUSLEEP	AUTH
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1/0*1	1/0*1	0

Bit	Symbol	Bit name	Description	R/W
b0	AUTH		0: Authentication failed 1: Authentication succeeded.	R
b1	CPUSLEEP		0: CPU is not in Sleep mode 1: CPU is in Sleep mode.	R
b2	CPUSTOPCLK		0: CPU clock is not stopped, indicating that the MCU is in Normal mode or Sleep mode 1: CPU clock is stopped, indicating that the MCU is in Snooze mode or Software Standby mode.	R
b31 to b3	—	Reserved	These bits are read as 0	R

Note 1. Depends on the MCU status.

2.6.6.3 MCU Control Register (MCUCTRL)

Address(es): MCUCTRL 8000 0410h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DBIRQ	—	—	—	—	—	—	—	EDBGRQ
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	EDBGRQ	External Debug Request	Writing 1 to the bit causes a CPU halt or debug monitor exception. 0: Debug event not requested 1: Debug event requested. When the EDBGRQ bit is set to 0 or the CPU is halted, the EDBCRQ bit is cleared.	R/W
b7 to b1	—	Reserved	These bits are read as 0	R
b8	DBIRQ	Debug Interrupt Request	Writing 1 to the bit wakes up the MCU from low power mode. 0: Debug interrupt not requested 1: Debug interrupt requested The condition can be cleared by writing 0 to the DBIRQ bit.	R/W
b31 to b9	—	Reserved	These bits are read as 0	R

Note: Set DBIRQ and EDBGRQ to the same value.

2.6.6.4 OCDREG CoreSight component registers

OCDREG provides the CoreSight component registers defined in the Arm CoreSight architecture. Table 2.13 lists these registers. See reference 5. in section 2.9 for details on each register.

Table 2.13 OCDREG CoreSight component registers

Name	Address	Access size	R/W	Initial value
PID4	8000 0FD0h	32 bits	Read only	00000004h
PID5	8000 0FD4h	32 bits	Read only	00000000h
PID6	8000 0FD8h	32 bits	Read only	00000000h
PID7	8000 0FDCh	32 bits	Read only	00000000h
PID0	8000 0FE0h	32 bits	Read only	00000004h
PID1	8000 0FE4h	32 bits	Read only	00000030h
PID2	8000 0FE8h	32 bits	Read only	0000000Ah
PID3	8000 0FECh	32 bits	Read only	00000000h
CID0	8000 0FF0h	32 bits	Read only	0000000Dh
CID1	8000 0FF4h	32 bits	Read only	000000F0h
CID2	8000 0FF8h	32 bits	Read only	00000005h
CID3	8000 0FFCh	32 bits	Read only	000000B1h

2.7 SysTick System Timer

The MCU has a SysTick system timer that provides a simple 24-bit down counter. The reference clock for the timer can be selected as the CPU clock (ICLK) or SysTick timer clock (SYSTICCLK).

See section 8, Clock Generation Circuit and reference 1.*1 for details.

Note 1. In the reference, SYSTICCLK (LOCO) is the IMPLEMENTATION DEFINED external reference clock, and ICLK is the processor clock.

2.8 OCD Emulator Connection

The MCU has a SWD authentication mechanism that checks access permission for debug and chip resources. To obtain full debug functionality, a pass result of the authentication mechanism is required.

Figure 2.3 shows a block diagram of the authentication mechanism.

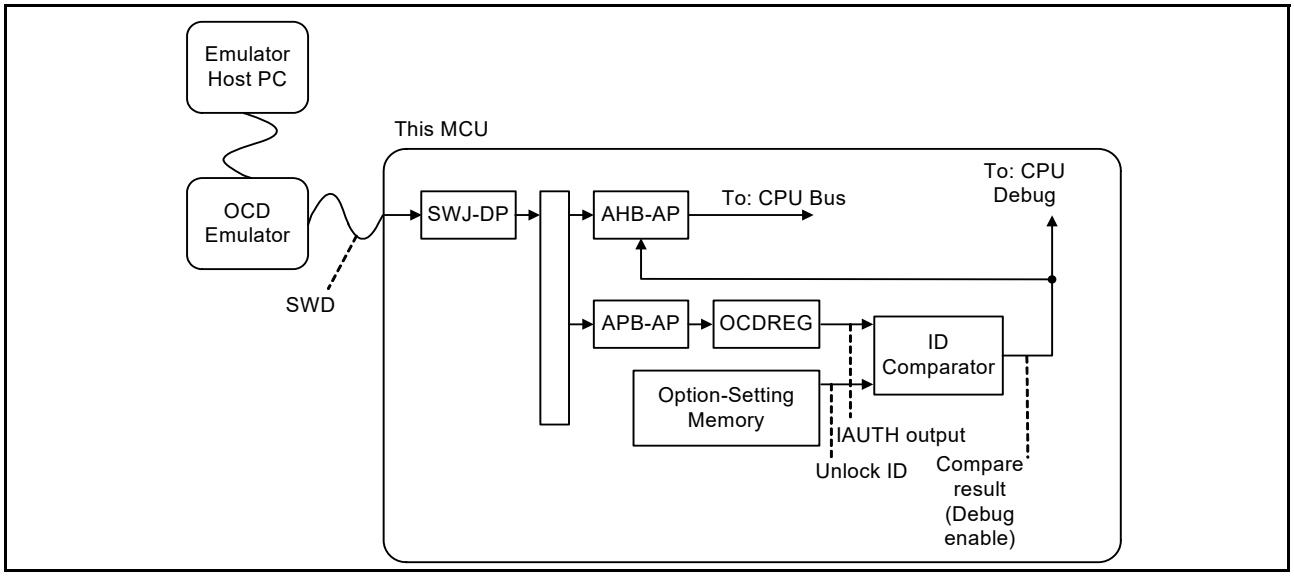


Figure 2.3 Authentication mechanism block diagram

An ID comparator is available in the MCU for authentication. The comparator compares 128-bit IAUTH output from the OCDREG and 128-bit unlock ID code from the option-setting memory. When the two outputs are identical, the CPU debug functions and system bus access from the OCD emulator are permitted.

2.8.1 DBGEN

After the OCD emulator gets access permission, the OCD emulator must set the DBGEN bit in the System Control OCD Control Register (SYOCDCR). In addition, the OCD emulator must clear the DBGEN bit before disconnecting it. See section 10, Low Power Modes for details.

2.8.2 Unlock ID Code

The unlock ID code is used for checking permissions for debug and access to on-chip resources. If the unlock ID code matches the 128-bit data written in the ID Authentication Registers 0 to 3, the SWD debugger obtains access permission. Unlock ID code is written in the OCD/Serial Programmer ID Setting Register (OSIS) in the option-setting memory. The initial value of the unlock ID code is all 1s (FFFFFFFF_FFFFFFFF_FFFFFFFF_FFFFFFFFh). See section 6, Option-Setting Memory for details.

2.8.3 Restrictions on Connecting an OCD emulator

This section describes the restrictions on emulator access.

2.8.3.1 Starting connection while in low power mode

When starting a SWD connection from an OCD emulator, the MCU must be in Normal or Sleep mode. If the MCU is in Software Standby or Snooze mode, the OCD emulator can cause the MCU to hang.

2.8.3.2 Changing low power mode while in OCD mode

When the MCU is in OCD mode, the low power mode can be changed. However, system bus access from AHB-AP is prohibited in Software Standby mode or Snooze mode. Only SWJ-DP, APB-AP, and OCDREG can be accessed from the

OCD emulator in these modes. Table 2.14 shows the restrictions.

Table 2.14 Restrictions by mode

Active mode	Start OCD emulator connection	Change low power mode	Access AHB-AP and system bus	Access APB-AP and OCDREG
Normal	Yes	Yes	Yes	Yes
Sleep	Yes	Yes	Yes	Yes
Software Standby	No	Yes	No	Yes
Snooze	No	Yes	No	Yes

If system bus access is required in Software Standby or Snooze mode, use the MCUCTRL.DBIRQ bit in OCDREG. This can wake up the MCU from the low power modes. Simultaneously, using the MCUCTRL.EDBGRQ bit in OCDREG, the OCD emulator can wake up the MCU without starting CPU execution by using a CPU break.

2.8.3.3 Modifying the unlock ID code in OSIS

After modifying the unlock ID code in the OSIS, the OCD emulator must reset the MCU by asserting the RES pin or setting the SYSRESETREQ bit of the Application Interrupt and Reset Control Register in the system control block to 1. The modified unlock ID code is reflected after reset.

2.8.3.4 Connecting sequence and SWD authentication

Because the OCD emulator is protected by the SWD authentication mechanism, OCD might be required to input the ID code to the authentication registers. The OSIS value in the option-setting memory determines whether the code is required. After negation of the reset, a 36 µs wait time is required before comparing the OSIS value at cold start.

(1) When MSB of OSIS bit [127] = 0

An emulator connection will be refused when OSIS bit [127] is set as 0 however the ALeRASE command will be accepted. When the ALeRASE command is executed, the User memory region and Option memory region are erased. The OSIS register value is also erased, so that the emulator can be connected again.

When OSIS bit [127] = 0, disabling acceptance of the ALeRASE command needs some additional settings as below.

User can select between two equivalent workarounds.

A) Setting SECMPUAC (when boot swap is set, the address of SECMPCAC shifts by 2000h.)

- Please set data as 0xFEFF at SECMPUAC
- Please set 0xFFFF_FFFC at SECMPUPCS0 and set 0xFFFF_FFFF at SECMPUPCE0.

Or

B) Setting AWSC

- Please set AWSC bit [14] = 0.

  AWSC bit [14] cannot be changed to 1 once it is set to 0. After clearing the AWSC bit, the access window and startup area selection options are permanently fixed and cannot be used again. In this case, the self-programming is prohibited because the startup area cannot be exchanged.

(2) When OSIS is all 1s (default)

OCD authentication is not required and OCD can use the AHB-AP without authentication.

1. Connect the OCD emulator to the MCU through the SWD interface.
2. Set up SWJ-DP to access the DAP bus. In the setup, the OCD emulator must assert CDBGPWRUPREQ in the SWJ-DP Control Status Register, and wait until CDBGPWRUPACK in the same register is asserted.
3. Set up AHB-AP to access the system address space. The AHB-AP is connected to the DAP bus port 0.
4. Start accessing the CPU debug resources using the AHB-AP.

(3) When OSIS[127:126] = 2'b10

OCD authentication is required and the OCD must write the unlock code to the IAUTH registers 0 to 3 in the OCDREG before using the AHB-AP.

1. Connect the OCD debugger to the MCU through the SWD interface.
2. Set up SWJ-DP to access the DAP bus. In the setup, the OCD emulator must assert CDBGPWRUPREQ in SWJ-DP Control Status Register, and wait until CDBGPWRUPACK in the same register is asserted.
3. Set up APB-AP to access OCDREG. The APB-AP is connected to the DAP bus port 1.
4. Write the 128-bit ID code to IAUTH registers 0 to 3 in the OCDREG using the APB-AP.
5. If the 128-bit ID code matches the OSIS value, the AHB-AP is authorized to issue an AHB transaction. The authorization result can be confirmed by the AUTH bit in the MCUSTAT Register or the DbgStatus bit in the AHB-AP Control Status Word Register.
   - When DbgStatus bit is 1, the 128-bit ID code is a match with the OSIS value. AHB transfers are permitted.
   - When DbgStatus bit is 0, the 128-bit ID code is not a match with the OSIS value. AHB transfers are not permitted.
6. Set up AHB-AP to access the system address space. The AHB-AP is connected to the DAP bus port 0.
7. Start accessing the CPU debug resources using the AHB-AP.

(4) When OSIS[127:126] is 2'b11

OCD authentication is required and the OCD must write the unlock ID code to IAUTH registers 0 to 3 in OCDREG. The connection sequence is the same when OSIS[127:126] is 2'b10 except for ALeRASE capability. When IATUH0-3 are ALeRASE in ASCII code, the contents of the code flash, data flash, and configuration area are erased at once. See section 42, Flash Memory for details.

ALeRASE sequence:

1. Connect the OCD debugger to the MCU through the JTAG or SWD interface.
2. Set up SWJ-DP to access DAP bus. In the setup, the OCD emulator must assert CDBGPWRUPREQ in the SWJDP Control Status Register, and then wait until CDBGPWRUPACK in the same register is asserted.
3. Set the APB-AP to access OCDREG. This APB-AP is connected to DAP bus port 1.
4. Write the 128-bit ID code to IAUTH registers 0 to 3 in the OCDREG using the APB-AP.
5. If the 128-bit ID code is ALeRASE in ASCII code (414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFFh), the contents of the code flash, data flash, and configuration area are erased. After that, the MCU transitions to Sleep mode.

2.9 References

1. *ARM®v6-M Architecture Reference Manual* (ARM DDI 0419C).
2. *ARM® Cortex®-M0+ Processor Technical Reference Manual* (ARM DDI 0484C).
3. *ARM® Cortex®-M0+ Devices Generic User Guide* (ARM DUI 0662B).
4. *ARM® CoreSight™ SoC-400 Technical Reference Manual* (ARM DDI 0480F).
5. *ARM® CoreSight™ Architecture Specification* (ARM IHI 0029D).
6. *ARM® CoreSight™ MTB-M0+ Technical Reference Manual* (ARM DDI 0486B).

3. Operating Modes

3.1 Overview

Table 3.1 shows the selection of operating modes by the mode-setting pin. For details, see section 3.2, Details on Operating Modes. Operation starts when the on-chip flash memory enabled, regardless of the mode in which operation started.

Table 3.1 Selection of operating modes by the mode-setting pin

Mode-setting pin	
MD	**Operating mode**
1	Single-chip mode
0	SCI boot mode

3.2 Details on Operating Modes

3.2.1 Single-Chip Mode

In single-chip mode, all I/O pins are available for use as input or output port, inputs or outputs for peripheral functions, or as interrupt inputs. When a reset is released while the MD pin is high, the chip starts in single-chip mode and the on-chip flash is enabled.

3.2.2 SCI Boot Mode

In this mode, the on-chip flash memory programming routine (SCI boot program), stored in a dedicated area within the MCU, is used. The on-chip flash, including the code flash memory and data flash memory, can be modified from outside the MCU by using a universal asynchronous receiver/transmitter (SCI). For details, see section 42, Flash Memory. The chip starts up in boot mode if the MD pin is held low on release from the reset state.

3.3 Operating Mode Transitions

3.3.1 Operating Mode Transitions as Determined by the Mode-Setting Pin

Figure 3.1 shows operating mode transitions determined by the settings of the MD pin.

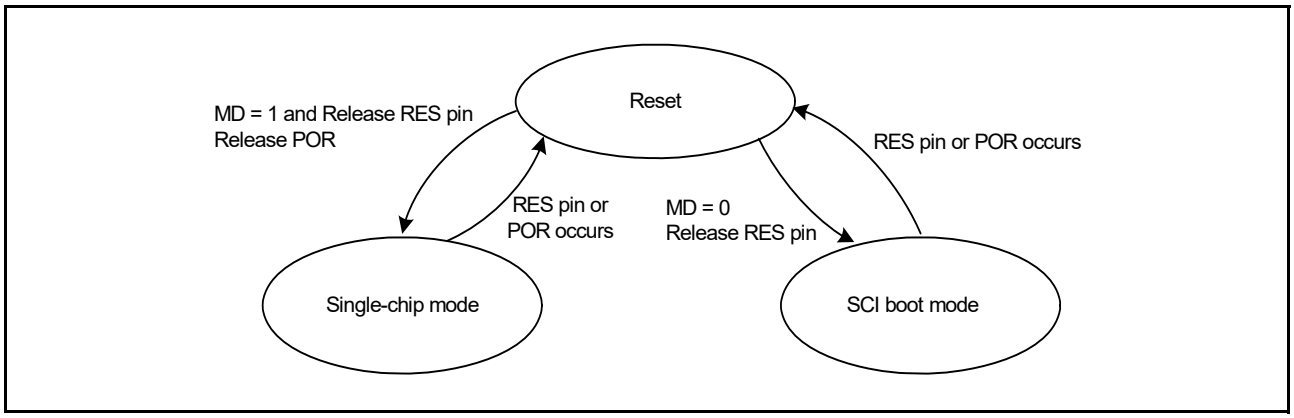
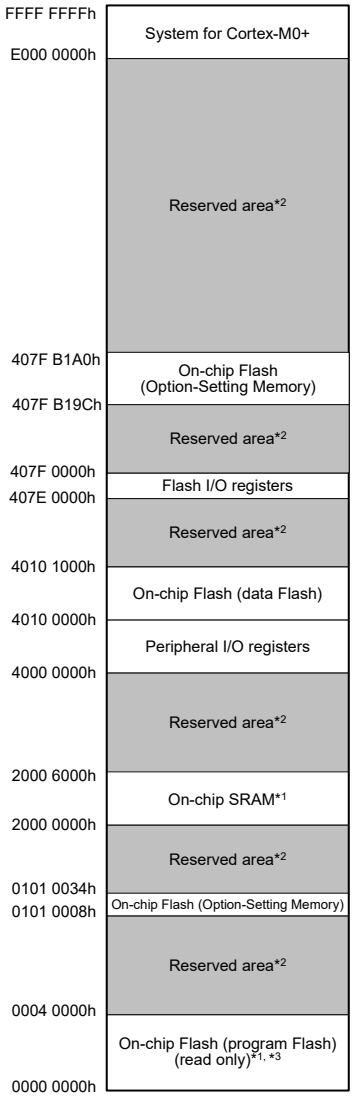


Figure 3.1 Mode-setting pin level and operating mode

4. Address Space

4.1 Overview

The MCU supports a 4-GB linear address space ranging from 0000 0000h to FFFF FFFFh that can contain both program and data. Figure 4.1 shows the memory map.



Note 1. The capacity of the flash or SRAM differs depending on the product.
Note 2. Do not access reserved areas.
Note 3. Some regions are reserved for the option-setting memory. For details on the regions, see section 6, Option-Setting Memory.

Figure 4.1 Memory map

5. Resets

5.1 Overview

The MCU has 13 types of resets:

- RES pin reset
- Power-on reset
- Independent watchdog timer reset
- Watchdog timer reset
- Voltage monitor 0 reset
- Voltage monitor 1 reset
- Voltage monitor 2 reset
- SRAM parity error reset
- SRAM ECC error reset
- Bus master MPU error reset
- Bus slave MPU error reset
- CPU stack pointer error reset
- Software reset.

Table 5.1 lists the reset names and sources.

Table 5.1 Reset names and sources

Reset name	Source
RES pin reset	Voltage input to the RES pin is driven low
Power-on reset	VCC rise (voltage detection V_{POR})*1
Independent Watchdog Timer reset	IWDT underflow or refresh error
Watchdog Timer reset	WDT underflow or refresh error
Voltage monitor 0 reset	VCC fall (voltage detection V_{det0})*1
Voltage monitor 1 reset	VCC fall (voltage detection V_{det1})*1
Voltage monitor 2 reset	VCC fall (voltage detection V_{det2})*1
SRAM parity error reset	SRAM parity error detection
SRAM ECC error reset	SRAM ECC error detection
Bus master MPU error reset	Bus master MPU error detection
Bus slave MPU error reset	Bus slave MPU error detection
CPU stack pointer error reset	CPU stack pointer error detection
Software reset	Register setting (use the Arm® software reset bit, AIRCR.SYSRESETREQ)

Note 1. For details on the voltages to be monitored (V_{POR}, V_{det0}, V_{det1}, and V_{det2}), see section 7, Low Voltage Detection (LVD), and section 46, Electrical Characteristics.

The internal state and pins are initialized by a reset. Table 5.2 and Table 5.3 list the targets initialized by resets.

Table 5.2 Reset detect flags initialized by each reset source

Flags to be initialized	Reset source				
	RES pin reset	Power-on reset	Voltage monitor 0 reset	Independent watchdog timer reset	Watchdog timer reset
Power-On Reset Detect Flag (RSTSR0.PORF)	✓	x	x	x	x
Voltage Monitor 0 Reset Detect Flag (RSTSR0.LVD0RF)	✓	✓	x	x	x
Independent Watchdog Timer Reset Detect Flag (RSTSR1.IWDTRF)	✓	✓	✓	x	x
Watchdog Timer Reset Detect Flag (RSTSR1.WDTRF)	✓	✓	✓	x	x
Voltage Monitor 1 Reset Detect Flag (RSTSR0.LVD1RF)	✓	✓	✓	x	x
Voltage Monitor 2 Reset Detect Flag (RSTSR0.LVD2RF)	✓	✓	✓	x	x
Software Reset Detect Flag (RSTSR1.SWRF)	✓	✓	✓	x	x
SRAM Parity Error Reset Detect Flag (RSTSR1.RPERF)	✓	✓	✓	x	x
SRAM ECC Error Reset Detect Flag (RSTSR1.REERF)	✓	✓	✓	x	x
Bus Slave MPU Error Reset Detect Flag (RSTSR1.BUSSRF)	✓	✓	✓	x	x
Bus Master MPU Error Reset Detect Flag (RSTSR1.BUSMRF)	✓	✓	✓	x	x
CPU Stack Pointer Error Reset Detect Flag (RSTSR1.SPERF)	✓	✓	✓	x	x
Cold Start/Warm Start Determination Flag (RSTSR2.CWSF)	x	✓	x	x	x

Flags to be initialized	Reset source				
	Voltage monitor 1 reset	Voltage monitor 2 reset	Software reset	SRAM parity error reset	SRAM ECC error reset
Power-On Reset Detect Flag (RSTSR0.PORF)	x	x	x	x	x
Voltage Monitor 0 Reset Detect Flag (RSTSR0.LVD0RF)	x	x	x	x	x
Independent Watchdog Timer Reset Detect Flag (RSTSR1.IWDTRF)	x	x	x	x	x
Watchdog Timer Reset Detect Flag (RSTSR1.WDTRF)	x	x	x	x	x
Voltage Monitor 1 Reset Detect Flag (RSTSR0.LVD1RF)	x	x	x	x	x
Voltage Monitor 2 Reset Detect Flag (RSTSR0.LVD2RF)	x	x	x	x	x
Software Reset Detect Flag (RSTSR1.SWRF)	x	x	x	x	x
SRAM Parity Error Reset Detect Flag (RSTSR1.RPERF)	x	x	x	x	x
SRAM ECC Error Reset Detect Flag (RSTSR1.REERF)	x	x	x	x	x
Bus Slave MPU Error Reset Detect Flag (RSTSR1.BUSSRF)	x	x	x	x	x
Bus Master MPU Error Reset Detect Flag (RSTSR1.BUSMRF)	x	x	x	x	x
CPU Stack Pointer Error Reset Detect Flag (RSTSR1.SPERF)	x	x	x	x	x
Cold Start/Warm Start Determination Flag (RSTSR2.CWSF)	x	x	x	x	x

Flags to be initialized	Reset source		
	Bus master MPU error reset	Bus slave MPU error reset	CPU stack pointer error reset
Power-On Reset Detect Flag (RSTSR0.PORF)	x	x	x
Voltage Monitor 0 Reset Detect Flag (RSTSR0.LVD0RF)	x	x	x
Independent Watchdog Timer Reset Detect Flag (RSTSR1.IWDTRF)	x	x	x
Watchdog Timer Reset Detect Flag (RSTSR1.WDTRF)	x	x	x
Voltage Monitor 1 Reset Detect Flag (RSTSR0.LVD1RF)	x	x	x
Voltage Monitor 2 Reset Detect Flag (RSTSR0.LVD2RF)	x	x	x
Software Reset Detect Flag (RSTSR1.SWRF)	x	x	x
SRAM Parity Error Reset Detect Flag (RSTSR1.RPERF)	x	x	x
SRAM ECC Error Reset Detect Flag (RSTSR1.REERF)	x	x	x
Bus Slave MPU Error Reset Detect Flag (RSTSR1.BUSSRF)	x	x	x
Bus Master MPU Error Reset Detect Flag (RSTSR1.BUSMRF)	x	x	x
CPU Stack Pointer Error Reset Detect Flag (RSTSR1.SPERF)	x	x	x

Flags to be initialized	Reset source		
	Bus master MPU error reset	Bus slave MPU error reset	CPU stack pointer error reset
Cold Start/Warm Start Determination Flag (RSTSR2.CWSF)	x	x	x

✓: Initialized to 0
x: Not initialized

Table 5.3 Module-related registers initialized by each reset source

Registers to be initialized		Reset source						
		RES pin reset	Power-on reset	Voltage monitor 0 reset	Independent watchdog timer reset	Watchdog timer reset	Voltage monitor 1 reset	Voltage monitor 2 reset
Registers related to the watchdog timer	WDTRR, WDTCR, WDTSR, WDTRCR, WDTCSTPR	✓	✓	✓	✓	✓	✓	✓
Registers related to the voltage monitor function 1	LVD1CR0, LVCMPCR.LVD1E, LVDLVLR.LVD1LVL	✓	✓	✓	✓	✓	x	x
	LVD1CR1/LVD1SR	✓	✓	✓	✓	✓	x	x
Registers related to the voltage monitor function 2	LVD2CR0, LVCMPCR.LVD2E, LVDLVLR.LVD2LVL	✓	✓	✓	✓	✓	x	x
	LVD2CR1/LVD2SR	✓	✓	✓	✓	✓	x	x
Register related to the SOSC	SOSCCR	x	✓	x	x	x	x	x
	SOMCR	x	✓	x	x	x	x	x
Register related to the LOCO	LOCOCR	✓	✓	✓	✓	✓	✓	✓
	LOCOUTCR	x	✓	✓	x	x	✓	✓
Register related to the MOSC	MOMCR	✓	✓	✓	✓	✓	✓	✓
Register related to the realtime clock*1		x	x	x	x	x	x	x
Register related to the AGT		x	✓	✓	x	x	✓	✓
Register related to the MPU		✓	✓	✓	✓	✓	✓	✓
Pin state (except XCIN/XCOUT pin)		✓	✓	✓	✓	✓	✓	✓
Pin state (XCIN/XCOUT pin)		x	✓	x	x	x	x	x
Registers other than the above, CPU, and internal state		✓	✓	✓	✓	✓	✓	✓

Registers to be initialized		Reset source					
		Software reset	SRAM parity error reset	SRAM ECC error reset	Bus master MPU error reset	Bus slave MPU error reset	CPU stack pointer error reset
Registers related to the watchdog timer	WDTRR, WDTCR, WDTSR, WDTRCR, WDTCSTPR	✓	✓	✓	✓	✓	✓
Registers related to the voltage monitor function 1	LVD1CR0, LVCMPCR.LVD1E, LVDLVLR.LVD1LVL	x	x	x	x	x	x
	LVD1CR1/LVD1SR	x	x	x	x	x	x
Registers related to the voltage monitor function 2	LVD2CR0, LVCMPCR.LVD2E, LVDLVLR.LVD2LVL	x	x	x	x	x	x
	LVD2CR1/LVD2SR	x	x	x	x	x	x
Register related to the SOSC	SOSCCR	x	x	x	x	x	x
	SOMCR	x	x	x	x	x	x
Register related to the LOCO	LOCOCR	✓	✓	✓	✓	✓	✓
	LOCOUTCR	x	x	x	x	x	x
Register related to the MOSC	MOMCR	✓	✓	✓	✓	✓	✓
Register related to the realtime clock*1		x	x	x	x	x	x
Register related to the AGT		x	x	x	x	x	x
Register related to the MPU		✓	✓	✓	x	x	x
Pin state (except XCIN/XCOUT pin)		✓	✓	✓	✓	✓	✓
Pin state (XCIN/XCOUT pin)		x	x	x	x	x	x
Registers other than the above, CPU, and internal state		✓	✓	✓	✓	✓	✓

✓: Initialized, x: Not initialized

Note 1. The RTC has a software reset. RCR1.RTCOS, RCR1.CIE, RCR2.RTCOE, RCR2.ADJ30, and RCR2.RESET are initialized by all types of resets. For details on the target bits, see section 23, Realtime Clock (RTC).

The RTC is not initialized by any reset source. SOSC and LOCO can be selected as the clock sources of RTC. Table 5.4 and Table 5.5 show the states of SOSC and LOCO when a reset occurs.

Table 5.4 States of SOSC when a reset occurs

		Reset source	
		POR	**Other**
SOSC	Enable or disable	Initialized to disable	Continue with the state that was selected before the reset occurred
	Drive capability	Initialized to Normal mode	Continue with the state that was selected before the reset occurred
	XCIN/XCOUT	Initialized to general-purpose input pins	Continue with the state that was selected before the reset occurred

Table 5.5 States of LOCO when a reset occurs

		Reset source	
		POR/LVD0/LVD1/LVD2	**Other**
LOCO	Enable or disable	Initialized to enable	
	Oscillation accuracy*1	Initialized to accuracy before trimming by Power-on (accuracy: +/- 15%)	Continue the accuracy that was trimmed by LOCOUTCR

Note 1. The LOCO User Trimming Control Register (LOCOUTCR) is reset by POR, LVD0, LVD1, and LVD2 resets, returning the LOCO to the default oscillation accuracy. This can affect RTC accuracy if the RTC uses the LOCO (with a user trimming value in LOCOUTCR) as the RTC source clock. To restore the pre-reset LOCO oscillation accuracy, reload the required trimming value into LOCOUTCR after any of these resets.

When a reset is canceled, reset exception handling starts.

Table 5.6 lists the pin related to the reset function.

Table 5.6 Pin related to reset

Pin name	I/O	Function
RES	Input	Reset pin

5.2 Register Descriptions

5.2.1 Reset Status Register 0 (RSTSR0)

Address(es): SYSTEM.RSTSR0 4001 E410h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	LVD2RF	LVD1RF	LVD0RF	PORF
Value after reset:	0	0	0	0	x*1	x*1	x*1	x*1

Bit	Symbol	Bit name	Description	R/W
b0	PORF	Power-On Reset Detect Flag	0: Power-on reset not detected 1: Power-on reset detected.	R(/W)*2
b1	LVD0RF	Voltage Monitor 0 Reset Detect Flag	0: Voltage monitor 0 reset not detected 1: Voltage monitor 0 reset detected.	R(/W)*2
b2	LVD1RF	Voltage Monitor 1 Reset Detect Flag	0: Voltage monitor 1 reset not detected 1: Voltage monitor 1 reset detected.	R(/W)*2
b3	LVD2RF	Voltage Monitor 2 Reset Detect Flag	0: Voltage monitor 2 reset not detected 1: Voltage monitor 2 reset detected.	R(/W)*2
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The value after reset depends on the reset source.

Note 2. Only 0 can be written to clear the flag. The flag must be cleared by writing 0 after 1 is read.

PORF flag (Power-On Reset Detect Flag)

The PORF flag indicates that a power-on reset occurred.

[Setting condition]

- When a power-on reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read and then 0 is written to PORF.

LVD0RF flag (Voltage Monitor 0 Reset Detect Flag)

The LVD0RF flag indicates that VCC voltage fell below V_{det0}.

[Setting condition]

- When a voltage monitor 0 reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read and then 0 is written to LVD0RF.

LVD1RF flag (Voltage Monitor 1 Reset Detect Flag)

The LVD1RF flag indicates that VCC voltage fell below V_{det1}.

[Setting condition]

- When a voltage monitor 1 reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read and then 0 is written to LVD1RF.

LVD2RF flag (Voltage Monitor 2 Reset Detect Flag)

The LVD2RF flag indicates that VCC voltage fell below V_{det2}.

[Setting condition]

- When a voltage monitor 2 reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read then and 0 is written to LVD2RF.

5.2.2 Reset Status Register 1 (RSTSR1)

Address(es): SYSTEM.RSTSR1 4001 E0C0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SPERF	BUSMRF	BUSSRF	REERF	RPERF	—	—	—	—	—	SWRF	WDTRF	IWDTRF
Value after reset:	0	0	0	x*1	x*1	x*1	x*1	x*1	0	0	0	0	0	x*1	x*1	x*1

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	IWDTRF	Independent Watchdog Timer Reset Detect Flag	0: Independent Watchdog Timer reset not detected 1: Independent Watchdog Timer reset detected.	R(/W) *2
b1	WDTRF	Watchdog Timer Reset Detect Flag	0: Watchdog Timer reset not detected 1: Watchdog Timer reset detected.	R(/W) *2
b2	SWRF	Software Reset Detect Flag	0: Software reset not detected 1: Software reset detected.	R(/W) *2
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	RPERF	SRAM Parity Error Reset Detect Flag	0: SRAM parity error reset not detected 1: SRAM parity error reset detected.	R(/W) *2
b9	REERF	SRAM ECC Error Reset Detect Flag	0: SRAM ECC error reset not detected 1: SRAM ECC error reset detected.	R(/W) *2
b10	BUSSRF	Bus Slave MPU Error Reset Detect Flag	0: Bus slave MPU error reset not detected 1: Bus slave MPU error reset detected.	R(/W) *2
b11	BUSMRF	Bus Master MPU Error Reset Detect Flag	0: Bus master MPU error reset not detected 1: Bus master MPU error reset detected.	R(/W) *2
b12	SPERF	CPU Stack Pointer Error Reset Detect Flag	0: CPU stack pointer error reset not detected 1: CPU stack pointer error reset detected.	R(/W) *2
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The value after reset depends on the reset source.
Note 2. Only 0 can be written to clear the flag. The flag must be cleared by writing 0 after 1 is read.

IWDTRF flag (Independent Watchdog Timer Reset Detect Flag)

The IWDTRF flag indicates that an independent watchdog timer reset occurred.

[Setting condition]

- When an independent watchdog timer reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read and then 0 is written to IWDTRF.

WDTRF flag (Watchdog Timer Reset Detect Flag)

The WDTRF flag indicates that a watchdog timer reset occurred.

[Setting condition]

- When a watchdog timer reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read and then 0 is written to WDTRF.

SWRF flag (Software Reset Detect Flag)

The SWRF flag indicates that a software reset occurred.

[Setting condition]

- When a software reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read and then 0 is written to SWRF.

RPERF flag (SRAM Parity Error Reset Detect Flag)

The RPERF flag indicates that a SRAM parity error reset occurred.

[Setting condition]

- When a SRAM parity error reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read as 1 and then 0 is written to RPERF.

REERF flag (SRAM ECC Error Reset Detect Flag)

The REERF flag indicates that a SRAM ECC error reset occurred.

[Setting condition]

- When a SRAM ECC error reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read and then 0 is written to REERF.

BUSSRF flag (Bus Slave MPU Error Reset Detect Flag)

The BUSSRF flag indicates that a bus slave MPU error reset occurs.

[Setting condition]

- When a bus slave MPU error reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read and then 0 is written to BUSSRF.

BUSMRF flag (Bus Master MPU Error Reset Detect Flag)

The BUSMRF flag indicates that a bus master MPU error reset occurs.

[Setting condition]

- When a bus master MPU error reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read and then 0 is written to BUSMRF.

SPERF flag (CPU Stack Pointer Error Reset Detect Flag)

The SPERF flag indicates that a stack pointer error reset occurs.

[Setting condition]

- When a stack pointer error reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read and then 0 is written to SPERF.

5.2.3 Reset Status Register 2 (RSTSR2)

Address(es): SYSTEM.RSTSR2 4001 E411h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CWSF
Value after reset:	0	0	0	0	0	0	0	x*1

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	CWSF	Cold/Warm Start Determination Flag	0: Cold start 1: Warm start.	R(/W) *2
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The value after reset depends on the reset source.
Note 2. Only 1 can be written to set the flag.

RSTSR2 determines whether a power-on reset caused the reset processing (cold start) or a reset signal input during operation caused the reset processing (warm start).

CWSF flag (Cold/Warm Start Determination Flag)

The CWSF flag indicates the type of reset processing, either cold start or warm start. The CWSF flag is initialized by a power-on reset. It is not initialized by a reset signal generated by the RES pin.

[Setting condition]

- When 1 is written by software. Writing 0 to CWSF does not set it to 0.

[Clearing condition]

- When a reset listed in Table 5.2 occurs.

5.3 Operation

5.3.1 RES Pin Reset

The RES pin generates this reset. When the RES pin is driven low, all the processing in progress is aborted and the MCU enters a reset state. To successfully reset the MCU, the RES pin must be held low for the specified power supply stabilization time at power-on.

When the RES pin is driven high from low, the internal reset is canceled after the post-RES cancellation wait time (tRESWT) elapses, and the CPU starts the reset exception handling.

For details, see section 46, Electrical Characteristics.

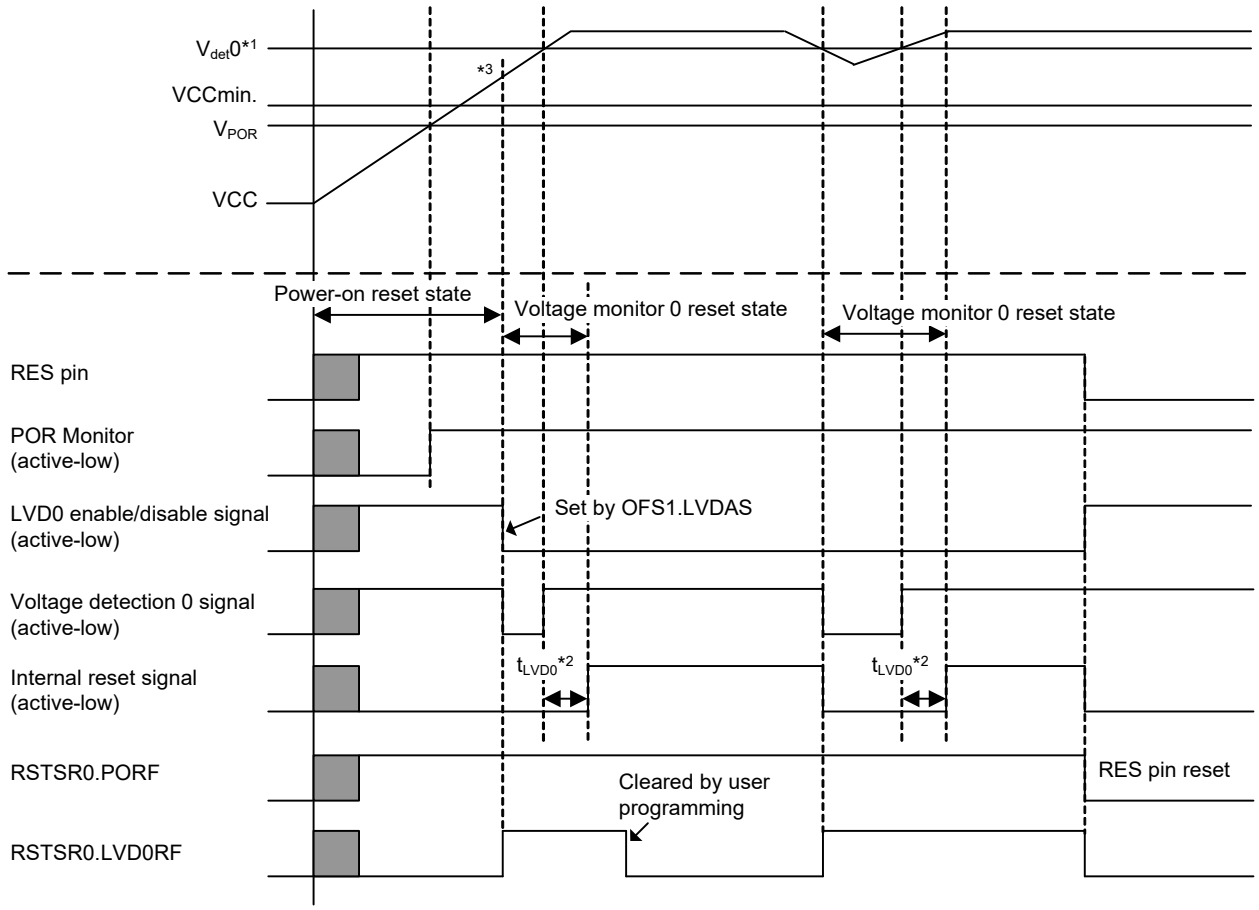
5.3.2 Power-On Reset

The power-on reset (POR) is an internal reset generated by the power-on reset circuit. If the RES pin is in a high level state when power is supplied, a power-on reset is generated. After VCC exceeds V_{POR} and the specified power-on reset time elapses, the internal reset is canceled and the CPU starts the reset exception handling. The power-on reset time is a stabilization period of the external power supply and the MCU circuit. After a power-on reset is generated, the PORF flag in the RSTSR0 is set to 1. The PORF flag is initialized by the RES pin reset.

The voltage monitor 0 reset is an internal reset generated by the voltage monitor circuit. If the Voltage Detection 0 Circuit Start (LVDAS) bit in the Option Function Select register 1 (OFS1) is 0 (voltage monitor 0 reset is enabled after a reset) and VCC falls below V_{det0}, the RSTSR0.LVD0RF flag is set to 1 and the voltage detection circuit generates voltage monitor 0 reset. Clear the OFS1.LVDAS bit to 0 if the voltage monitor 0 reset is to be used.

After VCC exceeds V_{det0} and the voltage monitor 0 reset time (tLVD0) elapses, the internal reset is canceled and the CPU starts the reset exception handling. The V_{det0} voltage detection level can be changed by the setting in the VDSEL1[2:0] bits in the Option Function Select register 1 (OFS1).

Figure 5.1 shows examples of operation during a power-on reset and voltage monitor 0 reset.



Note: For details on the electrical characteristics, see section 46, Electrical Characteristics.
Note 1. V_{det0} shows a voltage monitor 0 reset detection level, and V_{POR} shows a power-on reset detection level, and VCCmin shows the minimum guaranteed voltage of MCU.
Note 2. t_{LVD0} shows a time for voltage monitor 0 reset.
Note 3. At power-on, VCC should have risen to the minimum guaranteed voltage before the POR reset is released.

Figure 5.1 Example of operation during power-on reset and voltage monitor 0 reset

5.3.3 Voltage Monitor Reset

The voltage monitor 0 reset is an internal reset generated by the voltage monitor circuit. If the Voltage Detection 0 Circuit Start (LVDAS) bit in the Option Function Select register 1 (OFS1) is 0 (voltage monitor 0 reset is enabled after a reset) and VCC falls below V_{det0}, the RSTSR0.LVD0RF flag is set to 1 and the voltage detection circuit generates a voltage monitor 0 reset. Clear the OFS1.LVDAS bit to 0 if the voltage monitor 0 reset is to be used. After VCC exceeds V_{det0} and the voltage monitor 0 reset time (tLVD0) elapses, the internal reset is canceled and the CPU starts the reset exception handling.

When the Voltage Monitor 1 Interrupt/Reset Enable bit (RIE) is set to 1 (enabling generation of a reset or interrupt by the voltage detection circuit) and the Voltage Monitor 1 Circuit Mode Select bit (LVD1CR0.RI) is set to 1 (selecting generation of a reset in response to detection of a low voltage) in Voltage Monitor 1 Circuit Control Register 0 (LVD1CR0), the RSTSR0.LVD1RF flag is set to 1 and the voltage detection circuit generates a voltage monitor 1 reset if VCC falls to or below V_{det1}.

Likewise, when the Voltage Monitor 2 Interrupt/Reset Enable bit (RIE) is set to 1 (enabling generation of a reset or

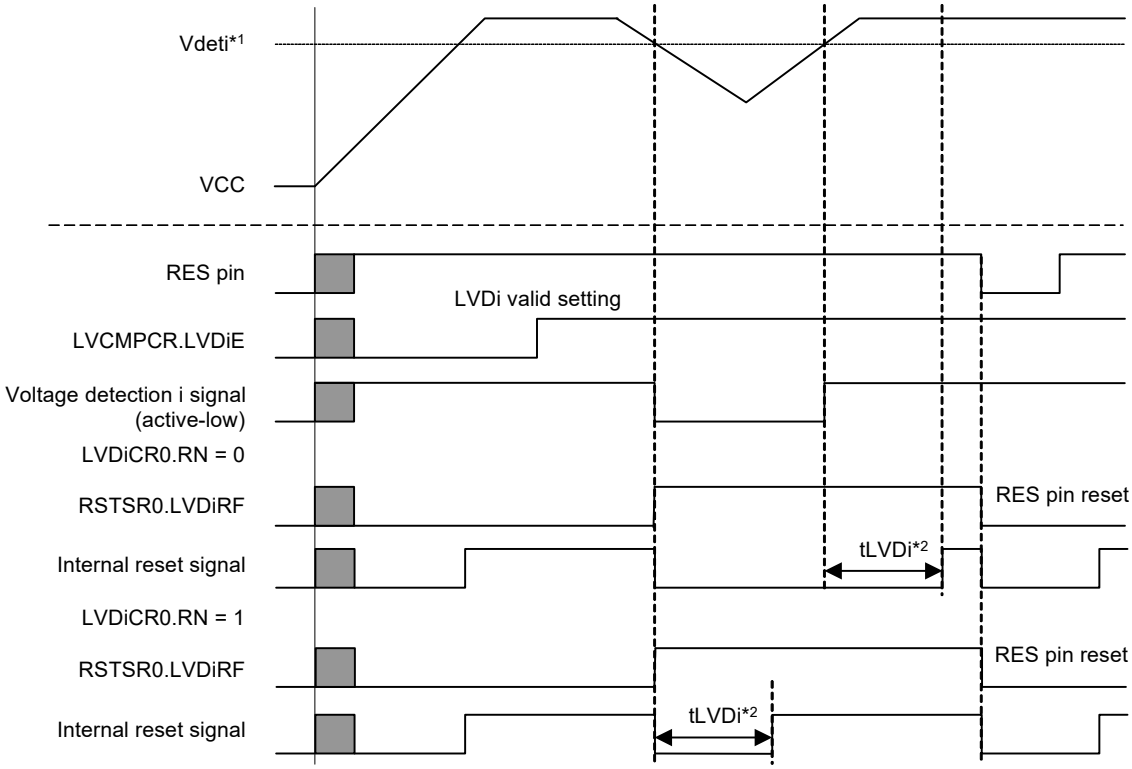
interrupt by the voltage detection circuit) and the Voltage Monitor 2 Circuit Mode Select bit (LVD2CR0.RI) is set to 1 (selecting generation of a reset in response to detection of a low voltage) in Voltage Monitor 2 Circuit Control Register 0 (LVD2CR0), the RSTSR0.LVD2RF flag is set to 1 and the voltage detection circuit generates a voltage monitor 2 reset if VCC falls to or below V_{det2}.

Similarly, timing for release from the voltage monitor 1 reset state is selectable with the Voltage Monitor 1 Reset Negate Select bit (RN) in the LVD1CR0. When the LVD1CR0.RN bit is 0 and VCC falls to or below V_{det1}, the CPU is released from the internal reset state and starts reset exception handling when the LVD1 reset time (tLVD1) elapses after VCC rises above V_{det1}. When the LVD1CR0.RN bit is 1 and VCC falls to or below V_{det1}, the CPU is released from the internal reset state and starts reset exception handling when the LVD1 reset time (tLVD1) elapses.

Likewise, timing for release from the voltage monitor 2 reset state is selectable by setting the Voltage Monitor 2 Reset Negate Select bit (RN) in the LDV2CR0 register.

Detection levels V_{det1} and V_{det2} can be changed in the Voltage Detection Level Select Register (LVDLVLR).

Figure 5.2 shows example of operations during voltage monitor 1 and 2 resets. For details on the voltage monitor 1 reset and voltage monitor 2 reset, see section 7, Low Voltage Detection (LVD).



Note: For details on the electrical characteristics, see section 46, Electrical Characteristics.
Note 1. Vdeti indicates the detection level of voltage monitor 1 reset and voltage monitor 2 reset (i = 1, 2).
Note 2. tLVDi indicates the time for voltage monitor 1 reset and voltage monitor 2 reset (i = 1, 2).

Figure 5.2 Example of operations during voltage monitor 1 and voltage monitor 2 resets

5.3.4 Independent Watchdog Timer Reset

The independent watchdog timer reset is an internal reset generated from the Independent Watchdog Timer (IWDT). Output of the independent watchdog timer reset from the IWDT can be selected in the Option Function Select register 0 (OFS0).

When output of the independent watchdog timer reset is selected, the reset is generated if the IWDT underflows, or if data is written when refresh operation is disabled. When the internal reset time (tRESW2) elapses after the independent watchdog timer reset is generated, the internal reset is canceled and the CPU starts the reset exception handling.

For details on the independent watchdog timer reset, see section 25, Independent Watchdog Timer (IWDT).

5.3.5 Watchdog Timer Reset

The watchdog timer reset is an internal reset generated from the Watchdog Timer (WDT). Output of the watchdog timer reset from the WDT can be selected in the WDT Reset Control Register (WDTRCR) or Option Function Select Register 0 (OFS0).

When output of the watchdog timer reset is selected, a watchdog timer reset is generated if the WDT underflows, or if data is written when refresh operation is disabled. When the internal reset time (tRESW2) elapses after the watchdog timer reset is generated, the internal reset is canceled and the CPU starts the reset exception handling.

For details on the watchdog timer reset, see section 24, Watchdog Timer (WDT).

5.3.6 Software Reset

The software reset is an internal reset generated by software setting of the SYSRESETREQ bit in the AIRCR register in the Arm core. When the SYSRESETREQ bit is set to 1, a software reset is generated. When the internal reset time (tRESW2) elapses after the software reset is generated, the internal reset is canceled and the CPU starts the reset exception handling.

For details on the SYSRESETREQ bit, see the *ARM® Cortex®-M0+ Technical Reference Manual*.

5.3.7 Determination of Cold/Warm Start

Read the CWSF flag in RSTSR2 to determine the cause of reset processing. The flag indicates whether a power-on reset caused the reset processing (cold start) or a reset signal input during operation caused the reset processing (warm start).

The CWSF flag is set to 0 when a power-on reset occurs (cold start). Otherwise, the flag is not set to 0. The flag is set to 1 when 1 is written to it through software. It is not set to 0 even on writing 0 to it.

Figure 5.3 shows an example of a cold/warm start determination operation.

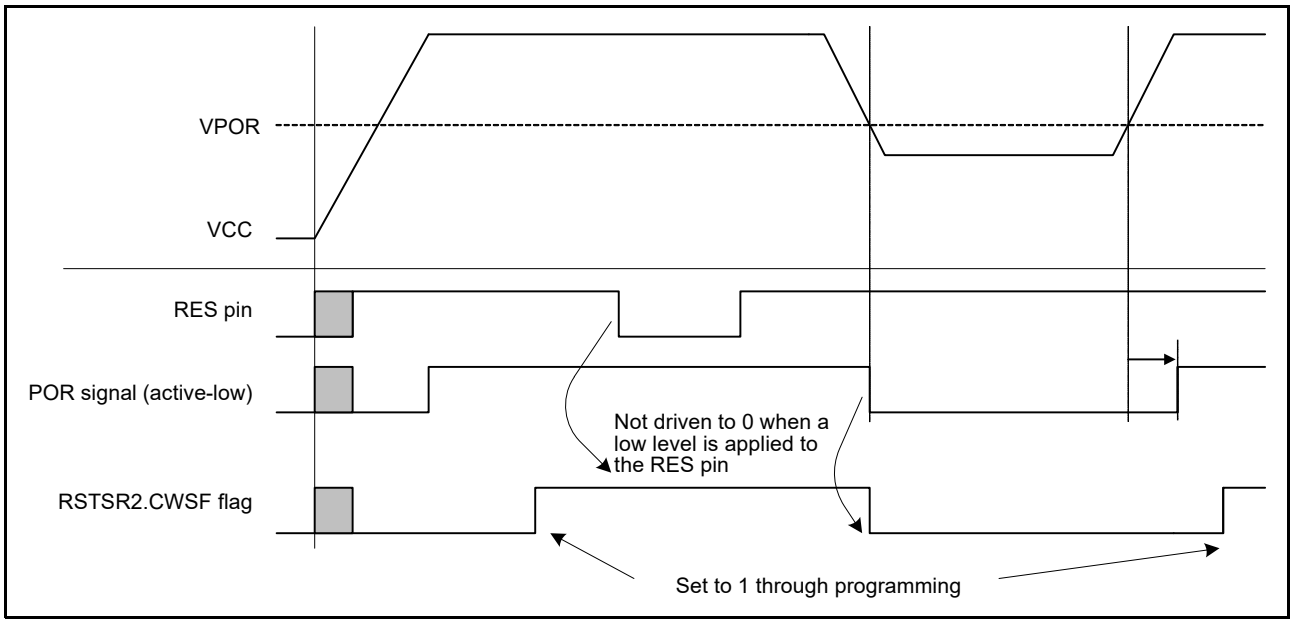
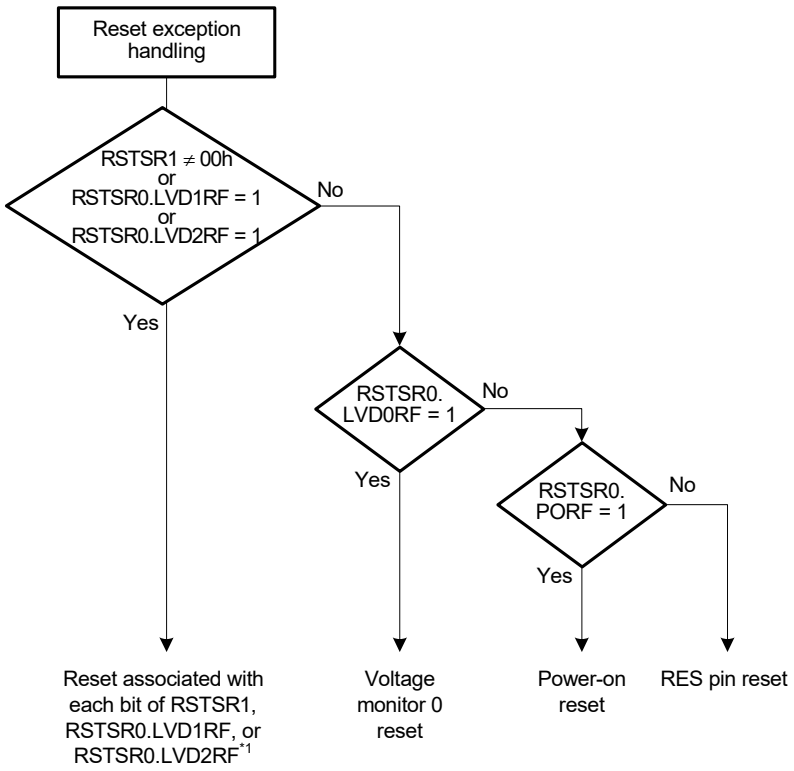


Figure 5.3 Example of a cold/warm start determination operation

5.3.8 Determination of Reset Generation Source

Read RSTSR0 and RSTSR1 to determine which reset executes the reset exception handling.

Figure 5.4 shows an example of the flow to identify a reset generation source. The reset flag must be written with 0 after the reset flag is read as 1.



Note 1. If a reset associated with each bit of RSTSR1, RSTSR0.LVD1RF, or RSTSR0.LVD2RF occurs at the same time, all reset flags are set to 1.

Figure 5.4 Example of reset generation source determination flow

6. Option-Setting Memory

6.1 Overview

The option-setting memory determines the state of the MCU after a reset. The option-setting memory is allocated to the configuration setting area and the program flash area of the flash memory, and the available methods of setting are different for the two areas. Figure 6.1 shows the option-setting memory area.

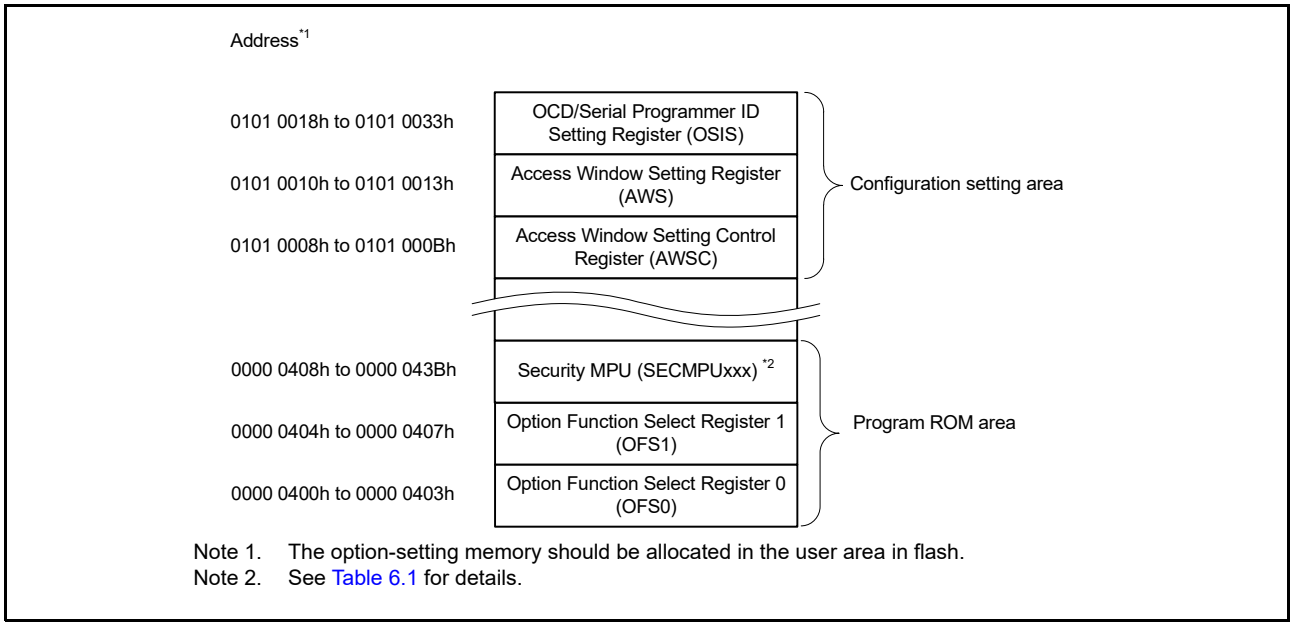


Figure 6.1 Option-setting memory area

6.2 Register Descriptions

6.2.1 Option Function Select Register 0 (OFS0)

Address(es): OFS0 0000 0400h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	WDTSTPCTL	—	WDTRSTIRQS	WDTRPSS[1:0]		WDTRPES[1:0]		WDTCKS[3:0]				WDTTOPS[1:0]		WDTSTRT	—
Value after reset:	The value set by the user*1															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	IWDTSTPCTL	—	IWDTRSTIRQS	IWDTRPSS[1:0]		IWDTRPES[1:0]		IWDTCKS[3:0]				IWDTTOPS[1:0]		IWDTSTRT	—
Value after reset:	The value set by the user*1															

Bit	Symbol	Bit name	Description	R/W
b0	—	Reserved	When read, this bit returns the written value. The write value should be 1.	R
b1	IWDTSTRT	IWDT Start Mode Select	0: Automatically activate IWDT after a reset (auto-start mode) 1: Disable IWDT.	R
b3, b2	IWDTTOPS[1:0]	IWDT Timeout Period Select	b3 b2 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1024 cycles (03FFh) 1 1: 2048 cycles (07FFh).	R

Bit	Symbol	Bit name	Description	R/W
b7 to b4	IWDTCKS[3:0]	IWDT-Dedicated Clock Frequency Division Ratio Select	b7 b4 0 0 0 0: × 1 0 0 1 0: × 1/16 0 0 1 1: × 1/32 0 1 0 0: × 1/64 1 1 1 1: × 1/128 0 1 0 1: × 1/256. Other settings are prohibited.	R
b9, b8	IWDTRPES[1:0]	IWDT Window End Position Select	b9 b8 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0% (no window end position setting).	R
b11, b10	IWDTRPSS[1:0]	IWDT Window Start Position Select	b11 b10 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100% (no window start position setting)	R
b12	IWDTRSTIRQS	IWDT Reset Interrupt Request Select	0: Interrupt 1: Reset	R
b13	—	Reserved	When read, this bit returns the written value. The write value should be 1.	R
b14	IWDTSTPCTL	IWDT Stop Control	0: Continue counting 1: Stop counting when in Sleep mode, Snooze mode, or Software Standby mode.	R
b16, b15	—	Reserved	When read, these bits return the written value. The write value should be 1.	R
b17	WDTSTRT	WDT Start Mode Select	0: Automatically activate WDT after a reset (auto-start mode) 1: Stop WDT after a reset (register-start mode).	R
b19, b18	WDTTOPS[1:0]	WDT Timeout Period Select	b19 b18 0 0: 1024 cycles (03FFh) 0 1: 4096 cycles (0FFFh) 1 0: 8192 cycles (1FFFh) 1 1: 16384 cycles (3FFFh).	R
b23 to b20	WDTCKS[3:0]	WDT Clock Frequency Division Ratio Select	b23 b20 0 0 0 1: PCLKB divided by 4 0 1 0 0: PCLKB divided by 64 1 1 1 1: PCLKB divided by 128 0 1 1 0: PCLKB divided by 512 0 1 1 1: PCLKB divided by 2048 1 0 0 0: PCLKB divided by 8192 Other settings are prohibited.	R
b25, b24	WDTRPES[1:0]	WDT Window End Position Select	b25 b24 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0% (No window end position setting).	R
b27, b26	WDTRPSS[1:0]	WDT Window Start Position Select	b27 b26 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100% (No window start position setting).	R
b28	WDTRSTIRQS	WDT Reset Interrupt Request Select	WDT Behavior Select: 0: Interrupt 1: Reset.	R
b29	—	Reserved	When read, this bit returns the written value. The write value should be 1.	R
b30	WDTSTPCTL	WDT Stop Control	0: Continue counting 1: Stop counting when entering Sleep mode.	R
b31	—	Reserved	When read, this bit returns the written value. The write value should be 1.	R

Note 1. The value in a blank product is FFFF FFFFh. It is set to the value written by your application.

IWDTSTRT bit (IWDT Start Mode Select)

The IWDTSTRT bit selects the mode in which the IWDT is activated after a reset (stopped state or activated state).

IWDTTOPS[1:0] bits (IWDT Timeout Period Select)

The IWDTTOPS[1:0] bits select the timeout period, the time it takes for the down counter to underflow as 128, 512, 1024, or 2048 cycles of the frequency-divided clock set in the IWDTCKS[3:0] bits. The number of clock cycles that the IWDT takes to underflow after a refresh operation is determined by the combination of the IWDTCKS[3:0] bits and IWDTTOPS[1:0] bits.

For details, see section 25, Independent Watchdog Timer (IWDT).

IWDTCKS[3:0] bits (IWDT-Dedicated Clock Frequency Division Ratio Select)

The IWDTCKS[3:0] bits specify the division ratio of the prescaler for dividing the frequency of the clock for the IWDT as 1/1, 1/16, 1/32, 1/64, 1/128, and 1/256. Using this setting combined with the IWDTTOPS[1:0] bit setting, the IWDT counting period can be set from 128 to 524288 IWDT clock cycles.

For details, see section 25, Independent Watchdog Timer (IWDT).

IWDTRPES[1:0] bits (IWDT Window End Position Select)

The IWDTRPES[1:0] bits specify the position where the window for the down counter ends as 0%, 25%, 50%, or 75% of the count value. The value of the window end position must be smaller than the value of the window start position. Otherwise, only the value for the window start position is valid.

The counter values associated with the settings for the start and end positions of the window in the IWDTRPSS[1:0] and IWDTRPES[1:0] bits vary with the setting in the IWDTTOPS[1:0] bits.

For details, see section 25, Independent Watchdog Timer (IWDT).

IWDTRPSS[1:0] bits (IWDT Window Start Position Select)

The IWDTRPSS[1:0] bits specify the position where the window for the down counter starts as 25%, 50%, 75%, or 100% of the counted value. The point at which counting starts is 100% and the point at which an underflow occurs is 0%. The interval between the window starts and ends positions becomes the period in which a refresh is possible. Refresh is not possible outside this period.

For details, see section 25, Independent Watchdog Timer (IWDT).

IWDTRSTIRQS bit (IWDT Reset Interrupt Request Select)

The IWDTRSTIRQS bit selects the operation on an underflow of the down counter or generation of a refresh error. The operation is selectable to an independent watchdog timer reset, a non-maskable interrupt request, or an interrupt request.

For details, see section 25, Independent Watchdog Timer (IWDT).

IWDTSTPCTL bit (IWDT Stop Control)

The IWDTSTPCTL bit specifies whether to stop counting when entering Sleep, Snooze, or Software Standby mode.

For details, see section 25, Independent Watchdog Timer (IWDT).

WDTSTRT bit (WDT Start Mode Select)

The WDTSTRT bit selects the mode in which the WDT is activated after a reset (stopped state or activated in auto-start mode). When WDT is activated in auto-start mode, the OFS0 register setting for the WDT is valid.

WDTTOPS[1:0] bits (WDT Timeout Period Select)

The WDTTOPS[1:0] bits specify the timeout period, the time it takes for the down counter to underflow, as 1024, 4096, 8192, or 16384 cycles of the frequency-divided clock set in the WDTCKS[3:0] bits. The number of PCLKB cycles that the counter takes to underflow after a refresh operation is determined by a combination of the WDTCKS[3:0] and WDTTOPS[1:0] bits.

For details, see section 24, Watchdog Timer (WDT).

WDTCKS[3:0] bits (WDT Clock Frequency Division Ratio Select)

The WDTCKS[3:0] bits specify the division ratio of the prescaler to divide the frequency of PCLKB as 1/4, 1/64, 1/128, 1/512, 1/2048, and 1/8192. Using this setting combined with the WDTTOPS[1:0] bit setting, the WDT counting period can be set from 4096 to 134217728 PCLKB cycles.

For details, see section 24, Watchdog Timer (WDT).

WDTRPES[1:0] bits (WDT Window End Position Select)

The WDTRPES[1:0] bits specify the position where the window for the down counter ends as 0%, 25%, 50%, or 75% of the counted value. The value of the window end position must be smaller than the value of the window start position. Otherwise, only the value for the window start position is valid.

The counter values associated with the settings for the start and end positions of the window, in the WDTRPSS[1:0] and WDTRPES[1:0] bits, vary with the setting of the WDTTOPS[1:0] bits.

For details, see section 24, Watchdog Timer (WDT).

WDTRPSS[1:0] bits (WDT Window Start Position Select)

The WDTRPSS[1:0] bits specify the position where the window for the down counter starts as 25%, 50%, 75%, or 100% of the counted value. The point at which counting starts is 100% and the point at which an underflow occurs is 0%. The interval between the positions where the window starts and ends becomes the period in which a refresh is possible. Refresh is not possible outside this period.

For details, see section 24, Watchdog Timer (WDT).

WDTRSTIRQS bit (WDT Reset Interrupt Request Select)

The WDTRSTIRQS bit selects the operation on an underflow of the down-counter or generation of a refresh error. The operation is selectable to a watchdog timer reset, a non-maskable interrupt request, or an interrupt request.

For details, see section 24, Watchdog Timer (WDT).

WDTSTPCTL bit (WDT Stop Control)

The WDTSTPCTL bit specifies whether to stop counting when entering Sleep mode.

For details, see section 24, Watchdog Timer (WDT).

6.2.2 Option Function Select Register 1 (OFS1)

Address(es): OFS1 0000 0404h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	The value set by the user*1															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	HOCOFRQ1[2:0]			—	—	—	HOCO EN	—	—	VDSEL1[2:0]			LVDAS	—	—
Value after reset:	The value set by the user*1															

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	When read, these bits return the written value. The write value should be 1.	R
b2	LVDAS	Voltage Detection 0 Circuit Start	0: Enable voltage monitor 0 reset after a reset 1: Disable voltage monitor 0 reset after a reset.	R

Bit	Symbol	Bit name	Description	R/W
b5 to b3	VDSEL1[2:0]	Voltage Detection 0 Level Select	b5 b3 0 0 0: Selects 3.84 V 0 0 1: Selects 2.82 V 0 1 0: Selects 2.51 V 0 1 1: Selects 1.90 V 1 0 0: Selects 1.70 V. Other settings are prohibited.	R
b7, b6	—	Reserved	When read, these bits return the written value. The write value should be 1.	R
b8	HOCOEN	HOCO Oscillation Enable	0: Enable HOCO oscillation after a reset 1: Disable HOCO oscillation after a reset.	R
b11 to b9	—	Reserved	When read, these bits return the written value. The write value should be 1.	R
b14 to b12	HOCOFRQ1[2:0]	HOCO Frequency Setting 1	b14 b12 0 0 0: 24 MHz 0 1 0: 32 MHz 1 0 0: 48 MHz 1 0 1: 64 MHz Other settings are prohibited.	R
b31 to b15	—	Reserved	When read, these bits return the written value. The write value should be 1.	R

Note 1. The value in a blank product is FFFF FFFFh. It is set to the value written by your application.

LVDAS bit (Voltage Detection 0 Circuit Start)

The LVDAS bit selects whether the voltage monitor 0 reset is enabled or disabled after a reset.

VDSEL1[2:0] bits (Voltage Detection 0 Level Select)

The VDSEL1[2:0] bits select the voltage detection level of the voltage detection 0 circuit.

HOCOEN bit (HOCO Oscillation Enable)

The HOCOEN bit selects whether the HOCO oscillation is enabled or disabled after a reset. Setting this bit to 0 allows the HOCO oscillation to start before the CPU starts operation, which reduces the wait time for oscillation stabilization.

Note: When the HOCOEN bit is set to 0, the system clock source is not switched to HOCO. The system clock source is only switched to HOCO by setting the Clock Source Select bits (SCKSCR.CKSEL[2:0]). To use the HOCO clock, you must set the OFS1.HOCOFRQ1[2:0] bits to an optimum value.

After a reset release, operation is in the low-voltage mode and therefore HOCOCR.HCSTP must be set immediately to 0.

HOCOFRQ1[2:0] bits (HOCO Frequency Setting 1)

The HOCOFRQ1[2:0] bits select the HOCO frequency after a reset as 24, 32, 48, or 64 MHz.

6.2.3 MPU Registers

Table 6.1 indicates the registers related to the MPU function. For detailed specifications, see 14. Memory Protection Unit (MPU).

The security MPU is disabled on erasure of flash memory. If incorrect data is written to an MPU register, the MCU may not work. See 14. Memory Protection Unit (MPU) to set the proper data.

Table 6.1 MPU registers (1 of 2)

Register Name	Symbol	Function	Address	Size (byte)
Security MPU Program Counter Start Address Register 0	SECMPUPCS0	Specifies the security fetch region of the code flash or SRAM.	0000 0408h	4
Security MPU Program Counter End Address Register 0	SECMPUPCE0	Specifies the security fetch region of the code flash or SRAM.	0000 040Ch	4

Table 6.1 MPU registers (2 of 2)

Register Name	Symbol	Function	Address	Size (byte)
Security MPU Program Counter Start Address Register 1	SECMPUPCS1	Specifies the security fetch region of the code flash or SRAM	0000 0410h	4
Security MPU Program Counter End Address Register 1	SECMPUPCE1	Specifies the security fetch region of the code flash or SRAM.	0000 0414h	4
Security MPU Region 0 Start Address Register	SECMPUS0	Specifies the security program and data of the code flash	0000 0418h	4
Security MPU Region 0 End Address Register	SECMPUE0	Specifies the security program and data of the code flash.	0000 041Ch	4
Security MPU Region 1 Start Address Register	SECMPUS1	Specifies the security program and data of the SRAM.	0000 0420h	4
Security MPU Region 1 End Address Register	SECMPUE1	Specifies the security program and data of the SRAM.	0000 0424h	4
Security MPU Region 2 Start Address Register	SECMPUS2	Specifies the security data of the Security Function.	0000 0428h	4
Security MPU Region 2 End Address Register	SECMPUE2	Specifies the security data of the Security Function.	0000 042Ch	4
Security MPU Region 3 Start Address Register	SECMPUS3	Specifies the security data of the Security Function.	0000 0430h	4
Security MPU Region 3 End Address Register	SECMPUE3	Specifies the security data of the Security Function.	0000 0434h	4
Security MPU Access Control Register	SECMPUAC	Specifies the security enabled/disabled region.	0000 0438h	4

6.2.4 Access Window Setting Control Register (AWSC)

Address(es): AWSC 0101 0008h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	The value set by the user															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	FSPR	—	—	—	—	—	BTFLG	—	—	—	—	—	—	—	—
Value after reset:	The value set by the user															

Bit	Symbol	Bit name	Description	R/W
b7 to b0	—	Reserved	When read, these bits return the written value. The write value should be 1.	R
b8	BTFLG	Startup Area Select Flag	This bit specifies whether the address of the startup area is exchanged for the boot swap function. 0: Exchange the first 8-KB area (0000 0000h to 0000 1FFFh) and second 8-KB area (0000 2000h to 0000 3FFFh) 1: Do not exchange the first 8-KB area (0000 0000h to 0000 1FFFh) and second 8-KB area (0000 2000h to 0000 3FFFh).	R
b13 to b9	—	Reserved	When read, these bits return the written value. The write value should be 1.	R

Bit	Symbol	Bit name	Description	R/W
b14	FSPR	Protection of Access Window and Startup Area Select Function	This bit controls the programming/erase protection for the access window, the Startup Area Select Flag (BTFLG), and the temporary boot swap. Once this bit is set to 0, it cannot be changed to 1. 0: Executing the configuration setting command for programming the access window (FAWE[11:0], FAWS[11:0]) and the Startup Area Select flag (BTFLG) is invalid. 1: Executing the configuration setting command for programming the access window (FAWE[11:0], FAWS[11:0]) and the Startup Area Select flag (BTFLG) is valid.	R
b31 to b15	—	Reserved	When read, these bits return the written value. The write value should be 1.	R

6.2.5 Access Window Setting Register (AWS)

Address(es): AWS 0101 0010h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	FAWE[11:0]											
Value after reset:	The value set by the user															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	FAWS[11:0]											
Value after reset:	The value set by the user															

Bit	Symbol	Bit name	Description	R/W
b11 to b0	FAWS[11:0]	Access Window Start Block Address	These bits specify the start block address for the access window. They do not represent the block number of the access window. The access window is only valid in the program flash area. The block address specifies the first address of the block and consists of the address bits [21:10].	R
b15 to b12	—	Reserved	When read, these bits return the written value. The write value should be 1.	R
b27 to b16	FAWE[11:0]	Access Window End Block Address	These bits specify the end block address for the access window. They do not represent the block number of the access window. The access window is only valid in the program flash area. The end block address for the access window is the next block to the region acceptable for programming and erasure defined by the access window. The block address specifies the first address of the block and consists of the address bits [21:10].	R
b31 to b28	—	Reserved	When read, these bits return the written value. The write value should be 1.	R

Issuing the program or erase command to an area outside the access window causes a command-locked state. The access window is only valid in the program flash area. The access window provides protection in self-programming mode, serial programming mode, and on-chip debug mode. The access window can be locked by the FSPR bit.

The access window is specified in both the FAWS[11:0] bits and the FAWE[11:0] bits. The following describes how to set the FAWS[11:0] and the FAWE[11:0] bits.

- FAWE[11:0] = FAWS[11:0]: The P/E command is allowed to execute in the full program flash area.
- FAWE[11:0] > FAWS[11:0]: The P/E command is only allowed to execute in the window from the block pointed to by the FAWS[11:0] bits to the block one lower than the block pointed to by the FAWE[11:0] bits.
- FAWE[11:0] < FAWS[11:0]: The P/E command is not allowed to execute in the program flash area.

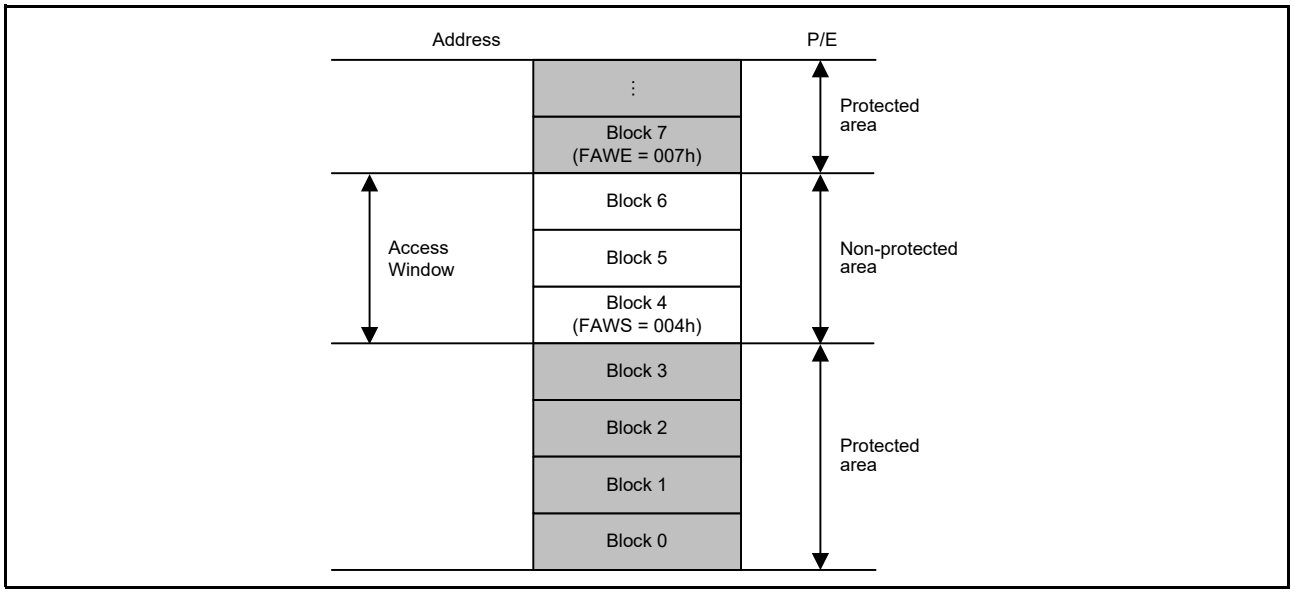


Figure 6.2 Access window overview

6.2.6 OCD/Serial Programmer ID Setting Register (OSIS)

This register stores the ID for ID code protection of the OCD/serial programmer. When connecting the OCD/serial programmer, write values so that the MCU can determine whether to permit the connection. This register checks whether a code transmitted from the OCD/serial programmer matches the ID code in the option-setting memory. When the ID codes match, the connection of the OCD/serial programmer is permitted, if not, connection with the OCD/serial programmer is not possible. The OSIS register must be set in 32-bit units.

Address(es): OSIS 0101 0018h, OSIS 0101 0020h, OSIS 0101 0028h, OSIS 0101 0030h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	The value set by the user															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	The value set by the user															

These fields hold the ID for use in ID authentication for the OCD/serial programmer.

ID code bit [127] and bit [126] determine whether ID code protection is enabled and the method of authentication to use with the host. Table 6.2 shows how ID code determines the method of authentication.

Table 6.2 Specifications for ID code protection

Operating mode on boot up	ID code	State of protection	Operations on connection to programmer or on-chip debugger
Serial programming mode (SCI boot mode) On-chip debug mode (SWD boot mode)	FFh, …, FFh (all bytes FFh)	Protection disabled	The ID code is not checked, the ID code always matches, and the connection to the serial programmer or on-chip debugger is permitted.
	Bit [127] = 1, bit [126] = 1, and at least one of the 16 bytes is not FFh	Protection enabled	Matching ID code indicates that authentication is complete and connection to the serial programmer or the on-chip debugger is permitted. Mismatching ID code indicates transition to the ID code protection wait state. When the ID code sent from the serial programmer or the on-chip debugger is ALeRASE in ASCII code (0x414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFF), the content of the user flash area is erased and all bits in the OSIS register are 1. However, when the AWS.FSPR bit is 0 or security MPU is enabled, the content of the user flash area is not erased.
	Bit [127] = 1 and bit [126] = 0	Protection enabled	Matching ID code indicates that authentication is complete and connection to the serial programmer or the on-chip debugger is permitted. Mismatching ID code indicates transition to the ID code protection wait state.
	Bit [127] = 0	Protection enabled	The ID code is not checked, the ID code is always mismatching, the connection to the serial programmer or the on-chip debugger is prohibited. When the ID code sent from the on-chip debugger is ALeRASE in ASCII code (0x414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFF), the content of the user flash area is erased and all bits in the OSIS register are 1. However, when the AWSC.FSPR bit is 0 or security MPU is enabled, the content of the user flash area is not erased.

6.3 Setting Option-Setting Memory

6.3.1 Allocation of Data in Option-Setting Memory

Programming data is allocated to the addresses in the option-setting memory shown in Figure 6.1. The allocated data is used by tools such as a flash programming software or an on-chip debugger.

Note: Programming formats vary depending on the compiler. See the compiler manual for details.

6.3.2 Setting Data for Programming Option-Setting Memory

Allocating data according to the procedure described in section 6.3.1, Allocation of Data in Option-Setting Memory, alone does not actually write the data to the option-setting memory. You must also follow one of the actions described in this section.

(1) Changing the option-setting memory by self-programming

Use the programming command to write data to the program flash area. Use the configuration setting command to write data to the option-setting memory in the configuration setting area. In addition, use the startup area select function to safely update the boot program that includes the option-setting memory.

For details on the programming command, the configuration setting command, and the startup area select function, see section 42, Flash Memory.

(2) Debugging through an OCD or programming by a flash writer

This procedure depends on the tool in use, so see the tool manual for details.

The MCU provides two setting procedures as follows:

- Read the data allocated as described in section 6.3.1, Allocation of Data in Option-Setting Memory, from an object file or Motorola S-format file generated by the compiler, and write the data to the MCU
- Use the GUI interface of the tool to program the same data as allocated in section 6.3.1, Allocation of Data in Option-Setting Memory.

6.4 Usage Note

6.4.1 Data for Programming Reserved Areas and Reserved Bits in the Option-Setting Memory

When reserved areas and reserved bits in the option-setting memory are within the scope of programming, write 1 to all bits of reserved areas and all reserved bits. If 0 is written to these bits, normal operation cannot be guaranteed.

7. Low Voltage Detection (LVD)

7.1 Overview

The Low Voltage Detection (LVD) module monitors the voltage level input to the VCC pin, and the detection level can be selected using a software program. The LVD module consists of three separate voltage level detectors, 0, 1, and 2, which measure the voltage level input to the VCC pin. LVD voltage detection registers allow your application to configure detection of VCC changes at various voltage thresholds.

Each voltage level detector has a voltage monitor associated with it, such as voltage monitor 0, 1, and 2. Voltage monitor registers are used to configure the LVD to trigger an interrupt, event link output, or reset when the thresholds are crossed.

Table 7.1 lists the LVD specifications. Figure 7.1 shows a block diagram of the voltage detectors 0, 1, and 2, Figure 7.2 shows a block diagram of the voltage monitor 1 interrupt/ reset circuit, and Figure 7.3 shows a block diagram of the voltage monitor 2 interrupt/reset circuit.

Table 7.1 LVD specifications

Parameter		Voltage monitor 0	Voltage monitor 1	Voltage monitor 2
VCC monitoring	Monitored voltage	V_{det0}	V_{det1}	V_{det2}
	Detected event	Voltage falls below V_{det0}	Voltage rises or falls past V_{det1}	Voltage rises or falls past V_{det2}
	Detection voltage	Selectable from 5 different levels in the OFS1.VDSEL1[2:0] bits	Selectable from 16 different levels using LVDLVLR.LVD1LVL[4:0] bits	Selectable from 4 different levels using LVDLVLR.LVD2LVL[2:0] bits
	Monitor flag	None	LVD1SR.MON flag: Monitors whether voltage is higher or lower than V_{det1}	LVD2SR.MON flag: Monitors whether voltage is higher or lower than V_{det2}
			LVD1SR.DET flag: V_{det1} passage detection	LVD2SR.DET flag: V_{det2} passage detection
Process upon voltage detection	Reset	Voltage monitor 0 reset	Voltage monitor 1 reset	Voltage monitor 2 reset
		Reset when V_{det0} > VCC CPU restart after specified time with VCC > V_{det0}	Reset when V_{det1} > VCC CPU restart timing selectable: after specified time with VCC > V_{det1} or V_{det1} > VCC	Reset when V_{det2} > VCC CPU restart timing selectable: after specified time with VCC > V_{det2} or V_{det2} > VCC
	Interrupt	No interrupt	Voltage monitor 1 interrupt	Voltage monitor 2 interrupt
			Non-maskable interrupt or maskable interrupt selectable	Non-maskable interrupt or maskable interrupt selectable
			Interrupt request issued when Vd_{det1} > VCC or VCC > V_{det1}	Interrupt request issued when V_{det2} > VCC or VCC > V_{det2}
Event linking		None	Available Output of event signals on detection of V_{det1} crossings	Available Output of event signals on detection of V_{det2} crossings

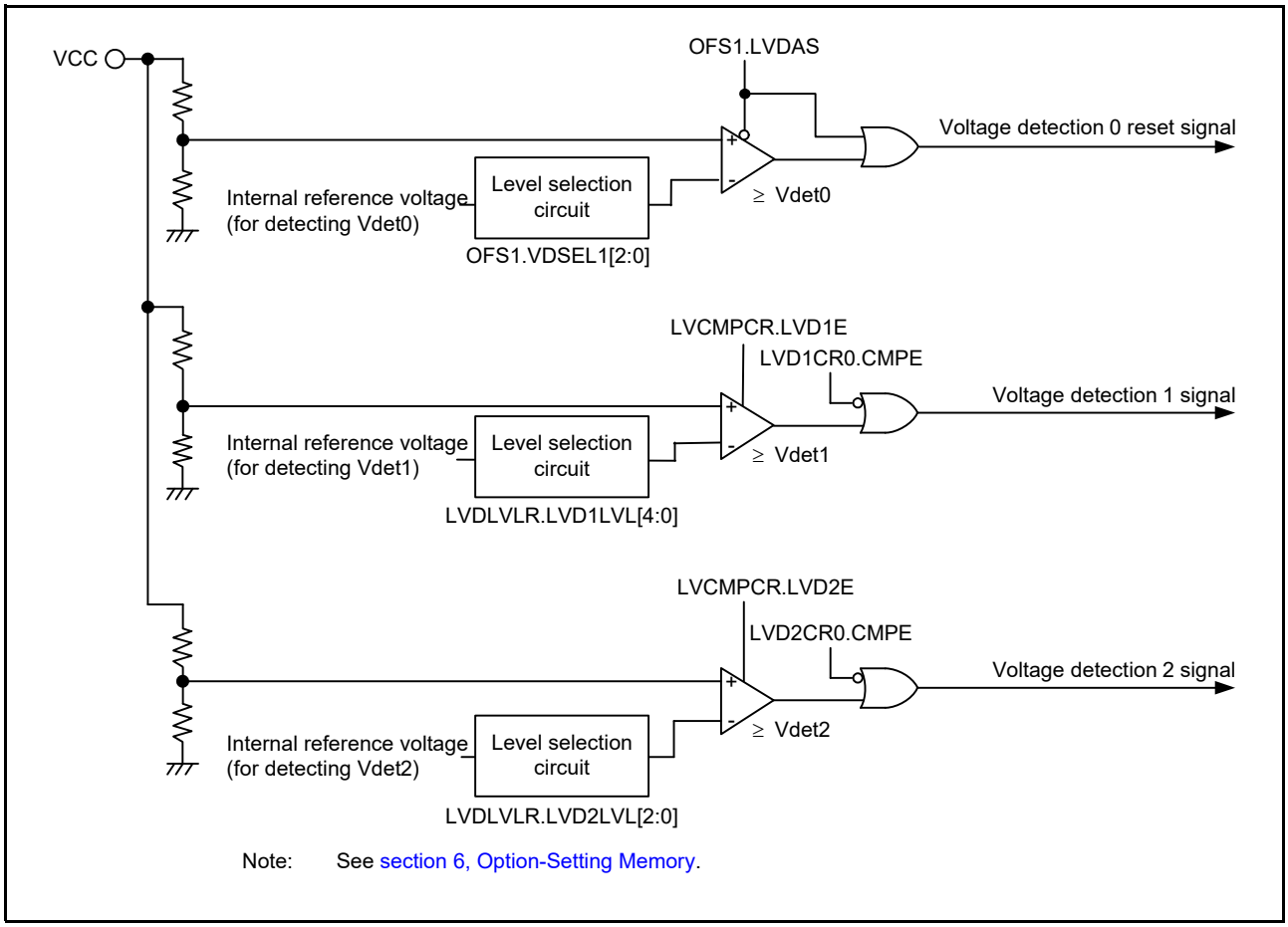


Figure 7.1 Voltage detection 0, 1, and 2 block diagram

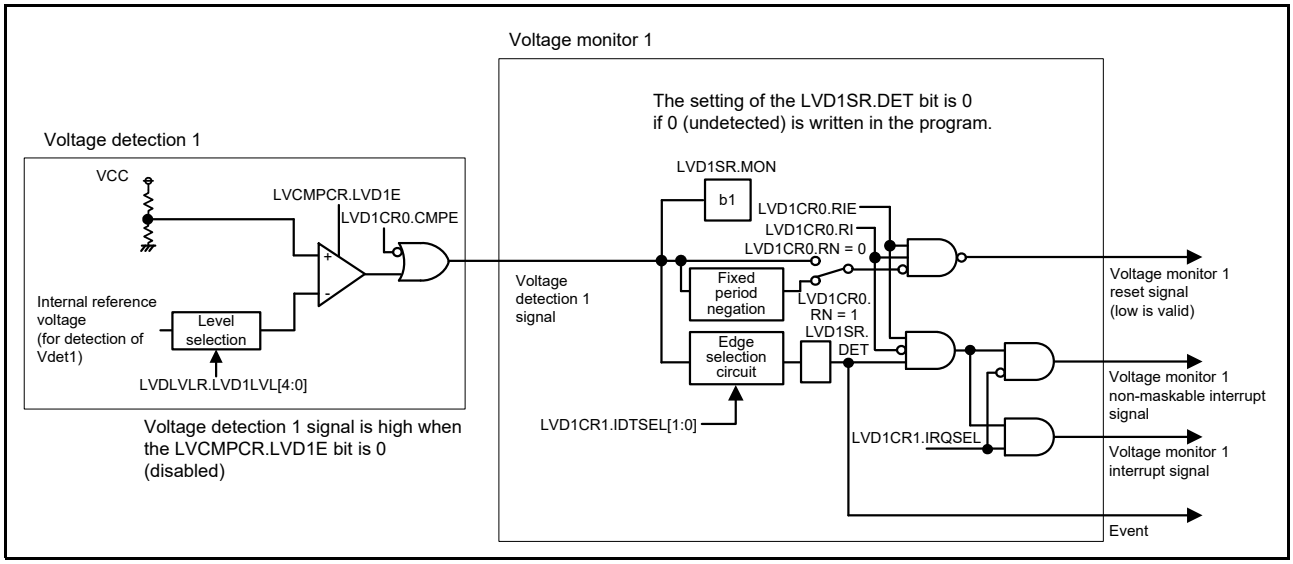


Figure 7.2 Voltage monitor 1 interrupt/reset circuit block diagram

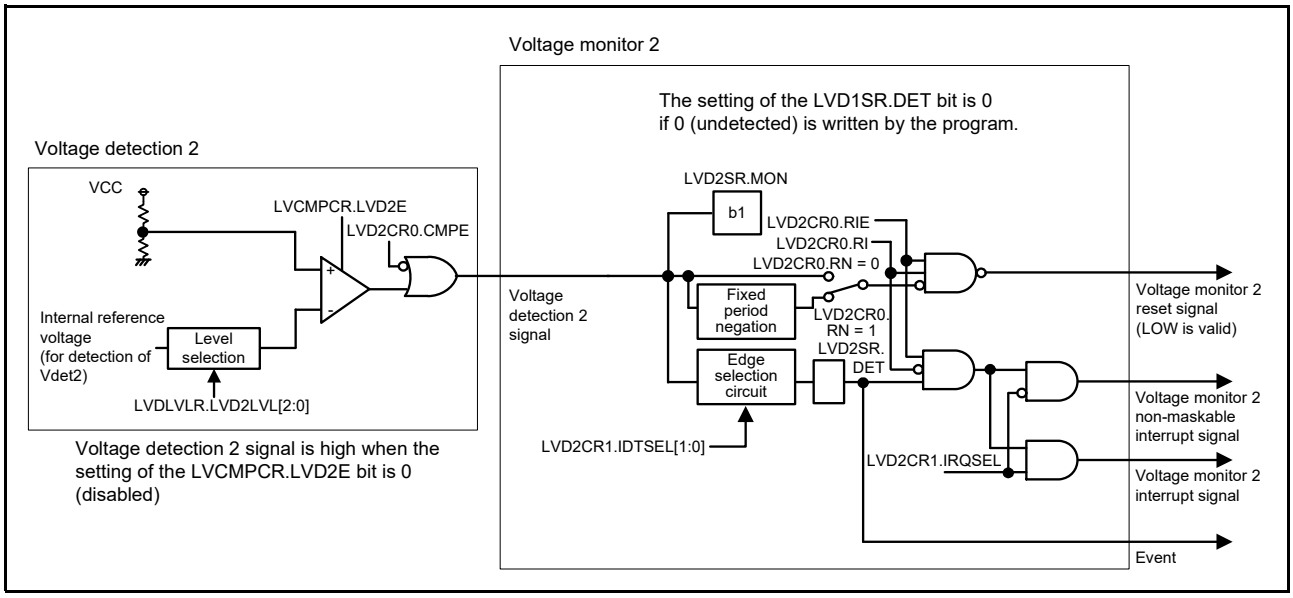


Figure 7.3 Voltage monitor 2 interrupt/reset circuit block diagram

7.2 Register Descriptions

7.2.1 Voltage Monitor 1 Circuit Control Register 1 (LVD1CR1)

Address(es): SYSTEM.LVD1CR1 4001 E0E0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	IRQSEL	IDTSEL[1:0]	
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b1, b0	IDTSEL[1:0]	Voltage Monitor 1 Interrupt Generation Condition Select	b1 b0 0 0: When VCC ≥ V_{det1} (rise) is detected 0 1: When VCC < V_{det1} (fall) is detected 1 0: When fall and rise are detected 1 1: Settings prohibited.	R/W
b2	IRQSEL	Voltage Monitor 1 Interrupt Type Select	0: Non-maskable interrupt 1: Maskable interrupt*1.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.
Note 1. When enabling maskable interrupts, do not change the value in the NMIER.LVD1EN bit in the ICU from the reset state.

7.2.2 Voltage Monitor 1 Circuit Status Register (LVD1SR)

Address(es): SYSTEM.LVD1SR 4001 E0E1h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	MON	DET
Value after reset:	0	0	0	0	0	0	1	0

Bit	Symbol	Bit name	Description	R/W
b0	DET	Voltage Monitor 1 Voltage Change Detection Flag	0: Not detected 1: V_{det1} passage detected.	R(/W) *1
b1	MON	Voltage Monitor 1 Signal Monitor Flag	0: VCC < V_{det1} 1: VCC ≥ V_{det1} or MON is disabled.	R
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.
Note 1. Only 0 can be written to this bit. After writing 0 to this bit, it takes 2 system clock cycles for the bit to be read as 0.

DET flag (Voltage Monitor 1 Voltage Change Detection Flag)

The DET flag is enabled when the LVCMPCR.LVD1E bit is 1 (voltage detection 1 circuit enabled) and the LVD1CR0.CMPE bit is 1 (voltage monitor 1 circuit comparison result output enabled).

Set the DET flag to 0 after LVD1CR0.RIE is set to 0 (disabled). LVD1CR0.RIE can be set to 1 (enabled) after 2 or more PCLKB clock cycles elapse.

MON Flag (Voltage Monitor 1 Signal Monitor Flag)

The MON flag is enabled when the LVCMPCR.LVD1E bit is 1 (voltage detection 1 circuit enabled) and the LVD1CR0.CMPE bit is 1 (voltage monitor 1 circuit comparison result output enabled).

7.2.3 Voltage Monitor 2 Circuit Control Register 1 (LVD2CR1)

Address(es): SYSTEM.LVD2CR1 4001 E0E2h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	IRQSEL	IDTSEL [1:0]	
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b1, b0	IDTSEL [1:0]	Voltage Monitor 2 Interrupt Generation Condition Select	b1 b0 0 0: When VCC ≥ V_{det2} (rise) is detected 0 1: When VCC < V_{det2} (fall) is detected 1 0: When fall and rise are detected 1 1: Settings prohibited.	R/W
b2	IRQSEL	Voltage Monitor 2 Interrupt Type Select	0: Non-maskable interrupt 1: Maskable interrupt*1.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.
Note 1. When enabling maskable interrupts, do not change the value of the NMIER.LVD2EN bit in the ICU from the reset state.

7.2.4 Voltage Monitor 2 Circuit Status Register (LVD2SR)

Address(es): SYSTEM.LVD2SR 4001 E0E3h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	MON	DET
Value after reset:	0	0	0	0	0	0	1	0

Bit	Symbol	Bit name	Description	R/W
b0	DET	Voltage Monitor 2 Voltage Change Detection Flag	0: Not detected 1: V_{det2} passage detected.	R(/W) *1
b1	MON	Voltage Monitor 2 Signal Monitor Flag	0: VCC < V_{det2} 1: VCC ≥ V_{det2} or MON is disabled.	R
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.
Note 1. Only 0 can be written to this bit. After writing 0 to this bit, it takes 2 system clock cycles for the bit to be read as 0.

DET flag (Voltage Monitor 2 Voltage Change Detection Flag)

The DET flag is enabled when the LVCMPCR.LVD2E bit is 1 (voltage detection 2 circuit enabled) and the LVD2CR0.CMPE bit is 1 (voltage monitor 2 circuit comparison result output enabled).

Set the DET flag to 0 after LVD2CR0.RIE is set to 0 (disabled). LVD2CR0.RIE can be set to 1 (enabled) after 2 or more cycles of PCLKB elapse.

MON flag (Voltage Monitor 2 Signal Monitor Flag)

The MON flag is enabled when the LVCMPCR.LVD2E bit is 1 (voltage detection 2 circuit enabled) and the LVD2CR0.CMPE bit is 1 (voltage monitor 2 circuit comparison result output enabled).

7.2.5 Voltage Monitor Circuit Control Register (LVCMPCR)

Address(es): SYSTEM.LVCMPCR 4001 E417h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	LVD2E	LVD1E	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	LVD1E	Voltage Detection 1 Enable	0: Disable voltage detection 1 circuit 1: Enable voltage detection 1 circuit.	R/W
b6	LVD2E	Voltage Detection 2 Enable	0: Disable voltage detection 2 circuit 1: Enable voltage detection 2 circuit.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

LVD1E bit (Voltage Detection 1 Enable)

When using voltage detection 1 interrupt/reset or the LVD1SR.MON bit, set the LVD1E bit to 1. The voltage detection 1 circuit starts when td(E-A) elapses after the LVD1E bit value is changed from 0 to 1.

LVD2E bit (Voltage Detection 2 Enable)

When using voltage detection 2 interrupt/reset or the LVD2SR.MON bit, set the LVD2E bit to 1. The voltage detection 2

circuit starts when td(E-A) elapses after the LVD2E bit value is changed from 0 to 1.

7.2.6 Voltage Detection Level Select Register (LVDLVLR)

Address(es): SYSTEM.LVDLVLR 4001 E418h

	b7	b6	b5	b4	b3	b2	b1	b0
	LVD2LVL[2:0]			LVD1LVL[4:0]				
Value after reset	0	0	0	0	0	1	1	1

Bit	Symbol	Bit name	Description	R/W
b4 to b0	LVD1LVL[4:0]	Voltage Detection 1 Level Select (Standard voltage during fall in voltage)	b4 b0 0 0 0 0 0: 4.29 V (Vdet1_0) 0 0 0 0 1: 4.14 V (Vdet1_1) 0 0 0 1 0: 4.02 V (Vdet1_2) 0 0 0 1 1: 3.84 V (Vdet1_3) 0 0 1 0 0: 3.10 V (Vdet1_4) 0 0 1 0 1: 3.00 V (Vdet1_5) 0 0 1 1 0: 2.90 V (Vdet1_6) 0 0 1 1 1: 2.79 V (Vdet1_7) 0 1 0 0 0: 2.68 V (Vdet1_8) 0 1 0 0 1: 2.58 V (Vdet1_9) 0 1 0 1 0: 2.48 V (Vdet1_A) 0 1 0 1 1: 2.20 V (Vdet1_B) 0 1 1 0 0: 1.96 V (Vdet1_C) 0 1 1 0 1: 1.86 V (Vdet1_D) 0 1 1 1 0: 1.75 V (Vdet1_E) 0 1 1 1 1: 1.65 V (Vdet1_F). Other settings are prohibited.	R/W
b7 to b5	LVD2LVL[2:0]	Voltage Detection 2 Level Select (Standard voltage during fall in voltage)	b7 b5 0 0 0: 4.29 V (Vdet2_0) 0 0 1: 4.14 V (Vdet2_1) 0 1 0: 4.02 V (Vdet2_2) 0 1 1: 3.84 V (Vdet2_3) 1 0 0: Setting prohibited 1 0 1: Setting prohibited 1 1 0: Setting prohibited 1 1 1: Setting prohibited.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

The contents of the LVDLVLR register can only be changed if the LVCMPCR.LVD1E and LVCMPCR.LVD2E bits (voltage detection n circuit disable; n = 1, 2) are both 0. Do not set low voltage detectors 1 and 2 to the same voltage detection level.

7.2.7 Voltage Monitor 1 Circuit Control Register 0 (LVD1CR0)

Address(es): SYSTEM.LVD1CR0 4001 E41Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	RN	RI	—	—	—	CMPE	—	RIE
Value after reset:	1	0	0	0	x	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RIE	Voltage Monitor 1 Interrupt/Reset Enable	0: Disable 1: Enable.	R/W
b1	—	Reserved	The read value is 0. The write value should be 0.	R/W

Bit	Symbol	Bit name	Description	R/W
b2	CMPE	Voltage Monitor 1 Circuit Comparison Result Output Enable	0: Disable voltage monitor 1 circuit comparison result output 1: Enable voltage monitor 1 circuit comparison result output.	R/W
b3	—	Reserved	The read value is undefined. The write value should be 1.	R/W
b5 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	RI	Voltage Monitor 1 Circuit Mode Select	0: Generate voltage monitor 1 interrupt on V_{det1} passage 1: Enable voltage monitor 1 reset when the voltage falls to and below V_{det1}.	R/W
b7	RN	Voltage Monitor 1 Reset Negate Select	0: Negate after stabilization time (tLVD1) when VCC > V_{det1} is detected 1: Negate after stabilization time (tLVD1) on assertion of the LVD1 reset.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

RIE bit (Voltage Monitor 1 Interrupt/Reset Enable)

The RIE bit enables or disables voltage monitor 1 interrupt/reset. Use this bit to ensure that neither a voltage monitor 1 interrupt nor a voltage monitor 1 reset is generated during programming or erasure of the flash memory.

RN bit (Voltage Monitor 1 Reset Negate Select)

If the RN bit is to be set to 1 (negation follows a stabilization time after assertion of the LVD1 reset signal), set the MOCOCR.MCSTP bit to 0 (the MOCO operates). In addition, if a transition to Software Standby is to be made, the only possible value for the RN bit is 0 (negation follows a stabilization time after VCC > V_{det1} is detected). Do not set the RN bit to 1 (negation follows a stabilization time after assertion of the LVD1 reset signal) when this is the case.

7.2.8 Voltage Monitor 2 Circuit Control Register 0 (LVD2CR0)

Address(es): SYSTEM.LVD2CR0 4001 E41Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	RN	RI	—	—	—	CMPE	—	RIE
Value after reset:	1	0	0	0	x	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RIE	Voltage Monitor 2 Interrupt/Reset Enable	0: Disable 1: Enable.	R/W
b1	—	Reserved	The read value is 0. The write value should be 0.	R/W
b2	CMPE	Voltage Monitor 2 Circuit Comparison Result Output Enable	0: Disable voltage monitor 2 circuit comparison result output 1: Enable voltage monitor 2 circuit comparison result output.	R/W
b3	—	Reserved	The read value is undefined. The write value should be 1.	R/W
b5 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	RI	Voltage Monitor 2 Circuit Mode Select	0: Generate voltage monitor 2 interrupt on V_{det2} passage 1: Enable voltage monitor 2 reset when the voltage falls to and below V_{det2}.	R/W
b7	RN	Voltage Monitor 2 Reset Negate Select	0: Negate after stabilization time (t_{LVD2}) when VCC > V_{det2} is detected 1: Negate after stabilization time (t_{LVD2}) on assertion of the LVD2 reset.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

RIE bit (Voltage Monitor 2 Interrupt/Reset Enable)

The RIE bit enables or disables the voltage monitor 2 interrupt/ reset. Set this bit to ensure that neither a voltage monitor

2 interrupt nor a voltage monitor 2 reset is generated during programming or erasure of the flash memory.

RN bit (Voltage Monitor 2 Reset Negate Select)

If the RN bit is to be set to 1 (negation follows a stabilization time after assertion of the LVD2 reset signal), set the MOCOCR.MCSTP bit to 0 (the MOCO operates). Additionally, if a transition to Software Standby is to be made, the only possible value for the RN bit is 0 (negation follows a stabilization time after VCC > V_{det2} is detected). Do not set the RN bit to 1 (negation follows a stabilization time after assertion of the LVD2 reset signal) when this is the case.

7.3 VCC Input Voltage Monitor

7.3.1 Monitoring V_{det0}

The voltage monitor 0 comparison results are not available for reading.

7.3.2 Monitoring V_{det1}

Table 7.2 lists the procedures for setting up monitoring against V_{det1}. After the settings are complete, results of comparison from voltage monitor 1 can be monitored using the LVD1SR.MON flag.

Table 7.2 Procedure for setting up monitoring against V_{det1}

Step		Monitoring the comparison results from voltage monitor 1
Setting the voltage detection 1 circuit	1	Set LVCMPCR.LVD1E = 0 to disable voltage detection 1 before writing to LVDLVLR register.
	2	Select the detection voltage in the LVDLVLR.LVD1LVL[4:0] bits.
	3	Set LVCMPCR.LVD1E = 1 to enable voltage detection 1.
	4	Wait for at least $t_{d(E-A)}$ for LVD operation stabilization after LVD is enabled.
Enabling output	5	Set LVD1CR0.CMPE = 1 to enable output of the results of comparison from voltage monitor 1.

7.3.3 Monitoring V_{det2}

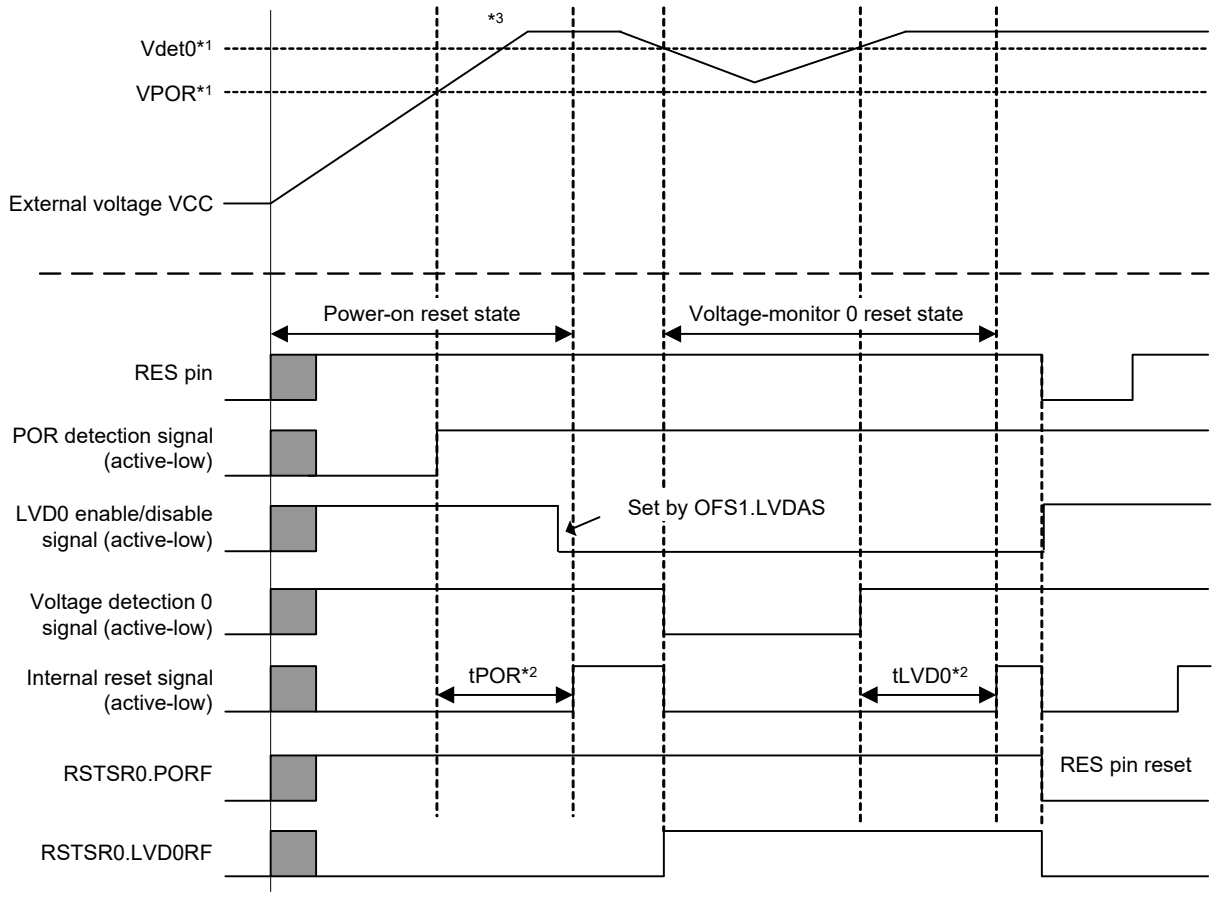
Table 7.3 lists the procedure for setting up monitoring against V_{det2}. After the settings are complete, results of comparison from voltage monitor 2 can be monitored using the LVD2SR.MON flag.

Table 7.3 Procedure for setting up monitoring against V_{det2}

Step		Monitoring the comparison results from voltage monitor 2
Setting the voltage detection 2 circuit	1	Set LVCMPCR.LVD2E = 0 to disable voltage detection 2 before writing to the LVDLVLR register.
	2	Select the detection voltage in the LVDLVLR.LVD2LVL[2:0] bits.
	3	Set LVCMPCR.LVD2E = 1 to enable the voltage detection 2 circuit.
	4	Wait for at least $t_{d(E-A)}$ for LVD operation stabilization after LVD is enabled.
Enabling output	5	Set LVD2CR0.CMPE = 1 to enable output of the results of comparison from voltage monitor 2.

7.4 Reset from Voltage Monitor 0

When using the reset from voltage monitor 0, clear the OFS1.LVDAS bit to 0 to enable the voltage monitor 0 reset after a reset. However, at boot mode, the reset from voltage monitor 0 is disabled regardless of the value of the OFS1.LVDAS bit. Figure 7.4 shows an example operation of a voltage monitor 0 reset.



Note: For details on the electrical characteristics, see section 46, Electrical Characteristics.
Note 1. V_{POR} indicates the detection level for a power-on reset and V_{det0} indicates the detection level for a voltage monitor 0 reset.
Note 2. t_{POR} indicates the period of a power-on reset and t_{LVD0} indicates the period of a voltage monitor 0 reset.
Note 3. At power-on, raise VCC to the minimum guaranteed voltage before the POR reset is released.

Figure 7.4 Example of voltage monitor 0 reset operation

7.5 Interrupt and Reset from Voltage Monitor 1

An interrupt or reset can be generated in response to the results of comparison by the voltage monitor 1 circuit.

Table 7.4 shows the procedure for setting bits related to the voltage monitor 1 interrupt/reset so that voltage monitoring occurs. Table 7.5 shows the procedure for setting bits related to the voltage monitor 1 interrupt/reset so that voltage monitoring stops. Figure 7.5 shows an example of operations for a voltage monitor 1 interrupt. For the operation of the voltage monitor 1 reset, see Figure 5.2 in section 5, Resets.

When using the voltage monitor 1 circuit in Software Standby mode, set up the circuit using the following procedures.

(1) Setting in Software Standby mode

- When VCC > V_{det1} is detected, negate the voltage monitor 1 reset signal (LVD1CR0.RN = 0) following a stabilization time.

Table 7.4 Procedure for setting bits related to the voltage monitor 1 interrupt and voltage monitor 1 reset so that voltage monitoring occurs

Step		Voltage monitor 1 interrupt (voltage monitor 1 ELC event output)	Voltage monitor 1 reset
Setting the voltage detection 1 circuit	1	Set LVCMPCR.LVD1E = 0 to disable voltage detection 1 before writing to the LVDLVLR register.	
	2	Select the detection voltage by setting the LVDLVLR.LVD1LVL[4:0] bits.	
	3	Set LVCMPCR.LVD1E = 1 to enable the voltage detection 1 circuit.	
	4	Wait for at least td(E-A) for the LVD operation stabilization time after LVD is enabled.*1	
Setting the voltage monitor 1 interrupt/ reset	5	Set LVD1CR0.RI = 0 to select the voltage monitor 1 interrupt.	• Set LVD1CR0.RI = 1 to select the voltage monitor 1 reset • Select the type of the reset negation by setting the LVD1CR0.RN bit.
	6	• Select the timing of interrupt requests by setting the LVD1CR1.IDTSEL[1:0] bits • Select the type of interrupt by setting the LVD1CR1.IRQSEL bit.	—
Enabling output	7	Set LVD1SR.DET = 0.	
	8	Set LVD1CR0.RIE = 1 to enable the voltage monitor 1 interrupt or reset.*2	
	9	Set LVD1CR0.CMPE = 1 to enable output of the results of comparison from voltage monitor 1.	

Note 1. Steps 5 to 8 can be performed during the wait time of step 4. For details on td(E-A), see section 46, Electrical Characteristics.
Note 2. Step 8 is not required if only the ELC event signal is to be output.

Table 7.5 Procedure for setting bits related to the voltage monitor 1 interrupt and voltage monitor 1 reset so that voltage monitoring stops

Step		Voltage monitor 1 interrupt (voltage monitor 1 ELC event output), voltage monitor 1 reset
Settings to stop enabling of output	1	Set LVD1CR0.CMPE = 0 to disable output of the results of comparison from voltage monitor 1.
	2	Set LVD1CR0.RIE = 0 to disable the voltage monitor 1 interrupt or reset.*1
Stopping the voltage detection 1 circuit	3	Set LVCMPCR.LVD1E = 0 to disable the voltage detection 1 circuit.

Note 1. Step 2 is not required if only the ELC event signal is to be output.

If the voltage monitor 1 interrupt or reset setting is to be made again after it is used and stopped once, omit the following steps in the procedures for stopping and setting, depending on the conditions:

- Setting or stopping the voltage detection 1 circuit is not required if the settings for the voltage detection 1 circuit do not change
- Setting the voltage monitor 1 interrupt or reset is not required if the settings for the voltage monitor 1 interrupt or reset do not change.

Figure 7.5 shows an example of the voltage monitor 1 interrupt operation.

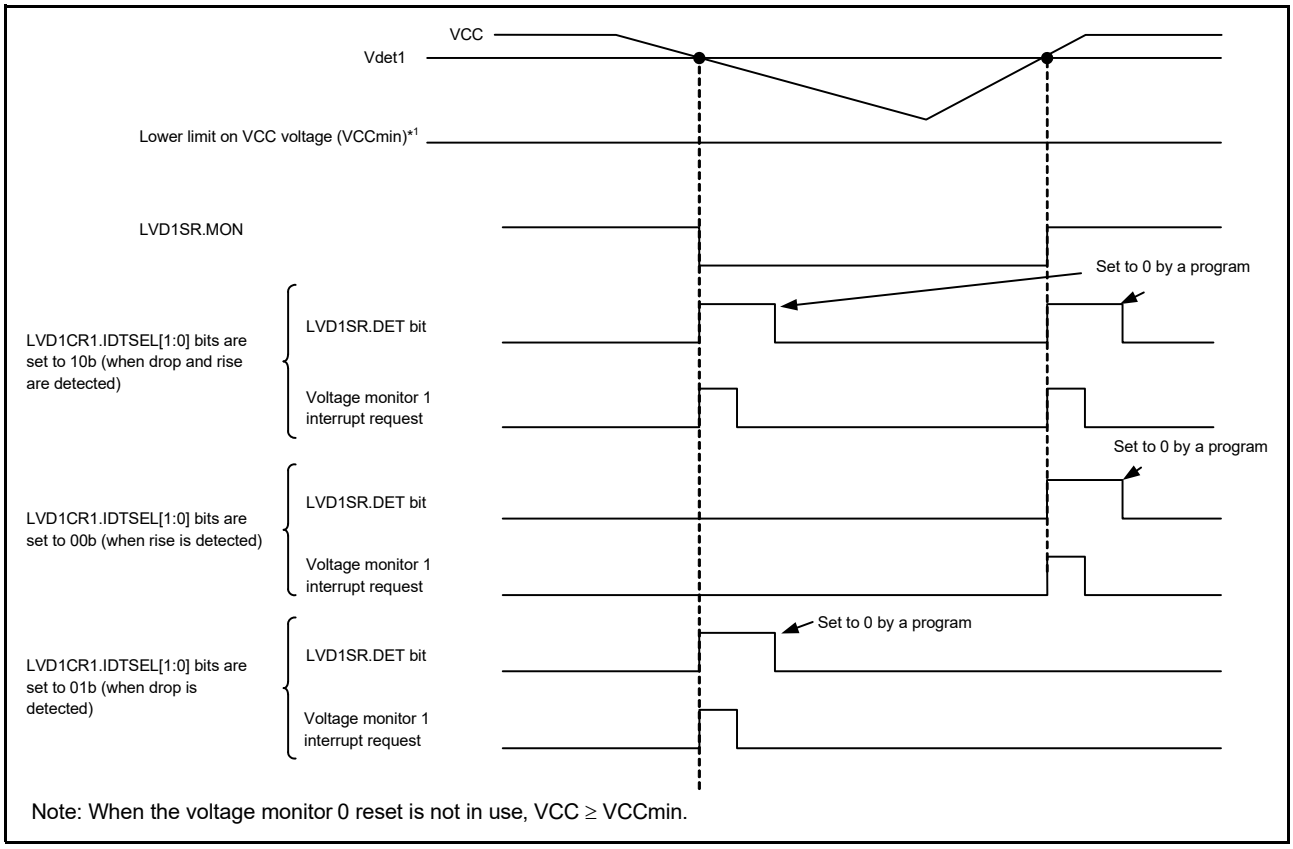


Figure 7.5 Voltage monitor 1 interrupt operation example

7.6 Interrupt and Reset from Voltage Monitor 2

An interrupt or reset can be generated in response to the results of comparison by the voltage monitor 2 circuit.

Table 7.6 shows the procedures for setting bits related to the voltage monitor 2 interrupt and voltage monitor 2 reset so that voltage monitor operates. Table 7.7 shows the procedure for setting bits related to the voltage monitor 2 interrupt and voltage monitor 2 reset so that voltage monitor stops. Figure 7.6 shows an example of operations of the voltage monitor 2 interrupt. For the operation of the voltage monitor 2 reset, see Figure 5.2 in section 5, Resets.

When using the voltage monitor 2 circuit in Software Standby mode, set the voltage monitor 2 circuit using the following procedures:

(1) Setting in Software Standby mode

- When VCC > V_{det2} is detected, clear the LVDD2CR0.RN bit (LVD2CR0.RN = 0) following a stabilization time.

Table 7.6 Procedure for setting bits related to voltage monitor 2 interrupt and voltage monitor 2 reset so that voltage monitor operates (1 of 2)

Step		Voltage monitor 2 interrupt (voltage monitor 2 ELC event output)	Voltage monitor 2 reset
Setting the voltage detection 2 circuit	1	Set LVCMPCR.LVD2E = 0 to disable voltage detection 2 before writing to the LVDLVLR register.	
	2	Select the detection voltage by setting the LVDLVLR.LVD2LVL[2:0] bits.	
	3	Set LVCMPCR.LVD2E = 1 to enable the voltage detection 2 circuit.	
	4	Wait for at least $t_{d(E-A)}$ for the LVD operation stabilization time after LVD is enabled.*1	

Table 7.6 Procedure for setting bits related to voltage monitor 2 interrupt and voltage monitor 2 reset so that voltage monitor operates (2 of 2)

Step		Voltage monitor 2 interrupt (voltage monitor 2 ELC event output)	Voltage monitor 2 reset
Setting the voltage monitor 2 interrupt or reset	5	Set LVD2CR0.RI = 0 to select the voltage monitor 2 interrupt.	• Set LVD2CR0.RI = 1 to select the voltage monitor 2 reset • Select the type of the reset negation by setting the LVD2CR0.RN bit.
	6	• Select the timing of interrupt requests by setting the LVD2CR1.IDTSEL[1:0] bits • Select the type of interrupt by setting the LVD2CR1.IRQSEL bit.	—
Enabling output	7	Set LVD2SR.DET = 0.	
	8	Set LVD2CR0.RIE = 1 to enable the voltage monitor 2 interrupt or reset.*2	
	9	Set LVD2CR0.CMPE = 1 to enable output of the results of comparison by voltage monitor 2.	

Note 1. Steps 5 to 8 can be performed during the waiting time of step 4. For details on td(E-A), see section 46, Electrical Characteristics.

Note 2. Step 8 is not required if only the ELC event signal is to be output.

Table 7.7 Procedure for setting bits related to voltage monitor 2 interrupt and voltage monitor 2 reset so that voltage monitor stops

Step		Voltage monitor 2 interrupt (voltage monitor 2 ELC event output), voltage monitor 2 reset
Settings to stop enabling of output	1	Set LVD2CR0.CMPE = 0 (disabling output of the results of comparison by voltage monitor 2).
	2	Set LVD2CR0.RIE = 0 (disabling the voltage monitor 2 interrupt or reset).*1
Stopping the voltage detection 2 circuit	3	Set LVCMPCR.LVD2E = 0 (disabling the voltage detection 2 circuit).

Note 1. Step 2 is not required if only the ELC event signal is to be output.

If the voltage monitor 2 interrupt or reset setting is to be made again after it is used and stopped once, omit the following steps in the procedures for stopping and setting, depending on the conditions:

- Setting or stopping the voltage detection 2 circuit is not required if the settings for the voltage detection 2 circuit do not change
- Setting the voltage monitor 2 interrupt or reset is not required if the settings for the voltage monitor 2 interrupt/reset do not change.

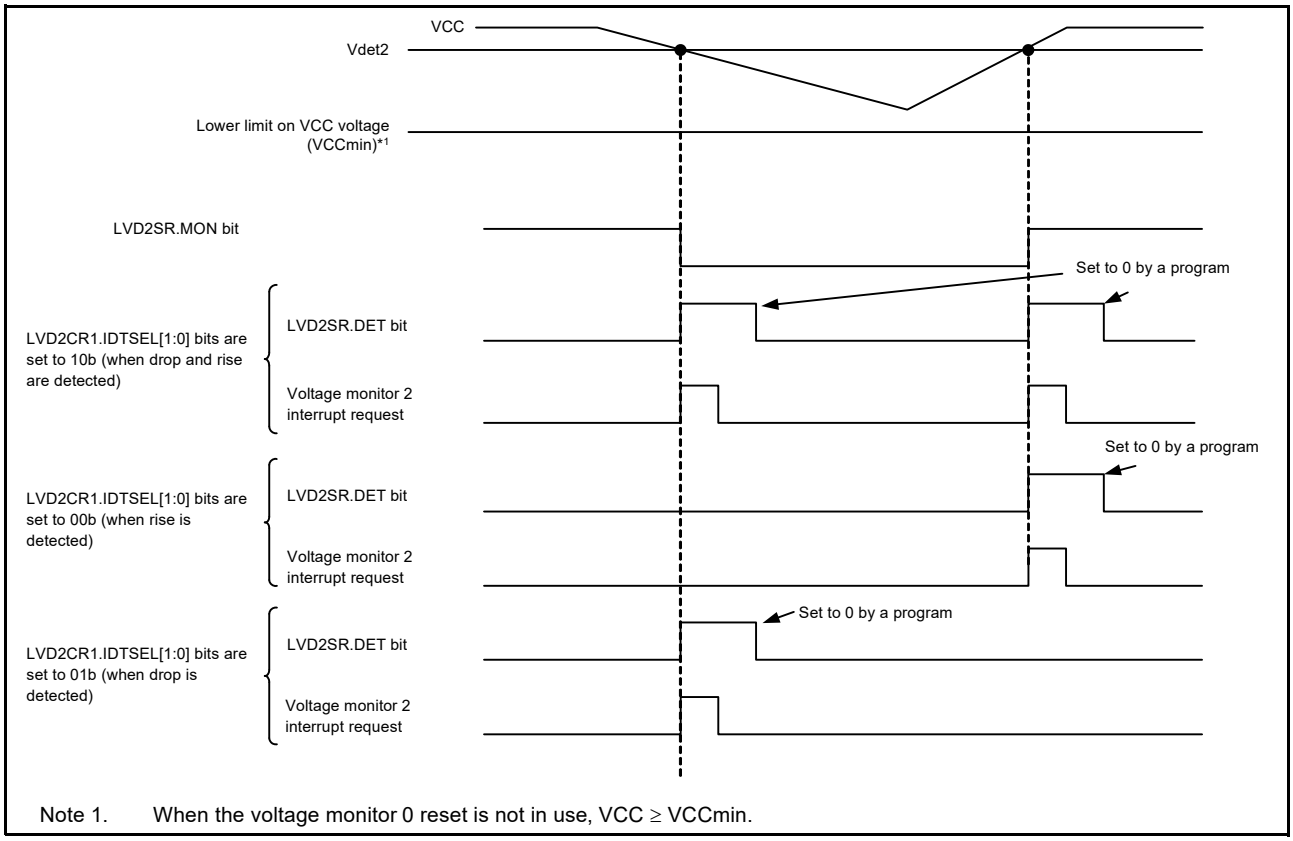


Figure 7.6 Example of voltage monitor 2 interrupt operation

7.7 Event Link Output

The LVD can output the event signals to the Event Link Controller (ELC).

The LVD outputs the event signal when it detects that the voltage has passed the V_{det1} voltage while both the voltage detection 1 circuit and the voltage monitor 1 circuit comparison result output are enabled.

The LVD outputs the event signal when it detects that the voltage has passed the V_{det2} voltage while both the voltage detection 2 circuit and the voltage monitor 2 circuit comparison result output are enabled.

When enabling the event link output function of the LVD, you must enable the LVD before enabling the LVD event link function of the ELC. To stop the event link output function of the LVD, you must stop the LVD before disabling the LVD event link function of the ELC.

7.7.1 Interrupt Handling and Event Linking

The LVD provides bits to individually enable or disable the voltage monitor 1 and 2 interrupts. When an interrupt source is generated and the interrupt is enabled by the interrupt enable bit, the interrupt signal (LVD1CR0.RIE and LVD2CR0.RIE) is output to the CPU.

In contrast, an event link signal is output as the event signal to the other module through the ELC, as soon as an interrupt source is generated, regardless of the state of the interrupt enable bit.

It is possible to output voltage monitor 1 and 2 interrupts in Software Standby mode. The event signals for the ELC in Software Standby mode are output as follows:

- When a V_{det1} or V_{det2} passage event is detected in Software Standby mode, event signals are not generated for the ELC because the clock is not supplied in Software Standby mode. Because the V_{det1} or V_{det2} passage detection flags are saved, when the clock supply resumes after returning from Software Standby mode, the event signals for the ELC are output based on the state of the V_{det1} or V_{det2} detection flags.

8. Clock Generation Circuit

8.1 Overview

The MCU provides a clock generation circuit.

Table 8.1 and Table 8.2 list the clock generation circuit specifications. Figure 8.1 shows a block diagram, and Table 8.3 lists the I/O pins.

Table 8.1 Clock generation circuit specifications for the clock sources

Clock source	Description	Specification
Main clock oscillator (MOSC)	Resonator frequency	• 1 MHz to 20 MHz*1
	External clock input frequency	Up to 20 MHz*1
	External resonator or additional circuit: ceramic resonator, crystal	Available
	Connection pins: EXTAL, XTAL	
	Drive capability switching	
	Oscillation stop detection function	
Sub-clock oscillator (SOSC)	Resonator frequency	32.768 kHz
	External resonator or additional circuit: crystal resonator	Available
	Connection pins: XCIN, XCOUT	
	Drive capability switching	
High-speed on-chip oscillator (HOCO)	Oscillation frequency	24, 32, 48, 64 MHz
	User trimming	Available
Middle-speed on-chip oscillator (MOCO)	Oscillation frequency	8 MHz
	User trimming	Available
Low-speed on-chip oscillator (LOCO)	Oscillation frequency	32.768 kHz
	User trimming	Available
IWDT-dedicated on-chip oscillator (IWDTLOCO)	Oscillation frequency	15 kHz
	User trimming	Not available
External clock input for SWD (SWCLK)	Input clock frequency	Up to 12.5 MHz

Note 1. The frequency depends on the supply voltage. See the table of Clock timing in the Electrical Characteristics chapter for more information.

Table 8.2 Clock generation circuit specifications for the internal clocks (1 of 2)

Parameter	Clock source	Clock supply	Specification
System clock (ICLK)	MOSC/SOSC/HOCO/ MOCO/LOCO	CPU, DTC, FLASH, SRAM, FlashIF	1 MHz to 32 MHz (P/E) Up to 32 MHz Division ratios: 1, 2, 4, 8, 16, 32, 64
Peripheral module clock B (PCLKB)	MOSC/SOSC/HOCO/ MOCO/LOCO	Peripheral module (CAC, ELC, I/O Ports, KINT, POEG, GPT, PWM Delay Generation Circuit, AGT, RTC, WDT, IWDT, USBFS, SCI, DALI, IIC, CAN, SPI, CRC, ADC14, DAC8, OPAMP, ACMPHS, ACMPLP, CTSU, DOC, AES, and TRNG)	Up to 32 MHz Division ratios:1, 2, 4, 8, 16, 32, 64
Peripheral module clock D (PCLKD)	MOSC/SOSC/HOCO/ MOCO/LOCO	Peripheral module (GPT count clock, PWM Delay Generation Circuit, ADC14 conversion clock)	Up to 64 MHz Division ratios: 1, 2, 4, 8, 16, 32, 64
USB clock (UCLK)	HOCO	USBFS	48 MHz

Table 8.2 Clock generation circuit specifications for the internal clocks (2 of 2)

Parameter	Clock source	Clock supply	Specification
CAN clock (CANMCLK)	MOSC	CAN	1 MHz to 20 MHz
AGT clock (AGTSCLK/AGTLCLK)	SOSC/LOCO	AGT	32.768 kHz
CAC Main clock (CACMCLK)	MOSC	CAC	Up to 20 MHz
CAC Sub clock (CACSCLK)	SOSC	CAC	32.768 kHz
CAC LOCO clock (CACLCLK)	LOCO	CAC	32.768 kHz
CAC MOCO clock (CACMOCLK)	MOCO	CAC	8 MHz
CAC HOCO clock (CACHCLK)	HOCO	CAC	24, 32, 48, 64 MHz
CAC IWDTLOCO clock (CACILCLK)	IWDTLOCO	CAC	15 kHz
RTC clock (RTCSCLK/ RTCLCLK)	SOSC/LOCO	RTC	32.768 kHz
IWDT clock (IWDTCLK)	IWDTLOCO	IWDT	15 kHz
SysTick Timer clock (SYSTICCLK)	LOCO	SysTick Timer	32.768 kHz
Clock/buzzer output (CLKOUT)	MOSC/SOSC/LOCO/ MOCO/HOCO	CLKOUT pin	Up to 16 MHz Division ratios: 1, 2, 4, 8, 16, 32, 64, 128
Serial wire clock (SWCLK)	SWCLK pin	OCD	Up to 12.5 MHz

Note: Restrictions on setting clock frequency: ICLK ≥ PCLKB, PCLKD ≥ PCLKB
Restrictions on clock frequency ratio: (N: integer, and up to 64)
ICLK:PCLKB = N: 1, ICLK:PCLKD = N:1 or 1:N

Note: Minimum ICLK frequency is 1 MHz in Programming/Erasure (P/E) mode.

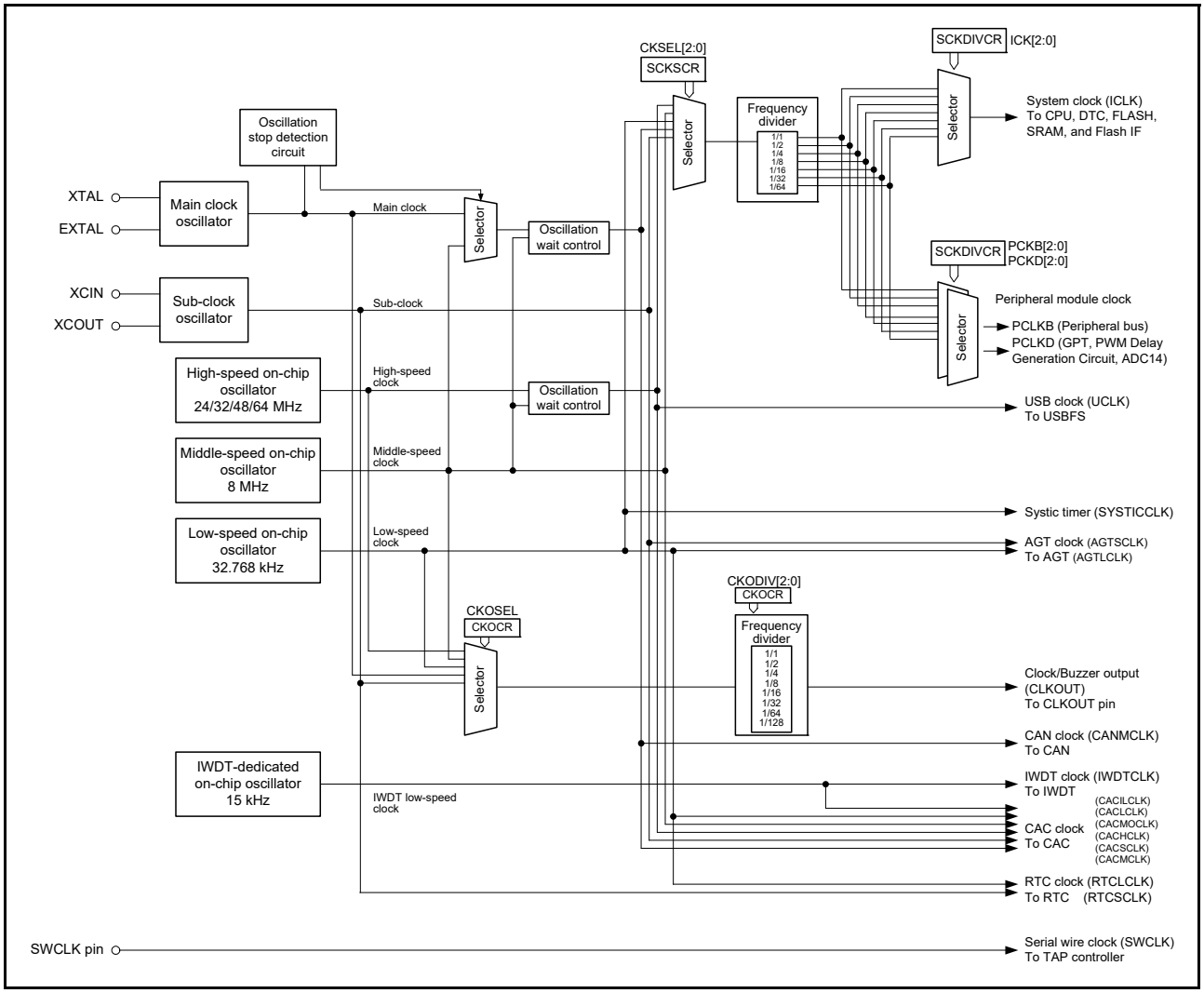


Figure 8.1 Clock generation circuit block diagram

Table 8.3 Clock generation circuit input/output pins

Pin name	I/O	Description
XTAL	Output	These pins are used to connect a crystal resonator. The EXTAL pin can also be used to input an external clock. For details, see section 8.3.2, External Clock Input.
EXTAL	Input	
XCIN	Input	These pins are used to connect to a 32.768-kHz crystal resonator
XCOUT	Output	
CLKOUT	Output	This pin is used to output the CLKOUT/BUZZER clock
SWCLK	Input	This pin is used to input from the SWD

8.2 Register Descriptions

8.2.1 System Clock Division Control Register (SCKDIVCR)

Address(es): SYSTEM.SCKDIVCR 4001 E020h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	ICK[2:0]			—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	PCKB[2:0]			—	—	—	—	—	PCKD[2:0]		
Value after reset:	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	PCKD[2:0]	Peripheral Module Clock D (PCLKD) Select*2	b2 b0 0 0 0: ×1/1 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 1 0 1: ×1/32 1 1 0: ×1/64. Other settings are prohibited.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b10 to b8	PCKB[2:0]	Peripheral Module Clock B (PCLKB) Select*1	b10 b8 0 0 0: ×1/1 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 1 0 1: ×1/32 1 1 0: ×1/64. Other settings are prohibited.	R/W
b23 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b26 to b24	ICK[2:0]	System Clock (ICLK) Select *1, *2	b26 b24 0 0 0: ×1/1 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 1 0 1: ×1/32 1 1 0: ×1/64. Other settings are prohibited.	R/W
b31 to b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The association between the frequencies of the system clock (ICLK) and the peripheral module clock (PCLKB) should be ICLK:PCLKB = N:1 (N: integer)
If a setting is written where ICLK < PCLKB, the write is ignored.

Note 2. The association between the frequencies of the system clock (ICLK) and the peripheral module clock (PCLKD) should be ICLK:PCLKD = N:1 or 1:N (N: integer).

The SCKDIVCR register selects the frequencies of the system clock (ICLK) and peripheral module clock (PCLKB, PCLKD).

PCKD[2:0] bits (Peripheral Module Clock D (PCLKD) Select)

The PCKD[2:0] bits select the frequency of peripheral module clock D (PCLKD).

PCKB[2:0] bits (Peripheral Module Clock B (PCLKB) Select)

The PCKB[2:0] bits select the frequency of peripheral module clock B (PCLKB).

ICK[2:0] bits (System Clock (ICLK) Select)

The ICK[2:0] bits select the frequency of the system clock for the CPU and DTC.

8.2.2 System Clock Source Control Register (SCKSCR)

Address(es): SYSTEM.SCKSCR 4001 E026h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	CKSEL[2:0]		
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b2 to b0	CKSEL[2:0]	Clock Source Select	b2 b0 0 0 0: HOCO 0 0 1: MOCO 0 1 0: LOCO 0 1 1: Main clock oscillator (MOSC) 1 0 0: Sub-clock oscillator (SOSC). Other settings are prohibited.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The SCKSCR register selects the clock source for the system clock.

CKSEL[2:0] bits (Clock Source Select)

The CKSEL[2:0] bits select the source for the following modules:

- System clock (ICLK)
- Peripheral module clocks (PCLKB and PCLKD).

The bits select from one of the following sources:

- Low-speed on-chip oscillator (LOCO)
- Middle-speed on-chip oscillator (MOCO)
- High-speed on-chip oscillator (HOCO)
- Main clock oscillator (MOSC)
- Sub-clock oscillator (SOSC).

Transitions to clock sources that are not in operation are prohibited.

8.2.3 Main Clock Oscillator Control Register (MOSCCR)

Address(es): SYSTEM.MOSCCR 4001 E032h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	MOSTP
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b0	MOSTP	Main Clock Oscillator Stop	0: Operate the main clock oscillator*1 1: Stop the main clock oscillator.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. MOMCR register must be set before setting MOSTP to 0.

The MOSCCR register controls the main clock oscillator.

MOSTP bit (Main Clock Oscillator Stop)

The MOSTP bit starts or stops the main clock oscillator.

The main clock oscillator can be started by setting the MOSTP bit to operate. When changing the value of the MOSTP bit, execute subsequent instructions only after reading the bit to check that the value is updated.

When using the main clock, the Main Clock Oscillator Mode Oscillation Control Register (MOMCR) and the Main Clock Oscillator Wait Control Register (MOSCWTCR) must be set before setting MOSTP to 0. When the MOSCCR.MOSTP bit is modified for the main clock to run, only use the main clock after confirming that the OSCSF.MOSCSF bit is set to 1.

A fixed time is required for oscillation to become stable after setting the main clock oscillator. A fixed wait time is also required for oscillation to stop after stopping the main clock oscillator.

The following restrictions apply when starting and stopping operation:

- After stopping the main clock oscillator, confirm that the OSCSF.MOSCSF bit is 0 before restarting the main clock oscillator
- Confirm that the main clock oscillator operates and that the OSCSF.MOSCSF bit is 1 before stopping the main clock oscillator
- Regardless of whether the main clock oscillator is selected as the system clock, confirm that the OSCSF.MOSCSF bit is set to 1 before executing a WFI instruction to place the MCU in Software Standby mode
- When a transition to Software Standby mode is to follow the setting to stop the main clock oscillator, confirm that the OSCSF.MOSCSF bit is set to 0 before executing the WFI instruction.

Writing 1 to MOSTP is prohibited under the following condition:

- SCKSCR.CKSEL[2:0] = 011b (System clock source = MOSC).

8.2.4 Sub-Clock Oscillator Control Register (SOSCCR)

Address(es): SYSTEM.SOSCCR 4001 E480h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	SOSTP
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b0	SOSTP	Sub-Clock Oscillator Stop	0: Operate the sub-clock oscillator*1 1: Stop the sub-clock oscillator.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The SOMCR register must be set before setting SOSTP to 0.

The SOSCCR register controls the sub-clock oscillator.

SOSTP bit (Sub-Clock Oscillator Stop)

The SOSTP bit starts or stops the sub-clock oscillator.

When changing the value of the SOSTP bit, execute subsequent instructions after reading the bit and checking that its value is updated. When using the sub-clock oscillator as the source for a peripheral module, for example the RTC, use the SOSTP bit.

When using the sub-clock oscillator, set the Sub-Clock Oscillator Mode Control Register (SOMCR) before setting SOSTP to 0. After setting SOSTP to 0, use the sub-clock oscillator only after the sub-clock oscillation stabilization wait time (tSUBOSC) elapses. A fixed time for stabilization is required for oscillation to become stable after selecting the

sub-clock operation with the SOSTP bit. A fixed time is also required for oscillation to actually stop after setting the SOSTP bit.

The following restrictions apply when starting and stopping the operation:

- When restarting the sub-clock oscillator after it stops, allow an interval of at least 5 SOSC clock cycles for it to remain stopped
- Confirm that the sub-clock oscillator is stable when stopping the sub-clock oscillator
- Regardless of whether the sub-clock oscillator is selected as the system clock, ensure that the oscillation by the sub-clock oscillation is stable before executing a WFI instruction to place the MCU in Software Standby mode
- When a transition to Software Standby mode is to follow the setting to stop the sub-clock oscillator, wait for at least 3 SOSC clock cycles after setting the sub-clock oscillator to stop and before executing the WFI instruction.

Writing 1 to SOSTP is prohibited under the following condition:

- SCKSCR.CKSEL[2:0] = 100b (system clock source = SOSC).

8.2.5 Low-Speed On-Chip Oscillator Control Register (LOCOCR)

Address(es): SYSTEM.LOCOCR 4001 E490h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	LCSTP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	LCSTP	LOCO Stop	0: Operate the LOCO clock 1: Stop the LOCO clock.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The LOCOCR register controls the LOCO.

LCSTP bit (LOCO Stop)

The LCSTP bit starts or stops the LOCO.

After the LCSTP bit is modified to 0 to operate the LOCO clock, only use the LOCO after the LOCO clock-oscillation stabilization wait time (tLOCO) elapses. A fixed time for stabilization of oscillation is required for oscillation to become stable after setting the LOCO clock to start operation. A fixed time is also required for oscillation to stop after setting the oscillator.

The following restrictions apply when starting and stopping operation:

- When restarting the LOCO after it stops, allow an interval of at least 5 LOCO clock cycles for it to remain stopped
- Ensure that LOCO oscillation is stable before stopping the LOCO clock
- Regardless of whether the LOCO is selected as the system clock, ensure that LOCO oscillation is stable before executing a WFI instruction to place the MCU in Software Standby mode
- When a transition to Software Standby mode is to follow the setting to stop the LOCO clock, wait for at least 3 LOCO cycles before executing the WFI instruction.

Writing 1 to LCSTP is prohibited under the following condition:

- SCKSCR.CKSEL[2:0] = 010b (system clock source = LOCO).

8.2.6 High-Speed On-Chip Oscillator Control Register (HOCOCR)

Address(es): SYSTEM.HOCOCR 4001 E036h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	HCSTP
Value after reset:	0	0	0	0	0	0	0	0/1*1

Bit	Symbol	Bit name	Description	R/W
b0	HCSTP	HOCO Stop	0: Operate the HOCO clock*2, *3 1: Stop the HOCO clock.	R/W*Note:
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Writing to OPCCR.OPCM[1:0] is prohibited while HOCOCR.HCSTP = 0 and OSCSF.HOCOSF = 0 (HOCO is in stabilization wait counting).
Note: Writing HCSTP is prohibited while OPCCR.OPCMTSF = 1 or SOPCCR.SOPCMTSF = 1 (during transition of operating power control mode) or FLSTOP.CFLSTOPF = 1 (during transition of flash).
Note 1. The HCSTP bit value after a reset is 0 when the OFS1.HOCOEN bit is 0. It is 1 when the OFS1.HOCOEN bit is 1.
Note 2. If the operating frequency of HOCO is 48 MHz, VCC must be more than 1.8 V (VCC ≥ 1.8 V) when operating the HOCO.
If the operating frequency of HOCO is 64 MHz, VCC must be more than 2.4 V (VCC ≥ 2.4 V) when operating the HOCO.
Note 3. If you are using the HOCO (HCSTP = 0), set the OFS1.HOCOFRQ1[2:0] bits to an optimum value.
During low-voltage mode, HOCOCR.HCSTP must always be 0.

The HOCOCR register controls the HOCO.

HCSTP bit (HOCO Stop)

The HCSTP bit starts or stops the HOCO. For the HOCO to operate, the High-Speed On-Chip Oscillator Wait Control Register (HOCOWTCR) must also be set.

After the HCSTP bit setting is modified to run the HOCO, confirm that the OSCSF.HOCOSF is set to 1 before using the clock. When OFS1.HOCOEN is set to 0, confirm that OSCSF.HOCOSF is set to 1 before using the HOCO clock. A fixed time for stabilization is required for oscillation to become stable after setting the HOCO operation. A fixed wait time is also required for oscillation to actually stop after setting the HOCO clock to stop.

The following limitations apply when starting and stopping the operation:

- After stopping the HOCO, confirm that the OSCSF.HOCOSF bit is 0 before restarting the HOCO
- Confirm that the HOCO operates and that the OSCSF.HOCOSF bit is 1 before stopping the HOCO
- Regardless of whether the HOCO clock is selected as the system clock, confirm that the OSCSF.HOCOSF bit is set to 1 before executing a WFI instruction to place the MCU in Software Standby while HOCOCR. HCSTP bit is 0
- When a transition to Software Standby mode is to follow the setting of the HOCO to stop, confirm that the OSCSF.HOCOSF bit is set to 0 after setting the HOCO and before executing the WFI instruction.

Writing 1 to HCSTP is prohibited under the following condition:

- SCKSCR.CKSEL[2:0] = 000b (system clock source = HOCO).

8.2.7 Middle-Speed On-Chip Oscillator Control Register (MOCOCR)

Address(es): SYSTEM.MOCOCR 4001 E038h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	MCSTP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	MCSTP	MOCO Stop	0: Operate MOCO 1: Stop MOCO.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The MOCOCR register controls the MOCO.

MCSTP bit (MOCO Stop)

The MCSTP bit starts or stops the MOCO.

After setting MCSTP to 0, use the MOCO clock only after the MOCO clock oscillation stabilization time (tMOCOWT) elapses. A fixed time for stabilization of oscillation is required after setting MCSTP to 0. A fixed time is also required for oscillation to stop after setting MCSTP to 1.

The following limitations apply when starting and stopping the oscillator:

- When restarting the MOCO clock after it has been stopped, allow a stop interval of at least 5 MOCO clock cycles for it to remain stopped
- Ensure that MOCO oscillation is stable when setting the MOCO clock to stop
- Regardless of whether the MOCO clock is selected as the system clock, ensure that MOCO oscillation is stable before executing a WFI instruction to place the MCU in Software Standby mode
- When a transition to Software Standby mode is to follow the setting to stop the MOCO clock, wait for at least 3 MOCO clock cycles before executing the WFI instruction.

Writing 1 to MCSTP is prohibited under the following condition:

- SCKSCR.CKSEL[2:0] = 001b (system clock source = MOCO).

Writing 1 to the MCSTP bit (stopping the MOCO) is prohibited if oscillation stop detection is enabled in the Oscillation Stop Detection Enable bit (OSTDCR.OSTDE) in the Oscillation Stop Detection Control Register.

Because the MOCO clock is used to measure the wait time for other oscillators, the MOCO clock oscillates when the wait time for other oscillators is measured, regardless of the setting of MOCOCR.MCSTP. The MOCO clock might be unintentionally supplied even when the MCSTP is set to stop.

8.2.8 Oscillation Stabilization Flag Register (OSCSF)

Address(es): SYSTEM.OSCSF 4001 E03Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	MOSC SF	—	—	HOCO SF
Value after reset:	0	0	0	0	0	0	0	0/1*1

Bit	Symbol	Bit name	Description	R/W
b0	HOCOSF	HOCO Clock Oscillation Stabilization Flag	0: The HOCO clock is stopped or is not stable yet 1: The HOCO clock is stable, so is available for use as the system clock.	R

Bit	Symbol	Bit name	Description	R/W
b2, b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3	MOSCSF	Main Clock Oscillation Stabilization Flag	0: The main clock oscillator is stopped (MOSTP = 1) or is not stable yet*2 1: The main clock oscillator is stable, so is available for use as the system clock.	R
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The value after reset depends on the OFS1.HOCOEN bit setting.
When OFS1.HOCOEN = 1, the value after reset of HOCOSF is 0.
When OFS1.HOCOEN = 0, the HOCOSF value is set to 0 immediately after reset is released, and the HOCOSF value is set to 1 after the HOCO oscillation stabilization wait time elapses.

Note 2. An appropriate value is set in the Wait Control register for the given oscillator. If the wait time value is not sufficient, the oscillation stabilization flag is set to 1 and supply of the clock signal to the internal circuits starts before oscillation is stable.

The OSCSF register contains flags to indicate the states of operation of the counters in the oscillation stabilization wait circuits for the individual oscillators.

After oscillation starts, these counters measure the wait time until each oscillator output clock is supplied to the internal circuits. An overflow of a counter indicates that the clock supply is stable and available for the associated circuit.

HOCOSF flag (HOCO Clock Oscillation Stabilization Flag)

The HOCOSF flag indicates the operating state of the counter that measures the wait time for the high-speed clock oscillator (HOCO). When OFS1.HOCOEN is set to 0, confirm that OSCSF.HOCOSF is set to 1 before using the HOCO clock.

[Setting condition]

- After the HOCO clock stops and the HOCOCR.HCSTP bit is set to 0, supply of the high-speed clock in the MCU starts after the middle-speed clock cycles set in the HOCOWTCR[2:0] bits elapse.

[Clearing condition]

- When the high-speed clock oscillator is operating and then is deactivated because the HOCOCR.HCSTP bit is set to 1.

MOSCSF flag (Main Clock Oscillation Stabilization Flag)

The MOSCSF flag indicates the operating state of the counter that measures the wait time for the main clock oscillator.

[Setting condition]

- After the main clock oscillator stops and the MOSCCR.MOSTP bit is set to 0, supply of the main clock in the MCU starts after the middle-speed clock cycles set in the MOSCWTCR.MSTS[3:0] bits elapse.

[Clearing condition]

- When the main clock oscillator is operating and then is deactivated because the MOSCCR.MOSTP bit is set to 1.

8.2.9 Oscillation Stop Detection Control Register (OSTDCR)

Address(es): SYSTEM.OSTDCR 4001 E040h

	b7	b6	b5	b4	b3	b2	b1	b0
	OSTDE	—	—	—	—	—	—	OSTDIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	OSTDIE	Oscillation Stop Detection Interrupt Enable	0: Disable oscillation stop detection interrupt (do not notify the POEG) 1: Enable oscillation stop detection interrupt (notify the POEG).	R/W

Bit	Symbol	Bit name	Description	R/W
b6 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	OSTDE	Oscillation Stop Detection Function Enable	0: Disable oscillation stop detection function 1: Enable oscillation stop detection function.	R/W

The OSTDCR register controls the oscillation stop detection function.

OSTDIE bit (Oscillation Stop Detection Interrupt Enable)

The OSTDIE bit enables the oscillation stop detection function interrupt. It also controls whether oscillation stop detection is reported to the POEG.

If the Oscillation Stop Detection Flag in the Oscillation Stop Detection Status Register (OSTDSR.OSTDF) requires clearing, set the OSTDIE bit to 0 before OSTDF is set to 0. Wait for at least 2 PCLKB cycles before setting the OSTDIE bit to 1. Depending on the number of cycles required to read a given I/O register, a wait time longer then 2 PCLKB cycles might be required.

OSTDE bit (Oscillation Stop Detection Function Enable)

The OSTDE bit enables the oscillation stop detection function.

When this bit is 1 (oscillation stop detection function enabled), the MOCO Stop bit (MOCOCR.MCSTP) is set to 0 and the MOCO operation starts. The MOCO clock cannot be stopped while the oscillation stop detection function is enabled. Writing 1 to the MOCOCR.MCSTP bit (MOCO stopped) is invalid.

When the Oscillation Stop Detection Flag in the Oscillation Stop Detection Status Register (OSTDSR.OSTDF) is 1 (main clock oscillation stop detected), writing 0 to the OSTDE bit is invalid.

The OSTDE bit must be set to 0 before transitioning to Software Standby mode. To transition to Software Standby mode, first set the OSTDE bit to 0, and then execute the WFI instruction.

The following restrictions apply when using the oscillation stop detection function:

- In low-speed mode, selecting division by 1, 2, 4, 8 for ICLK, PCLKB, and PCLKD is prohibited
- In low-voltage mode, selecting division by 1, 2 for ICLK, PCLKB, and PCLKD is prohibited.

8.2.10 Oscillation Stop Detection Status Register (OSTDSR)

Address(es): SYSTEM.OSTDSR 4001 E041h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	OSTDF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	OSTDF	Oscillation Stop Detection Flag	0: Main clock oscillation stop not detected 1: Main clock oscillation stop detected.	R(/W)*1
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R

Note 1. This bit can only be set to 0.

The OSTDSR register indicates the stop detection status of the main clock oscillator.

OSTDF flag (Oscillation Stop Detection Flag)

The OSTDF flag indicates the main clock oscillator status. When this flag is 1, it indicates that the main clock oscillation stop was detected. After this stop is detected, the OSTDF flag is not set to 0 even when the main clock oscillation is restarted. The OSTDF flag is set to 0 by writing 0 after reading it as 1.

At least 3 ICLK cycles of wait time are required between writing 0 to OSTDF and reading OSTDF as 0. If the OSTDF flag is set to 0 when the main clock oscillation is stopped, the OSTDF flag becomes 0 then returns to 1.

OSTDSR.OSTDF cannot be set to 0 under the following conditions:

- SCKSCR.CKSEL[2:0] = 011b (system clock source = MOSC).

The OSTDF flag must be set to 0 after switching the clock source to sources other than the main clock oscillator.

[Setting condition]

- The main clock oscillator is stopped when OSTDCR.OSTDE = 1 (oscillation stop detection function enabled).

[Clearing condition]

- 1 is read and then 0 is written when the SCKSCR.CKSEL[2:0] bits are not 011b (system clock is MOSC).

8.2.11 Main Clock Oscillator Wait Control Register (MOSCWTCR)

Address(es): SYSTEM.MOSCWTCR 4001 E0A2h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	MSTS[3:0]			
Value after reset:	0	0	0	0	0	1	0	1

Bit	Symbol	Bit name	Description	R/W
b3 to b0	MSTS[3:0]	Main Clock Oscillator Wait Time Setting	b3 b0 0 0 0 0: Wait time = 2 cycles (0.25 μs) 0 0 0 1: Wait time = 1024 cycles (128 μs) 0 0 1 0: Wait time = 2048 cycles (256 μs) 0 0 1 1: Wait time = 4096 cycles (512 μs) 0 1 0 0: Wait time = 8192 cycles (1024 μs) 0 1 0 1: Wait time = 16384 cycles (2048 μs) (value after reset) 0 1 1 0: Wait time = 32768 cycles (4096 μs) 0 1 1 1: Wait time = 65536 cycles (8192 μs) 1 0 0 0: Wait time = 131072 cycles (16384 μs) 1 0 0 1: Wait time = 262144 cycles (32768 μs). Other settings are prohibited. Wait time is calculated at MOCO = 8 MHz (typically 0.125 μs).	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R

MSTS[3:0] bits (Main Clock Oscillator Wait Time Setting)

Set the MSTS[3:0] bits to select the oscillation stabilization wait time for the main clock oscillator.

Set the main clock oscillation stabilization time to a period longer than or equal to the stabilization time recommended by the oscillator manufacturer. When the main clock is input externally, set these bits to 0000b because the oscillation stabilization time is not required.

The wait time set by the MSTS[3:0] bits is counted using the MOCO clock. The MOCO clock automatically oscillates when necessary, regardless of the value of the MOCOCR.MCSTP bit. After the set wait time elapses, supply of the main clock starts internally in the MCU, and the OSCSF.MOSCSF flag is set to 1. If the set wait time is short, supply of the main clock starts before oscillation of the clock becomes stable.

Only rewrite the MOSCWTCR register when the MOSCCR.MOSTP bit is 1 and the OSCSF.MOSCSF flag is 0. Do not rewrite this register under any other conditions.

8.2.12 High-Speed On-Chip Oscillator Wait Control Register (HOCOWTCR)

Address(es): SYSTEM.HOCOWTCR 4001 E0A5h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	HSTS[2:0]		
Value after reset:	0	0	0	0	0	1	0	1

Bit	Symbol	Bit name	Description	R/W
b2 to b0	HSTS[2:0]	HOCO wait time setting	b2 b0 1 0 1: • Wait time = 245 cycles (29.13 μs) when HOCO operating frequency is 24 MHz or 32 MHz, and the operation power control mode is other than low voltage mode. • Wait time = 287 cycles (35.875 μs) when HOCO operating frequency is 48 MHz and the operation power control mode is other than low voltage mode. • Wait time = 679 cycles (84.88 μs) (value after reset) when operation power control mode is low voltage mode. 1 1 0: • Wait time = 541 cycles (67.63 μs) when HOCO operating frequency is 64 MHz. Other settings are prohibited. Wait time is calculated at MOCO = 8 MHz (typically 0.125 μs).	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R

HOCOWTCR controls the wait time until output of the signal from the high-speed clock oscillator to the internal circuits starts. Only write to HOCOWTCR when the HOCOCR.HCSTP bit is 1 or the OSCSF.HOCOSF flag is 1. Do not write to this register under any other conditions.

HSTS[2:0] bits (HOCO wait time setting)

The oscillation stabilization wait circuit measures the wait time and controls the clock supply in the MCU. When the high-speed clock oscillator starts, the oscillation stabilization wait circuit starts counting cycles of the middle-speed clock set in the HOCOWTCR register. The MCU clock supply is disabled until counting of the set number of cycles is complete. After counting completes, supply of the clock signal in the MCU starts and the OSCSF.HOCOSF flag is set to 1.

The oscillation stabilization wait circuit continues to count the middle-speed clock cycles regardless of the MOCOCR.MCSTP bit setting. Hardware automatically controls the running and stopping of the middle-speed oscillator for wait time measurement.

8.2.13 Main Clock Oscillator Mode Oscillation Control Register (MOMCR)

Address(es): SYSTEM.MOMCR 4001 E413h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	MOSEL	—	—	MODRV1	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit name	Description	R/W
b3	MODRV1	Main Clock Oscillator Drive Capability 1 Switching	0: 10 MHz to 20 MHz 1: 1 MHz to 10 MHz.	R/W
b5, b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	MOSEL	Main Clock Oscillator Switching	0: Resonator 1: External clock input.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note: The EXTAL/XTAL pin is also used as a port. In the initial state, the pin is set as a port.
Note: The MOSCCR.MOSTP bit must be 1 (MOSC is stopped) before changing this register.

MODRV1 bit (Main Clock Oscillator Drive Capability 1 Switching)

The MODRV1 bit switches the drive capability of the main clock oscillator.

MOSEL bit (Main Clock Oscillator Switching)

The MOSEL bit switches the source for the main clock oscillator.

8.2.14 Sub-Clock Oscillator Mode Control Register (SOMCR)

Address(es): SYSTEM.SOMCR 4001 E481h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	SODRV[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	SODRV[1:0]	Sub-Clock Oscillator Drive Capability Switching	b1 b0 0 0: Normal mode 0 1: Low Power mode 1 1 0: Low Power mode 2 1 1: Low Power mode 3.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

This register must be modified when SOSCCR.SOSTP is 1 (SOSC is stopped).

SODRV[1:0] bits (Sub-Clock Oscillator Drive Capability Switching)

The SODRV[1:0] bits switch the drive capability of the sub-clock oscillator.

8.2.15 Clock Out Control Register (CKOCR)

Address(es): SYSTEM.CKOCR 4001 E03Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	CKOEN	CKODIV[2:0]			—	CKOSEL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	CKOSEL[2:0]	Clock Out Source Select	b2 b0 0 0 0: HOCO 0 0 1: MOCO 0 1 0: LOCO 0 1 1: MOSC 1 0 0: SOSC. Other settings are prohibited.	R/W

Bit	Symbol	Bit name	Description	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6 to b4	CKODIV[2:0]	Clock Out input frequency Division Select	b6 b4 0 0 0: ×1 0 0 1: /2 0 1 0: /4 0 1 1: /8 1 0 0: /16 1 0 1: /32 1 1 0: /64 1 1 1: /128.	R/W
b7	CKOEN	Clock Out Enable	0: Disable clock out 1: Enable clock out.	R/W

CKOSEL[2:0] bits (Clock Out Source Select)

The CKOSEL[2:0] bits specify the HOCO, MOCO, LOCO, MOSC, SOSC clock as the source clock to be output from the CLKOUT pin.

Set the CKOEN bit to 0 when changing the CLKOUT source clock.

CKODIV[2:0] bits (Clock Out input frequency Division Select)

The CKODIV[2:0] bits specify the clock division ratio.

Set the CKOEN bit to 0 when changing the division ratio. The division ratio of the output clock frequency must be set to a value no higher than the characteristics of the CLKOUT pin output frequency. For details on the characteristics of the CLKOUT pin, see section 46, Electrical Characteristics.

CKOEN bit (Clock Out Enable)

The CKOEN bit enables output from the CLKOUT pin.

When this bit is set to 1, the selected clock is output. When this bit is set to 0, low is output. When changing this bit, confirm that the clock out source clock selected in the CKOSEL[2:0] bits is stable. Otherwise, a glitch might be generated in the output.

Clear this bit before entering Software Standby mode if the selected clock source is stopped in that mode.

8.2.16 LOCO User Trimming Control Register (LOCOUTCR)

Address(es): SYSTEM.LOCOUTCR 4001 E492h

	b7	b6	b5	b4	b3	b2	b1	b0
	LOCOUTRM[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	LOCOUTRM[7:0]	LOCO User Trimming	b7 b0 1 0 0 0 0 0 0 0: -128 1 0 0 0 0 0 0 1: -127 1 0 0 0 0 0 1 0: -126 … 1 1 1 1 1 1 1 1: -1 0 0 0 0 0 0 0 0: Center Code 0 0 0 0 0 0 0 1: +1 … 0 1 1 1 1 1 0 1: +125 0 1 1 1 1 1 1 0: +126 0 1 1 1 1 1 1 1: +127 These bits are added to the original LOCO trimming bits.	R/W

MCU operation is not guaranteed when LOCOUTCR is set to a value that causes the LOCO frequency to be outside of the specification range. When LOCOUTCR is modified, the frequency stabilization time corresponds to the frequency stabilization time at the start of MCU operation. When the ratio of the LOCO frequency to the other oscillation frequency is an integer value, changing the LOCOUTCR value is prohibited.

8.2.17 MOCO User Trimming Control Register (MOCOUTCR)

Address(es): SYSTEM.MOCOUTCR 4001 E061h

	b7	b6	b5	b4	b3	b2	b1	b0
	MOCOUTRM[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	MOCOUTRM[7:0]	MOCO User Trimming	b7 b0 1 0 0 0 0 0 0 0: -128 1 0 0 0 0 0 0 1: -127 1 0 0 0 0 0 1 0: -126 … 1 1 1 1 1 1 1 1: -1 0 0 0 0 0 0 0 0: Center Code 0 0 0 0 0 0 0 1: +1 … 0 1 1 1 1 1 0 1: +125 0 1 1 1 1 1 1 0: +126 0 1 1 1 1 1 1 1: +127 These bits are added to the original MOCO trimming bits.	R/W

MCU operation is not guaranteed when MOCOUTCR is set to a value that causes the MOCO frequency to be outside of the specification range.

When MOCOUTCR is modified, the time when the frequency is stabilized corresponds to the time when it is stabilized at the start of the MCU operation.

When the ratio of the MOCO frequency to the other oscillation frequency is an integer value, changing the MOCOUTCR value is prohibited.

8.2.18 HOCO User Trimming Control Register (HOCOUTCR)

Address(es): SYSTEM.HOCOUTCR 4001 E062h

	b7	b6	b5	b4	b3	b2	b1	b0
	HOCOUTRM[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	HOCOUTRM[7:0]	HOCO User Trimming	b7 b0 1 0 0 0 0 0 0 0: -128 1 0 0 0 0 0 0 1: -127 1 0 0 0 0 0 1 0: -126 … 1 1 1 1 1 1 1 1: -1 0 0 0 0 0 0 0 0: Center Code 0 0 0 0 0 0 0 1: +1 … 0 1 1 1 1 1 0 1: +125 0 1 1 1 1 1 1 0: +126 0 1 1 1 1 1 1 1: +127. These bits are added to the original HOCO trimming bits.	R/W

MCU operation is not guaranteed when HOCOUTCR is set to a value that causes the HOCO frequency to be outside of the specification range. When HOCOUTCR is modified, the time taken for the frequency to stabilize corresponds to the time taken for the frequency to stabilize at the start of the MCU operation.

When UCKSEL.UCKSELC = 1, writing any other value except 00h to HOCOUTCR is prohibited. For UCKSEL register, see section 26, USB 2.0 Full-Speed Module (USBFS).

8.3 Main Clock Oscillator

To supply the clock signal to the main clock oscillator, use one of the following ways:

- Connect an oscillator
- Connect the input of an external clock signal.

8.3.1 Connecting the Crystal Resonator

Figure 8.2 shows an example of connecting a crystal resonator.

A damping resistor (Rd) can be added, if required. Because the resistor values vary according to the resonator and the oscillation drive capability, use values recommended by the resonator manufacturer. If the manufacturer recommends using an external feedback resistor (Rf), insert an Rf between EXTAL and XTAL by following the instructions.

When connecting a resonator to supply the clock, the frequency of the resonator must be in the frequency range of the resonator for the main clock oscillator as described in Table 8.1.

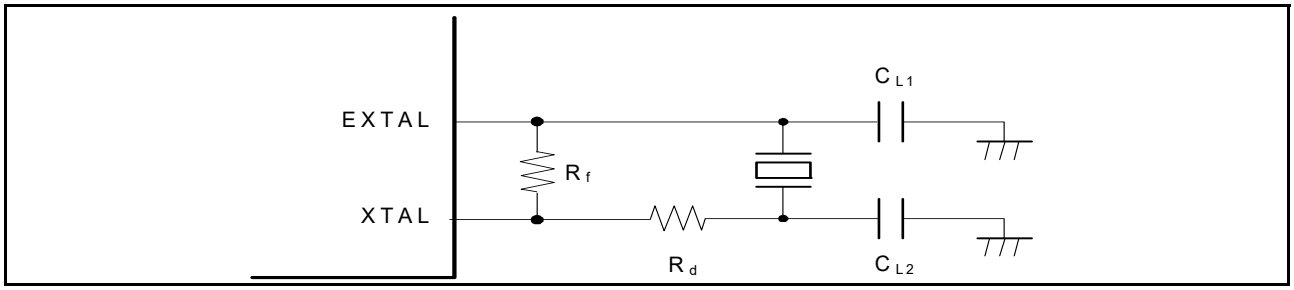


Figure 8.2 Example of crystal resonator connection

8.3.2 External Clock Input

Figure 8.3 shows an example of connecting an external clock input. To operate the oscillator with an external clock signal, set the MOMCR.MOSEL bit to 1. The XTAL pin goes to high impedance.

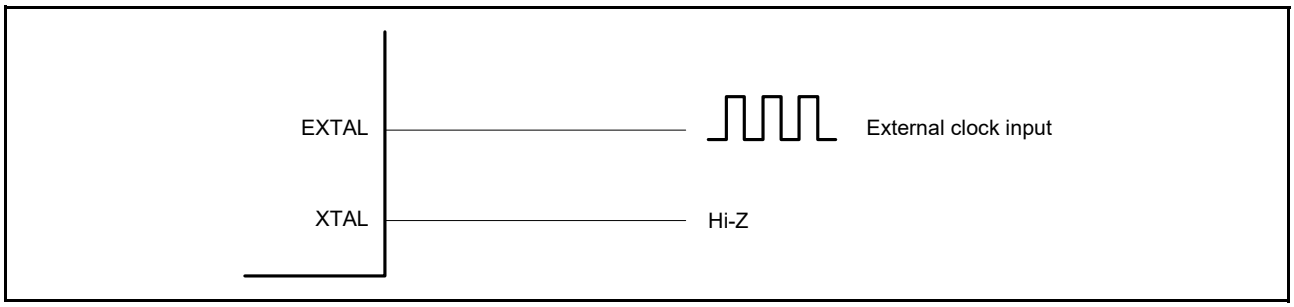


Figure 8.3 Equivalent circuit for external clock

8.3.3 Notes on External Clock Input

The frequency of the external clock input can only be changed when the main clock oscillator is stopped. Do not change the frequency of the external clock input when the setting of the Main Clock Oscillator Stop bit (MOSCCR.MOSTP) is 0.

8.4 Sub-Clock Oscillator

The only way of supplying a clock signal to the sub-clock oscillator is by connecting a crystal oscillator.

8.4.1 Connecting a 32.768-kHz Crystal Resonator

To supply a clock to the sub-clock oscillator, connect a 32.768-kHz crystal resonator as shown in Figure 8.4.

A damping resistor (Rd) can be added, if required. Because the resistor values vary according to the resonator and the oscillation drive capability, use values recommended by the resonator manufacturer. If the resonator manufacturer recommends the use of an external feedback resistor (Rf), insert an Rf between XCIN and XCOUT by following the instructions. When connecting a resonator to supply the clock, the frequency of the resonator must be in the frequency range of the resonator for the sub-clock oscillator as described in Table 8.1.

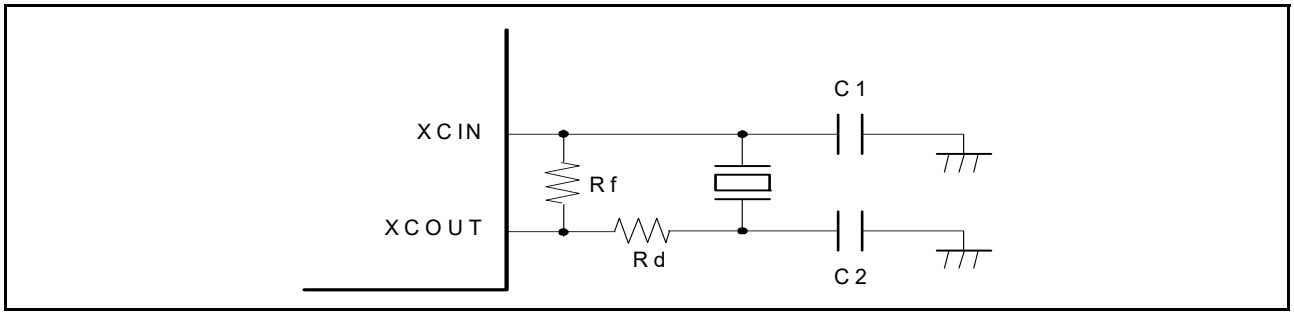


Figure 8.4 Connection example of 32.768-kHz crystal resonator

8.5 Oscillation Stop Detection Function

8.5.1 Oscillation Stop Detection and Operation after Detection

The oscillation stop detection function detects the main clock oscillator stop.

When oscillation stop is detected, the system clock switches as follows:

- If an oscillation stop is detected with SCKSCR.CKSEL[2:0] = 011b (system clock source = MOSC), the system clock source switches to the MOCO clock.

An oscillation stop detection interrupt request can be generated when an oscillation stop is detected. In addition, the

General PWM Timer (GPT) output can be forced to a high-impedance state on detection.

The main clock oscillation stop is detected when the input clock remains at 0 or 1 for a certain period, for example, when a malfunction occurs in the main clock oscillator. See section 46, Electrical Characteristics.

Switching between the main clock oscillator and the MOCO clock is controlled by the Oscillation Stop Detection Flag (OSTDSR.OSTDF).

OSTDF controls the switched clock as follows:

- SCKSCR.CKSEL[2:0] = 011b (system clock source = MOSC):
  When OSTDF changes from 0 to 1, the clock source switches to the MOCO clock
  When OSTDF changes from 1 to 0, the clock source switches to MOSC clock again.

To switch the clock source to the main clock again after the oscillation stop detection, set the CKSEL[2:0] bits to a clock source other than the main clock and clear the OSTDF flag to 0. Also, check that the OSTDF flag is not 1, then set the CKSEL[2:0] bits to the main clock after the specified oscillation stabilization time elapses.

After a reset release, the main clock oscillator is stopped and the oscillation stop detection function is disabled. To enable the oscillation stop detection function, activate the main clock oscillator and write 1 to the oscillation stop detection function enable bit (OSTDCR.OSTDE) after a specified oscillation stabilization time elapses.

The oscillation stop detection function detects when the main clock is stopped by an external cause. Therefore, the oscillation stop detection function must be disabled before the main clock oscillator is stopped by software or a transition is made to Software Standby mode.

The oscillation stop detection function switches the following clocks to the MOCO clock (when system clock is MOSC):

- All clocks that can be selected as the MOSC except CLKOUT
- The system clock (ICLK) frequency during the MOCO operation (when system clock is MOSC) is specified in the MOCO oscillation frequency and the division ratio set in the System Clock Select bits (SCKDIVCR.ICK[2:0]).

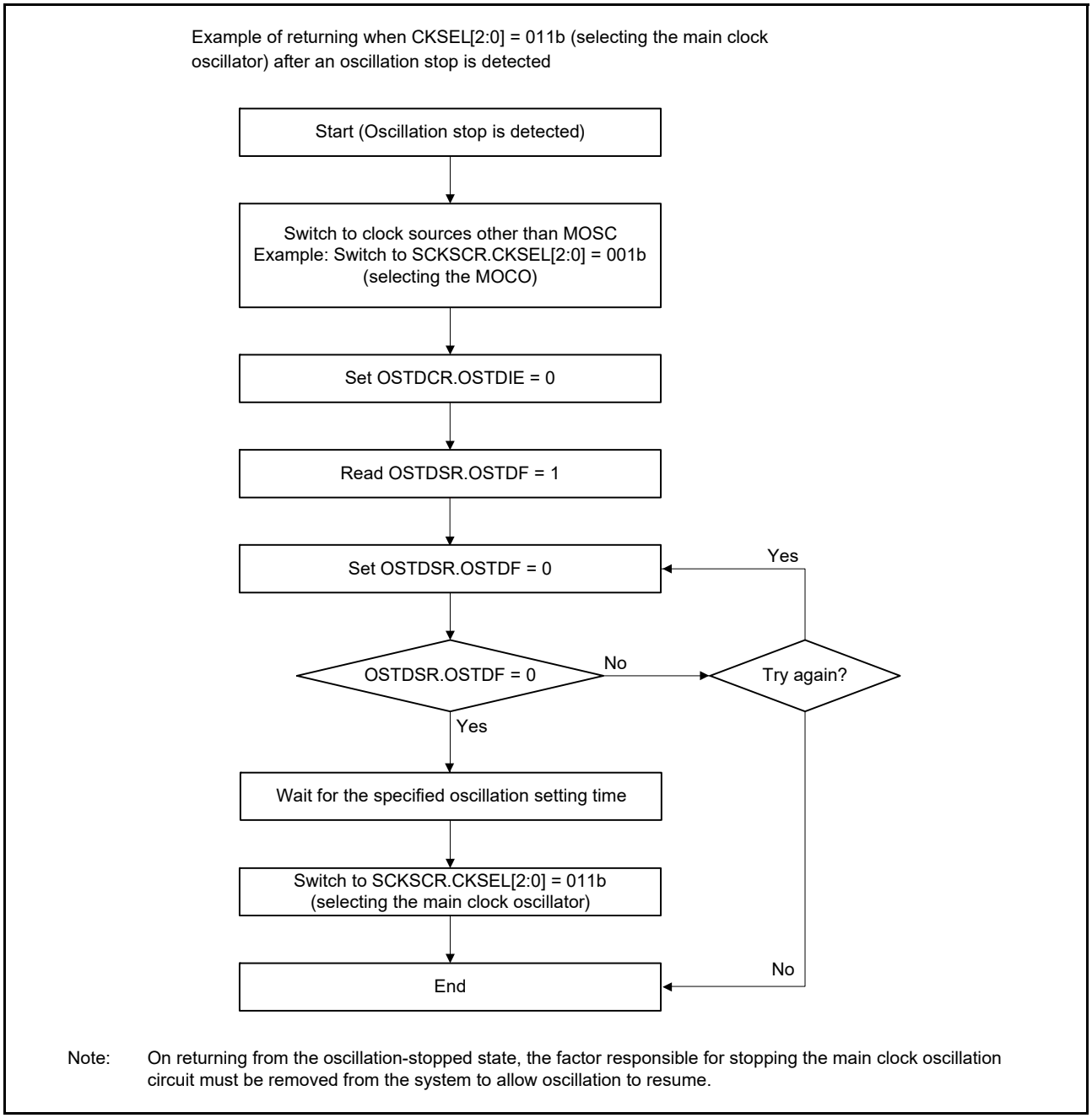


Figure 8.5 Flow of recovery on detection of oscillator stop

8.5.2 Oscillation Stop Detection Interrupts

An oscillation stop detection interrupt (MOSC_STOP) is generated when the Oscillation Stop Detection Flag (OSTDSR.OSTDF) is 1 and the Oscillation Stop Detection Interrupt Enable bit in the Oscillation Stop Detection Control Register (OSTDCR.OSTDIE) is 1 (enabled). The Port Output Enable for GPT (POEG) is notified of the main clock oscillator stop. On receiving the notification, the POEG sets the Oscillation Stop Detection Flag in the POEG Group n Setting Register (POEGGn.OSTPF) to 1 (n = A, B).

After the oscillation stop is detected, wait at least 10 PCLKB cycles before writing to the POEGGn.OSTPF flag. When the OSTDSR.OSTDF flag requires clearing, do so after clearing the Oscillation Stop Detection Interrupt Enable bit in the Oscillation Stop Detection Control Register (OSTDCR.OSTDIE). Wait at least 2 PCLKB clock cycles before setting the OSTDCR.OSTDIE bit to 1 again. A longer PCLKB wait time might be required, depending on the number of cycles required to read a given I/O register.

The oscillation stop detection interrupt is a non-maskable interrupt. Because non-maskable interrupts are disabled in the

initial state after a reset release, enable the non-maskable interrupts through software before using the oscillation stop detection interrupts. For details, see section 12, Interrupt Controller Unit (ICU).

8.6 Internal Clock

Clock sources for the internal clock signals include:

- Main clock oscillator
- Sub-clock oscillator
- HOCO clock
- MOCO clock
- LOCO clock
- Dedicated clock for the IWDT.

The following internal clocks are produced from these sources:

- Operating clock for the CPU, DTC, flash memory, and SRAM — system clock (ICLK)
- Operating clocks for peripheral modules — PCLKB and PCLKD
- Operating clock for the flash interface — ICLK
- Operating clock for the CAN — CANMCLK
- Operating clock for the USBFS — UCLK
- Operating clocks for the CAC — CACCLK
- Operating clock for the RTC LOCO clock — RTCLCLK
- Operating clock for the RTC sub clock — RTCSCLK
- Operating clock for the IWDT — IWDTCLK
- Operating clock for the AGT LOCO clock — AGTLCLK
- Operating clock for the AGT sub clock — AGTSCLK
- Operating clock for the SysTick timer — SYSTICCLK
- Clock for external pin output — CLKOUT.

For details on the registers used to set the frequencies of the internal clocks, see section 8.6.1, System Clock (ICLK) to section 8.6.11, Clock/Buzzer Output Clock (CLKOUT).

If the value of any of these bits is changed, subsequent operation is at a frequency determined by the new value.

8.6.1 System Clock (ICLK)

The system clock, ICLK, is the operating clock for the CPU, DTC, flash memory, flash interface, and SRAM.

The ICLK frequency is specified in the ICK[2:0] bits in SCKDIVCR, the CKSEL[2:0] bits in SCKSCR, and the HOCOFRQ1[2:0] bits in OFS1.

8.6.2 Peripheral Module Clock (PCLKB, PCLKD)

The peripheral module clocks, PCLKB and PCLKD, are the operating clocks for the peripheral modules.

The frequency of the given clock is specified in the following bits:

- PCKB[2:0] and PCKD[2:0] in SCKDIVCR
- CKSEL[2:0] in SCKSCR
- HOCOFRQ1[2:0] in OFS1.

8.6.3 Flash Interface Clock (ICLK)

The flash interface clock, ICLK, is the operating clock for the flash memory interface. In addition to reading from the data flash, ICLK is used for the programming and erasure of the code flash and data flash.

8.6.4 USB Clock (UCLK)

The USB clock, UCLK, is an operating clock for the USBFS module. A 48-MHz clock must be supplied to the USBFS module. When the USBFS module is used, the setting must be 48 MHz for the UCLK clock. The UCLK frequency is specified by HOCOFRQ1[2:0] bits in OFS1.

8.6.5 CAN Clock (CANMCLK)

The CAN clock, CANMCLK, is an operating clock for the CAN module. CANMCLK is generated by the main clock oscillator.

8.6.6 CAC Clock (CACCLK)

The CAC clock, CACCLK, is an operating clock for the CAC.

CACCLK is generated by the following oscillators:

- Main clock oscillator
- Sub-clock oscillator
- High-speed clock oscillator (HOCO)
- Middle-speed clock oscillator (MOCO)
- Low-speed on-chip oscillator (LOCO)
- IWDT-dedicated on-chip oscillator.

8.6.7 RTC-Dedicated Clock (RTCSCLK, RTCLCLK)

The RTC-dedicated clocks, RTCSCLK and RTCLCLK, are the operating clocks for the RTC.

RTCSCLK is generated by the sub-clock oscillator, and RTCLCLK is generated by the LOCO clock.

8.6.8 IWDT-Dedicated Clock (IWDTCLK)

The IWDT-dedicated clock, IWDTCLK, is the operating clock for the IWDT.

IWDTCLK is internally generated by the IWDT-dedicated on-chip oscillator.

8.6.9 AGT-Dedicated Clock (AGTSCLK, AGTLCLK)

The AGT-dedicated clocks, AGTSCLK and AGTLCLK, are the operating clocks for the AGT.

AGTSCLK is generated by the sub-clock oscillator, and AGTLCLK is generated by the LOCO clock.

8.6.10 SysTick Timer-Dedicated Clock (SYSTICCLK)

The SysTick timer-dedicated clock, SYSTICCLK, is the operating clock for the SysTick timer. SYSTICCLK is generated by the LOCO clock.

8.6.11 Clock/Buzzer Output Clock (CLKOUT)

The CLKOUT is output externally from the CLKOUT pin for the clock or buzzer output. CLKOUT is output to the CLKOUT pin when CKOCR.CKOEN is set to 1. Only change the value of CKODIV[2:0] or CKOSEL[2:0] bits in CKOCR when the CKOCR.CKOEN bit is 0.

The CLKOUT clock frequency is specified in the following bits:

- CKODIV[2:0] or CKOSEL[2:0] in CKOCR
- HOCOFRQ1[2:0] in OFS1.

8.7 Usage Notes

8.7.1 Notes on Clock Generation Circuit

The frequencies of the system clock (ICLK), peripheral module clock (PCLKB and PCLKD), and flash interface clock (ICLK) supplied to each module change according to the settings of SCKDIVCR. Each frequency must meet the following conditions:

- Select each frequency that is within the operation-guaranteed range of the clock cycle time (t_{cyc}) specified in the AC characteristics. See section 46, Electrical Characteristics.
- The frequencies must not exceed the ranges listed in Table 8.2
- The peripheral modules operate on the PCLKB. As a result, the operating speed of modules such as the timer and SCI is different before and after the frequency is changed.
- The system clock (ICLK), peripheral module clock (PCLKB and PCLKD), and flash interface clock (ICLK) must be set according to Table 8.2.

To ensure correct processing after the clock frequency changes, first modify the relevant Clock Control register to change the frequency, then read the value from the register, and finally perform the subsequent processing.

8.7.2 Notes on Resonator

Because various resonator characteristics relate closely to your board design, adequate evaluation is required before use. See the resonator connection example in Figure 8.4. The circuit constants for the resonator depend on the resonator to be used and the stray capacitance of the mounting circuit. Therefore, consult the resonator manufacturer when determining the circuit constants. The voltage to be applied between the resonator pins must be within the absolute maximum rating.

8.7.3 Notes on Board Design

When using a crystal resonator, place the resonator and its load capacitors as close to the XTAL and EXTAL pins as possible. Other signal lines should be routed away from the oscillation circuit as shown in Figure 8.6 to prevent electromagnetic induction from interfering with correct oscillation.

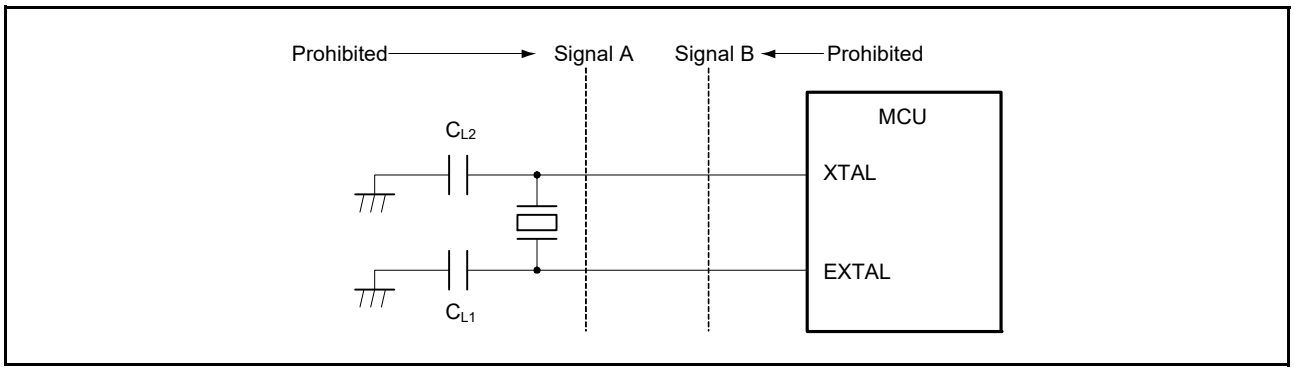


Figure 8.6 Signal routing in board design for oscillation circuit (applies to the sub-clock oscillator for the main clock oscillator)

8.7.4 Notes on Resonator Connect Pin

When the main clock is not used, the EXTAL and XTAL pins can be used as general ports P212 and P213. When these pins are used as the general ports, the main clock must be stopped (MOSCCR.MOSTP should be set to 1).

9. Clock Frequency Accuracy Measurement Circuit (CAC)

9.1 Overview

The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock to be used as a measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range.

When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated.

Table 9.1 lists the CAC specifications, Figure 9.1 shows a block diagram, and Table 9.2 shows the I/O pins.

Table 9.1 CAC specifications

Parameter	Description
Measurement target clocks	Frequency can be measured for: • Main clock oscillator • Sub-clock oscillator • HOCO clock • MOCO clock • LOCO clock • IWDTCLK clock • Peripheral module clock B (PCLKB).
Measurement reference clocks	Frequency can be referenced to: • External clock input to the CACREF pin • Main clock oscillator • Sub-clock oscillator • HOCO clock • MOCO clock • LOCO clock • IWDTCLK clock • Peripheral module clock B (PCLKB).
Selectable function	Digital filter
Interrupt sources	• Measurement end • Frequency error • Overflow.
Module-stop function	Module-stop state can be set to reduce power consumption

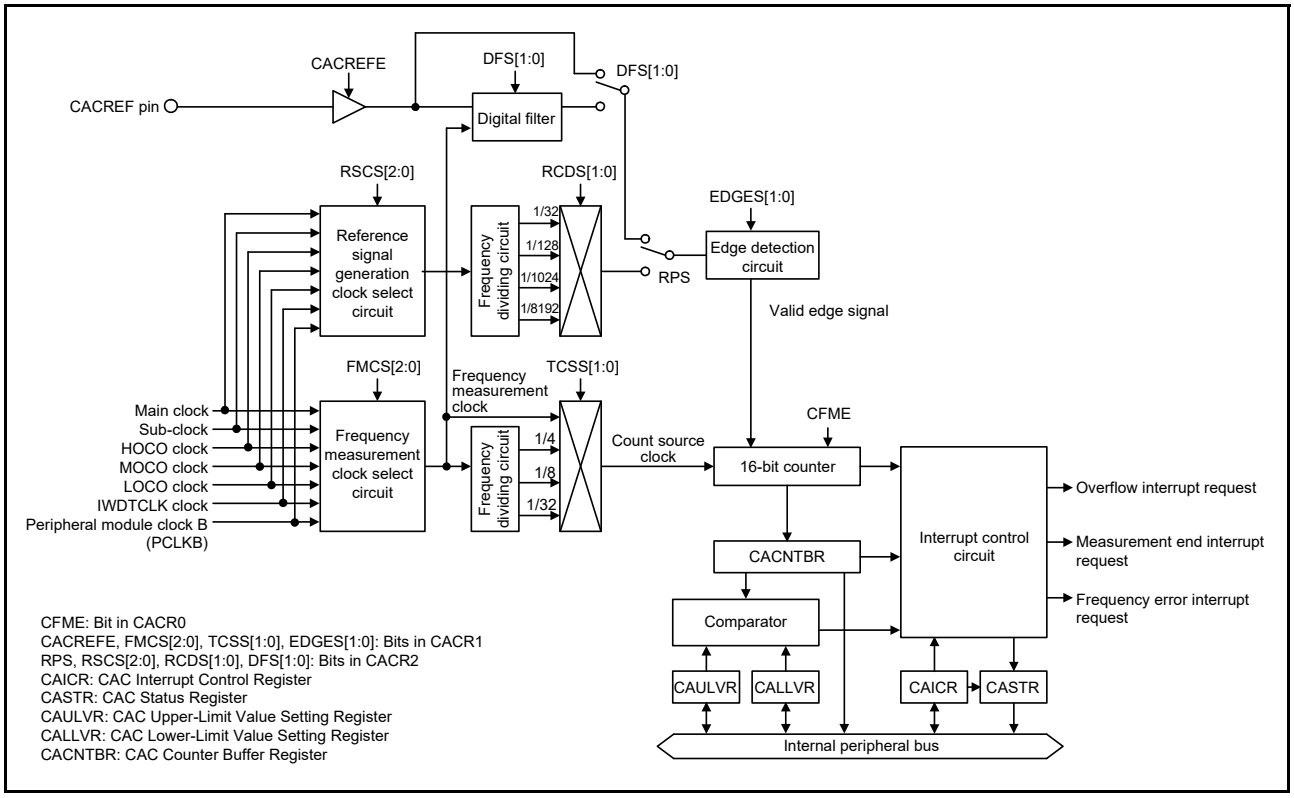


Figure 9.1 CAC block diagram

Table 9.2 CAC pin configuration

Pin name	I/O	Function
CACREF	Input	Measurement reference clock input pin

9.2 Register Descriptions

9.2.1 CAC Control Register 0 (CACR0)

Address(es): CAC.CACR0 4004 4600h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CFME
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CFME	Clock Frequency Measurement Enable	0: Disable 1: Enable.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CFME bit (Clock Frequency Measurement Enable)

The CFME bit enables clock frequency measurement. Read the CFME bit to confirm that the bit value has changed. Additional write accesses are ignored before the change is complete.

9.2.2 CAC Control Register 1 (CACR1)

Address(es): CAC.CACR1 4004 4601h

	b7	b6	b5	b4	b3	b2	b1	b0
	EDGES[1:0]		TCSS[1:0]		FMCS[2:0]			CACREFE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CACREFE	CACREF Pin Input Enable	0: Disable 1: Enable.	R/W
b3 to b1	FMCS[2:0]	Measurement Target Clock Select	b3 b1 0 0 0: Main clock oscillator 0 0 1: Sub-clock oscillator 0 1 0: HOCO clock 0 1 1: MOCO clock 1 0 0: LOCO clock 1 0 1: Peripheral module clock (PCLKB) 1 1 0: IWDTCLK clock 1 1 1: Setting prohibited.	R/W
b5, b4	TCSS[1:0]	Measurement Target Clock Frequency Division Ratio Select	b5 b4 0 0: No division 0 1: ×1/4 clock 1 0: ×1/8 clock 1 1: ×1/32 clock.	R/W
b7, b6	EDGES[1:0]	Valid Edge Select	b7 b6 0 0: Rising edge 0 1: Falling edge 1 0: Both rising and falling edges 1 1: Setting prohibited.	R/W

Note 1. Set the CACR1 register when the CACR0.CFME bit is 0.

CACREFE bit (CACREF Pin Input Enable)

The CACREFE bit enables the CACREF pin input.

FMCS[2:0] bits (Measurement Target Clock Select)

The FMCS[2:0] bits select the measurement target clock whose frequency is to be measured.

TCSS[1:0] bits (Measurement Target Clock Frequency Division Ratio Select)

The TCSS[1:0] bits select the division ratio of the measurement target clock.

EDGES[1:0] bits (Valid Edge Select)

The EDGES[1:0] bits select the valid edge for the reference signal.

9.2.3 CAC Control Register 2 (CACR2)

Address(es): CAC.CACR2 4004 4602h

	b7	b6	b5	b4	b3	b2	b1	b0
	DFS[1:0]		RCDS[1:0]		RSCS[2:0]			RPS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RPS	Reference Signal Select	0: CACREF pin input 1: Internal clock (internally generated signal).	R/W
b3 to b1	RSCS[2:0]	Measurement Reference Clock Select	b3 b1 0 0 0: Main clock oscillator 0 0 1: Sub-clock oscillator 0 1 0: HOCO clock 0 1 1: MOCO clock 1 0 0: LOCO clock 1 0 1: Peripheral module clock (PCLKB) 1 1 0: IWDTCLK clock 1 1 1: Setting prohibited.	R/W
b5, b4	RCDS[1:0]	Measurement Reference Clock Frequency Division Ratio Select	b5 b4 0 0: ×1/32 clock 0 1: ×1/128 clock 1 0: ×1/1024 clock 1 1: ×1/8192 clock.	R/W
b7, b6	DFS[1:0]	Digital Filter Select	b7 b6 0 0: Disable digital filtering 0 1: Use sampling clock for the digital filter as the frequency measuring clock 1 0: Use sampling clock for the digital filter as the frequency measuring clock divided by 4 1 1: Use sampling clock for the digital filter as the frequency measuring clock divided by 16.	R/W

Note: Set the CACR2 register when the CACR0.CFME bit is 0.

RPS bit (Reference Signal Select)

The RPS bit selects whether to use the CACREF pin input or an internal clock (internally generated signal) as the reference signal.

RSCS[2:0] bits (Measurement Reference Clock Select)

The RSCS[2:0] bits select the reference clock for measurement.

RCDS[1:0] bits (Measurement Reference Clock Frequency Division Ratio Select)

The RCDS[1:0] bits select the division ratio of the reference clock when an internal reference clock is selected (RPS = 1). When RPS = 0 (the CACREF pin is used as the reference clock source), the reference clock is not divided.

DFS[1:0] bits (Digital Filter Select)

The DFS[1:0] bits enable or disable the digital filter and select its sampling clock.

9.2.4 CAC Interrupt Control Register (CAICR)

Address(es): CAC.CAICR 4004 4603h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	OVFFCL	MENDFCL	FERRFCL	—	OVFIE	MENDIE	FERRIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	FERRIE	Frequency Error Interrupt Request Enable	0: Disable frequency error interrupt request 1: Enable frequency error interrupt request.	R/W
b1	MENDIE	Measurement End Interrupt Request Enable	0: Disable measurement end interrupt request 1: Enable measurement end interrupt request.	R/W
b2	OVFIE	Overflow Interrupt Request Enable	0: Disable overflow interrupt request 1: Enable overflow interrupt request.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	FERRFCL	FERRF Clear	When 1 is written to this bit, the FERRF flag is cleared. This bit is read as 0.	R/W
b5	MENDFCL	MENDF Clear	When 1 is written to this bit, the MENDF flag is cleared. This bit is read as 0.	R/W
b6	OVFFCL	OVFF Clear	When 1 is written to this bit, the OVFF flag is cleared. This bit is read as 0.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

FERRIE bit (Frequency Error Interrupt Request Enable)

The FERRIE bit enables the frequency error interrupt request.

MENDIE bit (Measurement End Interrupt Request Enable)

The MENDIE bit enables the measurement end interrupt request.

OVFIE bit (Overflow Interrupt Request Enable)

The OVFIE bit enables the overflow interrupt request.

FERRFCL bit (FERRF Clear)

Setting the FERRFCL bit to 1 clears the FERRF flag.

MENDFCL bit (MENDF Clear)

Setting the MENDFCL bit to 1 clears the MENDF flag.

OVFFCL bit (OVFF Clear)

Setting the OVFFCL bit to 1 clears the OVFF flag.

9.2.5 CAC Status Register (CASTR)

Address(es): CAC.CASTR 4004 4604h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	OVFF	MENDF	FERRF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	FERRF	Frequency Error Flag	0: Clock frequency is within the allowable range 1: Clock frequency has deviated beyond the allowable range (frequency error).	R
b1	MENDF	Measurement End Flag	0: Measurement is in progress 1: Measurement ended.	R
b2	OVFF	Overflow Flag	0: The counter has not overflowed 1: The counter overflowed.	R
b7 to b3	—	Reserved	These bits are read as 0.	R

FERRF flag (Frequency Error Flag)

The FERRF flag indicates a deviation of the clock frequency from the set value (frequency error).

[Setting condition]

- The clock frequency is outside the allowable range defined in the CAULVR and CALLVR registers.

[Clearing condition]

- 1 is written to the FERRFCL bit.

MENDF flag (Measurement End Flag)

The MENDF flag indicates the end of measurement.

[Setting condition]

- Measurement ends.

[Clearing condition]

- 1 is written to the MENDFCL bit.

OVFF flag (Overflow Flag)

The OVFF flag indicates that the counter overflowed.

[Setting condition]

- The counter overflowed.

[Clearing condition]

- 1 is written to the OVFFCL bit.

9.2.6 CAC Upper-Limit Value Setting Register (CAULVR)

Address(es): CAC.CAULVR 4004 4606h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CAULVR is a 16-bit read/write register that specifies the upper value of the allowable range. When the counter value

rises above the value specified in this register, a frequency error is detected. Write to this register when the CACR0.CFME bit is 0.

The counter value stored in CACNTBR can vary depending on the difference between the phases of the digital filter and edge-detection circuit, and the signal on the CACREF pin. Ensure that this setting allows an adequate margin.

9.2.7 CAC Lower-Limit Value Setting Register (CALLVR)

Address(es): CAC.CALLVR 4004 4608h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CALLVR is a 16-bit read/write register that specifies the lower value of the allowable range. When the counter value falls below the value specified in this register, a frequency error is detected.

Write to this register when the CACR0.CFME bit is 0.

The counter value stored in CACNTBR can vary depending on the difference between the phases of the digital filter and edge-detection circuit, and the signal on the CACREF pin. Ensure that this setting allows an adequate margin.

9.2.8 CAC Counter Buffer Register (CACNTBR)

Address(es): CAC.CACNTBR 4004 460Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CACNTBR is a 16-bit read-only register that retains the measurement result.

9.3 Operation

9.3.1 Measuring Clock Frequency

The CAC measures the clock frequency using the CACREF pin input or an internal clock as a reference. Figure 9.2 shows an operating example of the CAC.

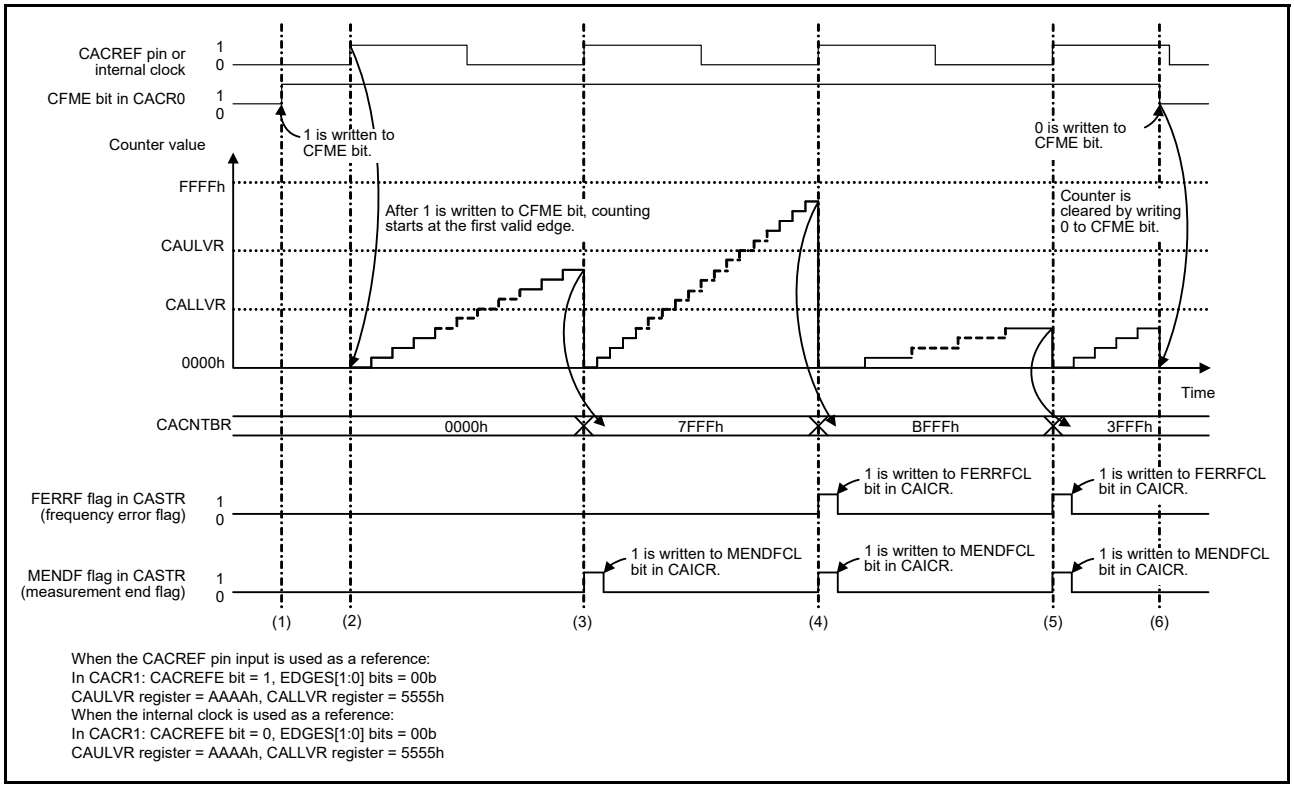


Figure 9.2 CAC operating example

1. Before writing 1 to CACR0.CFME, set CACR1 and CACR2 to define the measurement target clock and measurement reference clock. Writing 1 to the CACR0.CFME bit enables clock frequency measurement.
2. The timer starts counting up if the valid edge selected in the CACR1.EDGES[1:0] bits is input from the measurement reference clock. The valid edge is a rising edge (CACR1.EDGES[1:0] = 00b) as shown in Figure 9.2.
3. When the next valid edge is input, the counter value is transferred to CACNTBR and compared with the values of CAULVR and CALLVR. If both CACNTBR ≤ CAULVR and CACNTBR ≥ CALLVR are true, only the MENDF flag in CASTR is set to 1 because the clock frequency is correct. If the MENDIE bit in CAICR is 1, a measurement end interrupt is generated.
4. When the next valid edge is input, the counter value is transferred to CACNTBR and compared with the values of CAULVR and CALLVR. If CACNTBR > CAULVR, the FERRF flag in CASTR is set to 1 because the clock frequency is erroneous. If the FERRIE bit in CAICR is 1, a frequency error interrupt is generated. The MENDF flag in CASTR is set to 1 at the end of measurement. If the MENDIE bit in CAICR is 1, a measurement end interrupt is generated.
5. When the next valid edge is input, the counter value is transferred to CACNTBR and compared with the values of CAULVR and CALLVR. If CACNTBR < CALLVR, the FERRF flag in CASTR is set to 1 because the clock frequency is erroneous. If the FERRIE bit in CAICR is 1, a frequency error interrupt is generated. The MENDF flag in CASTR is set to 1 at the end of measurement. If the MENDIE bit in CAICR is 1, a measurement end interrupt is generated.
6. When the CFME bit in CACR0 is 1, the counter value is transferred to CACNTBR and compared with the values of CAULVR and CALLVR every time a valid edge is input. Writing 0 to the CFME bit in CACR0 clears the counter and stops counting up.

9.3.2 Digital Filtering of Signals on CACREF Pin

The CACREF pin has a digital filter, and levels on the CACREF pin are transmitted to the internal circuitry after three consecutive matches at the selected sampling interval. The same level continues to be transmitted internally until the level on the pin has three consecutive matches again. Enabling or disabling of the digital filter and its sampling clock are selectable.

The counter value transferred in CACNTBR might be in error by up to 1 cycle of the sampling clock because of the difference between the phases of the digital filter and the signal input to the CACREF pin. When a frequency dividing clock is selected as a count source clock, the counter value error is obtained using the following formula:

Counter value error = (1 cycle of the count source clock) / (1 cycle of the sampling clock)

9.4 Interrupt Requests

The CAC generates three types of interrupt requests:

- Frequency error interrupt
- Measurement end interrupt
- Overflow interrupt.

When an interrupt source is generated, the associated status flag becomes 1. Table 9.3 provides information on the CAC interrupt requests.

Table 9.3 CAC interrupt requests

Interrupt request	Interrupt enable bit	Status flag	Interrupt source
Frequency error interrupt	CAICR.FERRIE	CASTR.FERRF	The result of comparing CACNTBR with CAULVR and CALLVR is either CACNTBR > CAULVR or CACNTBR < CALLVR
Measurement end interrupt	CAICR.MENDIE	CASTR.MENDF	• Valid edge is input from the CACREF pin or internal clock • Measurement end interrupt does not occur at the first valid edge after writing 1 to the CACR0.CFME bit.
Overflow interrupt	CAICR.OVFIE	CASTR.OVFF	The counter overflows

9.5 Usage Note

9.5.1 Module-Stop State Setting

The CAN operation can be disabled or enabled with the Module Stop Control Register C (MSTPCRC). The initial setting of the CAC is in the module-stop state. Register access is enabled by releasing the module-stop state. For details, see section 10, Low Power Modes.

10. Low Power Modes

10.1 Overview

The MCU has several functions for reducing power consumption, such as setting clock dividers, stopping modules, selecting power control mode in Normal mode, and transitioning to Low power modes.

Table 10.1 lists the specifications of the low power mode functions. Table 10.2 lists the conditions to transition to low power modes, the states of the CPU and peripheral modules, and the method for canceling each mode. After a reset, the MCU enters the program execution state, but only the DTC and SRAM operate.

Table 10.1 Specifications of the low power mode functions

Parameter	Specifications
Reducing power consumption by switching clock signals	The frequency division ratio can be selected independently for the system clock (ICLK), and peripheral module clock (PCLKB and PCLKD)*1
Module-stop	Peripheral module functions can be stopped independently
Low power modes	• Sleep mode • Software Standby mode • Snooze mode.
Power control modes	Power consumption can be reduced in Normal, Sleep, and Snooze modes by selecting an appropriate operating power control mode according to the operating frequency and voltage. Five operating power control modes are available: • High-speed mode • Middle-speed mode • Low-speed mode • Low-voltage mode • Subosc-speed mode.

Note 1. For details, see section 8, Clock Generation Circuit.

Table 10.2 Operating conditions of each low power mode (1 of 2)

Parameter	Sleep mode	Software Standby mode	Snooze mode*1
Transition condition	WFI instruction while SBYCR.SSBY = 0	WFI instruction while SBYCR.SSBY = 1	Snooze request in Software Standby mode. SNZCR.SNZE = 1.
Canceling method	All interrupts. Any reset available in the mode.	Interrupts shown in Table 10.3. Any reset available in the mode.	Interrupts shown in Table 10.3. Any reset available in the mode.
State after cancellation by an interrupt	Program execution state (interrupt processing)	Program execution state (interrupt processing)	Program execution state (interrupt processing)
State after cancellation by a reset	Reset state	Reset state	Reset state
Main clock oscillator	Selectable	Stop	Selectable*2
Sub-clock oscillator	Selectable	Selectable	Selectable
High-speed on-chip oscillator	Selectable	Stop	Selectable
Middle-speed on-chip oscillator	Selectable	Selectable*10	Selectable*10
Low-speed on-chip oscillator	Selectable	Selectable	Selectable
IWDT-dedicated on-chip oscillator	Selectable*4	Selectable*4	Selectable*4
Oscillation stop detection function	Selectable	Operation prohibited	Operation prohibited
Clock/buzzer output function	Selectable	Selectable*3	Selectable
CPU	Stop (Retained)	Stop (Retained)	Stop (Retained)
SRAM	Operating	Stop (Retained)	Selectable
Flash memory	Operating	Stop (Retained)	Stop (Retained)
Data Transfer Controller (DTC)	Selectable	Stop (Retained)	Selectable
USB 2.0 Full-Speed Module (USBFS)	Selectable	Stop (Retained)*5	Operation prohibited*5
Watchdog Timer (WDT)	Selectable*4	Stop (Retained)	Stop (Retained)

Table 10.2 Operating conditions of each low power mode (2 of 2)

Parameter	Sleep mode	Software Standby mode	Snooze mode*1
Independent Watchdog Timer (IWDT)	Selectable*4	Selectable*4	Selectable*4
Realtime clock (RTC)	Selectable	Selectable	Selectable
Low Power Asynchronous General Purpose Timer (AGTn, n = 0, 1)	Selectable	Selectable*6	Selectable*6
14-Bit A/D Converter (ADC14)	Selectable	Stop (Retained)	Selectable*12
8-Bit D/A Converter (DAC8)	Selectable	Stop (Retained)	Selectable
Capacitive Touch Sensing Unit (CTSU)	Selectable	Stop (Retained)	Selectable
Data Operation Circuit (DOC)	Selectable	Stop (Retained)	Selectable
Serial Communications Interface (SCI0)	Selectable	Stop (Retained)	Selectable*9
Serial Communications Interface (SCIn, n = 1, 9)	Selectable	Stop (Retained)	Operation prohibited
Digital Addressable Lighting Interface	Selectable	Stop (Retained)	Selectable
I^2C Bus Interface (IIC0)	Selectable	Selectable	Selectable*11
I^2C Bus Interface (IIC1)	Selectable	Stop (Retained)	Operation prohibited
Event Link Controller (ELC)	Selectable	Stop (Retained)	Selectable*7
High-Speed Analog Comparator (ACMPHS)	Selectable	Selectable*8	Selectable*8
Low-Power Analog Comparator (ACMPLP0)	Selectable	Selectable*8	Selectable*8
Low-Power Analog Comparator (ACMPLP1)	Selectable	Selectable*8	Selectable*8
Operational Amplifier (OPAMP)	Selectable	Selectable	Selectable
NMI, IRQn (n = 0 to 7) pin interrupt	Selectable	Selectable	Selectable
Key Interrupt Function (KINT)	Selectable	Selectable	Selectable
Low voltage detection (LVD)	Selectable	Selectable	Selectable
Power-on reset circuit	Operating	Operating	Operating
Other peripheral modules	Selectable	Stop (Retained)	Operation prohibited
I/O Ports	Operating	Retained	Operating

Note: Selectable means that operating or not operating can be selected in the control registers.
Stop (Retained) means that the contents of the internal registers are retained but the operations are suspended.
Operation prohibited means that the function must be stopped before entering Software Standby mode.
Otherwise, proper operation is not guaranteed in Snooze mode.

Note 1. All modules whose module-stop bits are 0 start as soon as PCLKs are supplied after entering Snooze mode. To avoid an increase in power consumption in Snooze mode, set the module-stop bit of modules that are not required in Snooze mode to 1 before entering Software Standby mode.

Note 2. When using SCI0 in Snooze mode, MOSCCR.MOSTP bits must be 1.

Note 3. Stopped when the Clock Output Source Select bits (CKOCR.CKOSEL[2:0]) are set to a value other than 010b (LOCO) and 100b (SOSC).

Note 4. In IWDT-dedicated on-chip oscillator and IWDT, operating or stopping is selected by setting the IWDT Stop Control bit (IWDTSTPCTL) in the Option Function Select Register 0 (OFS0) in IWDT auto start mode. In WDT, operating or stopping is selected by setting the WDT Stop Control bit (WDTSTPCTL) in the Option Function Select Register 0 (OFS0) in WDT auto start mode.

Note 5. Detection of USBFS resumption is possible.

Note 6. AGT0 operation is possible when 100b (LOCO) or 110b (SOSC) is selected in the AGT0.AGTMR1.TCK[2:0] bits. AGT1 operation is possible when 100b (LOCO), 110b (SOSC), or 101 (underflow event signal from AGT0) is selected in the AGT1.AGTMR1.TCK[2:0] bits.

Note 7. Event lists the restrictions described in section 10.9.13, ELC Event in Snooze Mode.

Note 8. Only VCOUT function is permitted. The VCOUT pin operates when ACMPHS and ACMPLP use no digital filter. For details on digital filter, see section 37, High-Speed Analog Comparator (ACMPHS) and section 38, Low-Power Analog Comparator (ACMPLP).

Note 9. Serial communication of SCI0 is only in asynchronous mode.

Note 10. When DACPC.PUMPEN is 1, MOCO clock divided by 8 is supplied to ANSW which is used for DAC output.

Note 11. Only wakeup interrupt is available.

Note 12. When using the 14-Bit A/D Converter (ADC14) in Snooze mode, the ADCMPCR.CMPAE and ADCMPCR.CMPBE bit must be 1.

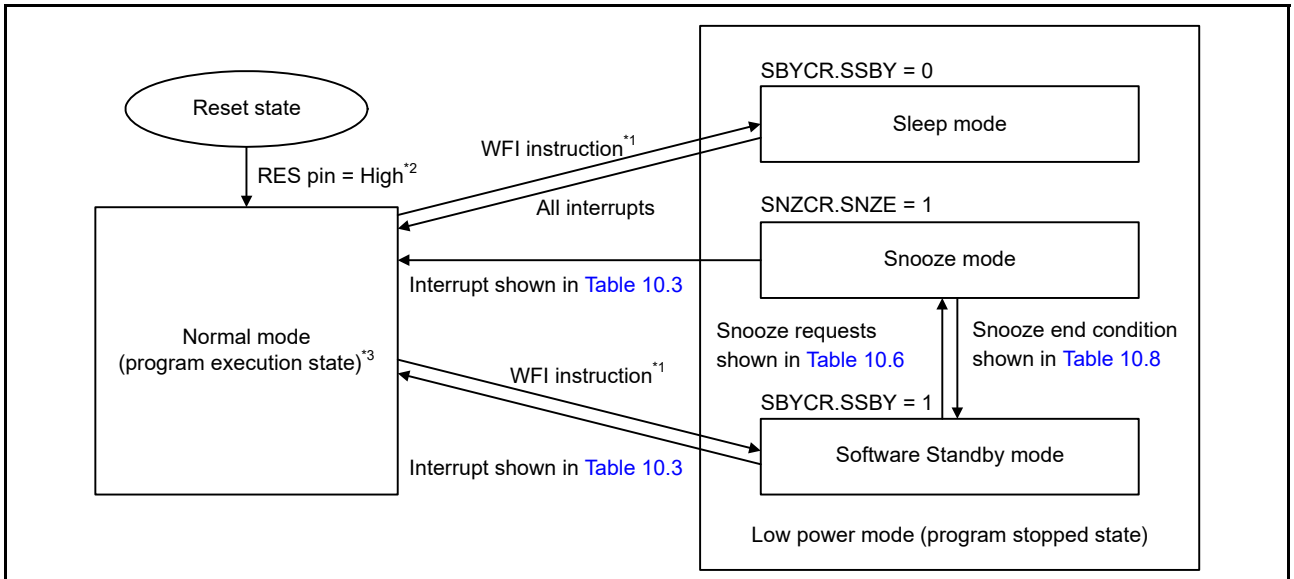
Table 10.3 Interrupt sources to transition to Normal mode from Snooze mode and Software Standby mode

Interrupt source	Name	Software Standby mode	Snooze mode
NMI		Yes	Yes
Port	PORT_IRQn (n = 0 to 7)	Yes	Yes
LVD	LVD_LVD1	Yes	Yes
	LVD_LVD2	Yes	Yes
IWDT	IWDT_NMIUNDF	Yes	Yes
USBFS	USBFS_USBR	Yes	Yes
RTC	RTC_ALM	Yes	Yes
	RTC_PRD	Yes	Yes
KINT	KEY_INTKR	Yes	Yes
AGT1	AGT1_AGTI	Yes	Yes*3
	AGT1_AGTCMAI	Yes	Yes
	AGT1_AGTCMBI	Yes	Yes
ACMPLP	ACMP_LP0	Yes	Yes
IIC0	IIC0_WUI	Yes	Yes
ADC140	ADC140_WCMPM	No	Yes with SELSR0*1, *3
	ADC140_WCMPUM	No	Yes with SELSR0*1, *3
SCI0	SCI0_AM	No	Yes with SELSR0*1, *2
	SCI0_RXI_OR_ERI	No	Yes with SELSR0*1, *2
DALI	DALI_SDI_OR_BPI	No	Yes with SELSR0*1, *3
DTC	DTC_COMPLETE	No	Yes with SELSR0*1
DOC	DOC_DOPCI	No	Yes with SELSR0*1
CTSU	CTSU_CTSUFN	No	Yes with SELSR0*1

Note 1. To use the interrupt request as a trigger for exiting Snooze mode, the request must be selected in SELSR0. See section 12, Interrupt Controller Unit (ICU). When a trigger selected in SELSR0 occurs after executing a WFI instruction, and during the transition from Normal mode to Software Standby mode, whether the request can be accepted depending on the timing of the occurrence.

Note 2. Only one of either SCI0_AM or SCI0_RXI_OR_ERI can be selected.

Note 3. The event that is enabled by the SNZEDCR register must not be used.



Note 1. When an interrupt that acts as a trigger for cancel is received during a transition to the program stopped state after the execution of a WFI instruction, the MCU executes interrupt exception handling instead of a transition to low power mode.
Note 2. The MOCO is the source of the operating clock following a transition from the reset state to Normal mode.
Note 3. The transition to Normal mode is made from an interrupt in Sleep mode, Software Standby mode, or Snooze mode. The clock source is the same as before entering the low power mode.

Figure 10.1 Mode transitions

10.2 Register Descriptions

10.2.1 Standby Control Register (SBYCR)

Address(es): SYSTEM.SBYCR 4001 E00Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SSBY	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b14 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	SSBY	Software Standby	0: Sleep mode 1: Software Standby mode.	R/W

SSBY bit (Software Standby)

The SSBY bit specifies the transition destination after a WFI instruction is executed.

When the SSBY bit is set to 1, the MCU enters Software Standby mode after execution of a WFI instruction. When the MCU returns to Normal mode from Software Standby mode by an interrupt, the SSBY bit remains 1. The SSBY bit can be cleared by writing 0 to it.

While the OSTDCR.OSTDE bit is 1, setting of the SSBY bit is ignored. Even if the SSBY bit is 1, the MCU enters Sleep mode on execution of a WFI instruction.

While the FENTRYR.FENTRY0 bit is 1 or the FENTRYR.FENTRYD bit is 1, setting of the SSBY bit is ignored. Even if the SSBY bit is 1, the MCU enters Sleep mode on execution of a WFI instruction.

10.2.2 Module Stop Control Register A (MSTPCRA)

Address(es): SYSTEM.MSTPCRA 4001 E01Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	MSTPA22	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b21 to b0	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b22	MSTPA22	Data Transfer Controller Module Stop*1	Target module: DTC 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b31 to b23	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

Note 1. When rewriting the MSTPA22 bit from 0 to 1, disable the DTC before setting the MSTPA22 bit.

10.2.3 Module Stop Control Register B (MSTPCRB)

Address(es): MSTP.MSTPCRB 4004 7000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MSTPB31	MSTPB30	—	—	—	—	—	—	—	MSTPB22	—	—	MSTPB19	MSTPB18	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	MSTPB11	—	MSTPB9	MSTPB8	—	—	—	MSTPB4	—	MSTPB2	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b1 to b0	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b2	MSTPB2	Controller Area Network 0 Module Stop*1	Target module: CAN0 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b3	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b4	MSTPB4	Digital Addressable Lighting Interface Module Stop	Target module: DALI 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b7 to b5	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b8	MSTPB8	I^2C Bus Interface 1 Module Stop	Target module: IIC1 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b9	MSTPB9	I^2C Bus Interface 0 Module Stop	Target module: IIC0 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b10	—	Reserved	This bit is read as 1. The write value should be 1.	R/W

Bit	Symbol	Bit name	Description	R/W
b11	MSTPB11	Universal Serial Bus 2.0 Full Speed Interface Module Stop*2	Target module: USBFS 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b17 to b12	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b18	MSTPB18	Serial Peripheral Interface 1 Module Stop	Target module: SPI1 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b19	MSTPB19	Serial Peripheral Interface 0 Module Stop	Target module: SPI0 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b21, b20	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b22	MSTPB22	Serial Communication Interface 9 Module Stop	Target module: SCI9 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b29 to b23	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b30	MSTPB30	Serial Communication Interface 1 Module Stop	Target module: SCI1 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b31	MSTPB31	Serial Communication Interface 0 Module Stop	Target module: SCI0 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W

Note 1. The MSTPB2 bit must be written while the oscillation of the clock controlled by this bit is stable. To enter Software Standby mode after writing this bit, wait for 2 CAN clock (CANMCLK) cycles after writing, then execute a WFI instruction.

Note 2. To enter Software Standby mode after writing to the MSTPB11 bit, wait for 2 USB clock (UCLK) cycles after writing, and then execute a WFI instruction.

10.2.4 Module Stop Control Register C (MSTPCRC)

Address(es): MSTP.MSTPCRC 4004 7004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MSTPC31	—	—	MSTPC28	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	MSTPC14	MSTPC13	—	—	—	—	—	—	—	—	—	MSTPC3	—	MSTPC1	MSTPC0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b0	MSTPC0	Clock Frequency Accuracy Measurement Circuit Module Stop*1	Target module: CAC 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b1	MSTPC1	Cyclic Redundancy Check Calculator Module Stop	Target module: CRC 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b2	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b3	MSTPC3	Capacitive Touch Sensing Unit Module Stop	Target module: CTSU 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b12 to b4	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b13	MSTPC13	Data Operation Circuit Module Stop	Target module: DOC 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W

Bit	Symbol	Bit name	Description	R/W
b14	MSTPC14	Event Link Controller Module Stop	Target module: ELC 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b27 to b15	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b28	MSTPC28	Random Number Generator Module Stop*2	Target module: TRNG 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b30, b29	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b31	MSTPC31	AES Module Stop	Target module: AES 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W

Note 1. The MSTPC0 bit must be written while the oscillation of the clock to be controlled by this bit is stable. To enter Software Standby mode after writing this bit, wait for 2 cycles of the slowest clock from the clocks output by the oscillators, and then execute a WFI instruction.

Note 2. Set the MSTPC28 bit once to 0 at the beginning of the program to initialize the unused circuit even if the TRNG is not used in this MCU. See section 10.9.15, Module-Stop Function for an Unused Circuit.

10.2.5 Module Stop Control Register D (MSTPCRD)

Address(es): MSTP.MSTPCRD 4004 7008h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MSTPD 31	—	MSTPD 29	MSTPD 28	MSTPD 27	MSTPD 26	—	—	—	—	—	—	MSTPD 19	—	—	MSTPD 16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	MSTPD 14	—	—	—	—	—	—	—	MSTPD 6	MSTPD 5	—	MSTPD 3	MSTPD 2	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b2	MSTPD2	Low Power Asynchronous General Purpose Timer 1 Module Stop*1	Target module: AGT1 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b3	MSTPD3	Low Power Asynchronous General Purpose Timer 0 Module Stop*2	Target module: AGT0 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b4	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b5	MSTPD5	General PWM Timer 320 Module Stop	Target module: GPT320 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b6	MSTPD6	General PWM Timer 16H1 to 16H3 and 164 to 166 and PWM Delay Generation Circuit Module Stop	Target module: GPT16H1 to GPT16H3, GPT164 to GPT166, and PWM delay generation circuit 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b13 to b7	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b14	MSTPD14	Port Output Enable for GPT Module Stop	Target module: POEG 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b15	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b16	MSTPD16	14-Bit A/D Converter Module Stop	Target module: ADC140 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b18, b17	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

Bit	Symbol	Bit name	Description	R/W
b19	MSTPD19	8-bit D/A Converter Module Stop	Target module: DAC8 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b25 to b20	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b26	MSTPD26	High-Speed Analog Comparator 2 Module Stop	Target module: ACMPHS2 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b27	MSTPD27	High-Speed Analog Comparator 1 Module Stop	Target module: ACMPHS1 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b28	MSTPD28	High-Speed Analog Comparator 0 Module Stop	Target module: ACMPHS0 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b29	MSTPD29	Low-Power Analog Comparator Module Stop	Target module: ACMPLP 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b30	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b31	MSTPD31	Operational Amplifier Module Stop	Target module: OPAMP 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W

Note 1. When the count source is sub-clock oscillator or LOCO, AGT1 counting does not stop even if MSTPD2 is set to 1. If the count source is the sub-clock oscillator or LOCO, this bit must be set to 1 except when accessing the AGT1 registers.

Note 2. When the count source is sub-clock oscillator or LOCO, AGT0 counting does not stop even if MSTPD3 is set to 1. If the count source is the sub-clock oscillator or LOCO, this bit must be set to 1 except when accessing the AGT0 registers.

10.2.6 Operating Power Control Register (OPCCR)

Address(es): SYSTEM.OPCCR 4001 E0A0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	OPCM TSF	—	—	OPCM[1:0]	
Value after reset:	0	0	0	0	0	0	1	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	OPCM[1:0]	Operating Power Control Mode Select	b1 b0 0 0: High-speed mode 0 1: Middle-speed mode 1 0: Low-voltage mode*1 1 1: Low-speed mode.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	OPCMTSF	Operating Power Control Mode Transition Status Flag	0: Transition completed 1: During transition.	R
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. HOCOCR.HCSTP must always be 0.

The OPCCR register is used to reduce power consumption in Normal mode, Sleep mode, and Snooze mode. Power consumption can be reduced according to the operating frequency and operating voltage used by the OPCCR setting.

For the procedure to change the operating power control modes, see section 10.5, Function for Lower Operating Power Consumption.

OPCM[1:0] bits (Operating Power Control Mode Select)

The OPCM[1:0] bits select the operating power control mode in Normal mode, Sleep mode, and Snooze mode.

Table 10.4 shows the relationship between the operating power control modes, the OPCM[1:0] and SOPCM bits settings.

Writing to OPCCR.OPCM[1:0] is prohibited while HOCOCR.HCSTP and OSCSF.HOCOSF are 0 as the oscillation of the HOCO clock is not stable yet.

OPCMTSF flag (Operating Power Control Mode Transition Status Flag)

The OPCMTSF flag indicates the switching control state when the operating power control mode is switched. This flag becomes 1 when the OPCM bit is written, and 0 when mode transition completed. Read this flag and confirm that it is 0 before proceeding.

10.2.7 Sub Operating Power Control Register (SOPCCR)

Address(es): SYSTEM.SOPCCR 4001 E0AAh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SOPCMTSF	—	—	—	SOPCM
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SOPCM	Sub Operating Power Control Mode Select	0: Not Subosc-speed mode 1: Subosc-speed mode.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	SOPCMTSF	Sub Operating Power Control Mode Transition Status Flag	0: Transition completed 1: During transition.	R
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The SOPCCR register is used to reduce power consumption in Normal mode, Sleep mode, and Snooze mode. Setting this register initiates the entry to and exit from Subosc-speed mode. Subosc-speed mode is available only when using the sub-clock oscillator or LOCO without dividing the frequency.

For the procedure to change operating power control modes, see section 10.5, Function for Lower Operating Power Consumption.

SOPCM bit (Sub Operating Power Control Mode Select)

The SOPCM bit selects the operating power control mode in Normal mode, Sleep mode, and Snooze mode. Setting this bit to 1 allows transition to Subosc-speed mode. Setting this bit to 0 allows a return to the operating mode (operating mode set by OPCCR.OPCM[1:0]) before the transition to Subosc-speed mode.

Table 10.4 shows the relationship between the operating power control modes, the OPCM[1:0] and SOPCM bits settings.

SOPCMTSF flag (Sub Operating Power Control Mode Transition Status Flag)

The SOPCMTSF flag indicates the switching control state when the operating power control mode is switched to or from Subosc-speed mode. This flag becomes 1 when the SOPCM bit is written, and 0 when mode transition is complete. Read this flag and confirm that it is 0 before proceeding.

Table 10.4 shows each operating power control mode.

Table 10.4 Operating power control mode

Operating power control mode	OPCM[1:0] bits	SOPCM bit	Power consumption
High-speed mode	00b	0	High
Middle-speed mode	01b	0	↓
Low-voltage mode	10b	0	
Low-speed mode	11b	0	
Subosc-speed mode	xxb	1	Low

10.2.8 Snooze Control Register (SNZCR)

Address(es): SYSTEM.SNZCR 4001 E092h

	b7	b6	b5	b4	b3	b2	b1	b0
	SNZE	—	—	—	—	—	SNZDTCEN	RXDREQEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RXDREQEN	RXD0/DRX0 Snooze Request Enable	0: Ignore RXD0 or DRX0 falling edge in Software Standby mode 1: Detect RXD0 or DRX0 falling edge in Software Standby mode.	R/W
b1	SNZDTCEN	DTC Enable in Snooze mode	Enable DTC operation in Snooze mode: 0: Disable DTC operation 1: Enable DTC operation.	R/W
b6 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	SNZE	Snooze mode Enable	0: Disable Snooze mode 1: Enable Snooze mode.	R/W

RXDREQEN bit (RXD0/DRX0 Snooze Request Enable)

- SCI0

The RXDREQEN bit specifies whether to detect a falling edge of the RXD0 pin in Software Standby mode. This bit is only available when SCI0 operates in asynchronous mode. To detect a falling edge of the RXD0 pin, set this bit before entering Software Standby mode. When this bit is set to 1, a falling edge of the RXD0 pin in Software Standby mode causes the MCU to enter Snooze mode.

- DALI

The RXDREQEN bit specifies whether to detect a falling edge of the DRX0 pin in Software Standby mode. To detect a falling edge of the DRX0 pin, set this bit before entering Software Standby mode. When this bit is set to 1, a falling edge of the DRX0 pin in Software Standby mode causes the MCU to enter Snooze mode.

Note: SCI0 and DALI must not be used in Snooze mode simultaneously. When RXDREQEN is 1, SCI0.RXD0 and DALI.DRX0 must not be selected with PSEL simultaneously.

SNZDTCEN bit (DTC Enable in Snooze mode)

The SNZDTCEN bit specifies whether to use the DTC and SRAM in Snooze mode. To use the DTC and SRAM in Snooze mode, set this bit to 1 before entering Software Standby mode. When this bit is set to 1, the DTC can be activated by setting IELSRn (ICU event link setting register n).

SNZE bit (Snooze mode Enable)

The SNZE bit specifies whether to enable a transition from Software Standby mode to Snooze mode. To use Snooze mode, set this bit to 1 before entering Software Standby mode. When this bit is set to 1, a trigger as shown in Table 10.6

in Software Standby mode causes the MCU to enter Snooze mode. After the MCU transfers from Software Standby mode or Snooze mode to Normal mode, clear the SNZE bit once then set it before re-entering Software Standby mode. For details, see section 10.8, Snooze Mode.

10.2.9 Snooze End Control Register (SNZEDCR)

Address(es): SYSTEM.SNZEDCR 4001 E094h

	b7	b6	b5	b4	b3	b2	b1	b0
	SCI0UMTED	—	—	AD0UMTED	AD0MATED	DTCNZRED	DTCZRED	AGTUNFED
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	AGTUNFED	AGT1 Underflow Snooze End Enable	0: Disable the Snooze end request 1: Enable the Snooze end request.	R/W
b1	DTCZRED	Last DTC Transmission Completion Snooze End Enable	0: Disable the Snooze end request 1: Enable the Snooze end request.	R/W
b2	DTCNZRED	Not Last DTC Transmission Completion Snooze End Enable	0: Disable the snooze end request 1: Enable the snooze end request.	R/W
b3	AD0MATED	ADC140 Compare Match Snooze End Enable	0: Disable the snooze end request 1: Enable the snooze end request.	R/W
b4	AD0UMTED	ADC140 Compare Mismatch Snooze End Enable	0: Disable the snooze end request 1: Enable the snooze end request.	R/W
b6, b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	SCI0UMTED	SCI0 Address Mismatch Snooze End Enable	0: Disable the snooze end request 1: Enable the snooze end request.	R/W

To use a trigger shown in Table 10.8 as a condition to switch from Snooze mode to Software Standby mode, set the associated bit in the SNZEDCR register to 1.

The event that is used to return to Normal mode from Snooze mode listed in Table 10.3 must not be enabled by SNZEDCR.

AGTUNFED bit (AGT1 Underflow Snooze End Enable)

The AGTUNFED bit specifies whether to enable a transition from Snooze mode to Software Standby mode by an AGT1 underflow. For details on the condition of the trigger, see section 22, Low Power Asynchronous General Purpose Timer (AGT).

DTCZRED bit (Last DTC Transmission Completion Snooze End Enable)

The DTCZRED bit specifies whether to enable a transition from Snooze mode to Software Standby mode by completion of the last DTC transmission, that is, CRA or CRB registers in the DTC is 0. For details on the condition of the trigger, see section 15, Data Transfer Controller (DTC).

DTCNZRED bit (Not Last DTC Transmission Completion Snooze End Enable)

The DTCNZRED bit specifies whether to enable a transition from Snooze mode to Software Standby mode by completion of each DTC transmission, that is, CRA or CRB registers in the DTC is not 0. For details on the condition of the trigger, see section 15, Data Transfer Controller (DTC).

AD0MATED bit (ADC140 Compare Match Snooze End Enable)

The AD0MATED bit specifies whether to enable a transition from Snooze mode to Software Standby mode by an ADC140 event when a conversion result matches the expected data. For details on the condition of the trigger, see section 33, 14-Bit A/D Converter (ADC14).

AD0UMTED bit (ADC140 Compare Mismatch Snooze End Enable)

The AD0UMTED bit specifies whether to enable a transition from Snooze mode to Software Standby mode by an ADC140 event when the conversion result does not match the expected data. For details on the condition of the trigger, see section 33, 14-Bit A/D Converter (ADC14).

SCI0UMTED bit (SCI0 Address Mismatch Snooze End Enable)

The SCI0UMTED bit specifies whether to enable a transition from Snooze mode to Software Standby mode by an SCI0 event when an address received in Software Standby mode does not match the expected data. For details on the condition of the trigger, see section 27, Serial Communications Interface (SCI). Only set this bit to 1 when SCI0 operates in asynchronous mode.

10.2.10 Snooze Request Control Register (SNZREQCR)

Address(es): SYSTEM.SNZREQCR 4001 E098h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	SNZREQEN30	SNZREQEN29	SNZREQEN28	—	—	SNZREQEN25	SNZREQEN24	SNZREQEN23	—	—	—	—	—	SNZREQEN17	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	SNZREQEN7	SNZREQEN6	SNZREQEN5	SNZREQEN4	SNZREQEN3	SNZREQEN2	SNZREQEN1	SNZREQEN0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SNZREQEN0	Snooze Request Enable 0	Enable IRQ0 pin Snooze request: 0: Disable the Snooze request 1: Enable the Snooze request.	R/W
b1	SNZREQEN1	Snooze Request Enable 1	Enable IRQ1 pin Snooze request: 0: Disable the Snooze request 1: Enable the Snooze request.	R/W
b2	SNZREQEN2	Snooze Request Enable 2	Enable IRQ2 pin Snooze request: 0: Disable the Snooze request 1: Enable the Snooze request.	R/W
b3	SNZREQEN3	Snooze Request Enable 3	Enable IRQ3 pin Snooze request: 0: Disable the Snooze request 1: Enable the Snooze request.	R/W
b4	SNZREQEN4	Snooze Request Enable 4	Enable IRQ4 pin Snooze request: 0: Disable the Snooze request 1: Enable the Snooze request.	R/W
b5	SNZREQEN5	Snooze Request Enable 5	Enable IRQ5 pin Snooze request: 0: Disable the Snooze request 1: Enable the Snooze request.	R/W
b6	SNZREQEN6	Snooze Request Enable 6	Enable IRQ6 pin Snooze request: 0: Disable the Snooze request 1: Enable the Snooze request.	R/W
b7	SNZREQEN7	Snooze Request Enable 7	Enable IRQ7 pin Snooze request: 0: Disable the Snooze request 1: Enable the Snooze request.	R/W
b16 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b17	SNZREQEN17	Snooze Request Enable 17	Enable Key Interrupt Snooze request: 0: Disable the Snooze request 1: Enable the Snooze request.	R/W
b22 to b18	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit name	Description	R/W
b23	SNZREQEN23	Snooze Request Enable 23	Enable ACMPLP0 Snooze request: 0: Disable the Snooze request 1: Enable the Snooze request.	R/W
b24	SNZREQEN24	Snooze Request Enable 24	Enable RTC alarm Snooze request: 0: Disable the Snooze request 1: Enable the Snooze request.	R/W
b25	SNZREQEN25	Snooze Request Enable 25	Enable RTC period Snooze request: 0: Disable the Snooze request 1: Enable the Snooze request.	R/W
b27, b26	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b28	SNZREQEN28	Snooze Request Enable 28	Enable AGT1 underflow Snooze request: 0: Disable the Snooze request 1: Enable the Snooze request.	R/W
b29	SNZREQEN29	Snooze Request Enable 29	Enable AGT1 compare match A Snooze request: 0: Disable the Snooze request 1: Enable the Snooze request.	R/W
b30	SNZREQEN30	Snooze Request Enable 30	Enable AGT1 compare match B Snooze request: 0: Disable the Snooze request 1: Enable the Snooze request.	R/W
b31	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

The SNZREQCR register controls the trigger that causes the MCU to switch from Software Standby mode to Snooze mode. If a trigger is selected as a request to cancel Software Standby mode by setting the WUPEN register, see section 12, Interrupt Controller Unit (ICU), the MCU enters Normal mode when the trigger is generated while the associated bit of the SNZREQCR is 1. The setting of the WUPEN register always has higher priority than the setting of the SNZREQCR register. For details, see section 10.8, Snooze Mode and section 12, Interrupt Controller Unit (ICU).

10.2.11 Flash Operation Control Register (FLSTOP)

Address(es): SYSTEM.FLSTOP 4001 E09Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	FLSTPF	—	—	—	FLSTOP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	FLSTOP	Selecting On/Off of the Flash Memory Operation	0: Code flash and data flash memory operates 1: Code flash and data flash memory stops.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	FLSTPF	Flash Memory Operation Status Flag	0: Transition completed 1: During transition (from the flash-stop-status to flash-operating-status or flash-operating-status to flash-stop-status).	R
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

FLSTOP bit (Selecting On/Off of the Flash Memory Operation)

The FLSTOP bit enables or disables flash memory. The FLSTOP bit must be written in a program executing in the SRAM. To use an interrupt when the FLSTOP bit is 1, be sure to place the interrupt vector in the SRAM. Set this bit to 0 when low voltage mode is not selected.

Note 1. When changing the value of the FLSTOP bit from 1 to 0 to start flash memory operation, ensure the FLSTPF flag is 0 and OSCSF.HOCOSF is 1 before restarting access to the flash memory. After that, instructions can be executed in the code flash memory.

Note 2. Writing to FLSTOP.FLSTOP is prohibited while the HOCOCR.HCSTP and OSCSF.HOCOSF bits are 0 (HOCO is in stabilization wait counting).

FLSTPF flag (Flash Memory Operation Status Flag)

The FLSTPF flag indicates the status of the transition from the flash-stop-status to flash-operating-status or from the flash-operating-status to the flash-stop-status. When the transition completes, the flag is read as 0. When using flash memory again after stopping it once, make sure that the FLSTPF flag is 0 before proceeding.

10.2.12 System Control OCD Control Register (SYOCDCR)

Address(es): SYSTEM.SYOCDCR 4001 E40Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	DBGEN	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	DBGEN	Debugger Enable bit	0: On-chip debugger is disabled 1: On-chip debugger is enabled. Set to 1 first in on-chip debug mode.	R/W

DBGEN bit (Debugger Enable bit)

DBGEN bit enables the on-chip debug mode. This bit must be set to 1 first in the on-chip debugger mode.

[Setting condition]

- Writing 1 to the bit when the debugger is connected.

[Clearing condition]

- Power-on reset is generated
- Writing 0 to the bit.

10.3 Reducing Power Consumption by Switching Clock Signals

When the SCKDIVCR.ICK[2:0], PCKB[2:0], and PCKD[2:0] bits are set, the clock frequency changes. The CPU, DTC, Flash, and SRAM use the operating clock specified in the ICK[2:0] bits.

Peripheral modules use the operating clock specified in the PCKB[2:0] and PCKD[2:0] bits.

The flash memory interface uses the operating clock specified in the ICK[2:0] bits.

For details, see section 8, Clock Generation Circuit.

10.4 Module-Stop Function

The module-stop function can be set for each on-chip peripheral module.

When the MSTPmi bit (m = A to D; i = 31 to 0) in MSTPCRA to MSTPCRD is set to 1, the specified module stops operating and enters the module-stop state, but the CPU continues to operate independently. Clearing the MSTPmi bit to 0 cancels the module-stop state, allowing the module to resume operation at the end of the bus cycle.

The internal states of modules are retained in the module-stop state.

After a reset is canceled, all modules other than the DTC is placed in the module-stop state. Do not access the module while the corresponding MSTPmi bit is 1, otherwise the read/write data or the operation of the module is not guaranteed. Also, do not set 1 to the MSTPmi bit while the corresponding module is accessed.

10.5 Function for Lower Operating Power Consumption

By selecting an appropriate operating power consumption control mode according to the operating frequency and operating voltage, power consumption can be reduced in Normal mode, Sleep mode, and Snooze mode.

10.5.1 Setting Operating Power Control Mode

Make sure that the operating condition such as the voltage range and the frequency range is always within the specified range before and after switching the operating power control modes.

This section provides example procedures for switching operating power control modes.

Table 10.5 Available oscillators in each mode

Mode	Oscillator					
	High-Speed on-chip oscillator	Middle-Speed on-chip oscillator	Low-Speed on-chip oscillator	Main clock oscillator	Sub-clock oscillator	IWDT-dedicated on-chip oscillator
High-Speed	Available	Available	Available	Available	Available	Available
Middle-Speed	Available	Available	Available	Available	Available	Available
Low-Voltage	Available	Available	Available	Available	Available	Available
Low-Speed	Available	Available	Available	Available	Available	Available
Subosc-Speed	N/A	N/A	Available	N/A	Available	Available

(1) Switching from a higher power mode to a lower power mode

Example 1: From High-speed mode to Low-speed mode:

(Operation in High-speed mode)

1. Change the oscillator to what is used in Low-speed mode. Set the frequency of each clock lower than or equal to the maximum operating frequency in Low-speed mode.
2. Turn off the oscillator that is not required in Low-speed mode.
3. Confirm that the OPCCR.OPCMTSF flag is 0 (indicates transition completed).
4. Set the OPCCR.OPCM bit to 11b (Low-speed mode).
5. Confirm that OPCCR.OPCMTSF flag is 0 (indicates transition completed).

(Operation in Low-speed mode)

Example 2: From High-speed mode to Subosc-speed mode

(Operation in High-speed mode)

1. Switch the clock source to sub-clock oscillator. Turn off HOCO, MOCO, and main oscillator
2. Confirm that all clock sources other than the sub-clock oscillator are stopped
3. Confirm that the SOPCCR.SOPCMTSF flag is 0 (indicates transition completed)
4. Set the SOPCCR.SOPCM bit to 1 (Subosc-speed mode)
5. Confirm that the SOPCCR.SOPCMTSF flag is 0 (indicates transition completed)

(Operation in Subosc-speed mode)

(2) Switching from a lower power mode to a higher power mode

Example 1: From Subosc-speed mode to High-speed mode

(Operation in Subosc-speed mode)

1. Confirm that the SOPCCR.SOPCMTSF flag is 0 (indicates transition completed)
2. Set SOPCCR.SOPCM bit to 0 (High-speed mode)
3. Confirm that SOPCCR.SOPCMTSF flag is 0 (indicates transition completed)
4. Turn on the oscillator needed in High-speed mode
5. Set the frequency of each clock to lower than or equal to the maximum operating frequency for High-speed mode

(Operation in High-speed mode)

Example 2: From Low-speed mode to High-speed mode

(Operation in Low-speed mode)

↓

Confirm that OPCCR.OPCMTSF flag is 0 (indicates transition completed)

↓

Set the OPCCR.OPCM bit to 00b (High-speed mode)

↓

Confirm that the OPCCR.OPCMTSF flag is 0 (indicates transition completed)

↓

Turn on any oscillator needed in High-speed mode

↓

Set the frequency of each clock to lower than or equal to the maximum operating frequency for High-speed mode

↓

(Operation in High-speed mode)

10.5.2 Operating Range

High-speed mode

The maximum operating frequency during flash read is 32 MHz for ICLK. The operating voltage range is 2.4 to 5.5 V during flash read. However, for ICLK, the maximum operating frequency during flash read is 16 MHz when the operating voltage is 2.4 V or larger and smaller than 2.7 V.

During flash programming/erasure, the operating frequency range is 1 to 32 MHz and the operating voltage range is 2.7 to 5.5 V.

Figure 10.2 shows the operating voltages and frequencies in High-speed mode.

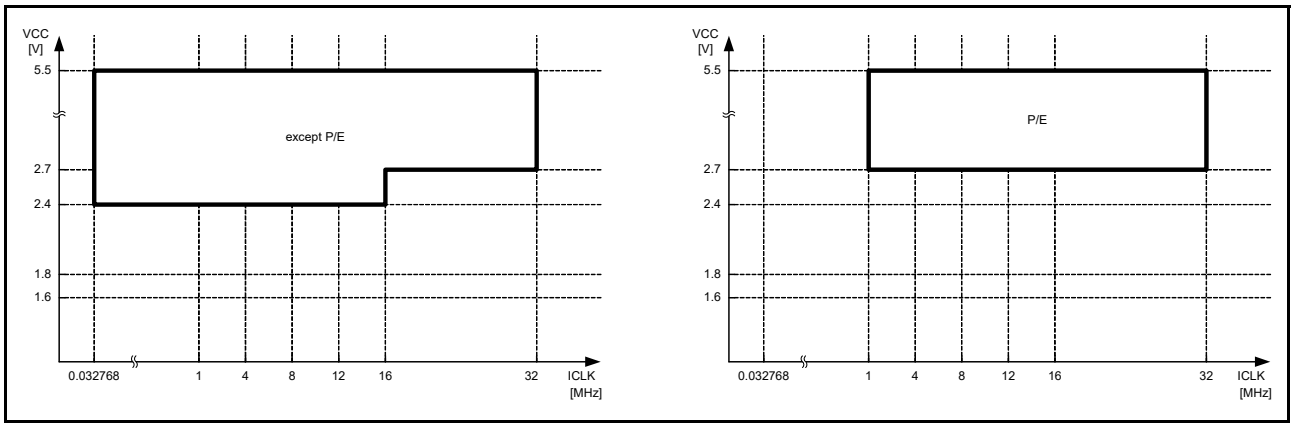


Figure 10.2 Operating voltages and frequencies in High-speed mode

Middle-speed mode

The power consumption of this mode is lower than that of High-speed mode under the same conditions.

The maximum operating frequency during flash read is 12 MHz for ICLK. The operating voltage range is 1.8 to 5.5 V during flash read. However, for ICLK, the maximum operating frequency during flash read is 8 MHz when the operating voltage is 1.8 V or larger and smaller than 2.4 V.

During flash programming/erasure, the operating frequency range is 1 to 12 MHz and the operating voltage range is 1.8 to 5.5 V. The maximum operating frequency during flash programming/erasure is 8 MHz when the operating voltage is 1.8 V or larger and smaller than 2.4 V.

Figure 10.3 shows the operating voltages and frequencies in Middle-speed mode.

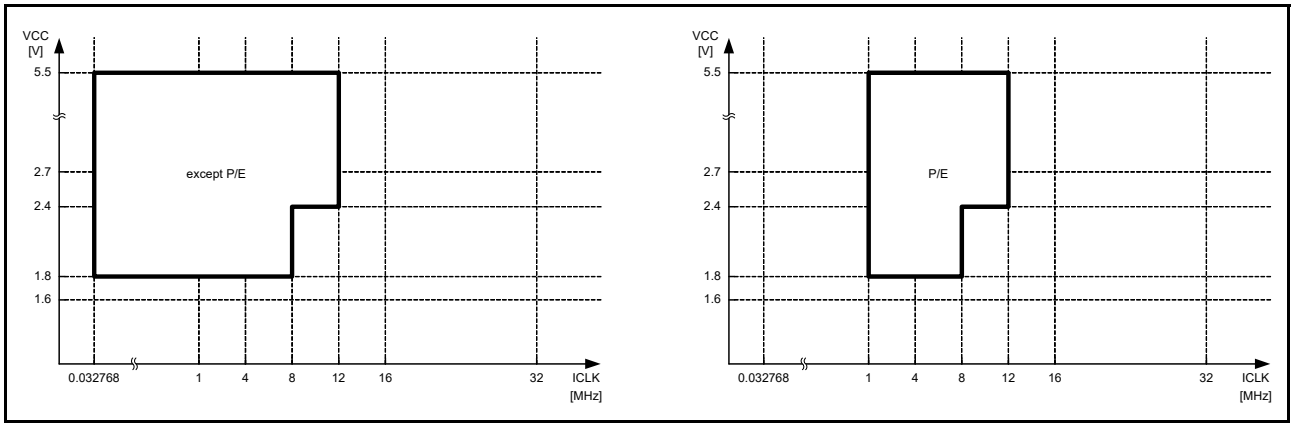


Figure 10.3 Operating voltages and frequencies in Middle-speed mode

Low-voltage mode

After a reset is canceled, operation is started from this mode.

The maximum operating frequency during flash read is 4 MHz for ICLK. The operating voltage range is 1.6 to 5.5 V during flash read.

During flash programming/erasure, the operating frequency range is 1 to 4 MHz and the operating voltage range is 1.8 to 5.5 V.

Figure 10.4 shows the operating voltages and frequencies in Low-voltage mode.

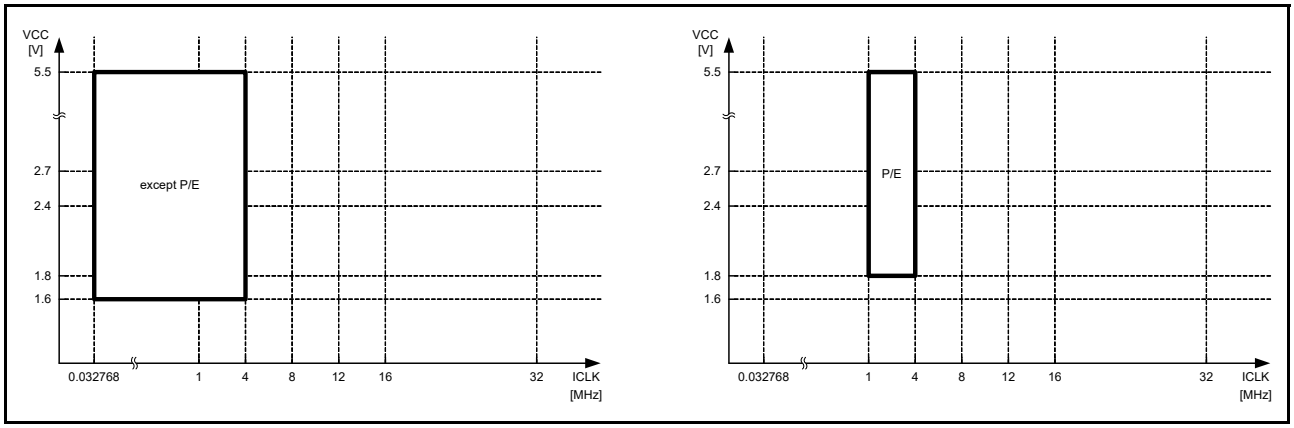


Figure 10.4 Operating voltages and frequencies in Low-voltage mode

Low-speed mode

The maximum operating frequency during flash read is 1 MHz for ICLK. The operating voltage range is 1.8 to 5.5 V during flash read.

P/E operations for flash memory are prohibited.

Figure 10.5 shows the operating voltages and frequencies in Low-speed mode.

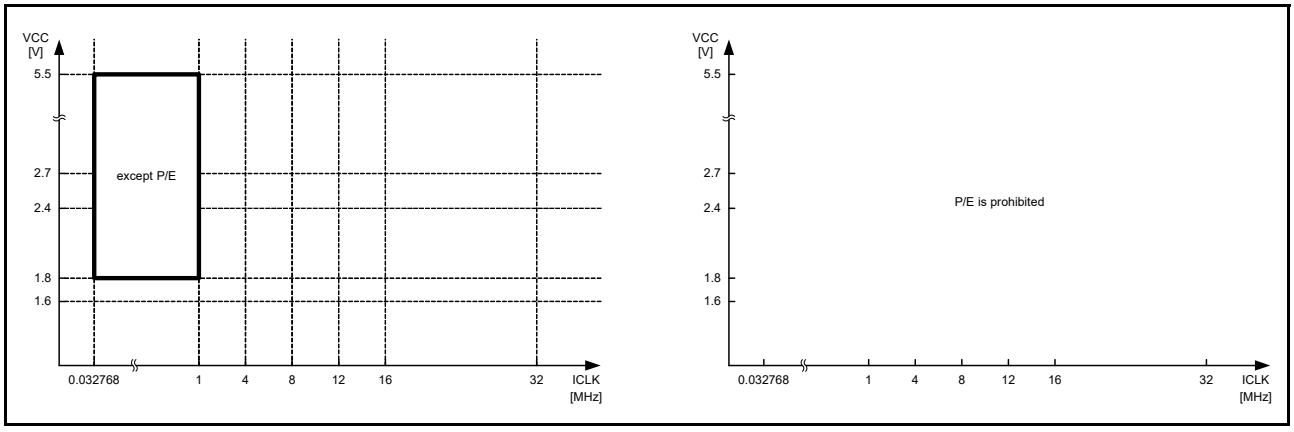


Figure 10.5 Operating voltages and frequencies in Low-speed mode

Subosc-speed mode

The maximum operating frequency during flash read is 37.6832 kHz for ICLK. The operating voltage range is 1.8 to 5.5 V during flash read. P/E operations for flash memory are prohibited.

Using the oscillators other than the sub-clock oscillator or low-speed on-chip oscillator is prohibited.

Figure 10.6 shows the operating voltages and frequencies in Subosc-speed mode.

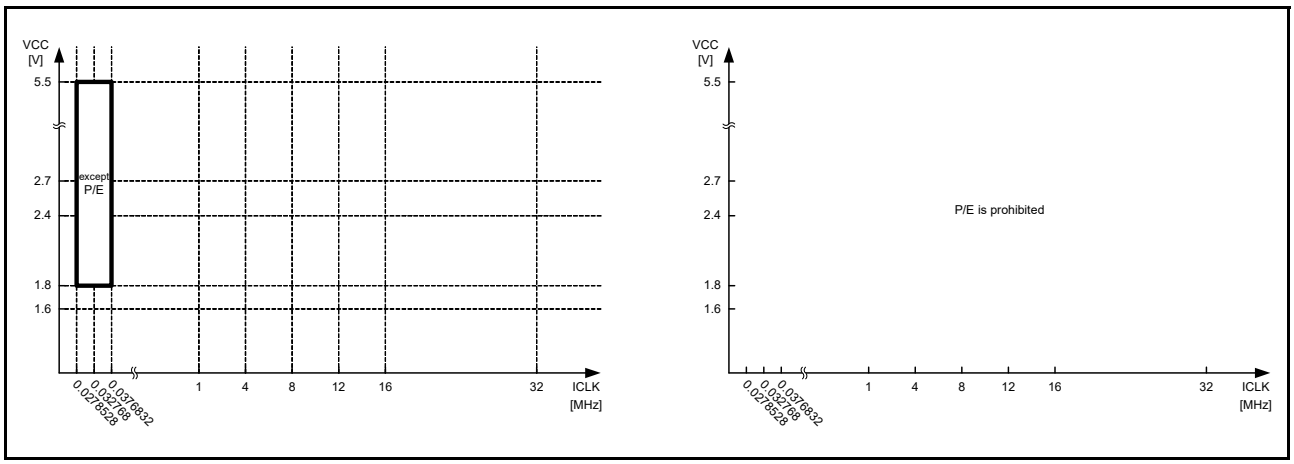


Figure 10.6 Operating voltages and frequencies in Subosc-speed mode

10.6 Sleep Mode

10.6.1 Transition to Sleep Mode

When a WFI instruction is executed while SBYCR.SSBY bit is 0, the MCU enters Sleep mode. In this mode, the CPU stops operating but the contents of its internal registers are retained. Other peripheral functions do not stop. Available resets or interrupts in Sleep mode cause the MCU to cancel Sleep mode. All interrupt sources are available. If using an interrupt to cancel Sleep mode, you must set the associated IELSRn register before executing a WFI instruction. For details, see section 12, Interrupt Controller Unit (ICU).

Counting by IWDT stops when the MCU enters Sleep mode while the IWDT is in auto-start mode and the OFS0.IWDTSTPCTL bit is 1 (IWDT stops in Sleep mode, Software Standby mode or Snooze mode).

Counting by IWDT continues when the MCU enters Sleep mode while the IWDT is in auto-start mode and the OFS0.IWDTSTPCTL bit is 0 (IWDT does not stop in Sleep mode, Software Standby mode or Snooze mode).

Counting by WDT stops when the MCU enters Sleep mode while the WDT is in auto-start mode and the OFS0.WDTSTPCTL bit is 1 (WDT stops in Sleep mode). Similarly, counting by WDT stops when the MCU enters Sleep mode while the WDT is in register start mode and the WDTCSTPR.SLCSTP bit in is 1 (WDT stops in Sleep

mode).

Counting by WDT continues when the MCU enters Sleep mode while the WDT is in auto-start mode and the OFS0. WDTSTPCTL bit is 0 (WDT does not stop in Sleep mode). Similarly, counting by WDT continues when the MCU enters Sleep mode while the WDT is in register start mode and the WDTCSTPR.SLCSTP bit is 0 (WDT does not stop in Sleep mode).

10.6.2 Canceling Sleep Mode

Sleep mode is canceled by any interrupt, RES pin reset, a power-on reset, a voltage monitor reset, an SRAM parity error reset, an SRAM ECC error reset, bus master MPU error reset, bus slave MPU error reset, or a reset caused by an IWDT or a WDT underflow.

1. Canceling by an interrupt
   When an interrupt request is generated, Sleep mode is canceled and the MCU starts interrupt handling.
2. Canceling by RES pin reset
   When RES pin is driven low, the MCU enters the reset state. Make sure to keep RES pin low for the time period specified in section 46, Electrical Characteristics. When RES pin is driven high after the specified time period, the CPU starts the reset exception handling.
3. Canceling by IWDT reset
   Sleep mode is canceled by an internal reset generated by an IWDT underflow and the MCU starts the reset exception handling. However, IWDT stops in Sleep mode and an internal reset for canceling Sleep mode is not generated in the following conditions:
   - OFS0.IWDTSTRT = 0 and OFS0.IWDTSTPCTL = 1.
4. Canceling by WDT reset
   Sleep mode is canceled by an internal reset generated by a WDT underflow and the MCU starts the reset exception handling. However, WDT stops in Sleep mode even when counting in Normal mode and an internal reset for canceling Sleep mode is not generated in the following conditions:
   - OFS0.WDTSTRT = 0 (auto-start mode) and OFS0.WDTSTPCTL = 1
   - OFS0.WDTSTRT = 1 (register start mode) and WDTCSTPR.SLCSTP = 1.
5. Canceling by other resets available in Sleep mode
   Sleep mode is canceled by other resets and the MCU starts the reset exception handling.

Note: For details on proper setting for interrupt, see section 12, Interrupt Controller Unit (ICU).

10.7 Software Standby Mode

10.7.1 Transition to Software Standby Mode

When a WFI instruction is executed while SBYCR.SSBY bit is 1, the MCU enters Software Standby mode. In this mode, the CPU, most of the on-chip peripheral functions and oscillators stop. However, the contents of the CPU internal registers and SRAM data, the states of on-chip peripheral functions and the I/O Ports are retained. Software Standby mode allows a significant reduction in power consumption because most of the oscillators stops in this mode. Table 10.2 shows the status of each on-chip peripheral functions and oscillators. Available resets or interrupts in Software Standby mode cause the MCU to cancel Software Standby mode. See Table 10.3 for available interrupt sources and section 12.2.8 Wake Up Interrupt Enable Register (WUPEN) for information on how to wake up the MCU from Software Standby mode. If using an interrupt to cancel Software Standby mode, you must set the associated IELSRn register before executing a WFI instruction. For details, see section 12, Interrupt Controller Unit (ICU).

Clear the DTCST.DTCST bit to 0 before executing WFI instruction except when using DTC in Snooze mode. If DTC is required in Snooze mode, set the DTCST.DTCST bit to 1 before executing a WFI instruction.

Counting by IWDT stops when the MCU enters Software Standby mode while the IWDT is in auto-start mode and the OFS0.IWDTSTPCTL bit is 1 (IWDT stops in Sleep mode, Software Standby mode and Snooze mode). Counting by IWDT continues if the MCU enters Software Standby mode while the IWDT is in auto-start mode and the OFS0.IWDTSTPCTL bit is 0 (IWDT does not stop in Sleep, Software Standby, or Snooze mode).

WDT stops counting when the MCU enters Software Standby mode.

Do not enter Software Standby mode while OSTDCR.OSTDE = 1 (oscillation stop detection function is enabled). To enter Software Standby mode, execute a WFI instruction after disabling the oscillation stop detection function (OSTDCR.OSTDE = 0). If executing a WFI instruction while OSTDCR.OSTDE = 1, the MCU enters Sleep mode even when SBYCR.SSBY = 1. In addition, do not enter Software Standby mode while the flash memory performs a programming or erasing procedure. To enter Software Standby mode, execute a WFI instruction after the programming or erasure procedure completes.

10.7.2 Canceling Software Standby Mode

Software Standby mode is canceled by an available interrupt shown in Table 10.3, RES pin reset, a power-on reset, a voltage monitor reset, or a reset caused by an IWDT underflow.

The oscillators that operate before the transition to Software Standby mode restart. After all the oscillators are stabilized, the MCU returns to Normal mode from Software Standby mode. See section 12.2.8 Wake Up Interrupt Enable Register (WUPEN) for information on how to wake up the MCU from Software Standby mode.

You can cancel Software Standby mode in any of the following ways:

1. Canceling by an interrupt
   When an available interrupt request (for available interrupts, see Table 10.3) is generated, an oscillator that operates before the transition to Software Standby mode restarts. After all the oscillators are stabilized, the MCU returns to Normal mode from Software Standby mode and starts the interrupt handling.
2. Canceling by a RES pin reset
   When the RES pin is driven low, the MCU enters the reset state, and the oscillators whose default status is operating, start the oscillation. Be sure to keep the RES pin low for the time period specified in section 46, Electrical Characteristics. When the RES pin is driven high after the specified time period, the CPU starts the reset exception handling.
3. Canceling by a power-on reset
   Software Standby mode is canceled by a power-on reset and the MCU starts the reset exception handling.
4. Canceling by a voltage monitor reset
   Software Standby mode is canceled by a voltage monitor reset from the voltage detection circuit and the MCU starts the reset exception handling.
5. Canceling by IWDT reset
   Software Standby mode is canceled by an internal reset generated by an IWDT underflow and the MCU starts the reset exception handling. However, IWDT stops in Software Standby mode and an internal reset for canceling Software Standby mode is not generated in the following condition:
   - OFS0.IWDTSTRT = 0 and OFS0.IWDTSTPCTL = 1.

10.7.3 Example of Software Standby Mode Application

Figure 10.7 shows an example of entry to Software Standby mode on detection of a falling edge of the IRQn pin, and exit from Software Standby mode on a rising edge of the IRQn pin.

In this example, an IRQn pin interrupt is accepted with the IRQCRi.IRQMD[1:0] bits of the ICU set to 00b (falling edge) in Normal mode, and the IRQCRi.IRQMD[1:0] bits are set to 01b (rising edge). Then, the SBYCR.SSBY bit is set to 1 and a WFI instruction is executed. As a result, entry to Software Standby mode completes and exit from Software Standby mode is initiated on a rising edge of the IRQn pin.

Setting the ICU is also required to exit Software Standby mode. For details, see section 12, Interrupt Controller Unit (ICU). The oscillation stabilization time in Figure 10.7 is specified in section 46, Electrical Characteristics.

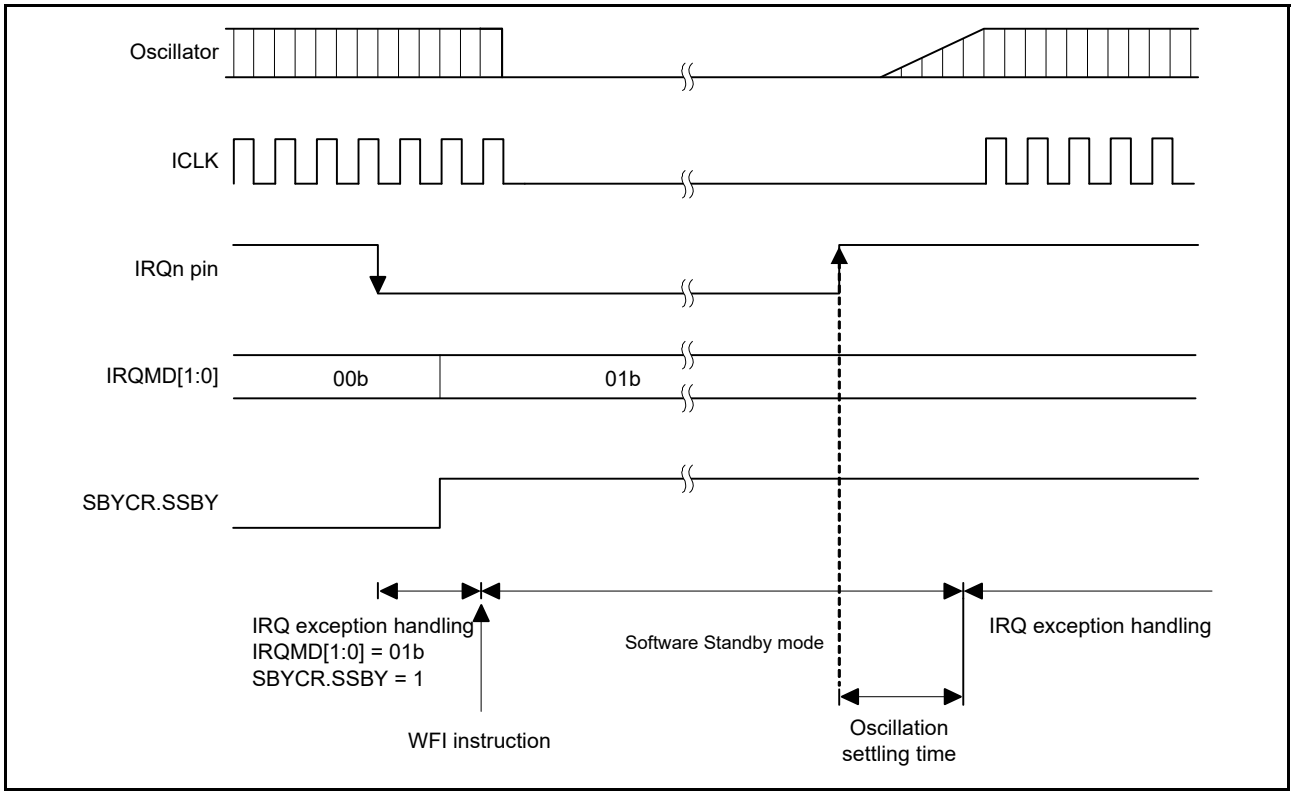


Figure 10.7 Example of Software Standby mode application

10.8 Snooze Mode

10.8.1 Transition to Snooze Mode

Figure 10.8 shows the Snooze mode entry configuration. When the Snooze control circuit receives a Snooze request in Software Standby mode, the MCU transitions to Snooze mode. In this mode, some peripheral modules operate without waking up the CPU. The peripheral modules that can operate in Snooze mode are shown in Table 10.2, Operating conditions of each low power mode. DTC operation in Snooze mode can also be selected by setting the SNZCR.SNZDTCEN bit.

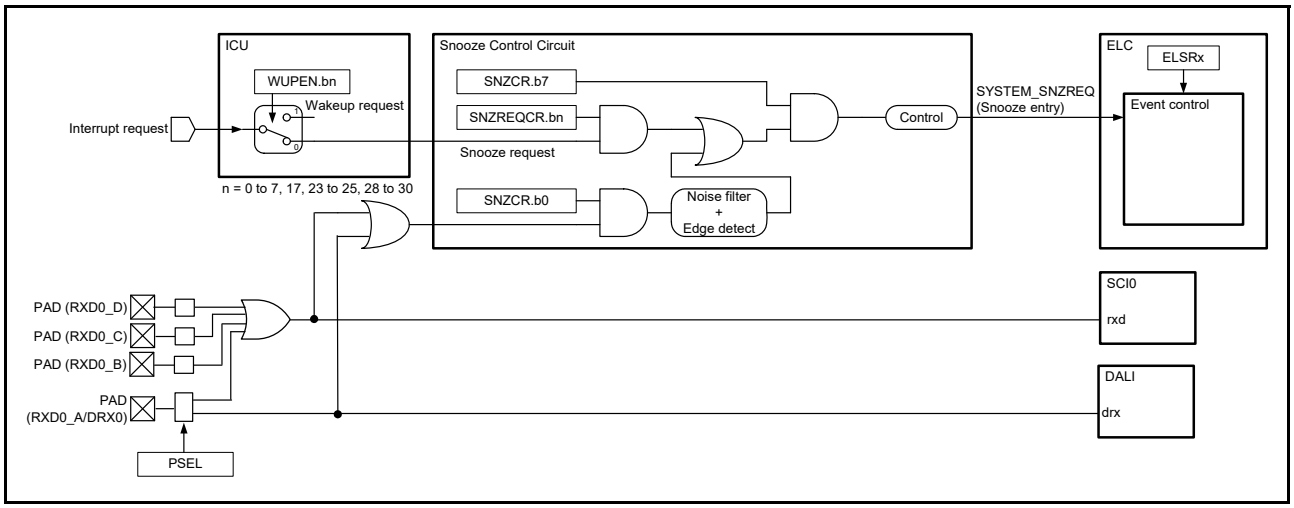


Figure 10.8 Snooze mode entry configuration

Table 10.6 shows the Snooze requests to switch from Software Standby mode to Snooze mode. To use the listed Snooze requests as a trigger to switch to Snooze mode, the associated SNZREQENn bit of the SNZREQCR register or

RXDREQEN bit of the SNZCR register must be set before entering Software Standby mode. Do not enable multiple Snooze requests at the same time.

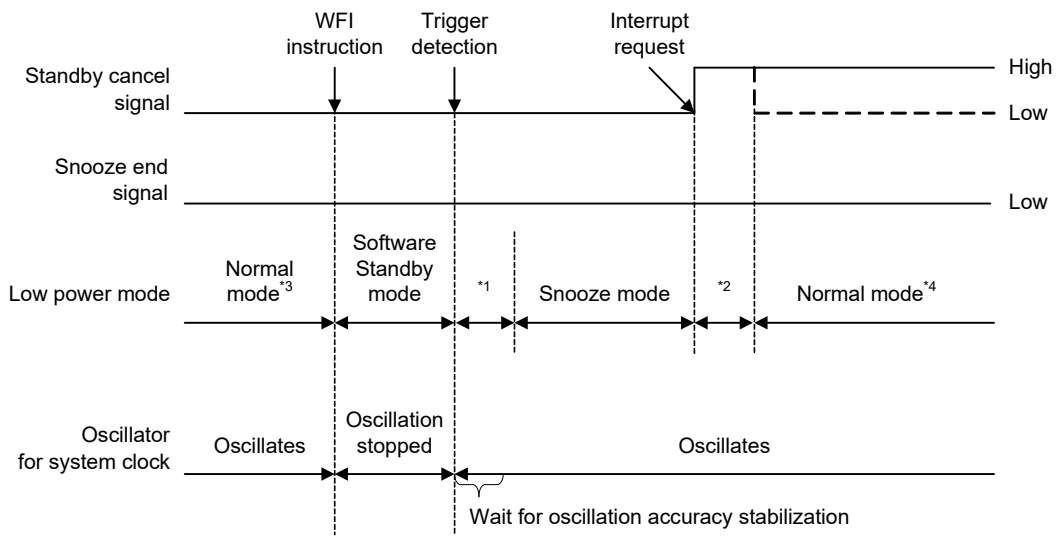
Table 10.6 Available Snooze requests to switch to Snooze mode

	Control Register	
Snooze request	**Register**	**Bit**
PORT_IRQn (n = 0 to 7)	SNZREQCR	SNZREQENn (n = 0 to 7)
KEY_INTKR	SNZREQCR	SNZREQEN17
ACMP_LP0	SNZREQCR	SNZREQEN23
RTC_ALM	SNZREQCR	SNZREQEN24
RTC_PRD	SNZREQCR	SNZREQEN25
AGT1_AGTI	SNZREQCR	SNZREQEN28
AGT1_AGTCMAI	SNZREQCR	SNZREQEN29
AGT1_AGTCMBI	SNZREQCR	SNZREQEN30
RXD0 or DRX0 falling edge	SNZCR	RXDREQEN*1

Note 1. RXDREQEN bit must not be set to 1 unless in asynchronous mode.

10.8.2 Canceling Snooze Mode

Snooze mode is canceled by an interrupt request that is available in Software Standby mode or any reset. Table 10.3 shows the requests that can be used to exit each mode. After canceling the Snooze mode, the MCU enters Normal mode and proceeds with exception processing for the given interrupt or reset. The action triggered by the interrupt requests, that is selected by SELSR0, cancels Snooze mode. Interrupt canceling Snooze mode must be selected by IELSRn (n = 0 to 31) to link to the NVIC for the corresponding interrupt handling. See section 12, Interrupt Controller Unit (ICU) for the setting of SELSR0 and IELSRn.



Note 1. Transition time from Software Standby mode to Snooze mode.
Note 2. Transition time from Snooze mode to Normal mode.
Note 3. Enable Snooze mode (SNZCR.SNZE = 1) immediately before switching to Software Standby mode.
Note 4. Be sure to disable Snooze mode (SNZCR.SNZE = 0) immediately after returning to Normal mode.

Figure 10.9 When interrupt request signal is generated in Snooze mode

10.8.3 Return to Software Standby Mode

Table 10.7 shows the snooze end request that can be used as triggers to return to Software Standby mode. The snooze end requests are available only in Snooze mode. If the requests are generated when the MCU is not in Snooze mode, they are

ignored. When multiple requests are selected, each of the requests invokes transition to Software Standby mode from Snooze mode.

Table 10.8 shows the Snooze end conditions that consist of the Snooze end requests and the conditions of the peripheral modules. CTSU, SCI0, ADC140, and DTC can keep the MCU in Snooze mode until they complete operation. However, an AGT1 underflow as a trigger to return to Software Standby mode cancels Snooze mode without waiting for the completion of SCI0 operation.

Figure 10.10 shows the timing diagram for the transition from Snooze mode to Software Standby mode. This mode transition occurs according to the Snooze end requests set in the SNZEDCR register. A Snooze request is cleared automatically after the transition to Software Standby mode.

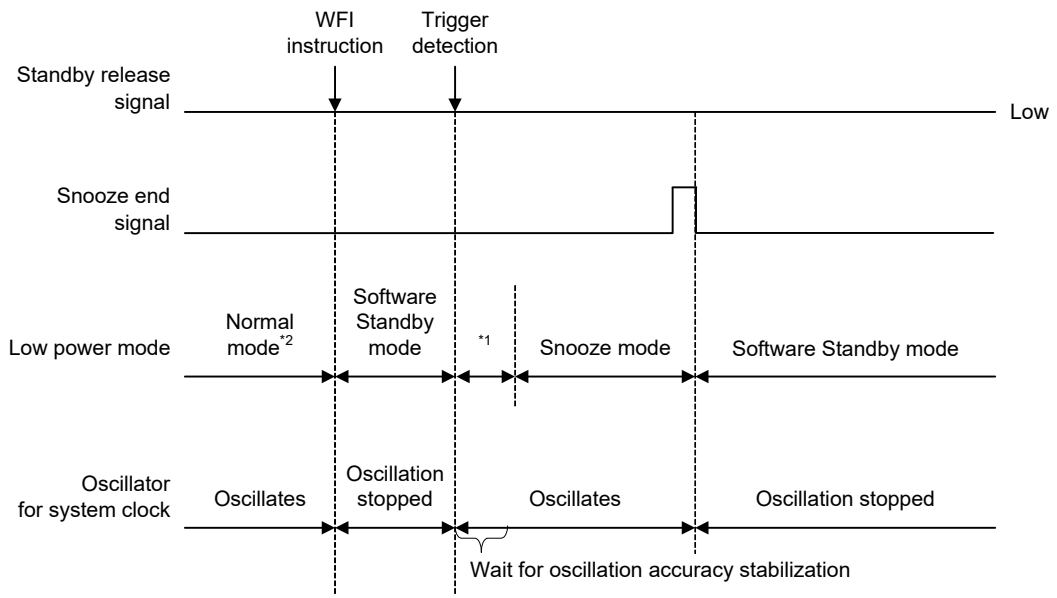
Table 10.7 Available snooze end requests (triggers to return to Software Standby mode)

Snooze end request	Enable/Disable control	
	Register	Bit
AGT1 underflow or measurement complete (AGT1_AGTI)	SNZEDCR	b0
DTC transfer completion (DTC_COMPLETE)	SNZEDCR	b1
Not DTC transfer completion (DTC_TRANSFER)	SNZEDCR	b2
ADC140 window A/B compare match (ADC140_WCMPM)	SNZEDCR	b3
ADC140 window A/B compare mismatch (ADC140_WCMPUM)	SNZEDCR	b4
SCI0 address mismatch (SCI0_DCUF)	SNZEDCR	b7

Table 10.8 Snooze end conditions

Operating module when a snooze end request occurs	Snooze end request	
	AGT1 underflow	Other than AGT1 underflow
DTC	The MCU transfers to the Software Standby mode after all of the modules listed to the left of this column complete operation.	The MCU transfers to the Software Standby mode after all of the modules listed to the left complete operation.
ADC140		
CTSU		
SCI0	The MCU transitions to the Software Standby mode immediately after a snooze end request is generated.	
Other than above	The MCU transfers to the Software Standby mode immediately after a snooze end request is generated.	

Note: If the DTC is used to activate the ADC140, CTSU, or SCI, the MCU transitions to software standby mode after a snooze end request is generated.



Note 1. Transition time from Software Standby mode to Snooze mode.
Note 2. Enable Snooze mode (SNZCR.SNZE = 1) immediately before switching to Software Standby mode.

Figure 10.10 When interrupt request signal is not generated in Snooze mode

10.8.4 Snooze Operation Example

Figure 10.11 shows an example setting for using ELC in Snooze mode.

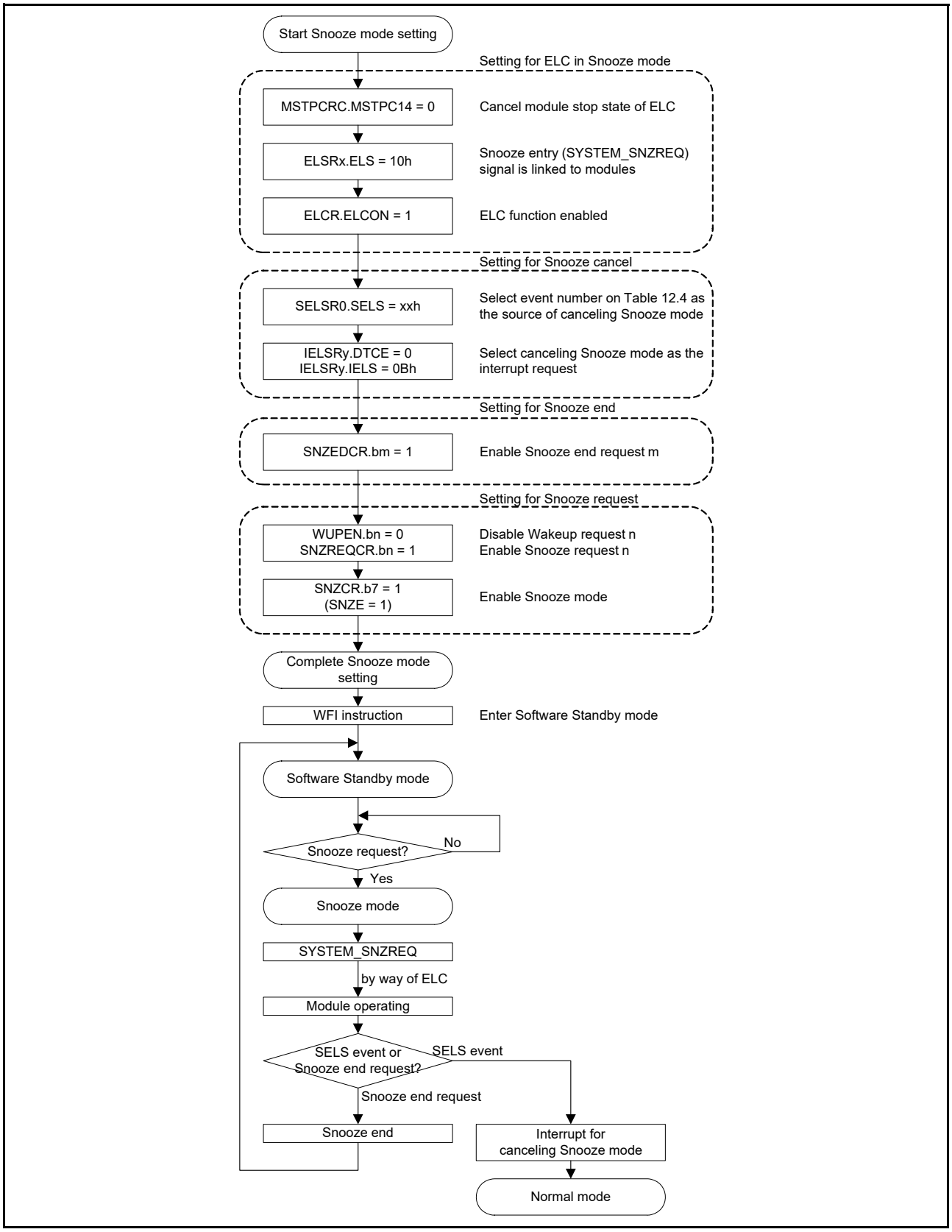


Figure 10.11 Setting example of using ELC in Snooze mode

The MCU can transmit and receive data in SCI0 asynchronous mode or the DALI without CPU intervention. When using the SCI0 or DALI in Snooze mode, use one of the following operating modes:

- High-speed mode
- Middle-speed mode
- Low-speed mode.

Do not use Low-voltage mode or Subosc-speed mode. Table 10.9 and Table 10.10 show the maximum transfer rate of SCI0 in Snooze mode. When using the SCI0 in Snooze mode, the following settings must be used:

- BGDM = 0
- ABCS = 0
- ABCSE = 0.

See section 27, Serial Communications Interface (SCI) for information on these bits.

High-speed mode, Middle-speed mode, Low-speed mode

Table 10.9 HOCO: ± 1.0% (Ta = -20 to 85°C) **(Unit: bps)**

Maximum division ratio of ICLK, PCLKB, and PCLKD	HOCO frequency			
	24 MHz	32 MHz	48 MHz	64 MHz
1	9600*1	9600*4	-	-
2	9600*2	9600*5	4800	2400
4	9600*3	9600*6	4800	2400
8	4800	4800	4800	2400
16	4800	4800	4800	2400
32	2400	2400	2400	2400
64	2400	2400	2400	2400

Note 1. SCI0.SMR.CKS[1:0] = 00b, SCI0.SEMR.BRME = 1, SCI0.BRR = 3Dh, SCI0.MDDR = CEh must be used for 9600 bps.
Note 2. SCI0.SMR.CKS[1:0] = 00b, SCI0.SEMR.BRME = 1, SCI0.BRR = 1Eh, SCI0.MDDR = CEh must be used for 9600 bps.
Note 3. SCI0.SMR.CKS[1:0] = 00b, SCI0.SEMR.BRME = 1, SCI0.BRR = 0Dh, SCI0.MDDR = BAh must be used for 9600 bps.
Note 4. SCI0.SMR.CKS[1:0] = 00b, SCI0.SEMR.BRME = 1, SCI0.BRR = 3Eh, SCI0.MDDR = 9Dh must be used for 9600 bps.
Note 5. SCI0.SMR.CKS[1:0] = 00b, SCI0.SEMR.BRME = 1, SCI0.BRR = 32h, SCI0.MDDR = FEh must be used for 9600 bps.
Note 6. SCI0.SMR.CKS[1:0] = 00b, SCI0.SEMR.BRME = 1, SCI0.BRR = 18h, SCI0.MDDR = F9h must be used for 9600 bps.

High-speed mode, Middle-speed mode, Low-speed mode

Table 10.10 HOCO: ± 2.0% (Ta = -40 to -20°C, 85 to 105°C) **(Unit: bps)**

Maximum division ratio of ICLK, PCLKB, and PCLKD	HOCO frequency			
	24 MHz	32 MHz	48 MHz	64 MHz
1	2400	2400	-	-
2	2400	2400	2400	1200
4	2400	2400	2400	1200
8	2400	2400	2400	1200
16	2400	2400	2400	1200
32	1200	1200	1200	1200
64	1200	1200	1200	1200

Figure 10.12 shows a setting example for using SCI0 or the DALI in Snooze mode entry.

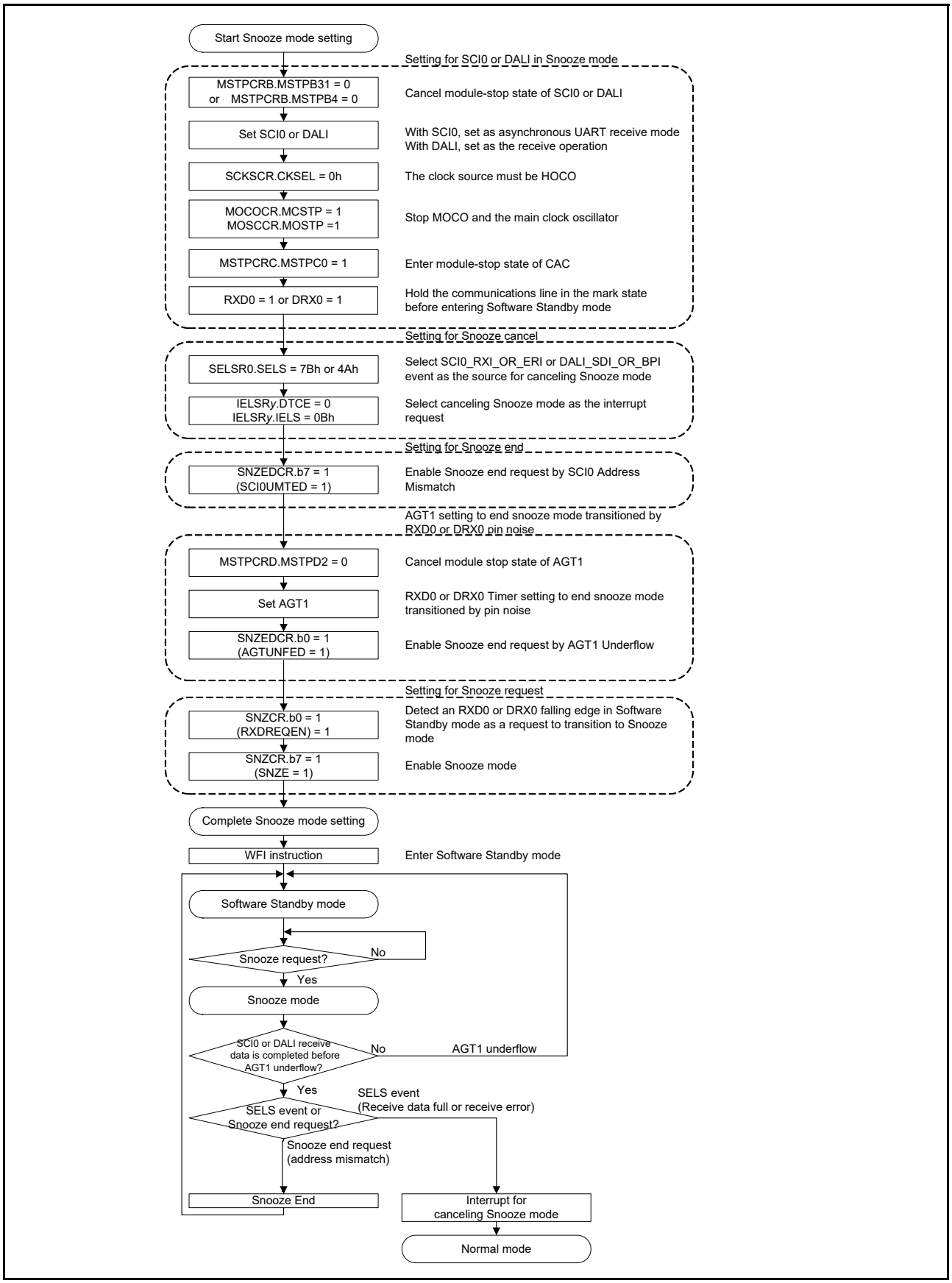


Figure 10.12 Setting example for using SCI0 or the DALI in Snooze mode entry

10.9 Usage Note

10.9.1 Register Access

(1) Do not write to registers listed in this section in any of the following conditions:

[Registers]

- All registers with a peripheral name of SYSTEM.

[Conditions]

- OPCCR.OPCMTSF = 1 or SOPCCR.SOPCMTSF = 1 (during transition of the operating power control mode)
- Time period from executing a WFI instruction to returning to Normal mode
- FENTRYR.FENTRY0 = 1 or FENTRYR.FENTRYD = 1 (flash P/E mode, data flash P/E mode)
- FLSTOP.FLSTPF = 1 (during transition).

(2) Valid setting of the clock related registers

Table 10.11 and Table 10.12 show the valid setting of the clock-related registers in each operating power control mode. Do not write any value other than the valid setting, otherwise it is ignored. Additionally, each register has some prohibited settings under certain conditions other than the operating power control modes. See section 8, Clock Generation Circuit for other conditions of each register.

Table 10.11 Valid setting of clock related registers (1)

Mode	Valid setting						
	SCKSCR.CKSEL[2:0] CKOCR.CKOSEL[2:0]	SCKDIVCR.ICK[2:0]	HOCOCR. HCSTP	MOCOCR. MCSTP	LOCOCR. LCSTP	MOSCCR. MOSTP	SOSCCR. SOSTP
High-speed Middle-speed Low-voltage Low-speed	000b (HOCO) 001b (MOCO) 010b (LOCO) 011b (MOSC) 100b (SOSC)	000b (1/1) 001b (1/2) 010b (1/4) 011b (1/8) 100b (1/16) 101b (1/32) 110b (1/64)	0 (operating) 1 (stop)	0 (operating) 1 (stop)	0 (operating) 1 (stop)	0 (operating) 1 (stop)	0 (operating) 1 (stop)
Subosc-speed	010b (LOCO) 100b (SOSC)	000b (1/1)	1 (stop)	1 (stop)	0 (operating) 1 (stop)	1 (stop)	0 (operating) 1 (stop)

Table 10.12 Valid setting for clock-related registers (2)

Operating oscillator	Valid setting	
	SOPCCR.SOPCM	OPCCR.OPCM[1:0]
High-speed on-chip oscillator	0	00b, 01b, 10b, 11b
Middle-speed on-chip oscillator		
Main clock oscillator		
Low-speed on-chip oscillator	0, 1	00b, 01b, 10b, 11b
Sub-clock oscillator		
IWDT-dedicated on-chip oscillator		

(3) Do not write to registers listed in this section for the following condition:

[Registers]

- SCKSCR, OPCCR.

[Condition]

- SOPCCR.SOPCM = 1 (Subosc-speed mode).

(4) Do not write to registers listed in this section by DTC:

[Registers]

- MSTPCRA.

(5) Do not write to registers listed in this section in Snooze mode. They must be set before entering Software Standby mode:

[Registers]

- SNZCR, SNZEDCR, SNZREQCR.

(6) Do not set the FLSTOP.FLSTOP bit to 1 in any of the following conditions:

[Conditions]

- SOPCCR.SOPCM = 0, OPCCR.OPCM[1:0] = 00b (High-speed mode)
- SOPCCR.SOPCM = 0, OPCCR.OPCM[1:0] = 01b (Middle-speed mode)
- SOPCCR.SOPCM = 0, OPCCR.OPCM[1:0] = 11b (Low-speed mode)
- SOPCCR.SOPCM = 1 (Subosc-speed mode).

(7) Write access to registers listed in this section is invalid when PRCR.PRC1 bit is 0:

[Registers]

- SBYCR, SNZCR, SNZEDCR, SNZREQCR, FLSTOP, OPCCR, SOPCCR.

10.9.2 I/O Port States

The I/O port states in Software Standby mode and Snooze mode, unless modifying in Snooze mode, are the same before entering the modes. Therefore, the supply current is not reduced while the output signals are held high.

10.9.3 Module-Stop State of DTC

Before writing 1 to MSTPCRA.MSTPA22, clear the DTCST.DTCST bit of the DTC to 0. For details, see section 15, Data Transfer Controller (DTC).

10.9.4 Internal Interrupt Sources

Interrupts do not operate in the module-stop state. If setting the module-stop bit while an interrupt request is generated, a CPU interrupt source or a DTC startup source cannot be cleared. For this reason, make sure you disable the corresponding interrupts before setting the module-stop bits.

10.9.5 Transition to Low Power Modes

Because the MCU does not support wakeup by event, do not enter low power modes (Sleep mode or Software Standby mode) by executing a WFE instruction. Also, do not set the SLEEPDEEP bit of the System Control Register in the Cortex®-M0+ core because the MCU does not support low power modes by SLEEPDEEP.

10.9.6 Timing of WFI Instruction

It is possible for the WFI instruction to be executed before I/O register writes are complete, in which case the operation might not proceed as intended. This can happen if the WFI is placed immediately after a write to an I/O register. To avoid this problem, it is recommended that you read back the register that was written to confirm that the write completed.

10.9.7 Writing WDT/IWDT Registers by DTC in Sleep Mode or Snooze Mode

Do not write registers in WDT or IWDT by DTC while WDT or IWDT stops by entering Sleep mode or Snooze mode.

10.9.8 Oscillators in Snooze Mode

Oscillators that stop by entering Software Standby mode automatically restart when a trigger to switch to Snooze mode is generated. The MCU does not enter Snooze mode until all the oscillators stabilize. If in Snooze mode, make sure to disable oscillators that are not required in Snooze mode before entering Software Standby mode, otherwise it takes longer to transition from Software Standby mode to Snooze mode.

10.9.9 Snooze Mode Entry by RXD0 or DRX0 Falling Edge

When the SNZCR.RXDREQEN bit is 1, noise on the RXD0 or DRX0 pin might cause the MCU to transfer from Software Standby mode to Snooze mode. Any subsequent RXD0 or DRX0 data can be received in Snooze mode by a noise on the RXD0 or DRX0 pin. If the MCU does not receive RXD0 or DRX0 data after the noise, an interrupt such as SCI0_ERI, SCI0_RXI, DALI_SDI, or DALI_BPI, or an address mismatch event is not generated, and the MCU stays in Snooze mode. To avoid this, an AGT1 underflow interrupt must be used to return to Software Standby mode or Normal mode when using SCI0 or the DALI in Snooze mode. However, do not use the AGT1 underflow as a source to return to Software Standby mode during an SCI or DALI communication. This causes SCI0 or the DALI to stop the operation in a half-finished state.

10.9.10 Using SCI0 or the DALI in Snooze Mode

When using SCI0 or the DALI in Snooze mode, a wakeup request other than an AGT1 underflow must not be used.

When using SCI0 or the DALI in Snooze mode, the following conditions must be satisfied:

- The clock source must be HOCO
- MOCO and the main clock oscillator must stop before entering Software Standby mode
- The RXD0 or DRX0 pin must be kept high before entering Software Standby mode
- A transition to Software Standby mode must not occur during an SCI or DALI communication
- The MSTPCRC.MSTPC0 bit must be 1 before entering Software Standby mode.

10.9.11 Conditions of A/D Conversion Start in Snooze Mode

The A/D converter can only be triggered by the ELC in Snooze mode. Software trigger or ADTRG0 pin must not be used.

10.9.12 Conditions of CTSU in Snooze Mode

The CTSU can only be started by the ELC in Snooze mode.

10.9.13 ELC Event in Snooze Mode

The ELC events available in Snooze mode are listed in this section. Do not use any other events. If starting peripheral modules for the first time after entering Snooze mode, the Event Link Setting Register (ELSRn) must set a Snooze mode entry event (SYSTEM_SNZREQ) as the trigger.

- Snooze mode entry (SYSTEM_SNZREQ)
- DTC transfer end (DTC_DTCEND)
- ADC140 window A/B compare match (ADC140_WCMPM)
- ADC140 window A/B compare mismatch (ADC140_WCMPUM)
- Data operation circuit interrupt (DOC_DOPCI).

10.9.14 Module-Stop Function for ADC140

When entering the Software Standby mode, it is recommended that you set the ADC140 module-stop state to reduce power consumption. In this case, the ADC140 can be available in Snooze mode by releasing the ADC140 module-stop using the DTC. Similarly, set the module-stop state using the DTC before returning to Software Standby mode from Snooze mode.

10.9.15 Module-Stop Function for an Unused Circuit

A circuit that is not used in user mode might not be reset, and might operate in an unstable state because the clocks are not supplied during an MCU reset. In this case, when the MCU transitions to Low speed mode or Software Standby mode, the supply current can be increased to a value greater than that stated in this User's Manual by up to 600 µA. Initialize the unused circuit as shown in Figure 10.13.

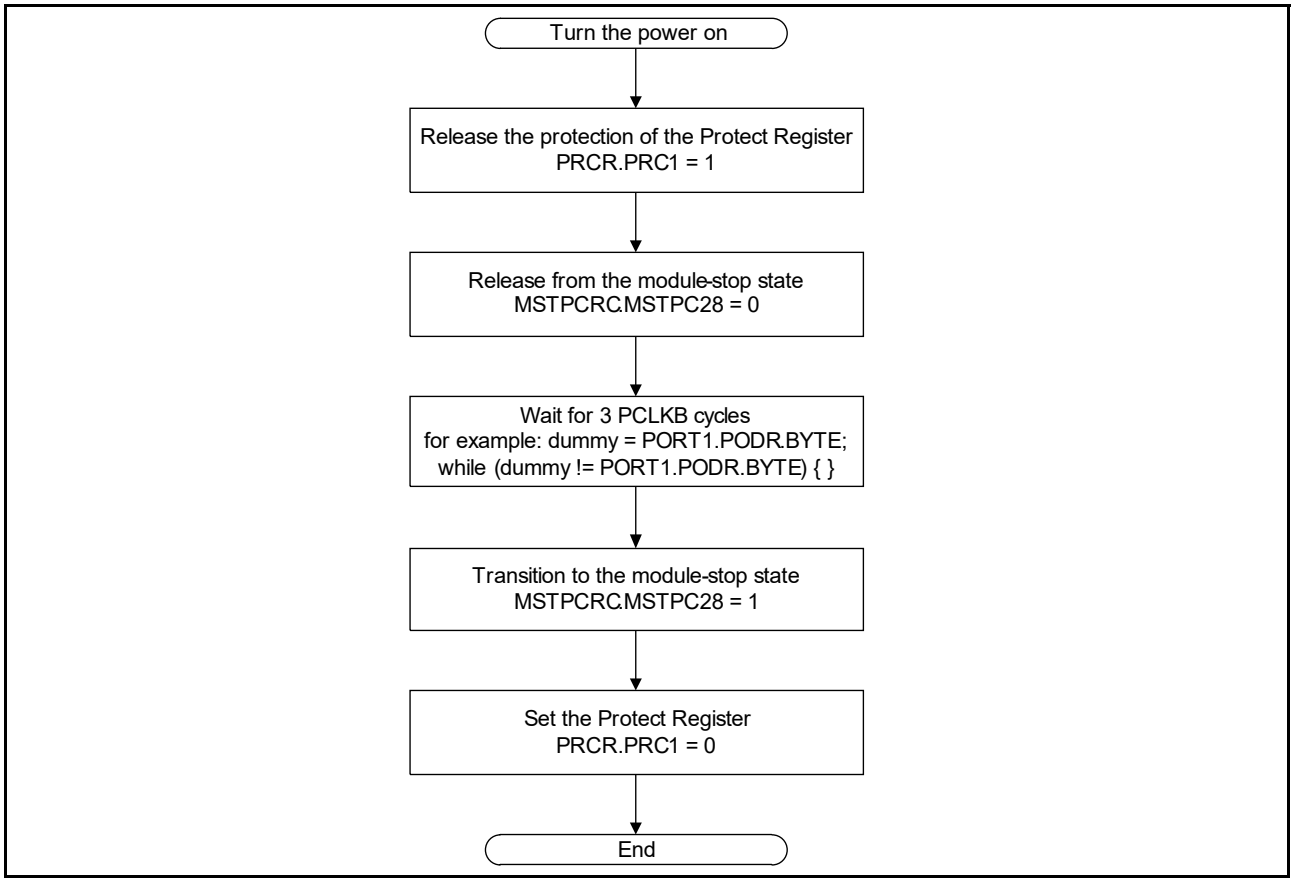


Figure 10.13 Example of initial setting flow for an unused circuit

11. Register Write Protection

11.1 Overview

The Register Write Protection function protects important registers from being overwritten because of software errors. The registers to be protected are set with the Protect Register (PRCR).

Table 11.1 lists the association between the PRCR bits and the registers to be protected.

Table 11.1 Association between PRCR bits and registers to be protected

PRCR bit	Register to be protected
PRC0	• Registers related to the Clock Generation Circuit: SCKDIVCR, SCKSCR, MOSCCR, HOCOCR, MOCOCR, CKOCR, OSTDCR, OSTDSR, MOCOUTCR, HOCOUTCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR, HOCOWTCR.
PRC1	• Registers related to the low power modes: SBYCR, SNZCR, SNZEDCR, SNZREQCR, FLSTOP, OPCCR, SOPCCR, SYOCDCR.
PRC3	• Registers related to the LVD: LVD1CR1, LVD1SR, LVD2CR1, LVD2SR, LVCMPCR, LVDLVLR, LVD1CR0, LVD2CR0.

11.2 Register Descriptions

11.2.1 Protect Register (PRCR)

Address(es): SYSTEM.PRCR 4001 E3FEh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PRKEY[7:0]								—	—	—	—	PRC3	—	PRC1	PRC0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Function	R/W
b0	PRC0	Protect Bit 0	Enables writing to the registers related to the clock generation circuit: 0: Disable writes 1: Enable writes.	R/W
b1	PRC1	Protect Bit 1	Enables writing to the registers related to the low power modes: 0: Disable writes 1: Enable writes.	R/W
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b3	PRC3	Protect Bit 3	Enables writing to the registers related to the LVD: 0: Disable writes 1: Enable writes.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	PRKEY[7:0]	PRC Key Code	These bits control the write access to the PRCR register. To modify the PRCR register, write A5h to the 8 higher-order bits and the desired value to the 8 lower-order bits as a 16-bit unit.	W*1

Note 1. Write data is not saved. Always reads 00h.

PRCi bits (Protect Bit i) (i = 0, 1, 3)

The PRCi bits enable or disable writing to the protected registers as described in Table 11.1. Setting the PRCi bits to 1 enables writing, and setting them to 0 disables writing.

12. Interrupt Controller Unit (ICU)

12.1 Overview

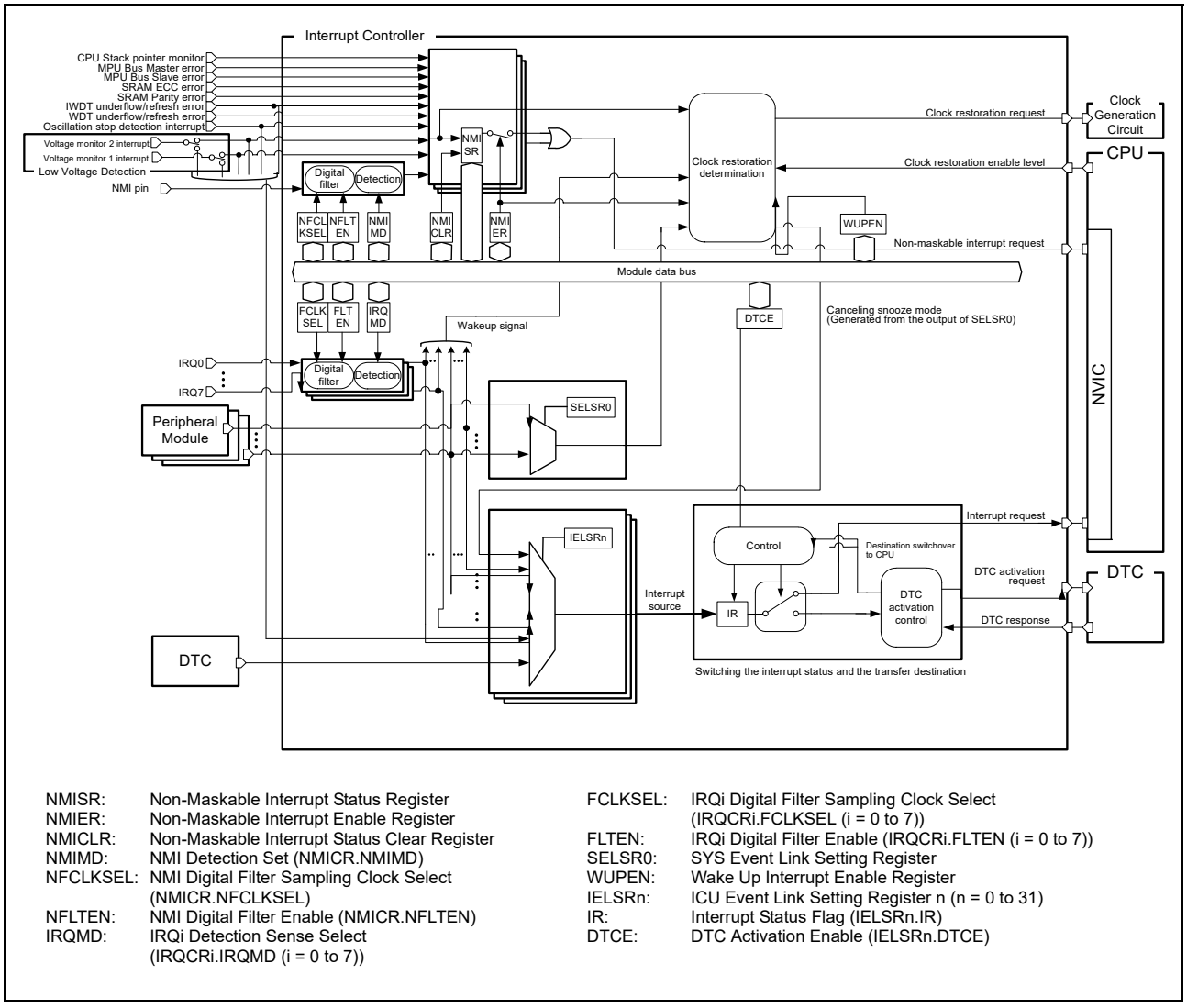
The Interrupt Controller Unit (ICU) controls which event signals are linked to the NVIC/DTC module. The ICU also controls non-maskable interrupts.

Table 12.1 lists the ICU specifications, Figure 12.1 shows a block diagram of the ICU, and Table 12.2 lists the I/O pins.

Table 12.1 ICU specifications

Parameter		Description
Interrupts	Peripheral function interrupts	• Interrupts from peripheral modules Number of sources: 137 (select factor within event list numbers 9 to 146)
	External pin interrupts	• Interrupt detection on low level[*4], falling edge, rising edge, rising and falling edges. One of these detection methods can be set for each source. • Digital filter function supported • 8 sources, with interrupts from IRQ0 to IRQ7 pins.
	DTC control	The DTC is activated by interrupt sources[*1]
	Interrupt sources for NVIC	• 32 sources
Non-maskable interrupts[*2]	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection on falling edge or rising edge • Digital filter function supported.
	Oscillation stop detection interrupt[*3]	Interrupt on detecting that the main oscillation has stopped
	WDT underflow/refresh error[*3]	Interrupt on an underflow of the down-counter or occurrence of a refresh error
	IWDT underflow/refresh error[*3]	Interrupt on an underflow of the down-counter or occurrence of a refresh error
	Voltage monitor 1 interrupt[*3]	Voltage monitor interrupt of low voltage detector 1 (LVD_LVD1)
	Voltage monitor 2 interrupt[*3]	Voltage monitor interrupt of low voltage detector 2 (LVD_LVD2)
	RPEST	Interrupt on SRAM parity error
	RECCST	Interrupt on SRAM ECC error
	BUSSST	Interrupt on MPU bus slave error
	BUSMST	Interrupt on MPU bus master error
	SPEST	Interrupt on CPU stack pointer monitor
Return from low power mode		• Sleep mode: return is initiated by non-maskable interrupts or any other interrupt source • Software Standby mode: return is initiated by non-maskable interrupts. Interrupt is selected in the WUPEN register • Snooze mode: return is initiated by non-maskable interrupts. Interrupt is selected in the SELSR0 and WUPEN registers. See section 12.2.7, SYS Event Link Setting Register (SELSR0) and section 12.2.8, Wake Up Interrupt Enable Register (WUPEN).

Note 1. For the DTC activation sources, see Table 12.4, Event table.
Note 2. Non-maskable interrupts can be enabled only once after a reset release.
Note 3. These non-maskable interrupts can also be used as event signals. When used as interrupts, do not change the value of the NMIER register from the reset state. To enable voltage monitor 1 and voltage monitor 2 interrupts, set the LVD1CR1.IRQSEL and LVD2CR1.IRQSEL bits to 1.
Note 4. Low level: Interrupt detection is not canceled if you do not clear it after a detection.



NMISR: Non-Maskable Interrupt Status Register
NMIER: Non-Maskable Interrupt Enable Register
NMICLR: Non-Maskable Interrupt Status Clear Register
NMIMD: NMI Detection Set (NMICR.NMIMD)
NFCLKSEL: NMI Digital Filter Sampling Clock Select (NMICR.NFCLKSEL)
NFLTEN: NMI Digital Filter Enable (NMICR.NFLTEN)
IRQMD: IRQi Detection Sense Select (IRQCRi.IRQMD (i = 0 to 7))
FCLKSEL: IRQi Digital Filter Sampling Clock Select (IRQCRi.FCLKSEL (i = 0 to 7))
FLTEN: IRQi Digital Filter Enable (IRQCRi.FLTEN (i = 0 to 7))
SELSR0: SYS Event Link Setting Register
WUPEN: Wake Up Interrupt Enable Register
IELSRn: ICU Event Link Setting Register n (n = 0 to 31)
IR: Interrupt Status Flag (IELSRn.IR)
DTCE: DTC Activation Enable (IELSRn.DTCE)

Figure 12.1 ICU block diagram

Table 12.2 ICU configuration pins

Pin name	I/O	Description
NMI	Input	Non-maskable interrupt request pin
IRQ0 to IRQ7	Input	External interrupt request pins

12.2 Register Descriptions

This chapter does not describe the Arm® NVIC internal registers. For information about these registers, see the *ARM® Cortex®-M0+ Processor Technical Reference Manual (ARM DDI 0484C).*

12.2.1 IRQ Control Register i (IRQCRi) (i = 0 to 7)

Address(es): ICU.IRQCR0 4000 6000h, ICU.IRQCR1 4000 6001h, ICU.IRQCR2 4000 6002h, ICU.IRQCR3 4000 6003h, ICU.IRQCR4 4000 6004h, ICU.IRQCR5 4000 6005h, ICU.IRQCR6 4000 6006h, ICU.IRQCR7 4000 6007h

	b7	b6	b5	b4	b3	b2	b1	b0
	FLTEN	—	FCLKSEL[1:0]		—	—	IRQMD[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	IRQMD[1:0]	IRQi Detection Sense Select	b1 b0 0 0: Falling edge 0 1: Rising edge 1 0: Rising and falling edges 1 1: Low level.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5, b4	FCLKSEL[1:0]	IRQi Digital Filter Sampling Clock Select	b5 b4 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64.	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	FLTEN	IRQi Digital Filter Enable	0: Disable digital filter 1: Enable digital filter.	R/W

IRQCRi register changes must satisfy the following:

1. For a CPU interrupt or DTC trigger:
   Change the IRQCRi register setting before setting the target IELSRn (n = 0 to 31).
   You can change the register values only when the IELSRn.IELS[8:0] bits are 000h.
2. For a wakeup enable signal:
   Change the IRQCRi register setting before setting the target WUPEN.IRQWUPENi (i = 0 to 7).
   You change the register values only when the target WUPEN.IRQWUPENi is 0.

IRQMD[1:0] bits (IRQi Detection Sense Select)

The IRQMD[1:0] bits set the detection sensing method for the external pin interrupt sources IRQi. For setting method when using external pin interrupt, see section 12.4.4, External Pin Interrupts.

FCLKSEL[1:0] bits (IRQi Digital Filter Sampling Clock Select)

The FCLKSEL[1:0] bits select the digital filter sampling clock for the external pin interrupt request pins IRQi, selectable to:

- PCLKB (every cycle)
- PCLKB/8 (once every 8 cycles)
- PCLKB/32 (once every 32 cycles)
- PCLKB/64 (once every 64 cycles.

For details on the digital filter, see section 12.4.3, Digital Filter.

FLTEN bit (IRQi Digital Filter Enable)

The FLTEN bits enable the digital filter used for the external pin interrupt sources IRQi. The digital filter is enabled when the IRQCRi.FLTEN bit is 1 and disabled when the IRQCRi.FLTEN bit is 0. The IRQi pin level is sampled at the clock cycle specified with the IRQCRi.FCLKSEL[1:0] bits. When the sampled level matches three times, the output level from the digital filter changes. For details on the digital filter, see section 12.4.3, Digital Filter.

12.2.2 Non-Maskable Interrupt Status Register (NMISR)

Address(es): ICU.NMISR 4000 6140h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SPEST	BUSMST	BUSSST	RECCST	RPEST	NMIST	OSTST	—	—	LVD2ST	LVD1ST	WDTST	IWDTST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	IWDTST	IWDT Underflow/Refresh Error Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b1	WDTST	WDT Underflow/Refresh Error Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b2	LVD1ST	Voltage Monitor 1 Interrupt Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b3	LVD2ST	Voltage Monitor 2 Interrupt Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b5, b4	—	Reserved	These bits are read as 0.	R
b6	OSTST	Main Clock Oscillation Stop Detection Interrupt Status Flag	0: Interrupt not requested for main clock oscillation stop 1: Interrupt requested for main clock oscillation stop.	R
b7	NMIST	NMI Pin Interrupt Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b8	RPEST	SRAM Parity Error Interrupt Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b9	RECCST	SRAM ECC Error Interrupt Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b10	BUSSST	MPU Bus Slave Error Interrupt Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b11	BUSMST	MPU Bus Master Error Interrupt Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b12	SPEST	CPU Stack Pointer Monitor Interrupt Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b15 to b13	—	Reserved	These bits are read as 0.	R

The NMISR register monitors the status of non-maskable interrupt sources. Writes to the NMISR register are ignored. The setting in the Non-Maskable Interrupt Enable Register (NMIER) does not affect the status flags in this register. Before the end of the non-maskable interrupt handler, check that all of the bits in this register are set to 0 to confirm that no other NMI requests are generated during handler processing.

IWDTST flag (IWDT Underflow/Refresh Error Status Flag)

The IWDTST flag indicates the IWDT underflow/refresh error interrupt request. It is read-only and is cleared by the NMICLR.IWDTCLR bit.

[Setting condition]

When the IWDT underflow/refresh error interrupt is generated and this interrupt source is enabled.

[Clearing condition]

When 1 is written to the NMICLR.IWDTCLR bit.

WDTST flag (WDT Underflow/Refresh Error Status Flag)

The WDTST flag indicates the WDT underflow/refresh error interrupt request. It is read-only and is cleared by the NMICLR.WDTCLR bit.

[Setting condition]

When the WDT underflow/refresh error interrupt is generated.

[Clearing condition]

When 1 is written to the NMICLR.WDTCLR bit.

LVD1ST flag (Voltage Monitor 1 Interrupt Status Flag)

The LVD1ST flag indicates the request for voltage monitor 1 interrupt. It is read-only and is cleared by the NMICLR.LVD1CLR bit.

[Setting condition]

When the voltage monitor 1 interrupt is generated while this interrupt is enabled at its source.

[Clearing condition]

When 1 is written to the NMICLR.LVD1CLR bit.

LVD2ST flag (Voltage Monitor 2 Interrupt Status Flag)

The LVD2ST flag indicates the request for voltage monitor 2 interrupt. It is read-only and is cleared by the NMICLR.LVD2CLR bit.

[Setting condition]

When the voltage monitor 2 interrupt is generated and this interrupt source is enabled.

[Clearing condition]

When 1 is written to the NMICLR.LVD2CLR bit.

OSTST flag (Main Clock Oscillation Stop Detection Interrupt Status Flag)

The OSTST flag indicates the main clock oscillation stop detection interrupt request. It is read-only and is cleared by the NMICLR.OSTCLR bit.

[Setting condition]

When the main clock oscillation stop detection interrupt is generated.

[Clearing condition]

When 1 is written to the NMICLR.OSTCLR bit.

NMIST flag (NMI Pin Interrupt Status Flag)

The NMIST flag indicates the NMI pin interrupt request. It is read-only and is cleared by the NMICLR.NMICLR bit.

[Setting condition]

When an edge specified by the NMICR.NMIMD bit is input to the NMI pin.

[Clearing condition]

When 1 is written to the NMICLR.NMICLR bit.

RPEST flag (SRAM Parity Error Interrupt Status Flag)

The RPEST flag indicates the SRAM parity error interrupt request.

[Setting condition]

When an interrupt is generated in response to an SRAM parity error.

[Clearing condition]

When 1 is written to the NMICLR.RPECLR bit.

RECCST flag (SRAM ECC Error Interrupt Status Flag)

The RECCST flag indicates the SRAM ECC error interrupt request.

[Setting condition]

When an interrupt is generated in response to an SRAM ECC error.

[Clearing condition]

When 1 is written to the NMICLR.RECCCLR bit.

BUSSST flag (MPU Bus Slave Error Interrupt Status Flag)

The BUSSST flag indicates the bus slave error interrupt request.

[Setting condition]

When an interrupt is generated in response to a bus slave error.

[Clearing condition]

When 1 is written to the NMICLR.BUSSCLR bit.

BUSMST flag (MPU Bus Master Error Interrupt Status Flag)

The BUSMST flag indicates the bus master error interrupt request.

[Setting condition]

When an interrupt is generated in response to a bus master error.

[Clearing condition]

When 1 is written to the NMICLR.BUSMCLR bit.

SPEST flag (CPU Stack Pointer Monitor Interrupt Status Flag)

The SPEST flag indicates the CPU stack pointer monitor interrupt request.

[Setting condition]

When an interrupt is generated in response to a CPU stack pointer monitor error.

[Clearing condition]

When 1 is written to the NMICLR.SPECLR bit.

12.2.3 Non-Maskable Interrupt Enable Register (NMIER)

Address(es): ICU.NMIER 4000 6120h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SPEEN	BUSMEN	BUSSEN	RECCEN	RPEEN	NMIEN	OSTEN	—	—	LVD2EN	LVD1EN	WDTEN	IWDTEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	IWDTEN	IWDT Underflow/Refresh Error Interrupt Enable	0: Disable 1: Enable.	R/(W) *1, *2
b1	WDTEN	WDT Underflow/Refresh Error Interrupt Enable	0: Disable 1: Enable.	R/(W) *1, *2
b2	LVD1EN	Voltage Monitor 1 Interrupt Enable	0: Disable 1: Enable.	R/(W) *1, *2
b3	LVD2EN	Voltage Monitor 2 Interrupt Enable	0: Disable 1: Enable.	R/(W) *1, *2
b5, b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	OSTEN	Main clock Oscillation Stop Detection Interrupt Enable	0: Disable 1: Enable.	R/(W) *1, *2

Bit	Symbol	Bit name	Description	R/W
b7	NMIEN	NMI Pin Interrupt Enable	0: Disable 1: Enable.	R/(W) *1
b8	RPEEN	SRAM Parity Error Interrupt Enable	0: Disable 1: Enable.	R/(W) *1
b9	RECCEN	SRAM ECC Error Interrupt Enable	0: Disable 1: Enable.	R/(W) *1
b10	BUSSEN	MPU Bus Slave Error Interrupt Enable	0: Disable 1: Enable.	R/(W) *1
b11	BUSMEN	MPU Bus Master Error Interrupt Enable	0: Disable 1: Enable.	R/(W) *1
b12	SPEEN	CPU Stack Pointer Monitor Interrupt Enable	0: Disable 1: Enable.	R/(W) *1
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. You can write 1 to this bit only once after reset. Subsequent write accesses are invalid. Writing 0 to this bit is invalid.
Note 2. Do not write 1 to this bit when the source is used as an event signal.

IWDTEN bit (IWDT Underflow/Refresh Error Interrupt Enable)

The IWDTEN bit enables the IWDT underflow/refresh error interrupt as an NMI trigger.

WDTEN bit (WDT Underflow/Refresh Error Interrupt Enable)

The WDTEN bit enables the WDT underflow/refresh error interrupt as an NMI trigger.

LVD1EN bit (Voltage Monitor 1 Interrupt Enable)

The LVD1EN bit enables the voltage monitor 1 interrupt as an NMI trigger.

LVD2EN bit (Voltage Monitor 2 Interrupt Enable)

The LVD2EN bit enables the voltage monitor 2 interrupt as an NMI trigger.

OSTEN bit (Main clock Oscillation Stop Detection Interrupt Enable)

The OSTEN bit enables the main clock oscillation stop detection interrupt as an NMI trigger.

NMIEN bit (NMI Pin Interrupt Enable)

The NMIEN bit enables the NMI pin interrupt as an NMI trigger.

RPEEN bit (SRAM Parity Error Interrupt Enable)

The RPEEN bit enables the SRAM parity error interrupt as an NMI trigger.

RECCEN bit (SRAM ECC Error Interrupt Enable)

The RECCEN bit enables the SRAM ECC error interrupt as an NMI trigger.

BUSSEN bit (MPU Bus Slave Error Interrupt Enable)

The BUSSEN bit enables the Bus Slave error interrupt as an NMI trigger.

BUSMEN bit (MPU Bus Master Error Interrupt Enable)

The BUSMEN bit enables the Bus Master error interrupt as an NMI trigger.

SPEEN bit (CPU Stack Pointer Monitor Interrupt Enable)

The SPEEN bit enables the CPU Stack pointer monitor interrupt as an NMI trigger.

12.2.4 Non-Maskable Interrupt Status Clear Register (NMICLR)

Address(es): ICU.NMICLR 4000 6130h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SPECLR	BUSMCLR	BUSSCLR	RECCCLR	RPECLR	NMICLR	OSTCLR	—	—	LVD2CLR	LVD1CLR	WDTCLR	IWDTCLR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	IWDTCLR	IWDT Clear	0: No effect 1: Clear the NMISR.IWDTST flag.	R/(W)*1
b1	WDTCLR	WDT Clear	0: No effect 1: Clear the NMISR.WDTST flag.	R/(W)*1
b2	LVD1CLR	LVD1 Clear	0: No effect 1: Clear the NMISR.LVD1ST flag.	R/(W)*1
b3	LVD2CLR	LVD2 Clear	0: No effect 1: Clear the NMISR.LVD2ST flag.	R/(W)*1
b5, b4	—	Reserved	The write value should be 0.	R/(W)*1
b6	OSTCLR	OST Clear	0: No effect 1: Clear the NMISR.OSTST flag.	R/(W)*1
b7	NMICLR	NMI Clear	0: No effect 1: Clear the NMISR.NMIST flag.	R/(W)*1
b8	RPECLR	SRAM Parity Error Clear	0: No effect 1: Clear the NMISR.RPEST flag.	R/(W)*1
b9	RECCCLR	SRAM ECC Error Clear	0: No effect 1: Clear the NMISR.RECCST flag.	R/(W)*1
b10	BUSSCLR	Bus Slave Error Clear	0: No effect 1: Clear the NMISR.BUSSST flag.	R/(W)*1
b11	BUSMCLR	Bus Master Error Clear	0: No effect 1: Clear the NMISR.BUSMST flag.	R/(W)*1
b12	SPECLR	CPU Stack Pointer Monitor Interrupt Clear	0: No effect. 1: Clear the NMISR.SPEST flag.	R/(W)*1
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only write 1 to this bit.

IWDTCLR bit (IWDT Clear)

Writing 1 clears the NMISR.IWDTST flag. This bit is read as 0.

WDTCLR bit (WDT Clear)

Writing 1 clears the NMISR.WDTST flag. This bit is read as 0.

LVD1CLR bit (LVD1 Clear)

Writing 1 clears the NMISR.LVD1ST flag. This bit is read as 0.

LVD2CLR bit (LVD2 Clear)

Writing 1 clears the NMISR.LVD2ST flag. This bit is read as 0.

OSTCLR bit (OST Clear)

Writing 1 clears the NMISR.OSTST flag. This bit is read as 0.

NMICLR bit (NMI Clear)

Writing 1 clears the NMISR.NMIST flag. This bit is read as 0.

RPECLR bit (SRAM Parity Error Clear)

Writing 1 clears the NMISR.RPEST flag. This bit is read as 0.

RECCCLR bit (SRAM ECC Error Clear)

Writing 1 clears the NMISR.RECCST flag. This bit is read as 0.

BUSSCLR bit (Bus Slave Error Clear)

Writing 1 clears the NMISR.BUSSST flag. This bit is read as 0.

BUSMCLR bit (Bus Master Error Clear)

Writing 1 clears the NMISR.BUSMST flag. This bit is read as 0.

SPECLR bit (CPU Stack Pointer Monitor Interrupt Clear)

Writing 1 clears the NMISR.SPEST flag. This bit is read as 0.

12.2.5 NMI Pin Interrupt Control Register (NMICR)

Address(es): ICU.NMICR 4000 6100h

	b7	b6	b5	b4	b3	b2	b1	b0
	NFLTEN	—	NFCLKSEL[1:0]		—	—	—	NMIMD
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	NMIMD	NMI Detection Set	0: Falling edge 1: Rising edge.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5, b4	NFCLKSEL[1:0]	NMI Digital Filter Sampling Clock Select	b5 b4 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64.	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	NFLTEN	NMI Digital Filter Enable	0: Disabled 1: Enabled.	R/W

Change the NMICR register settings before enabling NMI pin interrupts, that is, before setting NMIER.NMIEN to 1.

NMIMD bit (NMI Detection Set)

The NMIMD bit selects the detection sensing method for NMI pin interrupts.

NFCLKSEL[1:0] bits (NMI Digital Filter Sampling Clock Select)

The NFCLKSEL[1:0] bits select the digital filter sampling clock for NMI pin interrupts, selectable to:

- PCLKB (every cycle)
- PCLKB/8 (once every 8 cycles)
- PCLKB/32 (once every 32 cycles)
- PCLKB/64 (once every 64 cycles).

For details on the digital filter, see section 12.4.3, Digital Filter.

NFLTEN bit (NMI Digital Filter Enable)

The NFLTEN bit enables the digital filter used for the NMI pin interrupt. The filter is enabled when NFLTEN is 1, and disabled when NFLTEN is 0. The NMI pin level is sampled at the clock cycle specified in NMICR.NFCLKSEL[1:0]. When the sampled level matches three times, the output level from the digital filter changes. For details on the digital filter, see section 12.4.3, Digital Filter.

12.2.6 ICU Event Link Setting Register n (IELSRn)

Address(es): ICU.IELSR0 4000 6300h, ICU.IELSR1 4000 6304h, ICU.IELSR2 4000 6308h, ICU.IELSR3 4000 630Ch……
……ICU.IELSR28 4000 6370h, ICU.IELSR29 4000 6374h, ICU.IELSR30 4000 6378h, ICU.IELSR31 4000 637Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	DTCE	—	—	—	—	—	—	—	IR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	IELS[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	IELS[7:0]	ICU Event Link Select	b7 b0 00000000: Disable interrupts to the associated NVIC or DTC module. 00000001 to 10010010: Event signal number to be linked. Other settings are prohibited. For details, see Table 12.4.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	IR	Interrupt Status Flag	0: No interrupt request generated 1: An interrupt request generated.	R/(W) *1
b23 to b17	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b24	DTCE	DTC Activation Enable	0: Disable DTC activation 1: Enable DTC activation.	R/W
b31 to b25	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This register requires halfword or word access.
Note 1. Writing 1 to the IR flag is prohibited.

The IELSRn register selects the IRQ source used by NVIC. For details, see Table 12.4. IELSRn, where n = 0 to 31, corresponds to the NVIC-IRQ input source numbers 0 to 31.

IELS[7:0] bits (ICU Event Link Select)

The IELS[7:0] bits link an event signal to the associated NVIC or DTC module.

IR flag (Interrupt Status Flag)

The IR status flag indicates an individual interrupt request from the event specified in IELS[7:0].

[Setting condition]

- When an interrupt request is received from the associated peripheral module or IRQi pin.

[Clearing conditions]

- When 0 is written to the IR flag. DTCE must be set to 0 before writing 0 to the IR flag.

To clear the IR flag:

1. Negate the input interrupt signal.
2. Read access the peripheral once and wait for 2 clock cycles of the target module clock PCLKB or PCLKD.

3. Clear the IR flag by writing 0.

DTCE bit (DTC Activation Enable)

When the DTCE bit is set to 1, the associated event is selected as the source for DTC activation.

[Setting condition]

When 1 is written to the DTCE bit.

[Clearing conditions]

- When the specified number of transfers is complete. For chain transfer, when the specified number of transfers for the last chain transfer is complete.
- When 0 is written to the DTCE bit.

12.2.7 SYS Event Link Setting Register (SELSR0)

Address(es): ICU.SELSR0 4000 6200h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	SELS[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	SELS[7:0]	SYS Event Link Select	b7 b0 00000000: Disable event output to the associated low-power mode module 00000001 to 10010010: Event signal number to be linked. Other settings are prohibited. For details, see Table 12.4.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. This register requires halfword access.

The SELSR0 register selects the events that wake up the CPU from Snooze mode. You can use only the events listed in Table 12.4 checked under "Canceling Snooze mode using SELSR0". When 0Bh is set in IELSRn.IELS[7:0] bits, an SELSR0 event interrupt occurs.

12.2.8 Wake Up Interrupt Enable Register (WUPEN)

Address(es): ICU.WUPEN 4000 61A0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IIC0WUPEN	AGT1CBWUPEN	AGT1CAWUPEN	AGT1UDWUPEN	USBFSWUPEN	—	RTCPRDWUPEN	RTCALMWUPEN	ACMPLP0WUPEN	—	—	—	LVD2WUPEN	LVD1WUPEN	KEYWUPEN	IWDTWUPEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	IRQWUPEN[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	IRQWUPEN[7:0]	IRQ Interrupt Software Standby Returns Enable	0: Software Standby returns by IRQ interrupt disabled 1: Software Standby returns by IRQ interrupt enabled.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	IWDTWUPEN	IWDT Interrupt Software Standby Returns Enable	0: Software Standby returns by IWDT interrupt disabled 1: Software Standby returns by IWDT interrupt enabled.	R/W
b17	KEYWUPEN	Key Interrupt Software Standby Returns Enable	0: Software Standby returns by KEY interrupt disabled 1: Software Standby returns by KEY interrupt enabled.	R/W
b18	LVD1WUPEN	LVD1 Interrupt Software Standby Returns Enable	0: Software Standby returns by LVD1 interrupt disabled 1: Software Standby returns by LVD1 interrupt enabled.	R/W
b19	LVD2WUPEN	LVD2 Interrupt Software Standby Returns Enable	0: Software Standby returns by LVD2 interrupt disabled 1: Software Standby returns by LVD2 interrupt enabled.	R/W
b22 to b20	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b23	ACMPLP0WUPEN	ACMPLP0 Interrupt Software Standby Returns Enable	0: Software Standby returns by ACMPLP0 interrupt disabled 1: Software Standby returns by ACMPLP0 interrupt enabled.	R/W
b24	RTCALMWUPEN	RTC Alarm Interrupt Software Standby Returns Enable	0: Software Standby returns by RTC alarm interrupt disabled 1: Software Standby returns by RTC alarm interrupt enabled.	R/W
b25	RTCPRDWUPEN	RTC Period Interrupt Software Standby Returns Enable	0: Software Standby returns by RTC period interrupt disabled 1: Software Standby returns by RTC period interrupt enabled.	R/W
b26	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b27	USBFSWUPEN	USBFS Interrupt Software Standby Returns Enable	0: Software Standby returns by USBFS interrupt disabled 1: Software Standby returns by USBFS interrupt enabled.	R/W
b28	AGT1UDWUPEN	AGT1 Underflow Interrupt Software Standby Returns Enable	0: Software Standby returns by AGT1 underflow interrupt disabled 1: Software Standby returns by AGT1 underflow interrupt enabled.	R/W
b29	AGT1CAWUPEN	AGT1 Compare Match A Interrupt Software Standby Returns Enable	0: Software Standby returns by AGT1 compare match A interrupt disabled 1: Software Standby returns by AGT1 compare match A interrupt enabled.	R/W
b30	AGT1CBWUPEN	AGT1 Compare Match B Interrupt Software Standby Returns Enable	0: Software Standby returns by AGT1 compare match B interrupt disabled 1: Software Standby returns by AGT1 compare match B interrupt enabled.	R/W
b31	IIC0WUPEN	IIC0 Address Match Interrupt Software Standby Returns Enable	0: Software Standby returns by IIC0 address match interrupt disabled 1: Software Standby returns by IIC0 address match interrupt enabled.	R/W

The bits in this register control whether the associated interrupt can wake up the CPU from Software Standby mode.

IRQWUPEN[7:0] bits (IRQ Interrupt Software Standby Returns Enable)

The IRQWUPEN[7:0] bits enable the use of IRQn interrupts to cancel Software Standby mode.

IWDTWUPEN bit (IWDT Interrupt Software Standby Returns Enable)

The IWDTWUPEN bit enables the use of IWDT interrupts to cancel Software Standby mode.

KEYWUPEN bit (Key Interrupt Software Standby Returns Enable)

The KEYWUPEN bit enables the use of Key interrupts to cancel Software Standby mode.

LVD1WUPEN bit (LVD1 Interrupt Software Standby Returns Enable)

The LVD1WUPEN bit enables the use of LVD1 interrupts to cancel Software Standby mode.

LVD2WUPEN bit (LVD2 Interrupt Software Standby Returns Enable)

The LVD2WUPEN bit enables the use of LVD2 interrupts to cancel Software Standby mode.

ACMPLP0WUPEN bit (ACMPLP0 Interrupt Software Standby Returns Enable)

The ACMPLP0WUPEN bit enables the use of ACMPLP0 interrupts to cancel Software Standby mode.

RTCALMWUPEN bit (RTC Alarm Interrupt Software Standby Returns Enable)

The RTCALMWUPEN bit enables the use of RTC alarm interrupts to cancel Software Standby mode.

RTCPRDWUPEN bit (RTC Period Interrupt Software Standby Returns Enable)

The RTCPRDWUPEN bit enables the use of RTC period interrupts to cancel Software Standby mode.

USBFSWUPEN bit (USBFS Interrupt Software Standby Returns Enable)

The USBFSWUPEN bit enables the use of USBFS interrupts to cancel Software Standby mode.

AGT1UDWUPEN bit (AGT1 Underflow Interrupt Software Standby Returns Enable)

The AGT1UDWUPEN bit enables the use of the AGT1 underflow interrupts to cancel Software Standby mode.

AGT1CAWUPEN bit (AGT1 Compare Match A Interrupt Software Standby Returns Enable)

The AGT1CAWUPEN bit enables the use of AGT1 compare match A interrupts to cancel Software Standby mode.

AGT1CBWUPEN bit (AGT1 Compare Match B Interrupt Software Standby Returns Enable)

The AGT1CBWUPEN bit enables the use of AGT1 compare match B interrupts to cancel Software Standby mode.

IIC0WUPEN bit (IIC0 Address Match Interrupt Software Standby Returns Enable)

The IIC0WUPEN bit enables the use of IIC0 interrupts to cancel Software Standby mode.

12.3 Vector Table

The ICU detects two types of interrupts, maskable and non-maskable interrupts. Interrupt priorities are set up in the Arm NVIC. For information on these registers, see the NVIC chapter of the *ARM® Cortex®-M0+ Processor Technical Reference Manual (ARM DDI 0484C).*

12.3.1 Interrupt Vector Table

Table 12.3 describes the interrupt vector table. The interrupt vector addresses conform to the NVIC specifications.

Table 12.3 Interrupt vector table (1 of 2)

Exception number	IRQ number	Vector offset	Source	Description
0	—	000h	Arm	Initial stack pointer
1	—	004h	Arm	Initial program counter (reset vector)
2	—	008h	Arm	Non-Maskable Interrupt (NMI)
3	—	00Ch	Arm	Hard Fault
4	—	010h	Arm	Reserved
5	—	014h	Arm	Reserved
6	—	018h	Arm	Reserved
7	—	01Ch	Arm	Reserved
8	—	020h	Arm	Reserved
9	—	024h	Arm	Reserved

Table 12.3 Interrupt vector table (2 of 2)

Exception number	IRQ number	Vector offset	Source	Description
10	—	028h	Arm	Reserved
11	—	02Ch	Arm	Supervisor call (SVCall)
12	—	030h	Arm	Reserved
13	—	034h	Arm	Reserved
14	—	038h	Arm	Pendable request for system service (PendableSrvReq)
15	—	03Ch	Arm	System tick timer (SysTick)
16	0	040h	ICU.IELSR0	Event selected in the ICU.IELSR0 register
17	1	044h	ICU.IELSR1	Event selected in the ICU.IELSR1 register
18	2	048h	ICU.IELSR2	Event selected in the ICU.IELSR2 register
19	3	04Ch	ICU.IELSR3	Event selected in the ICU.IELSR3 register
20	4	050h	ICU.IELSR4	Event selected in the ICU.IELSR4 register
21	5	054h	ICU.IELSR5	Event selected in the ICU.IELSR5 register
22	6	058h	ICU.IELSR6	Event selected in the ICU.IELSR6 register
23	7	05Ch	ICU.IELSR7	Event selected in the ICU.IELSR7 register
24	8	060h	ICU.IELSR8	Event selected in the ICU.IELSR8 register
25	9	064h	ICU.IELSR9	Event selected in the ICU.IELSR9 register
26	10	068h	ICU.IELSR10	Event selected in the ICU.IELSR10 register
27	11	06Ch	ICU.IELSR11	Event selected in the ICU.IELSR11 register
28	12	070h	ICU.IELSR12	Event selected in the ICU.IELSR12 register
29	13	074h	ICU.IELSR13	Event selected in the ICU.IELSR13 register
30	14	078h	ICU.IELSR14	Event selected in the ICU.IELSR14 register
31	15	07Ch	ICU.IELSR15	Event selected in the ICU.IELSR15 register
32	16	080h	ICU.IELSR16	Event selected in the ICU.IELSR16 register
33	17	084h	ICU.IELSR17	Event selected in the ICU.IELSR17 register
34	18	088h	ICU.IELSR18	Event selected in the ICU.IELSR18 register
35	19	08Ch	ICU.IELSR19	Event selected in the ICU.IELSR19 register
36	20	090h	ICU.IELSR20	Event selected in the ICU.IELSR20 register
37	21	094h	ICU.IELSR21	Event selected in the ICU.IELSR21 register
38	22	098h	ICU.IELSR22	Event selected in the ICU.IELSR22 register
39	23	09Ch	ICU.IELSR23	Event selected in the ICU.IELSR23 register
40	24	0A0h	ICU.IELSR24	Event selected in the ICU.IELSR24 register
41	25	0A4h	ICU.IELSR25	Event selected in the ICU.IELSR25 register
42	26	0A8h	ICU.IELSR26	Event selected in the ICU.IELSR26 register
43	27	0ACh	ICU.IELSR27	Event selected in the ICU.IELSR27 register
44	28	0B0h	ICU.IELSR28	Event selected in the ICU.IELSR28 register
45	29	0B4h	ICU.IELSR29	Event selected in the ICU.IELSR29 register
46	30	0B8h	ICU.IELSR30	Event selected in the ICU.IELSR30 register
47	31	0BCh	ICU.IELSR31	Event selected in the ICU.IELSR31 register

12.3.2 Event Number

The following table lists heading details for Table 12.4, which describes each event number.

Parameter	Description
Interrupt request source	Name of the source generating the interrupt request
Name	Name of the interrupt
Connect to NVIC	"✓" indicates the interrupt can be used as a CPU interrupt
Invoke DTC	"✓" indicates the interrupt can be used to request DTC activation
Canceling Snooze mode	"✓" indicates the interrupt can be used to request a return from Snooze mode
Canceling Software Standby mode	"✓" indicates the interrupt can be used to request a return from Software Standby mode

Table 12.4 Event table (1 of 4)

Event number	Interrupt request source	Name	IELSRn		Canceling Snooze	Canceling Software Standby
			Connect to NVIC	Invoke DTC		
01h	Port	PORT_IRQ0	✓	✓	✓	✓
02h		PORT_IRQ1	✓	✓	✓	✓
03h		PORT_IRQ2	✓	✓	✓	✓
04h		PORT_IRQ3	✓	✓	✓	✓
05h		PORT_IRQ4	✓	✓	✓	✓
06h		PORT_IRQ5	✓	✓	✓	✓
07h		PORT_IRQ6	✓	✓	✓	✓
08h		PORT_IRQ7	✓	✓	✓	✓
09h	DTC	DTC_COMPLETE	✓		✓*4	
0Bh	ICU	ICU_SNZCANCEL	✓		✓	
0Ch	FCU	FCU_FRDYI	✓			
0Dh	LVD	LVD_LVD1	✓		✓	✓
0Eh		LVD_LVD2	✓		✓	✓
0Fh	MOSC	MOSC_STOP	✓			
10h	Low power mode	SYSTEM_SNZREQ		✓		
11h	AGT0	AGT0_AGTI	✓	✓		
12h		AGT0_AGTCMAI	✓	✓		
13h		AGT0_AGTCMBI	✓	✓		
14h	AGT1	AGT1_AGTI	✓	✓	✓	✓
15h		AGT1_AGTCMAI	✓	✓	✓	✓
16h		AGT1_AGTCMBI	✓	✓	✓	✓
17h	IWDT	IWDT_NMIUNDF	✓		✓	✓
18h	WDT	WDT_NMIUNDF	✓			
19h	RTC	RTC_ALM	✓		✓	✓
1Ah		RTC_PRD	✓		✓	✓
1Bh		RTC_CUP	✓			

Table 12.4 Event table (2 of 4)

Event number	Interrupt request source	Name	IELSRn		Canceling Snooze	Canceling Software Standby
			Connect to NVIC	Invoke DTC		
1Ch	ADC140	ADC140_ADI	✓	✓		
1Dh		ADC140_GBADI	✓	✓		
1Eh		ADC140_CMPAI	✓			
1Fh		ADC140_CMPBI	✓			
20h		ADC140_WCMPM		✓	✓*4	
21h		ADC140_WCMPUM		✓	✓*4	
22h	ACMPHS	ACMP_HS0	✓			
23h		ACMP_HS1	✓			
24h		ACMP_HS2	✓			
25h	ACMPLP	ACMP_LP0	✓		✓	✓
26h		ACMP_LP1	✓			
27h	USBFS	USBFS_USBI	✓			
28h		USBFS_USBR	✓		✓	✓
29h	IIC0	IIC0_RXI	✓	✓		
2Ah		IIC0_TXI	✓	✓		
2Bh		IIC0_TEI	✓			
2Ch		IIC0_EEI	✓			
2Dh		IIC0_WUI	✓		✓	✓
2Eh	IIC1	IIC1_RXI	✓	✓		
2Fh		IIC1_TXI	✓	✓		
30h		IIC1_TEI	✓			
31h		IIC1_EEI	✓			
32h	CTSU	CTSU_CTSUWR	✓	✓		
33h		CTSU_CTSURD	✓	✓		
34h		CTSU_CTSUFN	✓		✓*4	
35h	KINT	KEY_INTKR	✓		✓*1	✓*1
36h	DOC	DOC_DOPCI	✓		✓*4	
37h	CAC	CAC_FERRI	✓			
38h		CAC_MENDI	✓			
39h		CAC_OVFI	✓			
3Ah	CAN0	CAN0_ERS	✓			
3Bh		CAN0_RXF	✓			
3Ch		CAN0_TXF	✓			
3Dh		CAN0_RXM	✓			
3Eh		CAN0_TXM	✓			
3Fh	I/O Ports	IOPORT_GROUP1	✓	✓*2		
40h		IOPORT_GROUP2	✓	✓*2		
41h	ELC	ELC_SWEVT0	✓*3	✓		
42h		ELC_SWEVT1	✓*3	✓		
43h	POEG	POEG_GROUP0	✓			
44h		POEG_GROUP1	✓			

Table 12.4 Event table (3 of 4)

Event number	Interrupt request source	Name	IELSRn		Canceling Snooze	Canceling Software Standby
			Connect to NVIC	Invoke DTC		
45h	DALI	DALI_DEI	✓			
46h		DALI_CLI	✓			
47h		DALI_SDI	✓	✓		
48h		DALI_BPI	✓	✓		
49h		DALI_FEI	✓	✓		
4Ah		DALI_SDI_OR_BPI			✓*4	
4Bh	GPT320	GPT0_CCMPA	✓	✓		
4Ch		GPT0_CCMPB	✓	✓		
4Dh		GPT0_CMPC	✓	✓		
4Eh		GPT0_CMPD	✓	✓		
4Fh		GPT0_OVF	✓	✓		
50h		GPT0_UDF	✓	✓		
51h	GPT16H1	GPT1_CCMPA	✓	✓		
52h		GPT1_CCMPB	✓	✓		
53h		GPT1_CMPC	✓	✓		
54h		GPT1_CMPD	✓	✓		
55h		GPT1_OVF	✓	✓		
56h		GPT1_UDF	✓	✓		
57h	GPT16H2	GPT2_CCMPA	✓	✓		
58h		GPT2_CCMPB	✓	✓		
59h		GPT2_CMPC	✓	✓		
5Ah		GPT2_CMPD	✓	✓		
5Bh		GPT2_OVF	✓	✓		
5Ch		GPT2_UDF	✓	✓		
5Dh	GPT16H3	GPT3_CCMPA	✓	✓		
5Eh		GPT3_CCMPB	✓	✓		
5Fh		GPT3_CMPC	✓	✓		
60h		GPT3_CMPD	✓	✓		
61h		GPT3_OVF	✓	✓		
62h		GPT3_UDF	✓	✓		
63h	GPT164	GPT4_CCMPA	✓	✓		
64h		GPT4_CCMPB	✓	✓		
65h		GPT4_CMPC	✓	✓		
66h		GPT4_CMPD	✓	✓		
67h		GPT4_OVF	✓	✓		
68h		GPT4_UDF	✓	✓		
69h	GPT165	GPT5_CCMPA	✓	✓		
6Ah		GPT5_CCMPB	✓	✓		
6Bh		GPT5_CMPC	✓	✓		
6Ch		GPT5_CMPD	✓	✓		
6Dh		GPT5_OVF	✓	✓		
6Eh		GPT5_UDF	✓	✓		

Table 12.4 Event table (4 of 4)

Event number	Interrupt request source	Name	IELSRn		Canceling Snooze	Canceling Software Standby
			Connect to NVIC	Invoke DTC		
6Fh	GPT166	GPT6_CCMPA	✓	✓		
70h		GPT6_CCMPB	✓	✓		
71h		GPT6_CMPC	✓	✓		
72h		GPT6_CMPD	✓	✓		
73h		GPT6_OVF	✓	✓		
74h		GPT6_UDF	✓	✓		
75h	GPT	GPT_UVWEDGE	✓			
76h	SCI0	SCI0_RXI	✓	✓		
77h		SCI0_TXI	✓	✓		
78h		SCI0_TEI	✓			
79h		SCI0_ERI	✓			
7Ah		SCI0_AM	✓		✓*4	
7Bh		SCI0_RXI_OR_ERI			✓*4	
7Ch	SCI1	SCI1_RXI	✓	✓		
7Dh		SCI1_TXI	✓	✓		
7Eh		SCI1_TEI	✓			
7Fh		SCI1_ERI	✓			
80h		SCI1_AM	✓			
81h	SCI9	SCI9_RXI	✓	✓		
82h		SCI9_TXI	✓	✓		
83h		SCI9_TEI	✓			
84h		SCI9_ERI	✓			
85h		SCI9_AM	✓			
86h	SPI0	SPI0_SPRI	✓	✓		
87h		SPI0_SPTI	✓	✓		
88h		SPI0_SPII	✓			
89h		SPI0_SPEI	✓			
8Ah		SPI0_SPTEND	✓			
8Bh	SPI1	SPI1_SPRI	✓	✓		
8Ch		SPI1_SPTI	✓	✓		
8Dh		SPI1_SPII	✓			
8Eh		SPI1_SPEI	✓			
8Fh		SPI1_SPTEND	✓			
90h	AES	AES_WRREQ	✓	✓		
91h		AES_RDREQ	✓	✓		
92h	TRNG	TRNG_RDREQ	✓			

Note 1. Only supported when KRCTL.KRMD is 1.
Note 2. Only the first edge detection is valid.
Note 3. Only interrupts after DTC transfer are supported.
Note 4. Using SELSR0.

12.4 Interrupt Operation

The ICU performs the following functions:

- Detecting interrupts
- Enabling and disabling interrupts

- Selecting interrupt request destinations such as CPU interrupt or DTC activation.

12.4.1 Detecting Interrupts

External pin interrupt requests are detected in either:

- Edges (falling edge, rising edge, or rising and falling edges) of the interrupt signal
- Level (low level) of the interrupt signal.

Set the IRQMD[1:0] bits in the IRQCRi register to select the detection mode for the IRQi pins. For interrupt sources associated with peripheral module, see section 12.3.2, Event Number. Events must be accepted by the NVIC before an interrupt occurs and is accepted by the CPU.

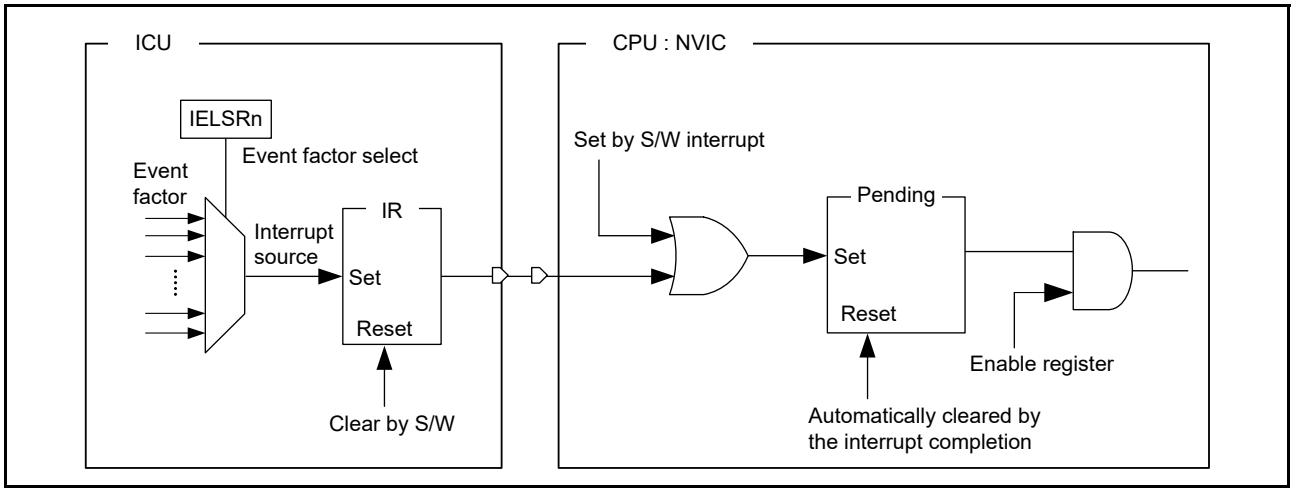


Figure 12.2 Interrupt path of the ICU and CPU (NVIC)

Operations during an interrupt:

- When a non-software interrupt is generated:
  The IELSRn.IR flag and Interrupt Set/Clear-Pending register (NVIC) are set.
- When a software interrupt is generated:
  Set the Interrupt Set-Pending register.
- When an interrupt is complete:
  Clear the IELSRn.IR flag with software.
  The Interrupt Set/Clear Pending register clears automatically.

When interrupts are enabled:

1. Set the Interrupt Set-Enable register.
2. Set the IELSRn.IELS[7:0] bits as the interrupt source.
3. Specify the operation settings for the event source.

When interrupts are disabled:

1. Disable the settings for the event source.
2. Clear the IELSRn.IELS[7:0] bits (IELSRn.IELS = 00h). Clear the IELSRn.IR flag as required.
3. Clear the Interrupt Clear-Enable register. Clear the Interrupt Clear-Pending register as required.

When polling for interrupts:

1. Set the Interrupt Clear-Enable register (disabling interrupts).
2. Set the IELSRn.IELS[7:0] bits (selecting the source).
3. Specify the operation settings for the event source.

4. Poll the Interrupt Set-Pending register.
5. When polling is no longer required, follow the procedure for clearing an interrupt when it is complete.

12.4.2 Selecting Interrupt Request Destinations

The interrupt output destination, CPU or DTC, can be independently selected for each interrupt source. The available destinations are fixed for each interrupt as described in Table 12.4.

Note: Do not use an interrupt request destination setting that is not indicated by a check, ✓, in the event list (Table 12.4).

If you select the CPU or DTC in the IELSRn register, setting the same interrupt factor in any other IELSRn register is prohibited.

If the DTC is selected as the destination for requests from an IRQi pin, you must set the IRQMD[1:0] bits in IRQCRi for that interrupt to select edge detection.

12.4.2.1 CPU interrupt request

When IELSRn.DTCE = 0, the event specified in the IELSRn register is output to the NVIC.

Set the IELSRn.IELS[7:0] bits to the target event and set the IELSRn.DTCE bit to 0.

12.4.2.2 DTC activation

When IELSRn.DTCE = 1, the event specified in the IELSRn register is output to the DTC. Use the following procedure:

1. Set the IELSRn.IELS[7:0] bits to the target event and set the IELSRn.DTCE bit to 1.
2. Set the DTC module activation bit (DTCST.DTCST) to 1.

Table 12.5 shows operation when the DTC is the request destination.

Table 12.5 Operation when DTC is activated

Interrupt request destination	DISEL*1	Remaining transfer operations	Operation per request	IR*2	Interrupt request destination after transfer
DTC*3	1	≠ 0	DTC transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	DTC
		= 0	DTC transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	The IELSRn.DTCE bit is cleared and the CPU becomes the destination
	0	≠ 0	DTC transfer	Cleared at the start of DTC data transfer after reading DTC transfer data	DTC
		= 0	DTC transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	The IELSRn.DTCE bit is cleared and the CPU becomes the destination

Note 1. Set the interrupt request mode for the DTC in the DTC.MRB.DISEL bit.
Note 2. When the IELSRn.IR flag is 1, an interrupt request (DTC activation request) that is generated again is ignored.
Note 3. For chain transfer, DTC transfer continues until the last chain transfer ends. The DISEL bit state and the remaining transfer count determine whether a CPU interrupt is generated, the IELSRn.IR flag clear timing, and the interrupt request destination after transfer. See Table 15.3, Chain transfer conditions in section 15, Data Transfer Controller (DTC).

12.4.3 Digital Filter

A digital filter function is provided for the external interrupt request pins (IRQi, i = 0 to 7) and the NMI pin interrupt. It samples input signals on the filter sampling clock (PCLKB) and removes any signal with a pulse width that is less than 3 sampling cycles.

To use the digital filter for an IRQi pin:

1. Set the sampling clock cycle to PCLKB, PCLKB/8, PCLKB/32, or PCLKB/64 with the IRQCRi.FCLKSEL[1:0]

bits (i = 0 to 7).

2. Set the IRQCRi.FLTEN bit (i = 0 to 7) to 1 (digital filter enabled).

To use the digital filter for the NMI pin:

1. Set the sampling clock cycle to PCLKB, PCLKB/8, PCLKB/32, or PCLKB/64 with the NMICR.NFCLKSEL[1:0] bits.
2. Set the NMICR.NFLTEN bit to 1 (digital filter enabled).

Figure 12.3 shows an example of digital filter operation.

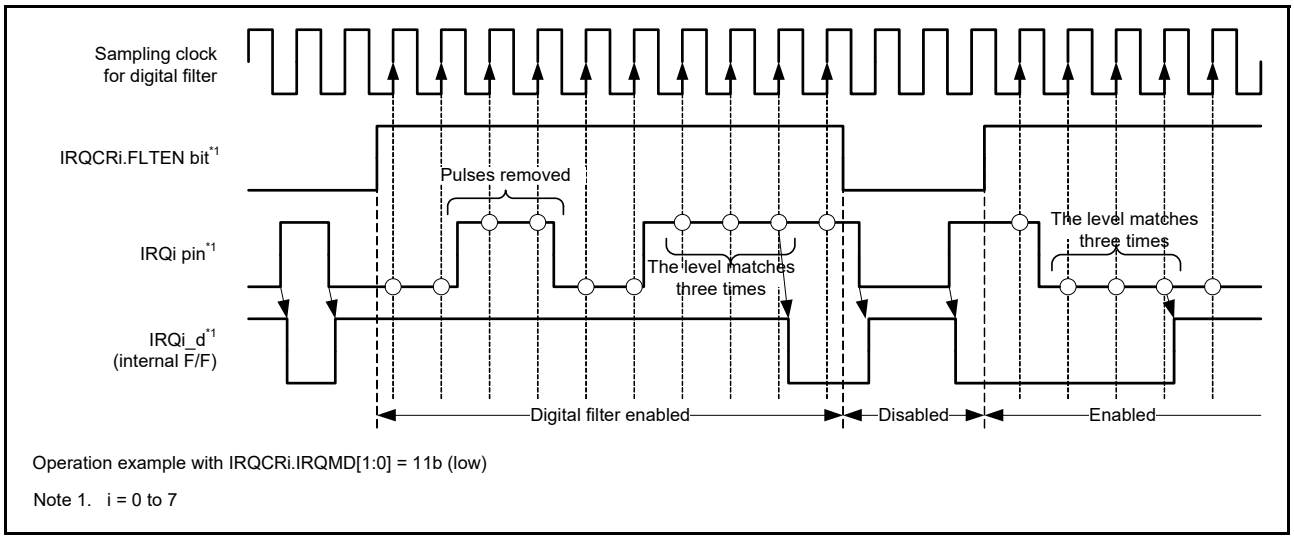


Figure 12.3 Digital filter operation example

Before entering Software Standby mode, disable the digital filters by clearing the IRQCRi.FLTEN and NMICR.NFLTEN bits. The clock of the ICU stops in Software Standby mode. On exiting Software Standby mode, you can enable the digital filters again. The circuit detects the edge by comparing the state before standby to the state after standby release. If the input changes during Software Standby mode, an incorrect edge might be detected.

12.4.4 External Pin Interrupts

To use external pin interrupts:

1. Clear the IRQCRi.FLTEN bit (i = 0 to 7) to 0 (digital filter disabled).
2. Set or confirm the I/O port settings.
3. Set the IRQMD[1:0] bits, the FCLKSEL[1:0] bits, and the FLTEN bit of the IRQCRi register.
4. Select the IRQ pin as follows:
   - If the IRQ pin is to be used for CPU interrupt requests, set the IELSRn.IELS[7:0] bits and the IELSRn.DTCE bit to 0
   - If the IRQ pin is to be used for DTC activation, set the IELSRn.IELS[7:0] bits and the IELSRn.DTCE bit to 1.

12.5 Non-Maskable Interrupt Operation

The following sources can trigger a non-maskable interrupt:

- NMI pin interrupt
- Oscillation stop detection interrupt
- WDT underflow/refresh error interrupt
- IWDT underflow/refresh error interrupt
- Voltage monitor 1 interrupt

- Voltage monitor 2 interrupt
- SRAM parity error interrupt
- SRAM ECC error interrupt
- MPU bus master error interrupt
- MPU bus slave error interrupt
- CPU stack pointer monitor interrupt.

Non-maskable interrupts can only be used with the CPU, not to activate the DTC. Non-maskable interrupts take precedence over all other interrupts. The non-maskable interrupt states can be verified in the Non-Maskable Interrupt Status Register (NMISR). Confirm that all bits in the NMISR are 0 before returning from the NMI handler.

Non-maskable interrupts are disabled by default. To use non-maskable interrupts, use the following procedure:

To use the NMI pin, follow steps 1 to 3.

1. Clear the NMICR.NFLTEN bit to 0 (digital filter disabled).
2. Set the NMIMD bit, NFCLKSEL[1:0] bits, and NFLTEN bit of NMICR register.
3. Write 1 to the NMICLR.NMICLR bit to clear the NMISR.NMIST flag to 0.
4. Enable the non-maskable interrupt by writing 1 to the associated bit in the Non-Maskable Interrupt Enable Register (NMIER).

After 1 is written to the NMIER register, subsequent write access to the NMIEN bit in NMIER is ignored. When an NMI interrupt is enabled, it can be disabled only by a reset.

12.6 Return from Low Power Modes

Table 12.4, Event table lists the interrupt sources you can use to exit Sleep mode or Software Standby mode. For details, see section 10, Low Power Modes. Sections 12.6.1 to 12.6.3 describe how to use interrupts to return from Sleep, Software Standby, and Snooze modes.

12.6.1 Return from Sleep Mode

To return from Sleep mode in response to an interrupt:

1. Select the CPU as the interrupt request destination.
2. Enable the interrupt in the NVIC.

To return from Sleep mode in response to a non-maskable interrupt, enable the given interrupt request in the NMIER register.

12.6.2 Return from Software Standby Mode

The ICU can return from Software Standby mode using a non-maskable interrupt or an interrupt selected in the WUPEN register. See section 12.2.8, Wake Up Interrupt Enable Register (WUPEN).

To return from Software Standby mode:

1. Select the interrupt source that enables return from Software Standby:
   - For non-maskable interrupts, use the NMIER register to enable the target interrupt request
   - For maskable interrupts, use the WUPEN register to enable the target interrupt request.
2. Select the CPU as the interrupt request destination.
3. Enable the interrupt in the NVIC.

Interrupt requests through the IRQ pins that do not satisfy these conditions are not detected while the clock is stopped in Software Standby mode.

12.6.3 Return from Snooze Mode

The ICU can return from Snooze mode using the interrupts provided for this mode.

To return to Normal mode from Snooze mode:

1. Use either of the following methods to select the event that you want to trigger a return to Normal mode from Snooze mode:
   - Set the event that you want to trigger a return to Normal mode from Snooze mode in SELSR0.SEL and set the value 0Bh (ICU_SNZCANCEL) in IELSRn.IELS
   - Set the event that you want to trigger a return to Normal mode from Snooze mode in IELSRn.IELS.
2. Select the CPU as the interrupt request destination.
3. Enable the interrupt in the NVIC.

Note: In Snooze mode, a clock is supplied to the ICU. If an event selected in IELSRn is detected, the CPU acknowledges the interrupt after returning to Normal mode from Software Standby mode.

12.7 Using the WFI Instruction with Non-maskable Interrupt

Whenever a WFI instruction is executed, confirm that all status flags in the NMISR register are 0.

12.8 Reference

ARM® Cortex®-M0+ Processor Technical Reference Manual (ARM DDI 0484C).

13. Buses

13.1 Overview

Table 13.1 lists the bus specifications, Figure 13.1 shows the bus configuration, and Table 13.2 lists the addresses assigned for each bus.

Table 13.1 Bus specifications

Bus type		Description
Main bus	System bus (CPU)	• Connected to CPU • Connected to on-chip memory and internal peripheral bus.
	DMA bus	• Connected to DTC • Connected to on-chip memory and internal peripheral bus.
Slave Interface	Memory bus 1	• Connected to code flash memory.
	Memory bus 4	• Connected to SRAM0.
	Internal peripheral bus 1	• Connected to system control related to peripheral modules.
	Internal peripheral bus 3	• Connected to peripheral modules (CAC, ELC, I/O Ports, POEG, RTC, WDT, IWDT, IIC, CAN, ADC14, DOC, GPT, PWM Delay Generation Circuit, SCI, SPI, and CRC).
	Internal peripheral bus 5	• Connected to peripheral modules (KINT, AGT, USBFS, DALI, DAC8, OPAMP, ACMPHS, ACMPLP, and CTSU).
	Internal peripheral bus 7	• Connected to Secure IPs.
	Internal peripheral bus 9	• Connected to flash memory (in P/E) and data flash memory.

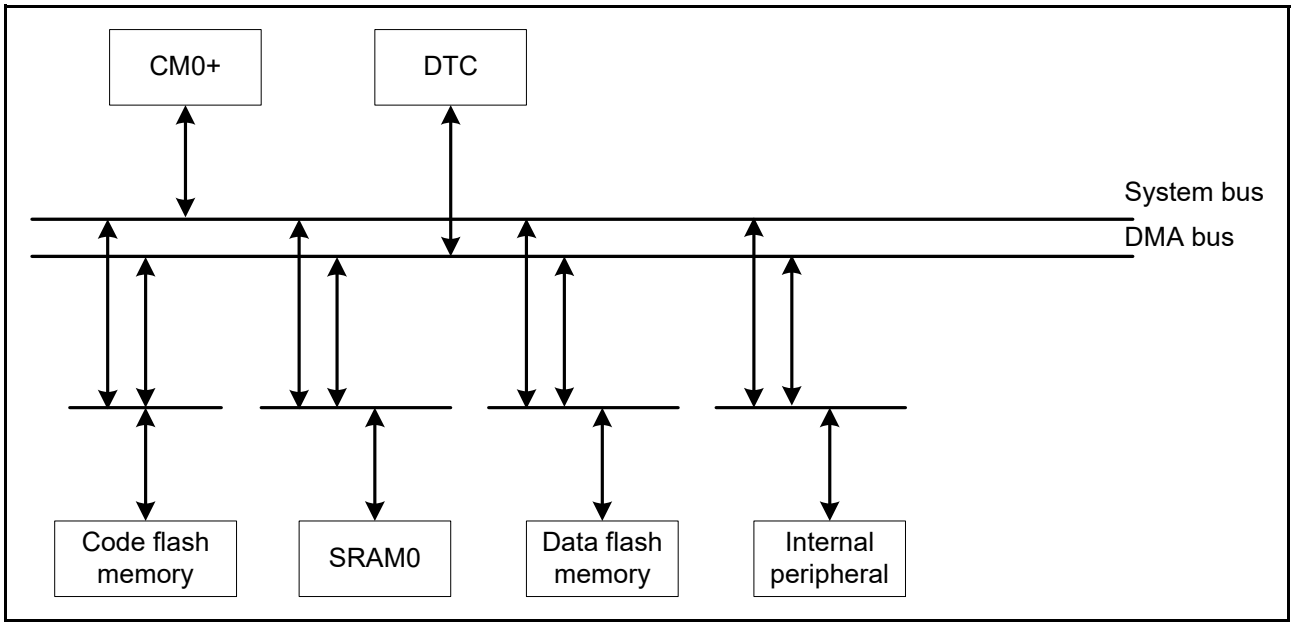


Figure 13.1 Bus configuration

Table 13.2 Addresses assigned for each bus (1 of 2)

Address	Bus	Area
0000 0000h to 01FF FFFFh	Memory bus 1	Code flash memory
2000 0000h to 2000 5FFFh	Memory bus 4	SRAM0
4000 0000h to 4001 8FFFh	Internal peripheral bus 1	Peripheral I/O registers
4001 9000h to 4001 9FFFh	Memory bus 4	MTB I/O registers

Table 13.2 Addresses assigned for each bus (2 of 2)

Address	Bus	Area
4001 A000h to 4001 FFFFh	Internal peripheral bus 1	Peripheral I/O registers
4004 0000h to 4007 FFFFh	Internal peripheral bus 3	
4008 0000h to 400B FFFFh	Internal peripheral bus 5	
400C 0000h to 400D FFFFh	Internal peripheral bus 7	Secure IPs
4010 0000h to 407F FFFFh	Internal peripheral bus 9	Flash memory (in P/E*1) and data flash memory

Note 1. P/E = Programming/Erasure

13.2 Description of Buses

13.2.1 Main Buses

The main bus consists of the system bus and DMA bus. System bus and DMA bus are connected to the following:

- Code flash memory
- SRAM0
- Data flash memory
- Internal peripheral bus.

The system bus is used for instruction code and data code access to the CPU.

Different master and slave transfer combinations can proceed simultaneously. In addition, requests for bus access from masters other than the DTC are not accepted during reads of transfer control information for the DTC.

13.2.2 Slave Interface

For connections from the main bus to the slave interface, see the slave interface in Table 13.1, Bus specifications.

Bus access from the system bus and DMA bus are arbitrated. The arbitration method is selectable to fixed priority or round-robin. For more information, see section 13.3.2.

Different master and slave transfer combinations can proceed simultaneously.

13.2.3 Parallel Operation

Parallel operations are possible when different bus masters request access to different slave modules. Figure 13.2 shows an example of parallel operations. In this example, the CPU uses the instruction and operand buses for simultaneous access to the flash and SRAM, respectively. Additionally, the DTC simultaneously uses the DMA bus for access to a peripheral bus during access to the flash and SRAM by the CPU.

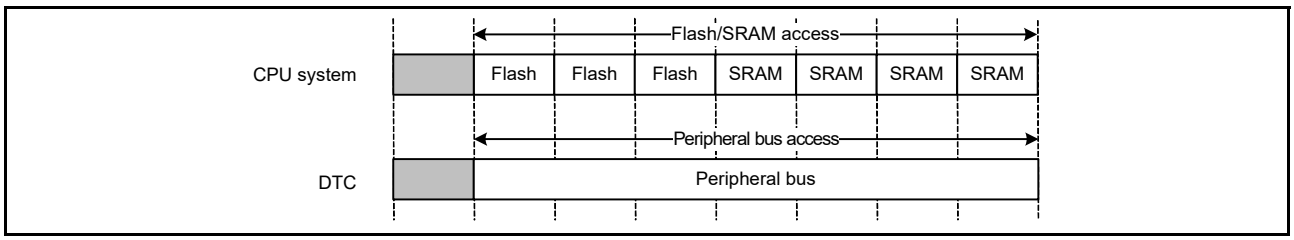


Figure 13.2 Example of parallel operations

13.2.4 Constraints

(1) Endianness Constraint

Memory space must be little-endian to execute code on the Cortex®-M0+ core.

13.3 Register Descriptions

13.3.1 Master Bus Control Register (BUSMCNT<master>)

Address(es): BUS.BUSMCNTSYS 4000 4008h, BUS.BUSMCNTDMA 4000 400Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IERES	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b14 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	IERES	Ignore Error Responses	0: A bus error is reported 1: A bus error is not reported.	R/W

Note: Changing reserved bits from the initial value of 0 is prohibited. Operation during the change is not guaranteed.

IERES bit (Ignore Error Responses)

The IERES bit disables the AHB-Lite protocol error response.

Table 13.3 shows the registers associated with each bus type.

Table 13.3 Associations between bus types and registers

Bus type	Master Bus Control Register	Slave Bus Control Register	Bus Error Address Register	Bus Error Status Register
System bus (CPU)	BUSMCNTSYS	—	BUS3ERRADD	BUS3ERRSTAT
DMA bus	BUSMCNTDMA	—	BUS4ERRADD	BUS4ERRSTAT
Memory bus 1	—	BUSSCNTFLI	—	—
Memory bus 4	—	BUSSCNTRAM0	—	—
Internal peripheral bus 1, 3, 5, 7	—	BUSSCNTPnB [n=0, 2, 4, 6]	—	—
Internal peripheral bus 9	—	BUSSCNTFBU	—	—

13.3.2 Slave Bus Control Register (BUSSCNT<slave>)

Address(es): BUS.BUSSCNTFLI 4000 4100h, BUS.BUSSCNTRAM0 4000 410Ch, BUS.BUSSCNTP0B 4000 4114h, BUS.BUSSCNTP2B 4000 4118h, BUS.BUSSCNTP4B 4000 4120h, BUS.BUSSCNTP6B 4000 4128h, BUS.BUSSCNTFBU 4000 4130h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	ARBMET[1:0]		—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5, b4	ARBMET[1:0]	Arbitration Method	Specifies the group priorities: b5 b4 0 0: Fixed priority 0 1: Round-robin 1 0: Setting prohibited 1 1: Setting prohibited.	R/W
b15 to b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Changing reserved bits from the initial value of 0 is prohibited. Operation during the change is not guaranteed.

ARBMET[1:0] bits (Arbitration Method)

The ARBMET[1:0] bits specify the arbitration method, with priority defined for all bus masters. For fixed priority, see Table 13.4. For round-robin, see Table 13.5. For the associations between bus types and registers, see Table 13.3.

Table 13.4 Fixed priority (ARBMET[1:0] = 00b)

Slave Bus Control Register	Slave interface	Priority
BUSSCNTFLI	Memory bus 1	DMA bus > System bus (CPU)
BUSSCNTRAM0	Memory bus 4	DMA bus > System bus (CPU)
BUSSCNTPnB [n = 0, 2, 4, 6]	Internal peripheral bus 1, 3, 5, 7	DMA bus > System bus (CPU)
BUSSCNTFBU	Internal peripheral bus 9	DMA bus > System bus (CPU)

Table 13.5 Round-robin priority (ARBMET[1:0] = 01b)

Slave Bus Control Register	Slave interface	Priority*1
BUSSCNTFLI	Memory bus 1	DMA bus ↔ System bus (CPU)
BUSSCNTRAM0	Memory bus 4	DMA bus ↔ System bus (CPU)
BUSSCNTPnB [n = 0, 2, 4, 6]	Internal peripheral bus 1, 3, 5, 7	DMA bus ↔ System bus (CPU)
BUSSCNTFBU	Internal peripheral bus 9	DMA bus ↔ System bus (CPU)

Note 1. Round-robin priority is denoted by '↔'.

13.3.3 Bus Error Address Register (BUSnERRADD) (n = 3, 4)

Address(es): BUS.BUS3ERRADD 4000 4820h, BUS.BUS4ERRADD, 4000 4830h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BERAD[31:16]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BERAD[15:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Bit name	Description	R/W
b31 to b0	BERAD[31:0]	Bus Error Address	When a bus error occurs, these bits store the error address	R

Note: This register is only cleared by resets other than MPU-related resets. For more information, see section 5, Resets, and section 14, Memory Protection Unit (MPU).

Table 13.3 lists the registers associated with each bus type.

BERAD[31:0] bits (Bus Error Address)

The BERAD[31:0] bits store the address being accessed when a bus error occurred. For more information, see the description of the BUSnERRSTAT.ERRSTAT bit and section 13.4, Bus Error Monitoring Section.

The value of the BUSnERRADD.BERAD[31:0] bits (n = 3, 4) is valid only when the BUSnERRSTAT.ERRSTAT bit (n = 3, 4) is set to 1.

13.3.4 BUS Error Status Register (BUSnERRSTAT) (n = 3, 4)

Address(es): BUS.BUS3ERRSTAT 4000 4824h, BUS.BUS4ERRSTAT 4000 4834h

	b7	b6	b5	b4	b3	b2	b1	b0
	ERRSTAT	—	—	—	—	—	—	ACCSTAT
Value after reset:	0	0	0	0	0	0	0	x

Bit	Symbol	Bit name	Description	R/W
b0	ACCSTAT	Error Access Status	Access status when the error occurred: 1: Write access 0: Read access.	R
b6 to b1	—	Reserved	These bits are read as 0.	R
b7	ERRSTAT	Bus Error Status	0: No bus error occurred 1: Bus error occurred.	R

Note: This register is only cleared by resets other than MPU-related resets. For more information, see section 5, Resets, and section 14, Memory Protection Unit (MPU).

Table 13.3 lists the registers associated with each bus type.

ACCSTAT bit (Error Access Status)

The ACCSTAT bit indicates the access status (write or read) when a bus error occurs. For more information, see the description of the BUSnERRSTAT.ERRSTAT bit and section 13.4, Bus Error Monitoring Section.

The value is valid only when the BUSnERRSTAT.ERRSTAT bit (n = 3, 4) is set to 1.

ERRSTAT bit (Bus Error Address)

The ERRSTAT bit indicates whether a bus error occurred. When a bus error occurs, the BUSnERRSTATn.ERRSTAT (n = 3, 4) bit is set to 1 and the access address and access status (write or read) are stored.

There are four types of bus errors as listed below:

- Illegal address access
- Bus master MPU error
- Bus slave MPU error
- Time out.

When detecting bus master-MPU errors or bus slave-MPU errors, with the reset selected in the OAD bit, if the bus access that caused the MPU error completes later than the internal reset signal being generated (this can occur with the wait setting), BUSnERRSTAT.ERRSTAT (n = 3, 4) is not set to 1.

When detecting bus master-MPU errors or bus slave-MPU errors, and NMI is selected by the OAD bit, after the bus access that caused the MPU error completes, BUSnERRSTAT.ERRSTAT (n = 3,4) is set to 1.

For more information on these bus errors, see section 13.4, Bus Error Monitoring Section and section 14, Memory Protection Unit (MPU).

13.4 Bus Error Monitoring Section

The monitoring system monitors each individual area, and whenever it detects an error, it returns the error to the requesting master IP using the AHB-Lite protocol.

13.4.1 Error Type that Occurs by Bus

There are four types of bus errors:

- Illegal address access

- Bus master MPU error
- Bus slave MPU error
- Timeout.

Table 13.6 lists the address ranges where access leads to illegal address access errors. The reserved area in the slave does not trigger an illegal address access error. For more information on bus master MPU and bus slave MPU, see section 14, Memory Protection Unit (MPU).

13.4.2 Operation when a Bus Error Occurs

When a bus error occurs, operation is not guaranteed, and the error is returned to the requesting master IP. The bus errors that occur for each master are stored in the BUSnERRADD and BUSnERRSTAT registers. These registers must be cleared by reset only. For more information, see sections 13.3.3 and 13.3.4.

Note: DTC does not receive bus errors. If the DTC accesses the bus, the transfer continues.

13.4.3 Conditions Leading to Illegal Address Access Errors

Table 13.6 lists the address spaces for each bus that trigger illegal address access errors.

Table 13.6 Conditions leading to illegal address access errors

Address	Slave bus name	Master bus	
		CPU	
		System	DMA
0000 0000h to 01FF FFFFh	Memory bus 1	-	-
0200 0000h to 1FFF FFFFh	Reserved	E	E
2000 0000h to 2000 5FFFh	Memory bus 4	-	-
2000 6000h to 3FFF FFFFh	Reserved	E	E
4000 0000h to 4001 FFFFh	Peripheral bus 1	-	-
4002 0000h to 4003 FFFFh	Reserved	E	E
4004 0000h to 4007 FFFFh	Peripheral bus 3	-	-
4008 0000h to 400B FFFFh	Peripheral bus 5	-	-
400C 0000h to 400D FFFFh	Peripheral bus 7	-	-
400E 0000h to 400F FFFFh	Reserved	E	E
4010 0000h to 407F FFFFh	Peripheral bus 9	-	-
4080 0000h to DFFF FFFFh	Reserved	E	E
E000_0000h to FFFF_FFFFh	System for Cortex-M0+	-	E

Note: E indicates the path where an illegal address access error occurs.
Note: — indicates the path where an illegal address access error did not occur.
Note: The bus module detects an access error resulting from access to reserved area, for example if no area is assigned for the slave.
0200 0000h to 1FFF FFFFh: Access error detection.
0000 0000h to 01FF FFFFh: Memory bus 1 no access error detection.

13.4.4 Timeout

For some peripheral modules, a timeout error occurs with the module-stop function. When there is no response from the slave for a certain time period, a timeout error is detected. A timeout error is returned to the requesting master IP using the AHB-Lite error response protocol.

13.5 References

1. *ARM® Cortex®-M0+ Devices Generic User Guide* (ARM DUI 0662B)
2. *ARM® AMBA® 3 AHB-Lite Protocol v1.0 Specification* (ARM IHI 0033A).

14. Memory Protection Unit (MPU)

14.1 Overview

The MCU provides four Memory Protection Units (MPUs) and a CPU stack pointer monitor function. Table 14.1 lists the supported MPU specifications, and Table 14.2 shows the behavior on detection of each MPU error.

Table 14.1 MPU specifications

Classification	Module/Function	Description
Illegal memory access	Arm® Cortex®-M CPU	• Arm CPU has a default memory map. If the CPU makes an illegal access, an exception interrupt occurs • The MPU can change a default memory map.
	CPU stack pointer monitor	2 regions: • Main Stack Pointer (MSP) • Process Stack Pointer (PSP).
Memory protection	Arm MPU	Memory protection function for the CPU: • 8 MPU regions with subregions and background region.
	Bus master MPU	Memory protection function for each bus master except for the CPU: • Bus master MPU group A: 4 regions.
	Bus slave MPU	Memory protection function for each bus slave
Security	Security MPU	Protect accesses from non-secure programs to the following secure regions: • 2 regions (PC) • 4 regions (code flash, SRAM, two secure function).

Table 14.2 Behavior on MPU error detection

MPU type	Notification type	Bus access on error detection	Storing of error access information
CPU stack pointer monitor	Reset or non-maskable interrupt	Don't care	Not stored
Arm MPU	Hard fault	• Does not correctly have write access • Does not correctly have read access.	Not stored
Bus master MPU	Reset or non-maskable interrupt	• Write access to the protection region • Read access to the protection region.	Stored
Bus slave MPU	• Reset or non-maskable interrupt • Hard fault.	• Write access ignored • Read access read as 0.	Stored
Security MPU	Not notified	• Does not correctly have write access • Does not correctly have read access.	Not stored

For information on error access for Arm MPU, see section 14.7. For information on error access for other MPUs, see section 13.3.3, Bus Error Address Register (BUSnERRADD) (n = 3, 4) and section 13.3.4, BUS Error Status Register (BUSnERRSTAT) (n = 3, 4) in section 13, Buses.

14.2 CPU Stack Pointer Monitor

The CPU stack pointer monitor detects underflows and overflows of the stack pointer. Because the Arm CPU has two stack pointers, a Main Stack Pointer (MSP) and a Process Stack Pointer (PSP), it supports two CPU stack pointer monitors. If a stack pointer underflow or overflow is detected, the CPU stack pointer monitor generates a reset or a non-maskable interrupt. The CPU stack pointer monitor is enabled by setting the Stack Pointer Monitor Enable bit in the Stack Pointer Monitor Access Control Register (MSPMPUCTL, PSPMPUCTL) to 1.

Table 14.3 lists the specifications of the CPU stack pointer monitor. Figure 14.1 shows a CPU stack pointer monitor block diagram, and Figure 14.2 shows the register setting flow.

Table 14.3 CPU stack pointer monitor specifications

Parameter	Description
SRAM region	Region to be covered by memory protection
Number of regions	2 regions: • main stack pointer • process stack pointer
Address specification for individual regions	Region start and end addresses configurable
Stack pointer monitor enable or disable setting for individual regions	Stack pointer monitor for individual regions can be enabled or disabled
Operation on error detection	Reset or non-maskable interrupt
Register protection	Registers can be protected from illegal writes

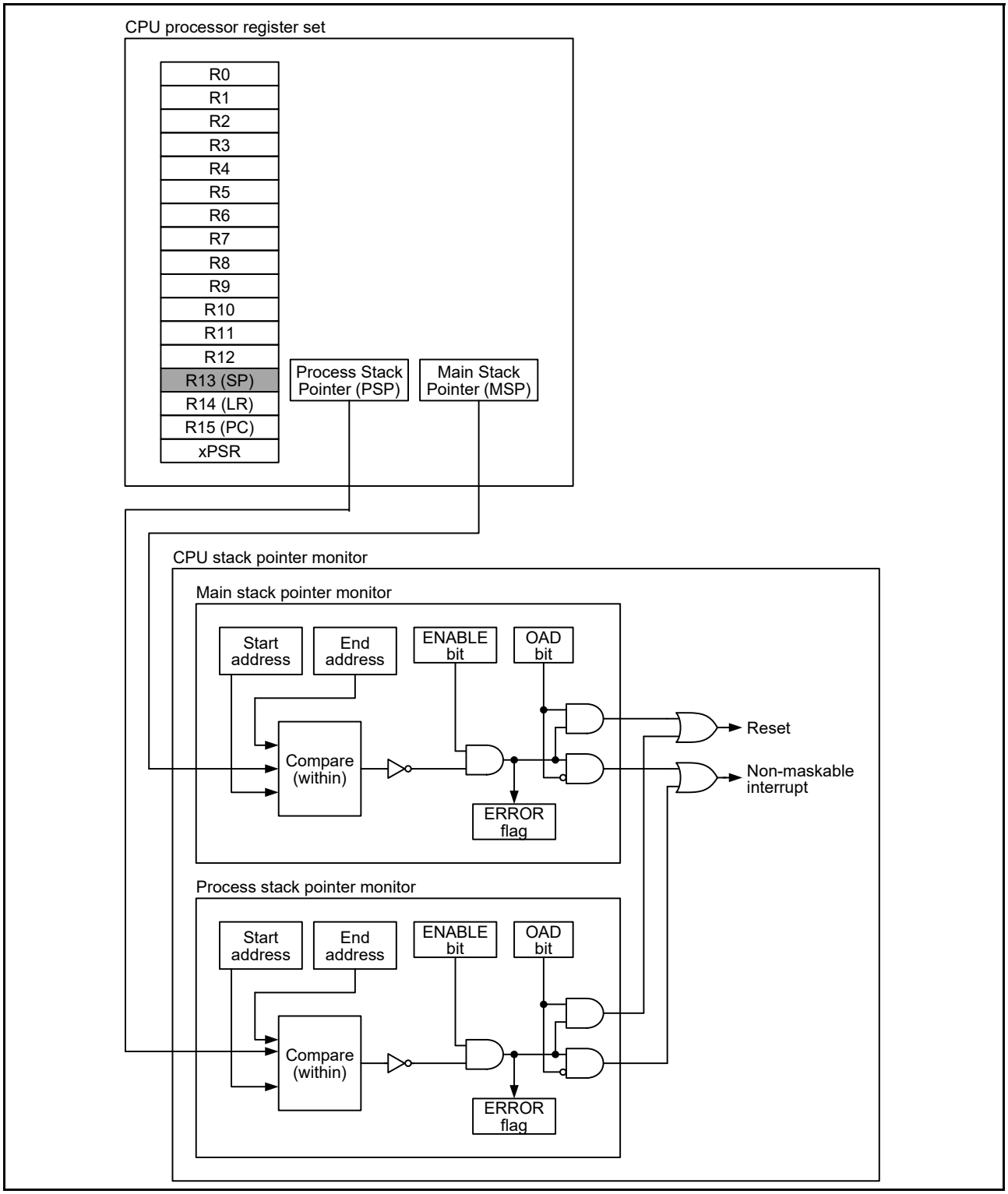


Figure 14.1 CPU stack pointer monitor block diagram

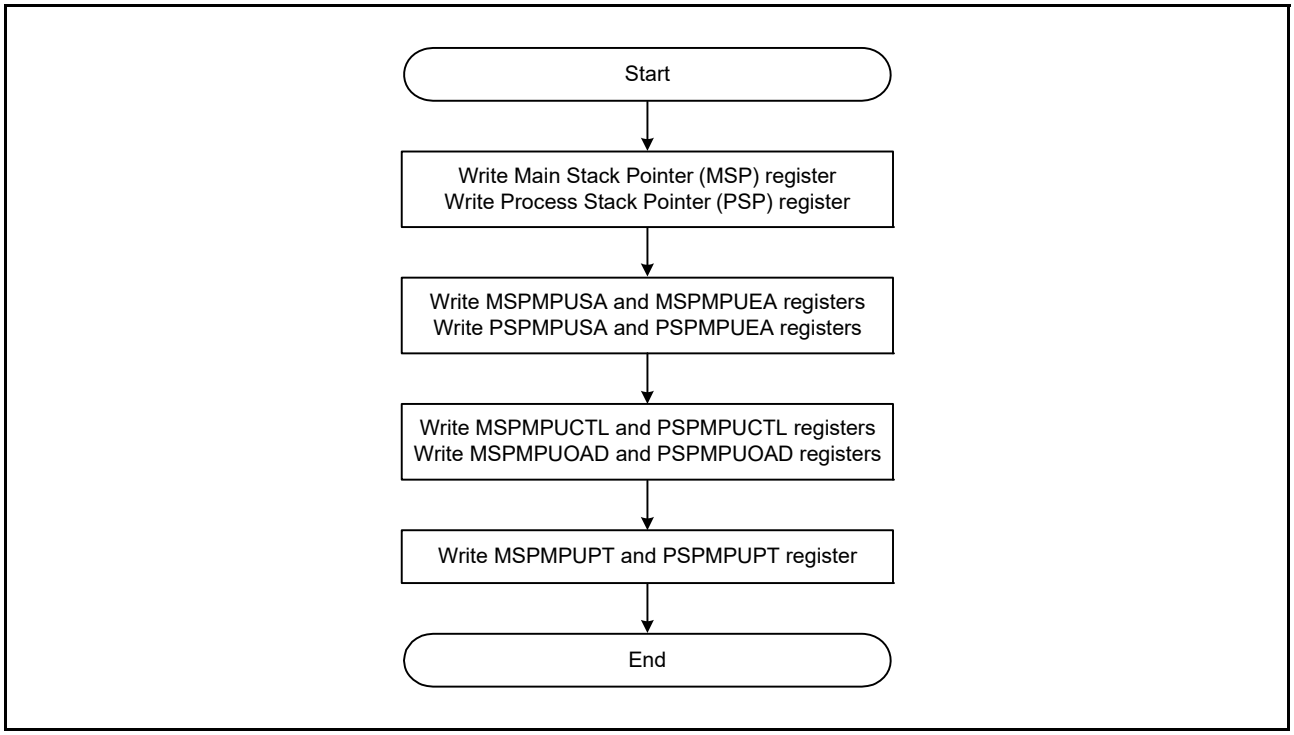


Figure 14.2 Register setting flow

14.2.1 Protection of Registers

Registers related to the CPU stack pointer monitor can be protected with the PROTECT bit.

14.2.2 Overflow/Underflow Error

If an overflow or underflow is detected, the CPU stack pointer monitor generates an overflow or underflow error. The memory protection error is selectable to a non-maskable interrupt or a reset in the OAD bit setting.

The non-maskable interrupt status is indicated in ICU.NMISR.SPEST. For details, see section 12, Interrupt Controller Unit (ICU). The reset status is indicated in SYSTEM.RSTSR1.SPERF. For details, see section 5, Resets.

When ICU.NMISR.SPEST indicates that a CPU stack pointer monitor interrupt occurred, check the ERROR bits in the MSPMPUCTL and PSPMPUCTL registers to determine whether it is a main stack pointer monitor error or a process stack pointer monitor error.

A non-maskable interrupt is generated continuously when the stack pointer overflows or underflows. To clear the non-maskable interrupt flag, set the stack pointer in the specified region and then set the ICU.NMICLR.SPECLR bit to 1. Then, write 0 to clear the ERROR bit in the MSPMPUCTL and PSPMPUCTL registers.

14.2.3 Register Descriptions

Note: Stop bus access before writing to MPU registers.

14.2.3.1 Main Stack Pointer (MSP) Monitor Start Address Register (MSPMPUSA)

Address(es): SPMON.MSPMPUSA 4000 0D08h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MSPMPUSA[31:16]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MSPMPUSA[15:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b31 to b0	MSPMPUSA[31:0]	Region Start Address	Address that determines where the region starts. The lower 2 bits should be 0. The value range is from 1FF0 0000h to 200F FFFCh, not including the reserved areas.	R/W

The MSPMPUSA and MSPMPUEA registers specify the CPU stack region in the SRAM (1FF0 0000h to 200F FFFFh), not including the reserved areas. For SRAM area to be covered, see Figure 4.1, Memory map.

14.2.3.2 Main Stack Pointer (MSP) Monitor End Address Register (MSPMPUEA)

Address(es): SPMON.MSPMPUEA 4000 0D0Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MSPMPUEA[31:16]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MSPMPUEA[15:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b31 to b0	MSPMPUEA[31:0]	Region End Address	Address where the region ends, for use in region determination. The lower 2 bits should be 1. The value range is from 1FF0 0003h to 200F FFFFh, not including the reserved areas.	R/W

14.2.3.3 Process Stack Pointer (PSP) Monitor Start Address Register (PSPMPUSA)

Address(es): SPMON.PSPMPUSA 4000 0D18h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PSPMPUSA[31:16]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PSPMPUSA[15:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b31 to b0	PSPMPUSA[31:0]	Region Start Address	Address where the region starts, for use in region determination. The lower 2 bits should be 0. The value range is from 1FF0 0000h to 200F FFFCh, not including the reserved areas.	R/W

The PSPMPUSA and PSPMPUEA registers specify the CPU stack region in the SRAM (1FF0 0000h to 200F FFFFh), not including the reserved areas. For SRAM area to be covered, see Figure 4.1, Memory map.

14.2.3.4 Process Stack Pointer (PSP) Monitor End Address Register (PSPMPUEA)

Address(es): SPMON.PSPMPUEA 4000 0D1Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PSPMPUEA[31:16]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PSPMPUEA[15:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b31 to b0	PSPMPUEA[31:0]	Region End Address	Address where the region ends, for use in region determination. The lower 2 bits should be 1. The value range is from 1FF0 0003h to 200F FFFFh, not including the reserved areas.	R/W

14.2.3.5 Stack Pointer Monitor Operation After Detection Register (MSPMPUOAD, PSPMPUOAD)

Address(es): SPMON.MSPMPUOAD 4000 0D00h, SPMON.PSPMPUOAD 4000 0D10h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	—	OAD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	OAD	Operation after Detection	0: Non-maskable interrupt 1: Reset.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	KEY[7:0]	Key Code	These bits enable or disable writes to the OAD bit	R/(W)*1

Note 1. Write data is not retained.

OAD bit (Operation after Detection)

The OAD bit selects a reset or a non-maskable interrupt when a stack pointer underflow or overflow is detected by the CPU stack pointer monitor.

The main stack pointer monitor and the process stack pointer monitor each uses the OAD bit to determine which signal is generated when a stack pointer underflow or overflow is detected. When writing to the OAD bit, write A5h simultaneously to the KEY[7:0] bits using halfword access.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writes to the OAD bit. When writing the OAD bit, write A5h simultaneously to KEY[7:0]. When values other than A5h are written to the KEY[7:0] bits, the OAD bit is not updated. The KEY[7:0] bits are always read as 00h.

14.2.3.6 Stack Pointer Monitor Access Control Register (MSPMPUCTL, PSPMPUCTL)

Address(es): SPMON.MSPMPUCTL 4000 0D04h, SPMON.PSPMPUCTL 4000 0D14h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ERROR	—	—	—	—	—	—	—	ENABLE
Value after reset:	0	0	0	0	0	0	0	0/1*1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ENABLE	Stack Pointer Monitor Enable	0: Disable stack pointer monitor 1: Enable stack pointer monitor.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	ERROR	Stack Pointer Monitor Error Flag	0: Stack pointer has not overflowed or underflowed 1: Stack pointer has overflowed or underflowed.	R/W
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The initial value depends on the reset generation sources.

ENABLE bit (Stack Pointer Monitor Enable)

The ENABLE bit enables or disables the stack pointer monitor function, independently set for the main stack pointer monitor and the process stack pointer monitor.

When the MSPMPUCTL.ENABLE bit is set to 1, the following registers are available:

- MSPMPUSA
- MSPMPUEA
- MSPMPUOAD.

When the PSPMPUCTL.ENABLE bit is set to 1, the following registers are available:

- PSPMPUSA
- PSPMPUEA
- PSPMPUOAD.

ERROR bit (Stack Pointer Monitor Error Flag)

The ERROR bit indicates the state of stack pointer monitor. Each stack pointer monitor has an independent ERROR bit.

[Setting condition]

- Overflow or underflow of the stack pointer.

[Clearing condition]

- 0 is written to this bit
- A reset other than the bus master MPU error reset, bus slave MPU error reset, and stack pointer error reset.

Note: Only 0 can be written to the ERROR bit.

14.2.3.7 Stack Pointer Monitor Protection Register (MSPMPUPT, PSPMPUPT)

Address(es): SPMON.MSPMPUPT 4000 0D06h, SPMON.PSPMPUPT 4000 0D16h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PROTECT	Protection of register	0: Stack Pointer Monitor register writes are possible 1: Stack Pointer Monitor register writes are protected. Read is possible.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	KEY[7:0]	Key Code	These bits enable or disable writes to the PROTECT bit	R/(W)*1

Note 1. Write data is not retained.

PROTECT bit (Protection of register)

The PROTECT bit enables or disables writes to the associated registers to be protected, independently set for the main stack pointer monitor and the process stack pointer monitor.

MSPMPUPT.PROTECT controls the following main stack pointer protection registers:

- MSPMPUCTL
- MSPMPUSA
- MSPMPUEA.

PSPMPUPT.PROTECT controls the following process stack pointer protection registers:

- PSPMPUCTL
- PSPMPUSA
- PSPMPUEA.

When writing to the PROTECT bit, simultaneously write A5h to KEY[7:0] using halfword access.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writes to the PROTECT bit.

When writing the PROTECT bit, write A5h to KEY[7:0] simultaneously. When values other than A5h are written to the KEY[7:0] bits, the PROTECT bit is not updated. The KEY[7:0] bits are always read as 0.

14.3 Arm MPU

The Arm MPU has eight region memory protection units and provides full support for:

- Protected regions
- Overlapping protected regions, with ascending region priority:
  7 = highest priority
  0 = lowest priority.
- Access permissions
- Export of memory attributes to the system.

Arm MPU mismatches and permission violations invoke the HardFault handler. For details, see section 14.7, References.

14.4 Bus Master MPU

The bus master MPU monitors the addresses accessed by the bus master in the entire address space (0000 0000h to FFFF FFFFh).

Access control, consisting of read and write permissions, can be independently set for up to four regions. The bus master MPU monitors access to each region based on these settings. If access to the protected region is detected, the bus master MPU generates an internal reset or a non-maskable interrupt. For details on error access, see section 13.3.3, Bus Error Address Register (BUSnERRADD) (n = 3, 4) and section 13.3.4, BUS Error Status Register (BUSnERRSTAT) (n = 3, 4) in section 13, Buses.

Table 14.4 lists the specifications of the bus master MPU and Figure 14.3 shows a block diagram.

Table 14.4 Bus master MPU specifications

Specifications	Description
Protected master groups	Bus master MPU group A: DMA bus
Protected region	0000 0000h to FFFF FFFFh
Number of regions	Bus master MPU group A: 4 regions
Address specification for individual regions	Region start and end addresses configurable
Enable/disable setting for memory protection in individual regions	Settings enabled or disabled for the associated region
Access-control settings for individual regions	Permission to read and write
Operation on error detection	Reset or non-maskable interrupts
Register protection	Register can be protected from illegal writes

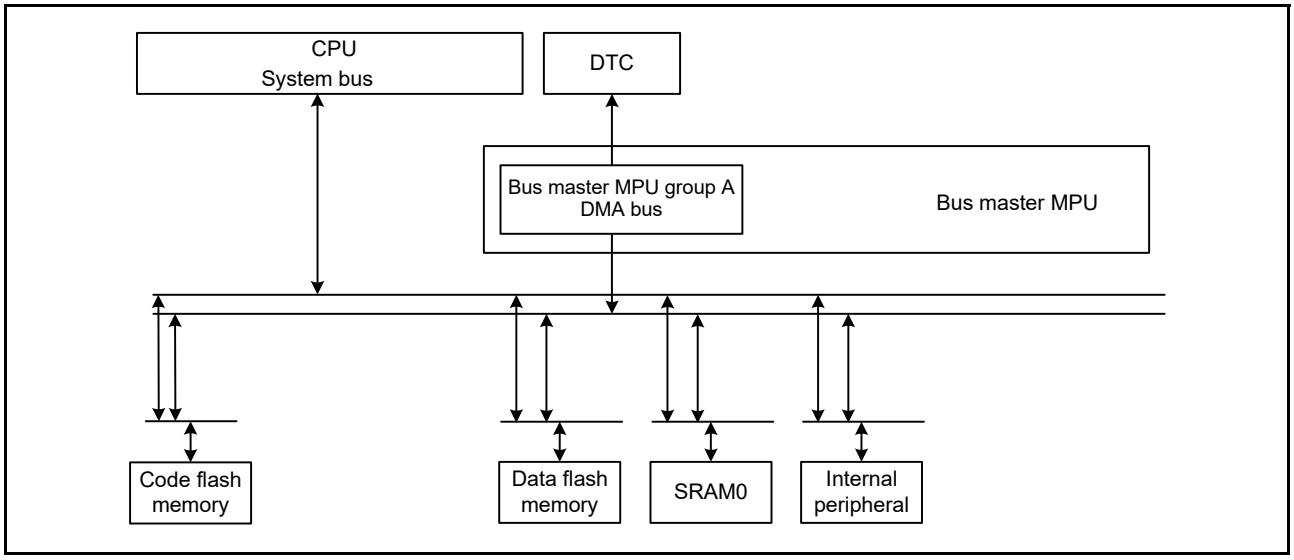


Figure 14.3 MPU bus master diagram

Figure 14.4 shows the MPU bus master group A.

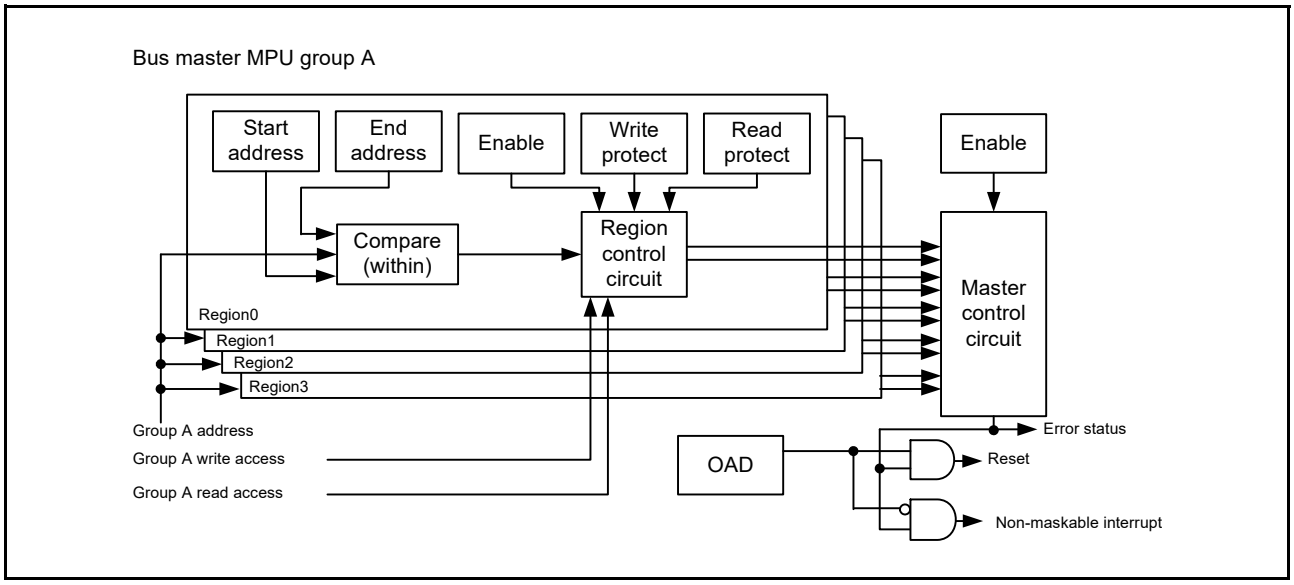


Figure 14.4 MPU bus master group A

14.4.1 Register Descriptions

Note: Stop bus access before processing register writes.

14.4.1.1 Group A Region n Start Address Register (MMPUSAn) (n = 0 to 3)

Address(es): MMPU.MMPUSA0 4000 0204h, MMPU.MMPUSA1 4000 0214h, MMPU.MMPUSA2 4000 0224h, MMPU.MMPUSA3 4000 0234h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MMPUSA[31:16]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MMPUSA[15:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	MMPUSA[31:0]	Region Start Address	Address where the region starts, for use in region determination. The lower 2 bits should be 0.	R/W

14.4.1.2 Group A Region n End Address Register (MMPUEAn) (n = 0 to 3)

Address(es): MMPU.MMPUEA0 4000 0208h, MMPU.MMPUEA1 4000 0218h, MMPU.MMPUEA2 4000 0228h, MMPU.MMPUEA3 4000 0238h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MMPUEA[31:16]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MMPUEA[15:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b31 to b0	MMPUEA[31:0]	Region End Address	Address where the region ends, for use in region determination. The lower 2 bits should be 1.	R/W

14.4.1.3 Group A Region n Access Control Register (MMPUACAn) (n = 0 to 3)

Address(es): MMPU.MMPUACA0 4000 0200h, MMPU.MMPUACA1 4000 0210h, MMPU.MMPUACA2 4000 0220h, MMPU.MMPUACA3 4000 0230h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	WP	RP	ENABLE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ENABLE	Region Enable	0: Group A region n unit disabled 1: Group A region n unit enabled.	R/W
b1	RP	Read Protection	0: Read access permitted 1: Read access protected.	R/W
b2	WP	Write Protection	0: Write access permitted 1: Write access protected.	R/W
b15 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The ENABLE, RP, and WP bits are individually configurable for each group A region n.

ENABLE bit (Region Enable)

The ENABLE bit enables or disables group A region n unit.

When the ENABLE bit is set to 1, the RP and WP bits can be set to permit or protect access to the region that is set in MMPUSmn and MMPUEmn. When the ENABLE bit is set to 0, no region is specified for group A region n access.

RP bit (Read Protection)

The RP bit enables or disables read protection for group A region n. The RP bit is available when the ENABLE bit is set to 1.

WP bit (Write Protection)

The WP bit enables or disables write protection for group A region n. The WP bit is available when the ENABLE bit is set to 1.

Table 14.5 Function of region control circuit

MMPUACAn.ENABLE	MMPUACAn.RP	MMPUACAn.WP	Access	Region	Output of Group A Region n unit
0	—	—	Read	—	Outside of region
			Write		Outside of region
1	0	0	Read	Inside	Permitted region
				Outside	Outside of region
			Write	Inside	Permitted region
				Outside	Outside of region
	0	1	Read	Inside	Permitted region
				Outside	Outside of region
			Write	Inside	Protection region
				Outside	Outside of region
	1	0	Read	Inside	Protection region
				Outside	Outside of region
			Write	Inside	Permitted region
				Outside	Outside of region
	1	1	Read	Inside	Protection region
				Outside	Outside of region
			Write	Inside	Protection region
				Outside	Outside of region

n = 0 to 3

Table 14.6 Function of master control circuit

MMPUCTLA.ENABLE	Output of group A region 0 unit	Output of group A region 1 unit	Output of group A region 2 to 3 unit	Function of group A
1	Protected region	Don't care	Don't care	Generate error
1	Don't care	Protected region	Don't care	Generate error
1	Don't care	Don't care	Protected region	Generate error
1	Outside of region	Outside of region	Outside of region	Generate error
Other case				No error

A master MPU error occurs on the following conditions:

- MMPUCTLA.ENABLE = 1, and output of one or more region n units is to a protected region
- MMPUCTLA.ENABLE = 1, and output of all region n units is outside of region.

Other cases are for permitted regions.

14.4.1.4 Bus Master MPU Control Register (MMPUCTLA)

Address(es): MMPU.MMPUCTLA 4000 0000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	OAD	ENABLE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ENABLE	Master Group Enable	0: Master group A disabled 1: Master group A enabled.	R/W
b1	OAD	Operation After Detection	0: Non-maskable interrupt 1: Reset.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	KEY[7:0]	Key Code	These bits enable or disable writes to the OAD and ENABLE bits	R/(W)*1

Note 1. Write data is not retained.

ENABLE bit (Master Group Enable)

The ENABLE bit enables or disables the bus master MPU function for master group A. When this bit is set to 1, MMPUACAn is available. When this bit is set to 0, MMPUACAn is unavailable, including permission for all regions. When the ENABLE bit is set, write A5h to KEY[7:0] simultaneously using halfword access.

OAD bit (Operation After Detection)

The OAD bit generates a reset or non-maskable interrupt when access to the protected region is detected by the bus master MPU. When the OAD bit is set, write A5h to KEY[7:0] simultaneously using halfword access.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writes to the ENABLE and OAD bits. When writing to the ENABLE and OAD bits, write A5h to KEY[7:0] simultaneously. When values other than A5h are written to the KEY[7:0] bits, the ENABLE and the OAD bits are not updated. The KEY[7:0] bits are always read as 00h.

14.4.1.5 Group A Protection of Register (MMPUPTA)

Address(es): MMPU.MMPUPTA 4000 0102h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PROTECT	Protection of register	0: All bus master MPU group A register writes are permitted 1: All bus master MPU group A register writes are protected. Read access is possible.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	KEY[7:0]	Key Code	These bits enable or disable writes to the PROTECT bit	R/(W)*1

Note 1. Write data is not retained.

PROTECT bit (Protection of register)

The PROTECT bit enables or disables writes to the associated registers to be protected. MMPUPTA.PROTECT controls the bus master MPU group A protection registers. The following registers are protected by MMPUPTA.PROTECT:

- MMPUSAn
- MMPUEAn
- MMPUACAn
- MMPUCTLA.

When the PROTECT bit is set, write A5h to KEY[7:0] simultaneously using halfword access.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writes to the PROTECT bit. When writing to the PROTECT bit, write A5h to KEY[7:0] simultaneously. When values other than A5h are written to the KEY[7:0] bits, the PROTECT bit is not updated. The KEY[7:0] bits are always read as 00h.

14.4.2 Functions

(1) Memory protection

The bus master MPU monitors memory access using the control settings made individually for the access control regions. If access to the protected region is detected, the bus master MPU generates a memory protection error.

The bus master MPU can be set for up to 4 protected regions. Protected regions include those with overlapping permitted and protected regions, and those with two overlapping permitted regions.

The bus master MPU has group A. The memory protection function checks the address of the bus for the master group, and all master group accesses are protected. The bus master MPU sets the permission for all the regions after reset. Setting MMPUCTLA.ENABLE to 1 protects all of the regions. Each region sets up a permitted region within the protected region. If access to the protected region is detected, the bus master MPU generates an error.

Figure 14.5 shows the use case of a bus master MPU.

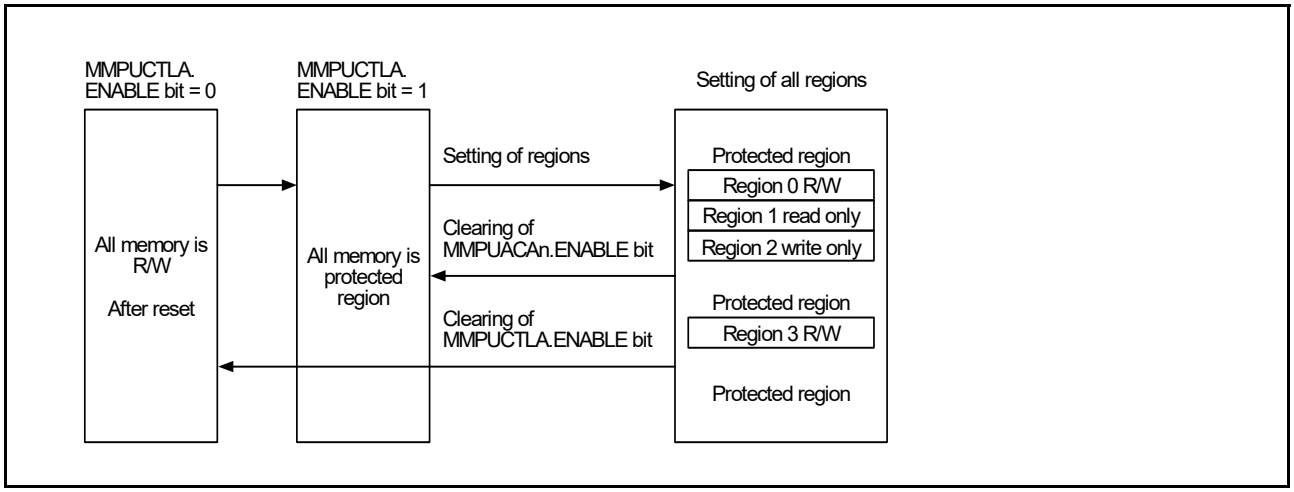


Figure 14.5 Use case of bus master MPU

Figure 14.6 shows the access permission or protection for the overlapping bus master MPU regions. Access control for the overlapping regions is as follows:

1. The region is handled as a protected region when output of one or more region unit is a protected region.
2. The region is handled as a protected region when output of all region units is outside of the region.
3. Other cases are handled as permitted regions.

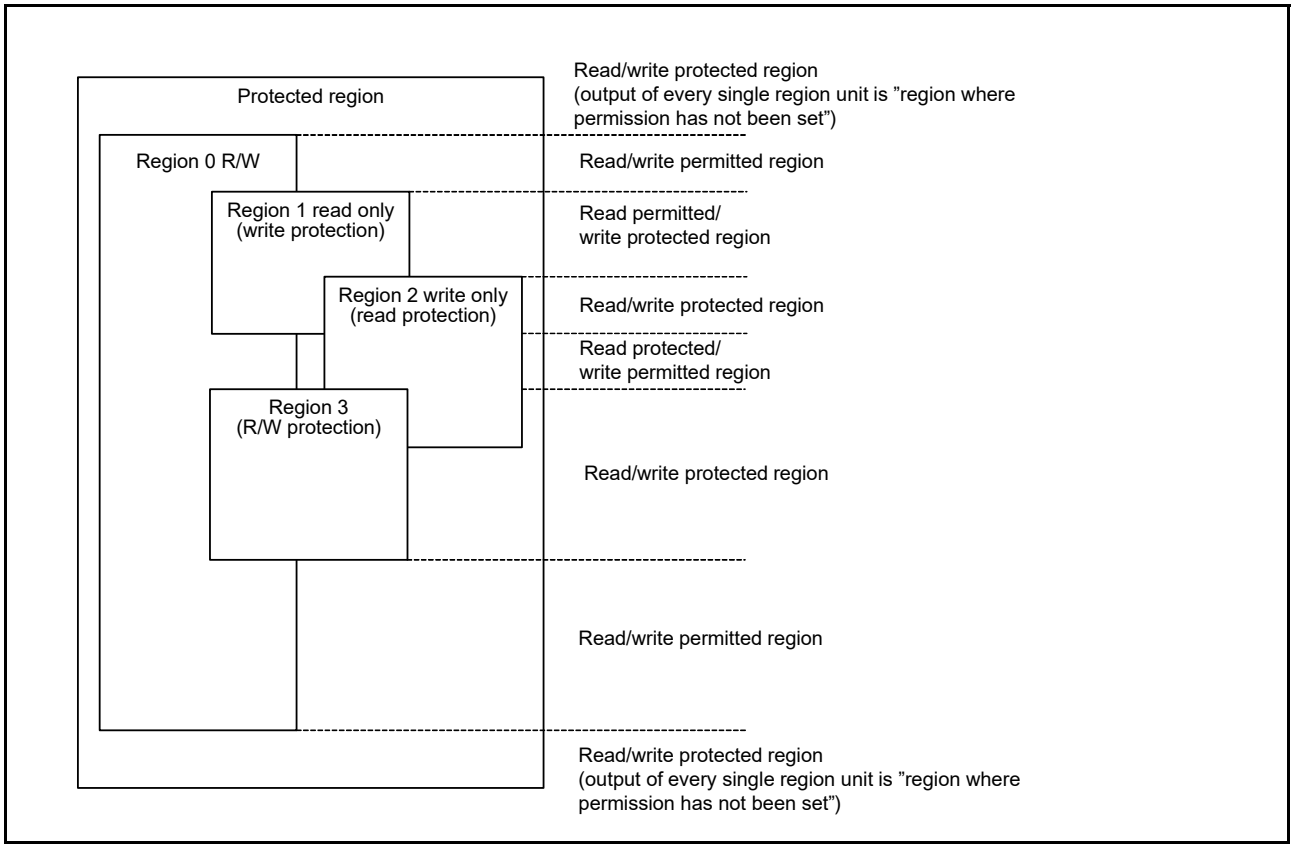


Figure 14.6 Access permission or protection by overlap of the bus master MPU regions

Figure 14.7 shows the register setting flow after reset. During this register setting, stop all the masters except the CPU.

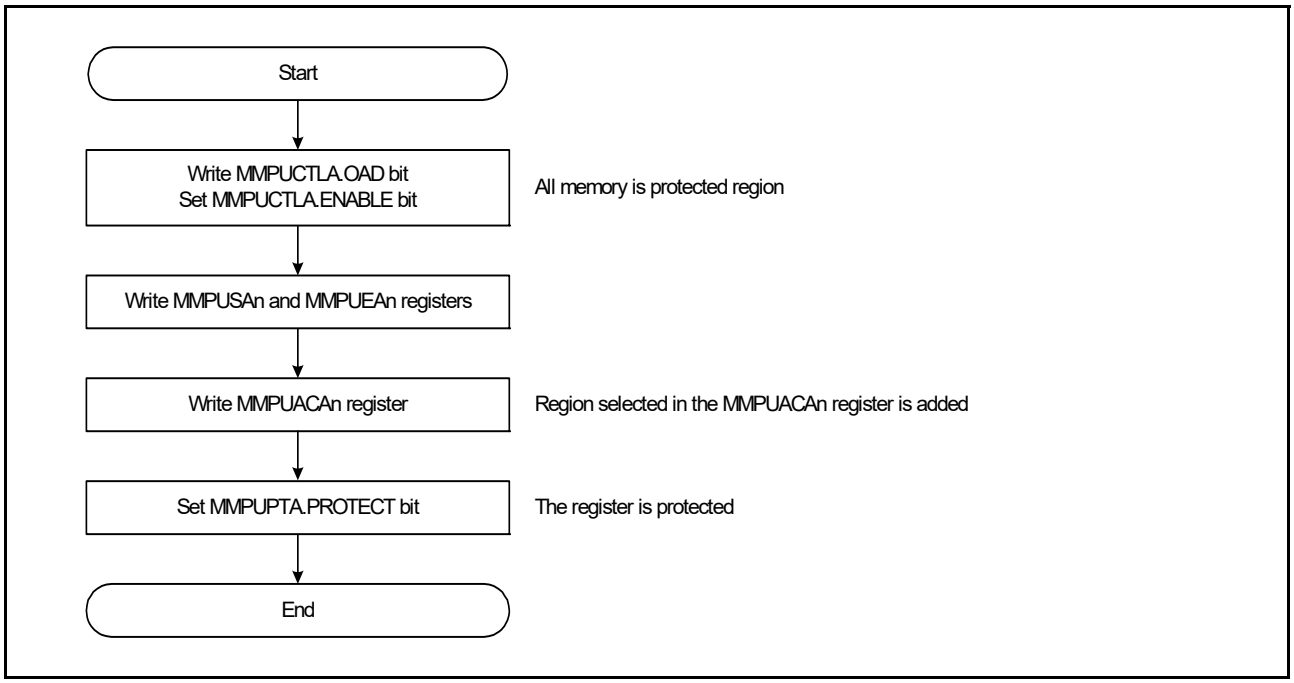


Figure 14.7 Register setting flow after reset

Figure 14.8 shows the register setting flow for adding regions. During this register setting, stop all the masters except the CPU.

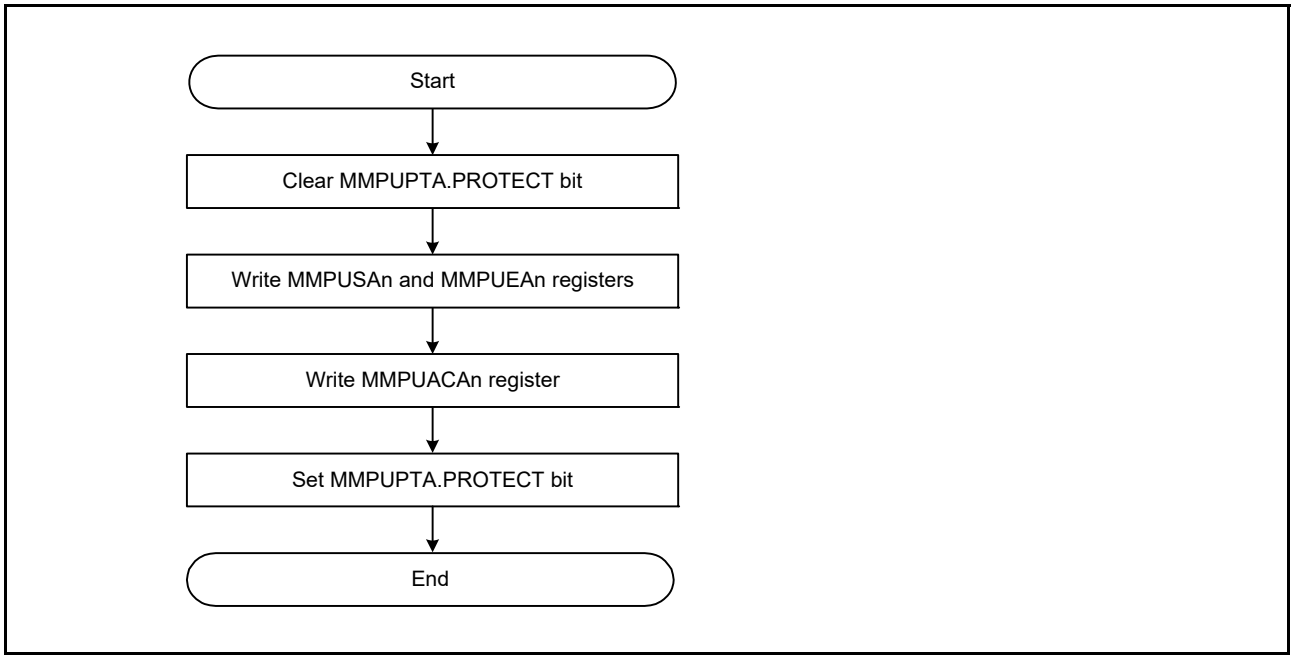


Figure 14.8 Register setting flow for region addition

14.4.2.1 Protection of registers

To protect the registers related to the bus master MPU, set the PROTECT bit in the MMPUPTA register.

14.4.2.2 Memory protection error

If access to the protected region is detected, the bus master MPU generates an error. Set the OAD bit to select whether the error is reported as a non-maskable interrupt or reset. The non-maskable interrupt is indicated in ICU.NMISR.BUSMST. For details, see section 12, Interrupt Controller Unit (ICU). The reset status is indicated in SYSTEM.RSTSR1.BUSMRF. For details, see section 5, Resets.

14.5 Bus Slave MPU

The bus slave MPU monitors access to the bus slave function, such as flash or SRAM. The bus slave function can be accessed from the CPU bus master and the bus master MPU group A. The bus slave MPU has a separate protection register for each of the two bus masters, with individual access protection control. If access to a protected region is detected, the bus slave MPU generates a reset or a non-maskable interrupt, and can store the bus error status, error access status, and bus error address in the I/O Registers. For details, see section 13.3.3, Bus Error Address Register (BUSnERRADD) (n = 3, 4) and section 13.3.4, BUS Error Status Register (BUSnERRSTAT) (n = 3, 4) in section 13, Buses. The supported access control information for the individual regions consists of permission to read and write.

Table 14.7 lists the specifications of the bus slave MPU and Figure 14.9 shows a block diagram.

Table 14.7 Bus slave MPU specifications (1 of 2)

Specifications	Description
Protected bus master	Bus master MPU group A: DMA bus
Protected slave functions	Memory bus 1: Code flash memory Memory bus 4: SRAM0 Internal peripheral bus 1: Peripheral modules related system control Internal peripheral bus 3: CAC, ELC, I/O ports, POEG, RTC, WDT, IWDT, IIC, CAN, ADC14, DOC, GPT, PWM Delay Generation Circuit, SCI, SPI, and CRC Internal peripheral bus 5: KINT, AGT, USBFS, DALI, DAC8, OPAMP, ACMPHS, ACMPLP, and CTSU Internal peripheral bus 7: SecureIP (AES and TRNG) Internal peripheral bus 9: Flash memory (in P/E) and data flash memory

Table 14.7 Bus slave MPU specifications (2 of 2)

Specifications	Description
Access-control information settings for individual regions	Permission to read and write
Operation after detection	Reset or non-maskable interrupt
Protection of register	Register can be protected from illegal writes

The bus slave MPU is located on each bus slave side and controls the permission or protection of access from each bus master to each bus slave.

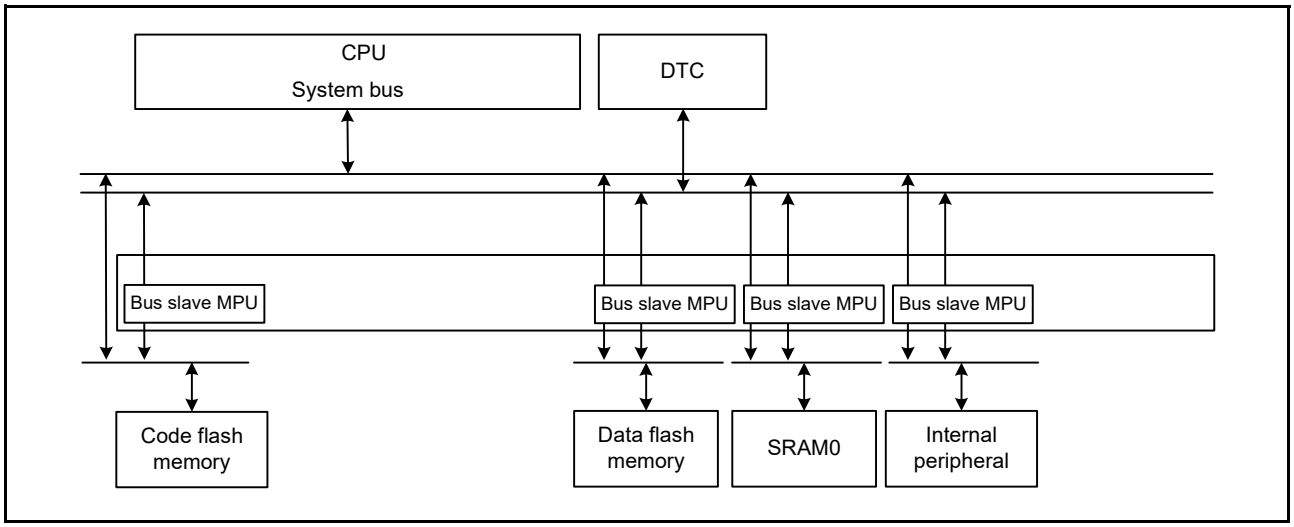


Figure 14.9 Bus slave MPU block diagram

14.5.1 Register Descriptions

Note: Stop bus access before processing register writes.

14.5.1.1 Access Control Register for Memory Bus 1 (SMPUMBIU)

Address(es): SMPU.SMPUMBIU 4000 0C10h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b2	RPGRPA	Master Group A Read Protection	0: Master group A read memory protection disabled 1: Master group A read memory protection enabled.	R/W
b3	WPGRPA	Master Group A Write Protection	0: Master group A write memory protection disabled 1: Master group A write memory protection enabled.	R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RPGRPA bit (Master Group A Read Protection)

The RPGRPA bit enables or disables memory protection for master group A reads on memory bus 1.

WPGRPA bit (Master Group A Write Protection)

The WPGRPA bit enables or disables memory protection for master group A writes on memory bus 1.

14.5.1.2 Access Control Register for Internal Peripheral Bus 9 (SMPUFBIU)

Address(es): SMPU.SMPUFBIU 4000 0C14h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	WPCPU	RPCPU
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RPCPU	CPU Read Protection	0: CPU read memory protection disabled 1: CPU read memory protection enabled.	R/W
b1	WPCPU	CPU Write Protection	0: CPU write memory protection disabled 1: CPU write memory protection enabled.	R/W
b2	RPGRPA	Master Group A Read Protection	0: Master group A read memory protection disabled 1: Master group A read memory protection enabled.	R/W
b3	WPGRPA	Master Group A Write Protection	0: Master group A write memory protection disabled 1: Master group A write memory protection enabled.	R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RPCPU bit (CPU Read Protection)

The RPCPU bit enables or disables memory protection for CPU reads on internal peripheral bus 9.

WPCPU bit (CPU Write Protection)

The WPCPU bit enables or disables memory protection for CPU writes on internal peripheral bus 9.

RPGRPA bit (Master Group A Read Protection)

The RPGRPA bit enables or disables memory protection for master group A reads on internal peripheral bus 9.

WPGRPA bit (Master Group A Write Protection)

The WPGRPA bit enables or disables memory protection for master group A writes on internal peripheral bus 9.

14.5.1.3 Access Control Register for Memory Bus 4 (SMPUSRAM0)

Address(es): SMPU.SMPUSRAM0 4000 0C18h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	WPCPU	RPCPU
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RPCPU	CPU Read Protection	0: CPU read memory protection disabled 1: CPU read memory protection enabled.	R/W
b1	WPCPU	CPU Write Protection	0: CPU write memory protection disabled 1: CPU write memory protection enabled.	R/W
b2	RPGRPA	Master Group A Read Protection	0: Master group A read memory protection disabled 1: Master group A read memory protection enabled.	R/W
b3	WPGRPA	Master Group A Write Protection	0: Master group A write memory protection disabled 1: Master group A write memory protection enabled.	R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RPCPU bit (CPU Read Protection)

The RPCPU bit enables or disables memory protection for CPU reads on memory bus 4.

WPCPU bit (CPU Write Protection)

The WPCPU bit enables or disables memory protection for CPU writes on memory bus 4.

RPGRPA bit (Master Group A Read Protection)

The RPGRPA bit enables or disables memory protection for master group A reads on memory bus 4.

WPGRPA bit (Master Group A Write Protection)

The WPGRPA bit enables or disables memory protection for master group A writes on memory bus 4.

14.5.1.4 Access Control Register for Internal Peripheral Bus 1 (SMPUP0BIU)

Address(es): SMPU.SMPUP0BIU 4000 0C20h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	WPCPU	RPCPU
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RPCPU	CPU Read Protection	0: CPU read memory protection disabled 1: CPU read memory protection enabled.	R/W
b1	WPCPU	CPU Write Protection	0: CPU write memory protection disabled 1: CPU write memory protection enabled.	R/W
b2	RPGRPA	Master Group A Read Protection	0: Master group A read memory protection disabled 1: Master group A read memory protection enabled.	R/W
b3	WPGRPA	Master Group A Write Protection	0: Master group A write memory protection disabled 1: Master group A write memory protection enabled.	R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RPCPU bit (CPU Read Protection)

The RPCPU bit enables or disables memory protection for CPU reads on internal peripheral bus 1.

WPCPU bit (CPU Write Protection)

The WPCPU bit enables or disables memory protection for CPU writes on internal peripheral bus 1.

RPGRPA bit (Master Group A Read Protection)

The RPGRPA bit enables or disables memory protection for master group A reads on internal peripheral bus 1.

WPGRPA bit (Master Group A Write Protection)

The WPGRPA bit enables or disables memory protection for master group A writes on internal peripheral bus 1.

14.5.1.5 Access Control Register for Internal Peripheral Bus 3 (SMPUP2BIU)

Address(es): SMPU.SMPUP2BIU 4000 0C24h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	WPCPU	RPCPU
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RPCPU	CPU Read Protection	0: CPU read memory protection disabled 1: CPU read memory protection enabled.	R/W
b1	WPCPU	CPU Write Protection	0: CPU write memory protection disabled 1: CPU write memory protection enabled.	R/W
b2	RPGRPA	Master Group A Read Protection	0: Master group A read memory protection disabled 1: Master group A read memory protection enabled.	R/W
b3	WPGRPA	Master Group A Write Protection	0: Master group A write memory protection disabled 1: Master group A write memory protection enabled.	R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RPCPU bit (CPU Read Protection)

The RPCPU bit enables or disables memory protection for CPU reads on internal peripheral bus 3 and internal peripheral bus 5.

WPCPU bit (CPU Write Protection)

The WPCPU bit enables or disables memory protection for CPU writes on internal peripheral bus 3 and internal peripheral bus 5.

RPGRPA bit (Master Group A Read Protection)

The RPGRPA bit enables or disables memory protection for master group A reads on internal peripheral bus 3 and internal peripheral bus 5.

WPGRPA bit (Master Group A Write Protection)

The WPGRPA bit enables or disables memory protection for master group A writes on internal peripheral bus 3 and internal peripheral bus 5.

14.5.1.6 Access Control Register for Internal Peripheral Bus 7 (SMPUP6BIU)

Address(es): SMPU.SMPUP6BIU 4000 0C28h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	WPCPU	RPCPU
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RPCPU	CPU Read Protection	0: CPU read memory protection disabled 1: CPU read memory protection enabled.	R/W
b1	WPCPU	CPU Write Protection	0: CPU write memory protection disabled 1: CPU write memory protection enabled.	R/W
b2	RPGRPA	Master Group A Read Protection	0: Master group A read memory protection disabled 1: Master group A read memory protection enabled.	R/W
b3	WPGRPA	Master Group A Write Protection	0: Master group A write memory protection disabled 1: Master group A write memory protection enabled.	R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RPCPU bit (CPU Read Protection)

The RPCPU bit enables or disables memory protection for CPU reads on internal peripheral bus 7.

WPCPU bit (CPU Write Protection)

The WPCPU bit enables or disables memory protection for CPU writes on internal peripheral bus 7.

RPGRPA bit (Master Group A Read Protection)

The RPGRPA bit enables or disables memory protection for master group A reads on internal peripheral bus 7.

WPGRPA bit (Master Group A Write Protection)

The WPGRPA bit enables or disables memory protection for master group A writes on internal peripheral bus 7.

14.5.1.7 Slave MPU Control Register (SMPUCTL)

Address(es): SMPU.SMPUCTL 4000 0C00h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	PROTECT	OAD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	OAD	Operation after Detection	0: Non-maskable interrupt 1: Reset.	R/W
b1	PROTECT	Protection of Register	0: All bus slave register writes are permitted 1: All bus slave register writes are protected. Read is possible.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	KEY[7:0]	Key Code	These bits enable or disable writes to the OAD and PROTECT bits	R/(W)*1

Note 1. Write data is not retained.

OAD bit (Operation after Detection)

The OAD bit generates a reset or non-maskable interrupt when access to the protected region is detected by the bus slave MPU. When the OAD bit is set, write A5h to KEY[7:0] simultaneously using halfword access.

PROTECT bit (Protection of Register)

The PROTECT bit enables or disables writes to the associated registers to be protected. The following registers are protected by SMPUCTL.PROTECT:

- SMPUMBIU
- SMPUFBIU

- SMPUSRAM0
- SMPUP0BIU
- SMPUP2BIU
- SMPUP6BIU.

When the PROTECT bit is set, write A5h to KEY[7:0] simultaneously using halfword access.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writes to the OAD and PROTECT bits. When writing to the OAD and PROTECT bits, write A5h to KEY[7:0] simultaneously. When values other than A5h are written to the KEY[7:0] bits, the OAD and the PROTECT bits are not updated. The KEY[7:0] bits are always read as 00h.

14.5.2 Functions

14.5.2.1 Memory protection

The bus slave MPU monitoring uses access control information that is set for the individual access control registers, whether or not access by the bus slaves violates the access control settings. If access to the protected region is detected, the bus slave MPU generates a memory protection error.

The bus slave MPU is enabled by writing 1 to the Write Protect (WPCPU or WPGRPA) bit or the Read Protect (RPCPU or RPGRPA) bit in the access control registers SMPUMBIU, SMPUFBIU, SMPUSRAM0, SMPUP0BIU, SMPUP2BIU, and SMPUP6BIU.

14.5.2.2 Protection of registers

Registers related to the bus slave MPU can be protected with the PROTECT bit in the SMPUCTL register.

14.5.2.3 Memory protection error

If access to a protected region is detected, the bus slave MPU generates a memory protection error. Set the OAD bit to select whether the error is reported as a non-maskable interrupt or reset.

The non-maskable interrupt status is indicated in ICU.NMISR.BUSSST. For details, see section 12, Interrupt Controller Unit (ICU). The reset status is indicated in SYSTEM.RSTSR1.BUSSRF. For details, see section 5, Resets.

14.6 Security MPU

The MCU incorporates a security MPU and has four secure regions. The secure region can be protected from non-secure program accesses. In addition, the security MPU provides four secure regions that include the code flash, the SRAM, and two security functions.

Table 14.8 lists the specifications of the security MPU.

Table 14.8 Security MPU specifications

Specifications	Description
Secure region	Code flash, SRAM, two security functions
Protected regions	0000 0000h to FFFF FFFFh
Number of regions	Program Counter = 2 regions, Data Access = 4 regions
Addresses specification for individual regions	Setting the address where regions start and end
Enable/disable setting for memory protection in individual regions	Setting enabled or disabled for the associated region

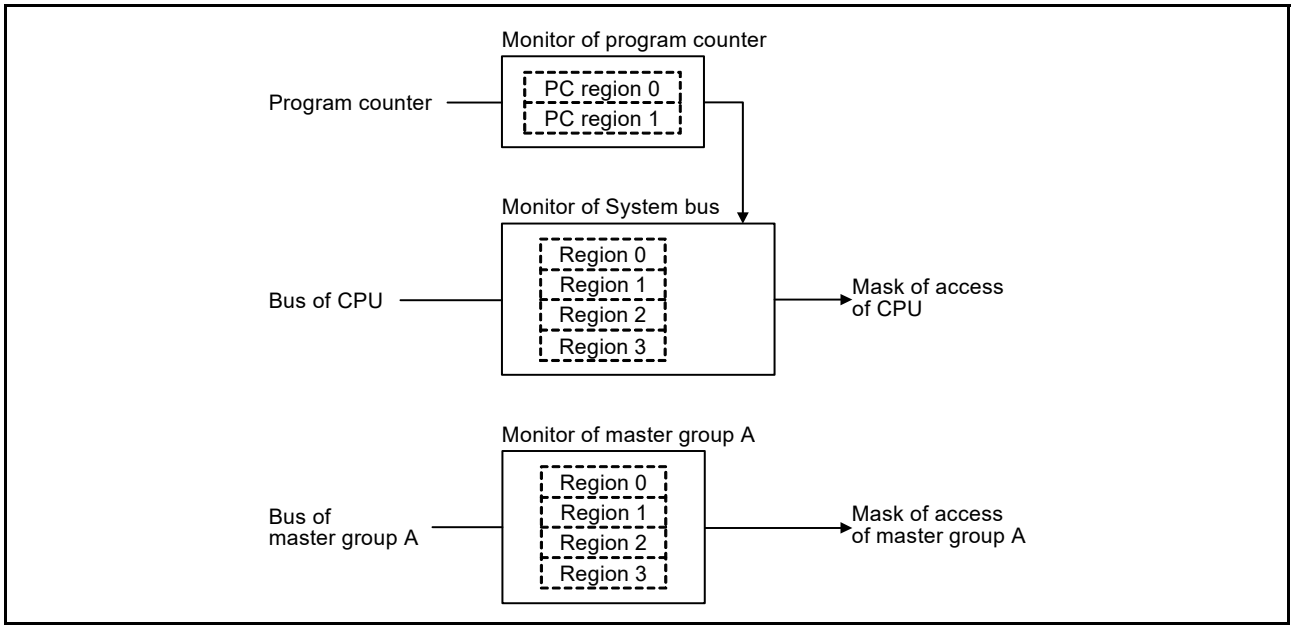


Figure 14.10 Security MPU block diagram

14.6.1 Register Descriptions (Option-Setting memory)

All security MPU registers are option-setting memory. Option-setting memory refers to a set of registers that are available for selecting the state of the microcontroller after a reset. The option-setting memory is allocated in the code flash.

14.6.1.1 Security MPU Program Counter Start Address Register n (SECMPUPCSn) (n = 0, 1)

Address(es): SECMPUPCS0 0000 0408h, SECMPUPCS1 0000 0410h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SECMPUPCS[31:16]															
Value after reset:	The value set by user															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUPCS[15:0]															
Value after reset:	The value set by user															

Bit	Symbol	Bit name	Description	R/W
b31 to b0	SECMPUPCS[31:0]	Region Start Address	Address where the region starts, for use in region determination. The lower 2 bits are read as 0. The write value should be 0. The value range is from 0000 0000h to 000F FFFCh or 1FF0 0000h to 200F FFFCh, not including the reserved areas.	R

The SECMPUPCSn and SECMPUPCEn registers specify the security fetch region for the code flash (0000 0000h to 000F FFFFh, not including the reserved areas) or SRAM (1FF0 0000h to 200F FFFFh, not including the reserved areas). The secure program is executed in the memory space defined by the SECMPUPCSn and SECMPUPCEn registers and can access the secure data specified in the SECMPUSm and SECMPUEm registers (m = 0 to 3).

14.6.1.2 Security MPU Program Counter End Address Register n (SECMPUPCEn) (n = 0, 1)

Address(es): SECMPUPCE0 0000 040Ch, SECMPUPCE1 0000 0414h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SECMPUPCE[31:16]															
Value after reset:	The value set by user															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUPCE[15:0]															
Value after reset:	The value set by user															

Bit	Symbol	Bit name	Description	R/W
b31 to b0	SECMPUPCE[31:0]	Region End Address	Address where the region ends, for use in region determination. The lower 2 bits are read as 1. When programming to the code flash, the write value should be 1. The value range is from 0000 0003h to 000F FFFFh or 1FF0 0003h to 200F FFFFh, not including the reserved areas.	R

14.6.1.3 Security MPU Region 0 Start Address Register (SECMPUS0)

Address(es): SECMPUS0 0000 0418h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	SECMPUS0[23:16]							
Value after reset:	0	0	0	0	0	0	0	0	The value set by user							

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUS0[15:0]															
Value after reset:	The value set by user															

Bit	Symbol	Bit name	Description	R/W
b23 to b0	SECMPUS0[23:0]	Region Start Address	Address where the region starts, for use in region determination. The lower 2 bits are read as 0. When programming to the code flash, the write value should be 0. The value range is from 0000 0000h to 000F FFFCh, not including the reserved areas.	R
b31 to b24	—	Reserved	These bits are read as 0. When programming to the code flash, the write value should be 0.	R

The SECMPUS0 and SECMPUE0 registers specify the secure program and the flash data (0000 0000h to 000F FFFFh, not including the reserved areas). The memory space defined in the SECMPUS0 and SECMPUE0 registers can only be accessed from the secure program set in the SECMPUPCSn and SECMPUPCEn registers.

Setting of the vector table area is prohibited.

14.6.1.4 Security MPU Region 0 End Address Register (SECMPUE0)

Address(es): SECMPUE0 0000 041Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	SECMPUE0[23:16]							
Value after reset:	0	0	0	0	0	0	0	0	The value set by user							

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUE0[15:0]															
Value after reset:	The value set by user															

Bit	Symbol	Bit name	Description	R/W
b23 to b0	SECMPUE0[23:0]	Region End Address	Address where the region ends, for use in region determination. The lower 2 bits are read as 1. When programming to the code flash, the write value should be 1. The value range is from 0000 0003h to 000F FFFFh, not including the reserved areas.	R
b31 to b24	—	Reserved	These bits are read as 0. When programming to the code flash, the write value should be 0.	R

14.6.1.5 Security MPU Region 1 Start Address Register (SECMPUS1)

Address(es): SECMPUS1 0000 0420h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SECMPUS1[31:16]															
Value after reset:	The value set by user															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUS1[15:0]															
Value after reset:	The value set by user															

Bit	Symbol	Bit name	Description	R/W
b31 to b0	SECMPUS1[31:0]	Region Start Address	Address where the region starts, for use in region determination. The lower 2 bits are read as 0. When programming to the code flash, the write value should be 0. The value range is from 1FF0 0000h to 200F FFFCh, not including the reserved areas.	R

The SECMPUS1 and SECMPUE1 registers specify the secure data of the SRAM (1FF0 0000h to 200F FFFFh, not including the reserved areas). The memory space defined in the SECMPUS1 and SECMPUE1 registers can only be accessed from the secure program set in the SECMPUPCSn and SECMPUPCEn registers.

Setting of the stack area and the vector table are prohibited.

14.6.1.6 Security MPU Region 1 End Address Register (SECMPUE1)

Address(es): SECMPUE1 0000 0424h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SECMPUE1[31:16]															
Value after reset:	The value set by user															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUE1[15:0]															
Value after reset:	The value set by user															

Bit	Symbol	Bit name	Description	R/W
b31 to b0	SECMPUE1[31:0]	Region End Address	Address where the region ends, for use in region determination. The lower 2 bits are read as 1. When programming to the code flash, the write value should be 1. The value range is from 1FF0 0003h to 200F FFFCh, not including the reserved areas.	R

14.6.1.7 Security MPU Region 2 Start Address Register (SECMPUS2)

Address(es): SECMPUS2 0000 0428h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SECMPUS2[31:16]															
Value after reset:	The value set by user															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUS2[15:0]															
Value after reset:	The value set by user															

Bit	Symbol	Bit name	Description	R/W
b31 to b0	SECMPUS2[31:0]	Region Start Address	Address where the region starts, for use in region determination. The lower 2 bits are read as 0. When programming to the code flash, the write value should be 0. The value range is from 400C 0000h to 400D FFFCh and 4010 0000h to 407F FFFCh.	R

The SECMPUS2 and SECMPUE2 registers specify the secure data of the security function (400C 0000h to 400D FFFFh and 4010 0000h to 407F FFFFh). The memory space defined in the SECMPUS2 and SECMPUE2 registers can only be accessed from the secure program set in the SECMPUPCSn and SECMPUPCEn registers.

14.6.1.8 Security MPU Region 2 End Address Register (SECMPUE2)

Address(es): SECMPUE2 0000 042Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SECMPUE2[31:16]															
Value after reset:	The value set by user															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUE2[15:0]															
Value after reset:	The value set by user															

Bit	Symbol	Bit name	Description	R/W
b31 to b0	SECMPUE2[31:0]	Region End Address	Address where the region ends, for use in region determination. The lower 2 bits are read as 1. When programming to the code flash, the write value should be 1. The value range is from 400C 0003h to 400D FFFFh and 4010 0003h to 407F FFFFh.	R

14.6.1.9 Security MPU Region 3 Start Address Register (SECMPUS3)

Address(es): SECMPUS3 0000 0430h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SECMPUS3[31:16]															
Value after reset:	The value set by user															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUS3[15:0]															
Value after reset:	The value set by user															

Bit	Symbol	Bit name	Description	R/W
b31 to b0	SECMPUS3[31:0]	Region Start Address	Address where the region starts, for use in region determination. The lower 2 bits are read as 0. When programming to the code flash, the write value should be 0. The value range is from 400C 0000h to 400D FFFCh and 4010 0000h to 407F FFFCh.	R

The SECMPUS3 and SECMPUE3 registers specify the secure data of the security function (400C 0000h to 400D FFFFh and 4010 0000h to 407F FFFFh). The memory space defined in the SECMPUS3 and SECMPUE3 registers can only be accessed from the secure program set in the SECMPUPCSn and SECMPUPCEn registers.

14.6.1.10 Security MPU Region 3 End Address Register (SECMPUE3)

Address(es): SECMPUE3 0000 0434h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SECMPUE3[31:16]															
Value after reset:	The value set by user															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUE3[15:0]															
Value after reset:	The value set by user															

Bit	Symbol	Bit name	Description	R/W
b31 to b0	SECMPUE3[31:0]	Region End Address	Address determines where the region ends. The lower 2 bits are read as 1. When programming to the code flash, the write value should be 1. The value range is from 400C 0003h to 400D FFFFh and 4010 0003h to 407F FFFFh.	R

14.6.1.11 Security MPU Access Control Register (SECMPUAC)

Address(es): SECMPUAC 0000 0438h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	DISPC 1	DISPC 0	—	—	—	—	DIS3	DIS2	DIS1	DIS0
Value after reset:	1	1	1	1	1	1	The value set by user		1	1	1	1	The value set by user			

Bit	Symbol	Bit name	Description	R/W
b0	DIS0	Region 0 Disable	0: Security MPU Region 0 enabled 1: Security MPU Region 0 disabled.	R
b1	DIS1	Region 1 Disable	0: Security MPU Region 1 enabled 1: Security MPU Region 1 disabled.	R
b2	DIS2	Region 2 Disable	0: Security MPU Region 2 enabled 1: Security MPU Region 2 disabled.	R
b3	DIS3	Region 3 Disable	0: Security MPU Region 3 enabled 1: Security MPU Region 3 disabled.	R
b7 to b4	—	Reserved	These bits are read as 1. When programming to the code flash, the write value should be 1.	R
b8	DISPC0	PC Region 0 Disable	0: Security MPU PC Region 0 enabled 1: Security MPU PC Region 0 disabled.	R
b9	DISPC1	PC Region 1 Disable	0: Security MPU PC Region 1 enabled 1: Security MPU PC Region 1 disabled.	R
b15 to b10	—	Reserved	These bits are read as 1. When programming to the code flash, the write value should be 1.	R

Note: When flash memory is erased, security MPU is disabled.
Note: To enable or disable the security MPU, see section 14.6.2, Memory Protection.

DIS0 bit (Region 0 Disable)

The DIS0 bit enables or disables the security MPU region 0. If the security MPU region 0 is enabled, the code flash region within the limits set by SECMPUS0 and SECMPUE0 is the secure data.

DIS1 bit (Region 1 Disable)

The DIS1 bit enables or disables the security MPU region 1. If the security MPU region 1 is enabled, the SRAM region within the limits set by SECMPUS1 and SECMPUE1 is the secure data.

DIS2 bit (Region 2 Disable)

The DIS2 bit enables or disables the security MPU region 2. If the security MPU region 2 is enabled, the security function region within the limits set by SECMPUS2 and SECMPUE2 is the secure data.

DIS3 bit (Region 3 Disable)

The DIS3 bit enables or disables the security MPU region 3. If the security MPU region 3 is enabled, the security function region within the limits set by SECMPUS3 and SECMPUE3 is the secure data.

DISPC0 bit (PC Region 0 Disable)

The DISPC0 bit enables or disables the security MPU PC region 0. If the security MPU PC region 0 is enabled, the code flash or SRAM region within the limits set by SECMPUPCS0 and SECMPUPCE0 is the secure program.

DISPC1 bit (PC Region 1 Disable)

The DISPC1 bit enables or disables the security MPU PC region 1. If the security MPU PC region 1 is enabled, the code flash or SRAM region within the limits set by SECMPUPCS1 and SECMPUPCE1 is the secure program.

14.6.2 Memory Protection

The security MPU protects the secure memories (code flash, SRAM, and security function) from being accessed by programs other than a secure program. If access to the protected region is detected, the access becomes invalid.

When the security MPU is enabled, DISPC0 or DISPC1 in the Security MPU Access Control Register (SECMPUAC) and DIS0, DIS1, DIS2, or DIS3 in the Security MPU Access Control Register (SECMPUAC) must be set to 0.

When the security MPU is disabled, all bits in DISPC0, DISPC1, DIS0, DIS1, DIS2, and DIS3 in the Security MPU Access Control Register (SECMPUAC) must be set to 1. Other settings in the Security MPU Access Control Register (SECMPUAC) are prohibited.

The security MPU provides access protection in the following conditions:

- Secure data is accessed from a non-secure program
- Secure data is accessed from other than the CPU (DTC)
- Secure data is accessed from a debugger.

Secure data is accessible only from a secure program.

Note: Secure program: Code flash or SRAM region within the limits set by SECMPUPCS0 and SECMPUPCE0
Code flash or SRAM region within the limits set by SECMPUPCS1 and SECMPUPCE1
Non-secure program: All regions without the secure program.
Secure data: - Code flash region within the limits set by SECMPUS0 and SECMPUE0.
- SRAM region within the limits set by SECMPUS1 and SECMPUE1.
- Security function region within the limits set by SECMPUS2 and SECMPUE2.
- Security function region within the limits set by SECMPUS3 and SECMPUE3.

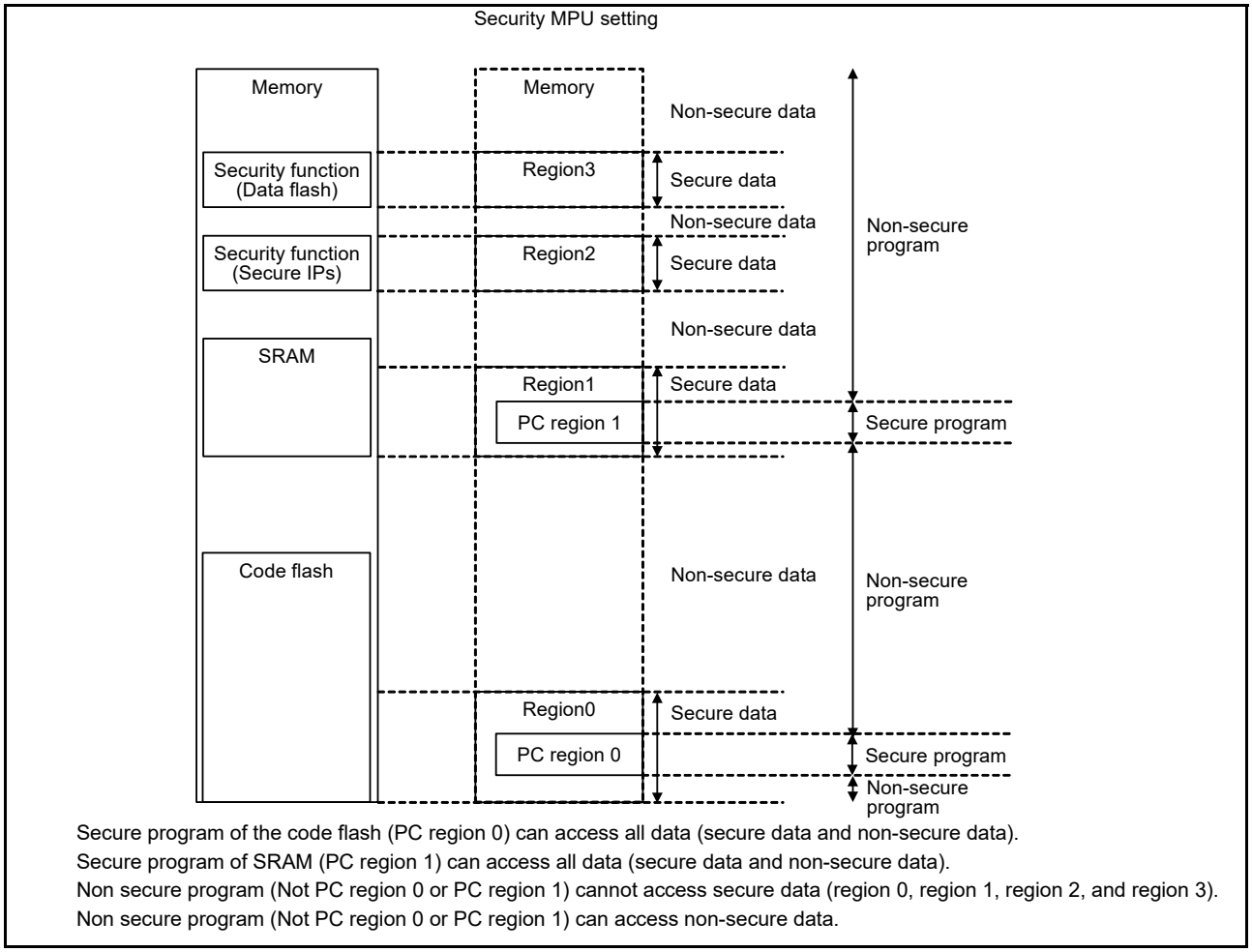


Figure 14.11 Use case of security MPU

14.6.3 Usage Notes

When debugging a secure program, disable the security MPU.

14.7 References

- *ARM®v6-M Architecture Reference Manual* (ARM DDI 0419C)
- *ARM® Cortex®-M0+ Processor Technical Reference Manual* (ARM DDI 0484C)
- *ARM® Cortex®-M0+ Devices Generic User Guide* (ARM DUI 0662B).

15. Data Transfer Controller (DTC)

15.1 Overview

The Data Transfer Controller (DTC) performs data transfers when activated by an interrupt request. Table 15.1 lists the DTC specifications, and Figure 15.1 shows a block diagram.

Table 15.1 DTC specifications

Parameter	Description
Transfer modes	• Normal transfer mode A single activation leads to a single data transfer. • Repeat transfer mode A single activation leads to a single data transfer. The transfer address returns to the start address after the number of data transfers reaches the specified repeat size. The maximum number of repeat transfers is 256 and the maximum data transfer size is 256 × 32 bits (1024 bytes). • Block transfer mode A single activation leads to a transfer of a single block. The maximum block size is 256 × 32 bits = 1024 bytes.
Transfer channel	• Channel transfer can be associated with the interrupt source (transferred by a DTC activation request from the ICU) • Multiple data units can be transferred on a single activation source (chain transfer) • Chain transfers selectable to either executed when the counter is 0, or always execute.
Transfer space	• 4 GB area from 0000 0000h to FFFF FFFF, not including the reserved areas
Data transfer units	• Single data unit: 1 byte (8 bits), 1 halfword (16 bits), 1 word (32 bits) • Single block size: 1 to 256 data units.
CPU interrupt source	• An interrupt request can be generated to the CPU on a DTC activation interrupt • An interrupt request can be generated to the CPU after a single data transfer • An interrupt request can be generated to the CPU after data transfer of a specified volume.
Event link function	An event link request is generated after one data transfer (for block, after one block transfer)
Read skip	Read of transfer information can be skipped
Write-back skip	When the transfer source or destination address is specified as fixed, a write-back of transfer information can be skipped
Module-stop function	Module-stop state can be set to reduce power consumption

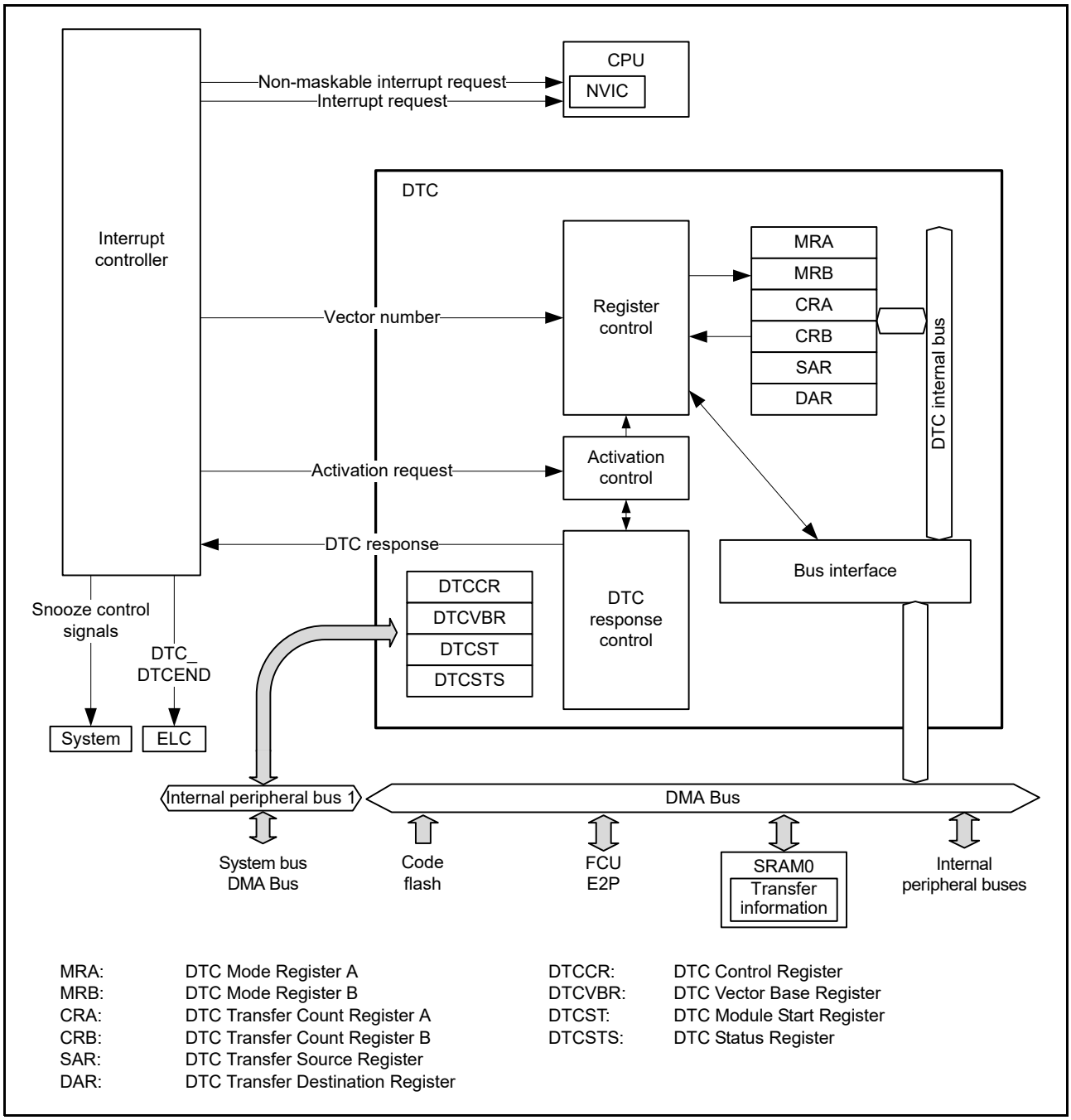


Figure 15.1 DTC block diagram

See Overview in section 12, Interrupt Controller Unit (ICU) for the connections between the DTC and NVIC in the CPU.

15.2 Register Descriptions

The MRA, MRB, SAR, DAR, CRA, and CRB are all DTC internal registers that cannot be directly accessed from the CPU. Values to be set in these DTC internal registers are placed in the SRAM area as transfer information. When an activation request is generated, the DTC reads the transfer information from the SRAM area and sets it in its internal registers. After the data transfer ends, the internal register contents are written back to the SRAM area as transfer information.

15.2.1 DTC Mode Register A (MRA)

Address(es): (inaccessible directly from the CPU. See section 15.3.1)

	b7	b6	b5	b4	b3	b2	b1	b0
	MD[1:0]		SZ[1:0]		SM[1:0]		—	—
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as undefined. The write value should be 0.	—
b3, b2	SM[1:0]	Transfer Source Address Addressing Mode	b3 b2 0 0: Address in the SAR register is fixed (write-back to SAR is skipped.) 0 1: Address in the SAR register is fixed (write-back to SAR is skipped.) 1 0: SAR value is incremented after data transfer (+1 when SZ[1:0] bits = 00b, +2 when SZ[1:0] bits = 01b, +4 when SZ[1:0] bits = 10b) 1 1: SAR value is decremented after data transfer (-1 when SZ[1:0] bits = 00b, -2 when SZ[1:0] bits = 01b, -4 when SZ[1:0] bits = 10b)	—
b5, b4	SZ[1:0]	DTC Data Transfer Size	b5 b4 0 0: Byte (8-bit) transfer 0 1: Halfword (16-bit) transfer 1 0: Word (32-bit) transfer 1 1: Setting prohibited.	—
b7, b6	MD[1:0]	DTC Transfer Mode Select	b7 b6 0 0: Normal transfer mode 0 1: Repeat transfer mode 1 0: Block transfer mode 1 1: Setting prohibited.	—

The MRA register cannot be accessed directly from the CPU. The CPU can access SRAM area (transfer information (n) start address + 03h) and DTC transfer it automatically from and to the MRA register. See section 15.3.1, Allocating Transfer Information and DTC Vector Table.

15.2.2 DTC Mode Register B (MRB)

Address(es): (inaccessible directly from the CPU. See section 15.3.1)

	b7	b6	b5	b4	b3	b2	b1	b0
	CHNE	CHNS	DISEL	DTS	DM[1:0]		—	—
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as undefined. The write value should be 0.	—

Bit	Symbol	Bit name	Description	R/W
b3, b2	DM[1:0]	Transfer Destination Address Addressing Mode	b3 b2 0 0: Address in the DAR register is fixed (Write-back to DAR is skipped) 0 1: Address in the DAR register is fixed (Write-back to DAR is skipped) 1 0: DAR value is incremented after data transfer (+1 when MRA.SZ[1:0] bits = 00b, +2 when SZ[1:0] bits = 01b, +4 when SZ[1:0] bits = 10b) 1 1: DAR value is decremented after data transfer (-1 when MRA.SZ[1:0] bits = 00b, -2 when SZ[1:0] bits = 01b, -4 when SZ[1:0] bits = 10b).	—
b4	DTS	DTC Transfer Mode Select	0: Transfer destination is the repeat or block area 1: Transfer source is the repeat or block area.	—
b5	DISEL	DTC Interrupt Select	0: An interrupt request to the CPU is generated when specified data transfer is complete 1: An interrupt request to the CPU is generated each time DTC data transfer is performed.	—
b6	CHNS	DTC Chain Transfer Select	0: Chain transfer is continuous 1: Chain transfer occurs only when the transfer counter changes from 1 to 0 or 1 to CRAH.	—
b7	CHNE	DTC Chain Transfer Enable	0: Chain transfer is disabled 1: Chain transfer is enabled.	—

The MRB register cannot be accessed directly from the CPU. The CPU can access the SRAM area (transfer information (n) start address + 02h) and DTC transfer it automatically from and to the MRB register. See section 15.3.1, Allocating Transfer Information and DTC Vector Table.

DTS bit (DTC Transfer Mode Select)

The DTS bit specifies whether the transfer source or destination is the repeat or block area in repeat or block transfer mode.

CHNS bit (DTC Chain Transfer Select)

The CHNS bit selects the chain transfer condition. When CHNE is 0, the CHNS setting is ignored. For details on the conditions for chain transfer, see Table 15.3, Chain transfer conditions.

When the next transfer is chain transfer, completion of the specified number of transfers is not determined, the activation source flag is not cleared, and an interrupt request to the CPU is not generated.

CHNE bit (DTC Chain Transfer Enable)

The CHNE bit enables chain transfer. The chain transfer condition is selected by the CHNS bit. For details on chain transfer, see section 15.4.6, Chain Transfer.

15.2.3 DTC Transfer Source Register (SAR)

Address(es): (inaccessible directly from the CPU. See section 15.3.1)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

The SAR sets the transfer source start address and cannot be accessed directly from the CPU. The CPU can access the SRAM area (transfer information (n) start address + 04h) and DTC transfer it automatically from and to the SAR register.

See section 15.3.1, Allocating Transfer Information and DTC Vector Table.

Note: Misalignment is prohibited for DTC transfers.

15.2.4 DTC Transfer Destination Register (DAR)

Address(es): (inaccessible directly from the CPU. See section 15.3.1)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

The DAR sets the transfer destination start address and cannot be accessed directly from the CPU. The CPU can access the SRAM area (transfer information (n) start address + 08h) and DTC transfer it automatically from and to the DAR register. See section 15.3.1, Allocating Transfer Information and DTC Vector Table. Misalignment is prohibited for DTC transfers. Bit 0 must be 0 when MRA.SZ[1:0] = 01b, and bit [1] and bit [0] must be 0 when MRA.SZ[1:0] = 10b.

Note: Misalignment is prohibited for DTC transfers.

15.2.5 DTC Transfer Count Register A (CRA)

Address(es): (inaccessible directly from the CPU. See section 15.3.1)

- Normal transfer mode

CRA

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

- Repeat transfer mode/block transfer mode

CRAH CRAL

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Symbol	Register name	Description	R/W
CRAL	Transfer Counter A Lower Register	Set transfer count	—
CRAH	Transfer Counter A Upper Register		—

Note: The function depends on the transfer mode.
Note: Set CRAH and CRAL to the same value in repeat transfer mode and block transfer mode.

CRA cannot be accessed directly from the CPU. The CPU can access the SRAM area (transfer information (n) start address + 0Eh) and DTC transfer it automatically from and to the CRA register. See section 15.3.1, Allocating Transfer Information and DTC Vector Table.

(1) Normal Transfer mode (MRA.MD[1:0] bits = 00b)

The CRA functions as a 16-bit transfer counter in normal transfer mode. The transfer count is 1, 65535, and 65536 when

the set value is 0001h, FFFFh, and 0000h, respectively. The CRA value is decremented (-1) at each data transfer.

(2) Repeat Transfer mode (MRA.MD[1:0] bits = 01b)

In repeat transfer mode, the CRAH register holds the transfer count and the CRAL register functions as an 8-bit transfer counter. The transfer count is 1, 255, and 256 when the set value is 01h, FFh, and 00h, respectively. The CRAL value is decremented (-1) at each data transfer. When it reaches 00h, the CRAH value is transferred to CRAL.

(3) Block Transfer mode (MRA.MD[1:0] bits = 10b)

In block transfer mode, the CRAH register holds the block size and the CRAL register functions as an 8-bit block size counter. The transfer count is 1, 255, and 256 when the set value is 01h, FFh, and 00h, respectively. The CRAL value is decremented (-1) at each data transfer. When it reaches 00h, the CRAH value is transferred to CRAL.

15.2.6 DTC Transfer Count Register B (CRB)

Address(es): (inaccessible directly from the CPU. See section 15.3.1)

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

The CRB sets the block transfer count for block transfer mode. The transfer count is 1, 65535, and 65536 when the set value is 0001h, FFFFh, and 0000h, respectively. The CRB value is decremented (-1) when the final data of a single block size is transferred. When normal transfer mode or repeat transfer mode is selected, this register is not used and the set value is ignored.

The CRB cannot be accessed directly from the CPU. The CPU can access the SRAM area (transfer information (n) start address + 0Ch) and DTC transfer it automatically from and to the CRB register. See section 15.3.1, Allocating Transfer Information and DTC Vector Table.

15.2.7 DTC Control Register (DTCCR)

Address(es): DTC.DTCCR 4000 5400h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	RRS	—	—	—	—
Value after reset:	0	0	0	0	1	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b4	RRS	DTC Transfer Information Read Skip Enable	0: Transfer information read is not skipped 1: Transfer information read is skipped when vector numbers match.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RRS bit (DTC Transfer Information Read Skip Enable)

The RRS bit enables skipping of transfer information reads when vector numbers match.

The DTC vector number is compared with the vector number in the previous activation process. When these vector numbers match and the RRS bit is set to 1, DTC data transfer is performed without reading the transfer information. However, when the previous transfer is chain transfer, the transfer information is read regardless of the value of the RRS bit.

When the transfer counter (CRA register) becomes 0 during the previous normal transfer and when the transfer counter (CRB register) becomes 0 during the previous block transfer, the transfer information is read regardless of the RRS bit

value.

15.2.8 DTC Vector Base Register (DTCVBR)

Address(es): DTC.DTCVBR 4000 5404h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Bit name	Description	R/W
b31 to b0	DTC Vector Base Address	Set the DTC Vector Base Address (lower 10 bits should be 0)	R/W

The DTCVBR sets the base address for calculating the DTC vector table address, which can be set in the range of 0000 0000h to FFFF FFFFh (4 GB) in 1-KB units.

15.2.9 DTC Module Start Register (DTCST)

Address(es): DTC.DTCST 4000 540Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DTCST
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DTCST	DTC Module Start	0: DTC module stop 1: DTC module start.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DTCST bit (DTC Module Start)

Set the DTCST bit to 1 to enable the DTC to accept transfer requests. When this bit is set to 0, transfer requests are no longer accepted. If this bit is set to 0 during a data transfer, the accepted transfer request is active until the processing completes.

The DTCST bit must be set to 0 before making a transition to the module-stop state or Software Standby mode without Snooze mode transition.

For details on these transitions, see section 15.10, Module-Stop Function, and section 10, Low Power Modes.

15.2.10 DTC Status Register (DTCSTS)

Address(es): DTC.DTCSTS 4000 540Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ACT	—	—	—	—	—	—	—	VECN[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	VECN[7:0]	DTC-Activating Vector Number Monitoring	These bits indicate the vector number for the activation source when a DTC transfer is in progress. The value is only valid if a DTC transfer is in progress (the value of the ACT flag is 1).	R
b14 to b8	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b15	ACT	DTC Active Flag	0: DTC transfer operation is not in progress 1: DTC transfer operation is in progress.	R

VECN[7:0] bits (DTC-Activating Vector Number Monitoring)

While transfer by the DTC is in progress, these bits indicate the vector number associated with the activation source for the transfer. The value read from the VECN[7:0] bits is valid if the value of the ACT flag is 1, indicating a DTC transfer in progress, and invalid if the value of the ACT flag is 0, indicating no DTC transfer is in progress.

ACT flag (DTC Active Flag)

This flag indicates the state of the DTC transfer operation.

[Setting condition]

- When the DTC is activated by a transfer request.

[Clearing condition]

- When transfer by the DTC, in response to a transfer request, is complete.

15.3 Activation Sources

The DTC is activated by an interrupt request. Setting the ICU.IELSRn.DTCE bit of the ICU to 1 enables activation of the DTC by the associated interrupt. The number of selector output *n* by ICU.IELSR is defined as the interrupt vector number, where n = 0 to 31. For an enabled interrupt, the specific DTC interrupt source associated with each interrupt vector number *n* is selected by ICU.IELSRn.IELS[7:0], where n = 0 to 31.

For the setup of ICU.IELSRn.IELS[7:0] (n = 0 to 31), see Table 12.4, Event table in section 12, Interrupt Controller Unit (ICU). For activation by software, see section 16.2.2, Event Link Software Event Generation Register n (ELSEGRn) where n = 0, 1.

The interrupt vector number is equivalent to the DTC vector table number. After the DTC accepts an activation request, it does not accept another activation request until transfer for that single request completes, regardless of the priority of the requests. When multiple activation requests are generated during a DTC transfer, a request with the highest priority on completion of the transfer is accepted. When multiple activation requests are generated while the DTC module start bit (DTCST.DTCST) is 0, the DTC accepts the request with the highest priority at the time when the bit is subsequently set to 1. The small interrupt vector number has high priority.

The DTC performs the following operations at the start of a single data transfer, or for a chain transfer, after the last of the consecutive transfers:

- On completion of a specified round of data transfer, the ICU.IELSRn.DTCE bit is set to 0, and an interrupt request is sent to the CPU
- If the MRB.DISEL bit is 1, an interrupt request is sent to the CPU on completion of a data transfer
- For other transfers, the ICU.IELSRn.IR bit of the activation source is set to 0 at the start of the data transfer.

15.3.1 Allocating Transfer Information and DTC Vector Table

The DTC reads the start address of the transfer information associated with each activation source from the vector table and reads the transfer information starting at that address.

The vector table must be located so that the lower 10 bits of the base address (start address) are 0. Use the DTC Vector Base Register (DTCVBR) to set the base address of the DTC vector table. Transfer information is allocated in the SRAM area. In the SRAM area, the start address of the transfer information *n* with vector number *n* must be 4n added to the base address in the vector table.

Figure 15.2 shows the relationship between the DTC vector table and transfer information. Figure 15.3 shows the allocation of transfer information in the SRAM area.

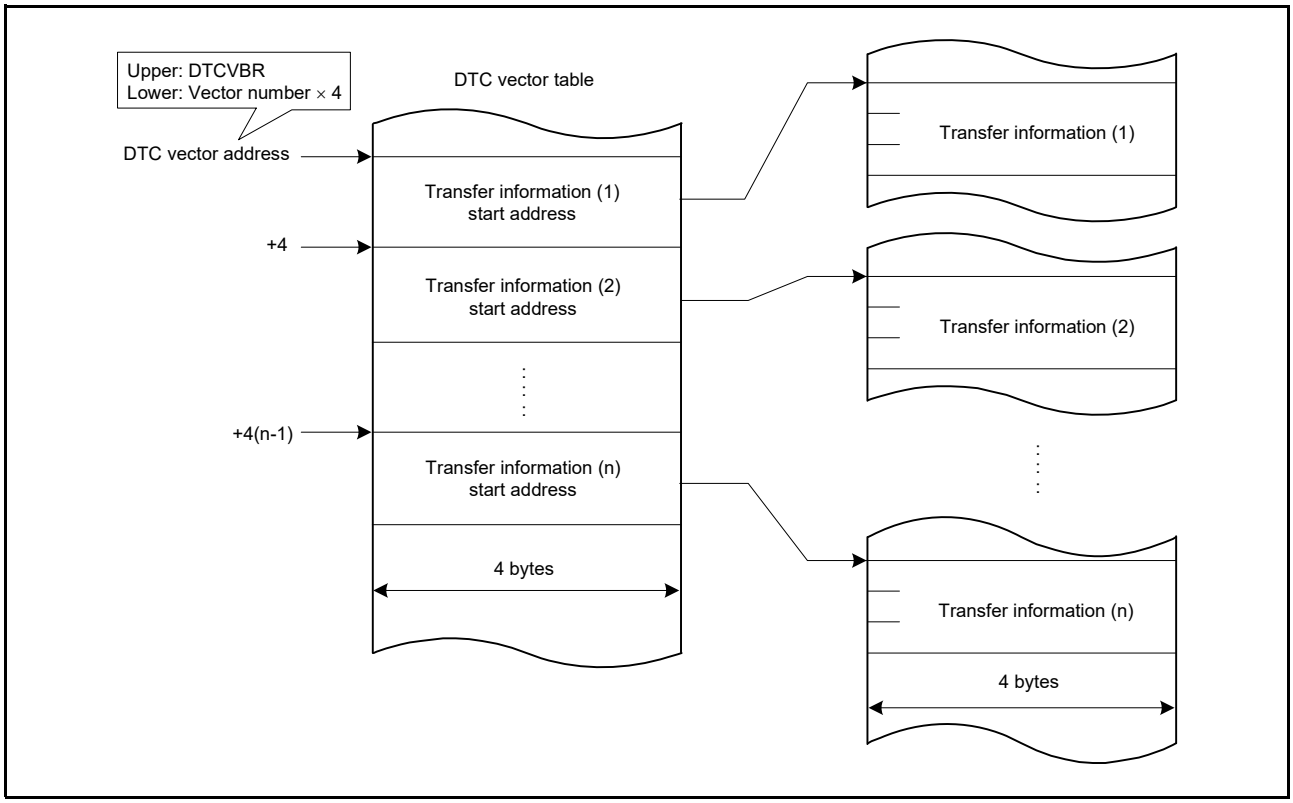


Figure 15.2 DTC vector table and transfer information

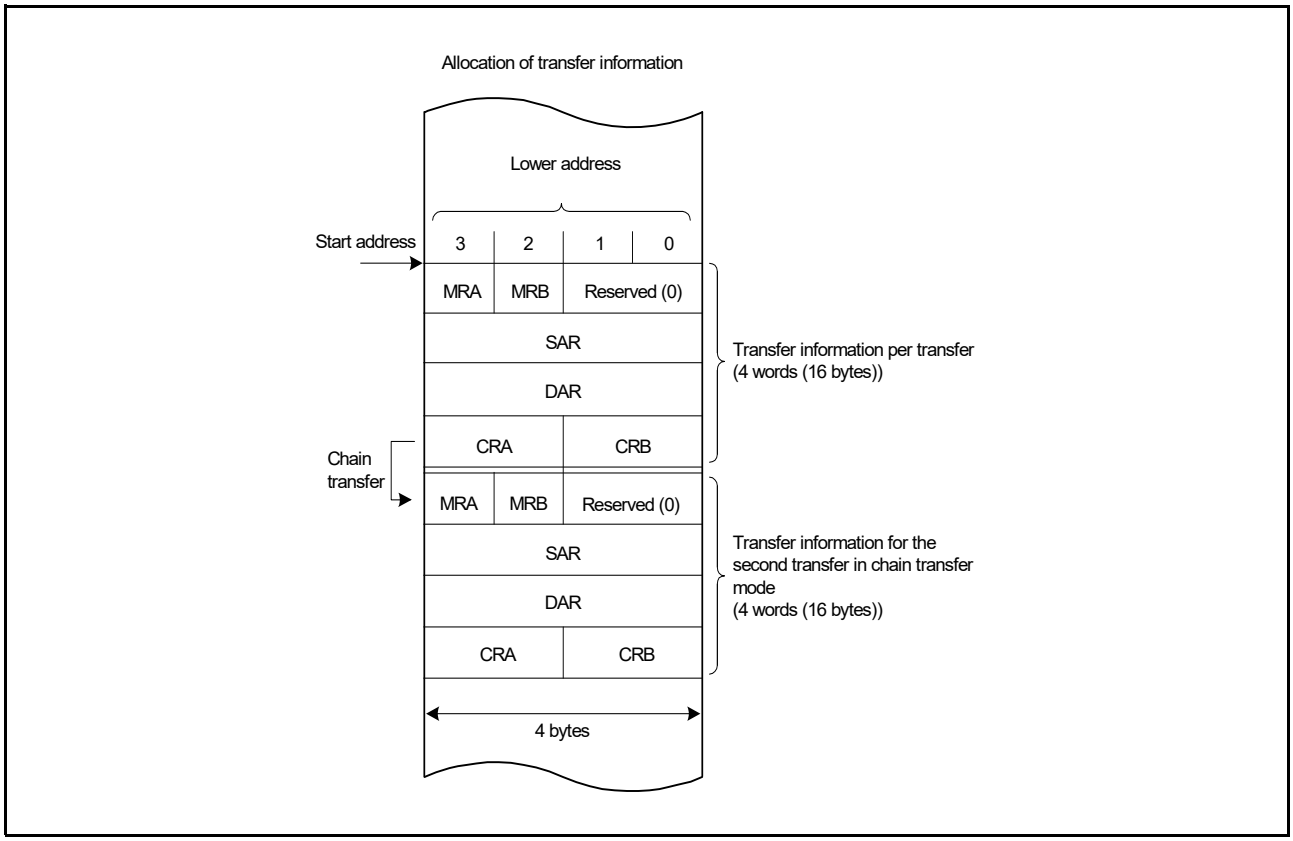


Figure 15.3 Allocation of transfer information in the SRAM area

15.4 Operation

The DTC transfers data according to the transfer information. Storage of the transfer information in the SRAM area is required before a DTC operation. When the DTC is activated, it reads the DTC vector associated with the vector number. The DTC reads the transfer information from the transfer information store address referenced by the DTC vector then transfers the data. After the data transfer, the DTC writes back the transfer information. Storing the transfer information in the SRAM area allows data transfer of any number of channels.

There are three transfer modes:

- Normal transfer mode
- Repeat transfer mode
- Block transfer mode.

The DTC specifies a transfer source address in the SAR register and a transfer destination address in the DAR register. The values of these registers are incremented, decremented, or address-fixed independently after the data transfer.

Table 15.2 lists the DTC transfer modes.

Table 15.2 DTC transfer modes

Transfer mode	Data size transferred on single transfer request	Increment or decrement of memory address	Settable transfer count
Normal transfer mode	1 byte (8 bit), 1 halfword (16 bit), 1 word (32 bit)	Incremented/decremented by 1, 2, or 4 or address fixed	1 to 65536
Repeat transfer mode*1	1 byte (8 bit), 1 halfword (16 bit), 1 word (32 bit)	Incremented/decremented by 1, 2, or 4 or address fixed	1 to 256*3
Block transfer mode*2	Block size specified in CRAH (1 to 256 bytes, 1 to 256 halfwords (2 to 512 bytes), 1 to 256 words (4 to 1024 bytes))	Incremented/decremented by 1, 2, or 4 or address fixed	1 to 65536

Note 1. Set the transfer source or transfer destination as the repeat area.
Note 2. Set the transfer source or transfer destination as the block area.
Note 3. After a data transfer of the specified count, the initial state is restored and operation restarts.

Setting the MRB.CHNE bit to 1 allows multiple transfers or chain transfer on a single activation source. It also enables a chain transfer when the specified data transfer is complete.

Figure 15.4 shows the operation flowchart of the DTC. Table 15.3 lists the chain transfer conditions. The combination of control information for the second and subsequent transfers are omitted in this table.

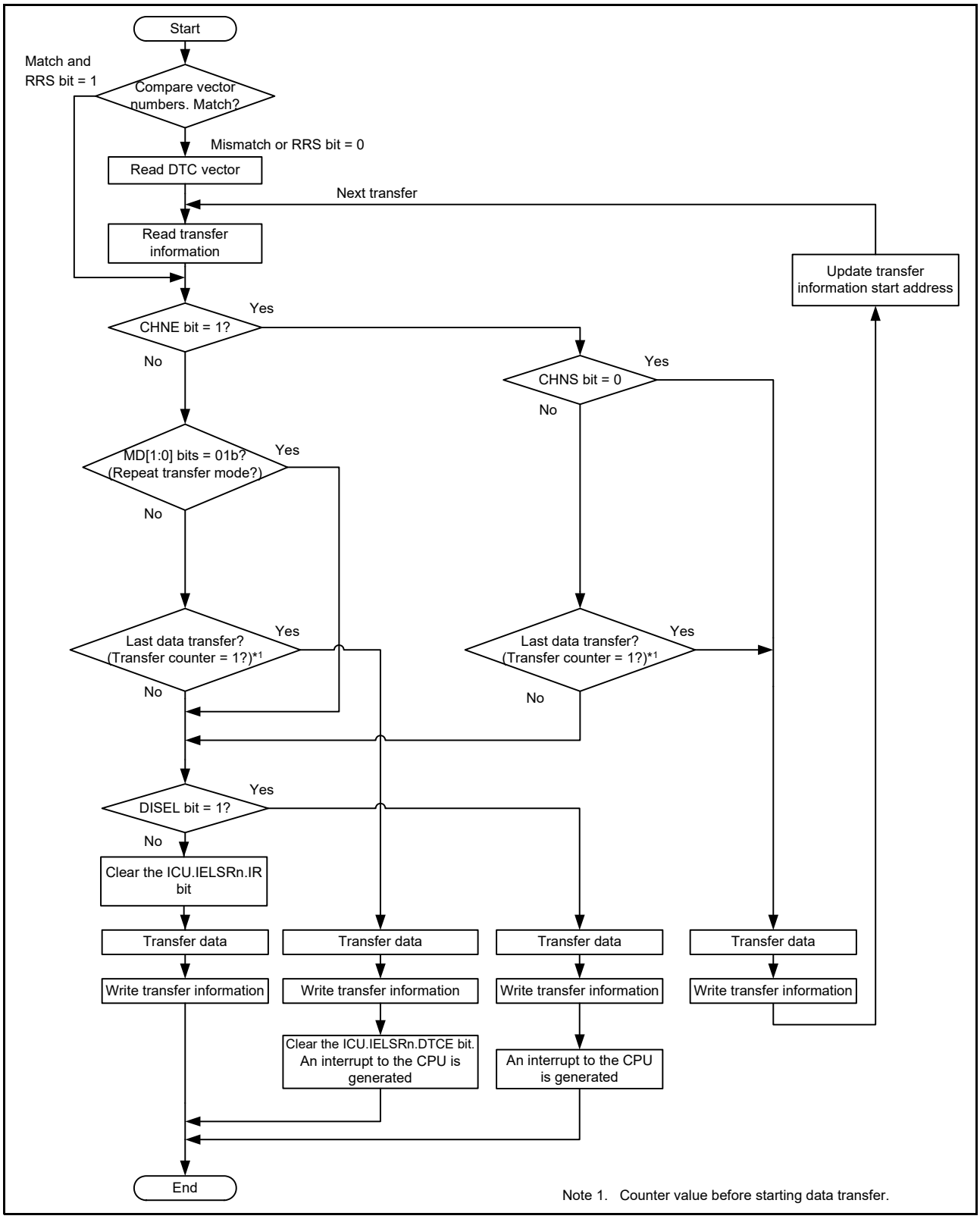


Figure 15.4 DTC operation flow

Table 15.3 Chain transfer conditions

First transfer				Second transfer*3				
CHNE bit	CHNS bit	DISEL bit	Transfer counter*1,*2	CHNE bit	CHNS bit	DISEL bit	Transfer counter*1,*2	DTC transfer
0	—	0	Other than (1 → 0)	—	—	—	—	Ends after the first transfer
0	—	0	(1 → 0)	—	—	—	—	Ends after the first transfer with an interrupt request to the CPU
0	—	1	—	—	—	—	—	
1	0	—	—	0	—	0	Other than (1 → 0)	Ends after the second transfer
				0	—	0	(1 → 0)	Ends after the second transfer with an interrupt request to the CPU
				0	—	1	—	
1	1	0	Other than (1 → *)	—	—	—	—	Ends after the first transfer
1	1	—	(1 → *)	0	—	0	Other than (1 → 0)	Ends after the second transfer
				0	—	0	(1 → 0)	Ends after the second transfer with an interrupt request to the CPU
				0	—	1	—	
1	1	1	Other than (1 → *)	—	—	—	—	Ends after the first transfer with an interrupt request to the CPU

Note 1. The transfer counters used depend on the transfer modes as follows:
Normal transfer mode — CRA register
Repeat transfer mode — CRAL register
Block transfer mode — CRB register

Note 2. On completion of a data transfer, the counters operate as follows:
1 → 0 in normal and block transfer modes
1 → CRAH in repeat transfer mode
(1 → *) in the table indicates both of these two operations, depending on the mode.

Note 3. Chain transfer can be selected for the second or subsequent transfers. The conditions for the combination of the second transfer and CHNE bit = 1 is omitted.

15.4.1 Transfer Information Read Skip Function

Reading of vector addresses and transfer information can be skipped through the setting in the DTCCR.RRS bit. When a DTC activation request is generated, the current DTC vector number is compared with the DTC vector number in the previous activation process. When these vector numbers match and the RRS bit is set to 1, DTC data transfer is performed without reading the vector address and transfer information. However, when the previous transfer is a chain transfer, the vector address and transfer information are read. Additionally, when the transfer counter (CRA register) becomes 0 during the previous normal transfer, and when the transfer counter (CRB register) becomes 0 during the previous block transfer, transfer information is read regardless of the value of the RRS bit. Figure 15.12 shows an example of a transfer information read skip.

To update the vector table and transfer information, set the RRS bit to 0, update the vector table and transfer information, then set the RRS bit to 1. The retained vector number is discarded by setting the RRS bit to 0. The updated DTC vector table and transfer information are read in the next activation process.

15.4.2 Transfer Information Write-Back Skip Function

When the MRA.SM[1:0] bits or the MRB.DM[1:0] bits are set to address fixed, a part of the transfer information is not written back. Table 15.4 lists the transfer information write-back skip conditions and associated registers. The CRA and CRB registers are written back, and the write-back of the MRA and MRB registers is skipped.

Table 15.4 Transfer information write-back skip conditions and associated registers

MRA.SM[1:0] bits		MRB.DM[1:0] bits		SAR register	DAR register
b3	b2	b3	b2		
0	0	0	0	Skip	Skip
0	0	0	1		
0	1	0	0		
0	1	0	1		
0	0	1	0	Skip	Write-back
0	0	1	1		
0	1	1	0		
0	1	1	1		
1	0	0	0	Write-back	Skip
1	0	0	1		
1	1	0	0		
1	1	0	1		
1	0	1	0	Write-back	Write-back
1	0	1	1		
1	1	1	0		
1	1	1	1		

15.4.3 Normal Transfer Mode

This mode allows a 1-byte (8 bit), 1-halfword (16 bit), 1-word (32 bit) data transfer on a single activation source. The transfer count can be set to 1 to 65536. Transfer source addresses and transfer destination addresses can be independently set to increment, decrement, or fixed. This mode enables an interrupt request to the CPU to be generated at the end of a specified-count transfer.

Table 15.5 lists register functions in normal transfer mode, and Figure 15.5 shows the memory map of normal transfer mode.

Table 15.5 Register functions in normal transfer mode

Register	Description	Value written back by writing transfer information
SAR	Transfer source address	Increment, decrement, or fixed*1
DAR	Transfer destination address	Increment, decrement, fixed*1
CRA	Transfer counter A	CRA - 1
CRB	Transfer counter B	Not updated

Note 1. Write-back operation is skipped in address-fixed mode.

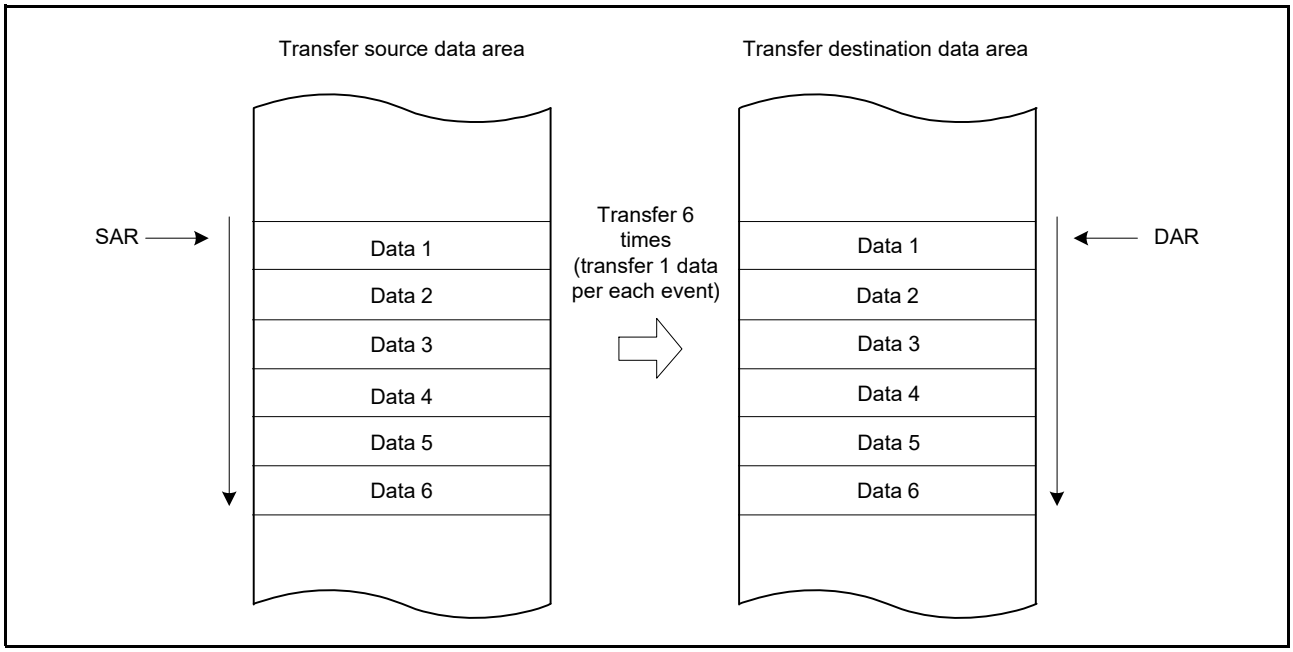


Figure 15.5 Memory map of normal transfer mode (MRA.SM[1:0] = 10b, MRB.DM[1:0] = 10b, CRA=0006h)

15.4.4 Repeat Transfer Mode

This mode allows a 1-byte, 1-halfword, or 1-word data transfer on a single activation source. Transfer source or transfer destination for the repeat area must be specified in the MRB.DTS bit. The transfer count can be set from 1 to 256. When the specified-count transfer is complete, the initial value of the address register specified in the repeat area is restored, the initial value of the transfer counter is restored and transfer is repeated. The other address register is incremented or decremented continuously or remains unchanged.

When the transfer counter CRAL decrements to 00h in repeat transfer mode, the CRAL value is updated to the value set in the CRAH register. As a result, the transfer counter does not become 00h, which disables interrupt requests to the CPU when the MRB.DISEL bit is set to 0. An interrupt request to the CPU is generated when the specified data transfer completes.

Table 15.6 lists the register functions in repeat transfer mode, and Figure 15.6 shows the memory map of repeat transfer mode.

Table 15.6 Register functions in repeat transfer mode

Register	Description	Value written back by writing transfer information	
		When CRAL is not 1	When CRAL is 1
SAR	Transfer source address	Increment, decrement, fixed*1	(When the MRB.DTS bit is 0) Increment, decrement, or fixed*1 (When the MRB.DTS bit is 1) SAR register initial value
DAR	Transfer destination address	Increment, decrement, or fixed*1	(When the MRB.DTS bit is 0) DAR register initial value (When the MRB.DTS bit is 1) Increment/decrement/fixed*1
CRAH	Retains transfer counter	CRAH	CRAH
CRAL	Transfer counter A	CRAL - 1	CRAH
CRB	Transfer counter B	Not updated	Not updated

Note 1. Write-back is skipped in address-fixed mode.

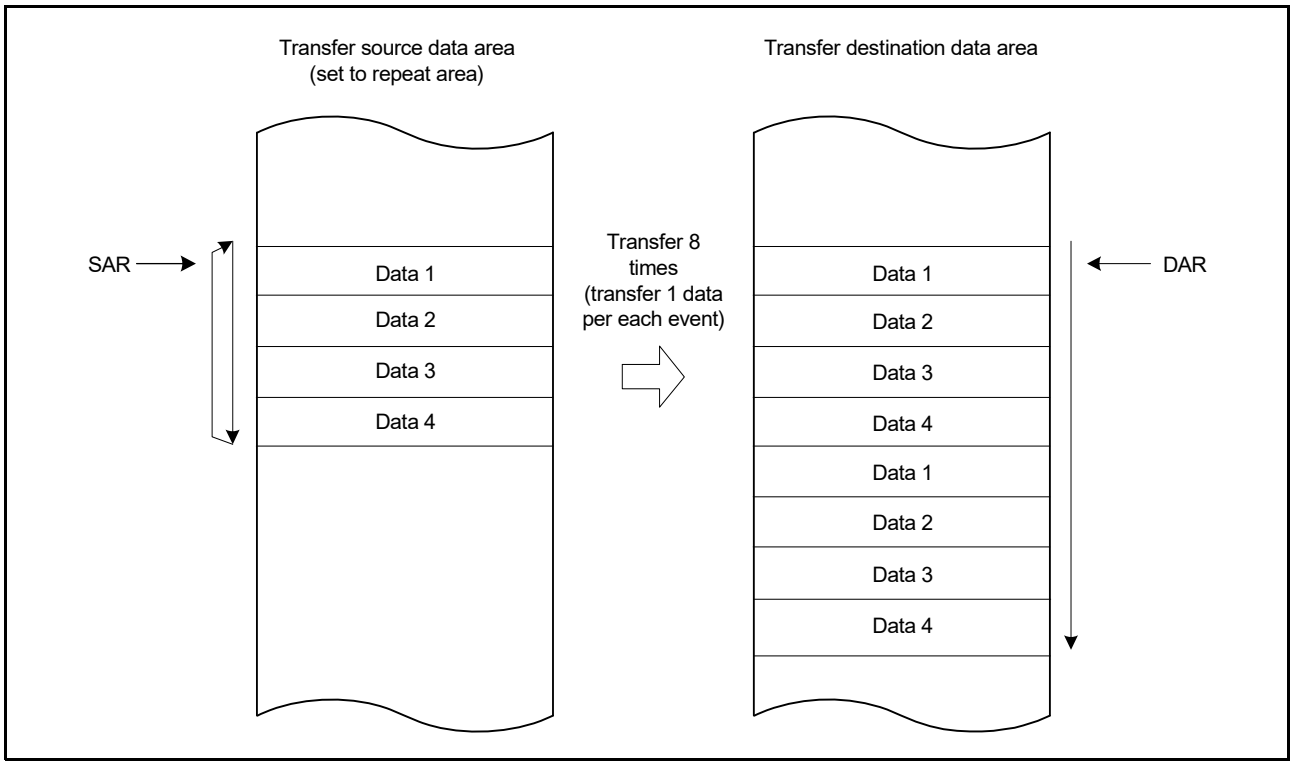


Figure 15.6 Memory map of repeat transfer mode when the transfer source is a repeat area (MRA.SM[1:0] = 10b, MRB.DM[1:0] =10b, CRAH=04h)

15.4.5 Block Transfer Mode

This mode allows single-block data transfer on a single activation source. Transfer source or transfer destination for the block area must be specified in the MRB.DTS bit. The block size can be set from 1 to 256 bytes, 1 to 256 halfwords (2 to 512 bytes), or 1 to 256 words (4 to 1024 bytes). When transfer of the specified block is complete, the initial values of the block size counter CRAL and the address register (the SAR register when the MRB.DTS bit = 1 or the DAR register when the DTS bit = 0) specified in the block area are restored. The other address register is incremented or decremented continuously or remains unchanged.

The transfer count (block count) can be set from 1 to 65536. This mode enables an interrupt request to the CPU to be generated at the end of the specified-count block transfer.

Table 15.7 lists the register functions in block transfer mode, and Figure 15.7 shows a memory map for block transfer mode.

Table 15.7 Register functions in block transfer mode

Register	Description	Value written back by writing transfer information
SAR	Transfer source address	• When MRB.DTS bit is 0 Increment, decrement, or fixed*1 • When MRB.DTS bit is 1 SAR register initial value
DAR	Transfer destination address	• When MRB.DTS bit is 0 DAR register initial value • When MRB.DTS bit is 1 Increment, decrement, or fixed*1
CRAH	Retains block size	CRAH
CRAL	Block size counter	CRAH
CRB	Block transfer counter	CRB - 1

Note 1. Write-back is skipped in address-fixed mode.

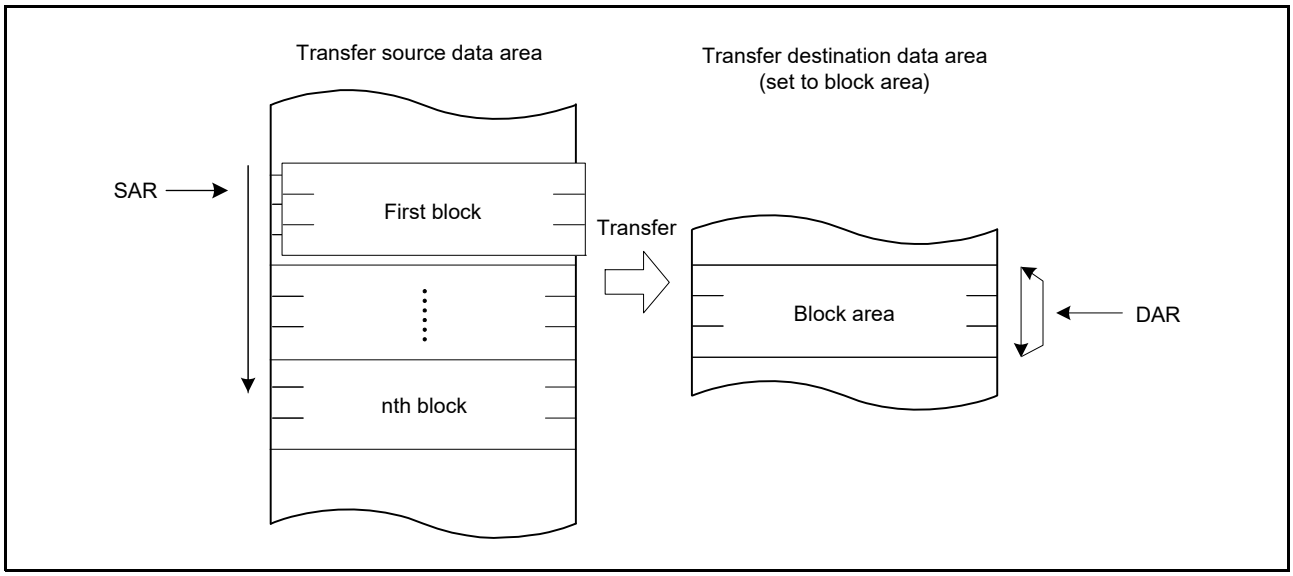


Figure 15.7 Memory map of block transfer mode

15.4.6 Chain Transfer

Setting the MRB.CHNE bit to 1 allows chain transfer to be performed continuously on a single activation source. If the MRB.CHNE is set to 1 and CHNS to 0, an interrupt request to the CPU is not generated on completion of the specified number of rounds of transfer or by setting the MRB.DISEL bit to 1. An interrupt request is sent to the CPU each time DTC data transfer is performed. Data transfer has no effect on the ICU.IELSRn.IR bit of the activation source.

The SAR, DAR, CRA, CRB, MRA, and MRB registers can be set independently of each other to define the data transfer. Figure 15.8 shows a chain transfer operation.

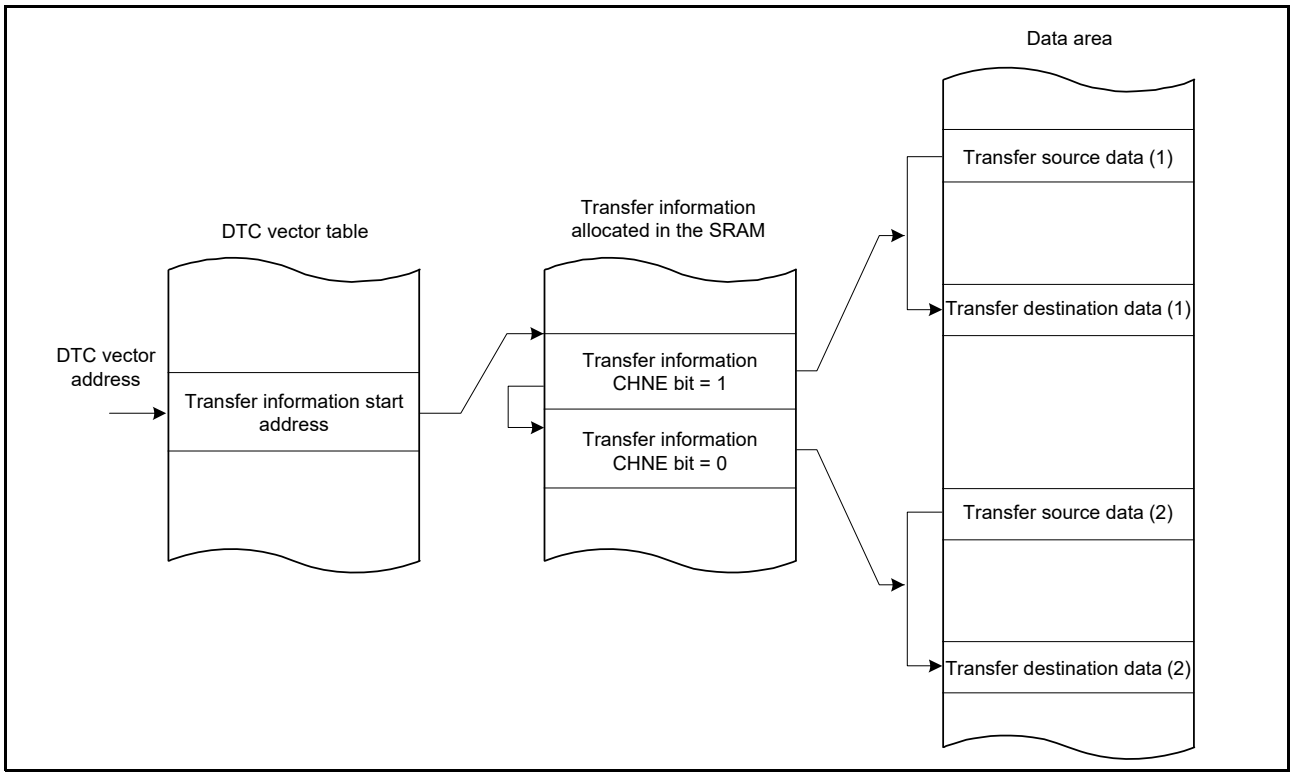


Figure 15.8 Chain transfer operation

Writing 1 to the MRB.CHNE and CHNS bits enables chain transfer to be performed only after completion of the

specified data transfer. In repeat transfer mode, chain transfer is performed after completion of the specified data transfer. For details on chain transfer conditions, see Table 15.3, Chain transfer conditions.

15.4.7 Operation Timing

Figure 15.9 to Figure 15.12 are timing diagrams that show the minimum number of execution cycles.

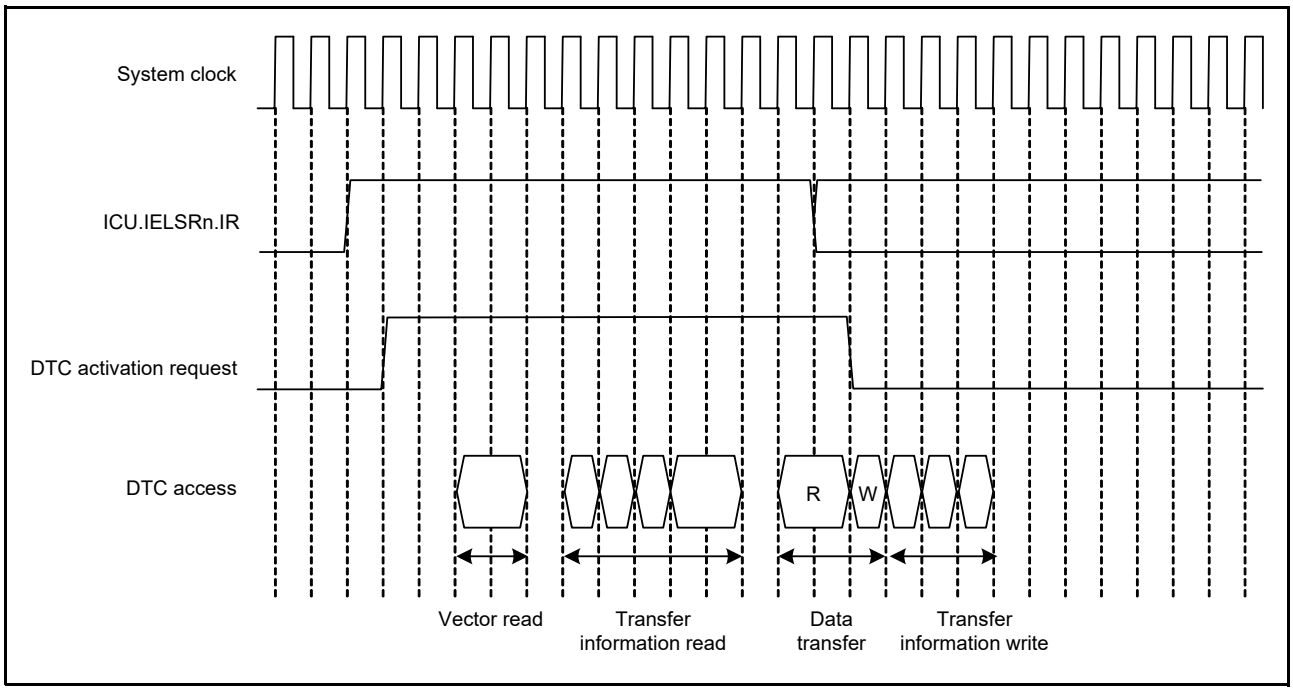


Figure 15.9 Example (1) of DTC operation timing in normal transfer and repeat transfer modes

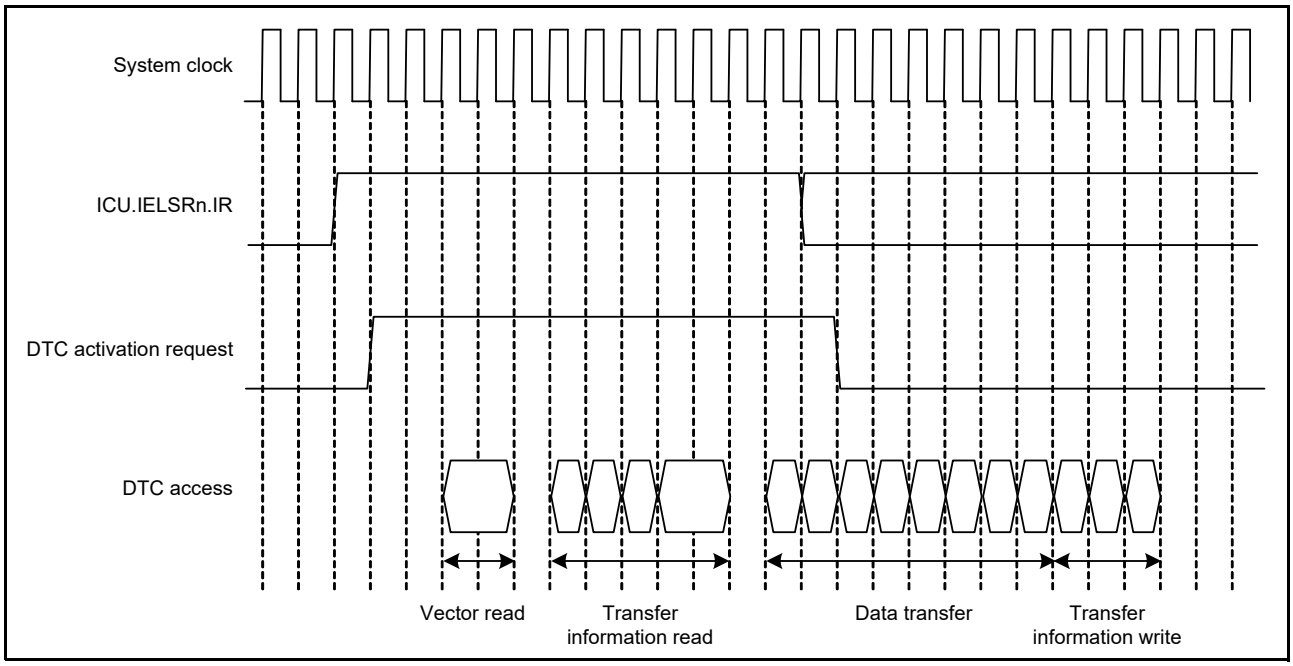


Figure 15.10 Example (2) of DTC operation timing in block transfer mode when the block size = 4

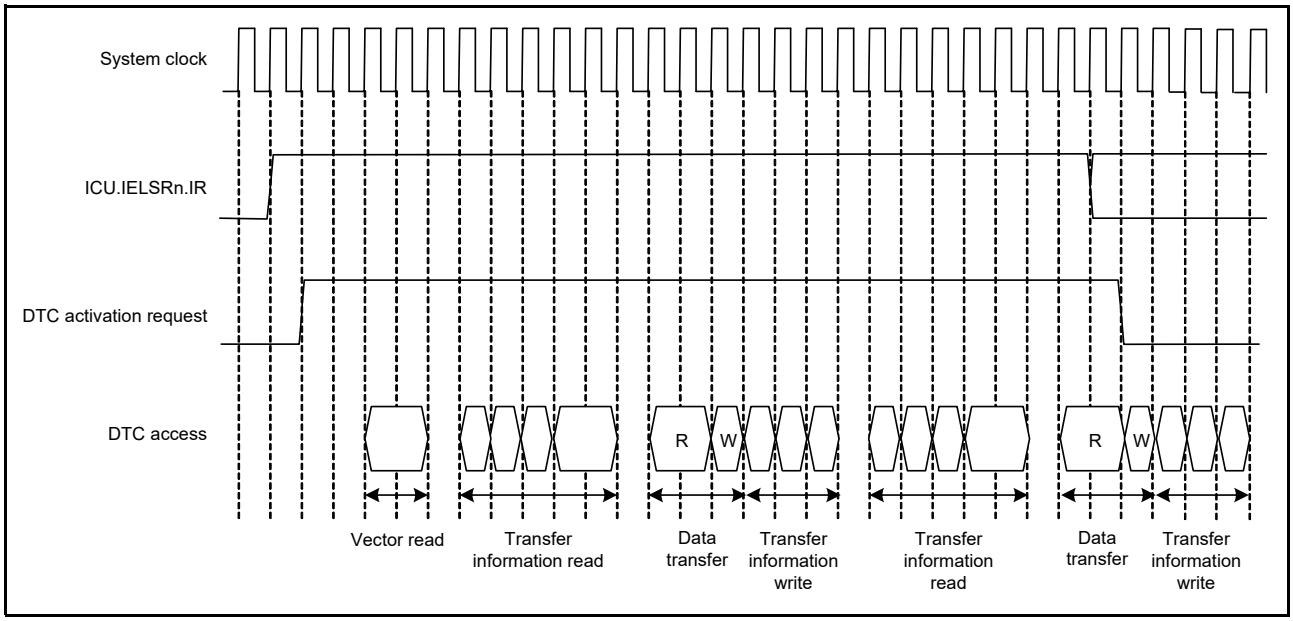
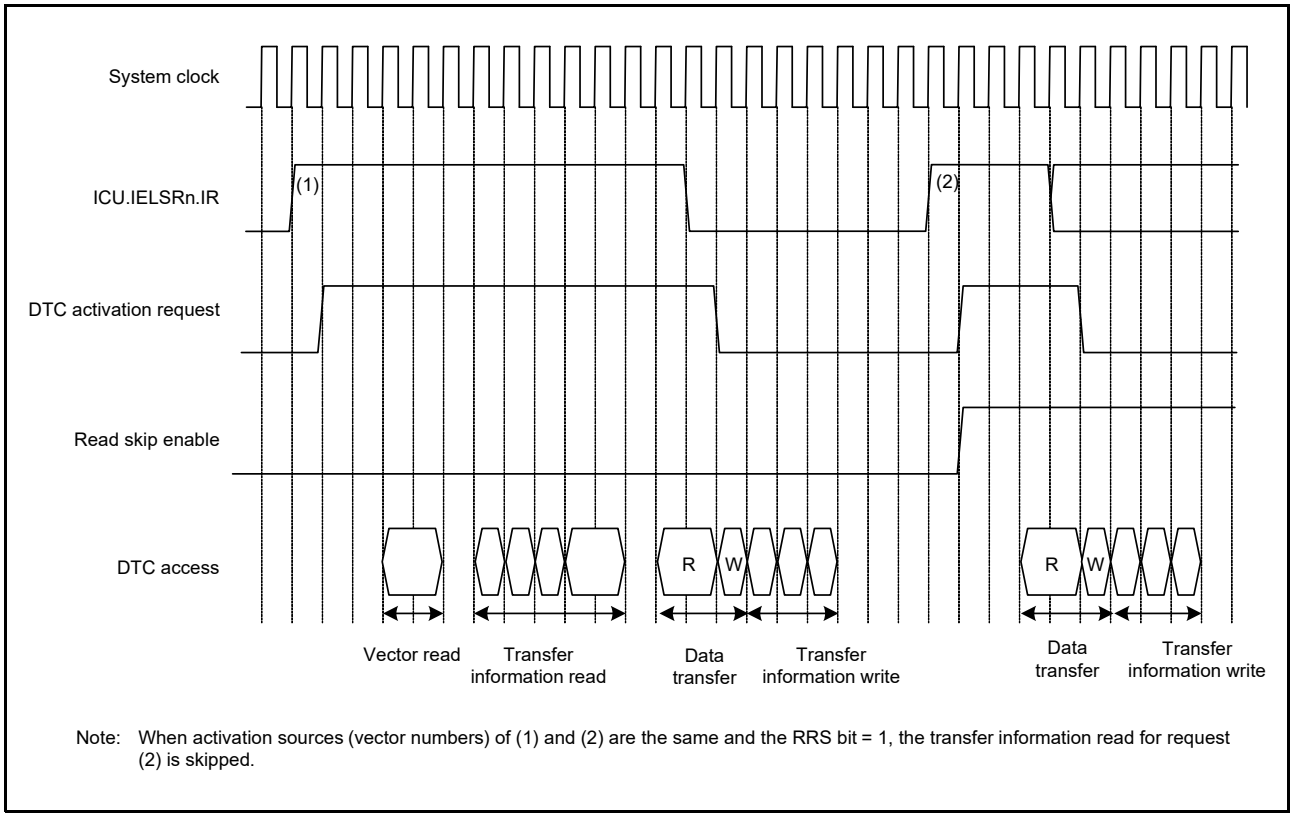


Figure 15.11 Example (3) of DTC operation timing for chain transfer



Note: When activation sources (vector numbers) of (1) and (2) are the same and the RRS bit = 1, the transfer information read for request (2) is skipped.

Figure 15.12 Example of operation when a transfer information read skip is executed with the vector, transfer information, and transfer destination data on the SRAM, and the transfer source data on the peripheral module

15.4.8 Execution Cycles of DTC

Table 15.8 lists the execution cycles of single data transfer of the DTC. For the order of the execution states, see section 15.4.7, Operation Timing.

Table 15.8 Execution cycles of DTC

Transfer mode	Vector read		Transfer information read		Transfer information write			Data transfer		Internal operation	
								Read	Write		
Normal	Cv + 1	0*1	4 x Ci + 1	0*1	3 x Ci + 1*2	2 x Ci + 1*3	Ci*4	Cr + 1	Cw + 1	2	0*1
Repeat								Cr + 1	Cw + 1		
Block								P x Cr	P x Cw		

Note 1. When transfer information read is skipped.
Note 2. When neither SAR nor DAR is set to address-fixed mode.
Note 3. When SAR or DAR is set to address-fixed mode.
Note 4. When SAR and DAR are set to address-fixed mode.
Note 5. When the block size is 2 or more. If the block size is 1, the cycle number for normal transfer applies.

P: Block size (initial settings of CRAH and CRAL)
Cv: Cycles for access to vector transfer information storage destination
Ci: Cycles for access to transfer information storage destination address
Cr: Cycles for access to data read destination
Cw: Cycles for access to data write destination
The unit is system clocks (ICLK) for + 1 in the Vector read, Transfer information read, and Data transfer read columns and 2 in the Internal operation column.
Cv, Ci, Cr, and Cw vary depending on the corresponding access destination. For the number of cycles for respective access destinations, see section 41, SRAM and section 42, Flash Memory.
The frequency ratio of the system clock and peripheral clock is also taken into consideration.
The DTC response time is the time from when the DTC activation source is detected until DTC transfer starts.
Table 15.8 does not include the time until DTC data transfer starts after the DTC activation source becomes active.

15.4.9 DTC Bus Mastership Release Timing

The DTC does not release the bus mastership during transfer information read. Before the transfer information is read or written, the bus is arbitrated according to the priority determined by the bus master arbitrator. For bus arbitration, see section 13, Buses.

15.5 DTC Setting Procedure

Before using the DTC, set the DTC Vector Base Register (DTCVBR). Figure 15.13 shows the procedure to set the DTC.

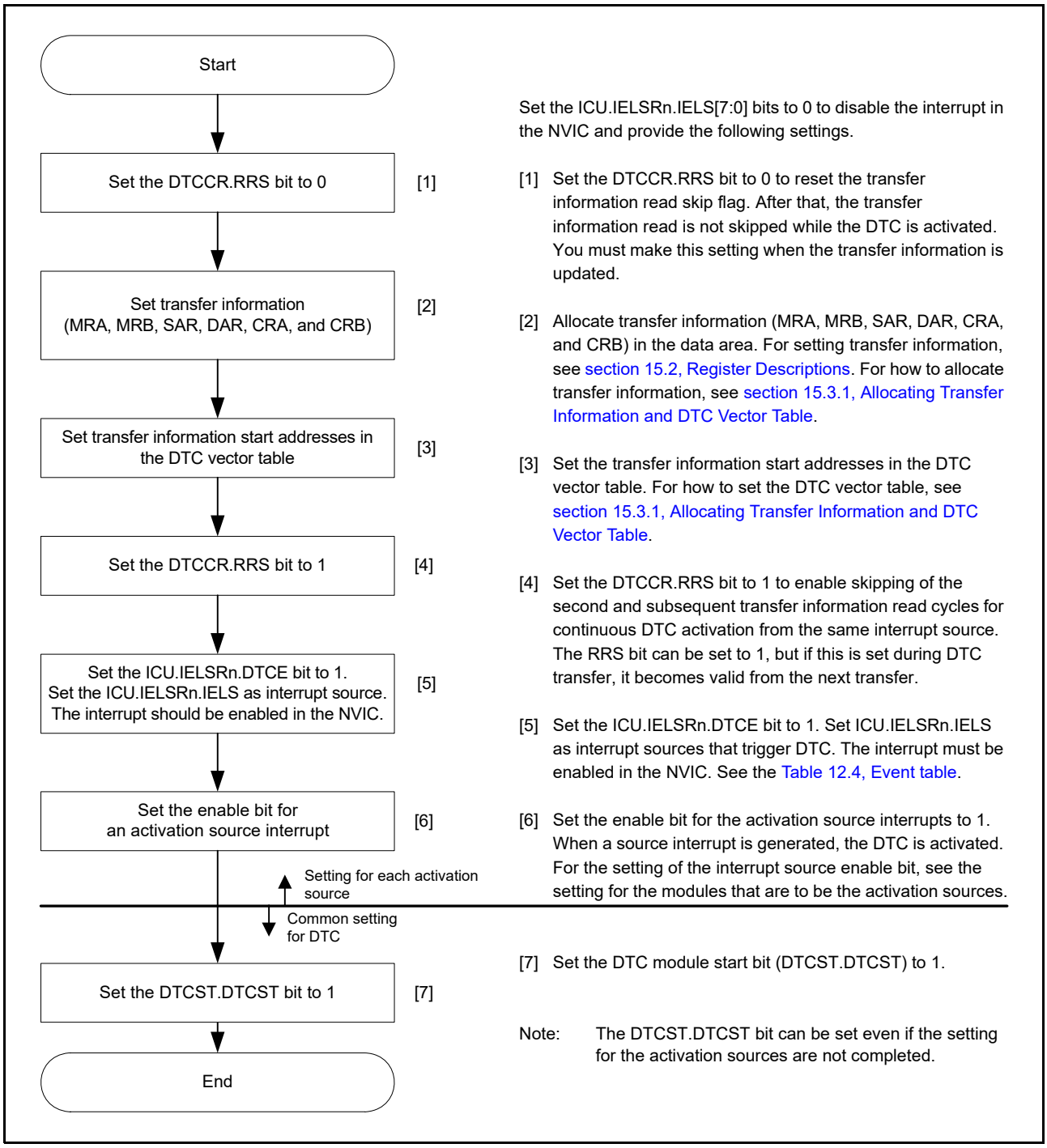


Figure 15.13 DTC setting procedure

15.6 Examples of DTC Usage

15.6.1 Normal Transfer

This section provides an example of DTC usage and its application in the reception of 128 bytes of data from an SCI.

(1) Transfer information setting

In the MRA register, select a fixed source address (MRA.SM[1:0] bits = 00b), normal transfer mode (MRA.MD[1:0] bits = 00b), and byte-sized transfer (MRA.SZ[1:0] bits = 00b). In the MRB register, specify incrementation of the destination address (MRB.DM[1:0] bits = 10b) and single data transfer by a single interrupt (MRB.CHNE bit = 0 and MRB.DISEL bit = 0). The MRB.DTS bit can be set to any value. Set the RDR register address of the SCI in the SAR register, the start

address of the SRAM area for data storage in the DAR register, and 128 (0080h) in the CRA register. The CRB register can be set to any value.

(2) DTC vector table setting

The start address of the transfer information for the RXI interrupt is set in the vector table for the DTC.

(3) ICU setting and DTC module activation

Set the ICU.IELSRn.DTCE bit to 1 and set ICU.IELSRn.IELS as the SCI interrupt. The interrupt must be enabled in the NVIC. Set the DTCST.DTCST bit to 1.

(4) SCI setting

Enable the RXI interrupt by setting the SCR.RIE bit in the SCI to 1. If a reception error occurs during the SCI receive operation, reception stops. To manage this, use settings that allow the CPU to accept receive error interrupts.

(5) DTC transfer

Every time a reception of 1 byte by the SCI is complete, an RXI interrupt is generated to activate the DTC. The DTC transfers the received byte from the RDR of the SCI to SRAM, after which the DAR register is incremented and the CRA register is decremented.

(6) Interrupt handling

After 128 rounds of data transfer are complete and the value in the CRA register becomes 0, an RXI interrupt request is generated for the CPU. Complete the process in the handling routine for this interrupt.

15.6.2 Chain transfer

This section provides an example of chain transfer by the DTC and describes its use in the output of pulses by the General PWM Timer (GPT). You can use chain transfer to transfer PWM timer compare data and change the period of the PWM timer for the GPT.

For the first of the chain transfers, normal transfer mode is specified for transfer to the GPTm.GTCCRC register (m = 320, 16H1 to 16H3, 164 to 166). For the second transfer, normal transfer mode is specified for transfer to the GPTm.GTCCRE registers. For the third transfer of the chained transfer, Normal Transfer mode for transfer to the GPTm.GTPBR registers is specified. This is because clearing of the activation source and generation of an interrupt on completion of the specified number of transfers are restricted to the third of the chain transfers, that is, transfers while MRB.CHNE bit = 0.

The following example shows how to use the counter overflow interrupt with the GPT320.GTPR register as an activating source for the DTC.

(1) First transfer information setting

Set up transfer to the GPT320.GTCCRC registers:

1. In the MRA register, select incrementation of the source address (MRA.SM[1:0] bits = 10b).
2. Set the transfer to normal transfer mode (MRA.MD[1:0] bits = 00b) and word-sized transfer (MRA.SZ[1:0] bits = 10b).
3. In the MRB register, select the destination address as fixed (MRB.DM[1:0] bits = 00b) and set up chain transfer (MRB.CHNE bit = 1 and MRB.CHNS bit = 0).
4. Set the SAR to the first address of the data table.
5. Set the DAR register to the address of the GPT320.GTCCRC register.
6. Set the CRAH and CRAL registers to the size of the data table. The CRB register can be set to any value.

(2) Second transfer information setting

Set up for transfer to the GPT320.GTCCRE registers.

1. In the MRA register, select incrementation of the source address (MRA.SM[1:0] bits = 10b).
2. Set the transfer to normal transfer mode (MRA.MD[1:0] bits = 00b) and word-sized transfer (MRA.SZ[1:0] bits =

10b).

3. In the MRB register, select the destination address as fixed (MRB.DM[1:0] bits = 00b) and set up chain transfer (MRB.CHNE bit = 1, MRB.CHNS bit = 0).
4. Set the SAR register to the first address of the data table.
5. Set the DAR register to the address of the GPT320.GTCCRE register.
6. Set the CRAH and CRAL registers to the size of the data table. The CRB register can be set to any value.

(3) Third transfer information set

Set up transfer to the GPT320.GTPBR registers.

1. In the MRA register, select incrementation of the source address (MRA.SM[1:0] bits = 10b).
2. Set the transfer to normal transfer mode (MRA.MD[1:0] bits = 00b) and word-sized transfer (MRA.SZ[1:0] bits = 10b)
3. In the MRB register, select the destination address as fixed (MRB.DM[1:0] bits = 00b) and set up single data transfer per interrupt (MRB.CHNE bit = 0, MRB.DISEL bit = 0). The MRB.DTS bit can be set to any value.
4. Set the SAR register to the first address of the data table.
5. Set the DAR register to the address of the GPT320.GTPBR registers.
6. Set the CRA register to the size of the data table. The CRB register can be set to any value.

(4) Transfer information assignment

Place the transfer information for use in the transfer to the GPT320.GTPBR immediately after the transfer control information for use in the GPT320.GTCCRC and GPT320.GTCCRE registers.

(5) DTC vector table

In the DTC vector table, set the address where the transfer control information for use in transfer to the GPT320.GTCCRC and GPT320.GTCCRE registers starts.

(6) ICU setting and DTC module activation

1. Set the ICU.IELSRn.DTCE bit associated with the GPT320 counter overflow interrupt.
2. Set the ICU.IELSRn.IELS[7:0] bits to 79 (4Fh) for the GPT320 counter overflow.
3. Set the DTCST.DTCST bit to 1.

(7) GPT setting

1. Set the GPT320.GTIOR register so that the GTCCRA and GTCCRB registers operate as output compare registers.
2. Set the default PWM timer compare values in the GPT320.GTCCRA and GPT320.GTCCRB registers and the next PWM timer compare values in the GPT320.GTCCRC and GPT320.GTCCRE registers.
3. Set the default PWM timer period values in the GPT320.GTPR register and the next PWM timer period values in the GPT320.GTPBR register.
4. Set 1 to the output bit in PmnPFS.PDR, and set 00011b to the peripheral select bits in PmnPFS.PSEL[4:0].

(8) GPT activation

Set the GPT320.GTSTR.CSTRT bits to 1 to start the GPT320.GTCNT counter.

(9) DTC transfer

Every time a GPT320 counter overflow is generated with the GPT320.GTPR register, the next PWM timer compare values are transferred to the GPT320.GTCCRC and GPT320.GTCCRE registers. The setting for the next PWM timer period is transferred to the GPT320.GTPBR register.

(10) Interrupt handling

After the specified rounds of data transfer are complete, for example when the value in the CRA register for GPT transfer

becomes 0, a GPT320 counter overflow interrupt request is issued for the CPU. Complete the process for this interrupt in the handling routine.

15.6.3 Chain Transfer when Counter = 0

The second data transfer is performed only when the transfer counter is set to 0 in the first data transfer, and information in the first data transfer is repeatedly changed in the second transfer. Chain transfer enables transfers to be repeated 256 times or more.

The following procedure shows an example of configuring a 128-KB input buffer, where the input buffer is set so that its lower address starts with 0000h. Figure 15.14 shows a chain transfer when the counter = 0.

1. Set the normal transfer mode to input data for the first data transfer. Set the following:
   a. Transfer source address = fixed.
   b. CRA register = 0000h (65,536) times.
   c. MRB.CHNE bit = 1 (chain transfer is enabled).
   d. MRB.CHNS bit = 1 (chain transfer is performed only when the transfer counter is 0).
   e. MRB.DISEL bit = 0 (an interrupt request to the CPU is generated when the specified data transfer completes).
2. Prepare the upper 8-bit address of the start address at every 65,536 times of the transfer destination address for the first data transfer in different area such as the flash. For example, when setting the input buffer to 20 0000h to 21 FFFFh, prepare 21h and 20h.
3. For the second data transfer:
   a. Set the repeat transfer mode (source side: repeat area) to reset the transfer destination address of the first data transfer.
   b. Specify the upper 8 bits of the DAR register in the first transfer information area for the transfer destination.
   c. Set the MRB.CHNE bit = 0 (chain transfer is disabled).
   d. Set the MRB.DISEL bit = 0 (an interrupt request to the CPU is generated when the specified data transfer completes).
   e. When setting the input buffer to 20 0000h to 21 FFFFh, also set the transfer counter to 2.
4. The first data transfer is performed by an interrupt 65,536 times. When the transfer counter of the first data transfer becomes 0, the second data transfer starts. Set the upper 8 bits of the transfer source address of the first data transfer to 21h. The lower 16 bits of the transfer destination address and the transfer counter of the first data transfer become 0000h.
5. In succession, the first data transfer is performed by an interrupt 65,536 times as specified for the first data transfer. When the transfer counter of the first data transfer becomes 0, the second data transfer starts. Set the upper 8 bits of the transfer source address of the first data transfer to 20h. The lower 16 bits of the transfer destination address and the transfer counter of the first data transfer become 0000h.
6. Steps 4 and 5 are repeated indefinitely. Because the second data transfer is in repeat transfer mode, no interrupt request to the CPU is generated.

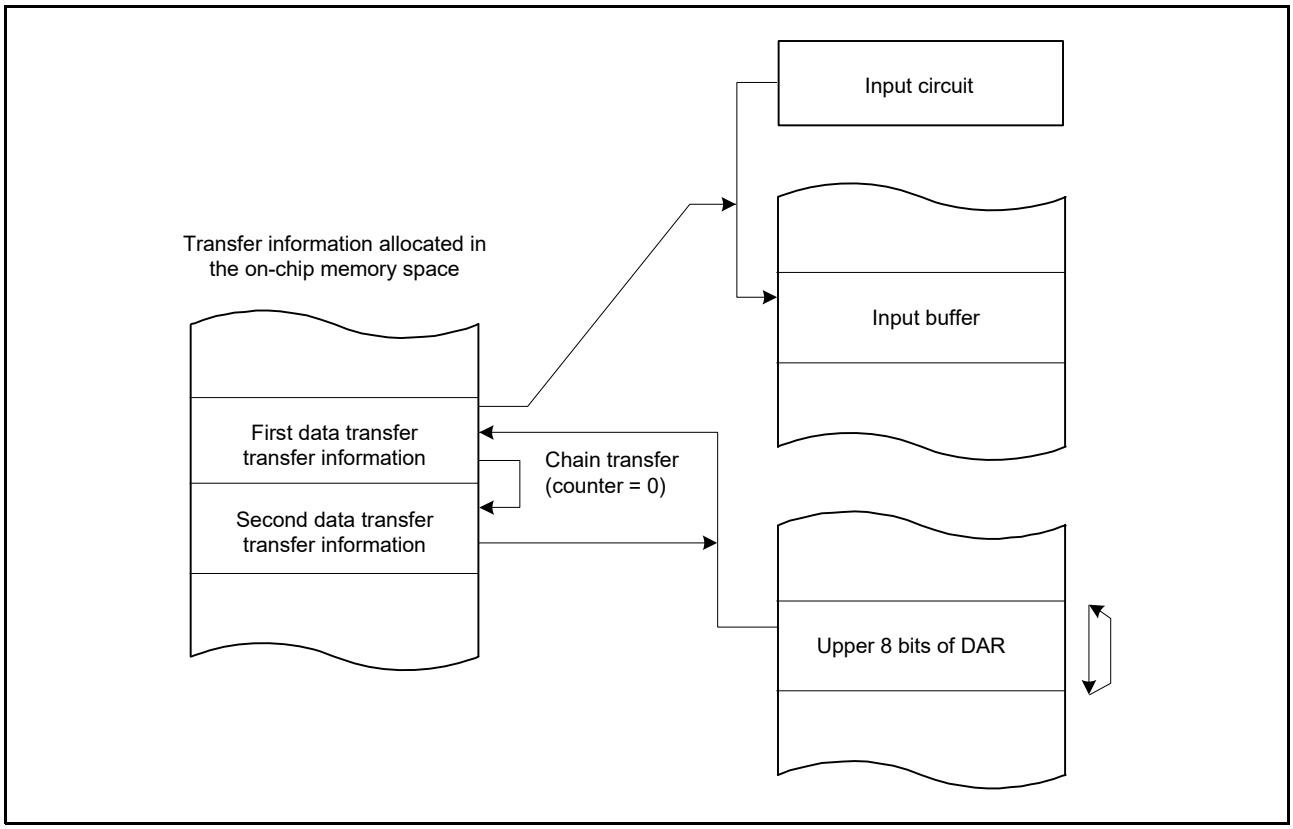


Figure 15.14 Chain transfer when counter = 0

15.7 Interrupt Source

When the DTC completes data transfer of the specified count or when data transfer with the MRB.DISEL set to 1 is complete, a DTC activation source generates an interrupt to the CPU. Interrupts to the CPU are controlled according to the settings in the NVIC and ICU.IELSRn.IELS[7:0] bits. See section 12, Interrupt Controller Unit (ICU). For priority of DTC activation source, the small interrupt vector number is of high priority. The priority of interrupts to the CPU is determined by the NVIC priority.

15.8 Event Link

The DTC can produce an event link request on completion of one transfer request.

15.9 Snooze Control Interface

To return to Software Standby mode from Snooze mode through the DTC, set the SYSTEM.SNZEDCR.DTCZRED or SYSTEM.SNZEDCR.DTCNZRED bit to 1. See section 10.8.3, Return to Software Standby Mode.

SYSTEM.SNZEDCR.DTCZRED enables or disables a snooze end request on completion of the last DTC transmission, detected on DTC transmission completion of CRA and CRB are 0.

SYSTEM.SNZEDCR.DTCNZRED enables or disables a snooze end request on a not last DTC transmission completion, detected on DTC transmission completion of CRA and CRB are not 0.

15.10 Module-Stop Function

Before transitioning to the module-stop function or Software Standby mode without Snooze mode transition, set the DTCST.DTCST bit to 0, then refer to information described in the following sections. The DTC is available in Snooze mode by setting the SYSTEM.SNZCR.SNZDTCEN bit to 1. See section 10, Low Power Modes.

(1) Module-stop function

Writing 1 to the MSTPCRA.MSTPA22 bit enables the module-stop function of the DTC. If the DTC transfer is in progress at the time, 1 is written to the MSTPCRA.MSTPA22 bit. The transition to the module-stop state proceeds after

DTC transfer ends. While the MSTPCRA.MSTPA22 bit is 1, accessing the DTC registers is prohibited.

Writing 0 to the MSTPCRA.MSTPA22 bit releases the DTC from the module-stop state.

(2) Software Standby mode

Use the settings described in section 10.7.1, Transition to Software Standby Mode.

If DTC transfer operations are in progress at the time the WFI instruction is executed, the transition to Software Standby mode follows the completion of the DTC transfer.

When the snooze control circuit receives a snooze request in Software Standby mode, the MCU transfers to Snooze mode. See section 10.8.1, Transition to Snooze Mode. DTC operation in Snooze mode can be selected in the SYSTEM.SNZCR.SNZDTCEN bit. If DTC operation is enabled in Snooze mode, before transitioning to Software Standby mode, set the DTCST.DTCST bit to 1. To return to Software Standby mode through DTC, set SYSTEM.SNZEDCR.DTCZRED or SYSTEM.SNZEDCR.DTCNZRED to 1. See section 10.8.3, Return to Software Standby Mode. The DTC activation request from the ICU is stopped during Software Standby mode but not during Snooze mode.

(3) Restrictions on module-stop function

For the WFI instruction and the register setting procedure, see section 10, Low Power Modes.

To perform a DTC transfer after returning from a low power mode without Snooze mode transition, set the DTCST.DTCST bit to 1 again.

To use a request that is generated in Software Standby mode as an interrupt request to the CPU but not as a DTC activation request, specify the CPU as the interrupt request destination as described in section 12.4.2, Selecting Interrupt Request Destinations, then execute the WFI instruction. If DTC operation is enabled in Snooze mode, do not use the module-stop function of the DTC.

15.11 Usage Notes

15.11.1 Transfer Information Start Address

You must set multiples of 4 for the transfer information start addresses in the vector table. Otherwise, such addresses are accessed with their lowest 2 bits regarded as 00b.

16. Event Link Controller (ELC)

16.1 Overview

The Event Link Controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link without CPU intervention.

Table 16.1 lists the ELC specifications, and Figure 16.1 shows a block diagram.

Table 16.1 ELC specifications

Parameter	Description
Event link function	116 types of event signals can be directly connected to modules. The ELC generates the ELC event signal and events that activate the DTC.
Module-stop function	Module-stop state can be set

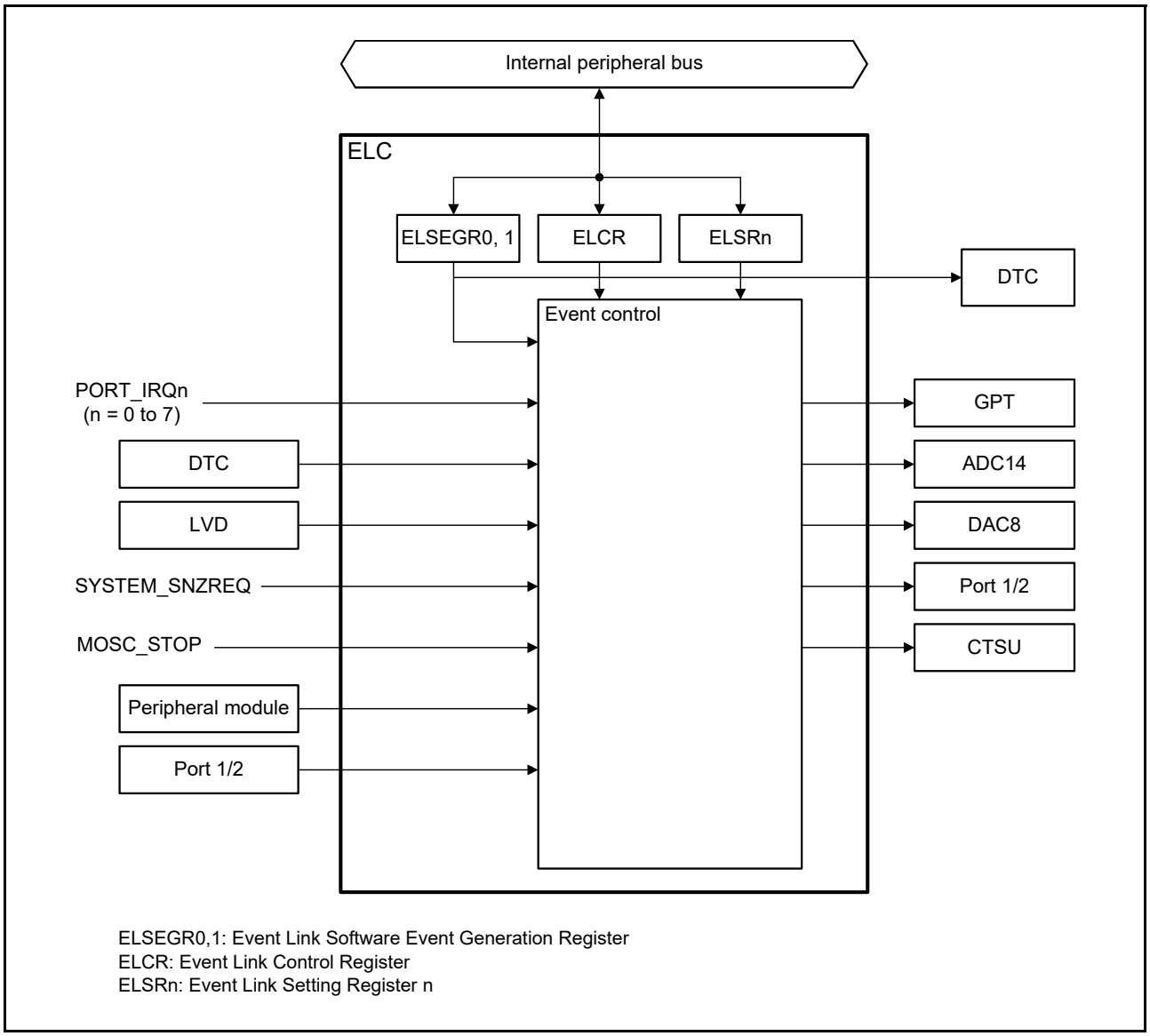


Figure 16.1 ELC block diagram when n = 0 to 3, 8, 9, 14, 15, 18 to 21

16.2 Register Descriptions

16.2.1 Event Link Controller Register (ELCR)

Address(es): ELC.ELCR 4004 1000h

	b7	b6	b5	b4	b3	b2	b1	b0
	ELCON	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	ELCON	All Event Link Enable	0: ELC function disabled 1: ELC function enabled.	R/W

The ELCR register controls the ELC operation.

16.2.2 Event Link Software Event Generation Register n (ELSEGRn) where n = 0, 1

Address(es): ELC.ELSEGR0 4004 1002h, ELC.ELSEGR1 4004 1004h

	b7	b6	b5	b4	b3	b2	b1	b0
	WI	WE	—	—	—	—	—	SEG
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SEG	Software Event Generation	0: Normal operation 1: Software event is generated.	W
b5 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	WE	SEG Bit Write Enable	0: Write to SEG bit disabled 1: Write to SEG bit enabled.	R/W
b7	WI	ELSEGR Register Write Disable	0: Write to ELSEGR register enabled 1: Write to ELSEGR register disabled.	W

SEG bit (Software Event Generation)

When 1 is written to this bit while the WE bit is 1, a software event is generated. This bit is read as 0. When 1 is written to this bit, data is not stored. The WE bit must be set to 1 before writing to this bit.

A software event can trigger a linked DTC event.

WE bit (SEG Bit Write Enable)

The SEG bit can only be written when the WE bit is 1. Clear the WI bit before writing to this bit.

[Setting condition]

- If 1 is written to this bit while the WI bit is 0, this bit becomes 1.

[Clearing condition]

- If 0 is written to this bit while the WI bit is 0, this bit becomes 0.

WI bit (ELSEGR Register Write Disable)

The ELSEGR register can only be written when the WI bit is 0. This bit is read as 1. The WI bit must be set to 0 before setting the WE or SEG bit.

16.2.3 Event Link Setting Register n (ELSRn)*1

Address(es): ELC.ELSR0 4004 1010h, ELC.ELSR1 4004 1014h, ELC.ELSR2 4004 1018h, ELC.ELSR3 4004 101Ch, ELC.ELSR8 4004 1030h, ELC.ELSR9 4004 1034h, ELC.ELSR14 4004 1048h, ELC.ELSR15 4004 104Ch, ELC.ELSR18 4004 1058h, ELC.ELSR19 4004 105Ch, ELC.ELSR20 4004 1060h, ELC.ELSR21 4004 1064h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	ELS[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	ELS[7:0]	Event Link Select	b7 b0 00000000: Event output disabled for the associated peripheral module 00000001 to 10001111: Number setting for the event signal to be linked. Other settings are prohibited.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. n = 0 to 3, 8, 9, 14, 15, 18 to 21

The ELSRn register specifies an event signal to be linked to each peripheral module. Table 16.2 shows the associations between the ELSRn register and the peripheral modules. Table 16.3 shows the associations between the event signal names set in the ELSRn register and the signal numbers.

Table 16.2 Associations between the ELSRn register and peripheral functions

Register name	Peripheral function	Event name
ELSR0	GPT (A)	ELC_GPTA
ELSR1	GPT (B)	ELC_GPTB
ELSR2	GPT (C)	ELC_GPTC
ELSR3	GPT (D)	ELC_GPTD
ELSR8	ADC14A	ELC_AD00
ELSR9	ADC14B	ELC_AD01
ELSR14	PORT 1	ELC_PORT1
ELSR15	PORT 2	ELC_PORT2
ELSR18	CTSU	ELC_CTSU
ELSR19	DA80	ELC_DA80
ELSR20	DA81	ELC_DA81
ELSR21	DA82	ELC_DA82

Table 16.3 Associations between event signal names set in ELSRn.ELS bits and signal numbers (1 of 3)

Event number	Interrupt request source	Name	Description
01h	Port	PORT_IRQ0*1	External pin interrupt 0
02h		PORT_IRQ1*1	External pin interrupt 1
03h		PORT_IRQ2*1	External pin interrupt 2
04h		PORT_IRQ3*1	External pin interrupt 3
05h		PORT_IRQ4*1	External pin interrupt 4
06h		PORT_IRQ5*1	External pin interrupt 5
07h		PORT_IRQ6*1	External pin interrupt 6
08h		PORT_IRQ7*1	External pin interrupt 7
0Ah	DTC	DTC_DTCEND*3	DTC transfer end
0Dh	LVD	LVD_LVD1	Voltage monitor 1 interrupt
0Eh		LVD_LVD2	Voltage monitor 2 interrupt
0Fh	MOSC	MOSC_STOP	Main clock oscillation stop
10h	Low Power mode	SYSTEM_SNZREQ*2, *3	Snooze entry
11h	AGT0	AGT0_AGTI	AGT interrupt
12h		AGT0_AGTCMAI	Compare match A
13h		AGT0_AGTCMBI	Compare match B
14h	AGT1	AGT1_AGTI	AGT interrupt
15h		AGT1_AGTCMAI	Compare match A
16h		AGT1_AGTCMBI	Compare match B
17h	IWDT	IWDT_NMIUNDF	IWDT underflow
18h	WDT	WDT_NMIUNDF	WDT underflow
1Ah	RTC	RTC_PRD	Periodic interrupt
1Ch	ADC140	ADC140_ADI	A/D scan end interrupt
20h		ADC140_WCMPM*3	Compare match
21h		ADC140_WCMPUM*3	Compare mismatch
22h	ACMPHS	ACMP_HS0*1	High-speed analog comparator interrupt 0
23h		ACMP_HS1*1	High-speed analog comparator interrupt 1
24h		ACMP_HS2*1	High-speed analog comparator interrupt 2
25h	ACMPLP	ACMP_LP0	Low-power analog comparator interrupt 0
26h		ACMP_LP1	Low-power analog comparator interrupt 1
29h	IIC0	IIC0_RXI	Receive data full
2Ah		IIC0_TXI	Transmit data empty
2Bh		IIC0_TEI	Transmit end
2Ch		IIC0_EEI	Transfer error
2Eh	IIC1	IIC1_RXI	Receive data full
2Fh		IIC1_TXI	Transmit data empty
30h		IIC1_TEI	Transmit end
31h		IIC1_EEI	Transfer error
36h	DOC	DOC_DOPCI*3	Data operation circuit interrupt
3Fh	I/O Ports	IOPORT_GROUP1	Port 1 event
40h		IOPORT_GROUP2	Port 2 event
41h	ELC	ELC_SWEVT0	Software event 0
42h		ELC_SWEVT1	Software event 1

Table 16.3 Associations between event signal names set in ELSRn.ELS bits and signal numbers (2 of 3)

Event number	Interrupt request source	Name	Description
45h	DALI	DALI_DEI	DALI Error interrupt
46h		DALI_CLI	CoLision detect interrupt
47h		DALI_SDI	Stop bit detect Interrupt
48h		DALI_BPI	Bus power down interrupt
49h		DALI_FEI	Fall Edge detect interrupt
4Bh	GPT320	GPT0_CCMPA	Compare match A
4Ch		GPT0_CCMPB	Compare match B
4Dh		GPT0_CMPC	Compare match C
4Eh		GPT0_CMPD	Compare match D
4Fh		GPT0_OVF	Overflow
50h		GPT0_UDF	Underflow
51h	GPT16H1	GPT1_CCMPA	Compare match A
52h		GPT1_CCMPB	Compare match B
53h		GPT1_CMPC	Compare match C
54h		GPT1_CMPD	Compare match D
55h		GPT1_OVF	Overflow
56h		GPT1_UDF	Underflow
57h	GPT16H2	GPT2_CCMPA	Compare match A
58h		GPT2_CCMPB	Compare match B
59h		GPT2_CMPC	Compare match C
5Ah		GPT2_CMPD	Compare match D
5Bh		GPT2_OVF	Overflow
5Ch		GPT2_UDF	Underflow
5Dh	GPT16H3	GPT3_CCMPA	Compare match A
5Eh		GPT3_CCMPB	Compare match B
5Fh		GPT3_CMPC	Compare match C
60h		GPT3_CMPD	Compare match D
61h		GPT3_OVF	Overflow
62h		GPT3_UDF	Underflow
63h	GPT164	GPT4_CCMPA	Compare match A
64h		GPT4_CCMPB	Compare match B
65h		GPT4_CMPC	Compare match C
66h		GPT4_CMPD	Compare match D
67h		GPT4_OVF	Overflow
68h		GPT4_UDF	Underflow
69h	GPT165	GPT5_CCMPA	Compare match A
6Ah		GPT5_CCMPB	Compare match B
6Bh		GPT5_CMPC	Compare match C
6Ch		GPT5_CMPD	Compare match D
6Dh		GPT5_OVF	Overflow
6Eh		GPT5_UDF	Underflow

Table 16.3 Associations between event signal names set in ELSRn.ELS bits and signal numbers (3 of 3)

Event number	Interrupt request source	Name	Description
6Fh	GPT166	GPT6_CCMPA	Compare match A
70h		GPT6_CCMPB	Compare match B
71h		GPT6_CMPC	Compare match C
72h		GPT6_CMPD	Compare match D
73h		GPT6_OVF	Overflow
74h		GPT6_UDF	Underflow
75h	GPT	GPT_UVWEDGE	UVW edge event
76h	SCI0	SCI0_RXI*4	Receive data full
77h		SCI0_TXI*4	Transmit data empty
78h		SCI0_TEI	Transmit end
79h		SCI0_ERI*4	Receive error
7Ah		SCI0_AM	Address match event
7Ch	SCI1	SCI1_RXI	Receive data full
7Dh		SCI1_TXI	Transmit data empty
7Eh		SCI1_TEI	Transmit end
7Fh		SCI1_ERI	Receive error
80h		SCI1_AM	Address match event
81h	SCI9	SCI9_RXI	Receive data full
82h		SCI9_TXI	Transmit data empty
83h		SCI9_TEI	Transmit end
84h		SCI9_ERI	Receive error
85h		SCI9_AM	Address match event
86h	SPI0	SPI0_SPRI	Receive buffer full
87h		SPI0_SPTI	Transmit buffer empty
88h		SPI0_SPII	Idle
89h		SPI0_SPEI	Error
8Ah		SPI0_SPTEND	Transmission completed event
8Bh	SPI1	SPI1_SPRI	Receive buffer full
8Ch		SPI1_SPTI	Transmit buffer empty
8Dh		SPI1_SPII	Idle
8Eh		SPI1_SPEI	Error
8Fh		SPI1_SPTEND	Transmission completed event

Note 1. Only pulse (edge detection) is supported.
Note 2. ELSR8, 9, 14, 15, and ELSR18 can select this event.
Note 3. This event occurs in Snooze mode.
Note 4. This event is not supported in FIFO mode.

16.3 Operation

16.3.1 Relation between Interrupt Handling and Event Linking

Event number for an event link is the same as that for the associated interrupt source. For information on generating event signals, see the explanation in the chapter for each event source module.

16.3.2 Linking Events

When an event occurs and that event is already set as a trigger in the Event Link Setting Register (ELSRn), the associated module is activated. The operation of the module must be set up in advance. Table 16.4 lists the operations of modules when an event occurs.

Table 16.4 Module operations when event occurs

Module	Operations when event occurs
GPT	• Start counting • Stop counting • Clear counting • Up counting • Down counting • Input capture.
ADC14	Starts A/D conversion
DAC8	Starts D/A conversion
I/O Ports	• Change pin output based on EORR (reset) or EOSR (set) • Latch pin state to EIDR • The following ports can be used for the ELC: PORT 1 PORT 2.
CTSU	Starts measurement operation
DTC	Starts DTC data transfer

16.3.3 Example Procedure for Linking Events

To link events:

1. Set the operation of the module for which an event is to be linked.
2. Set the appropriate ELSRn register for the module to be linked.
3. Set the ELCR.ELCON bit to 1 to enable linkage of all events.
4. Configure the module from which an event is output and activate the module. The link between the two modules is now active.

To stop event linkage of independent modules, set 00000000b in the ELSRn.ELS[7:0] bits associated with the modules.

To stop linkage of all events, set the ELCR.ELCON bit to 0.

If the event link output from the RTC is to be used, set the ELC after the RTC, such as for initialization and time setting. Unintended events can be generated if the RTC settings are made after the ELC settings.

16.4 Usage Notes

16.4.1 Linking DTC Transfer End Signals as Events

When linking the DTC transfer end signals as events, do not set the same peripheral module as the DTC transfer destination and event link destination. If set, the peripheral module might be started before DTC transfer to the peripheral module is complete.

16.4.2 Setting the Clocks

To link events, you must enable the ELC and the related modules. The modules cannot operate if the related modules are in the module-stop state or in the specific low power mode in which the module is stopped (Software Standby mode). Some modules perform in Snooze mode. For more information, see Table 16.3 and section 10, Low Power Modes.

16.4.3 Module-Stop Function Setting

The Module Stop Control Register C (MSTPCRC) can enable or disable ELC operation. After a reset, the ELC is disabled. The ELCON bit must be set to 0 before the ELC operation is disabled using the Module Stop Control Register. For more information, see Table 16.3 and section 10, Low Power Modes.

16.4.4 ELC Delay Time

In Figure 16.2, module A accesses module B through the ELC. There is a delay time in the ELC between module A and module B. The ELC delay time is shown in Table 16.5.

If the clock domains on both modules A and B are the same, the delay time is 0. However, if the clock domains on both modules are different, the ELC has some delay and the delay time is defined by the slower clock frequency between the clocks of module A and module B.

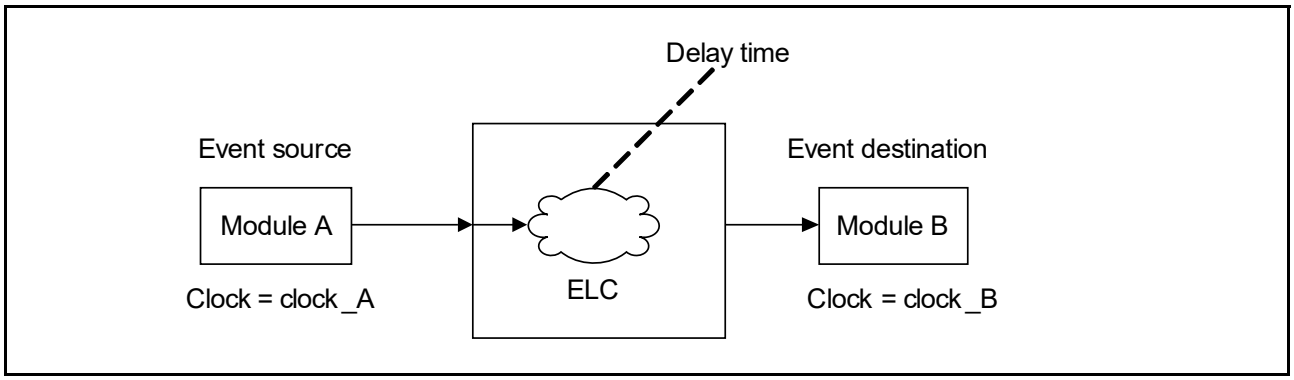


Figure 16.2 ELC delay time

Table 16.5 ELC delay time

Clock domain	Clock frequency	ELC delay time
clock_A = clock_B	clock_A = clock_B	0 cycle
clock_A ≠ clock_B	clock_A = clock_B	1 cycle to 2 cycles
	clock_A > clock_B	1 cycle to 2 cycles of B
	clock_A < clock_B	1 cycle to 2 cycles of A

17. I/O Ports

17.1 Overview

The pins of the I/O Ports operate as general I/O port pins, I/O pins for peripheral modules, interrupt input pins, analog I/O, or port group function for ELC.

All pins operate as input pins immediately after a reset and pin functions are switched by register settings. The setting of each pin is specified by the registers for the associated I/O Ports and peripheral modules.

Figure 17.1 shows the I/O Ports registers connection diagram.

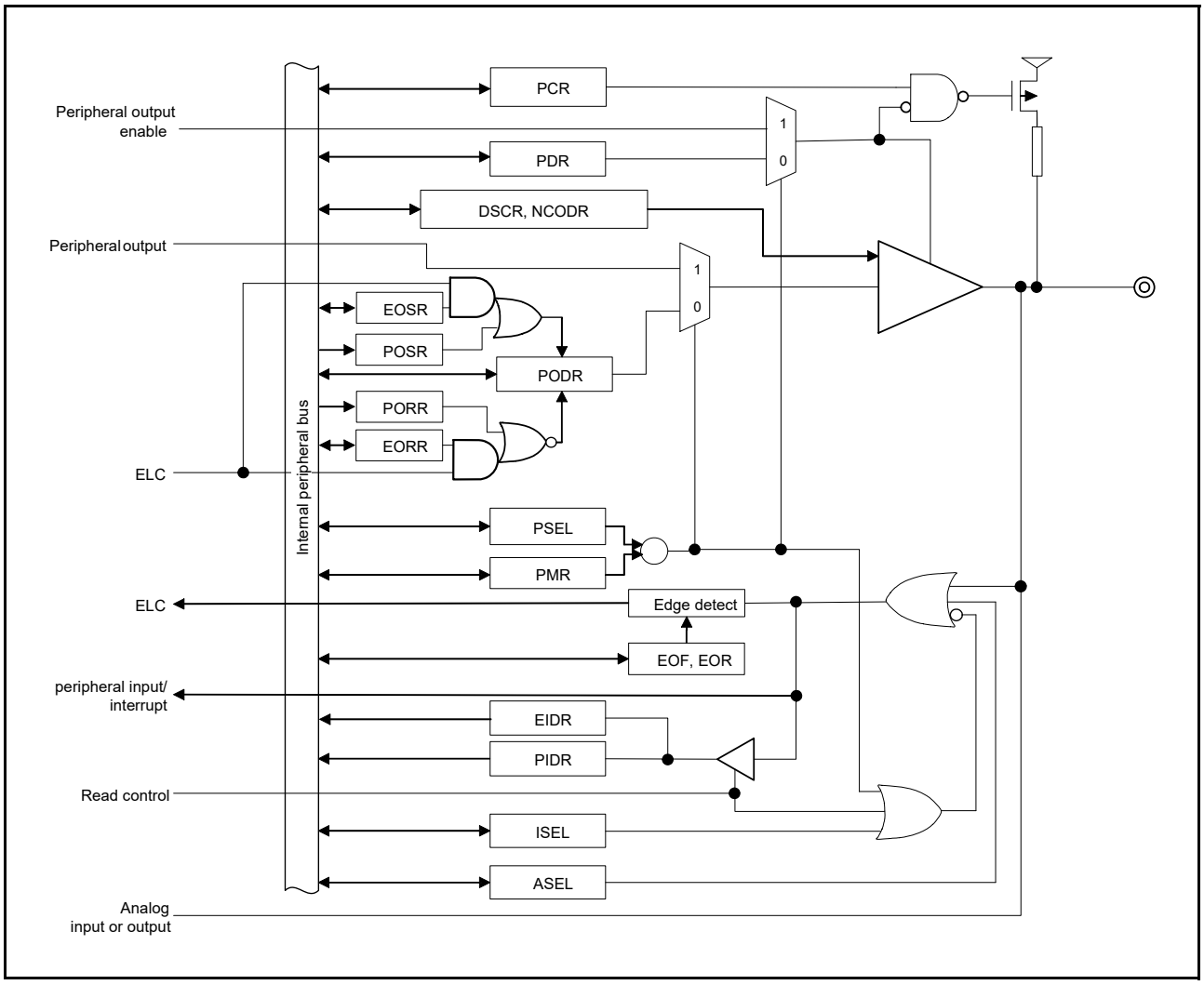


Figure 17.1 I/O Ports registers connection diagram

Note: This figure shows a basic configuration of ports. The configuration differs partially depending on ports.

The configuration of the I/O Ports depends on the package. Table 17.1 shows the specifications of I/O Ports and Table 17.2 lists the port functions.

Table 17.1 Specifications of I/O Ports

Port	Package		Package		Package		Package	
	64 pins	Number of pins	48 pins	Number of pins	36 pins	Number of pins	32 pins	Number of pins
PORT0	P000 to P004, P010 to P015	11	P000 to P002, P010 to P015	9	P000 to P002, P010 to P015	9	P010 to P015	6
PORT1	P100 to P113	14	P100 to P104, P108 to P112	10	P100 to P103, P108 to P112	9	P100 to P103, P108 to P110, P112	8
PORT2	P200, P201, P204 to P206, P212 to P215	9	P200, P201, P206, P212 to P215	7	P200, P201, P212 to P215	6	P200, P201, P212 to P215	6
PORT3	P300 to P304	5	P300 to P302	3	P300	1	P300	1
PORT4	P400 to P403, P407 to P411	9	P400, P401, P407 to P409	5	P407	1	P407	1
PORT5	P500 to P502	3	P500	1	N/A	0	N/A	0
PORT9	P914, P915	2	P914, P915	2	P914, P915	2	P914, P915	2
	Total of pins	53	Total of pins	37	Total of pins	28	Total of pins	24

Table 17.2 I/O port functions

Port	Port Name	Input Pull-up Function	Open Drain Output Function	Drive Capacity Switching	5-V Tolerant
PORT0	P000 to P004, P010 to P015	✓	-	low/middle	-
PORT1	P100, P101, P104, P109, P110, P112	✓	✓	low/middle	-
	P102, P103, P105 to P108, P111, P113	✓	-	low/middle	-
PORT2	P200, P214, P215	-	-	-	-
	P201	✓	-	low/middle	-
	P204	✓	✓	low/middle	-
	P205, P206	✓	✓	low/middle	✓
	P212, P213	✓	✓	-	-
PORT3	P300 to P304	✓	-	low/middle	-
PORT4	P400, P401, P407	✓	✓	low/middle	✓
	P402, P408 to P411	✓	✓	low/middle	-
	P403	✓	-	low/middle	-
PORT5	P500 to P502	✓	-	low/middle	-
PORT9	P914, P915	-	-	-	-

✓: Available
—: Setting prohibited

17.2 Register Descriptions

17.2.1 Port Control Register 1 (PCNTR1/PODR/PDR)

Address(es): PORT0.PCNTR1 4004 0000h, PORT1.PCNTR1 4004 0020h, PORT2.PCNTR1 4004 0040h, PORT3.PCNTR1 4004 0060h, PORT4.PCNTR1 4004 0080h, PORT5.PCNTR1 4004 00A0h, PORT9.PCNTR1 4004 0120h, PORT0.PODR 4004 0000h, PORT1.PODR 4004 0020h, PORT2.PODR 4004 0040h, PORT3.PODR 4004 0060h, PORT4.PODR 4004 0080h, PORT5.PODR 4004 00A0h, PORT9.PODR 4004 0120h, PORT0.PDR 4004 0002h, PORT1.PDR 4004 0022h, PORT2.PDR 4004 0042h, PORT3.PDR 4004 0062h, PORT4.PDR 4004 0082h, PORT5.PDR 4004 00A2h, PORT9.PDR 4004 0122h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PODR 15	PODR 14	PODR 13	PODR 12	PODR 11	PODR 10	PODR 09	PODR 08	PODR 07	PODR 06	PODR 05	PODR 04	PODR 03	PODR 02	PODR 01	PODR 00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PDR15	PDR14	PDR13	PDR12	PDR11	PDR10	PDR09	PDR08	PDR07	PDR06	PDR05	PDR04	PDR03	PDR02	PDR01	PDR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	PDRn	Pmn Direction	0: Input (functions as an input pin) 1: Output (functions as an output pin).	R/W
b31 to b16	PODRn	Pmn Output Data	0: Low output 1: High output.	R/W

m = 0 to 5, 9
n = 00 to 15

The Port Control Register 1 (PCNTR1/PODR/PDR) is a 32-bit and 16-bit read/write register that controls the port direction and the port output data.

The PCNTR1 specifies the port direction and port output data, and is accessed in 32-bit units. The PDRn (bits [15:0] in PCNTR1) and PODRn (bits [31:16] in PCNTR1) respectively, are accessed in 16-bit units.

PDRn bits (Pmn Direction)

The PDRn bits select the input or output direction for individual pins on the associated port when the pins are configured as general I/O pins. Each pin on port m is associated with a PORTm.PCNTR1.PDRn bit. The I/O direction can be specified in 1-bit units. Bits associated with non-existent pins are reserved. The write value should be 0. P200, P214, P215 are input only, so PORT2.PCNTR1.PDR00, PDR14, and PDR15 bits are reserved. The PDRn bit in the PORTm.PCNTR1 register serves the same function as the PDR bit in the PFS.PmnPFS register.

PODRn bits (Pmn Output Data)

The PODRn bits hold data to be output from the general I/O pins. Bits of non-existent port m are reserved. Write 0 to these bits. Bits associated with non-existent pins are reserved. The write value should be 0. P200, P214, and P215 are input only, so PORT2.PCNTR1.PODR00, PODR14, and PODR15 bits are reserved. The PODRn bit in the PORTm.PCNTR1 register serves the same function as the PODR bit in the PFS.PmnPFS register.

17.2.2 Port Control Register 2 (PCNTR2/EIDR/PIDR)

Address(es): PORT0.PCNTR2 4004 0004h, PORT1.PCNTR2 4004 0024h, PORT2.PCNTR2 4004 0044h, PORT3.PCNTR2 4004 0064h, PORT4.PCNTR2 4004 0084h, PORT5.PCNTR2 4004 00A4h, PORT9.PCNTR2 4004 0124h, PORT1.EIDR 4004 0024h, PORT2.EIDR 4004 0044h, PORT0.PIDR 4004 0006h, PORT1.PIDR 4004 0026h, PORT2.PIDR 4004 0046h, PORT3.PIDR 4004 0066h, PORT4.PIDR 4004 0086h, PORT5.PIDR 4004 00A6h, PORT9.PIDR 4004 0126h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	EIDR15	EIDR14	EIDR13	EIDR12	EIDR11	EIDR10	EIDR09	EIDR08	EIDR07	EIDR06	EIDR05	EIDR04	EIDR03	EIDR02	EIDR01	EIDR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PIDR15	PIDR14	PIDR13	PIDR12	PIDR11	PIDR10	PIDR09	PIDR08	PIDR07	PIDR06	PIDR05	PIDR04	PIDR03	PIDR02	PIDR01	PIDR00
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b15 to b0	PIDRn	Pmn State	0: Low level 1: High level.	R
b31 to b16	EIDRn	Port Event Input Data*1	When an ELC_PORTx occurs: 0: Low input 1: High input.	R

m = 0 to 5, 9
n = 00 to 15
x = 1 and 2

Note 1. Supported for PORT1 and PORT2.

The Port Control Register 2 (PCNTR2/EIDR/PIDR) allows read access to the Pmn state and the port event input data using 32-bit or 16-bit access.

The PCNTR2 specifies the Pmn state and the port event input data, and is accessed in 32-bit units. The PIDRn (bits [15:0] in PCNTR2) and EIDRn (bits [31:16] in PCNTR2) respectively, are accessed in 16-bit units. Bits associated with non-existent pins are reserved. Reserved bits are read as undefined.

PIDRn bits (Pmn State)

The PIDRn bits reflect the individual pin states of the port, regardless of the values set in PmnPFS.PMR and PORTm.PCNTR1.PDRn. The PIDRn bit in the PORTm.PCNTR2 register serves the same function as the PIDR bit in the PFS.PmnPFS register.

A pin state cannot be reflected in PIDRn when one of the following functions is enabled:

- Main clock oscillator (MOSC)
- Sub-clock oscillator (SOSC)
- Analog function (ASEL = 1)
- Capacitive Touch Sensing Unit (CTSU)
- USB 2.0 Full-Speed Module (USBFS).

EIDRn bits (Port Event Input Data)

The EIDRn bits latch a pin state when an ELC_PORTx signal occurs. Pin states can only be input to EIDRn when PmnPFS.PMR and PORTm.PCNTR1.PDRn are 0. When the PmnPFS.ASEL bit is set to 1, the associated pin state is not reflected in EIDRn.

17.2.3 Port Control Register 3 (PCNTR3/PORR/POSR)

Address(es): PORT0.PCNTR3 4004 0008h, PORT1.PCNTR3 4004 0028h, PORT2.PCNTR3 4004 0048h, PORT3.PCNTR3 4004 0068h, PORT4.PCNTR3 4004 0088h, PORT5.PCNTR3 4004 00A8h, PORT9.PCNTR3 4004 0128h, PORT0.PORR 4004 0008h, PORT1.PORR 4004 0028h, PORT2.PORR 4004 0048h, PORT3.PORR 4004 0068h, PORT4.PORR 4004 0088h, PORT5.PORR 4004 00A8h, PORT9.PORR 4004 0128h, PORT0.POSR 4004 000Ah, PORT1.POSR 4004 002Ah, PORT2.POSR 4004 004Ah, PORT3.POSR 4004 006Ah, PORT4.POSR 4004 008Ah, PORT5.POSR 4004 00AAh, PORT9.POSR 4004 012Ah

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PORR 15	PORR 14	PORR 13	PORR 12	PORR 11	PORR 10	PORR 09	PORR 08	PORR 07	PORR 06	PORR 05	PORR 04	PORR 03	PORR 02	PORR 01	PORR 00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	POSR 15	POSR 14	POSR 13	POSR 12	POSR 11	POSR 10	POSR 09	POSR 08	POSR 07	POSR 06	POSR 05	POSR 04	POSR 03	POSR 02	POSR 01	POSR 00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	POSRn	Pmn Output Set	0: No effect on output 1: High output.	W
b31 to b16	PORRn	Pmn Output Reset	0: No effect on output 1: Low output.	W

m = 0 to 5, 9
n = 00 to 15

Note: When EORRn or EOSRn is set, do not write to PODRn, PORRn and POSRn. Additionally, do not set PORRn and POSRn at the same time.

The Port Control Register 3 (PCNTR3/PORR/POSR) is a 32-bit and 16-bit write register that controls the setting or resetting of the port output data.

The PCNTR3 controls the setting or resetting of the port output data, and is accessed in 32-bit units. The POSRn (bits [15:0] in PCNTR3) and PORRn (bits [31:16] in PCNTR3) respectively, are accessed in 16-bit units.

POSRn bits (Pmn Output Set)

POSR changes PODR when set by a software write. For example, for P100, when PORT1.PCNTR3.POSR00 is 1, PORT1.PCNTR1.PODR00 outputs 1. Bits associated with non-existent pins are reserved. The write value should always be 0. P200, P214, and P215 are input only, so PORT2.PCNTR3.POSR00, POSR14, and POSR15 bits are reserved.

PORRn bits (Pmn Output Reset)

PORR changes PODR when reset by a software write. For example, for P100, when PORT1.PCNTR3.PORR00 is 1, PORT1.PCNTR1.PODR00 outputs 0. Bits associated with non-existent pins are reserved. The write value should always be 0. P200, P214, and P215 are input only, so PORT2.PCNTR3.PORR00, PORR14, and PORR15 bits are reserved.

17.2.4 Port Control Register 4 (PCNTR4/EORR/EOSR)

Address(es): PORT1.PCNTR4 4004 002Ch, PORT2.PCNTR4 4004 004Ch,
PORT1.EORR 4004 002Ch, PORT2.EORR 4004 004Ch,
PORT1.EOSR 4004 002Eh, PORT2.EOSR 4004 004Eh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	EORR 15	EORR 14	EORR 13	EORR 12	EORR 11	EORR 10	EORR 09	EORR 08	EORR 07	EORR 06	EORR 05	EORR 04	EORR 03	EORR 02	EORR 01	EORR 00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	EOSR 15	EOSR 14	EOSR 13	EOSR 12	EOSR 11	EOSR 10	EOSR 09	EOSR 08	EOSR 07	EOSR 06	EOSR 05	EOSR 04	EOSR 03	EOSR 02	EOSR 01	EOSR 00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	EOSRn	Pmn Event Output Set	When an ELC_PORTx occurs: 0: No effect on output 1: High output.	R/W
b31 to b16	EORRn	Pmn Event Output Reset	When an ELC_PORTx occurs: 0: No effect on output 1: Low output.	R/W

m = 1, 2
n = 00 to 15
x = 1 and 2

Note: When EORRn or EOSRn is set, do not write to PODRn, PORRn and POSRn. Additionally, do set EORRn and EOSRn at the same time.

The Port Control Register 4 (PCNTR4/EORR/EOSR) is a 32-bit and 16-bit read/write register that controls the setting or resetting of the port output data by event input from the ELC.

The PCNTR4 controls the setting or resetting of the port output data by an event input from the ELC, and is accessed in 32-bit units. The EOSRn (bits [15:0] in PCNTR4) and EORRn (bits [31:16] in PCNTR4) respectively, are accessed in 16-bit units.

EOSRn bits (Pmn Event Output Set)

EOSR changes PODR when set because an ELC_PORTx signal occurs. For example, for P100 if PORT1.PCNTR4.EOSR00 is set to 1 when the ELC_PORTx occurs, PORT1.PCNTR1.PODR00 outputs 1. Bits associated with non-existent pins are reserved. The write value should always be 0. P200, P214, and P215 are input only, so PORT2.PCNTR4.EOSR00, EOSR14, and EOSR15 bits are reserved.

EORRn bits (Pmn Event Output Reset)

EORR changes PODR when reset because an ELC_PORTx signal occurs. For example, for P100 if PORT1.PCNTR4.EORR00 is set to 1 when the ELC_PORTx occurs, PORT1.PCNTR1.PODR00 outputs 0. Bits associated with non-existent pins are reserved. The write value should always be 0. P200, P214, and P215 are input only, so PORT2.PCNTR4.EORR00, EORR14, and EORR15 bits are reserved.

17.2.5 Port mn Pin Function Select Register (PmnPFS/PmnPFS_HA/PmnPFS_BY) (m = 0 to 5, 9; n = 00 to 15)

Address(es): PFS.P000PFS 4004 0800h to PFS.P004PFS 4004 0810h, PFS.P010PFS 4004 0828h to PFS.P015PFS 4004 083Ch,
PFS.P100PFS 4004 0840h to PFS.P113PFS 4004 0874h,
PFS.P200PFS 4004 0880h to PFS.P201PFS 4004 0884h, PFS.P204PFS 4004 0890h to PFS.P206PFS 4004 0898h,
PFS.P212PFS 4004 08B0h to PFS.P215PFS 4004 08BCh,
PFS.P300PFS 4004 08C0h to PFS.P304PFS 4004 08D0h,
PFS.P400PFS 4004 0900h to PFS.P403PFS 4004 090Ch, PFS.P407PFS 4004 091Ch to PFS.P411PFS 4004 092Ch,
PFS.P500PFS 4004 0940h to PFS.P502PFS 4004 0948h,
PFS.P914PFS 4004 0A78h to PFS.P915PFS 4004 0A7Ch,
PFS.P000PFS_HA 4004 0802h to PFS.P004PFS_HA 4004 0812h, PFS.P010PFS_HA 4004 082Ah to PFS.P015PFS_HA 4004 083Eh,
PFS.P100PFS_HA 4004 0842h to PFS.P113PFS_HA 4004 0876h, PFS.P200PFS_HA 4004 0882h to PFS.P201PFS_HA 4004 0886h,
PFS.P204PFS_HA 4004 0892h to PFS.P206PFS_HA 4004 0896h, PFS.P212PFS_HA 4004 08B2h to PFS.P215PFS_HA 4004 08BEh,
PFS.P300PFS_HA 4004 08C2h to PFS.P304PFS_HA 4004 08D2h, PFS.P400PFS_HA 4004 0902h to PFS.P403PFS_HA 4004 090Eh,
PFS.P407PFS_HA 4004 091Eh to PFS.P411PFS_HA 4004 092Eh, PFS.P500PFS_HA 4004 0942h to PFS.P502PFS_HA 4004 094Ah,
PFS.P914PFS_HA 4004 0A7Ah to PFS.P915PFS_HA 4004 0A7Eh,
PFS.P000PFS_BY 4004 0803h to PFS.P004PFS_BY 4004 0813h, PFS.P010PFS_BY 4004 082Bh to PFS.P015PFS_BY 4004 083Fh,
PFS.P100PFS_BY 4004 0843h to PFS.P113PFS_BY 4004 0877h, PFS.P200PFS_BY 4004 0883h to PFS.P201PFS_BY 4004 0887h,
PFS.P204PFS_BY 4004 0893h to PFS.P206PFS_BY 4004 0897h, PFS.P212PFS_BY 4004 08B3h to PFS.P215PFS_BY 4004 08BFh,
PFS.P300PFS_BY 4004 08C3h to PFS.P304PFS_BY 4004 08D3h, PFS.P400PFS_BY 4004 0903h to PFS.P403PFS_BY 4004 090Fh,
PFS.P407PFS_BY 4004 091Fh to PFS.P411PFS_BY 4004 092Fh, PFS.P500PFS_BY 4004 0943h to PFS.P502PFS_BY 4004 094Bh,
PFS.P914PFS_BY 4004 0A7Bh to PFS.P915PFS_BY 4004 0A7Fh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	PSEL[4:0]					—	—	—	—	—	—	—	PMR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0*2

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ASEL	ISEL	EOF	EOR	—	DSCR	—	—	—	NCODR	PIM*3	PCR	—	PDR	PIDR	PODR
Value after reset:	0	0	0	0	0	0*2	0	0	0	0	0	0*2	0	0	x	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	PODR	Port Output Data	0: Low output 1: High output.	R/W
b1	PIDR	Pmn State	0: Low level 1: High level.	R
b2	PDR	Port Direction	0: Input (functions as an input pin) 1: Output (functions as an output pin).	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	PCR	Pull-up Control	0: Disables an input pull-up 1: Enables an input pull-up.	R/W
b5	PIM	Port Input Mode Control *3	0: CMOS input buffer 1: TTL input buffer.	R/W
b6	NCODR	N-Channel Open Drain Control	0: CMOS output 1: NMOS open-drain output.	R/W
b9 to b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b10	DSCR	Port Drive Capability	0: Low drive 1: Middle drive.	R/W
b11	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b13, b12	EOF/EOR	Event on Falling/Event on Rising *1	b13 b12 0 0: Don't care 0 1: Detect rising edge 1 0: Detect falling edge 1 1: Detect both edge.	R/W
b14	ISEL	IRQ Input Enable	0: Not used as an IRQn input pin 1: Used as an IRQn input pin.	R/W
b15	ASEL	Analog Input Enable	0: Used other than as an analog pin 1: Used as analog pin.	R/W
b16	PMR	Port Mode Control	0: Uses the pin as a general I/O pin. 1: Uses the pin as an I/O port for peripheral functions.	R/W

Bit	Symbol	Bit name	Description	R/W
b23 to b17	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b28 to b24	PSEL[4:0]	Peripheral Select	These bits select the peripheral function. For individual pin functions, see associated tables in this chapter.	R/W
b31 to b29	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Supported for PORT1 and PORT2.
Note 2. The initial value of P108, P201, P300, P914, and P915 is not 0000 0000h.
The initial value of P108 is 0001 0010h, P201 is 0000 0010h, P300 is 0001 0010h, and P914 and P915 is 0001 0000h.
Note 3. Supported for P100.

Port mn Pin Function Select register (PmnPFS/PmnPFS_HA/PmnPFS_BY) is a 32-bit, 16-bit, and 8-bit read/write control register that selects the port mn pin function, and is accessed in 32-bit units. PmnPFS_HA (bits [15:0] in PmnPFS) is accessed in 16-bit units. PmnPFS_BY (bits [7:0]) is accessed in 8-bit units.

PODR bit (Port Output Data), PIDR bit (Pmn State), PDR bit (Port Direction)

The PDR/PIDR/PODR bits serve the same function as the PCNTR. When these bits are read, the PCNTR value is read.

PCR bit (Pull-up Control)

The PCR bit is set when an input pull-up resistor is enabled or disabled for the individual pins of the port. When a pin is in the input state with the associated bit in PmnPFS set to 1, the pull-up resistor connected to the pin is enabled. When a pin is set as a general port output pin or a peripheral function output pin, the pull-up resistor for the pin is disabled regardless of the settings of PCR. The pull-up resistor is also disabled in the reset state. Bits associated with non-existent pins are reserved. The write value should be 0.

PIM bit (Port Input Mode Control)

The PIM bit specifies the input buffer (CMOS/TTL). This bit is reserved except when used for P100.

- When it is a reserved bit, the read and the write values are both 0
- When the SMBUS format is selected (ICMR3.SMBS = 1), TTL is selected as the IIC input level regardless of the PIM bit setting value.

NCODR bit (N-Channel Open Drain Control)

The NCODR bit specifies the output type for the port pins. Bits associated with non-existent pins are reserved. The write value should be 0.

DSCR bit (Port Drive Capability)

The DSCR bit switches the drive capacity of the port. If the drive capacity of a pin is fixed, the associated bit is read/write, but the drive capacity cannot be changed. Bits associated with non-existent pins are reserved. The write value should be 0.

EOF/EOR bits (Event on Falling/Event on Rising)

The EOR and EOF bits select the edge detection method for the port group input signal. These bits support rising, falling, or both edge detections. When the EOR/EOF bits are set to 01b, 10b, or 11b, the input enable of the I/O cell is asserted. Following that, the event pulse is input from the external pin, and GPIO outputs the event pulse to the ELC. Bits associated with non-existent pins are reserved. The write value should be 0.

ISEL bit (IRQ Input Enable)

The ISEL bit is set when a pin is used as an IRQ input pin. This setting can be used with the combination of the peripheral function, although IRQn (external pin interrupt) of the same number should not be enabled by two or more pins.

ASEL bit (Analog Input Enable)

The ASEL bit specifies analog pins. When a pin is set as an analog pin by this bit:

1. Specify it as a general I/O port with the Port Mode Control bit (PmnPFS.PMR)*1.
2. Disable the pull-up resistor with the Pull-up Control bit (PmnPFS.PCR).

3. Specify the input with the Port Direction bit (PmnPFS.PDR). The pin state cannot be read at this point. The PmnPFS register is protected by the Write-Protect Register (PWPR). Release write-protect before modifying the register.

Note 1. When the D/A converter output level is output to a port, select the I/O port for peripheral functions using the Port Mode Control bit because setting the D/A output by PmnPFS.PSEL bit is required.

The ISEL bit for an unspecified IRQn is reserved. The ASEL bit for an unspecified analog input/output is reserved.

PMR bit (Port Mode Control)

The PMR bit specifies the port pin function. Bits associated with non-existent pins are reserved. The write value should be 0.

PSEL[4:0] bits (Peripheral Select)

The PSEL[4:0] bits assign the assigned peripheral function.

For details on the peripheral select settings for each product, see section 17.6, Peripheral Select Settings for each product.

17.2.6 Write-Protect Register (PWPR)

Address(es): PMISC.PWPR 4004 0D03h

	b7	b6	b5	b4	b3	b2	b1	b0
	B0WI	PFSWE	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	PFSWE	PmnPFS Register Write Enable	0: Writing to the PmnPFS register is disabled 1: Writing to the PmnPFS register is enabled.	R/W
b7	B0WI	PFSWE Bit Write Disable	0: Writing to the PFSWE bit is enabled 1: Writing to the PFSWE bit is disabled.	R/W

PFSWE bit (PmnPFS Register Write Enable)

Writing to the PmnPFS register is enabled only when the PFSWE bit is set to 1. To set the PFSWE bit to 1, write 0 to the B0WI bit and then write 1 to the PFSWE bit.

B0WI bit (PFSWE Bit Write Disable)

Writing to the PFSWE bit is enabled only when the B0WI bit is set to 0.

17.3 Operation

17.3.1 General I/O Ports

All pins except P108 and P300 operate as general I/O ports after reset. General I/O ports are organized as 16 bits per port and can be accessed by port with the Port Control Registers (PCNTRn, where n=1 to 4) or by individual pin with the Pin Function Select Registers. For details on these registers, see section 17.2, Register Descriptions.

Each port has the following registers:

- Port Direction bit (PDRn), which selects input or output direction
- Port Output Data bit (PODRn), which holds data for output
- Port Input Data bit (PIDRn), which indicates the pin state
- Event Input Data bit (EIDRn), which indicates the pin state when an ELC_PORT1 or 2 occurs
- Port Output Set bit (POSRn), which indicates the output value when a software write occurs

- Port Output Reset bit (PORRn), which indicates the output value when a software write occurs
- Event Output Set bit (EOSRn), which indicates the output value when an ELC_PORT1 or 2 occurs
- Event Output Reset bit (EORRn), which indicates the output value when an ELC_PORT1 or 2 occurs.

17.3.2 Port Function Select

The following port functions are available for configuring each pin:

- I/O configuration: CMOS output or NMOS open-drain output, pull-up control, and drive strength
- General I/O port: Port direction, output data setting and read input data
- Alternate function: Configured function mapping to the pin.

Each pin is associated with a Pin Function Select Register (PmnPFS), which includes the associated PODR, PIDR, and PDR. In addition, the PmnPFS register includes:

- PCR: Pull-up control bit that turns the input pull-up MOS on or off
- PIM: Port input mode control bit that selects the input buffer type
- NCODR: N-channel open-drain control bit that selects the output type for each pin
- DSCR: Drive capacity bit that selects the drive capacity
- EOR: Event on rising bit used to detect rising edges on the port input
- EOF: Event on falling bit used to detect falling edges on the port input
- ISEL: IRQ input enable bit to specify an IRQ input pin
- ASEL: Analog input enable bit to specify an analog pin
- PMR: Port mode control bit to specify the pin function of each port
- PSEL[4:0]: Peripheral select bits to select the associated peripheral function.

This configuration is done by single-register access to the Port mn Pin Function Select register. For details, see section 17.2.5, Port mn Pin Function Select Register (PmnPFS/PmnPFS_HA/PmnPFS_BY) (m = 0 to 5, 9; n = 00 to 15).

17.3.3 Port Group Function for the ELC

PORT1 and PORT2 are assigned for the port group function.

17.3.3.1 Behavior when ELC_PORT1 or 2 is input from the ELC

The MCU supports two functions when the ELC_PORT1 or 2 comes from the ELC.

(1) Input to EIDR

For the GPI function (PDR = 0 and PMR = 0 in the PmnPFS register), when an ELC_PORT1 or 2 signal comes from the ELC, the input enable of the I/O cell is asserted, and data from the external pins are read into the EIDR bit. See Figure 17.2.

For the GPO function (PDR = 1) or the peripheral mode (PMR = 1), 0 is input into the EIDR bit from the external pins.

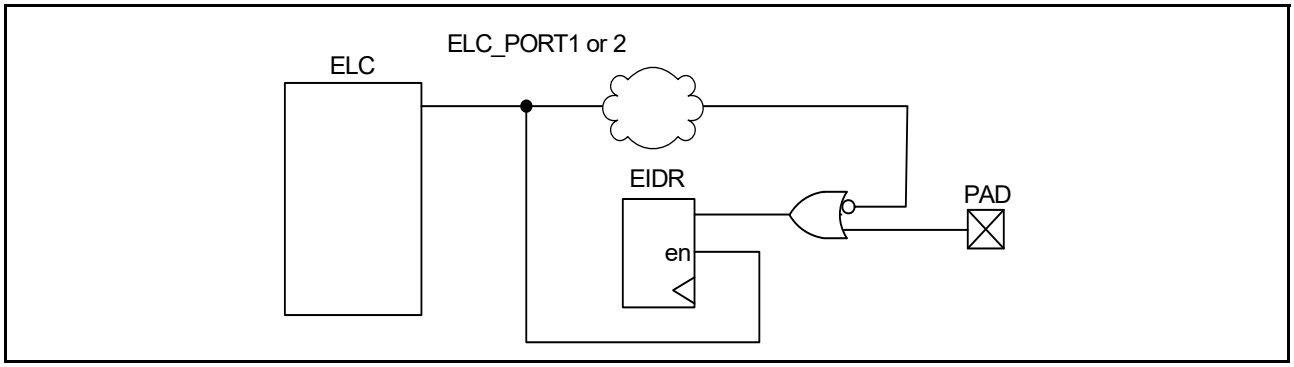


Figure 17.2 Port input data

(2) Output from PODR by EOSR/EORR

When an ELC_PORT1 or 2 signal occurs, the data is output from the PODR to the external pin based on the EOSR/EORR bit settings as follows:

- If EOSR is set to 1, when an ELC_PORT1 or 2 signal occurs, the PODR register outputs 1 to the external pin. Otherwise, when EOSR = 0, the PODR value is kept.
- If EORR is set to 1, when an ELC_PORT1 or 2 signal occurs, the PODR register outputs 0 to the external pin. Otherwise, when EORR = 0, the PODR value is kept.

See Figure 17.3.

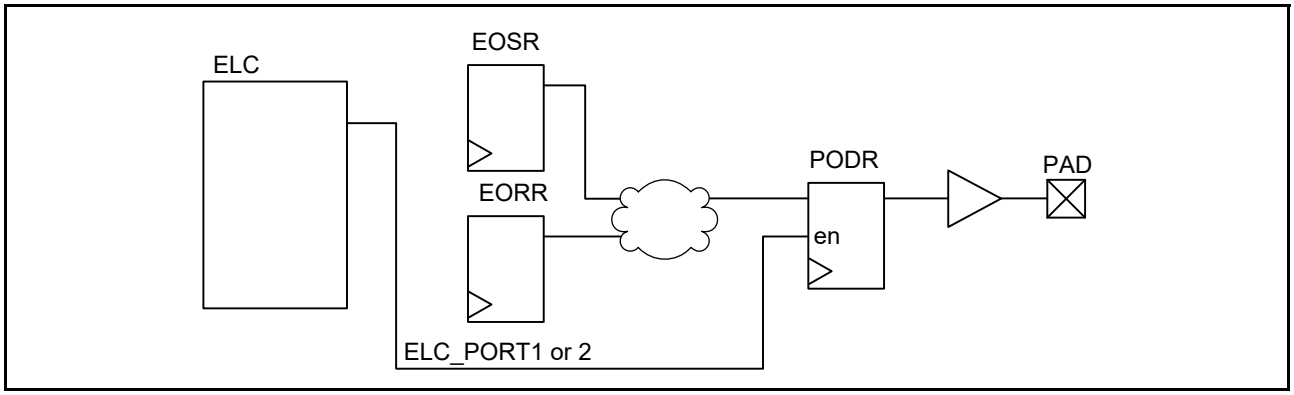


Figure 17.3 Ports output data

17.3.3.2 Behavior when an event pulse is output to the ELC

To output the event pulse from the external pins to the ELC, set the EOR/EOF bits in the PmnPFS register. For details, see section 17.2.5, Port mn Pin Function Select Register (PmnPFS/PmnPFS_HA/PmnPFS_BY) (m = 0 to 5, 9; n = 00 to 15). When the EOR/EOF bits are set, the input enable of the I/O cell is asserted.

Data from the external pin is the input. For example, for PORT1, when the data is input from P100 to P113, the data of those 14 pins is organized by OR logic. This data is formed into a one-shot pulse that goes to the ELC. The operation of PORT2 is also the same as PORT1. See Figure 17.4.

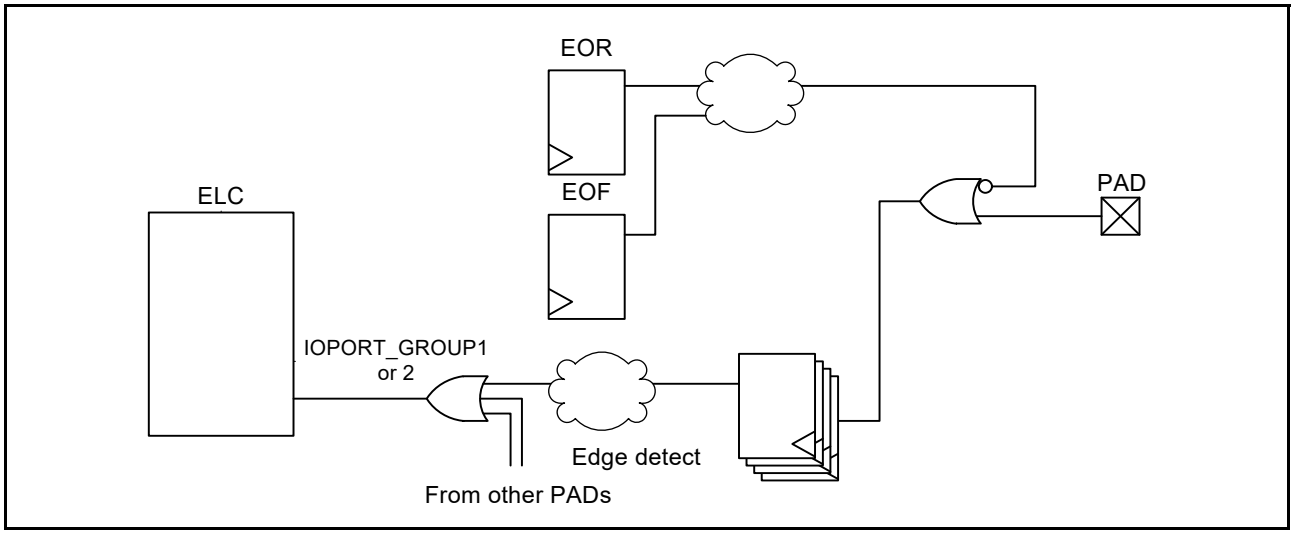


Figure 17.4 Generation of event pulse

17.4 Handling of Unused Pins

Details on the handling of unused pins are given in Table 17.3.

Table 17.3 Handling of unused pins

Pin Name	Description
P201/MD	Use this as a mode pin
RES	Connect this pin to VCC by a resistor (pulling up)
USB_DP, USB_DM	When both of P914PFS.PMR and P915PFS.PMR bits are set to 1. Keep these pins open. When P914PFS.PMR or P915PFS.PMR bit is set to 0, configure it in the same way as port 1 to 5, and port 9.
P200/NMI	Connect this pin to VCC by a resistor (pulling up)
P212/EXTAL	When the main clock oscillator is not used, set the MOSCCR.MOSTP bit to 1 (general port P212). When this pin is not used as port P212, it is configured in the same way as ports 1 to 5, and 9.
P213/XTAL	When the main clock oscillator is not used, set the MOSCCR.MOSTP bit to 1 (general port P213). When this pin is not used as port P213, it is configured in the same way as ports 1 to 5, and 9. When the external clock is input to the EXTAL pin, leave this pin open.
P215/XCIN	When the sub-clock oscillator is not used, set the SOSCCR.SOSTP bit to 1 (general port P215). When this pin is not used as port P215, it is configured in the same way as ports 1 to 5, and 9.
P214/XCOUT	When the sub-clock oscillator is not used, set the SOSCCR.SOSTP bit to 1 (general port P214). When this pin is not used as port P214, it is configured in the same way as ports 1 to 5, and 9.
P000 to P015	If the direction setting is for input (PCNTR1.PDRn = 0), the associated pin is connected to AVCC0 (pulled up) by a resistor or to AVSS0 (pulled down) by a resistor*1
P1x to P5x, P9x	• If the direction setting is for input (PCNTR1.PDRn = 0), the associated pin is connected to VCC (pulled up) by a resistor or to VSS (pulled down) by a resistor*1,*2 • If the direction setting is for output (PCNTR1.PDRn = 1), the pin is released.*1

Note 1. Clear the PmnPFS.PMR, PmnPFS.ISEL, PmnPFS.PCR, and PmnPFS.ASEL bits to 0.
Note 2. P108 and P300 are recommended for pull up VCC (pulled up) through a resistor, because these pins are input pull-up enabled from the initial value (PmnPFS.PCR = 1).

17.5 Usage Notes

17.5.1 Procedure for Specifying Pin Function

Perform the following steps to specify the input and output pin functions:

1. Clear the B0WI bit in the PWPR register. This enables writing to the PFSWE bit in the PWPR register.
2. Set 1 to the PFSWE bit in the PWPR register. This enables writing to the PmnPFS register.

3. Clear the Port Mode Control bit in the PMR for the target pin to select the general I/O port.
4. Specify the input/output function for the pin through the PSEL[4:0] bit settings in the PmnPFS register.
5. Set the PMR to 1 as required to switch to the selected input/output function for the pin.
6. Clear the PFSWE bit in the PWPR register. This disables writing to the PmnPFS register.
7. Set 1 to the B0WI bit in the PWPR register. This disables writing to the PFSWE bit in the PWPR register.

17.5.2 Procedure to Use Port Group Input

To use the port group input (PORT1 and PORT2):

1. Set the ELSRx.ELS[7:0] bits to 0000 0000b to ignore unexpected pulses. For more information, see section 16, Event Link Controller (ELC).
2. Set the EOF/EOR bit of the PmnPFS register to specify the rising, falling, or both edge detections.
3. Execute a dummy read or wait, for example 100 ns. Ignoring of unexpected pulses depends on the initial value of the external pin.
4. Set the ELSRx.ELS[7:0] bits to enable the event signals.

17.5.3 Port Output Data Register (PODR) Summary

This register outputs data as follows:

1. Output 0 if the PCNTR4.EORRn is set to 1 when an ELC_PORT1 or 2 occurs.
2. Output 1 if the PCNTR4.EOSRn is set to 1 when an ELC_PORT1 or 2 occurs.
3. Output 0 if the PCNTR3.PORRn is set to 1.
4. Output 1 if the PCNTR3.POSRn is set to 1.
5. Output 0 or 1 because PCNTR1.PODRn is set.
6. Output 0 or 1 because PmnPFS.PODRn is set.

Numbers in this list correspond to the priority for writing the PODR. For example, if 1. and 3. from the list occur at same time, the higher priority 1. is executed.

17.5.4 Notes on Use of Analog Functions

To use an analog function, set the Port Mode Control bit (PMR) and Port Direction bit (PDR) to 0 so that the pin acts as a general input port. Next, set the Analog Input Enable bit (ASEL) in the Port mn Pin Function Select register (PmnPFS.ASEL) to 1.

17.5.5 Selecting the USB_DP and USB_DM Pins

The USB_DP pin is shared with pin P914. The USB_DM pin is shared with pin P915. The USB_DP and P914 pins are set with the PFS.P914PFS.PMR bit and the USB_DM and P915 pins are set with the PFS.P915PFS.PMR bit. Table 17.4 shows setting values of bits PFS.P914PFS.PMR and PFS.P915PFS.PMR with each selected pin.

Table 17.4 Selecting the USB/PORT pins

PMR bits settings		Pins selected	
P914PFS.PMR bit	**P915PFS.PMR bit**	**P914/USB_DP pin**	**P915/USB_DM pin**
0	0	P914	P915
0	1	P914	P915
1	0	P914	P915
1	1	USB_DP	USB_DM

17.5.5.1 Notes on Using P914/USB_DP and P915/USB_DM

- When using P914/USB_DP and P915/USB_DM as GPIO pins (P914 and P915), use the USB-related registers with

their initial values

- When using P914/USB_DP and P915/USB_DM as USB pins (USB_DP and USB_DM), use the GPIO-related registers for P914 and P915 with their initial values
- When using P914/USB_DP and P915/USB_DM as GPIO pins or USB pins, set these pins only once after a reset.

17.6 Peripheral Select Settings for each product

This section provides details on the Pin Function Select configuration by the PmnPFS register. Some pin names have a _A, _B, _C, _D, or _E suffix. The suffix can be ignored when assigning functionality, but assigning the same function to two or more pins simultaneously is prohibited.

Table 17.5 Register settings for I/O pin functions (PORT0)

PSEL[4:0] bits settings	Function	Pin				
		P000	P001	P002	P003	P004
00000b (Value after reset)	Hi-Z/SWD	Hi-Z				
01010b	CAC/ADC14/DAC8	—	—	—	—	DA2_B
01100b	CTSU	TS21	TS22	—	—	TS25
ASEL bit		AN000/ AMP0+/ IVCMP2	AN001/ AMP0-/ IVREF2	AN002/ AMP0O	AN003/ AMP3O	AN004/ DA2_B
ISEL bit		IRQ6	IRQ7	IRQ2	—	IRQ3
DSCR bit		L/M	L/M	L/M	L/M	L/M
NCODR bit		—	—	—	—	—
PCR bit		✓	✓	✓	✓	✓
PIM bit		—	—	—	—	—
64-pin product		✓	✓	✓	✓	✓
48-pin product		✓	✓	✓	-	-
36-pin product		✓	✓	✓	-	-
32-pin product		-	-	-	-	-

PSEL[4:0] bits settings	Function	Pin					
		P010	P011	P012	P013	P014	P015
00000b (Value after reset)	Hi-Z/SWD	Hi-Z					
01010b	CAC/ADC14/DAC8	—	DA2_A	—	—	DA0	DA1_A
01100b	CTSU	—	—	—	—	TS29	TS28
ASEL bit		AN005/ VREFH0/ AMP1O	AN006/ VREFL0/ DA2_A/ AMP2O	AN007/ AMP1-/ IVREF0	AN008/ AMP1+/ IVCMP0	AN009/ DA0/ AMP2-/ IVREF1	AN010/ DA1_A/ AMP2+/ IVCMP1
ISEL bit		—	—	—	—	—	IRQ7
DSCR bit		L/M	L/M	L/M	L/M	L/M	L/M
NCODR bit		—	—	—	—	—	—
PCR bit		✓	✓	✓	✓	✓	✓
PIM bit		—	—	—	—	—	—
64-pin product		✓	✓	✓	✓	✓	✓
48-pin product		✓	✓	✓	✓	✓	✓
36-pin product		✓	✓	✓	✓	✓	✓
32-pin product		✓	✓	✓	✓	✓	✓

✓: Available
—: Setting prohibited
L/M: Low drive/Middle drive

Table 17.6 Register settings for I/O pin functions (PORT1) (1)

PSEL[4:0] Bits Settings	Function	Pin P100	P101	P102	P103	P104	P105	P106	P107
00000b (Value after reset)	Hi-Z/SWD	Hi-Z							
00001b	AGT	AGTIO0_A	AGTEE0	AGTO0	—	—	—	—	—
00010b	GPT	GTETRGA_A	GTETRGB_A	GTOWLO_A	GTOWUP_A	GTETRGB_B	GTETRGA_C	—	—
00011b	GPT	GTIOC5B_A	GTIOC5A_A	GTIOC2B_A	GTIOC2A_A	GTIOC1B_C	GTIOC1A_C	GTIOC0B_B	GTIOC0A_B
00100b	SCI	RXD0_A/ SCL0_A/ MISO0_A	TXD0_A/ SDA0_A/ MOSI0_A	SCK0_A	CTS0_RTS0_A /SS0_A/	RXD0_C/ SCL0_C/ MISO0_C	—	—	—
00101b	SCI	SCK1_A	CTS1_RTS1_A /SS1_A	—	—	—	—	—	—
00110b	SPI	MISOA_A	MOSIA_A	RSPCKA_A	SSLA0_A	SSLA1_A	SSLA2_A	SSLA3_A	—
00111b	IIC	SCL1_B	SDA1_B	—	—	—	—	—	—
01000b	KINT	KR00	KR01	KR02	KR03	KR04	KR05	KR06	KR07
01001b	CLKOUT/ ACMPHS/ ACMPLP/RTC	—	—	—	—	—	—	—	—
01010b	CAC/ADC14/DAC8	—	—	ADTRG0_A	—	—	—	—	—
01100b	CTSU	TS26	TS16	TS15	TS14	TS13	—	—	—
01110b	DALI	DRX0	DTX0	—	—	—	—	—	—
10000b	CAN	—	—	CRX0_C	CTX0_C	—	—	—	—
ASEL bit		AN022/ CMPIN0	AN021/ CMPREF0	AN020/ CMPIN1	AN019/ CMPREF1	AN018	AN017	AN016	—
ISEL bit		IRQ2	IRQ1	—	—	IRQ1	IRQ0	—	—
DSCR bit		L/M	L/M	L/M	L/M	L/M	L/M	L/M	L/M
NCODR bit		✓	✓	—	—	✓	—	—	—
PCR bit		✓	✓	✓	✓	✓	✓	✓	✓
PIM bit		✓	—	—	—	—	—	—	—
64-pin product		✓	✓	✓	✓	✓	✓	✓	✓
48-pin product		✓	✓	✓	✓	✓	-	-	-
36-pin product		✓	✓	✓	✓	-	-	-	-
32-pin product		✓	✓	✓	✓	-	-	-	-

✓: Available
—: Setting prohibited
L/M: Low drive/Middle drive

Table 17.7 Register settings for I/O pin functions (PORT1) (2) (1 of 2)

PSEL[4:0] bits settings	Function	Pin P108	P109	P110	P111	P112	P113
00000b (Value after reset)	Hi-Z/SWD	SWDIO	Hi-Z				
00001b	AGT	—	—	—	AGTOA0	AGTOB0	—
00010b	GPT	GTOULO_C	GTOVUP_A	GTOVLO_A	—	—	—
00011b	GPT	GTIOC0B_A	GTIOC1A_A	GTIOC1B_A	GTIOC3A_A	GTIOC3B_A	GTIOC2A_C
00100b	SCI	—	SCK1_E	CTS0_RTS0_C /SS0_C	SCK0_C	TXD0_C/ SDA0_C/ MOSI0_C	—
00101b	SCI	CTS9_RTS9_B /SS9_B	TXD9_B/ SDA9_B/ MOSI9_B	RXD9_B/ SCL9_B/ MISO9_B	SCK9_B	SCK1_D	—
00110b	SPI	SSLB0_B	MOSIB_B	MISOB_B	RSPCKB_B	SSLB0_C	—
00111b	IIC	—	—	—	—	—	—
01000b	KINT	—	—	—	—	—	—
01001b	CLKOUT/ ACMPHS/ ACMPLP/RTC	—	CLKOUT_B	VCOUT	—	—	—

Table 17.7 Register settings for I/O pin functions (PORT1) (2) (2 of 2)

PSEL[4:0] bits settings	Function	Pin P108	P109	P110	P111	P112	P113
01010b	CAC/ADC14/DAC8	—	—	—	—	—	—
01100b	CTSU	—	TS10	TS11	TS12	TSCAP_C	—
01110b	DALI	—	—	—	—	—	—
10000b	CAN	—	CTX0_A	CRX0_A	—	—	—
ASEL bit		—	—	—	—	—	—
ISEL bit		—	—	IRQ3	IRQ4	—	—
DSCR bit		L/M	L/M	L/M	L/M	L/M	L/M
NCODR bit		—	✓	✓	—	✓	—
PCR bit		✓	✓	✓	✓	✓	✓
PIM bit		—	—	—	—	—	—
64-pin product		✓	✓	✓	✓	✓	✓
48-pin product		✓	✓	✓	✓	✓	-
36-pin product		✓	✓	✓	✓	✓	-
32-pin product		✓	✓	✓	-	✓	-

✓: Available
—: Setting prohibited
L/M: Low drive/Middle drive

Table 17.8 Register settings for I/O pin functions (PORT2)

PSEL[4:0] bits settings	Function	Pin P200*1	P201	P204	P205	P206	P212	P213	P214	P215
00000b (Value after reset)	Hi-Z/SWD	Hi-Z								
00001b	AGT	—	—	AGTIO1_A	AGTO1	—	AGTEE1	—	—	—
00010b	GPT	—	—	GTIW_A	GTIV_A	GTIU_A	GTETRGB_D	GTETRGA_D	—	—
00011b	GPT	—	—	GTIOC4B_B	GTIOC4A_B	—	GTIOC0B_D	GTIOC0A_D	—	—
00100b	SCI	—	—	SCK0_D	TXD0_D/ SDA0_D/ MOSI0_D	RXD0_D/ SCL0_D/ MISO0_D	—	—	—	—
00101b	SCI	—	—	SCK9_A	CTS9_RTS9_ A/SS9_A	—	RXD1_A/ SCL1_A/ MISO1_A	TXD1_A/ SDA1_A/ MOSI1_A	—	—
00110b	SPI	—	—	RSPCKB_A	SSLB0_A	SSLB1_A	—	—	—	—
00111b	IIC	—	—	SCL0_B	SCL1_A	SDA1_A	—	—	—	—
01001b	CLKOUT/ ACMPHS/ ACMPLP/RTC	—	—	—	CLKOUT_A	—	—	—	—	—
01010b	CAC/ADC14/ DAC8	—	—	CACREF_A	—	—	—	—	—	—
01100b	CTSU	—	—	TS00	TSCAP_A	TS01	—	—	—	—
ASEL bit		—	—	—	—	—	—	—	—	—
ISEL bit		—	—	—	IRQ1	IRQ0	IRQ3	IRQ2	—	—
DSCR bit		—	L/M	L/M	L/M	L/M	—	—	—	—
NCODR bit		—	—	✓	✓	✓	✓	✓	—	—
PCR bit		—	✓	✓	✓	✓	✓	✓	—	—
PIM bit		—	—	—	—	—	—	—	—	—
64-pin product		✓	✓	✓	✓	✓	✓	✓	✓	✓
48-pin product		✓	✓	-	-	✓	✓	✓	✓	✓
36-pin product		✓	✓	-	-	-	✓	✓	✓	✓
32-pin product		✓	✓	-	-	-	✓	✓	✓	✓

✓: Available
—: Setting prohibited
L/M: Low drive/Middle drive

Note 1. When using NMI pin interrupt, Port related registers setting are not required.

Table 17.9 Register settings for I/O pin functions (PORT3)

PSEL[4:0] bits settings	Function	Pin P300	P301	P302	P303	P304
00000b (Value after reset)	Hi-Z/SWD	SWCLK	Hi-Z			
00001b	AGT	—	AGTIO0_D	—	—	—
00010b	GPT	GTOUUP_C	GTOULO_A	GTOUUP_A	—	—
00011b	GPT	GTIOC0A_A	GTIOC4B_A	GTIOC4A_A	GTIOC1B_B	GTIOC1A_B
00101b	SCI	—	CTS9_RTS9_D/SS9_D	—	—	—
00110b	SPI	SSLB1_B	SSLB2_B	SSLB3_B	—	—
01100b	CTSU	—	TS09	TS08	TS02	—
ASEL bit		—	—	—	—	—
ISEL bit		—	IRQ6	IRQ5	—	—
DSCR bit		L/M	L/M	L/M	L/M	L/M
NCODR bit		—	—	—	—	—
PCR bit		✓	✓	✓	✓	✓
PIM		—	—	—	—	—
64-pin product		✓	✓	✓	✓	✓
48-pin product		✓	✓	✓	-	-
36-pin product		✓	-	-	-	-
32-pin product		✓	-	-	-	-

✓: Available
—: Setting prohibited
L/M: Low drive/Middle drive

Table 17.10 Register settings for I/O pin functions (PORT4) (1 of 2)

PSEL[4:0] bits settings	Function	Pin P400	P401	P402	P403	P407	P408	P409	P410	P411
00000b (Value after reset)	Hi-Z/SWD	Hi-Z								
00001b	AGT	AGTIO1_D	—	—	—	AGTIO0_C	—	—	AGTOB1	AGTOA1
00010b	GPT	—	GTETRGA_B	—	—	—	GTOWLO_B	GTOWUP_B	GTOVLO_B	GTOVUP_B
00011b	GPT	GTIOC6A_A	GTIOC6B_A	GTIOC3B_B	GTIOC3A_B	GTIOC0A_E	GTIOC5B_B	GTIOC5A_B	GTIOC6B_B	GTIOC6A_B
00100b	SCI	SCK0_B	CTS0_RTS0_B/SS0_B	—	—	CTS0_RTS0_D/SS0_D	—	TXD0_E/SDA0_E/MOSI0_E	RXD0_B/SCL0_B/MISO0_B	TXD0_B/SDA0_B/MOSI0_B
00101b	SCI	SCK1_B	TXD1_B/SDA1_B/MOSI1_B	RXD1_B/SCL1_B/MISO1_B	CTS1_RTS1_B/SS1_B	—	RXD9_A/SCL9_A/MISO9_A	TXD9_A/SDA9_A/MOSI9_A	—	—
00110b	SPI	—	—	—	—	SSLB3_A	—	—	MISOA_B	MOSIA_B
00111b	IIC	SCL0_A	SDA0_A	—	—	SDA0_B	SCL0_C	—	—	—
01001b	CLKOUT/ACMPHS/ACMPLP/RTC	—	—	—	—	RTCOUT	—	—	—	—
01010b	CAC/ADC14/DAC8	CACREF_C	—	—	—	ADTRG0_B	—	—	—	—
01100b	CTSU	TS20	TS19	TS18	TS17	TS03	TS04	TS05	TS06	TS07
10000b	CAN	—	CTX0_B	CRX0_B	—	—	—	—	—	—
10011b	USBFS	—	—	—	—	USB_VBUS	—	—	—	—
ASEL bit		—	—	—	—	—	—	—	—	—
ISEL bit		IRQ0	IRQ5	IRQ4	—	—	IRQ7	IRQ6	IRQ5	IRQ4
DSCR bit		L/M	L/M	L/M	L/M	L/M	L/M	L/M	L/M	L/M
NCODR bit		✓	✓	✓	—	✓	✓	✓	✓	✓
PCR bit		✓	✓	✓	✓	✓	✓	✓	✓	✓
PIM bit		—	—	—	—	—	—	—	—	—
64-pin product		✓	✓	✓	✓	✓	✓	✓	✓	✓

Table 17.10 Register settings for I/O pin functions (PORT4) (2 of 2)

PSEL[4:0] bits settings	Function	Pin P400	P401	P402	P403	P407	P408	P409	P410	P411
48-pin product		✓	✓	-	-	✓	✓	✓	-	-
36-pin product		-	-	-	-	✓	-	-	-	-
32-pin product		-	-	-	-	✓	-	-	-	-

✓: Available
—: Setting prohibited
L/M: Low drive/Middle drive

Table 17.11 Register settings for I/O pin functions (PORT5)

PSEL[4:0] Bits Settings	Function	Pin P500	P501	P502
00000b (Value after reset)	Hi-Z/SWD	Hi-Z		
01010b	CAC/ADC14/ DAC8	DA1_B	—	—
01100b	CTSU	TS27	—	—
ASEL bit		AN013/ DA1_B	AN012/ AMP3+	AN011/ AMP3-
ISEL bit		—	—	—
DSCR bit		L/M	L/M	L/M
NCODR bit		—	—	—
PCR bit		✓	✓	✓
PIM bit		—	—	—
64-pin product		✓	✓	✓
48-pin product		✓	-	-
36-pin product		-	-	-
32-pin product		-	-	-

✓: Available
—: Setting prohibited
L/M: Low drive/Middle drive

Table 17.12 Register settings for I/O pin functions (PORT9)

PSEL[4:0] Bits Settings	Function	Pin P914	P915
00000b (Value after reset)	Hi-Z/SWD	Hi-Z	
ASEL bit		—	—
ISEL bit		—	—
DSCR bit		—	—
NCODR bit		—	—
PCR bit		—	—
PIM bit		—	—
64-pin product		✓	✓
48-pin product		✓	✓
36-pin product		✓	✓
32-pin product		✓	✓

✓: Available
—: Setting prohibited

18. Key Interrupt Function (KINT)

18.1 Overview

A key interrupt (KEY_INTKR) can be generated by setting the Key Return Mode Register (KRM) and inputting a rising edge/falling edge to the key interrupt input pins, KR00 to KR07. Table 18.1 shows the assignment for key interrupt detection. Table 18.2 shows the function configuration, and Figure 18.1 shows the block diagram.

Table 18.1 Assignment of key interrupt detection pins

Key interrupt mode control n (n = 0 - 7)	Description
KRM0	Controls KR00 signal in 1-bit units
KRM1	Controls KR01 signal in 1-bit units
KRM2	Controls KR02 signal in 1-bit units
KRM3	Controls KR03 signal in 1-bit units
KRM4	Controls KR04 signal in 1-bit units
KRM5	Controls KR05 signal in 1-bit units
KRM6	Controls KR06 signal in 1-bit units
KRM7	Controls KR07 signal in 1-bit units

Table 18.2 Configuration of key interrupt function (KINT)

Parameter	Configuration
Input	KR00 to KR07
Control registers	Key Return Control Register (KRCTL) Key Return Mode Register (KRM) Key Return Flag Register (KRF)

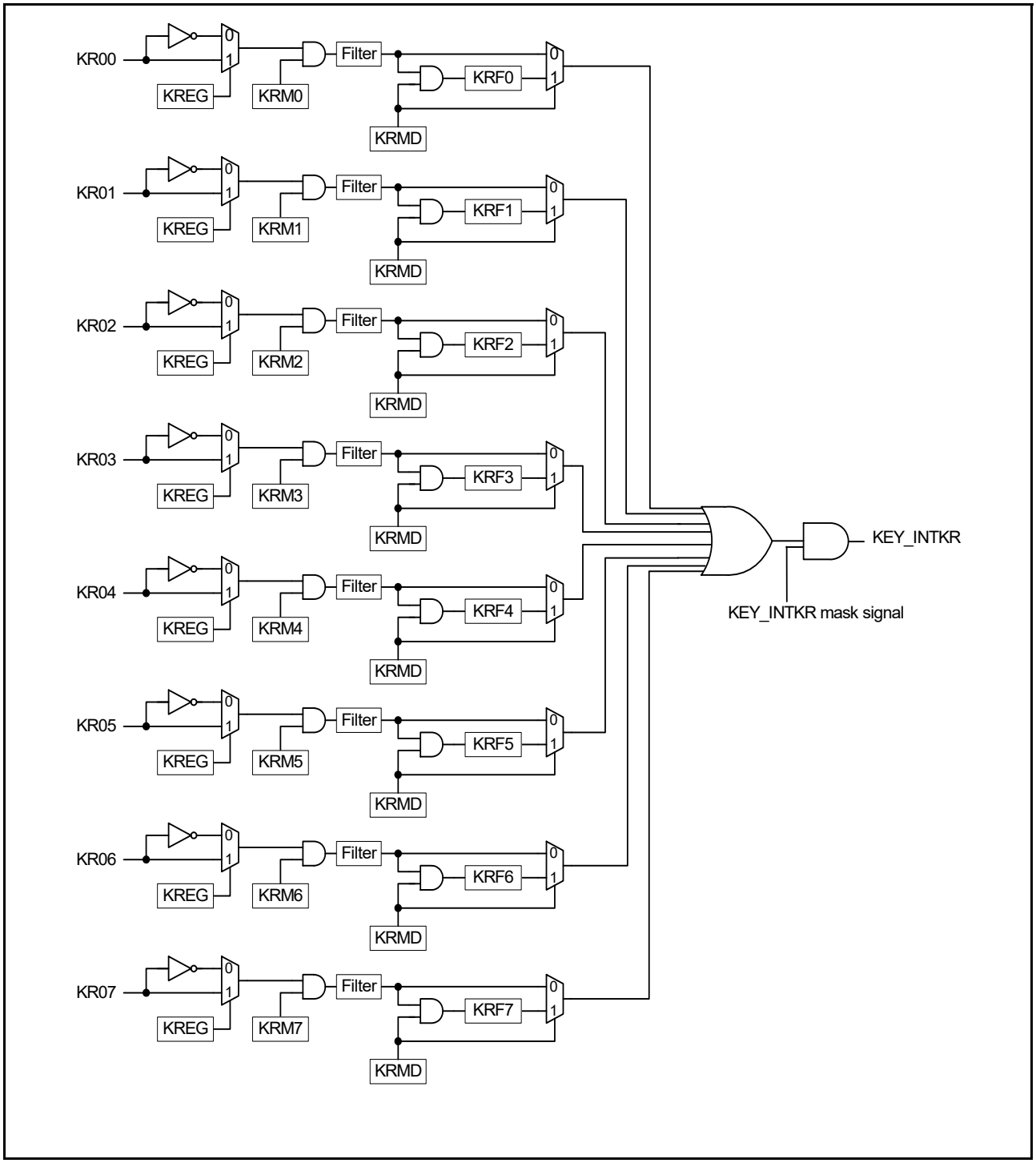


Figure 18.1 Key interrupt function block diagram

All key return factors are merged by an OR gate and the key interrupt (KEY_INTKR) is the output of the AND gate to mask the merged key return factor by the KEY_INTKR mask signal. When using KRFn (KRMD = 1), the KEY_INTKR mask signal is used as the output mask that is asserted by clearing KRFn.

18.2 Register Descriptions

18.2.1 Key Return Control Register (KRCTL)

Address(es): KINT.KRCTL 4008 0000h

	b7	b6	b5	b4	b3	b2	b1	b0
	KRMD	—	—	—	—	—	—	KREG
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	KREG	Selection of Detection Edge (KR00 to KR07)	0: Falling edge 1: Rising edge.	R/W
b6 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	KRMD	Usage of Key Interrupt Flags (KRF0 to KRF7)	0: Do not use key interrupt flags 1: Use key interrupt flags.	R/W

The KRCTL Register controls the usage of the key interrupt flags, KRF0 to KRF7, and sets the detection edge.

18.2.2 Key Return Flag Register (KRF)

Address(es): KINT.KRF 4008 0004h

	b7	b6	b5	b4	b3	b2	b1	b0
	KRF7	KRF6	KRF5	KRF4	KRF3	KRF2	KRF1	KRF0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	KRFn	Key Interrupt Flag n	0: No key interrupt detected 1: Key interrupt detected.	R/W

n = 0 to 7

Note: When KRMD = 0, setting the KRFn bit to 1 is prohibited.
When setting the KRFn bit to 1, the KRFn value does not change. To clear the KRFn bit, confirm the target bit is 1 before writing 0 to the bit, then write 1 to the other bits.

The KRF Register controls the key interrupt flags, KRF0 to KRF7.

18.2.3 Key Return Mode Register (KRM)

Address(es): KINT.KRM 4008 0008h

	b7	b6	b5	b4	b3	b2	b1	b0
	KRM7	KRM6	KRM5	KRM4	KRM3	KRM2	KRM1	KRM0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	KRMn	Key Interrupt Mode Control n	0: Do not detect key interrupt signal 1: Detect key interrupt signal.	R/W

n = 0 to 7

Note: The on-chip pull-up resistors can be applied by setting the associated key interrupt input pin in the pull-up resistor. For details, see section 17, I/O Ports.
Key interrupts can be assigned by the PmnPFS.PSEL bits. For details, see section 17, I/O Ports.
An interrupt is generated when the target bit in the KRM register is set when KREG is set to 0 or KREG is set to 1 is being input to the key interrupt input pin. To ignore this interrupt, set the KRM register after disabling the interrupt handling.

The KRM register sets the key interrupt mode.

18.3 Operation

18.3.1 When Not Using Key Interrupt Flag (KRMD = 0)

A key interrupt (KEY_INTKR) is generated when the valid edge specified in the KREG bit is input to a key interrupt pin, KR00 to KR07. To identify the channel to which the valid edge is input, read the port register and check the port level after the key interrupt (KEY_INTKR) is generated.

The KEY_INTKR signal changes according to the input level of the key interrupt input pin, KR00 to KR07.

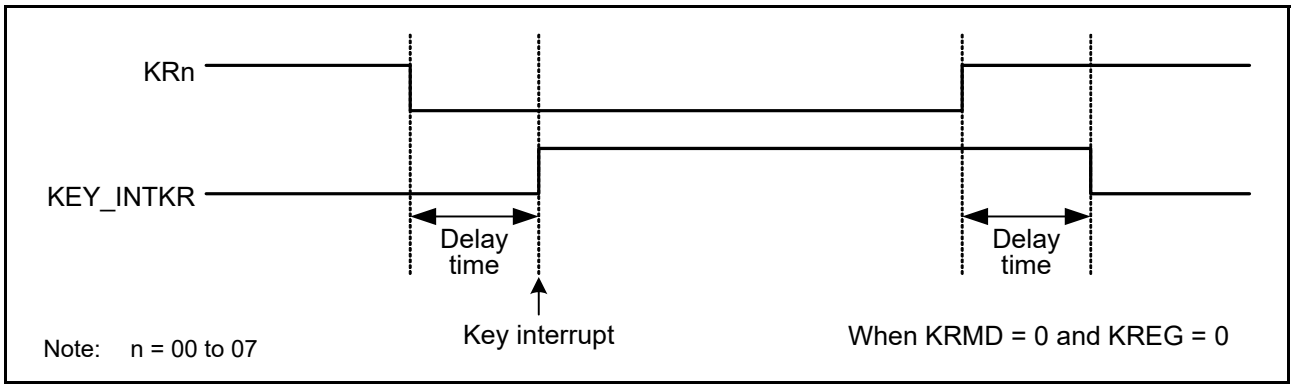


Figure 18.2 Operation of KEY_INTKR signal when key interrupt is input to a single channel

Figure 18.3 shows the operation when a valid edge is input to multiple key interrupt input pins. The KEY_INTKR signal is set while a low level is being input to one pin, that is, when KREG is set to 0. Therefore, even if a falling edge is input to another pin in this period, a key interrupt (KEY_INTKR) is not generated again. See [1] in Figure 18.3.

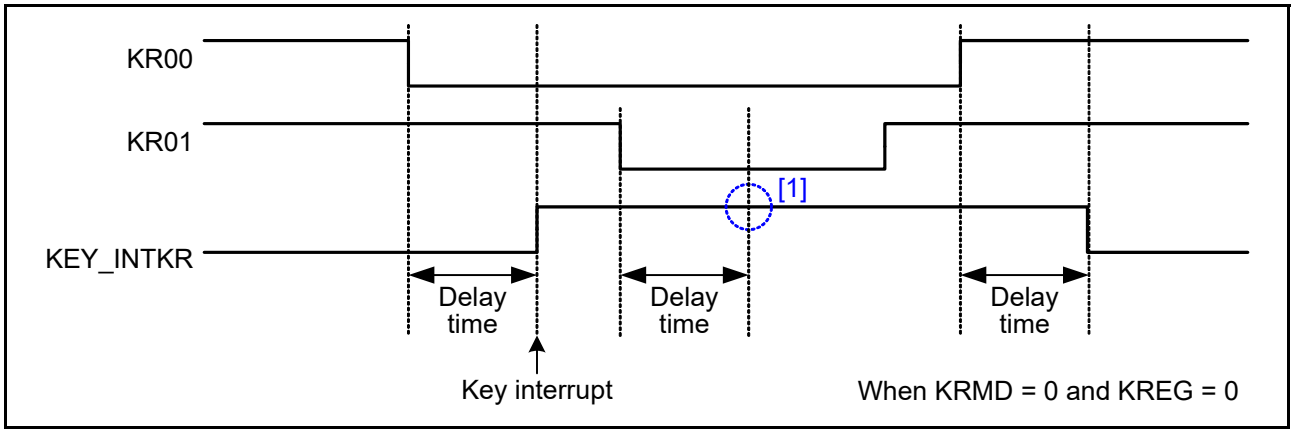


Figure 18.3 Operation of KEY_INTKR signal when key interrupts are input to multiple channels

18.3.2 When Using Key Interrupt Flag (KRMD = 1)

A key interrupt (KEY_INTKR) is generated when the valid edge specified in the KREG bit is input to a key interrupt pin, KR00 to KR07. To identify the channels to which the valid edge is input, read the Key Return Flag Register (KRF) after the key interrupt (KEY_INTKR) is generated. If the KRMD bit is set to 1, clear the KEY_INTKR signal by clearing the corresponding bit in the KRF Register.

As Figure 18.4 shows, only one interrupt is generated each time a falling edge is input to one channel, that is, when

KREG = 0, regardless of whether the KRFn bit is cleared before or after a rising edge is input.

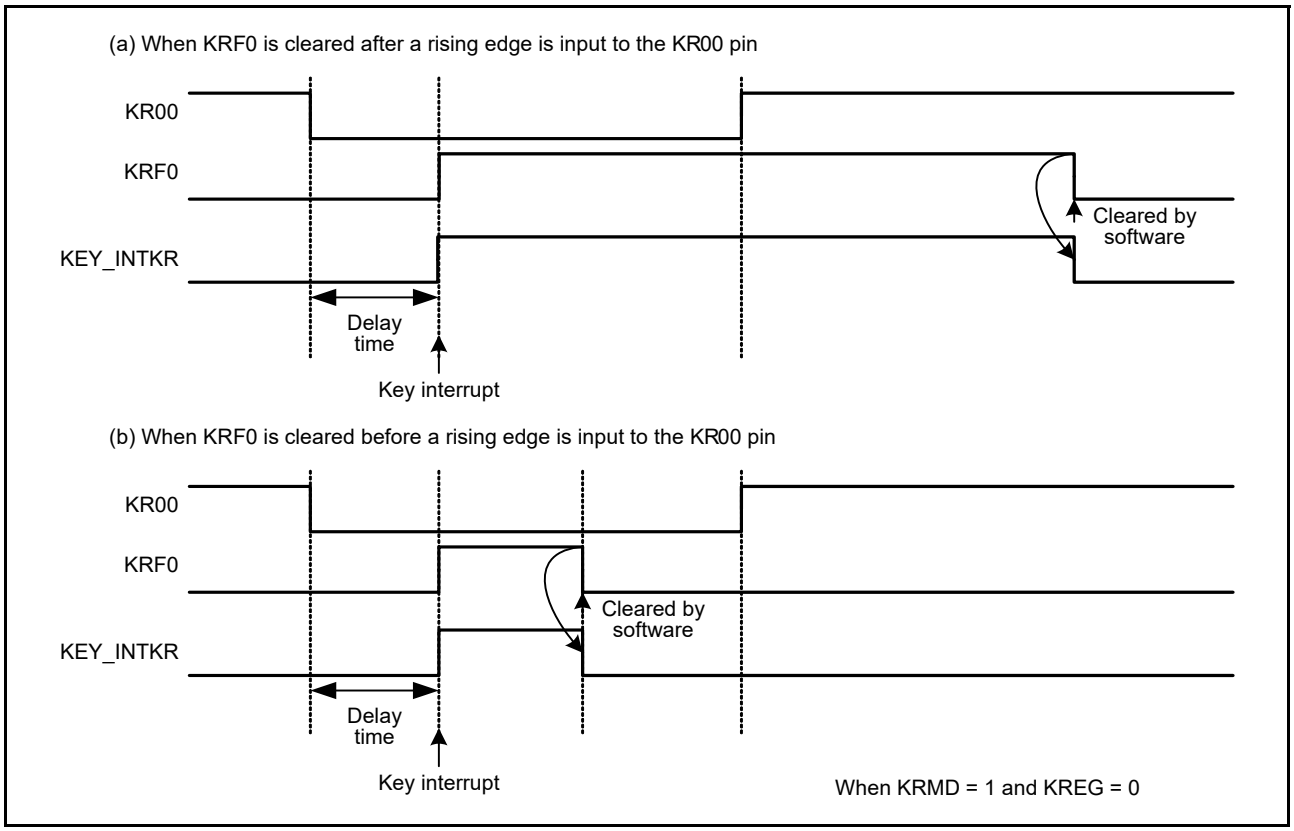


Figure 18.4 Basic operation of KEY_INTKR signal when key interrupt flag is used

Figure 18.5 shows the operation when a valid edge is input to multiple key interrupt input pins. A falling edge is also input to the KR01 and KR05 pins after a falling edge is input to the KR00 pin, that is, when KREG = 0. The KRF1 bit is set when the KRF0 bit is cleared. The KEY_INTKR signal is negated one PCLKB clock cycle, after the KRF0 bit is cleared. See [1] in Figure 18.5. Also, after a falling edge is input to the KR05 pin, the KRF5 bit is set. See [2] in the figure when the KRF1 bit is cleared. The KEY_INTKR signal is negated one PCLKB clock cycle, after the KRF1 bit is cleared. See [3] in the figure. It is therefore possible to generate a key interrupt when a valid edge is input to multiple channels.

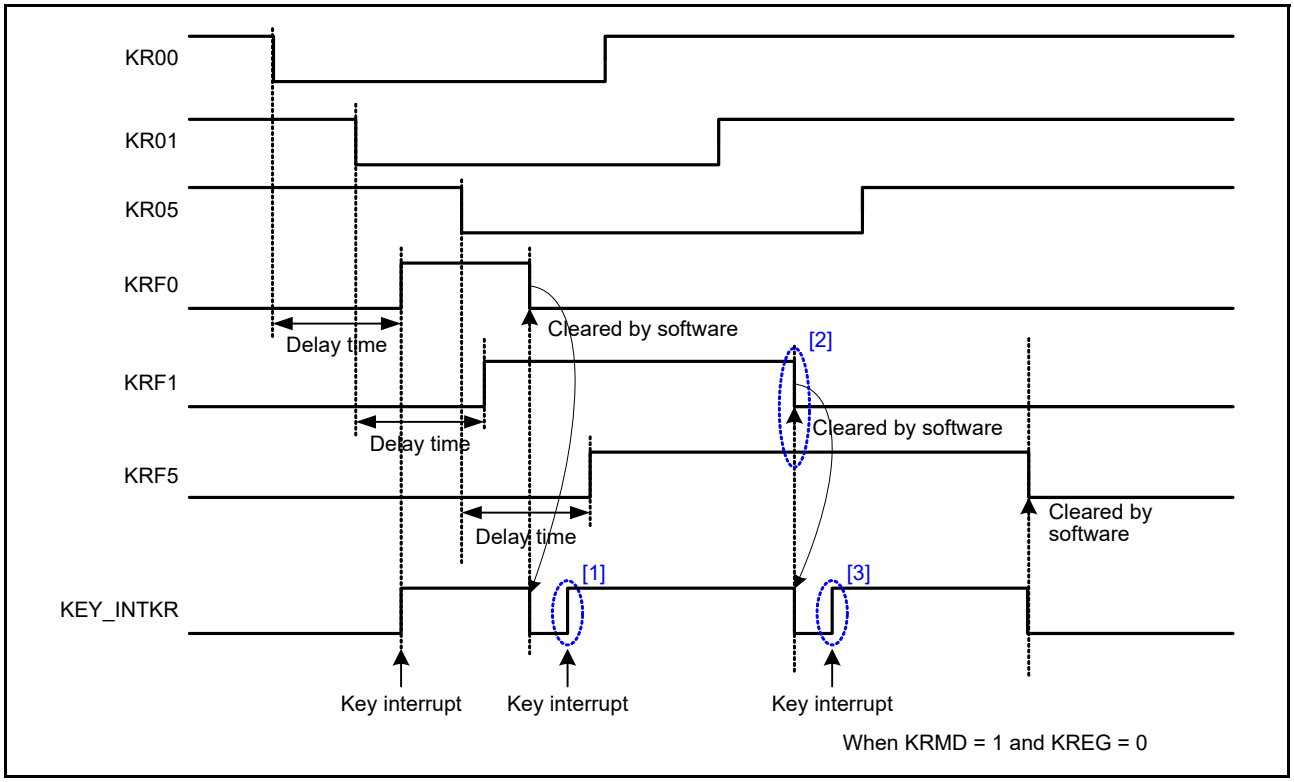


Figure 18.5 Operation of KEY_INTKR signal when key interrupts are input to multiple channels

18.4 Usage Note

- If the KEY_INTKR is used as the snooze request, the KRMD must be set to 0
- If the KEY_INTKR is used as the interrupt source for returning to Normal mode from Snooze and Software Standby modes, the KRMD must be set to 1
- When the key interrupt function is assigned to a pin, this pin input is always enabled in the Software Standby mode, and if this pin level changes, the corresponding KRFn might be set. Therefore, a key interrupt might occur on canceling the Software Standby mode.

To ignore changes to the key interrupt pin during software standby, clear the corresponding KRM bit before entering Software Standby mode. After canceling Software Standby mode, clear the KRF before the associated KRM bit can be set.

19. Port Output Enable for GPT (POEG)

19.1 Overview

The Port Output Enable (POEG) can place the General PWM Timer (GPT) output pins in the output disable state by the input level detection of the GTETRGn (n = A, B) pins, the output-disable request from GPT, the comparator (ACMPHS) interrupt request detection, the oscillation stop detection of the clock generation circuit, and the register settings. Additionally, the GTETRGn pins can be used for GPT external trigger input pins.

Table 19.1 lists the POEG specifications, Figure 19.1 shows a block diagram, and Table 19.2 shows the POEG input pins.

Table 19.1 POEG specifications

Parameter	Description
Output-disable control by input level detection	• The GPT output pins can be disabled when a GTETRGA or GTETRGB rising edge or high level is sampled after polarity and filter selection.
Output-disable request from GPT	• When the GTIOCA and GTIOCB pins are driven to an active level simultaneously, the GPT generates an output-disable request to the POEG. Through reception of these requests, the POEG can control whether the GTIOCA and GTIOCB pins are placed in output disable.
Output-disable control by the comparator (ACMPHS) interrupt request detection	• The GPT output pins can be disabled when an interrupt request is generated by a change in the output results of any of the comparators.
Output-disable control by oscillation stop detection	• The GPT output pins can be disabled when oscillation of the clock generation circuit stops.
Output-disable control by software (registers)	• The GPT output pins can be disabled by modifying the register settings.
Interrupts	• Output-disable control by input level detection • Output-disable request from the GPT or the comparator (ACMPHS) interrupt request detection.
External trigger output function to GPT (count start/count stop/count clear/up-count/down-count/input capture function)	• The GTETRGA and GTETRGB signals can be output to the GPT after polarity and filter selection.
Noise filtering	• Three times sampling for every PCLKB/1, PCLKB/8, PCLKB/32, or PCLKB/128 can be set for each input pin GTETRGA and GTETRGB • Positive or negative polarity can be selected for each input pin GTETRGA and GTETRGB • Signal state after polarity and filter selection can be monitored.

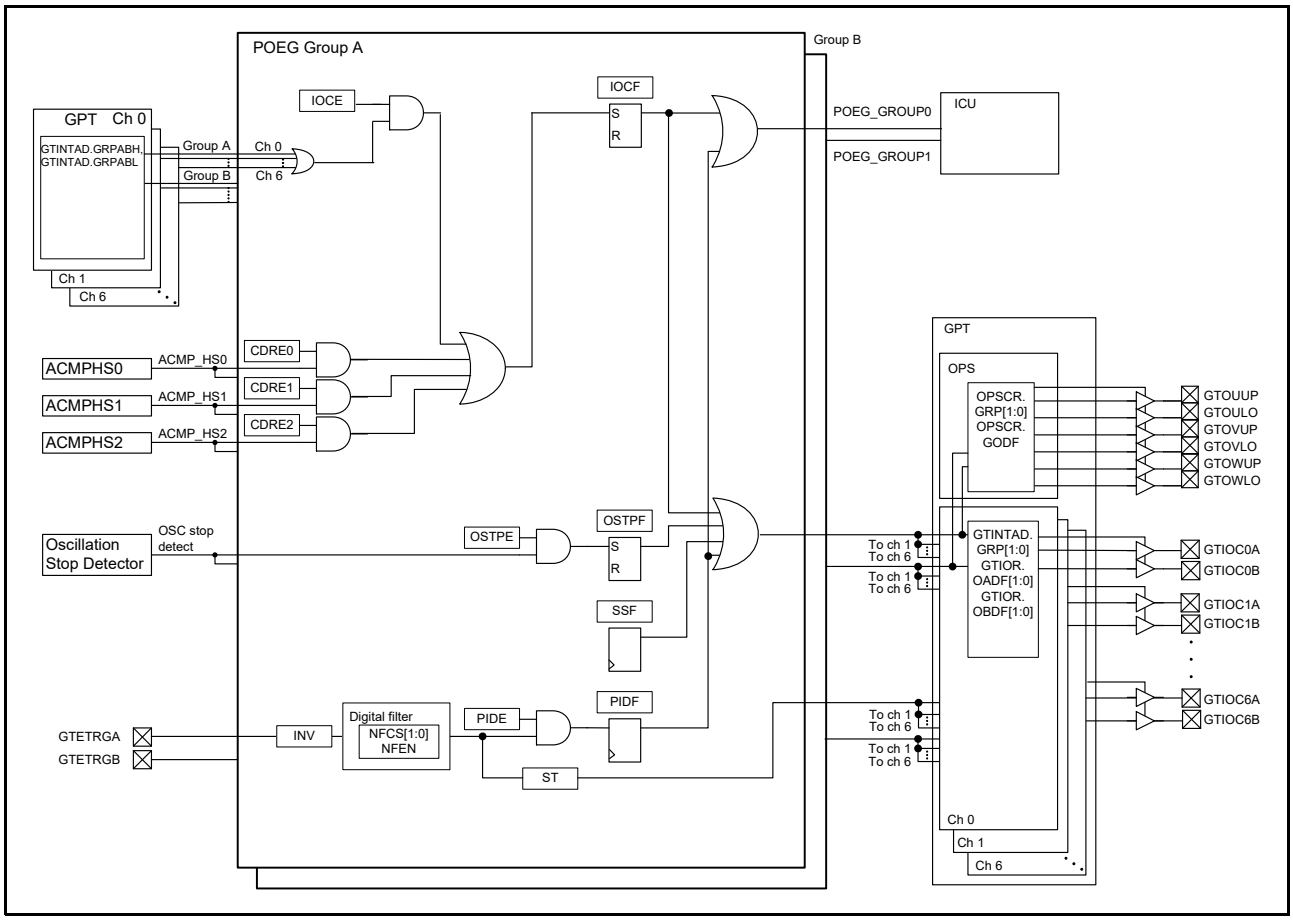


Figure 19.1 POEG block diagram

Table 19.2 POEG input pins

Pin name	I/O	Description
GTETRGA	Input	GPT output pin output-disable request signal and GPT external trigger input pin A
GTETRGB	Input	GPT output pin output-disable request signal and GPT external trigger input pin B

19.2 Register Descriptions

19.2.1 POEG Group n Setting Register (POEGGn) (n = A, B)

Address(es): POEG.POEGGA 4004 2000h, POEG.POEGGB 4004 2100h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	NFCS[1:0]		NFEN	INV	—	—	—	—	—	—	—	—	—	—	—	ST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	CDRE2	CDRE1	CDRE0	—	OSTPE	IOCE	PIDE	SSF	OSTPF	IOCF	PIDF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PIDF	Port Input Detection Flag	0: No output-disable request from the GTETRGn pin occurred 1: Output-disable request from the GTETRGn pin occurred.	R(/W)*1
b1	IOCF	Output-disable request Detection Flag from GPT or ACMPH	0: No output-disable request from the GPT or the ACMPHS occurred 1: Output-disable request from the GPT or the ACMPHS occurred.	R(/W)*1
b2	OSTPF	Oscillation Stop Detection Flag	0: No output-disable request from the oscillation stop detection occurred 1: Output-disable request from the oscillation stop detection occurred.	R(/W)*1
b3	SSF	Software Stop Flag	0: No output-disable request from software occurred 1: Output-disable request from software occurred.	R/W
b4	PIDE	Port Input Detection Enable	0: Disable output-disable request from the GTETRGn pins 1: Enable output-disable request from the GTETRGn pins.	R/W*2
b5	IOCE	Enable for GPT Output-disable request	0: Disable output-disable request from GPT disable request 1: Enable output-disable request from GPT disable request.	R/W*2
b6	OSTPE	Oscillation Stop Detection Enable	0: Disable output-disable request from the oscillation stop detection 1: Enable output-disable request from the oscillation stop detection.	R/W*2
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b8	CDRE0	ACMP_HS0 Enable	0: Disable output-disable request from ACMPHS0 1: Enable output-disable request from ACMPHS0.	R/W*2
b9	CDRE1	ACMP_HS1 Enable	0: Disable output-disable request from ACMPHS1 1: Enable output-disable request from ACMPHS1.	R/W*2
b10	CDRE2	ACMP_HS2 Enable	0: Disable output-disable request from ACMPHS2 1: Enable output-disable request from ACMPHS2.	R/W*2
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	ST	GTETRGn Input Status Flag	0: GTETRGn input after filtering is 0 1: GTETRGn input after filtering is 1.	R
b27 to b17	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b28	INV	GTETRGn Input Reverse	0: GTETRGn input 1: GTETRGn input reversed.	R/W
b29	NFEN	Noise Filter Enable	0: Disable filtering noise 1: Enable filtering noise.	R/W

Bit	Symbol	Bit name	Description	R/W
b31, b30	NFCS[1:0]	Noise Filter Clock Select	b1 b0 0 0: Sampling GTETRGn pin input level three times for every PCLKB 0 1: Sampling GTETRGn pin input level three times for every PCLKB/8 1 0: Sampling GTETRGn pin input level three times for every PCLKB/32 1 1: Sampling GTETRGn pin input level three times for every PCLKB/128.	R/W

Note 1. Only 0 can be written to clear the flag.
Note 2. Can be modified only once after a reset.

The POEGGA and POEGGB registers control the output-disable state of the GPT pins output, interrupts, and the external trigger input to GPT. In the sections that follow, POEGGn represents all the POEGGA and POEGGB registers.

19.3 Output-Disable Control Operation

If any of the following conditions is satisfied, the GTIOCxA, GTIOCxB, and the 3-phase PWM output for BLDC motor control pins can be set to output disable.

- Input level or edge detection of the GTETRGA and GTETRGB pins
  When POEGGn.PIDE is 1, the POEGGn.PIDF flag is set to 1.
- Output-disable request from the GPT
  When POEGGn.IOCE is 1, the POEGGn.IOCF flag is set to 1 if the disable request is enabled in GTINTAD. The GTINTAD.GRPABH or GTINTAD.GRPABL setting applies to the group selected in the GPT register GTINTAD.GRP[1:0] and OPSCR.GRP[1:0].
- Comparator (ACMPHS) interrupt request detection
  Comparator interrupt detection is activated when any of the POEGGn.CDRE[2:0] registers is 1. When the associated comparator interrupt is generated, the GPT output pins are disabled. POEGGn.IOCF indicates the detection status.
- Oscillation stop detection for the Clock Generation Circuit
  When POEGGn.OSTPE is 1, the POEGGn.OSTPF flag is set to 1.
- SSF bit setting
  When POEGGn.SSF is set to 1, the GPT and PWM output is disabled.

The state of output disable is controlled in the GPT. The output disable of the GTIOCxA and GTIOCxB pins are set to the GTINTAD.GRP, GTIOR.OADF, and GTIOR.OBDF bits in the GPT. The output disable of the 3-phase PWM output for BLDC motor control pins are set to the OPSCR.GRP and OPSCR.GODF bits in GPT_OPS.

19.3.1 Pin Input Level Detection Operation

If the input conditions set by POEGGn.PIDE, POEGGn.NFCS[1:0], POEGGn.NFEN and POEGGn.INV occur on the GTETRGA and GTETRGB pins, the GPT output pins are placed in output disable.

19.3.1.1 Digital filter

Figure 19.2 shows the high level detection by the digital filter. When a high level corresponding to the POEGGn.INV polarity setting is detected 3 times consecutively with the sampling clock selected by POEGGn.NFCS[1:0] and POEGGn.NFEN, the detected level is recognized as high, and the GPT output pins are placed in output disable. If even one low level is detected during this interval, the detected level is not recognized as high. In addition, in an interval where the sampling clock is not being output, changes of the levels on the GTETRGA and GTETRGB pins are ignored.

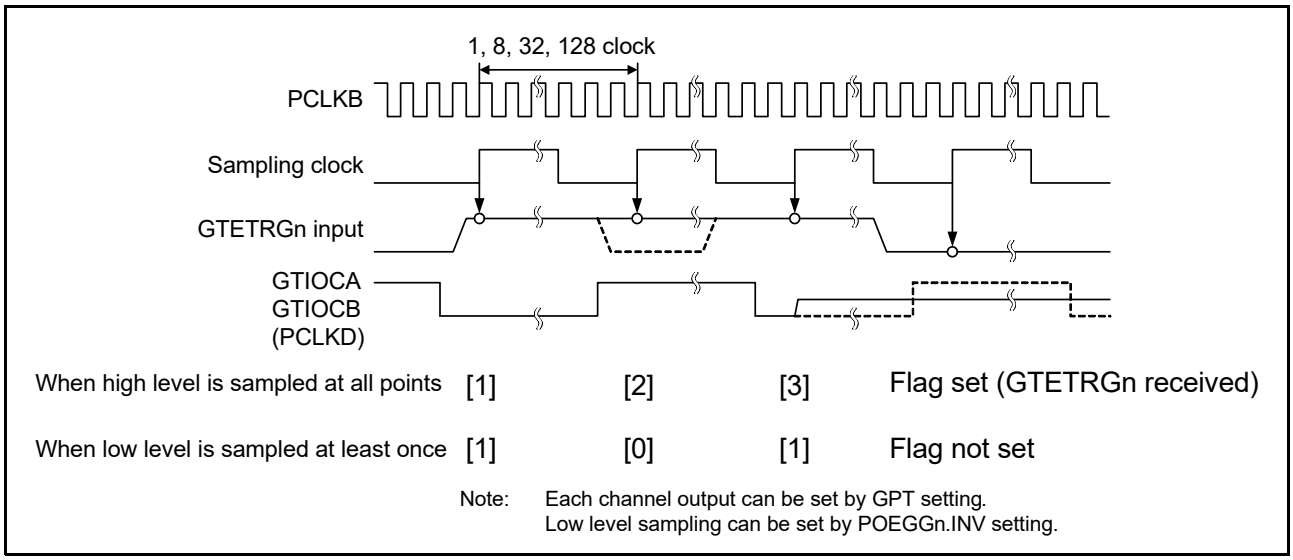


Figure 19.2 Example of digital filter operation

19.3.2 Output-Disable Request from GPT

For details on the operation, see the GTIOC Pin Output Negate Control in section 20, General PWM Timer (GPT).

19.3.3 Comparator Interrupt Detection

If POEGGn.CDRE[2:0] is 1 when a comparator interrupt request is generated, the GPT output pins are placed in output disable state for each group. The status flag is POEGGn.IOCF which is shared with GPT output disable detection.

19.3.4 Output Disable Control on Detection of Stopped Oscillation

When the oscillation stop detection function in the clock generation circuit detects stopped oscillation while POEGGn.OSTPE is 1, the GPT output pins are placed in output disable for each group.

19.3.5 Output Disable Control Using Registers

The GPT output pins can be directly controlled by writing to the software stop flag (POEGGn.SSF).

19.3.6 Release from Output Disable

The GPT output pins that are placed in output disable can be released from that state by either returning them to their initial state with a reset or clearing all of the following:

- POEGGn.PIDF flag
- POEGGn.IOCF flag
- POEGGn.OSTPF flag
- POEGGn.SSF flag.

Writing 0 to the POEGGn.PIDF flag is ignored (the flag is not cleared) if the external input pins GTETRGA and GTETRGB are not disabled and the POEGGn.ST bit is not set to 0.

Writing 0 to the POEGGn.IOCF flag is valid (the flag is cleared) only if all of the GTST.OABHF and GTST.OABLF flags in GPT are set to 0.

Writing 0 to the POEGGn.OSTPF flag is ignored (the flag is not cleared) if the OSTDSR.OSTDF flag in the clock generation circuit is not set to 0. In addition, when the flag set and release occur at the same time, the set takes precedence.

Figure 19.3 shows the released timing from the output disable. The output disable is released at the beginning of the next count cycle of the GPT after the flag is released.

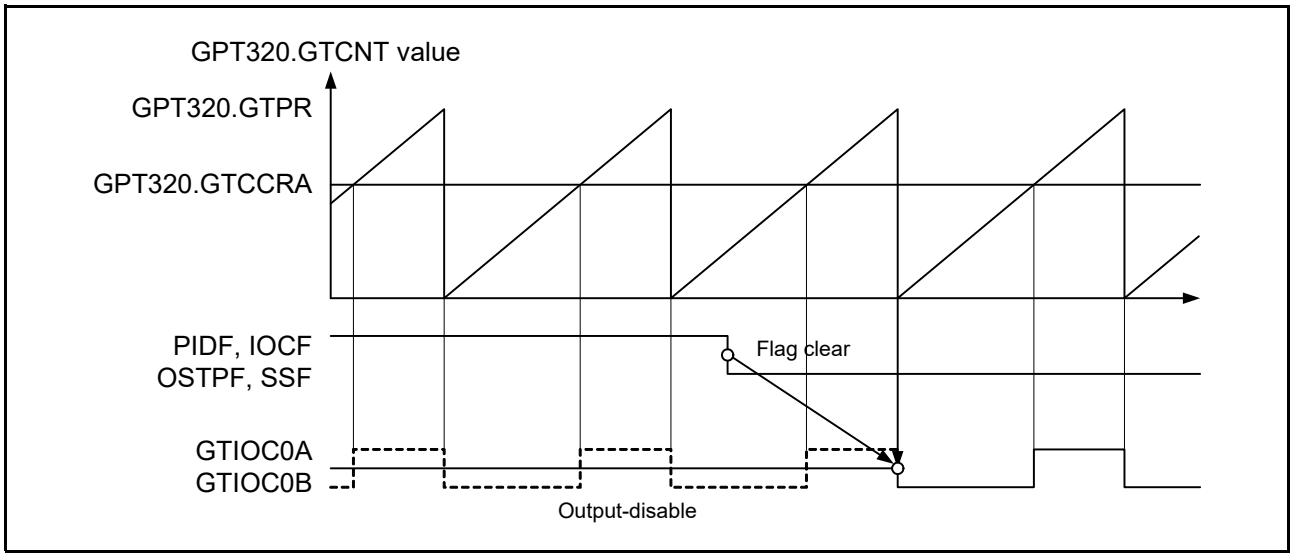


Figure 19.3 Released timing of GPT pin output from output disable

19.4 Interrupt Source

The POEG generates an interrupt request for the following factors:

- the output-disable control by the input level detection
- the output-disable request from GPT or the comparator (ACMPHS) interrupt request detection.

Table 19.3 lists the conditions of interrupt request.

Table 19.3 Interrupt source and condition

Interrupt source	Symbol	Associated flag	Description
POEG group A interrupt	POEG_GROUP0	POEGGA.IOCF	An output-disable request from GPT disable request is generated
			An output-disable request from ACMPHS interrupt is generated
		POEGGA.PIDF	An output-disable request from the GTETRGA pin is generated
POEG group B interrupt	POEG_GROUP1	POEGGB.IOCF	An output-disable request from GPT disable request is generated
			An output-disable request from ACMPHS interrupt is generated
		POEGGB.PIDF	An output-disable request from the GTETRGB pin is generated

19.5 External Trigger Output to GPT

The POEG outputs the GTETRGA and GTETRGB signals as the GPT operation trigger signals for the following:

- count start
- count stop
- count clear
- up-count
- down-count
- input capture.

For the POEGGn.INV polarity setting signal, when the same level is input 3 times continuously with the sampling clock

selected by the POEGGn.NFCS[1:0] and POEGGn.NFEN bits, that value is output. Also, the control register is the same as that of the input level detection operation described in section 19.3.1, Pin Input Level Detection Operation. The state after filtering can be monitored by POEGGn.ST.

Figure 19.4 shows the external trigger output timing to GPT.

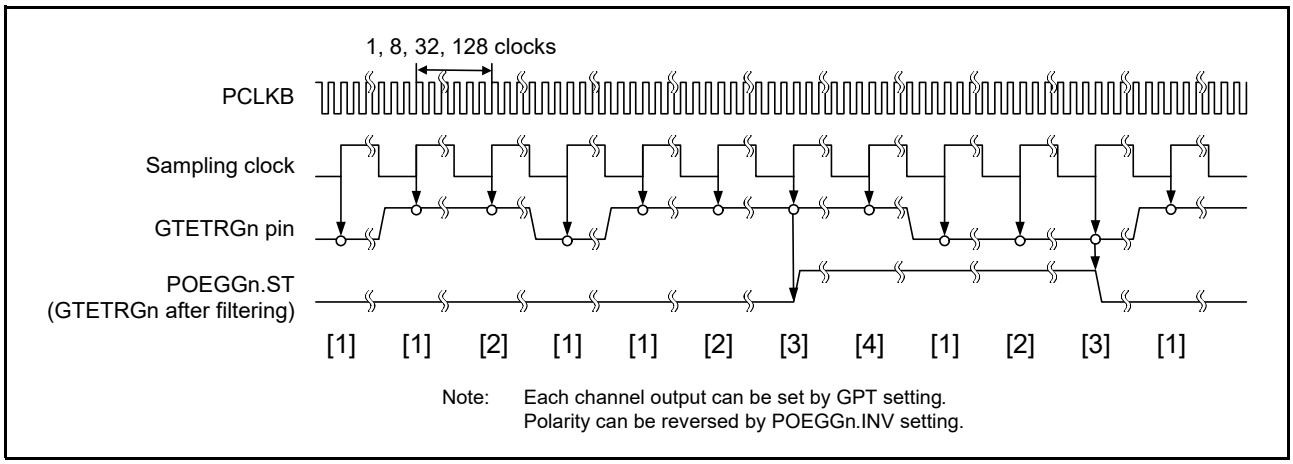


Figure 19.4 External trigger output timing to GPT

19.6 Usage Notes

19.6.1 Transition to Software Standby mode

When the POEG is used, do not transition to Software Standby mode. In this mode, the POEG stops and therefore output disable of the pins cannot be controlled.

19.6.2 Specifying Pins Associated with the GPT

The POEG operates the output disable control only when a pin is associated with the GPT by setting the PmnPFS.PMR and PmnPFS.PSEL bits. When the pin is specified as a general I/O pin, the POEG does not operate the output disable control.

20. General PWM Timer (GPT)

20.1 Overview

The General PWM Timer (GPT) is a 32-bit timer with one GPT32 channel, and a 16-bit timer with three GPT16H channels, and three GPT16 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. The GPT can also be used as a general-purpose timer.

Table 20.1 lists the GPT specifications, Table 20.2 shows the GPT functions, and Figure 20.1 shows a block diagram.

Table 20.1 GPT specifications

Parameter	Description
Functions	• GPT32 (32 bits) × 1 channel, GPT16H (16 bits) × 3 channels, GPT16 (16 bits) × 3 channels • Up-counting or down-counting (saw waves) or up/down-counting (triangle waves) for each counter • Clock sources independently selectable for each channel • Two input/output pins per channel • Two output compare/input capture registers per channel • For the two output compare/input capture registers of each channel, four registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at crests or troughs, enabling the generation of laterally asymmetric PWM waveforms • Registers for setting up frame cycles in each channel (with capability for generating interrupts at overflow or underflow) • Generation of dead times in PWM operation • Synchronous starting, stopping and clearing counters for arbitrary channels • Starting, stopping, clearing and up/down counters in response to a maximum of four ELC events • Starting, stopping, clearing and up/down counters in response to input level comparison • Starting, clearing, stopping and up/down counters in response to a maximum of two external triggers • Output pin disable function by detected short-circuits between output pins • PWM waveform for controlling brushless DC motors can be generated • Compare match A to D event, overflow/underflow event and input UVW edge event can be output to the ELC • Enables the noise filter for input capture and input UVW.

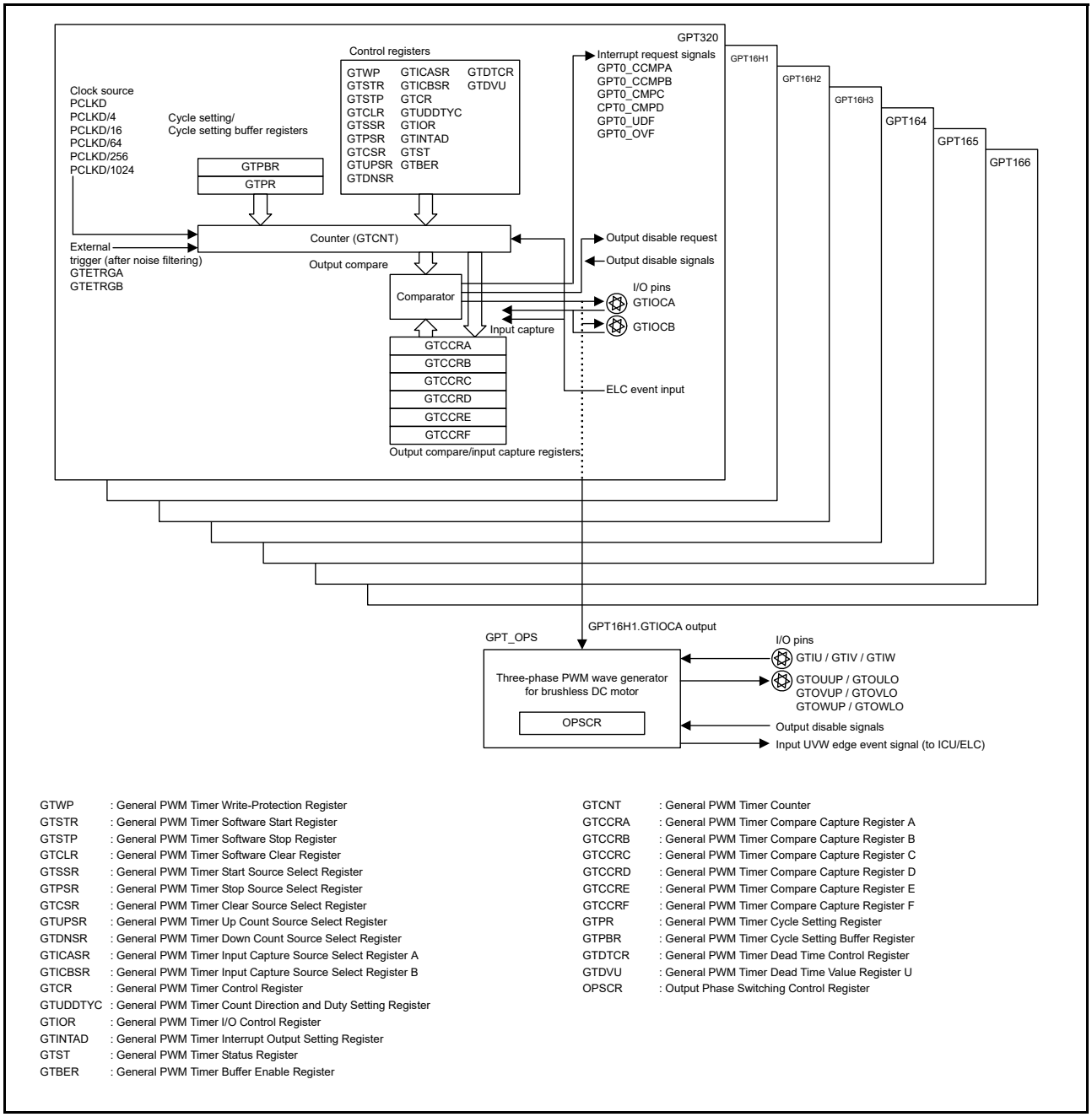
Table 20.2 GPT functions (1 of 2)

Parameter	GPT32, GPT16H, GPT16
Count clock	PCLKD PCLKD/4 PCLKD/16 PCLKD/64 PCLKD/256 PCLKD/1024
Output compare/input capture registers (GTCCR)	GTCCRA GTCCRB
Compare/buffer registers	GTCCRC GTCCRD GTCCRE GTCCRF
Cycle setting register	GTPR
Cycle setting buffer registers	GTPBR
I/O pins	GTIOCA GTIOCB
External trigger input pin*1	GTETRGA GTETRGB
Counter clear sources	GTPR register compare match, input capture, input pin status, ELC event input, and GTETRGn (n= A, B) pin input

Table 20.2 GPT functions (2 of 2)

Parameter		GPT32, GPT16H, GPT16
Compare match output	Low output	Available
	High output	Available
	Toggle output	Available
Input capture function		Available
Automatic addition of dead time		Available (no dead time buffer)
PWM mode		Available
Phase count function		Available
Buffer operation		Double buffer
One-shot operation		Available
DTC activation		All the interrupt sources
Brushless DC motor control function		Available
Interrupt sources		6 sources • GTCCRA compare match/input capture (GPTn_CCMPA) • GTCCRB compare match/input capture (GPTn_CCMPB) • GTCCRC compare match (GPTn_CMPC) • GTCCRD compare match (GPTn_CMPD) • GTCNT overflow (GTPR compare match) (GPTn_OVF) • GTCNT underflow (GPTn_UDF) Note: n = 0 to 6
Event linking (ELC) function		Available
Noise filtering function		Available

Note 1. GTETRGn connects to the POEG module before connecting to the GPT. Therefore, to use the GPT function, supply a clock for POEG by clearing MSTPD bit [14].



GTWP : General PWM Timer Write-Protection Register
GTSTR : General PWM Timer Software Start Register
GTSTP : General PWM Timer Software Stop Register
GTCLR : General PWM Timer Software Clear Register
GTSSR : General PWM Timer Start Source Select Register
GTPSR : General PWM Timer Stop Source Select Register
GTCSR : General PWM Timer Clear Source Select Register
GTUPSR : General PWM Timer Up Count Source Select Register
GTDNSR : General PWM Timer Down Count Source Select Register
GTICASR : General PWM Timer Input Capture Source Select Register A
GTICBSR : General PWM Timer Input Capture Source Select Register B
GTCR : General PWM Timer Control Register
GTUDDTYC : General PWM Timer Count Direction and Duty Setting Register
GTIOR : General PWM Timer I/O Control Register
GTINTAD : General PWM Timer Interrupt Output Setting Register
GTST : General PWM Timer Status Register
GTBER : General PWM Timer Buffer Enable Register
GTCNT : General PWM Timer Counter
GTCCRA : General PWM Timer Compare Capture Register A
GTCCRB : General PWM Timer Compare Capture Register B
GTCCRC : General PWM Timer Compare Capture Register C
GTCCRD : General PWM Timer Compare Capture Register D
GTCCRE : General PWM Timer Compare Capture Register E
GTCCRF : General PWM Timer Compare Capture Register F
GTPR : General PWM Timer Cycle Setting Register
GTPBR : General PWM Timer Cycle Setting Buffer Register
GTDTCR : General PWM Timer Dead Time Control Register
GTDVU : General PWM Timer Dead Time Value Register U
OPSCR : Output Phase Switching Control Register

Figure 20.1 GPT block diagram

Figure 20.2 shows the association between GPT channels and module names.

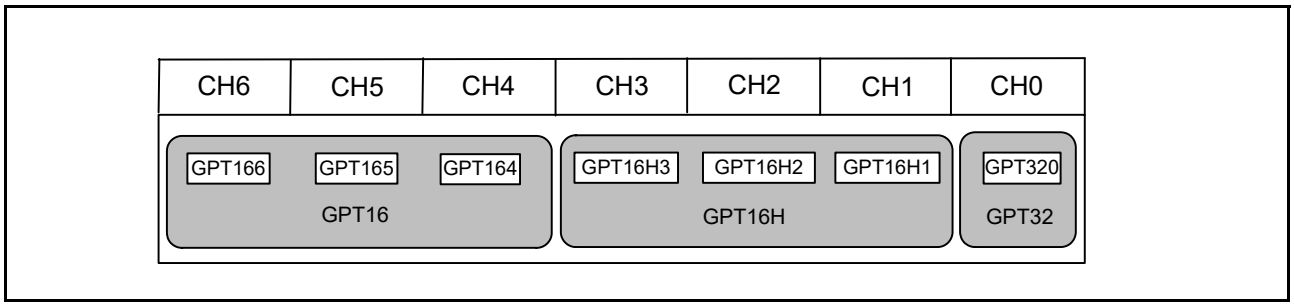


Figure 20.2 Association between GPT channels and module names

Table 20.3 lists the I/O pins used in the GPT.

Table 20.3 I/O pins of GPT

Channel	Pin name	I/O	Function
Common	GTETRGA	Input	External trigger input pin A (After noise filtering)
	GTETRGB	Input	External trigger input pin B (After noise filtering)
GPT320	GTIOC0A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC0B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT16H1	GTIOC1A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC1B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT16H2	GTIOC2A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC2B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT16H3	GTIOC3A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC3B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT164	GTIOC4A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC4B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT165	GTIOC5A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC5B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT166	GTIOC6A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC6B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT_OPS	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	Three-phase PWM output for BLDC motor control (positive U-phase)
	GTOULO	Output	Three-phase PWM output for BLDC motor control (negative U-phase)
	GTOVUP	Output	Three-phase PWM output for BLDC motor control (positive V-phase)
	GTOVLO	Output	Three-phase PWM output for BLDC motor control (negative V-phase)
	GTOWUP	Output	Three-phase PWM output for BLDC motor control (positive W-phase)
	GTOWLO	Output	Three-phase PWM output for BLDC motor control (negative W-phase)

20.2 Register Descriptions

Table 20.4 lists the registers in the GPT.

Table 20.4 GPT registers

Module symbol	Register name	Register symbol	Reset value	Address	Access Size
GPT320, GPT16Hn (n = 1 to 3) GPT16n (n = 4 to 6)	General PWM Timer Write-Protection Register	GTWP	00000000h	4007 8000h + 0100h × m	32
	General PWM Timer Software Start Register	GTSTR	00000000h	4007 8004h + 0100h × m	32
	General PWM Timer Software Stop Register	GTSTP	FFFFFFFFh	4007 8008h + 0100h × m	32
	General PWM Timer Software Clear Register	GTCLR	00000000h	4007 800Ch + 0100h × m	32
	General PWM Timer Start Source Select Register	GTSSR	00000000h	4007 8010h + 0100h × m	32
	General PWM Timer Stop Source Select Register	GTPSR	00000000h	4007 8014h + 0100h × m	32
	General PWM Timer Clear Source Select Register	GTCSR	00000000h	4007 8018h + 0100h × m	32
	General PWM Timer Up Count Source Select Register	GTUPSR	00000000h	4007 801Ch + 0100h × m	32
	General PWM Timer Down Count Source Select Register	GTDNSR	00000000h	4007 8020h + 0100h × m	32
	General PWM Timer Input Capture Source Select Register A	GTICASR	00000000h	4007 8024h + 0100h × m	32
	General PWM Timer Input Capture Source Select Register B	GTICBSR	00000000h	4007 8028h + 0100h × m	32
	General PWM Timer Control Register	GTCR	00000000h	4007 802Ch + 0100h × m	32
	General PWM Timer Count Direction and Duty Setting Register	GTUDDTYC	00000001h	4007 8030h + 0100h × m	32
	General PWM Timer I/O Control Register	GTIOR	00000000h	4007 8034h + 0100h × m	32
	General PWM Timer Interrupt Output Setting Register	GTINTAD	00000000h	4007 8038h + 0100h × m	32
	General PWM Timer Status Register	GTST	00008000h	4007 803Ch + 0100h × m	32
	General PWM Timer Buffer Enable Register	GTBER	00000000h	4007 8040h + 0100h × m	32
	General PWM Timer Counter	GTCNT	00000000h	4007 8048h + 0100h × m	32
	General PWM Timer Compare Capture Register A	GTCCRA	FFFFFFFFh*1	4007 804Ch + 0100h × m	32
	General PWM Timer Compare Capture Register B	GTCCRB	FFFFFFFFh*1	4007 8050h + 0100h × m	32
	General PWM Timer Compare Capture Register C	GTCCRC	FFFFFFFFh*1	4007 8054h + 0100h × m	32
	General PWM Timer Compare Capture Register E	GTCCRE	FFFFFFFFh*1	4007 8058h + 0100h × m	32
	General PWM Timer Compare Capture Register D	GTCCRD	FFFFFFFFh*1	4007 805Ch + 0100h × m	32
	General PWM Timer Compare Capture Register F	GTCCRF	FFFFFFFFh*1	4007 8060h + 0100h × m	32
	General PWM Timer Cycle Setting Register	GTPR	FFFFFFFFh*1	4007 8064h + 0100h × m	32
	General PWM Timer Cycle Setting Buffer Register	GTPBR	FFFFFFFFh*1	4007 8068h + 0100h × m	32
	General PWM Timer Dead Time Control Register	GTDTCR	00000000h	4007 8088h + 0100h × m	32
	General PWM Timer Dead Time Value Register U	GTDVU	FFFFFFFFh*1	4007 808Ch + 0100h × m	32
GPT_OPS	Output Phase Switching Control Register	OPSCR	00000000h	4007 8FF0h	32

m = 0 to 6

Note 1. If the effective size of counter is 16-bit, the reset value is 0000FFFFh.

20.2.1 General PWM Timer Write-Protection Register (GTWP)

Address(es): GPT320.GTWP 4007 8000h
GPT16Hm.GTWP 4007 8000h + 0100h × m (m = 1 to 3)
GPT16m.GTWP 4007 8000h + 0100h × m (m = 4 to 6)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PRKEY[7:0]								—	—	—	—	—	—	—	WP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	WP	Register Write Disable	0: Write to the register is enabled 1: Write to the register is disabled.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	PRKEY[7:0]	GTWP Key Code	When A5h is written to these bits, write to the WP bit is permitted. These bits are read as 0.	R/W
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

GTWP enables or disables writing to the registers to prevent accidental modification. The following is a list of write enabled or disabled registers:

GTSSR, GTPSR, GTCSR, GTUPSR, GTDNSR, GTICASR, GTICBSR, GTCR, GTUDDTYC, GTIOR, GTINTAD, GTST, GTBER, GTCNT, GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, GTCCRF, GTPR, GTPBR, GTDTCR, GTDVU.

20.2.2 General PWM Timer Software Start Register (GTSTR)

Address(es): GPT320.GTSTR 4007 8004h
GPT16Hm.GTSTR 4007 8004h + 0100h × m (m = 1 to 3)
GPT16m.GTSTR 4007 8004h + 0100h × m (m = 4 to 6)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	CSTRT 6	CSTRT 5	CSTRT 4	CSTRT 3	CSTRT 2	CSTRT 1	CSTRT 0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GTSTR starts the GTCNT counter operation for each channel n (n = 0 to 6).

The GTSTR bit number represents the channel number. The GTSTR register for each channel is common. The GTCNT counter starts for the associated channel that corresponds to the GTSTR bit number where 1 is written. Writing 0 has no effect on the status of GTCNT counter and the value of GTSTR register.

For the association between GTSTR bit number and channel number, see Figure 20.2.

CSTRTn bit (Channel n GTCNT Count Start) (n = 0 to 6)

The CSTRTn bit starts channel n of the GTCNT counter operation. Writing to GTSTR.CSTRTn bit (n = 0 to 6) has no effect unless GPTm.GTSSR.CSTRT bit is set to 1 (for GPT32, m = 320, for GPT16H, m = 16H1 to 16H3, for GPT16, m = 164 to 166).

The read data shows the counter status of each channel (GTCR.CST bit). Zero means the counter stops and 1 means the

counter is running.

20.2.3 General PWM Timer Software Stop Register (GTSTP)

Address(es): GPT320.GTSTP 4007 8008h
GPT16Hm.GTSTP 4007 8008h + 0100h × m (m = 1 to 3)
GPT16m.GTSTP 4007 8008h + 0100h × m (m = 4 to 6)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	CSTOP 6	CSTOP 5	CSTOP 4	CSTOP 3	CSTOP 2	CSTOP 1	CSTOP 0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GTSTP stops the GTCNT counter operation for each channel n (n = 0 to 6).

The GTSTP bit number represents the channel number. The GTSTP register of each channel is common. The GTCNT counter stops for the channel associated with the GTSTP bit number where 1 is written. Writing 0 has no effect on the status of GTCNT counter and the value of GTSTP register.

For the association between GTSTP bit number and a channel number, see Figure 20.2.

CSTOPn bit (Channel n GTCNT Count Stop) (n = 0 to 6)

The CSTOPn bit stops channel n of the GTCNT counter operation. Writing to GTSTP.CSTOPn bit (n = 0 to 6) has no effect unless GPTm.GTPSR.CSTOP bit is set to 1 (for GPT32, m = 320, for GPT16H, m = 16H1 to 16H3, for GPT16, m = 164 to 166).

The read data shows the counter status of each channel (invert of GTCR.CST bit). Zero means the counter is running and 1 means the counter stops.

20.2.4 General PWM Timer Software Clear Register (GTCLR)

Address(es): GPT320.GTCLR 4007 800Ch
GPT16Hm.GTCLR 4007 800Ch + 0100h × m (m = 1 to 3)
GPT16m.GTCLR 4007 800Ch + 0100h × m (m = 4 to 6)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	CCLR 6	CCLR 5	CCLR 4	CCLR 3	CCLR 2	CCLR 1	CCLR 0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GTCLR is a write-only register and clears the GTCNT counter operation for each channel n (n = 0 to 6).

The GTCLR bit number represents the channel number. The GTCLR register for each channel is common. The GTCNT counter is cleared for the channel associated with the GTCLR bit number where 1 is written. Writing 0 has no effect on the status of GTCNT counter.

For the association between GTCLR bit number and a channel number, see Figure 20.2.

CCLRn bit (Channel n GTCNT Count Clear) (n = 0 to 6)

Channel n of the GTCNT counter value is cleared on writing 1 to this bit. This bit is read as 0.

20.2.5 General PWM Timer Start Source Select Register (GTSSR)

Address(es): GPT320.GTSSR 4007 8010h
GPT16Hm.GTSSR 4007 8010h + 0100h × m (m = 1 to 3)
GPT16m.GTSSR 4007 8010h + 0100h × m (m = 4 to 6)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CSTRT	—	—	—	—	—	—	—	—	—	—	—	SSELCD	SSELCC	SSELCB	SSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SSCBFAH	SSCBFAL	SSCBRAH	SSCBRAL	SSCAFBH	SSCAFBL	SSCARBH	SSCARBL	—	—	—	—	SSGTRGBF	SSGTRGBR	SSGTRGAF	SSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SSGTRGAR	GTETRGA Pin Rising Input Source Counter Start Enable	0: Disable counter start on the rising edge of GTETRGA input 1: Enable counter start on the rising edge of GTETRGA input.	R/W
b1	SSGTRGAF	GTETRGA Pin Falling Input Source Counter Start Enable	0: Disable counter start on the falling edge of GTETRGA input 1: Enable counter start on the falling edge of GTETRGA input.	R/W
b2	SSGTRGBR	GTETRGB Pin Rising Input Source Counter Start Enable	0: Disable counter start on the rising edge of GTETRGB input 1: Enable counter start on the rising edge of GTETRGB input.	R/W
b3	SSGTRGBF	GTETRGB Pin Falling Input Source Counter Start Enable	0: Disable counter start on the falling edge of GTETRGB input 1: Enable counter start on the falling edge of GTETRGB input.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	SSCARBL	GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Start Enable	0: Disable counter start on the rising edge of GTIOCA input when GTIOCB input is 0 1: Enable counter start on the rising edge of GTIOCA input when GTIOCB input is 0.	R/W
b9	SSCARBH	GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Start Enable	0: Disable counter start on the rising edge of GTIOCA input when GTIOCB input is 1 1: Enable counter start on the rising edge of GTIOCA input when GTIOCB input is 1.	R/W
b10	SSCAFBL	GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Start Enable	0: Disable counter start on the falling edge of GTIOCA input when GTIOCB input is 0 1: Enable counter start on the falling edge of GTIOCA input when GTIOCB input is 0.	R/W
b11	SSCAFBH	GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Start Enable	0: Disable counter start on the falling edge of GTIOCA input when GTIOCB input is 1 1: Enable counter start on the falling edge of GTIOCA input when GTIOCB input is 1.	R/W
b12	SSCBRAL	GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Start Enable	0: Disable counter start on the rising edge of GTIOCB input when GTIOCA input is 0 1: Enable counter start on the rising edge of GTIOCB input when GTIOCA input is 0.	R/W
b13	SSCBRAH	GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Start Enable	0: Disable counter start on the rising edge of GTIOCB input when GTIOCA input is 1 1: Enable counter start on the rising edge of GTIOCB input when GTIOCA input is 1.	R/W

Bit	Symbol	Bit name	Description	R/W
b14	SSCBFAL	GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Start Enable	0: Disable counter start on the falling edge of GTIOCB input when GTIOCA input is 0 1: Enable counter start on the falling edge of GTIOCB input when GTIOCA input is 0.	R/W
b15	SSCBFAH	GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Start Enable	0: Disable counter start on the falling edge of GTIOCB input when GTIOCA input is 1 1: Enable counter start on the falling edge of GTIOCB input when GTIOCA input is 1.	R/W
b16	SSELCA	ELC_GPTA Event Source Counter Start Enable	0: Disable counter start on the ELC_GPTA event input 1: Enable counter start on the ELC_GPTA event input.	R/W
b17	SSELCB	ELC_GPTB Event Source Counter Start Enable	0: Disable counter start on the ELC_GPTB event input 1: Enable counter start on the ELC_GPTB event input.	R/W
b18	SSELCC	ELC_GPTC Event Source Counter Start Enable	0: Disable counter start on the ELC_GPTC event input 1: Enable counter start on the ELC_GPTC event input.	R/W
b19	SSELCD	ELC_GPTD Event Source Counter Start Enable	0: Disable counter start on the ELC_GPTD event input 1: Enable counter start on the ELC_GPTD event input.	R/W
b30 to b20	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b31	CSTRT	Software Source Counter Start Enable	0: Disable counter start by the GTSTR register 1: Enable counter start by the GTSTR register.	R/W

GTSSR sets the source to start the GTCNT counter.

SSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Start Enable)

The SSGTRGAR bit enables or disables GTCNT counter start on the rising edge of the GTETRGA pin input.

SSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Start Enable)

The SSGTRGAF bit enables or disables GTCNT counter start on the falling edge of the GTETRGA pin input.

SSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Start Enable)

The SSGTRGBR bit enables or disables GTCNT counter start on the rising edge of the GTETRGB pin input.

SSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Start Enable)

The SSGTRGBF bit enables or disables GTCNT counter start on the falling edge of the GTETRGB pin input.

SSCARBL bit (GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Start Enable)

The SSCARBL bit enables or disables GTCNT counter start on the rising edge of the GTIOCA pin input, when the GTIOCB input is 0.

SSCARBH bit (GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Start Enable)

The SSCARBH bit enables or disables GTCNT counter start on the rising edge of the GTIOCA pin input, when the GTIOCB input is 1.

SSCAFBL bit (GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Start Enable)

The SSCAFBL bit enables or disables GTCNT counter start on the falling edge of the GTIOCA pin input, when the GTIOCB input is 0.

SSCAFBH bit (GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Start Enable)

The SSCAFBH bit enables or disables GTCNT counter start on the falling edge of the GTIOCA pin input, when the GTIOCB input is 1.

SSCBRAL bit (GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Start Enable)

The SSCBRAL bit enables or disables GTCNT counter start on the rising edge of the GTIOCB pin input, when the GTIOCA input is 0.

SSCBRAH bit (GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Start Enable)

The SSCBRAH bit enables or disables GTCNT counter start on the rising edge of the GTIOCB pin input, when the GTIOCA input is 1.

SSCBFAL bit (GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Start Enable)

The SSCBFAL bit enables or disables GTCNT counter start on the falling edge of the GTIOCB pin input, when the GTIOCA input is 0.

SSCBFAH bit (GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Start Enable)

The SSCBFAH bit enables or disables GTCNT counter start on the falling edge of the GTIOCB pin input, when the GTIOCA input is 1.

SSELCm bit (ELC_GPTm Event Source Counter Start Enable) (m = A to D)

The SSELCm bit enables or disables GTCNT counter start at the ELC_GPTm event input.

CSTRT bit (Software Source Counter Start Enable)

The CSTRT bit enables or disables GTCNT counter start by GTSTR register.

20.2.6 General PWM Timer Stop Source Select Register (GTPSR)

Address(es): GPT320.GTPSR 4007 8014h
GPT16Hm.GTPSR 4007 8014h + 0100h × m (m = 1 to 3)
GPT16m.GTPSR 4007 8014h + 0100h × m (m = 4 to 6)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CSTOP	—	—	—	—	—	—	—	—	—	—	—	PSELCD	PSELCC	PSELCB	PSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PSCBFAH	PSCBFAL	PSCBRAH	PSCBRAL	PSCAFBH	PSCAFBL	PSCARBH	PSCARBL	—	—	—	—	PSGTRGBF	PSGTRGBR	PSGTRGAF	PSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PSGTRGAR	GTETRGA Pin Rising Input Source Counter Stop Enable	0: Disable counter stop on the rising edge of GTETRGA input 1: Enable counter stop on the rising edge of GTETRGA input.	R/W
b1	PSGTRGAF	GTETRGA Pin Falling Input Source Counter Stop Enable	0: Disable counter stop on the falling edge of GTETRGA input 1: Enable counter stop on the falling edge of GTETRGA input.	R/W
b2	PSGTRGBR	GTETRGB Pin Rising Input Source Counter Stop Enable	0: Disable counter stop on the rising edge of GTETRGB input 1: Enable counter stop on the rising edge of GTETRGB input.	R/W
b3	PSGTRGBF	GTETRGB Pin Falling Input Source Counter Stop Enable	0: Disable counter stop on the falling edge of GTETRGB input 1: Enable counter stop on the falling edge of GTETRGB input.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	PSCARBL	GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Stop Enable	0: Disable counter stop on the rising edge of GTIOCA input when GTIOCB input is 0 1: Enable counter stop on the rising edge of GTIOCA input when GTIOCB input is 0.	R/W

Bit	Symbol	Bit name	Description	R/W
b9	PSCARBH	GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Stop Enable	0: Disable counter stop on the rising edge of GTIOCA input when GTIOCB input is 1 1: Enable counter stop on the rising edge of GTIOCA input when GTIOCB input is 1.	R/W
b10	PSCAFBL	GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Stop Enable	0: Disable counter stop on the falling edge of GTIOCA input when GTIOCB input is 0 1: Enable counter stop on the falling edge of GTIOCA input when GTIOCB input is 0.	R/W
b11	PSCAFBH	GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Stop Enable	0: Disable counter stop on the falling edge of GTIOCA input when GTIOCB input is 1 1: Enable counter stop on the falling edge of GTIOCA input when GTIOCB input is 1.	R/W
b12	PSCBRAL	GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Stop Enable	0: Disable counter stop on the rising edge of GTIOCB input when GTIOCA input is 0 1: Enable counter stop on the rising edge of GTIOCB input when GTIOCA input is 0.	R/W
b13	PSCBRAH	GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Stop Enable	0: Disable counter stop on the rising edge of GTIOCB input when GTIOCA input is 1 1: Enable counter stop on the rising edge of GTIOCB input when GTIOCA input is 1.	R/W
b14	PSCBFAL	GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Stop Enable	0: Disable counter stop on the falling edge of GTIOCB input when GTIOCA input is 0 1: Enable counter stop on the falling edge of GTIOCB input when GTIOCA input is 0.	R/W
b15	PSCBFAH	GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Stop Enable	0: Disable counter stop disabled on the falling edge of GTIOCB input when GTIOCA input is 1 1: Counter stop is enabled on the falling edge of GTIOCB input when GTIOCA input is 1.	R/W
b16	PSELCA	ELC_GPTA Event Source Counter Stop Enable	0: Disable counter stop at the ELC_GPTA event input 1: Enable counter stop at the ELC_GPTA event input.	R/W
b17	PSELCB	ELC_GPTB Event Source Counter Stop Enable	0: Disable counter stop at the ELC_GPTB event input 1: Enable counter stop at the ELC_GPTB event input.	R/W
b18	PSELCC	ELC_GPTC Event Source Counter Stop Enable	0: Disable counter stop at the ELC_GPTC event input 1: Enable counter stop at the ELC_GPTC event input.	R/W
b19	PSELCD	ELC_GPTD Event Source Counter Stop Enable	0: Disable counter stop at the ELC_GPTD event input 1: Enable counter stop at the ELC_GPTD event input.	R/W
b30 to b20	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b31	CSTOP	Software Source Counter Stop Enable	0: Disable counter stop by the GTSTP register 1: Enable counter stop by the GTSTP register.	R/W

GTPSR sets the source to stop the GTCNT counter.

PSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Stop Enable)

The PSGTRGAR bit enables or disables the GTCNT counter stop on the rising edge of the GTETRGA pin input.

PSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Stop Enable)

The PSGTRGAF bit enables or disables the GTCNT counter stop on the falling edge of the GTETRGA pin input.

PSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Stop Enable)

The PSGTRGBR bit enables or disables the GTCNT counter stop on the rising edge of the GTETRGB pin input.

PSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Stop Enable)

The PSGTRGBF bit enables or disables the GTCNT counter stop on the falling edge of the GTETRGB pin input.

PSCARBL bit (GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Stop Enable)

The PSCARBL bit enables or disables the GTCNT counter stop on the rising edge of the GTIOCA pin input, when the GTIOCB input is 0.

PSCARBH bit (GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Stop Enable)

The PSCARBH bit enables or disables the GTCNT counter stop on the rising edge of the GTIOCA pin input, when the GTIOCB input is 1.

PSCAFBL bit (GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Stop Enable)

The PSCAFBL bit enables or disables the GTCNT counter stop on the falling edge of the GTIOCA pin input, when the GTIOCB input is 0.

PSCAFBH bit (GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Stop Enable)

The PSCAFBH bit enables or disables the GTCNT counter stop on the falling edge of the GTIOCA pin input, when the GTIOCB input is 1.

PSCBRAL bit (GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Stop Enable)

The PSCBRAL bit enables or disables the GTCNT counter stop on the rising edge of the GTIOCB pin input, when the GTIOCA input is 0.

PSCBRAH bit (GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Stop Enable)

The PSCBRAH bit enables or disables the GTCNT counter stop on the rising edge of the GTIOCB pin input, when the GTIOCA input is 1.

PSCBFAL bit (GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Stop Enable)

The PSCBFAL bit enables or disables the GTCNT counter stop on the falling edge of the GTIOCB pin input, when the GTIOCA input is 0.

PSCBFAH bit (GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Stop Enable)

The PSCBFAH bit enables or disables the GTCNT counter stop on the falling edge of the GTIOCB pin input, when the GTIOCA input is 1.

PSELCm bit (ELC_GPTm Event Source Counter Stop Enable) (m = A to D)

The PSELCm bit enables or disables the GTCNT counter stop at the ELC_GPTm event input.

CSTOP bit (Software Source Counter Stop Enable)

The CSTOP bit enables or disables the GTCNT counter stop by the GTSTP register.

20.2.7 General PWM Timer Clear Source Select Register (GTCSR)

Address(es): GPT320.GTCSR 4007 8018h
GPT16Hm.GTCSR 4007 8018h + 0100h × m (m = 1 to 3)
GPT16m.GTCSR 4007 8018h + 0100h × m (m = 4 to 6)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CCLR	—	—	—	—	—	—	—	—	—	—	—	CSELCD	CSELCC	CSELCB	CSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CSCBFAH	CSCBFAL	CSCBRAH	CSCBRAL	CSCAFBH	CSCAFBL	CSCARBH	CSCARBL	—	—	—	—	CSGTRGBF	CSGTRGBR	CSGTRGAF	CSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CSGTRGAR	GTETRGA Pin Rising Input Source Counter Clear Enable	0: Disable counter clear on the rising edge of GTETRGA input 1: Enable counter clear on the rising edge of GTETRGA input.	R/W

Bit	Symbol	Bit name	Description	R/W
b1	CSGTRGAF	GTETRGA Pin Falling Input Source Counter Clear Enable	0: Disable counter clear on the falling edge of GTETRGA input 1: Enable counter clear on the falling edge of GTETRGA input.	R/W
b2	CSGTRGBR	GTETRGB Pin Rising Input Source Counter Clear Enable	0: Disable counter clear on the rising edge of GTETRGB input 1: Enable counter clear on the rising edge of GTETRGB input.	R/W
b3	CSGTRGBF	GTETRGB Pin Falling Input Source Counter Clear Enable	0: Disable counter clear on the falling edge of GTETRGB input 1: Enable counter clear on the falling edge of GTETRGB input.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	CSCARBL	GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Clear Enable	0: Disable counter clear on the rising edge of GTIOCA input when GTIOCB input is 0 1: Enable counter clear on the rising edge of GTIOCA input when GTIOCB input is 0.	R/W
b9	CSCARBH	GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Clear Enable	0: Disable counter clear on the rising edge of GTIOCA input when GTIOCB input is 1 1: Enable counter clear on the rising edge of GTIOCA input when GTIOCB input is 1.	R/W
b10	CSCAFBL	GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Clear Enable	0: Disable counter clear on the falling edge of GTIOCA input when GTIOCB input is 0 1: Enable counter clear on the falling edge of GTIOCA input when GTIOCB input is 0.	R/W
b11	CSCAFBH	GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Clear Enable	0: Disable counter clear on the falling edge of GTIOCA input when GTIOCB input is 1 1: Enable counter clear on the falling edge of GTIOCA input when GTIOCB input is 1.	R/W
b12	CSCBRAL	GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Clear Enable	0: Disable counter clear on the rising edge of GTIOCB input when GTIOCA input is 0 1: Enable counter clear on the rising edge of GTIOCB input when GTIOCA input is 0.	R/W
b13	CSCBRAH	GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Clear Enable	0: Disable counter clear on the rising edge of GTIOCB input when GTIOCA input is 1 1: Enable counter clear on the rising edge of GTIOCB input when GTIOCA input is 1.	R/W
b14	CSCBFAL	GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Clear Enable	0: Disable counter clear on the falling edge of GTIOCB input when GTIOCA input is 0 1: Enable counter clear on the falling edge of GTIOCB input when GTIOCA input is 0.	R/W
b15	CSCBFAH	GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Clear Enable	0: Disable counter clear on the falling edge of GTIOCB input when GTIOCA input is 1 1: Enable counter clear on the falling edge of GTIOCB input when GTIOCA input is 1.	R/W
b16	CSELCA	ELC_GPTA Event Source Counter Clear Enable	0: Disable counter clear at the ELC_GPTA event input 1: Enable counter clear at the ELC_GPTA event input.	R/W
b17	CSELCB	ELC_GPTB Event Source Counter Clear Enable	0: Disable counter clear at the ELC_GPTB event input 1: Enable counter clear at the ELC_GPTB event input.	R/W
b18	CSELCC	ELC_GPTC Event Source Counter Clear Enable	0: Disable counter clear at the ELC_GPTC event input 1: Enable counter clear at the ELC_GPTC event input.	R/W
b19	CSELCD	ELC_GPTD Event Source Counter Clear Enable	0: Disable counter clear at the ELC_GPTD event input 1: Enable counter clear at the ELC_GPTD event input.	R/W
b30 to b20	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b31	CCLR	Software Source Counter Clear Enable	0: Disable counter clear by the GTCLR register 1: Enable counter clear by the GTCLR register.	R/W

GTCSR sets the source to clear the GTCNT counter.

CSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Clear Enable)

The CSGTRGAR bit enables or disables the GTCNT counter clear on the rising edge of the GTETRGA pin input.

CSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Clear Enable)

The CSGTRGAF bit enables or disables the GTCNT counter clear on the falling edge of the GTETRGA pin input.

CSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Clear Enable)

The CSGTRGBR bit enables or disables the GTCNT counter clear on the rising edge of the GTETRGB pin input.

CSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Clear Enable)

The CSGTRGBF bit enables or disables the GTCNT counter clear on the falling edge of the GTETRGB pin input.

CSCARBL bit (GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Clear Enable)

The CSCARBL bit enables or disables the GTCNT counter clear on the rising edge of the GTIOCA pin input, when the GTIOCB input is 0.

CSCARBH bit (GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Clear Enable)

The CSCARBH bit enables or disables the GTCNT counter clear on the rising edge of the GTIOCA pin input, when the GTIOCB input is 1.

CSCAFBL bit (GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Clear Enable)

The CSCAFBL bit enables or disables the GTCNT counter clear on the falling edge of the GTIOCA pin input, when the GTIOCB input is 0.

CSCAFBH bit (GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Clear Enable)

The CSCAFBH bit enables or disables the GTCNT counter clear on the falling edge of the GTIOCA pin input, when the GTIOCB input is 1.

CSCBRAL bit (GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Clear Enable)

The CSCBRAL bit enables or disables the GTCNT counter clear on the rising edge of the GTIOCB pin input, when the GTIOCA input is 0.

CSCBRAH bit (GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Clear Enable)

The CSCBRAH bit enables or disables the GTCNT counter clear on the rising edge of the GTIOCB pin input, when the GTIOCA input is 1.

CSCBFAL bit (GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Clear Enable)

The CSCBFAL bit enables or disables the GTCNT counter clear on the falling edge of the GTIOCB pin input, when the GTIOCA input is 0.

CSCBFAH bit (GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Clear Enable)

The CSCBFAH bit enables or disables the GTCNT counter clear on the falling edge of the GTIOCB pin input, when the GTIOCA input is 1.

CSELCm bit (ELC_GPTm Event Source Counter Clear Enable) (m = A to D)

The CSELCm bit enables or disables the GTCNT counter clear at the ELC_GPTm event input.

CCLR bit (Software Source Counter Clear Enable)

The CCLR bit enables or disables the GTCNT counter clear by the GTCLR register.

20.2.8 General PWM Timer Up Count Source Select Register (GTUPSR)

Address(es): GPT320.GTUPSR 4007 801Ch
GPT16Hm.GTUPSR 4007 801Ch + 0100h × m (m = 1 to 3)
GPT16m.GTUPSR 4007 801Ch + 0100h × m (m = 4 to 6)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	USELCD	USELCC	USELCB	USELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	USCBFAH	USCBFAL	USCBRAH	USCBRAL	USCAFBH	USCAFBL	USCARBH	USCARBL	—	—	—	—	USGTRGBF	USGTRGBR	USGTRGAF	USGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	USGTRGAR	GTETRGA Pin Rising Input Source Counter Count Up Enable	0: Disable counter count up on the rising edge of GTETRGA input 1: Enable counter count up on the rising edge of GTETRGA input.	R/W
b1	USGTRGAF	GTETRGA Pin Falling Input Source Counter Count Up Enable	0: Disable counter count up on the falling edge of GTETRGA input 1: Enable counter count up on the falling edge of GTETRGA input.	R/W
b2	USGTRGBR	GTETRGB Pin Rising Input Source Counter Count Up Enable	0: Disable counter count up on the rising edge of GTETRGB input 1: Enable counter count up on the rising edge of GTETRGB input.	R/W
b3	USGTRGBF	GTETRGB Pin Falling Input Source Counter Count Up Enable	0: Disable counter count up on the falling edge of GTETRGB input 1: Enable counter count up on the falling edge of GTETRGB input.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	USCARBL	GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Count Up Enable	0: Disable counter count up on the rising edge of GTIOCA input when GTIOCB input is 0 1: Enable counter count up on the rising edge of GTIOCA input when GTIOCB input is 0.	R/W
b9	USCARBH	GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Count Up Enable	0: Disable counter count up on the rising edge of GTIOCA input when GTIOCB input is 1 1: Enable counter count up on the rising edge of GTIOCA input when GTIOCB input is 1.	R/W
b10	USCAFBL	GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Count Up Enable	0: Disable counter count up on the falling edge of GTIOCA input when GTIOCB input is 0 1: Enable counter count up on the falling edge of GTIOCA input when GTIOCB input is 0.	R/W
b11	USCAFBH	GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Count Up Enable	0: Disable counter count up on the falling edge of GTIOCA input when GTIOCB input is 1 1: Enable counter count up on the falling edge of GTIOCA input when GTIOCB input is 1.	R/W
b12	USCBRAL	GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Count Up Enable	0: Disable counter count up on the rising edge of GTIOCB input when GTIOCA input is 0 1: Enable counter count up on the rising edge of GTIOCB input when GTIOCA input is 0.	R/W
b13	USCBRAH	GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Count Up Enable	0: Disable counter count up on the rising edge of GTIOCB input when GTIOCA input is 1 1: Enable counter count up on the rising edge of GTIOCB input when GTIOCA input is 1.	R/W

Bit	Symbol	Bit name	Description	R/W
b14	USCBFAL	GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Count Up Enable	0: Disable counter count up on the falling edge of GTIOCB input when GTIOCA input is 0 1: Enable counter count up on the falling edge of GTIOCB input when GTIOCA input is 0.	R/W
b15	USCBFAH	GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Count Up Enable	0: Disable counter count up on the falling edge of GTIOCB input when GTIOCA input is 1 1: Enable counter count up on the falling edge of GTIOCB input when GTIOCA input is 1.	R/W
b16	USELCA	ELC_GPTA Event Source Counter Count Up Enable	0: Disable counter count up at the ELC_GPTA event input 1: Enable counter count up at the ELC_GPTA event input.	R/W
b17	USELCB	ELC_GPTB Event Source Counter Count Up Enable	0: Disable counter count up at the ELC_GPTB event input 1: Enable counter count up at the ELC_GPTB event input.	R/W
b18	USELCC	ELC_GPTC Event Source Counter Count Up Enable	0: Disable counter count up at the ELC_GPTC event input 1: Enable counter count up at the ELC_GPTC event input.	R/W
b19	USELCD	ELC_GPTD Event Source Counter Count Up Enable	0: Disable counter count up at the ELC_GPTD event input 1: Enable counter count up at the ELC_GPTD event input.	R/W
b31 to b20	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

When at least one bit in the GTUPSR register is set to 1, the GTCNT counter is counted up by the source that is set to 1 in this register. In this case, GTCR.TPCS has no effect.

USGTRGAR bit (GTETRGA Pin Rising Input Source Counter Count Up Enable)

The USGTRGAR bit enables or disables the GTCNT counter count up on the rising edge of the GTETRGA pin input.

USGTRGAF bit (GTETRGA Pin Falling Input Source Counter Count Up Enable)

The USGTRGAF bit enables or disables the GTCNT counter count up on the falling edge of the GTETRGA pin input.

USGTRGBR bit (GTETRGB Pin Rising Input Source Counter Count Up Enable)

The USGTRGBR bit enables or disables the GTCNT counter count up on the rising edge of the GTETRGB pin input.

USGTRGBF bit (GTETRGB Pin Falling Input Source Counter Count Up Enable)

The USGTRGBF bit enables or disables the GTCNT counter count up on the falling edge of the GTETRGB pin input.

USCARBL bit (GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Count Up Enable)

The USCARBL bit enables or disables GTCNT counter count up on the rising edge of GTIOCA pin input, when GTIOCB input is 0.

USCARBH bit (GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Count Up Enable)

The USCARBH bit enables or disables the GTCNT counter count up on the rising edge of the GTIOCA pin input, when the GTIOCB input is 1.

USCAFBL bit (GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Count Up Enable)

The USCAFBL bit enables or disables the GTCNT counter count up on the falling edge of the GTIOCA pin input, when the GTIOCB input is 0.

USCAFBH bit (GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Count Up Enable)

The USCAFBH bit enables or disables the GTCNT counter count up on the falling edge of the GTIOCA pin input, when the GTIOCB input is 1.

USCBRAL bit (GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Count Up Enable)

The USCBRAL bit enables or disables the GTCNT counter count up on the rising edge of the GTIOCB pin input, when the GTIOCA input is 0.

USCBRAH bit (GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Count Up Enable)

The USCBRAH bit enables or disables the GTCNT counter count up on the rising edge of the GTIOCB pin input, when the GTIOCA input is 1.

USCBFAL bit (GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Count Up Enable)

The USCBFAL bit enables or disables the GTCNT counter count up on the falling edge of the GTIOCB pin input, when the GTIOCA input is 0.

USCBFAH bit (GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Count Up Enable)

The USCBFAH bit enables or disables the GTCNT counter count up on the falling edge of the GTIOCB pin input, when the GTIOCA input is 1.

USELCm bit (ELC_GPTm Event Source Counter Count Up Enable) (m = A to D)

The USELCm bit enables or disables the GTCNT counter count up at the ELC_GPTm event input.

20.2.9 General PWM Timer Down Count Source Select Register (GTDNSR)

Address(es): GPT320.GTDNSR 4007 8020h
GPT16Hm.GTDNSR 4007 8020h + 0100h × m (m = 1 to 3)
GPT16m.GTDNSR 4007 8020h + 0100h × m (m = 4 to 6)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	DSELCD	DSELCC	DSELCB	DSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DSCBFAH	DSCBFAL	DSCBRAH	DSCBRAL	DSCAFBH	DSCAFBL	DSCARBH	DSCARBL	—	—	—	—	DSGTRGBF	DSGTRGBR	DSGTRGAF	DSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DSGTRGAR	GTETRGA Pin Rising Input Source Counter Count Down Enable	0: Disable counter count down on the rising edge of GTETRGA input 1: Enable counter count down on the rising edge of GTETRGA input.	R/W
b1	DSGTRGAF	GTETRGA Pin Falling Input Source Counter Count Down Enable	0: Disable counter count down on the falling edge of GTETRGA input 1: Enable counter count down on the falling edge of GTETRGA input.	R/W
b2	DSGTRGBR	GTETRGB Pin Rising Input Source Counter Count Down Enable	0: Disable counter count down on the rising edge of GTETRGB input 1: Enable counter count down on the rising edge of GTETRGB input.	R/W
b3	DSGTRGBF	GTETRGB Pin Falling Input Source Counter Count Down Enable	0: Disable counter count down on the falling edge of GTETRGB input 1: Enable counter count down on the falling edge of GTETRGB input.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	DSCARBL	GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Count Down Enable	0: Disable counter count down on the rising edge of GTIOCA input when GTIOCB input is 0 1: Enable counter count down on the rising edge of GTIOCA input when GTIOCB input is 0.	R/W
b9	DSCARBH	GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Count Down Enable	0: Disable counter count down on the rising edge of GTIOCA input when GTIOCB input is 1 1: Enable counter count down on the rising edge of GTIOCA input when GTIOCB input is 1.	R/W

Bit	Symbol	Bit name	Description	R/W
b10	DSCAFBL	GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Count Down Enable	0: Disable counter count down on the falling edge of GTIOCA input when GTIOCB input is 0 1: Enable counter count down on the falling edge of GTIOCA input when GTIOCB input is 0.	R/W
b11	DSCAFBH	GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Count Down Enable	0: Disable counter count down on the falling edge of GTIOCA input when GTIOCB input is 1 1: Enable counter count down on the falling edge of GTIOCA input when GTIOCB input is 1.	R/W
b12	DSCBRAL	GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Count Down Enable	0: Disable counter count down on the rising edge of GTIOCB input when GTIOCA input is 0 1: Enable counter count down on the rising edge of GTIOCB input when GTIOCA input is 0.	R/W
b13	DSCBRAH	GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Count Down Enable	0: Disable counter count down on the rising edge of GTIOCB input when GTIOCA input is 1 1: Enable counter count down on the rising edge of GTIOCB input when GTIOCA input is 1.	R/W
b14	DSCBFAL	GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Count Down Enable	0: Disable counter count down on the falling edge of GTIOCB input when GTIOCA input is 0 1: Enable counter count down on the falling edge of GTIOCB input when GTIOCA input is 0.	R/W
b15	DSCBFAH	GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Count Down Enable	0: Disable counter count down on the falling edge of GTIOCB input when GTIOCA input is 1 1: Enable counter count down on the falling edge of GTIOCB input when GTIOCA input is 1	R/W
b16	DSELCA	ELC_GPTA Event Source Counter Count Down Enable	0: Disable counter count down at the ELC_GPTA event input 1: Enable counter count down at the ELC_GPTA event input.	R/W
b17	DSELCB	ELC_GPTB Event Source Counter Count Down Enable	0: Disable counter count down at the ELC_GPTB event input 1: Enable counter count down at the ELC_GPTB event input.	R/W
b18	DSELCC	ELC_GPTC Event Source Counter Count Down Enable	0: Disable counter count down at the ELC_GPTC event input 1: Enable counter count down at the ELC_GPTC event input.	R/W
b19	DSELCD	ELC_GPTD Event Source Counter Count Down Enable	0: Disable counter count down at the ELC_GPTD event input 1: Enable counter count down at the ELC_GPTD event input.	R/W
b31 to b20	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

GTDNSR sets the source to count down the GTCNT counter.

When at least one bit in the GTDNSR register is set to 1, the GTCNT counter is counted down by the source that is set to 1 in this register but the GTCNT counter set by GTCR.TPCS does not perform the count.

DSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Count Down Enable)

The DSGTRGAR bit enables or disables the GTCNT counter count down on the rising edge of the GTETRGA pin input.

DSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Count Down Enable)

The DSGTRGAF bit enables or disables the GTCNT counter count down on the falling edge of the GTETRGA pin input.

DSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Count Down Enable)

The DSGTRGBR bit enables or disables the GTCNT counter count down on the rising edge of the GTETRGB pin input.

DSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Count Down Enable)

The DSGTRGBF bit enables or disables the GTCNT counter count down on the falling edge of the GTETRGB pin input.

DSCARBL bit (GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Count Down Enable)

The DSCARBL bit enables or disables the GTCNT counter count down on the rising edge of the GTIOCA pin input, when the GTIOCB input is 0.

DSCARBH bit (GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Count Down Enable)

The DSCARBH bit enables or disables the GTCNT counter count down on the rising edge of the GTIOCA pin input, when the GTIOCB input is 1.

DSCAFBL bit (GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Count Down Enable)

The DSCAFBL bit enables or disables the GTCNT counter count down on the falling edge of the GTIOCA pin input, when the GTIOCB input is 0.

DSCAFBH bit (GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Count Down Enable)

The DSCAFBH bit enables or disables the GTCNT counter count down on the falling edge of the GTIOCA pin input, when the GTIOCB input is 1.

DSCBRAL bit (GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Count Down Enable)

The DSCBRAL bit enables or disables the GTCNT counter count down on the rising edge of the GTIOCB pin input, when the GTIOCA input is 0.

DSCBRAH bit (GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Count Down Enable)

The DSCBRAH bit enables or disables the GTCNT counter count down on the rising edge of GTIOCB pin input, when the GTIOCA input is 1.

DSCBFAL bit (GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Count Down Enable)

The DSCBFAL bit enables or disables the GTCNT counter count down on the falling edge of the GTIOCB pin input, when the GTIOCA input is 0.

DSCBFAH bit (GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Count Down Enable)

The DSCBFAH bit enables or disables the GTCNT counter count down on the falling edge of the GTIOCB pin input, when the GTIOCA input is 1.

DSELCm bit (ELC_GPTm Event Source Counter Count Down Enable) (m = A to D)

The DSELCm bit enables or disables the GTCNT counter count down at the ELC_GPTm event input.

20.2.10 General PWM Timer Input Capture Source Select Register A(GTICASR)

Address(es): GPT320.GTICASR 4007 8024h
GPT16Hm.GTICASR 4007 8024h + 0100h × m (m = 1 to 3)
GPT16m.GTICASR 4007 8024h + 0100h × m (m = 4 to 6)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	ASELCD	ASELCC	ASELCB	ASELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ASCBFAH	ASCBFAL	ASCBRAH	ASCBRAL	ASCAFBH	ASCAFBL	ASCARBH	ASCARBL	—	—	—	—	ASGTRGBF	ASGTRGBR	ASGTRGAF	ASGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ASGTRGAR	GTETRGA Pin Rising Input Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on the rising edge of GTETRGA input 1: Enable GTCCRA input capture on the rising edge of GTETRGA input.	R/W
b1	ASGTRGAF	GTETRGA Pin Falling Input Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on the falling edge of GTETRGA input 1: Enable GTCCRA input capture on the falling edge of GTETRGA input.	R/W
b2	ASGTRGBR	GTETRGB Pin Rising Input Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on the rising edge of GTETRGB input 1: Enable GTCCRA input capture on the rising edge of GTETRGB input.	R/W
b3	ASGTRGBF	GTETRGB Pin Falling Input Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on the falling edge of GTETRGB input 1: Enable GTCCRA input capture on the falling edge of GTETRGB input.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	ASCARBL	GTIOCA Pin Rising Input during GTIOCB Value Low Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on the rising edge of GTIOCA input when GTIOCB input is 0 1: Enable GTCCRA input capture on the rising edge of GTIOCA input when GTIOCB input is 0.	R/W
b9	ASCARBH	GTIOCA Pin Rising Input during GTIOCB Value High Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on the rising edge of GTIOCA input when GTIOCB input is 1 1: Enable GTCCRA input capture on the rising edge of GTIOCA input when GTIOCB input is 1.	R/W
b10	ASCAFBL	GTIOCA Pin Falling Input during GTIOCB Value Low Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on the falling edge of GTIOCA input when GTIOCB input is 0 1: Enable GTCCRA input capture on the falling edge of GTIOCA input when GTIOCB input is 0.	R/W
b11	ASCAFBH	GTIOCA Pin Falling Input during GTIOCB Value High Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on the falling edge of GTIOCA input when GTIOCB input is 1 1: Enable GTCCRA input capture on the falling edge of GTIOCA input when GTIOCB input is 1.	R/W
b12	ASCBRAL	GTIOCB Pin Rising Input during GTIOCA Value Low Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on the rising edge of GTIOCB input when GTIOCA input is 0 1: Enable GTCCRA input capture on the rising edge of GTIOCB input when GTIOCA input is 0.	R/W
b13	ASCBRAH	GTIOCB Pin Rising Input during GTIOCA Value High Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on the rising edge of GTIOCB input when GTIOCA input is 1 1: Enable GTCCRA input capture on the rising edge of GTIOCB input when GTIOCA input is 1.	R/W

Bit	Symbol	Bit name	Description	R/W
b14	ASCBFAL	GTIOCB Pin Falling Input during GTIOCA Value Low Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on the falling edge of GTIOCB input when GTIOCA input is 0 1: Enable GTCCRA input capture on the falling edge of GTIOCB input when GTIOCA input is 0.	R/W
b15	ASCBFAH	GTIOCB Pin Falling Input during GTIOCA Value High Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on the falling edge of GTIOCB input when GTIOCA input is 1 1: Enable GTCCRA input capture on the falling edge of GTIOCB input when GTIOCA input is 1.	R/W
b16	ASELCA	ELC_GPTA Event Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture at the ELC_GPTA event input 1: Enable GTCCRA input capture at the ELC_GPTA event input.	R/W
b17	ASELCB	ELC_GPTB Event Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture at the ELC_GPTB event input 1: Enable GTCCRA input capture at the ELC_GPTB event input.	R/W
b18	ASELCC	ELC_GPTC Event Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture at the ELC_GPTC event input 1: Enable GTCCRA input capture at the ELC_GPTC event input.	R/W
b19	ASELCD	ELC_GPTD Event Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture at the ELC_GPTD event input 1: Enable GTCCRA input capture at the ELC_GPTD event input.	R/W
b31 to b20	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

GTICASR sets the source of input capture for GTCCRA.

ASGTRGAR bit (GTETRGA Pin Rising Input Source GTCCRA Input Capture Enable)

The ASGTRGAR bit enables or disables the input capture for GTCCRA on the rising edge of the GTETRGA pin input.

ASGTRGAF bit (GTETRGA Pin Falling Input Source GTCCRA Input Capture Enable)

The ASGTRGAF bit enables or disables the input capture for GTCCRA on the falling edge of the GTETRGA pin input.

ASGTRGBR bit (GTETRGB Pin Rising Input Source GTCCRA Input Capture Enable)

The ASGTRGBR bit enables or disables the input capture for GTCCRA on the rising edge of the GTETRGB pin input.

ASGTRGBF bit (GTETRGB Pin Falling Input Source GTCCRA Input Capture Enable)

The ASGTRGBF bit enables or disables the input capture for GTCCRA on the falling edge of the GTETRGB pin input.

ASCARBL bit (GTIOCA Pin Rising Input during GTIOCB Value Low Source GTCCRA Input Capture Enable)

The ASCARBL bit enables or disables the input capture for GTCCRA on the rising edge of the GTIOCA pin input, when the GTIOCB input is 0.

ASCARBH bit (GTIOCA Pin Rising Input during GTIOCB Value High Source GTCCRA Input Capture Enable)

The ASCARBH bit enables or disables the input capture for GTCCRA on the rising edge of the GTIOCA pin input, when the GTIOCB input is 1.

ASCAFBL bit (GTIOCA Pin Falling Input during GTIOCB Value Low Source GTCCRA Input Capture Enable)

The ASCAFBL bit enables or disables the input capture for GTCCRA on the falling edge of the GTIOCA pin input, when the GTIOCB input is 0.

ASCAFBH bit (GTIOCA Pin Falling Input during GTIOCB Value High Source GTCCRA Input Capture Enable)

The ASCAFBH bit enables or disables the input capture for GTCCRA on the falling edge of the GTIOCA pin input, when the GTIOCB input is 1.

ASCBRAL bit (GTIOCB Pin Rising Input during GTIOCA Value Low Source GTCCRA Input Capture Enable)

The ASCBRAL bit enables or disables the input capture for GTCCRA on the rising edge of the GTIOCB pin input, when the GTIOCA input is 0.

ASCBRAH bit (GTIOCB Pin Rising Input during GTIOCA Value High Source GTCCRA Input Capture Enable)

The ASCBRAH bit enables or disables the input capture for GTCCRA on the rising edge of the GTIOCB pin input, when the GTIOCA input is 1.

ASCBFAL bit (GTIOCB Pin Falling Input during GTIOCA Value Low Source GTCCRA Input Capture Enable)

The ASCBFAL bit enables or disables the input capture for GTCCRA on the falling edge of the GTIOCB pin input, when the GTIOCA input is 0.

ASCBFAH bit (GTIOCB Pin Falling Input during GTIOCA Value High Source GTCCRA Input Capture Enable)

The ASCBFAH bit enables or disables the input capture for GTCCRA on the falling edge of the GTIOCB pin input, when the GTIOCA input is 1.

ASELCm bit (ELC_GPTm Event Source Counter GTCCRA Input Capture Enable) (m = A to D)

The ASELCm bit enables or disables the input capture for GTCCRA at the ELC_GPTm event input.

20.2.11 General PWM Timer Input Capture Source Select Register B(GTICBSR)

Address(es): GPT320.GTICBSR 4007 8028h
GPT16Hm.GTICBSR 4007 8028h + 0100h × m (m = 1 to 3)
GPT16m.GTICBSR 4007 8028h + 0100h × m (m = 4 to 6)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	BSELCD	BSELCC	BSELCB	BSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BSCBFAH	BSCBFAL	BSCBRAH	BSCBRAL	BSCAFBH	BSCAFBL	BSCARBH	BSCARBL	—	—	—	—	BSGTRGBF	BSGTRGBR	BSGTRGAF	BSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	BSGTRGAR	GTETRGA Pin Rising Input Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on the rising edge of GTETRGA input 1: Enable GTCCRB input capture on the rising edge of GTETRGA input.	R/W
b1	BSGTRGAF	GTETRGA Pin Falling Input Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on the falling edge of GTETRGA input 1: Enable GTCCRB input capture on the falling edge of GTETRGA input.	R/W
b2	BSGTRGBR	GTETRGB Pin Rising Input Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on the rising edge of GTETRGB input 1: Enable GTCCRB input capture on the rising edge of GTETRGB input.	R/W

Bit	Symbol	Bit name	Description	R/W
b3	BSGTRGBF	GTETRGB Pin Falling Input Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on the falling edge of GTETRGB input 1: Enable GTCCRB input capture on the falling edge of GTETRGB input.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	BSCARBL	GTIOCA Pin Rising Input during GTIOCB Value Low Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on the rising edge of GTIOCA input when GTIOCB input is 0 1: Enable GTCCRB input capture on the rising edge of GTIOCA input when GTIOCB input is 0.	R/W
b9	BSCARBH	GTIOCA Pin Rising Input during GTIOCB Value High Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on the rising edge of GTIOCA input when GTIOCB input is 1 1: Enable GTCCRB input capture on the rising edge of GTIOCA input when GTIOCB input is 1.	R/W
b10	BSCAFBL	GTIOCA Pin Falling Input during GTIOCB Value Low Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on the falling edge of GTIOCA input when GTIOCB input is 0 1: Enable GTCCRB input capture on the falling edge of GTIOCA input when GTIOCB input is 0.	R/W
b11	BSCAFBH	GTIOCA Pin Falling Input during GTIOCB Value High Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on the falling edge of GTIOCA input when GTIOCB input is 1 1: Enable GTCCRB input capture on the falling edge of GTIOCA input when GTIOCB input is 1.	R/W
b12	BSCBRAL	GTIOCB Pin Rising Input during GTIOCA Value Low Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on the rising edge of GTIOCB input when GTIOCA input is 0 1: Enable GTCCRB input capture on the rising edge of GTIOCB input when GTIOCA input is 0.	R/W
b13	BSCBRAH	GTIOCB Pin Rising Input during GTIOCA Value High Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on the rising edge of GTIOCB input when GTIOCA input is 1 1: Enable GTCCRB input capture on the rising edge of GTIOCB input when GTIOCA input is 1.	R/W
b14	BSCBFAL	GTIOCB Pin Falling Input during GTIOCA Value Low Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on the falling edge of GTIOCB input when GTIOCA input is 0 1: Enable GTCCRB input capture on the falling edge of GTIOCB input when GTIOCA input is 0.	R/W
b15	BSCBFAH	GTIOCB Pin Falling Input during GTIOCA Value High Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on the falling edge of GTIOCB input when GTIOCA input is 1 1: Enable GTCCRB input capture on the falling edge of GTIOCB input when GTIOCA input is 1.	R/W
b16	BSELCA	ELC_GPTA Event Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture at the ELC_GPTA event input 1: Enable GTCCRB input capture at the ELC_GPTA event input.	R/W
b17	BSELCB	ELC_GPTB Event Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture at the ELC_GPTB event input 1: Enable GTCCRB input capture at the ELC_GPTB event input.	R/W
b18	BSELCC	ELC_GPTC Event Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture at the ELC_GPTC event input 1: Enable GTCCRB input capture at the ELC_GPTC event input.	R/W
b19	BSELCD	ELC_GPTD Event Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture at the ELC_GPTD event input 1: Enable GTCCRB input capture at the ELC_GPTD event input.	R/W
b31 to b20	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

GTICBSR sets the source of input capture for GTCCRB.

BSGTRGAR bit (GTETRGA Pin Rising Input Source GTCCRB Input Capture Enable)

The BSGTRGAR bit enables or disables the input capture for GTCCRB on the rising edge of the GTETRGA pin input.

BSGTRGAF bit (GTETRGA Pin Falling Input Source GTCCRB Input Capture Enable)

The BSGTRGAF bit enables or disables the input capture for GTCCRB on the falling edge of the GTETRGA pin input.

BSGTRGBR bit (GTETRGB Pin Rising Input Source GTCCRB Input Capture Enable)

The BSGTRGBR bit enables or disables the input capture for GTCCRB on the rising edge of GTETRGB pin input.

BSGTRGBF bit (GTETRGB Pin Falling Input Source GTCCRB Input Capture Enable)

The BSGTRGBF bit enables or disables the input capture for GTCCRB on the falling edge of the GTETRGB pin input.

BSCARBL bit (GTIOCA Pin Rising Input during GTIOCB Value Low Source GTCCRB Input Capture Enable)

The BSCARBL bit enables or disables the input capture for GTCCRB on the rising edge of the GTIOCA pin input, when the GTIOCB input is 0.

BSCARBH bit (GTIOCA Pin Rising Input during GTIOCB Value High Source GTCCRB Input Capture Enable)

The BSCARBH bit enables or disables the input capture for GTCCRB on the rising edge of the GTIOCA pin input, when the GTIOCB input is 1.

BSCAFBL bit (GTIOCA Pin Falling Input during GTIOCB Value Low Source GTCCRB Input Capture Enable)

The BSCAFBL bit enables or disables the input capture for GTCCRB on the falling edge of the GTIOCA pin input, when the GTIOCB input is 0.

BSCAFBH bit (GTIOCA Pin Falling Input during GTIOCB Value High Source GTCCRB Input Capture Enable)

The BSCAFBH bit enables or disables the input capture for GTCCRB on the falling edge of the GTIOCA pin input, when the GTIOCB input is 1.

BSCBRAL bit (GTIOCB Pin Rising Input during GTIOCA Value Low Source GTCCRB Input Capture Enable)

The BSCBRAL bit enables or disables the input capture for GTCCRB on the rising edge of the GTIOCB pin input, when the GTIOCA input is 0.

BSCBRAH bit (GTIOCB Pin Rising Input during GTIOCA Value High Source GTCCRB Input Capture Enable)

The BSCBRAH bit enables or disables the input capture for GTCCRB on the rising edge of the GTIOCB pin input, when the GTIOCA input is 1.

BSCBFAL bit (GTIOCB Pin Falling Input during GTIOCA Value Low Source GTCCRB Input Capture Enable)

The BSCBFAL bit enables or disables the input capture for GTCCRB on the falling edge of the GTIOCB pin input, when the GTIOCA input is 0.

BSCBFAH bit (GTIOCB Pin Falling Input during GTIOCA Value High Source GTCCRB Input Capture Enable)

The BSCBFAH bit enables or disables the input capture for GTCCRB on the falling edge of the GTIOCB pin input, when the GTIOCA input is 1.

BSELCm bit (ELC_GPTm Event Source Counter GTCCRB Input Capture Enable) (m = A to D)

The BSELCm bit enables or disables the input capture for GTCCRB at the ELC_GPTm event input.

20.2.12 General PWM Timer Control Register (GTCR)

Address(es): GPT320.GTCR 4007 802Ch
GPT16Hm.GTCR 4007 802Ch + 0100h × m (m = 1 to 3)
GPT16m.GTCR 4007 802Ch + 0100h × m (m = 4 to 6)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	TPCS[2:0]			—	—	—	—	—	MD[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CST	Count Start	0: Stop count operation 1: Perform count operation.	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b18 to b16	MD[2:0]	Mode Select	b18 b16 0 0 0: Saw-wave PWM mode (single buffer or double buffer possible) 0 0 1: Saw-wave one-shot pulse mode (fixed buffer operation) 0 1 0: Setting prohibited 0 1 1: Setting prohibited 1 0 0: Triangle-wave PWM mode 1 (32-bit transfer at trough) (single buffer or double buffer is possible) 1 0 1: Triangle-wave PWM mode 2 (32-bit transfer at crest and trough) (single buffer or double buffer is possible) 1 1 0: Triangle-wave PWM mode 3 (64-bit transfer at trough) fixed buffer operation) 1 1 1: Setting prohibited.	R/W
b23 to b19	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b26 to b24	TPCS[2:0]	Timer Prescaler Select	b26 b24 0 0 0: PCLKD/1 0 0 1: PCLKD/4 0 1 0: PCLKD/16 0 1 1: PCLKD/64 1 0 0: PCLKD/256 1 0 1: PCLKD/1024.	R/W
b31 to b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

GTCR controls GTCNT.

CST bit (Count Start)

The CST bit controls the GTCNT counter start and stop.

[Setting conditions]

- GTSTR value where the channel number associated with the bit number is set to 1 with the GTSSR.CSTRT bit = 1
- The ELC event input or the GTIOCA/GTIOCB/GTETRGn port input that are enabled by GTSSR for starting counter source, occurs
- 1 is written by software directly.

[Clearing conditions]

- GTSTP value where the channel number associated with the bit number is set to 1 with the GTPSR.CSTOP bit = 1.
- The ELC event input or the GTIOCA/GTIOCB/GTETRGn port input that are enabled by GTPSR for stopping

counter source, occurs

- 0 is written by software directly.

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode. The MD[2:0] bits must be set while the GTCNT operation is stopped.

TPCS[2:0] bits (Timer Prescaler Select)

The TPCS[2:0] bits select the clock for GTCNT. A clock prescaler can be selected independently for each channel. The TPCS[2:0] bits should be set while the GTCNT operation is stopped.

20.2.13 General PWM Timer Count Direction and Duty Setting Register (GTUDDTYC)

Address(es): GPT320.GTUDDTYC 4007 8030h
GPT16Hm.GTUDDTYC 4007 8030h + 0100h × m (m = 1 to 3)
GPT16m.GTUDDTYC 4007 8030h + 0100h × m (m = 4 to 6)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	OBDTYR	OBDTYF	OBDTY[1:0]		—	—	—	—	OADTYR	OADTYF	OADTY[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UDF	UD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b0	UD	Count Direction Setting	0: Count down on GTCNT 1: Count up on GTCNT.	R/W
b1	UDF	Forcible Count Direction Setting	0: Do not force setting 1: Force setting.	R/W
b15 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b17, 16	OADTY[1:0]	GTIOCA Output Duty Setting	b17 b16 0 x: GTIOCA pin duty depends on compare match 1 0: GTIOCA pin duty 0% 1 1: GTIOCA pin duty 100%.	R/W
b18	OADTYF	Forcible GTIOCA Output Duty Setting	0: D not force setting 1: Force setting.	R/W
b19	OADTYR	GTIOCA Output Value Selecting after Releasing 0%/100% Duty Setting	0: Apply output value set in 0%/100% duty to GTIOA[3:2] function after releasing 0%/100% duty setting 1: Apply masked compare match output value to GTIOA[3:2] function after releasing 0%/100% duty setting.	R/W
b23 to b20	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b25, b24	OBDTY[1:0]	GTIOCB Output Duty Setting	b25 b24 0 x: GTIOCB pin duty is depended on the compare match 1 0: GTIOCB pin duty 0% 1 1: GTIOCB pin duty 100%	R/W
b26	OBDTYF	Forcible GTIOCB Output Duty Setting	0: Do not force setting 1: Force setting.	R/W
b27	OBDTYR	GTIOCB Output Value Selecting after Releasing 0%/100% Duty Setting	0: Apply output value set in 0%/100% duty to GTIOB[3:2] function after releasing 0%/100% duty setting 1: Apply masked compare match output value to GTIOB[3:2] function after releasing 0%/100% duty setting	R/W
b31 to b28	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

x: Don't care

GTUDDTYC sets the direction in which the GTCNT counts (up-counting or down-counting) and sets the duty of the GTIOCA/GTIOCB pin output.

Count Direction:

- In saw-wave mode.

When the UD value is set to 0 during up-counting, the count direction changes at an overflow (the timing synchronous with count clock after the GTCNT value becomes the GTPR value). When the UD value is set to 1 during down-counting, the count direction changes at an underflow (the timing synchronous with count clock after the GTCNT value becomes 0).

When the UD value changes from 1 to 0 with the UDF bit being 0 and while counting stops, the counter starts up-counting and the count direction changes at an overflow (the timing synchronous with count clock after the GTCNT value becomes the GTPR value). When the UD value changes from 0 to 1 with the UDF bit being 0 and while counting stops, the counter starts down-counting and the count direction changes at an underflow (the timing synchronous with count clock after the GTCNT value becomes 0).

When the UDF bit is set to 1 while counting stops, the UD bit value at that time is reflected in the count direction when counting starts.

- In triangle-wave mode.

When the UD value changes during counting, the count direction does not change. When the UD value changes while the UDF bit is 0 and counting stops, the change is not reflected in the count direction when counting starts.

When the UDF bit is set to 1 while counting is stopped, the UD value at that time is reflected in the count direction when counting starts.

UD bit (Count Direction Setting)

The UD bit sets the count direction (up-counting or down-counting) for GTCNT.

UDF bit (Forcible Count Direction Setting)

The UDF bit forcibly sets the count direction when GTCNT starts operation as the UD value. Only 0 should be written to this bit during counter operation. When 1 is written to this bit while counting stops, this bit must be returned to 0 before counting starts.

Output duty

- In saw-wave mode

When the OADTY/OBDTY value is changed during up-counting, the duty is reflected at an overflow (GTCNT = GTPR). When the OADTY/OBDTY value is changed during down-counting, the duty is reflected at an underflow (GTCNT = 0).

When the OADTY/OBDTY value is changed with the OADTYF/OBDTYF bit being 0 and while counting stops the output duty is not reflected at the starting counter operation. When the count direction is up, the output duty is reflected at an overflow (GTCNT = GTPR). When the count direction is down, the output duty is reflected at an underflow (GTCNT = 0).

When the OADTY/OBDTY value is changed with the OADTYF/OBDTYF bit being 1 and while counting stops, the output duty is reflected at starting counter operation.

- In triangle-wave mode

When the OADTY/OBDTY value is changed during counting, the duty is reflected at an underflow.

When the OADTY/OBDTY value is changed with the OADTYF/OBDTYF bit being 0 and while counting stops, the output duty is not reflected at the starting counter operation. The output duty is reflected at an underflow.

When the OADTY/OBDTY value is changed with the OADTYF/OBDTYF bit being 1 and while counting stops, the output duty is reflected at starting counter operation.

OmDTY[1:0] bits (GTIOCm Output Duty Setting) (m = A, B)

These bits set the output duty (0%, 100% or compare match control) of the GTIOCm pin.

OmDTYF bit (ForcibleGTIOCm Output Duty Setting) (m = A, B)

This bit forcibly sets the output duty cycle to the OmDTY setting. This bit must be set to 0 during counter operation.

When this bit is set to 1 while counting stops, this bit must be returned to 0 until the first period ends after the counter starts.

OmDTYR bit (GTIOCm Output Value Selecting after Releasing 0%/100% Duty Setting) (m = A, B)

These bits select the value that is the object of output retained/toggled at cycle end, when the control changes from 0%/100% duty setting to compare match for GTIOCm pin and GTIOR.GTIOm[3:2] are set to 00b (output retained at cycle end) or GTIOR.GTIOm[3:2] are set to 11b (output toggled at cycle end).

While the duty 0%/100% setting operation is running, the compare match operation continues in the GPT32. When the OmDTYR bit is set to 1, the GTIOCm pin is in the output state selected by the GTIOR.GTIOm[3:2] bits at the end of the cycle in the compare match operation.

20.2.14 General PWM Timer I/O Control Register (GTIOR)

Address(es): GPT320.GTIOR 4007 8034h
GPT16Hm.GTIOR 4007 8034h + 0100h × m (m = 1 to 3)
GPT16m.GTIOR 4007 8034h + 0100h × m (m = 4 to 6)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	NFCSB[1:0]		NFBEN	—	—	OBDF[1:0]		OBE	OBHLD	OBDFLT	—	GTIOB[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	NFCSA[1:0]		NFAEN	—	—	OADF[1:0]		OAE	OAHLD	OADFLT	—	GTIOA[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	GTIOA[4:0]	GTIOCA Pin Function Select	See Table 20.5.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	OADFLT	GTIOCA Pin Output Value Setting at the Count Stop	0: Output low on GTIOCA pin when counting stops 1: Output high on GTIOCA pin when counting stops.	R/W
b7	OAHLD	GTIOCA Pin Output Setting at the Start/Stop Count	0: Set GTIOCA pin output level on counting start and stop based on the register setting 1: Retain GTIOCA pin output level on counting start and stop.	R/W
b8	OAE	GTIOCA Pin Output Enable	0: Disable output 1: Enable output.	R/W
b10, b9	OADF[1:0]	GTIOCA Pin Disable Value Setting	b10 b9 0 0: None of the below options are specified 0 1: GTIOCA pin is set to Hi-Z in response to control the output negation 1 0: Set GTIOCA pin to 0 in response to control the output negation 1 1: Set GTIOCA pin to 1 in response to control the output negation.	R/W
b12, b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13	NFAEN	Noise Filter A Enable	0: Disable noise filter for GTIOCA pin 1: Enable noise filter for GTIOCA pin.	R/W
b15, b14	NFCSA[1:0]	Noise Filter A Sampling Clock Select	b15 b14 0 0: PCLKD/1 0 1: PCLKD/4 1 0: PCLKD/16 1 1: PCLKD/64.	R/W
b20 to b16	GTIOB[4:0]	GTIOCB Pin Function Select	See Table 20.5	R/W
b21	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b22	OBDFLT	GTIOCB Pin Output Value Setting at the Count Stop	0: Output low on GTIOCB pin when counting stops 1: Output high on GTIOCB pin when counting stops.	R/W

Bit	Symbol	Bit name	Description	R/W
b23	OBHLD	GTIOCB Pin Output Setting at the Start/Stop Count	0: Set GTIOCB pin output level on counting start and stop based on the register setting 1: Retain GTIOCB pin output level on counting start and stop.	R/W
b24	OBE	GTIOCB Pin Output Enable	0: Disable output 1: Enable output.	R/W
b26, b25	OBDF[1:0]	GTIOCB Pin Disable Value Setting	b26 b25 0 0: None of the below options are specified 0 1: GTIOCB pin is set to Hi-Z in response to control the output negation 1 0: Set GTIOCB pin to 0 in response to control the output negation 1 1: Set GTIOCB pin to 1 in response to control the output negation.	R/W
b28, b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b29	NFBEN	Noise Filter B Enable	0: Disable noise filter for GTIOCB pin 1: Enable noise filter for GTIOCB pin.	R/W
b31, b30	NFCSB[1:0]	Noise Filter B Sampling Clock Select	b31 b30 0 0: PCLKD/1 0 1: PCLKD/4 1 0: PCLKD/16 1 1: PCLKD/64.	R/W

GTIOR sets the functions of the GTIOCA and GTIOCB pins.

GTIOA[4:0] bits (GTIOCA Pin Function Select)

The GTIOA[4:0] bits select the GTIOCA pin function. For details, see Table 20.5.

OADFLT bit (GTIOCA Pin Output Value Setting at the Count Stop)

The OADFLT bit sets whether the GTIOCA pin outputs high or low when counting stops.

OAHLD bit (GTIOCA Pin Output Setting at the Start/Stop Count)

The OAHLD bit specifies whether the GTIOCA pin output level is retained or the level depends on the register setting when counting starts or stops.

When the OAHLD bit is set to 0

- The value specified by b4 of the GTIOA[4:0] bits is output when counting starts
- The value specified by the OADFLT bit is output when counting stops
- If the OADFLT bit is modified while counting stops, it is immediately reflected in the output.

When the OAHLD bit is set to 1

- The output is retained when counting starts or stops.

OAE bit (GTIOCA Pin Output Enable)

The OAE bit disables or enables the GTIOCA pin output.

When GTCCRA register is used as the input capture register (at least 1 bit in the GTICASR register is set to 1), the GTIOCA pin does not output independently of the OAE bit value.

OADF[1:0] bits (GTIOCA Pin Disable Value Setting)

The OADF[1:0] bits select the output value of the GTIOCA pin in response to a request to disable output from the POEG.

NFAEN bit (Noise Filter A Enable)

The NFAEN bit disables or enables the noise filter for input from the GTIOCA pin. Because changing the value of the bit might lead to internal generation of an unexpected edge, select the output compare function for the relevant pin in the GTIOR register before doing so.

NFCSA[1:0] bits (Noise Filter A Sampling Clock Select)

The NFCSA[1:0] bits set the sampling interval for the noise filter of the GTIOCA pin. When setting these bits, wait for 2 cycles of the selected sampling interval before setting the input capture function.

GTIOB[4:0] bits (GTIOCB Pin Function Select)

The GTIOB[4:0] bits select the GTIOCB pin function. For details, see Table 20.5.

OBDFLT bit (GTIOCB Pin Output Value Setting at the Count Stop)

The OBDFLT bit sets whether the GTIOCB pin outputs high or low when counting stops.

OBHLD bit (GTIOCB Pin Output Setting at the Start/Stop Count)

The OBHLD bit specifies whether the GTIOCB pin output level is retained or the level at the start/stop of counting depends on the register setting.

When the OBHLD bit is set to 0:

- The value specified by bit [4] of the GTIOB[4:0] bits is output when counting starts
- The value specified by the OBDFLT bit is output when counting stops
- If the OBDFLT bit is modified while counting stops, it is immediately reflected in the output.

When the OBHLD bit is set to 1:

- The output is retained when counting starts or stops.

OBE bit (GTIOCB Pin Output Enable)

The OBE bit disables or enables the GTIOCB pin output.

When GTCCRB register is used as the input capture register (at least one bit in the GTICBSR register is set to 1), the GTIOCB pin does not output independently of the OBE bit value.

OBDF[1:0] bits (GTIOCB Pin Disable Value Setting)

The OBDF[1:0] bits select the output value of the GTIOCB pin in response to a request to disable output from the POEG.

NFBEN bit (Noise Filter B Enable)

The NFBEN bit disables or enables the noise filter for input from the GTIOCB pin. Because changing the value of the bit might lead to the internal generation of an unexpected edge, select the output compare function for the relevant pin in the GTIOR register before doing so.

NFCSB[1:0] bits (Noise Filter B Sampling Clock Select)

The NFCSB[1:0] bits set the sampling interval for the noise filter of the GTIOCB pin. When setting these bits, wait for 2 cycles of the selected sampling interval before setting the input capture function.

Table 20.5 Settings of GTIOA[4:0] and GTIOB[4:0] bits

GTIOA/GTIOB[4:0] bits					Function		
b4	**b3**	**b2**	**b1**	**b0**	**b4**	**b3, b2*1, *2, *3**	**b1, b0*2**
0	0	0	0	0	Initial output is low.	Output retained at cycle end	Output retained at GTCCRA/GTCCRB compare match
0	0	0	0	1			Low output at GTCCRA/GTCCRB compare match
0	0	0	1	0			High output at GTCCRA/GTCCRB compare match
0	0	0	1	1			Output toggled at GTCCRA/GTCCRB compare match
0	0	1	0	0		Low output at cycle end	Output retained at GTCCRA/GTCCRB compare match
0	0	1	0	1			Low output at GTCCRA/GTCCRB compare match
0	0	1	1	0			High output at GTCCRA/GTCCRB compare match
0	0	1	1	1			Output toggled at GTCCRA/GTCCRB compare match
0	1	0	0	0		High output at cycle end	Output retained at GTCCRA/GTCCRB compare match
0	1	0	0	1			Low output at GTCCRA/GTCCRB compare match
0	1	0	1	0			High output at GTCCRA/GTCCRB compare match
0	1	0	1	1			Output toggled at GTCCRA/GTCCRB compare match
0	1	1	0	0		Output toggled at cycle end	Output retained at GTCCRA/GTCCRB compare match
0	1	1	0	1			Low output at GTCCRA/GTCCRB compare match
0	1	1	1	0			High output at GTCCRA/GTCCRB compare match
0	1	1	1	1			Output toggled at GTCCRA/GTCCRB compare match
1	0	0	0	0	Initial output is high.	Output retained at cycle end	Output retained at GTCCRA/GTCCRB compare match
1	0	0	0	1			Low output at GTCCRA/GTCCRB compare match
1	0	0	1	0			High output at GTCCRA/GTCCRB compare match
1	0	0	1	1			Output toggled at GTCCRA/GTCCRB compare match
1	0	1	0	0		Low output at cycle end	Output retained at GTCCRA/GTCCRB compare match
1	0	1	0	1			Low output at GTCCRA/GTCCRB compare match
1	0	1	1	0			High output at GTCCRA/GTCCRB compare match
1	0	1	1	1			Output toggled at GTCCRA/GTCCRB compare match
1	1	0	0	0		High output at cycle end	Output retained at GTCCRA/GTCCRB compare match
1	1	0	0	1			Low output at GTCCRA/GTCCRB compare match
1	1	0	1	0			High output at GTCCRA/GTCCRB compare match
1	1	0	1	1			Output toggled at GTCCRA/GTCCRB compare match
1	1	1	0	0		Output toggled at cycle end	Output retained at GTCCRA/GTCCRB compare match
1	1	1	0	1			Low output at GTCCRA/GTCCRB compare match
1	1	1	1	0			High output at GTCCRA/GTCCRB compare match
1	1	1	1	1			Output toggled at GTCCRA/GTCCRB compare match

Note 1. The cycle end means an overflow (GTCNT changes from GTPR to 0 in up-counting), an underflow (GTCNT changes from 0 to GTPR in down-counting), or counter clearing for saw-wave mode, and means a trough (GTCNT changes from 0 to 1) for triangle-wave mode.

Note 2. When the timing of a cycle end and the timing of a GTCCRA/GTCCRB compare match are the same in a compare-match operation, the b3 and b2 settings are given priority in saw-wave PWM mode, and the b1 and b0 settings are given priority in any other mode.

Note 3. In event count operation where at least one bit in GTUPSR or GTDNSR is set to 1, the setting of b3 and b2 is ignored.

20.2.15 General PWM Timer Interrupt Output Setting Register (GTINTAD)

Address(es): GPT320.GTINTAD 4007 8038h
GPT16Hm.GTINTAD 4007 8038h + 0100h × m (m = 1 to 3)
GPT16m.GTINTAD 4007 8038h + 0100h × m (m = 4 to 6)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	GRPABL	GRPABH	—	—	—	GRP[1:0]		—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b23 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b25, b24	GRP[1:0]	Output Disable Source Select	b25 b24 0 0: Select group A output disable request 0 1: Select group B output disable request 1 0: Setting Prohibited 1 1: Setting Prohibited.	R/W
b28 to b26	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b29	GRPABH	Same Time Output Level High Disable Request Enable	0: Disable same time output level high disable request 1: Enable same time output level high disable request.	R/W
b30	GRPABL	Same Time Output Level Low Disable Request Enable	0: Disable same time output level low disable request 1: Enable same time output level low disable request.	R/W
b31	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

GTINTAD enables or disables interrupt requests and output disable requests.

GRP[1:0] bits (Output Disable Source Select)

The GRP[1:0] bits select the GTIOCA pin and GTIOCB pin output disable source. The output disable request to POEG outputs to the group that is selected by GRP[1:0] bits when the same time output level high or same time output level low occurs based on the output disable request enable bit.

GTST.ODF shows the request of the output disable source group that is selected with the GRP[1:0] bits. Set the GRP[1:0] bits when both GTIOR.OAE and GTIOR.OBE are 0.

GRPABH bit (Same Time Output Level High Disable Request Enable)

The GRPABH bit enables or disables the output disable request when the GTIOCA pin and GTIOCB pin output 1 at the same time.

GRPABL bit (Same Time Output Level Low Disable Request Enable)

The GRPABL bit enables or disables the output disable request when the GTIOCA pin and GTIOCB pin output 0 at the same time.

20.2.16 General PWM Timer Status Register (GTST)

Address(es): GPT320.GTST 4007 803Ch
GPT16Hm.GTST 4007 803Ch + 0100h × m (m = 1 to 3)
GPT16m.GTST 4007 803Ch + 0100h × m (m = 4 to 6)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	OABLF	OABHF	—	—	—	—	ODF	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TUCF	—	—	—	—	—	—	—	TCFPU	TCFPO	TCFF	TCFE	TCFD	TCFC	TCFB	TCFA
Value after reset:	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TCFA	Input Capture/Compare Match Flag A	0: No input capture/compare match of GTCCRA is generated 1: An input capture/compare match of GTCCRA is generated.	R/(W)*1
b1	TCFB	Input Capture/Compare Match Flag B	0: No input capture/compare match of GTCCRB is generated 1: An input capture/compare match of GTCCRB is generated.	R/(W)*1
b2	TCFC	Input Compare Match Flag C	0: No compare match of GTCCRC is generated 1: A compare match of GTCCRC is generated.	R/(W)*1
b3	TCFD	Input Compare Match Flag D	0: No compare match of GTCCRD is generated 1: A compare match of GTCCRD is generated.	R/(W)*1
b4	TCFE	Input Compare Match Flag E	0: No compare match of GTCCRE is generated 1: A compare match of GTCCRE is generated.	R/(W)*1
b5	TCFF	Input Compare Match Flag F	0: No compare match of GTCCRF is generated 1: A compare match of GTCCRF is generated.	R/(W)*1
b6	TCFPO	Overflow Flag	0: No overflow (crest) occurred 1: An overflow (crest) occurred.	R/(W)*1
b7	TCFPU	Underflow Flag	0: No underflow (trough) occurred 1: An underflow (trough) occurred.	R/(W)*1
b14 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	TUCF	Count Direction Flag	0: GTCNT counter is counting down 1: GTCNT counter is counting up.	R
b23 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b24	ODF	Output Disable Flag	0: No output disable request is generated 1: An output disable request is generated.	R
b28 to b25	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b29	OABHF	Same Time Output Level High Flag	0: GTIOCA pin and GTIOCB pin do not output 1 at the same time 1: GTIOCA pin and GTIOCB pin output 1 at the same time.	R
b30	OABLF	Same Time Output Level Low Flag	0: GTIOCA pin and GTIOCB pin do not output 0 at the same time 1: GTIOCA pin and GTIOCB pin output 0 at the same time.	R
b31	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. Only 0 can be written to this bit; do not write 1.

GTST indicates the status of the GPT.

TCFA flag (Input Capture/Compare Match Flag A)

The TCFA flag indicates the status of the input capture or compare match of GTCCRA.

[Setting conditions]

- GTCNT = GTCCRA, when the GTCCRA register functions as a compare match register

- GTCNT counter value is transferred to GTCCRA by the input capture signal when the GTCCRA register functions as an input capture register.

[Clearing condition]

- 0 is written to this flag.

TCFB flag (Input Capture/Compare Match Flag B)

The TCFB flag indicates the status of the input capture or compare match of GTCCRB.

[Setting conditions]

- GTCNT = GTCCRB, when the GTCCRB register functions as a compare match register
- GTCNT counter value is transferred to GTCCRB by the input capture signal when the GTCCRB register functions as an input capture register.

[Clearing condition]

- 0 is written to this flag.

TCFC flag (Input Compare Match Flag C)

The TCFC flag indicates the status of the compare match of GTCCRC.

[Setting condition]

- GTCNT = GTCCRC.

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 01b, 10b, 11b (GTCCRC performs buffer operation).

TCFD flag (Input Compare Match Flag D)

The TCFD flag indicates the status of the compare match of GTCCRD.

[Setting condition]

- GTCNT = GTCCRD.

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 10b, 11b (GTCCRD performs buffer operation).

TCFE flag (Input Compare Match Flag E)

This bit is the status flag for the compare match of GTCCRE.

[Setting condition]

- GTCNT = GTCCRE.

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 01b, 10b, 11b (GTCCRE performs buffer operation).

TCFF flag (Input Compare Match Flag F)

This bit is the status flag for the compare match of GTCCRF.

[Setting condition]

- GTCNT = GTCCRF.

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 10b, 11b (GTCCRF performs buffer operation).

TCFPO flag (Overflow Flag)

The TCFPO flag indicates when an overflow or crest has occurred.

[Setting conditions]

- In saw-wave mode, an overflow (GTCNT changes from GTPR to 0 in up count) has occurred
- In triangle-wave mode, a crest (GTCNT changes from GTPR to GTPR-1) has occurred
- In counting by hardware sources, an overflow (GTCNT changes from GTPR to 0 in up count) has occurred.

[Clearing condition]

- 0 is written to this flag.

TCFPU flag (Underflow Flag)

The TCFPU flag indicates when underflow or trough has occurred.

[Setting conditions]

- In saw-wave mode, an underflow (GTCNT changes from 0 to GTPR in down count) has occurred
- In triangle-wave mode, a crest (GTCNT changes from 0 to 1) has occurred
- In counting by hardware sources, an underflow (GTCNT changes from 0 to GTPR in down count) has occurred.

[Clearing condition]

- 0 is written to this flag.

TUCF flag (Count Direction Flag)

The TUCF flag indicates the count direction of GTCNT.

In event count operation, this flag is set to 1 in up-counting and to 0 in down-counting.

ODF flag (Output Disable Flag)

The ODF flag shows the request of the output disable source group that is selected with the GRP[1:0] bits.

When output is disabled, the output disable control is not released within the same 1 cycle in which the output disable request is negated. It is released in the next cycle.

OABHF flag (Same Time Output Level High Flag)

The OABHF flag indicates that the GTIOCA pin and GTIOCB pin output 1 at the same time.

When the GTIOCA pin or GTIOCB pin output 0, this flag returns to 0. This flag is read only. Writing 0 to clear the flag is not allowed.

When an interrupt by the OABHF flag is enabled (GTINTAD.GRPABH = 1), the OABHF flag is output to POEG as an output disable request.

[Setting condition]

- GTIOCA pin and GTIOCB pin output 1 at the same time when both OAE bit and OBE bit are set to 1.

[Clearing conditions]

- GTIOCA pin output value is different from the GTIOCB pin output value when both OAE bit and OBE bit are set to 1
- GTIOCA pin and GTIOCB pin output 0 at the same time when both OAE bit and OBE bit are set to 1
- At least either OAE bit or OBE bit is set to 0.

OABLF flag (Same Time Output Level Low Flag)

The OABLF flag indicates that GTIOCA pin and GTIOCB pin output 0 at the same time.

When the GTIOCA pin or GTIOCB pin output 1, this flag returns to 0. This flag is read only. Writing 0 to clear the flag is not allowed.

When an interrupt by the OABLF flag is enabled (GTINTAD.GRPABL = 1), the OABLF flag is output to POEG as an output disable request.

[Setting condition]

- GTIOCA pin and GTIOCB pin output 0 at the same time when both OAE bit and OBE bit are set to 1.

[Clearing conditions]

- GTIOCA pin output value is different from GTIOCB pin output value when both OAE bit and OBE bit are set to 1
- GTIOCA pin and GTIOCB pin output 1 at the same time when both OAE bit and OBE bit are set to 1
- At least either OAE bit or OBE bit is set to 0.

The compare-target signals to generate the OABHF/OABLF flag are the compare match outputs (PWM outputs) signals before masked by the output disable function. When the output disable state is performed, a compare match is also performed continuously in the GPT and the OABHF/OABLF flag is updated in association with the result of the compared value.

20.2.17 General PWM Timer Buffer Enable Register (GTBER)

Address(es): GPT320.GTBER 4007 8040h
GPT16Hm.GTBER 4007 8040h + 0100h × m (m = 1 to 3)
GPT16m.GTBER 4007 8040h + 0100h × m (m = 4 to 6)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	CCRSWT	PR[1:0]		CCRB[1:0]		CCRA[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BD[1]	BD[0]
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	BD[0]	GTCCR Buffer Operation Disable	0: Enable buffer operation 1: Disable buffer operation.	R/W
b1	BD[1]	GTPR Buffer Operation Disable		R/W
b15 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit name	Description	R/W
b17, b16	CCRA[1:0]	GTCCRA Buffer Operation	b17 b16 0 0: No buffer operation 0 1: Single buffer operation (GTCCRA ↔ GTCCRC) 1 x: Double buffer operation (GTCCRA ↔ GTCCRC ↔ GTCCRD).	R/W
b19, b18	CCRB[1:0]	GTCCRB Buffer Operation	b19 b18 0 0: No buffer operation 0 1: Single buffer operation (GTCCRB ↔ GTCCRE) 1 x: Double buffer operation (GTCCRB ↔ GTCCRE ↔ GTCCRF).	R/W
b21, b20	PR[1:0]	GTPR Buffer Operation	b21 b20 0 0: No buffer operation 0 1: Single buffer operation (GTPBR → GTPR) 1 x: Setting prohibited.	R/W
b22	CCRSWT	GTCCRA and GTCCRB Forcible Buffer Operation	Writing 1 to this bit forces a buffer transfer of GTCCRA and GTCCRB. This bit automatically returns to 0 after 1 is writen. This bit is read as 0.	R/W
b31 to b23	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

GTBER provides settings for the buffer operation and must be set while the GTCNT operation stops.

BD[0] bit (GTCCR Buffer Operation Disable)

The BD[0] bit disables buffer operation using GTCCRA, GTCCRC, and GTCCRD combined and the buffer operation using GTCCRB, GTCCRE, and GTCCRF combined.

When GTDTCR.TDE is 1 and when BD[0] is set to 0, GTCCRB does not perform buffer operation. The GTCCRB register is automatically set to a compare match value for negative-phase waveform with dead time.

BD[1] bit (GTPR Buffer Operation Disable)

The BD[1] bit disables buffer operation using GTPR and GTPBR combined.

CCRA[1:0] bits (GTCCRA Buffer Operation)

The CCRA[1:0] bits set buffer operation using GTCCRA, GTCCRC, and GTCCRD combined. When the buffer operation is restricted by the operating mode set in GTCR, the GTCR setting is given priority.*1

CCRB[1:0] bits (GTCCRB Buffer Operation)

The CCRB[1:0] bits set buffer operation using GTCCRB, GTCCRE, and GTCCRF combined. When the buffer operation is restricted by the operating mode set in GTCR, the GTCR setting is given priority.*1

PR[1:0] bits (GTPR Buffer Operation)

The PR[1:0] bits set buffer operation using GTPR and GTPBR combined.

CCRSWT bit (GTCCRA and GTCCRB Forcible Buffer Operation)

Writing 1 to the CCRSWT bit forces a buffer transfer of GTCCRA and GTCCRB. This bit automatically returns to 0 after 1 is written. This bit is read as 0.

This bit is valid only when counting stops with the compare match operation specified.

Note 1. The buffer operation mode is fixed in saw-wave one-shot pulse mode or triangle-wave PWM mode 3 (64-bit transfer at trough).

20.2.18 General PWM Timer Counter (GTCNT)

Address(es): GPT320.GTCNT 4007 8048h
GPT16Hm.GTCNT 4007 8048h + 0100h × m (m = 1 to 3)
GPT16m.GTCNT 4007 8048h + 0100h × m (m = 4 to 6)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GTCNT is a 32-bit read/write counter for GPT320. For GPT16Hm (m = 1 to 3) and GPT16m (m = 4 to 6), GTCNT is a 16-bit register. GTCNT can only be written to after counting stops. GTCNT must be accessed in 32-bit units. Access in 8-bit/16-bit units is prohibited.

For GPT16Hm (m = 1 to 3) and GPT16m (m = 4 to 6), the upper 16 bits for access in a 32-bit unit are always read as 0000h, and writing to these bits is ignored.

GTCNT must be set within the range of 0 ≤ GTCNT ≤ GTPR.

20.2.19 General PWM Timer Compare Capture Register n (GTCCRn) (n = A to F)

Address(es): GPT320.GTCCRA 4007 804Ch
GPT320.GTCCRB 4007 8050h
GPT320.GTCCRC 4007 8054h
GPT320.GTCCRD 4007 805Ch
GPT320.GTCCRE 4007 8058h
GPT320.GTCCRF 4007 8060h

GPT16Hm.GTCCRA 4007 804Ch + 0100h × m (m = 1 to 3)
GPT16m.GTCCRA 4007 804Ch + 0100h × m (m = 4 to 6)
GPT16Hm.GTCCRB 4007 8050h + 0100h × m (m = 1 to 3)
GPT16m.GTCCRB 4007 8050h + 0100h × m (m = 4 to 6)
GPT16Hm.GTCCRC 4007 8054h + 0100h × m (m = 1 to 3)
GPT16m.GTCCRC 4007 8054h + 0100h × m (m = 4 to 6)
GPT16Hm.GTCCRD 4007 805Ch + 0100h × m (m = 1 to 3)
GPT16m.GTCCRD 4007 805Ch + 0100h × m (m = 4 to 6)
GPT16Hm.GTCCRE 4007 8058h + 0100h × m (m = 1 to 3)
GPT16m.GTCCRE 4007 8058h + 0100h × m (m = 4 to 6)
GPT16Hm.GTCCRF 4007 8060h + 0100h × m (m = 1 to 3)
GPT16m.GTCCRF 4007 8060h + 0100h × m (m = 4 to 6)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:*1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note 1. For GPT16Hm (m = 1 to 3) and GPT16m (m = 4 to 6), value of the upper 16 bits after reset is 0000h.

GTCCRn registers are read/write registers. The effective size of GTCCRn is the same as GTCNT (16- or 32-bit). If the effective size of GTCCRn is 16-bit, the upper 16 bits for access in a 32-bit unit are always read as 0000h, and writing to these bits is ignored.

GTCCRA and GTCCRB are registers used for both output compare and input capture.

GTCCRC and GTCCRE are compare match registers that can also function as buffer registers for GTCCRA and GTCCRB.

GTCCRD and GTCCRF are compare match registers that can also function as buffer registers for GTCCRC and

GTCCRE (double-buffer registers for GTCCRA and GTCCRB).

20.2.20 General PWM Timer Cycle Setting Register (GTPR)

Address(es): GPT320.GTPR 4007 8064h
GPT16Hm.GTPR 4007 8064h + 0100h × m (m = 1 to 3)
GPT16m.GTPR 4007 8064h + 0100h × m (m = 4 to 6)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:*1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note 1. For GPT16Hm (m = 1 to 3) and GPT16m (m = 4 to 6), value of the upper 16 bits after reset is 0000h.

GTPR is a read/write register that sets the maximum count value of GTCNT. The effective size of GTPR is same as GTCNT (16- or 32-bit). If the effective size of GTPR is 16-bit, the upper 16 bits for access in a 32-bit unit are always read as 0000h, and writing to these bits is ignored.

For saw waves, the value of (GTPR + 1) is the cycle. For triangle waves, the value of (GTPR value × 2) is the cycle.

20.2.21 General PWM Timer Cycle Setting Buffer Register (GTPBR)

Address(es): GPT320.GTPBR 4007 8068h
GPT16Hm.GTPBR 4007 8068h + 0100h × m (m = 1 to 3)
GPT16m.GTPBR 4007 8068h + 0100h × m (m = 4 to 6)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:*1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note 1. For GPT16Hm (m = 1 to 3) and GPT16m (m = 4 to 6), value of the upper 16 bits after reset is 0000h.

GTPBR is a read/write register that functions as a buffer register for GTPR. The effective size of GTPBR is the same as GTCNT (16- or 32-bit). If the effective size of GTPBR is 16-bit, the upper 16 bits for access in a 32-bit unit are always read as 0000h, and writing to these bits is ignored.

20.2.22 General PWM Timer Dead Time Control Register (GTDTCR)

Address(es): GPT320.GTDTCR 4007 8088h
GPT16Hm.GTDTCR 4007 8088h + 0100h × m (m = 1 to 3)
GPT16m.GTDTCR 4007 8088h + 0100h × m (m = 4 to 6)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TDE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TDE	Negative-Phase Waveform Setting	0: Set GTCCRB without using GTDVU 1: Use GTDVU to set the compare match value for negative-phase waveform with dead time automatically in GTCCRB.	R/W
b31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

GTDTCR enables the automatic setting of a compare match value for negative-phase waveform with dead time.

GPT has the dead time control function and the GTDVU register is used for setting dead time value.

TDE bit (Negative-Phase Waveform Setting)

The TDE bit specifies whether to use GTDVU. When GTDVU is used, the compare match value for a negative-phase waveform with dead time obtained by the compare match value of a positive-phase waveform (GTCCRA) and the dead time value (GTDVU) is automatically set in GTCCRB.

The TDE bit setting is ignored in saw-wave PWM mode, and automatic setting does not take place.

The GTCCRB value is automatically set and has the following upper and lower limit values. If the obtained GTCCRB value is not within the upper or lower limit, the following limit value is set in GTCCRB.

- Triangle waves:
  Upper limit value: GTPR – 1
  Lower limit value: 1 in up-counting, 0 in down-counting.
- Saw-wave one-shot pulse mode:
  Upper limit value: GTPR
  Lower limit value: 0.

20.2.23 General PWM Timer Dead Time Value Register U (GTDVU)

Address(es): GPT320.GTDVU 4007 808Ch
GPT16Hm.GTDVU 4007 808Ch + 0100h x m (m = 1 to 3)
GPT16m.GTDVU 4007 808Ch + 0100h x m (m = 4 to 6)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:*1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note 1. For GPT16Hm (m = 1 to 3) and GPT16m (m = 4 to 6), value of the upper 16 bits after reset is 0000h.

GTDVU is a read/write register that sets the dead time for generating PWM waveforms with dead time. The effective size of GTDVU is the same as GTCNT (16- or 32-bit). If the effective size of GTDVU is 16-bit, the upper 16 bits for access in a 32-bit unit are always read as 0000h, and writing to these bits is ignored.

Setting a dead time value that exceeds the cycle is prohibited. The set value can be confirmed by reading from GTCCRB. When GTDVU is used, writing to GTCCRB is prohibited. When this register is set to 0, waveforms without dead time are output.

While GPT is running, changing the GTDVU values is prohibited. To change GTDVU to a new value, the GPT should be stopped by the CST bit in the GTCR register. GTDVU must be accessed in 32-bit units. Access in 8-bit/16-bit units is prohibited.

20.2.24 Output Phase Switching Control Register (OPSCR)

Address(es): GPT_OPS.OPSCR 4007 8FF0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	NFCS[1:0]		NFEN	—	—	GODF	—	GRP	—	—	ALIGN	—	INV	N	P	FB
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	EN	—	W	V	U	—	WF	VF	UF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	UF	Input Phase Soft Setting	These bits set the input phase from the software settings. Setting these bits is valid when the OPSCR.FB bit = 1.	R/W
b1	VF			R/W
b2	WF			R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	U	Input U-Phase Monitor	These bits monitor the state of the input phase. OPSCR.FB = 0: External inputs that are synchronized by PCLKD are monitored by these bits OPSCR.FB = 1: The OPSCR.U, OPSCR.V and OPSCR.W bits can read the OPSCR.UF. OPSCR.VF, and OPSCR.WF bits.	R
b5	V	Input V-Phase Monitor		R
b6	W	Input W-Phase Monitor		R
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b8	EN	Enable-Phase Output Control	0: Do not Output (Hi-Z external pin) 1: Output*1.	R/W
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	FB	External Feedback Signal Enable	This bit selects the input phase from the software settings and external input: 0: Select the external input 1: Select the soft setting (OPSCR.UF, VF, WF).	R/W
b17	P	Positive-Phase Output (P) Control	0: Level signal output 1: PWM signal output (PWM of GPT16H1).	R/W
b18	N	Negative-Phase Output (N) Control	0: Level signal output 1: PWM signal output (PWM of GPT16H1).	R/W
b19	INV	Invert-Phase Output Control	0: Positive logic (active-high) output 1: Negative logic (active-low) output.	R/W
b20	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b21	ALIGN	Input Phase Alignment	0: Input phase is aligned to PCLKD 1: Input phase is aligned PWM.	R/W
b23, b22	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b24	GRP	Output Disabled Source Selection	0: Select group A output disable source 1: Select group B output disable source.	R/W

Bit	Symbol	Bit name	Description	R/W
b25	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b26	GODF	Group Output Disable Function	0: This bit function is ignored 1: Group disable clears the OPSCR.EN bit*1.	R/W
b28, b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b29	NFEN	External Input Noise Filter Enable	0: Do not use a noise filter to the external input 1: Use a noise filter to the external input.	R/W
b31, b30	NFCS[1:0]	External Input Noise Filter Clock Selection	Noise filter sampling clock setting of the external input: b31 b30 0 0: PCLKD/1 0 1: PCLKD/4 1 0: PCLKD/16 1 1: PCLKD/64.	R/W

Note 1. When OPSCR.GODF = 1 and signal value selected by the OPSCR.GRP bit is high, the OPSCR.EN bit is cleared to 0.

The OPSCR register sets the output of the signal waveform required for brushless DC motor control.

UF, VF, WF bits (Input Phase Soft Setting)

These bits set the input phase from the software settings.

When OPSCR.FB bit is 1, these bits are valid. The set value of the UF/VF/WF takes the place of the U/V/W external input.

U, V, W bits (Input Phase Monitor)

When OPSCR.FB bit is 0, external inputs that are synchronized by PCLKD, are monitored by these bits.

When OPSCR.FB bit is 1, the OPSCR.U, OPSCR.V, and OPSCR.W bits can read the OPSCR.UF, OPSCR.VF, and OPSCR.WF bits.

EN bit (Enable-Phase Output Control)

The EN bit controls the output enable signal output phase (positive phase/reverse phase). When OPSCR.EN bit is 1, the signal waveform is output.

When OPSCR.EN bit is 0, first set OPSCR.FB, OPSCR.UF/VF/WF (software setting is selected), OPSCR.P/N, OPSCR.INV, OPSCR.RV, OPSCR.ALIGN, OPSCR.GRP, OPSCR.GODF, OPSCR.NFEN, OPSCR.NFCS. Then, set this bit to 1. Also when OPSCR.GODF is 1 and the signal value selected by the OPSCR.GRP bit is high, the OPSCR.EN bit is cleared to 0.

FB bit (External Feedback Signal Enable)

The FB bit selects the input phase from the software settings (OPSCR.UF, VF, WF) and external input such as a Hall element.

P bit (Positive-Phase Output (P) Control)

The P bit selects one of the level signal output or PWM signal output for the positive-phase output (GTOUUP pin, GTOVUP pin, GTOWUP pin).

N bit (Negative-Phase Output (N) Control)

The N bit selects one of the level signal output or PWM signal output for the negative-phase output (GTOULO pin, GTOVLO pin, GTOWLO pin).

INV bit (Invert-Phase Output Control)

The INV bit selects one of the positive logic (active-high) output or negative logic (active-low) output for the output phase.

ALIGN bit (Input Phase Alignment)

The ALIGN bit selects the PCLKD or PWM for the sampling of the input phase (input phase is specified in the

OPSCR.FB bit). When OPSCR.ALIGN bit is 0, input phase is aligned to PCLKD.

Note: When PWM output is selected (OPSCR.P/N is 1) and the PCLKD input phase is aligned, the PWM pulse may be short-pulsed.

Note: When OPSCR.ALIGN bit is 1, input phase is aligned with PWM output.

GRP bit (Output Disabled Source Selection)

The GRP bit selects the output disable source A to B.

GODF bit (Group Output Disable Function)

When OPSCR.GODF is 1 and signal value selected by the OPSCR.GRP bit is high, the OPSCR.EN bit is cleared to 0. When OPSCR.GODF bit is 0, this bit is ignored.

NFEN bit (External Input Noise Filter Enable)

The NFEN bit selects the noise filter for external input. When OPSCR.NFEN bit is 0, a noise filter to the external input is not used. When OPSCR.NFEN bit is 1, a noise filter to the external input is used.

Note: When this bit is switched, because an unintentional internal edge occurs, first set OPSCR.EN bit = 0.

NFCS[1:0] bits (External Input Noise Filter Clock Selection)

When OPSCR.NFEN bit is 1, noise filter sampling clock setting of the external input is enabled.

1. Set the NFCS.
2. Wait for 2 cycles.
3. Set the OPSCR.EN bit to 1.

20.3 Operation

20.3.1 Basic Operation

Each channel has a 32-bit timer that performs a periodic count operation using the count clock and hardware sources. The count function provides both up-counting and down-counting. The GTPR controls the count cycle.

When the GTCNT counter value matches the value in GTCCRA or GTCCRB, the output from the corresponding pin GTIOCA or GTIOCB can be changed. GTCCRA or GTCCRB can be used as an input capture register with hardware resources.

GTCCRC and GTCCRD can function as buffer registers for GTCCRA. GTCCRE and GTCCRF can function as buffer registers for GTCCRB.

20.3.1.1 Counter operation

(1) Counter start/stop

The counter of each channel starts the count operation by setting GTCR.CST to 1 and stops the count operation by setting GTCR.CST to 0.

The GTCR.CST bit value is changed by the following sources:

- Writing to GTCR register
- Writing 1 to the bit in GTSTR associated with the GPT channel number when the GTSSR.CSTRT bit set to 1
- Writing 1 to the bit in GTSTP associated with the GPT channel number when the GTPSR.CSTOP bit set to 1
- The hardware source selected in the GTSSR register
- The hardware source selected in the GTPSR register.

(2) Periodic count operation in up-counting by count clock

The GTCNT counter in each channel starts up-counting when the corresponding GTCR.CST bit is set to 1 with GTUPSR and GTDNSR registers set to 00000000h. When the GTCNT value changes from the GTPR value to 0 (overflow), the GTST.TCFPO flag is set to 1. After GTCNT overflows, up-counting is resumed from 00000000h.

Figure 20.3 shows an example of a periodic count operation in up-counting.

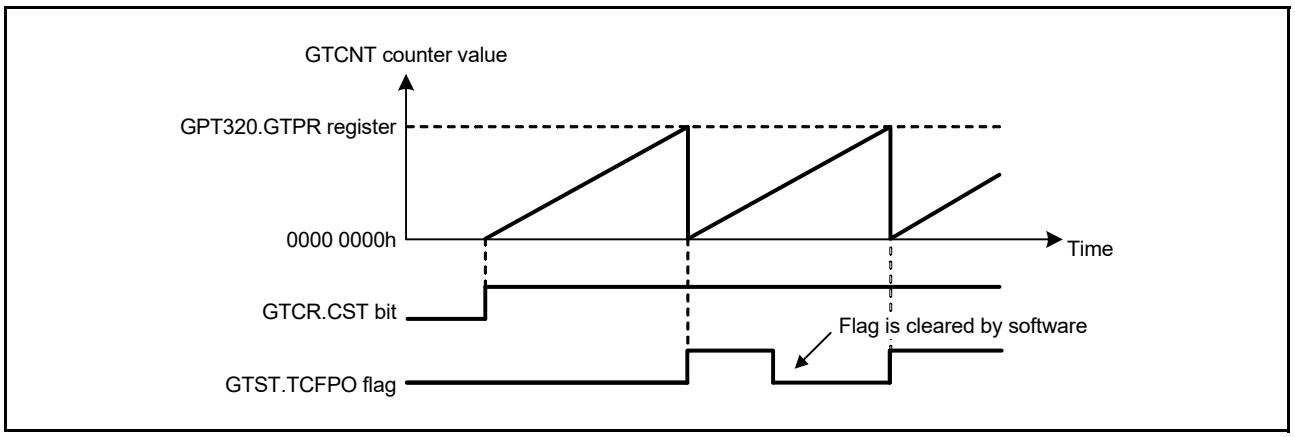


Figure 20.3 Example of periodic count operation in up-counting by the count clock

Figure 20.4 shows an example for setting periodic count operation in up-counting.

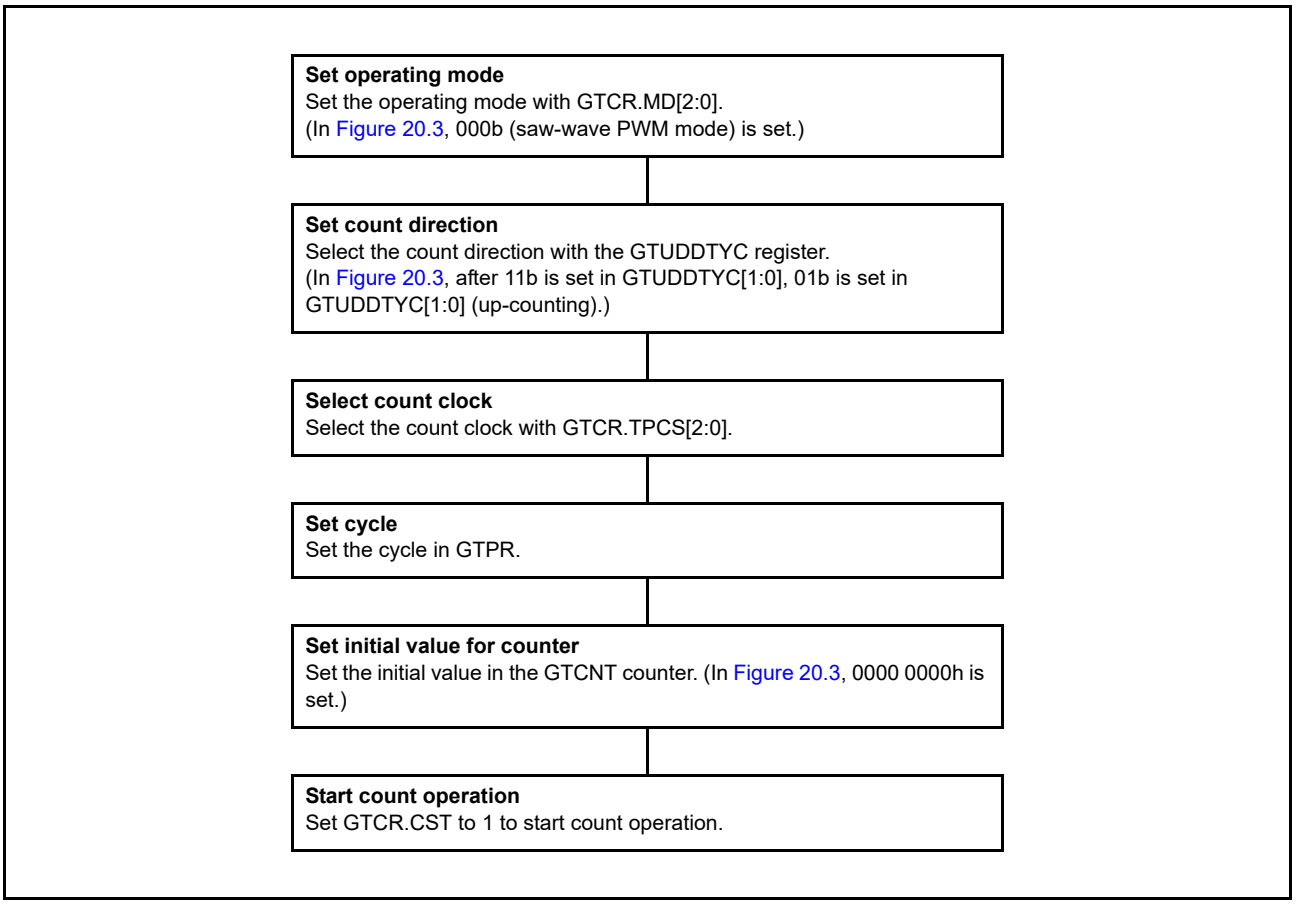


Figure 20.4 Example for setting a periodic count operation in up-counting by the count clock

(3) Periodic count operation in down-counting by count clock

The GTCNT counter in each channel can perform down-counting by setting GTUDDTYC.UD with GTUPSR and GTDNSR registers set to 00000000h. When GTCNT changes from 0 to the GTPR value (underflow), GTST.TCFPU is set to 1. After the GTCNT counter underflows, down-counting is resumed from the GTPR value.

Figure 20.5 shows an example of periodic count operation in down-counting by the count clock.

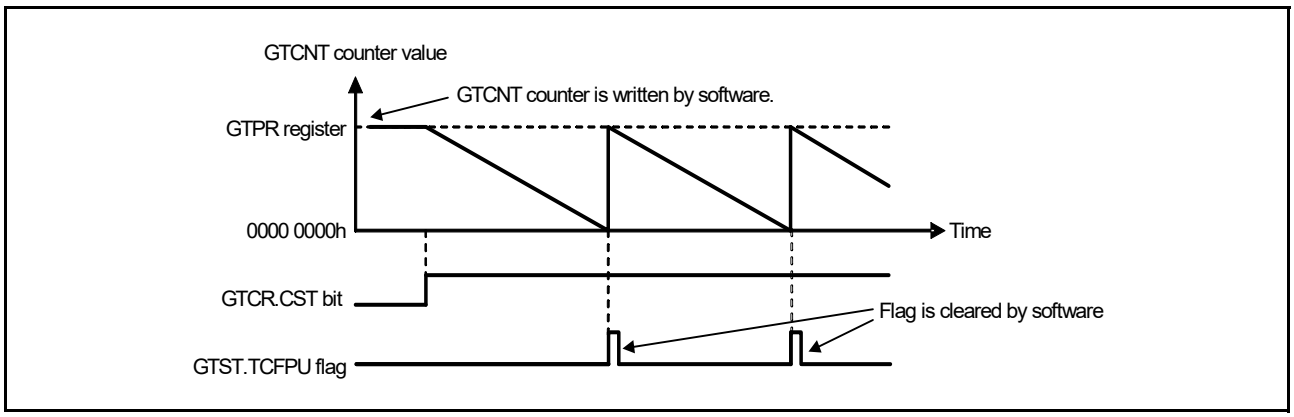


Figure 20.5 Example of periodic count operation in down-counting by the count clock

Figure 20.6 shows an example for setting periodic count operation in down-counting by the count clock.

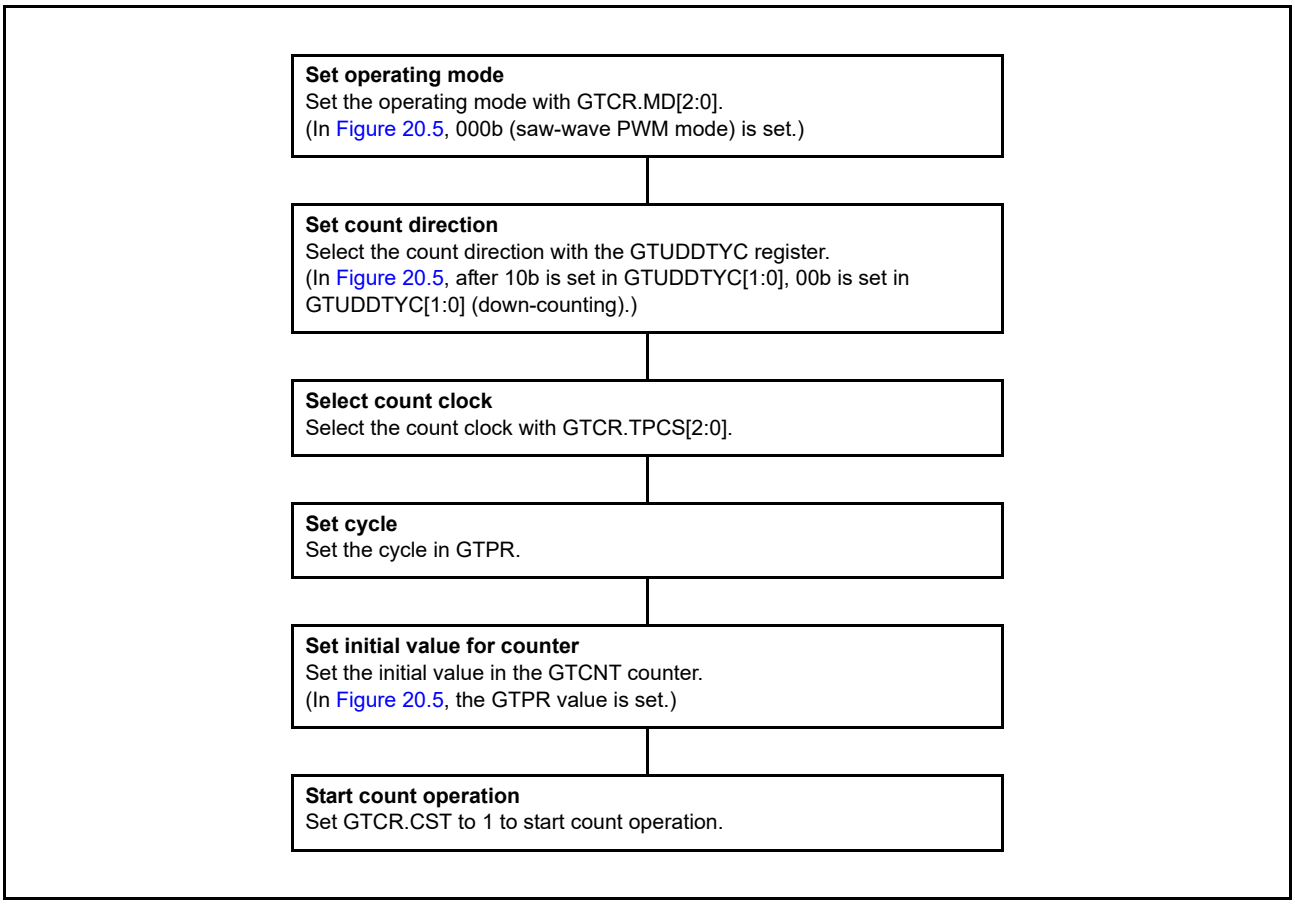


Figure 20.6 Example for setting periodic count operation in down-counting by count clock

(4) Event count operation in up-counting using hardware sources

The GTCNT counter in each channel can perform up-counting using hardware sources as set in GTUPSR.

When GTUPSR is set to enable, the count clock selected in GTCR.TPCS[2:0] and the count direction selected in GTUDDTYC.UD are ignored. If up-counting and down-counting using hardware sources occur at the same time, the GTCNT counter value does not change. The overflow behavior when up-counting using hardware sources is the same as when up-counting by the count clock.

If you are using a hardware source to count up, set the GTCR.CST bit to 1 to enable the counting operation. After GTCR.CST is set to 1, the counter cannot count up for 1 clock cycle as specified by GTCR.TPCS[2:0] because the count operation is synchronized by the count clock selected by GTCR.TPCS[2:0]. Set GTCR.TPCS[2:0] to 000b to count up with a 1 PCLKD delay after GTCR.CST is set to 1.

Figure 20.7 shows an example of a periodic count operation in up-counting by a hardware resource (rising edge of GTETRGA pin).

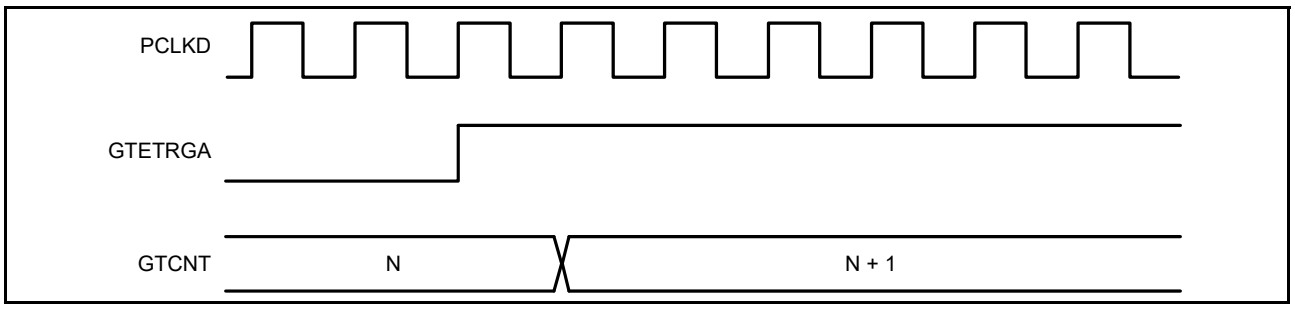


Figure 20.7 Example of periodic count operation in up-counting using hardware sources

Figure 20.8 shows an example for setting periodic count operation in down-counting by the count clock.

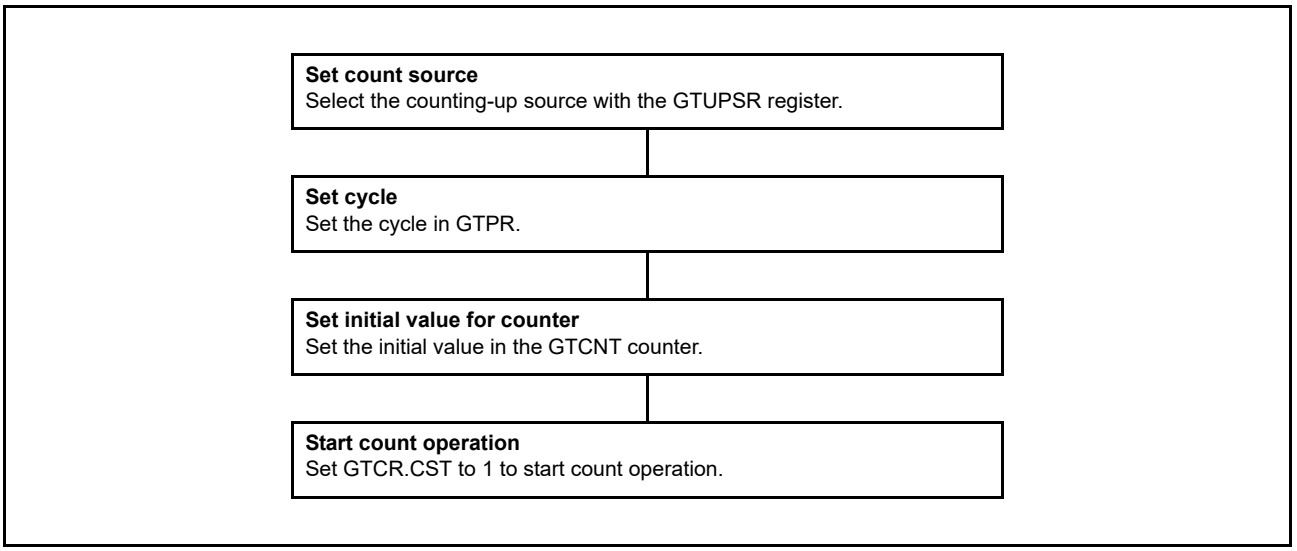


Figure 20.8 Example for setting an event count operation in up-counting using hardware sources

(5) Event count operation in down-counting using hardware sources

The GTCNT counter in each channel can perform down-counting using hardware sources set in the GTDNSR.

When GTDNSR is set to enable, the count clock selected in GTCR.TPCS[2:0] and the count direction selected in GTUDDTYC.UD are ignored. If up-counting and down-counting using hardware sources occur at the same time, the GTCNT counter value does not change. The underflow behavior when down-counting using hardware sources is the same as when down-counting by the count clock.

When GTCR.CST bit is set to 1 to count down using hardware sources, the count operation is enabled. After GTCR.CST is set to 1, the counter cannot count down for 1 clock cycle as specified by GTCR.TPCS[2:0] because the count operation

is synchronized with the count clock selected by GTCR.TPCS[2:0]. Set GTCR.TPCS[2:0] to 000b to count down with a 1 PCLKD delay after GTCR.CST is set to 1.

Figure 20.9 shows an example of a periodic count operation in down-counting by a hardware resource (rising edge of GTETRGA pin).

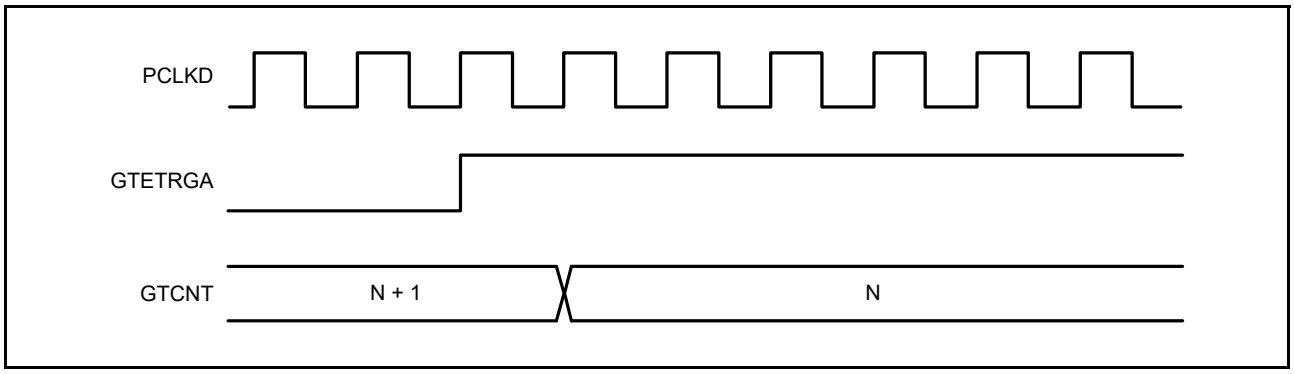


Figure 20.9 Example of event count operation in down-counting using hardware sources

Figure 20.10 shows an example for setting a periodic count operation in down-counting using a hardware resource.

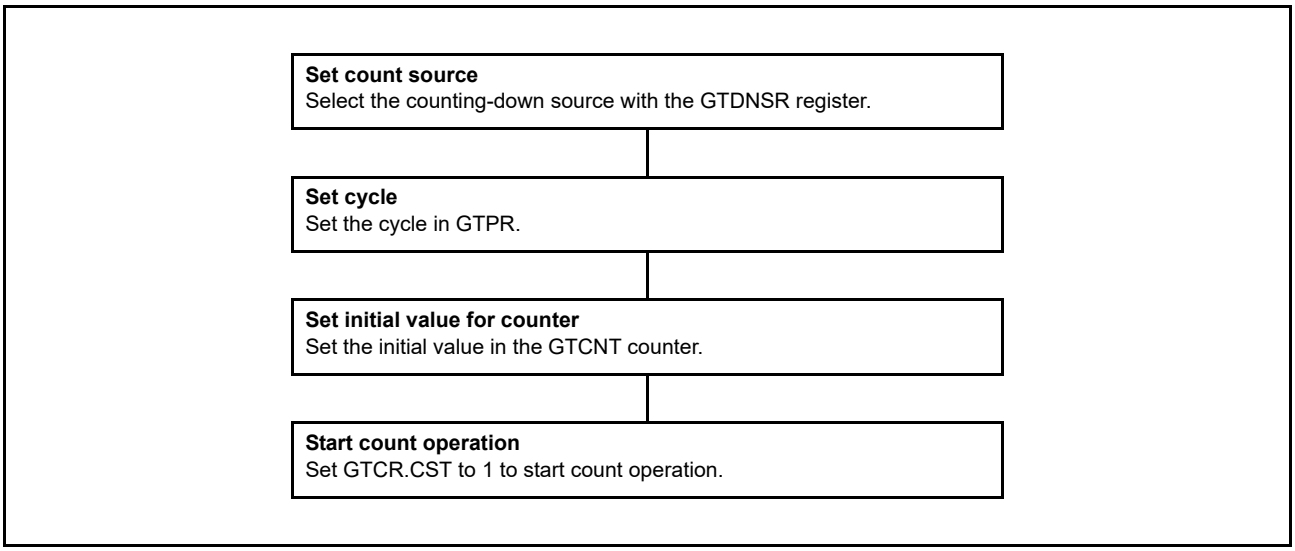


Figure 20.10 Example for setting an event count operation in down-counting using hardware sources

(6) Counter clear operation

The counter of each channel is cleared by following sources:

- Writing 0 to GTCNT register
- Writing 1 to the bit in GTCLR associated with the GPT channel number when the GTCSR.CCLR bit set to 1
- The hardware source selected in GTCSR register.

Writing to the GTCNT register is prohibited during count operation. The GTCNT counter can be cleared both by writing 1 to the GTCLR and by the clear request of hardware sources, whether GTCNT is counting (GTCR.CST is 1) or not (GTCR.CST is 0).

For saw waves selected by setting GTCR.MD[2:0] and the count direction flag showing down-counting (GTST.TUCF is 0), the GTCNT register is set to the value of the GTPR register when writing 1 to the GTCLR register or when clearing by hardware sources are performed.

When not in saw waves mode and down-counting, the GTCNT register is set to 0 when writing 1 to the GTCLR register and when clearing by hardware sources are performed.

In event count operation when at least 1 bit in the GTUPSR or GTDNSR is set to 1, after clear sources occur, both writing to GTCLR register and clearing by hardware sources are performed immediately to synchronize with PCLKD.

If other settings are used, clear is synchronized with the counter clock selected by GTCR.TPCS[2:0].

20.3.1.2 Waveform output by compare match

Compare match means that the GTCNT counter value matches the value of GTCCRA or GTCCRB.

When a compare match occurs, the compare match flag is generated synchronously with the count clock including the event count. At the same time, the GPT can output low, high, or toggle output from the corresponding GTIOCA or GTIOCB output pin.

In addition, the GTIOCA or GTIOCB pin output can be low, high, or toggled at the cycle end which is determined by GTPR.

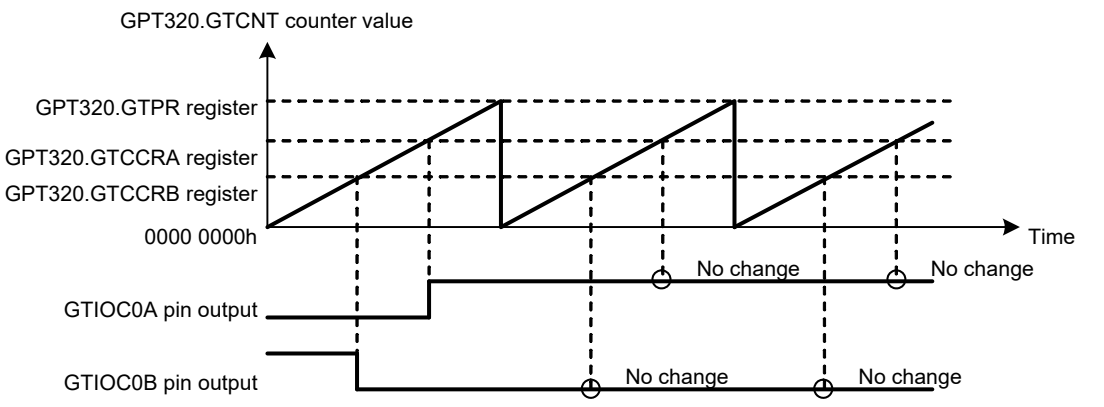
The cycle end is:

- For saw waves in up-counting — When GTCNT changes from the GTPR value to 0 (overflow)
- For saw waves in down-counting — When GTCNT changes from 0 to GTPR value (underflow)
- For saw waves — When the GTCNT counter is cleared
- For triangle waves — When the GTCNT changes from 0 to 1 (trough).

(1) Low output and high output

Figure 20.11 shows an example of low output and high output operation by a compare match of GTCCRA and GTCCRB.

In this example, the GPT320.GTCNT counter performs up-counting, and settings are made so that high is output from the GTIOC0A pin by a GPT320.GTCCRA compare match, and low is output from the GTOC0B pin by a GPT320.GTCCRB compare match. The pin level does not change when the specified level and pin level match.



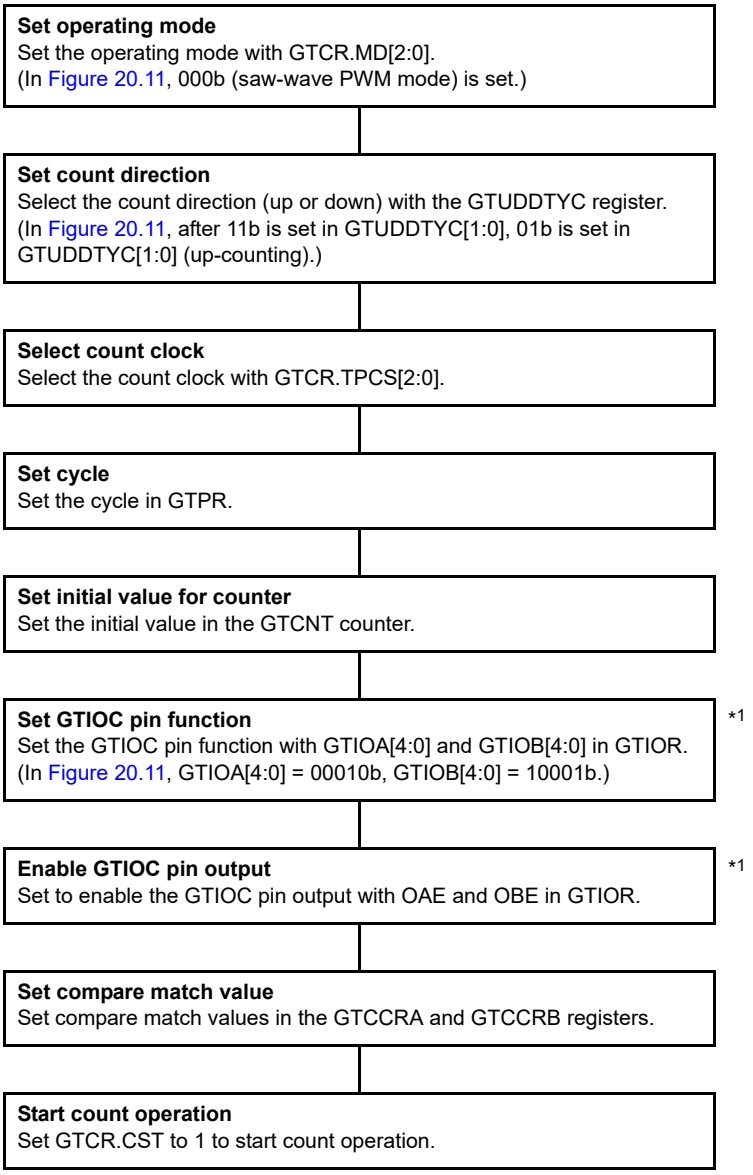
[Setting examples]

GPT320.GTIOR.GTIOA[4:0] bits: Initial output is low, high output at compare match, output retained at cycle end

GPT320.GTIOR.GTIOB[4:0] bits: Initial output is high, low output at compare match, output retained at cycle end

Figure 20.11 Example of low output and high output operation

Figure 20.12 shows an example for setting low output and high output operation.



Note 1. When PWM delay generate circuit is used, reverse the setting order of set GTIOC pin function and enable GTIOC pin output.

Figure 20.12 Example for setting low output and high output operation

(2) Toggled output

Figure 20.13 and Figure 20.14 show examples of toggled output operation by compare matches of GTCCRA and GTCCRB. In Figure 20.13, the GPT320.GTCNT counter performs up-counting, and settings are made so that the GTIOC0A pin output by a GPT320.GTCCRA compare match and GTIOC0B pin output by a GPT320.GTCCRB compare match are toggled.

In Figure 20.14, the GPT320.GTCNT counter performs up-counting, and settings are made so that the GTIOC0A output is toggled by a compare match of GPT320.GTCCRA and the GTIOC0B output is toggled at the cycle end.

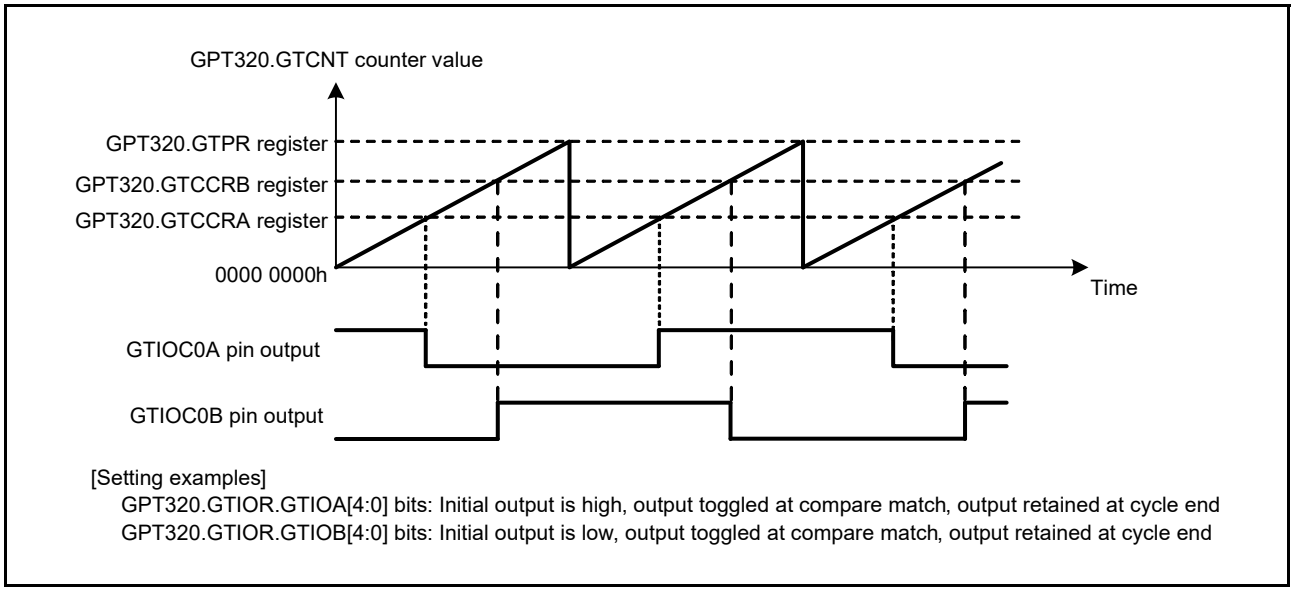


Figure 20.13 Example of toggled output operation (1)

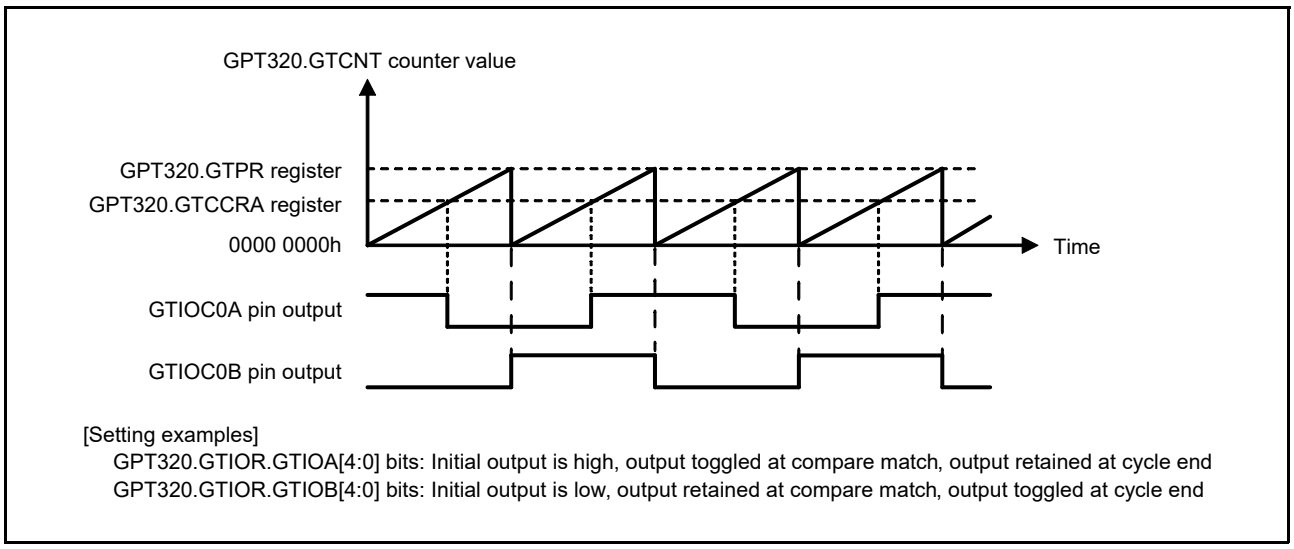
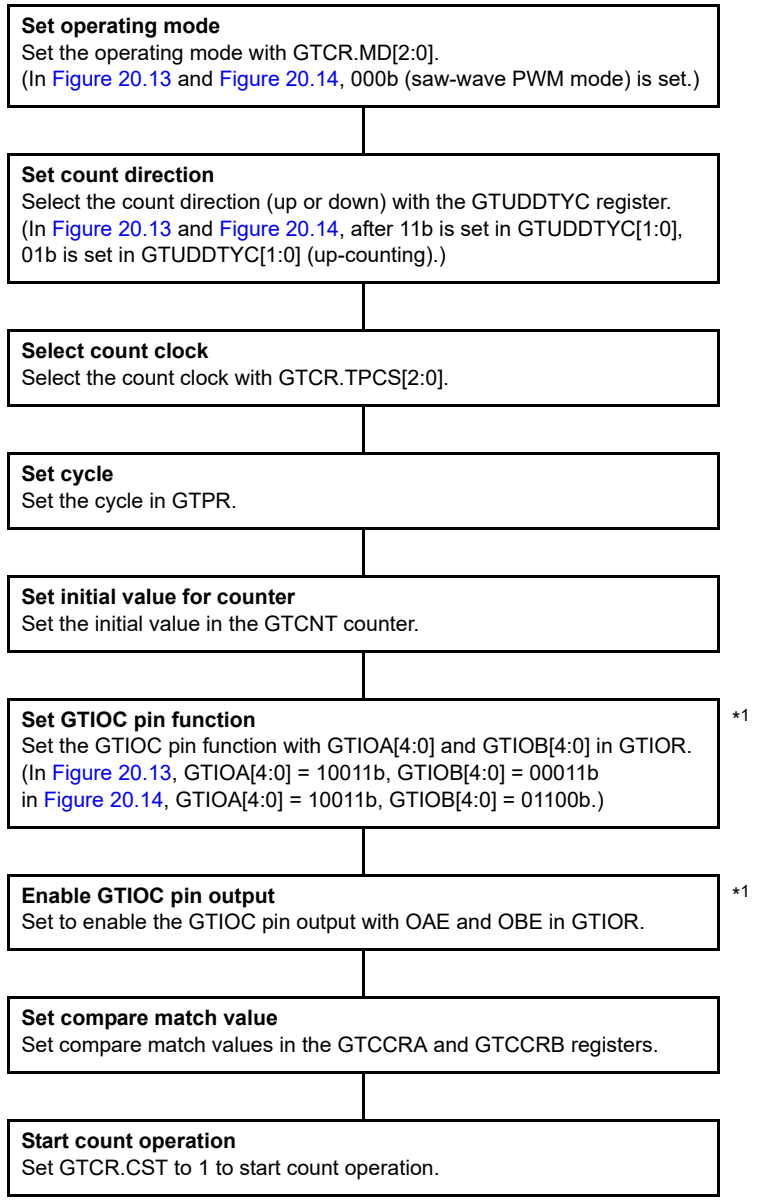


Figure 20.14 Example of toggled output operation (2)

Figure 20.15 shows an example for setting toggled output operation.



Note 1. When PWM delay generate circuit is used, reverse the setting order of set GTIOC pin function and enable GTIOC pin output.

Figure 20.15 Example for setting toggled output operation

20.3.1.3 Input capture function

The GTCNT counter value can be transferred to either GTCCRA or GTCCRB on detection of the hardware source that is set in GTICASR and GTICBSR.

Figure 20.16 shows an example of the input capture function.

In this example, the GPT320.GTCNT counter performs up-counting by the count clock, and settings are made so that an input capture is performed to GTCCRA at both edges of the GTIOC0A input pin and to GTCCRB on the rising edge of the GTIOC0B input pin.

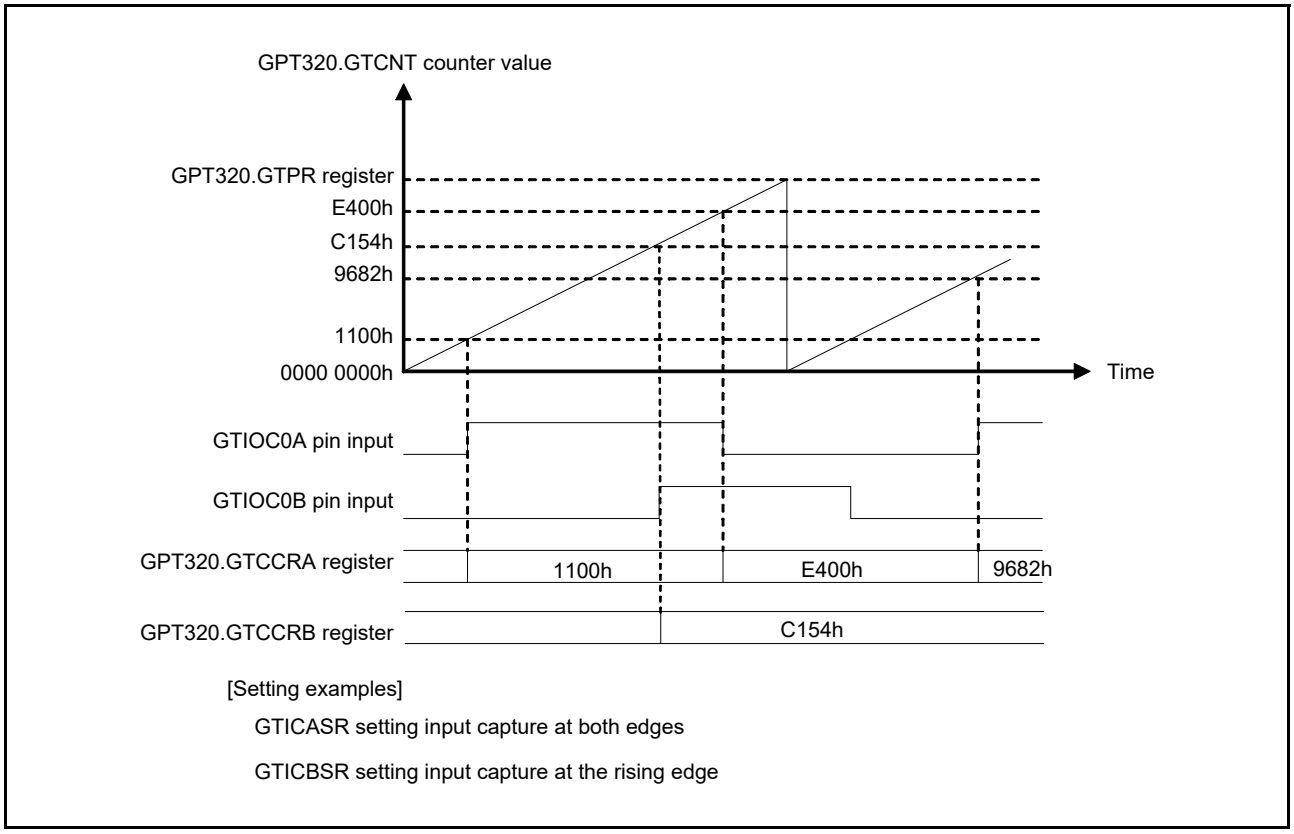


Figure 20.16 Example of input capture operation

Figure 20.17 shows an example for setting an input capture operation with count operation by the count clock.

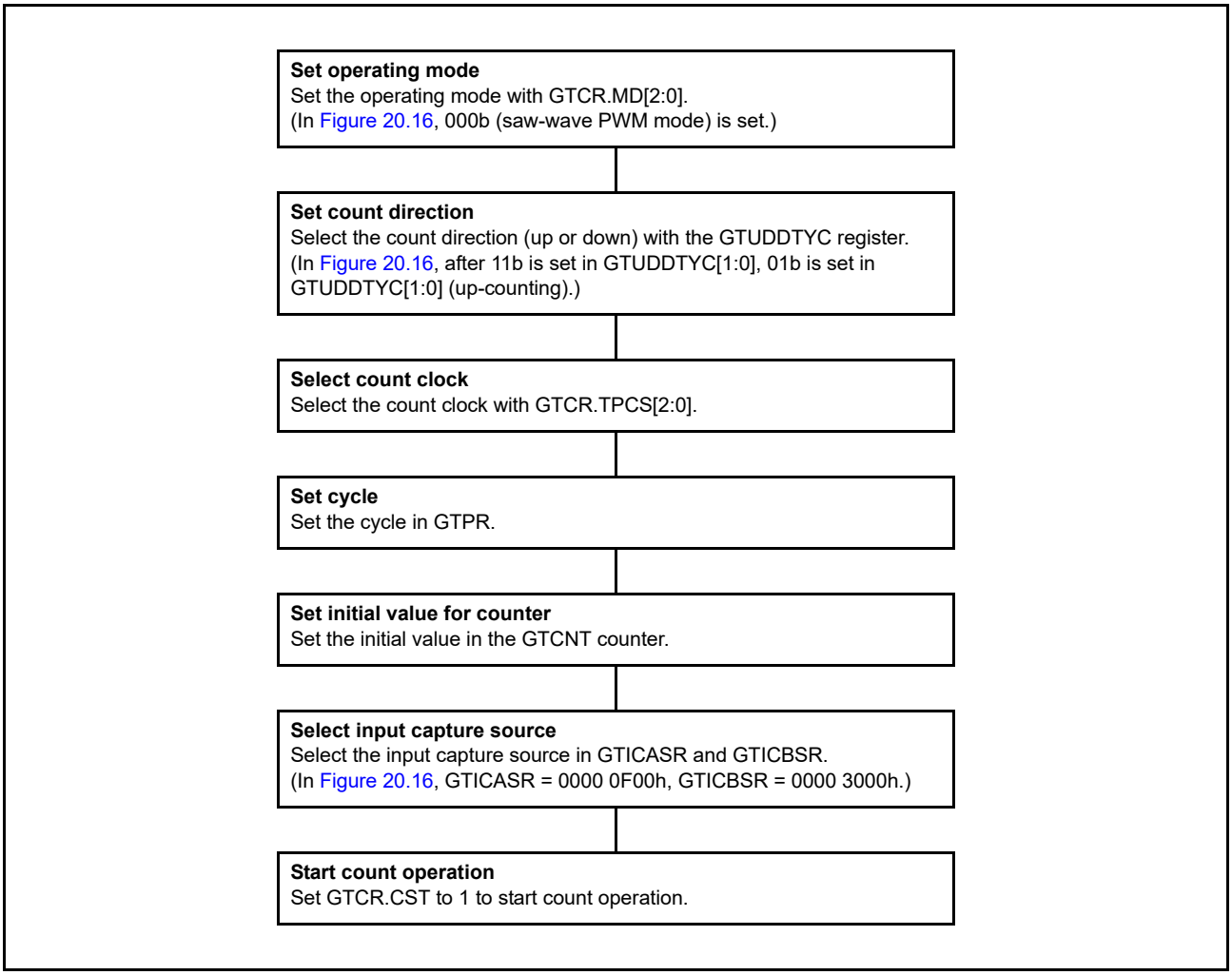


Figure 20.17 Example for setting input capture operation

20.3.2 Buffer Operation

The following buffer operations can be set with GTBER:

- Buffer operation with GTPR and GTPBR combined
- Buffer operation with GTCCRA, GTCCRC, and GTCCRD combined
- Buffer operation with GTCCRB, GTCCRE, and GTCCRF combined.

20.3.2.1 GTPR register buffer operation

GTPBR can function as a buffer register for GTPR. The buffer transfer is performed at an overflow (during up-counting) or an underflow (during down-counting) in saw-wave mode or in event count, and at a trough in triangle-wave mode.

In saw-wave mode or in event count, the buffer transfer is performed when the following counter clear operations occur during counting:

- Clear by hardware sources (the clear source is selected in GTCSR[23:0])
- Clear by software (when GTCSR.CCLR bit is 1 and GTCLR[n] bit is set to 1, n = channel number).

Figure 20.18 to Figure 20.20 show examples of GTPR buffer operation and Figure 20.21 shows an example for setting GTPR buffer operation.

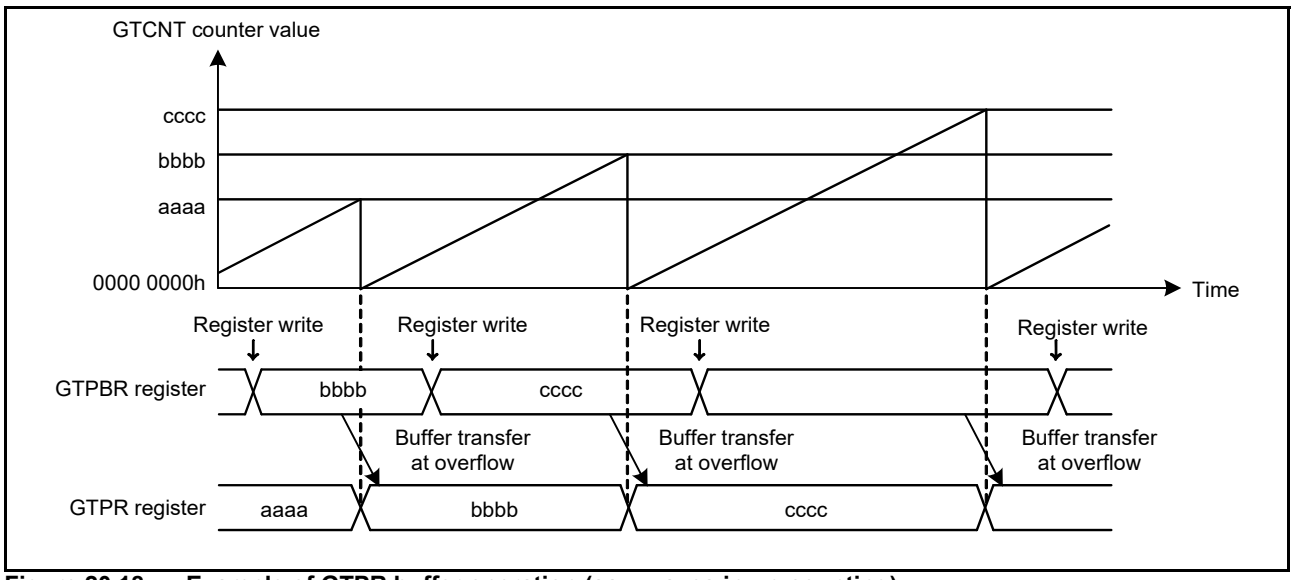


Figure 20.18 Example of GTPR buffer operation (saw waves in up-counting)

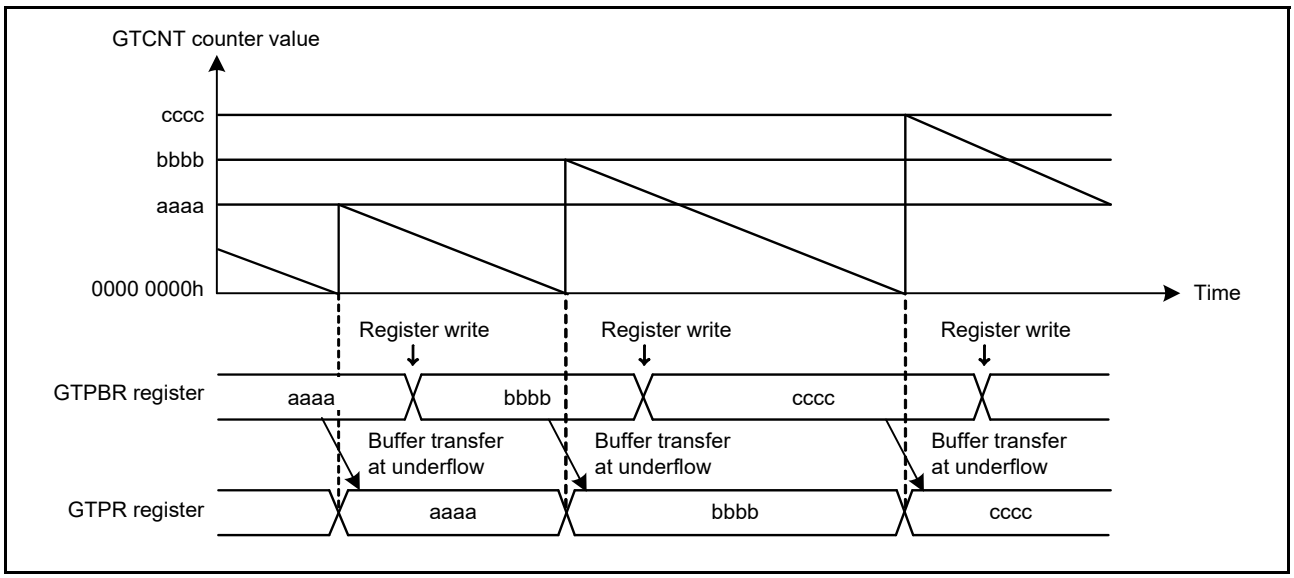


Figure 20.19 Example of GTPR buffer operation (saw waves in down-counting)

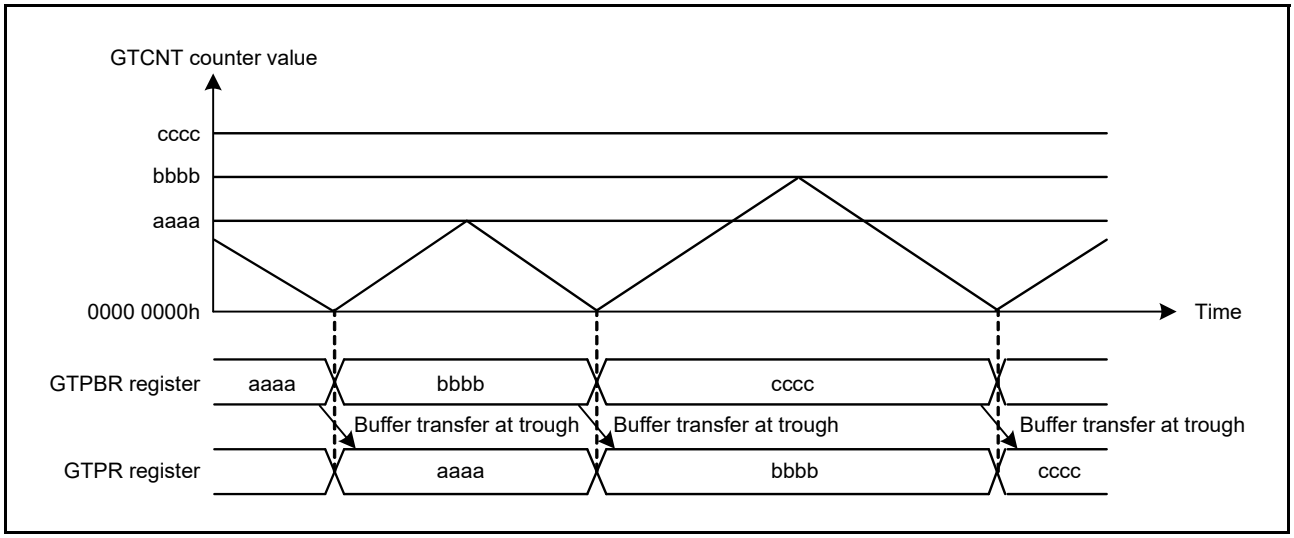


Figure 20.20 Example of GTPR buffer operation (triangle waves)

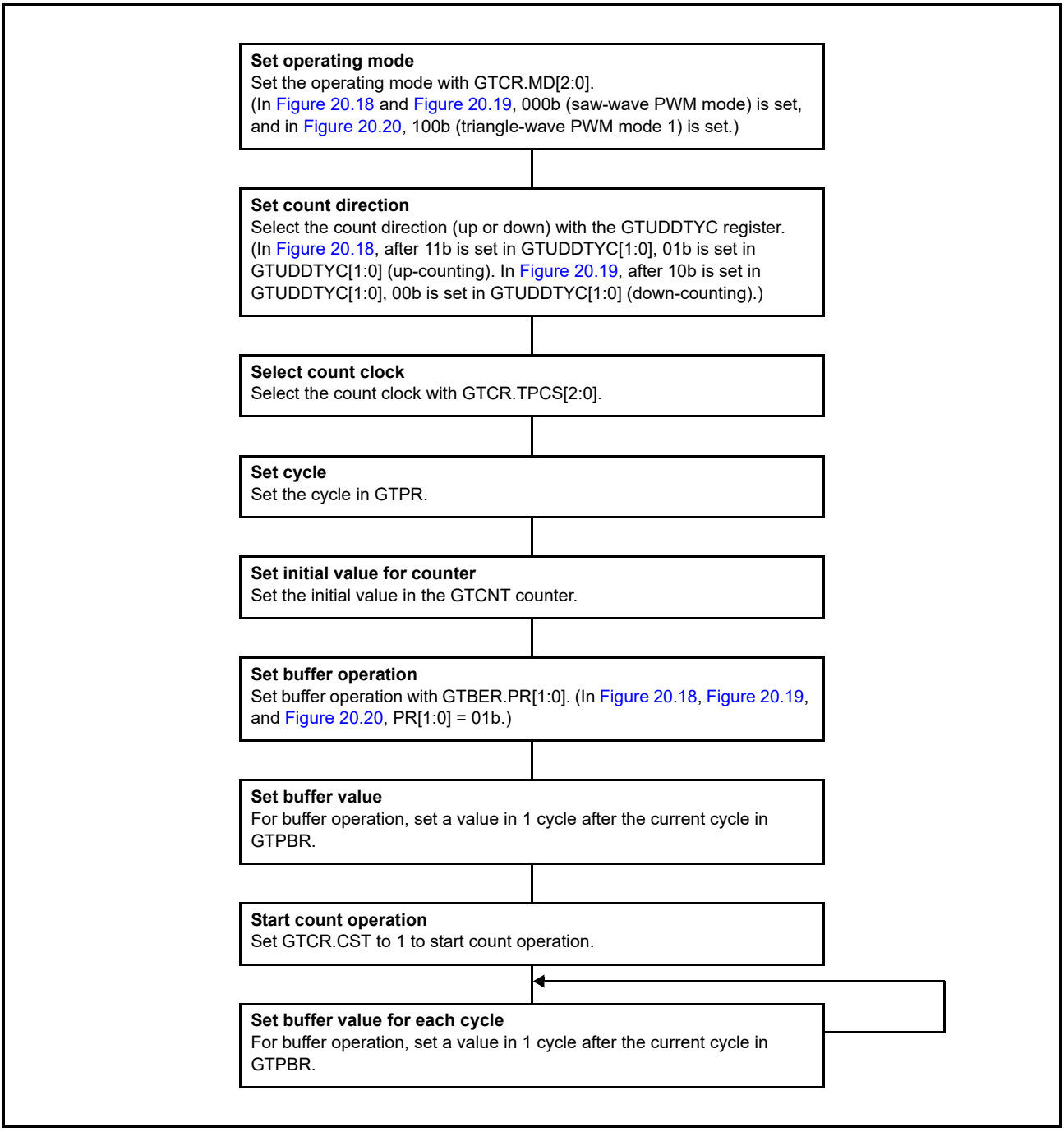


Figure 20.21 Example for setting GTPR buffer operation

20.3.2.2 Buffer operation for GTCCRA and GTCCRB

GTCCRC can function as the GTCCRA buffer register and GTCCRD can function as the GTCCRC buffer register (double-buffer register for GTCCRA). Similarly, GTCCRE can function as the GTCCRB buffer register and GTCCRF can function as the GTCCRE buffer register (double-buffer register for GTCCRB).

To set GTCCRA or GTCCRB to function as a double buffer, set GTBER.CCRA[1:0] or GTBER.CCRB[1:0] to 10b or 11b. For single buffer operation, set 01b. To set GTCCRA or GTCCRB to not function as a buffer, set 00b.

(1) When GTCCRA or GTCCRB functions as output compare register

Buffer transfer has the following cases:

- Buffer transfer by overflow or underflow

Buffer transfer is performed at an overflow (during up-counting) or an underflow (during down-counting) in saw-wave mode or in event count operation. In triangle-wave mode, buffer transfer is performed at a trough (triangle-wave PWM mode 1) or a crest and trough (triangle-wave PWM mode 2).

- Buffer transfer by counter clear
  In saw-wave mode or in event count operation, during counting, buffer transfer (which is the same as an overflow during up-counting or an underflow during down-counting) is performed by the counter clear sources the same as in the case of section 20.3.2.1, GTPR register buffer operation.
  In triangle-wave mode, buffer transfer is not performed by the counter clear.

- Forcible buffer transfer
  When GTBER.CCRSWT bit is set to 1 while the count operation stops, the GTCCRA and the GTCCRB register buffer transfer are performed forcibly in saw-wave mode, in event count operation and in triangle-wave mode. Additionally buffer transfer from the GTCCRD register to temporary register A and from the GTCCRF register to temporary register B are performed in saw-wave 1 shot pulse mode or triangle-wave PWM mode 3.

Figure 20.22 to Figure 20.24 show examples of GTCCRA and GTCCRB buffer operation and Figure 20.25 shows an example for setting GTCCRA and GTCCRB buffer operation.

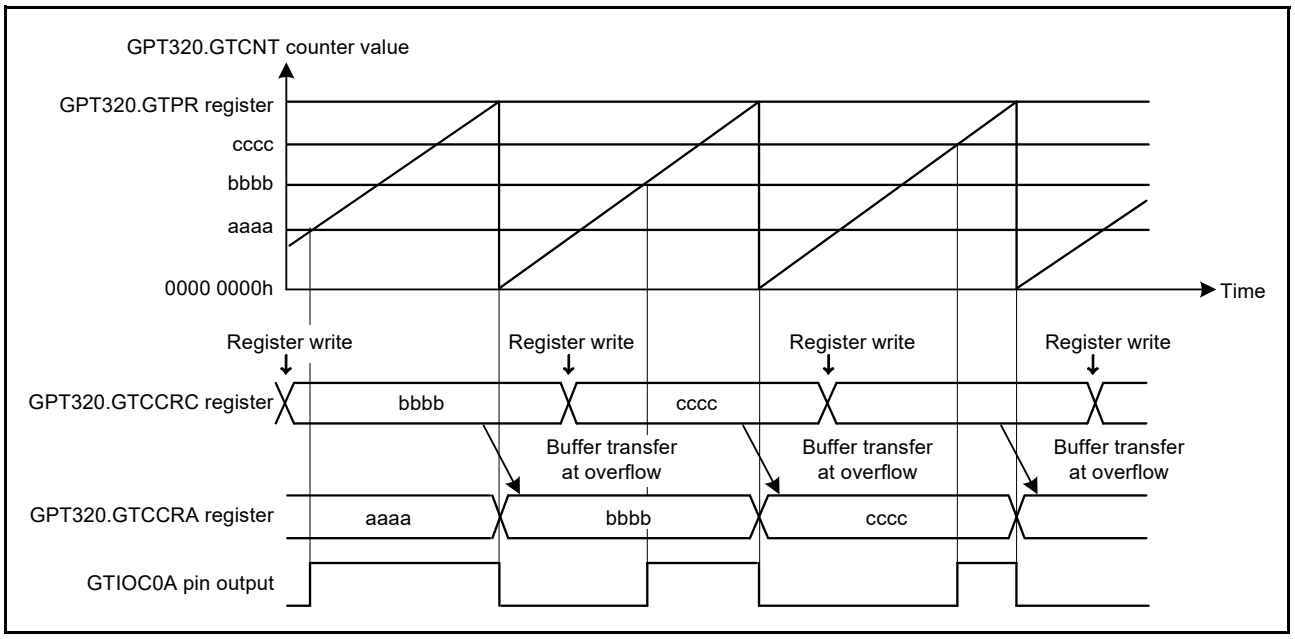


Figure 20.22 Example of GTCCRA and GTCCRB buffer operation with output compare, saw waves in up-counting, high output at GTCCRA compare match, and low output at cycle end

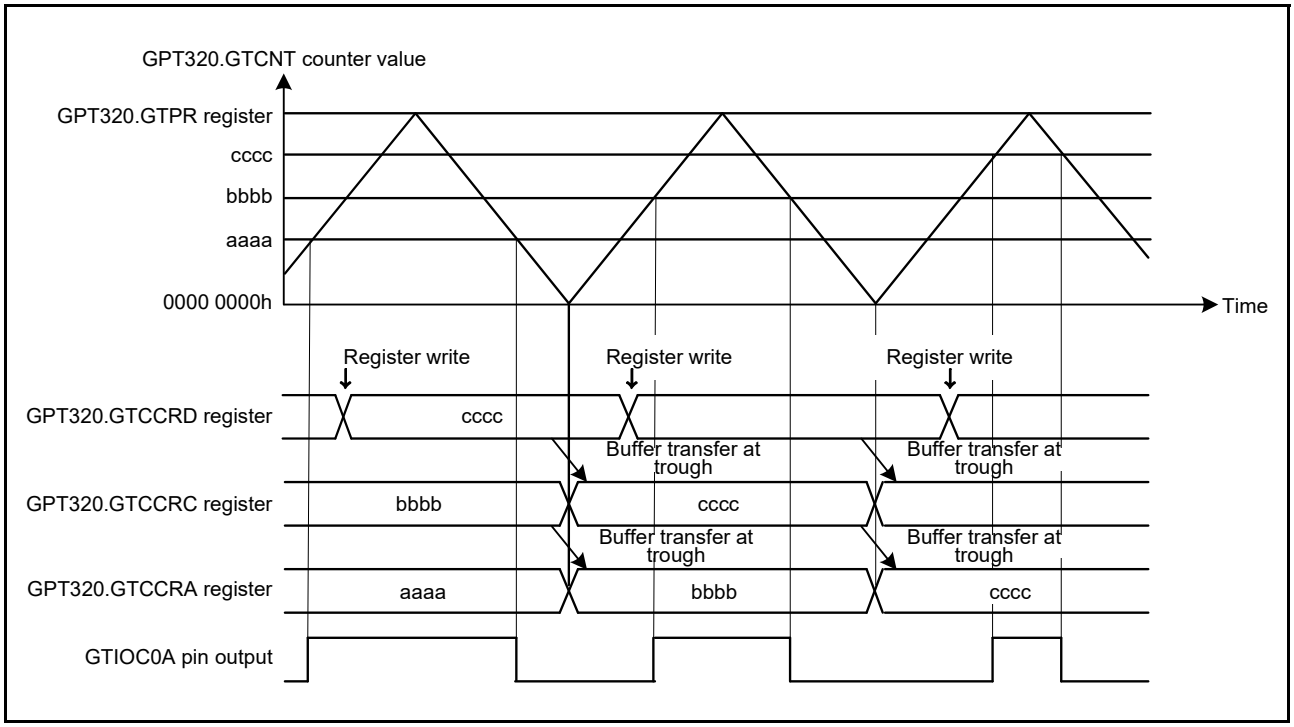


Figure 20.23 **Example of GTCCRA and GTCCRB double buffer operation with output compare, triangle waves, buffer operation at trough, output toggled at GTCCRA compare match, and output retained at cycle end**

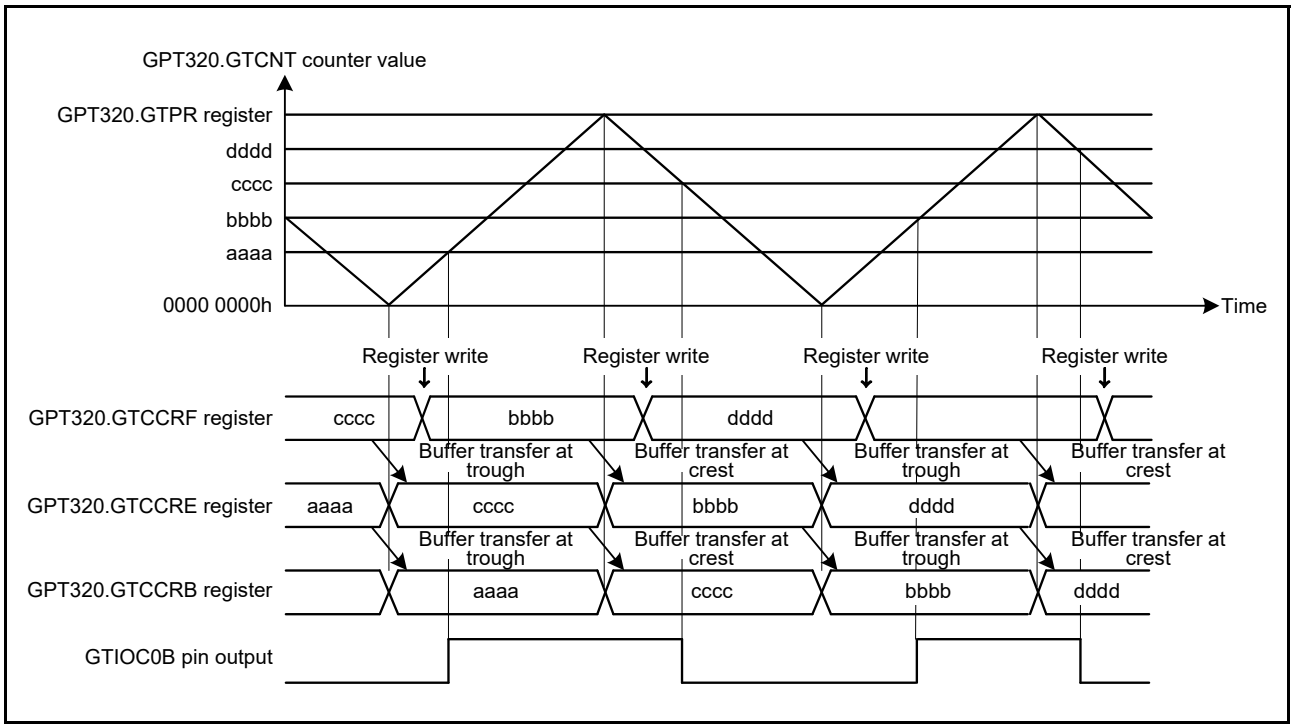


Figure 20.24 **Example of GTCCRA and GTCCRB double buffer operation with output compare, triangle waves, buffer operation at both troughs and crests, output toggled at GTCCRB compare match, and output retained at cycle end**

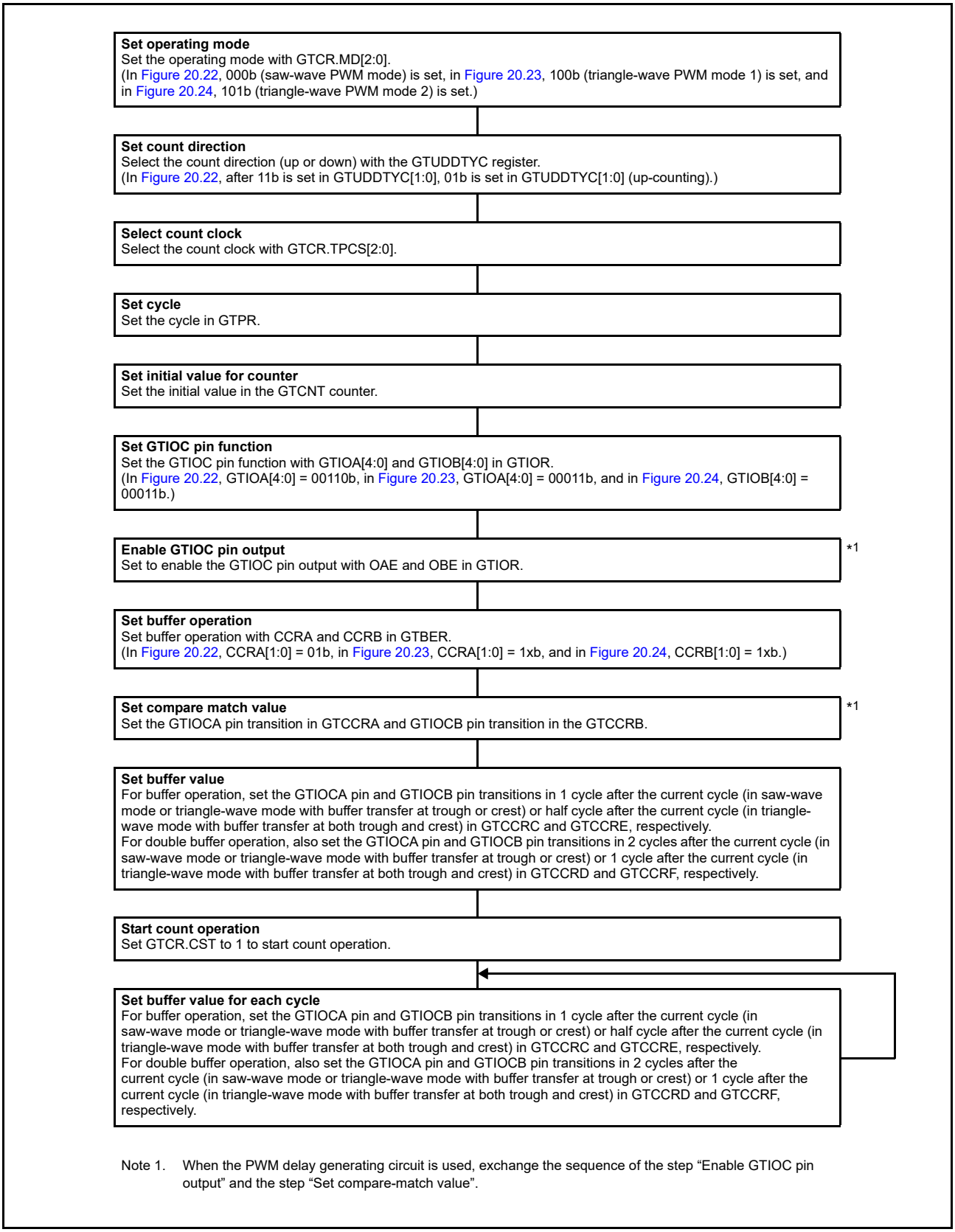


Figure 20.25 Example for setting GTCCRA and GTCCRB buffer operation for output compare

(2) When GTCCRA or GTCCRB functions as input capture register

When an input capture is generated, the GTCNT counter value is transferred to GTCCRA and GTCCRB and the stored GTCCRA and GTCCRB register values are transferred to the buffer registers. In input capture operation, the buffer transfer is not performed by the counter clear.

Figure 20.26 and Figure 20.27 show examples of GTCCRA and GTCCRB buffer operation and Figure 20.28 shows an example for setting GTCCRA and GTCCRB buffer operation.

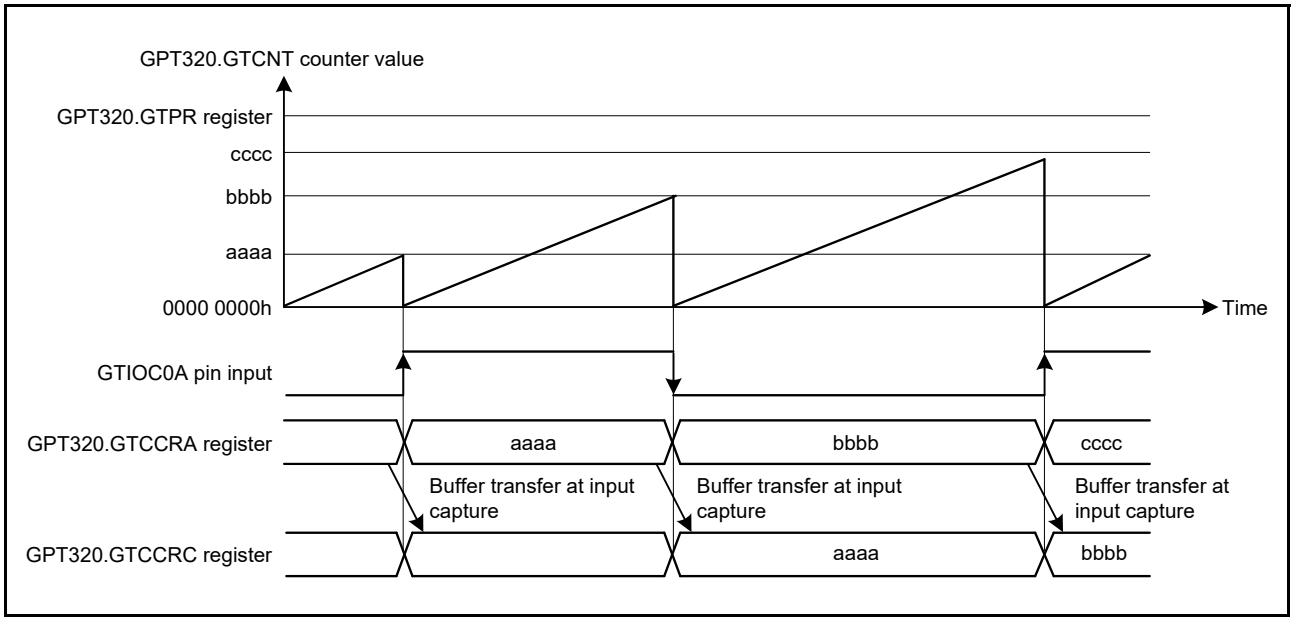


Figure 20.26 Example of GTCCRA and GTCCRB buffer operation with input capture at both edges of GTIOC0A input, saw waves in up-counting, and GTCNT counter cleared at both edges of GTIOC0A input

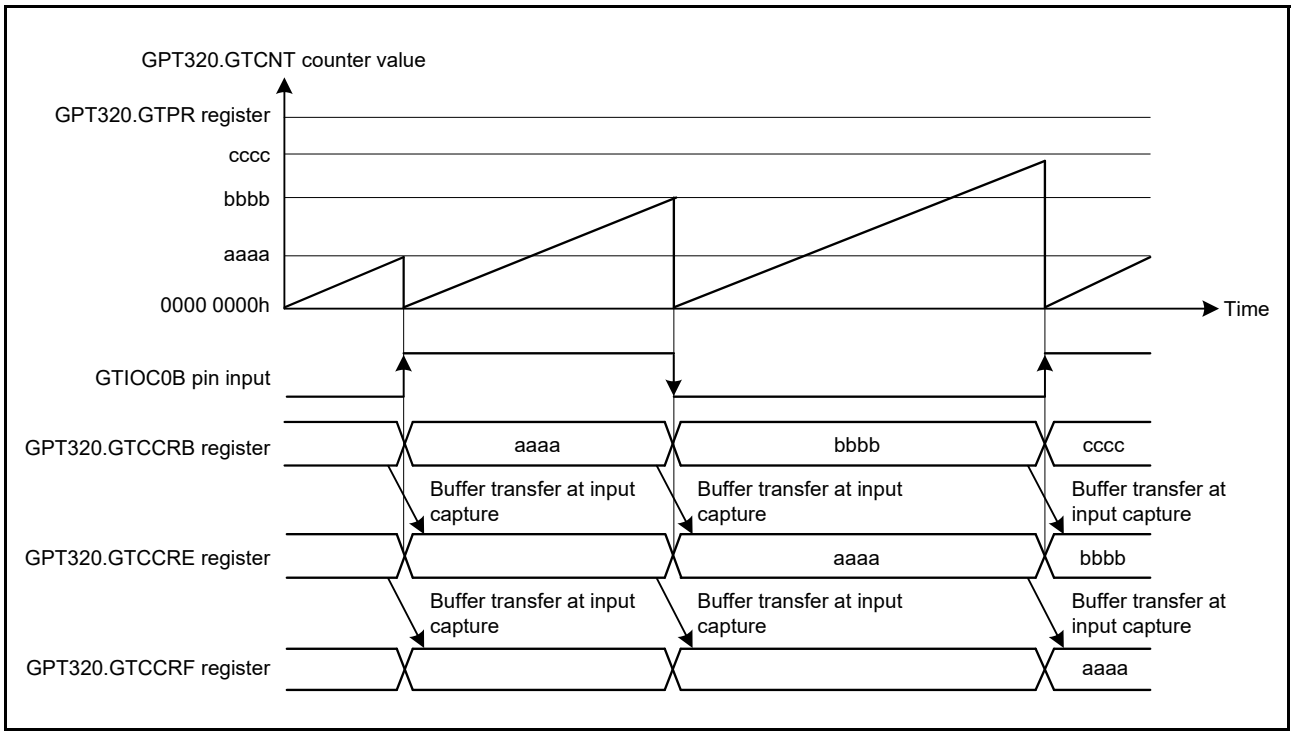


Figure 20.27 Example of GTCCRA and GTCCRB double buffer operation with input capture at both edges of GTIOC0B input, saw waves in up-counting, and GTCNT counter cleared at both edges of GTIOC0B input

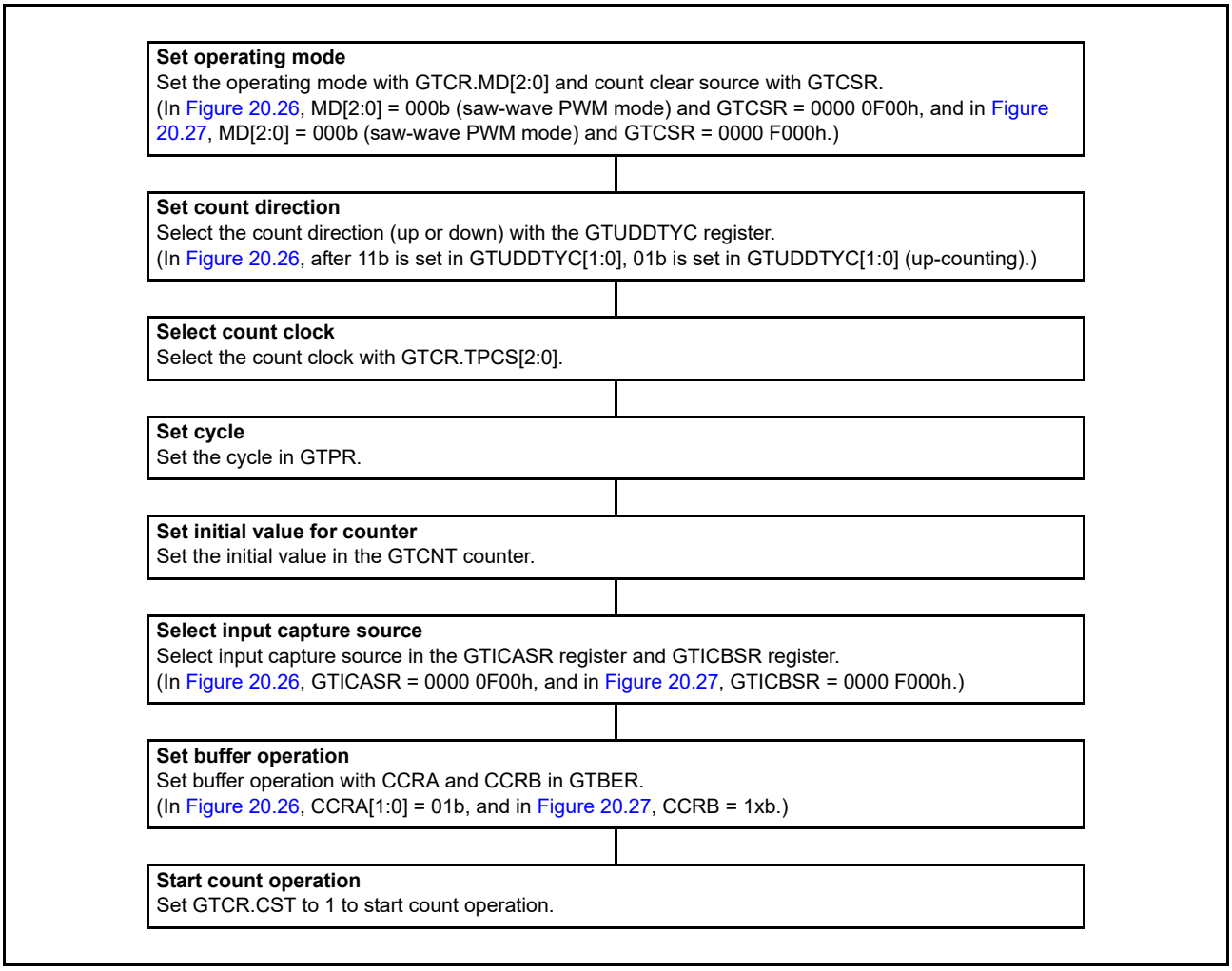


Figure 20.28 Example for setting GTCCRA and GTCCRB buffer operation for input capture

20.3.3 PWM Output Operating Mode

The GPT can output PWM waveforms to the GTIOCA pin or GTIOCB pin by a compare match between the GTCNT counter and GTCCRA or GTCCRB.

By setting GTDTCR and GTDVU, the compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

20.3.3.1 Saw-wave PWM mode

In saw-wave PWM mode, GTCNT performs saw-wave (half-wave) operation by setting the cycle in GTPR and a PWM waveform is output to the GTIOCA or GTIOCB pin when a GTCCRA or GTCCRB compare match occurs. The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the cycle end according to the GTIOR setting

Figure 20.29 shows an example of saw-wave PWM mode operation, and Figure 20.30 shows an example for setting saw-wave PWM mode.

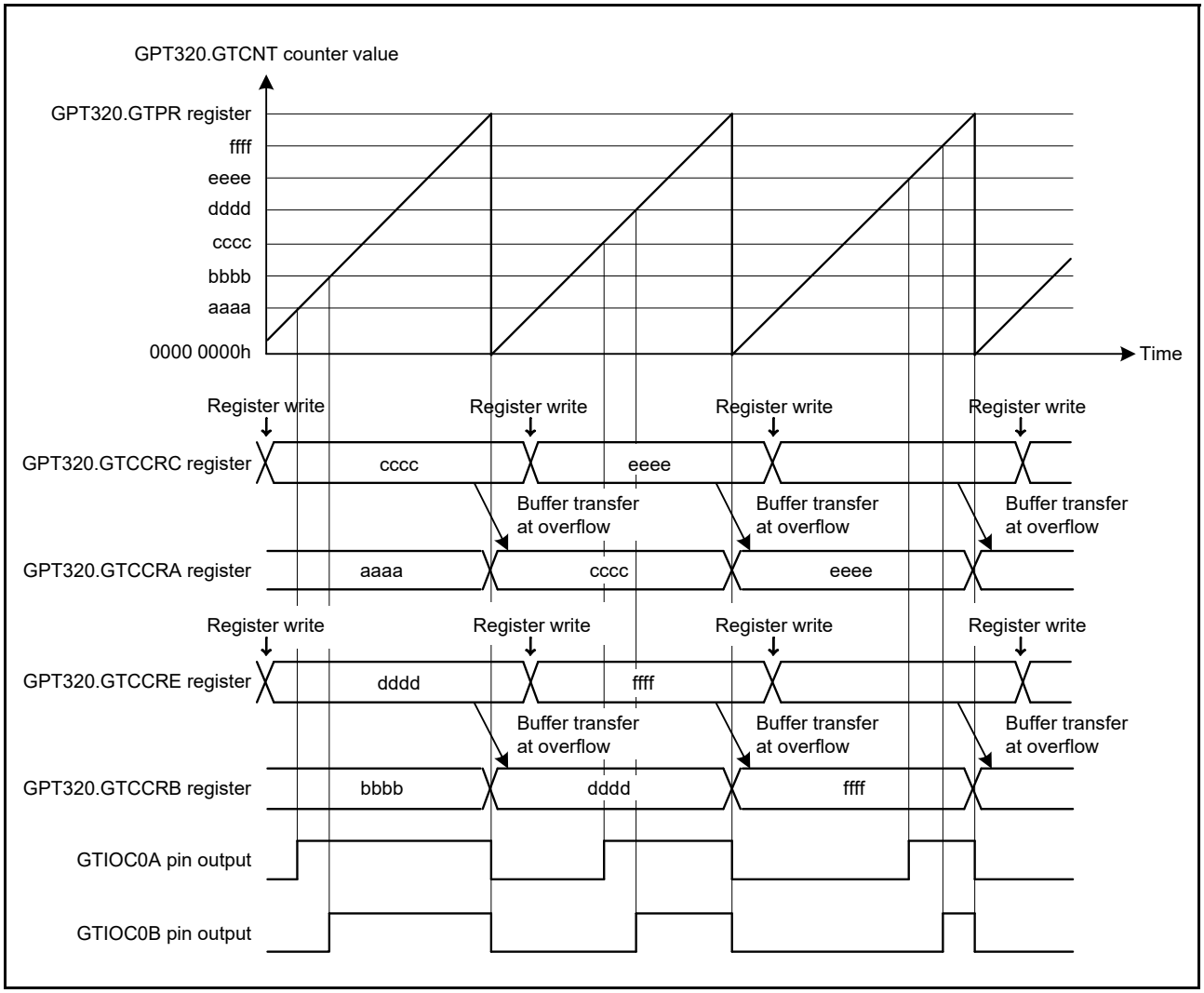
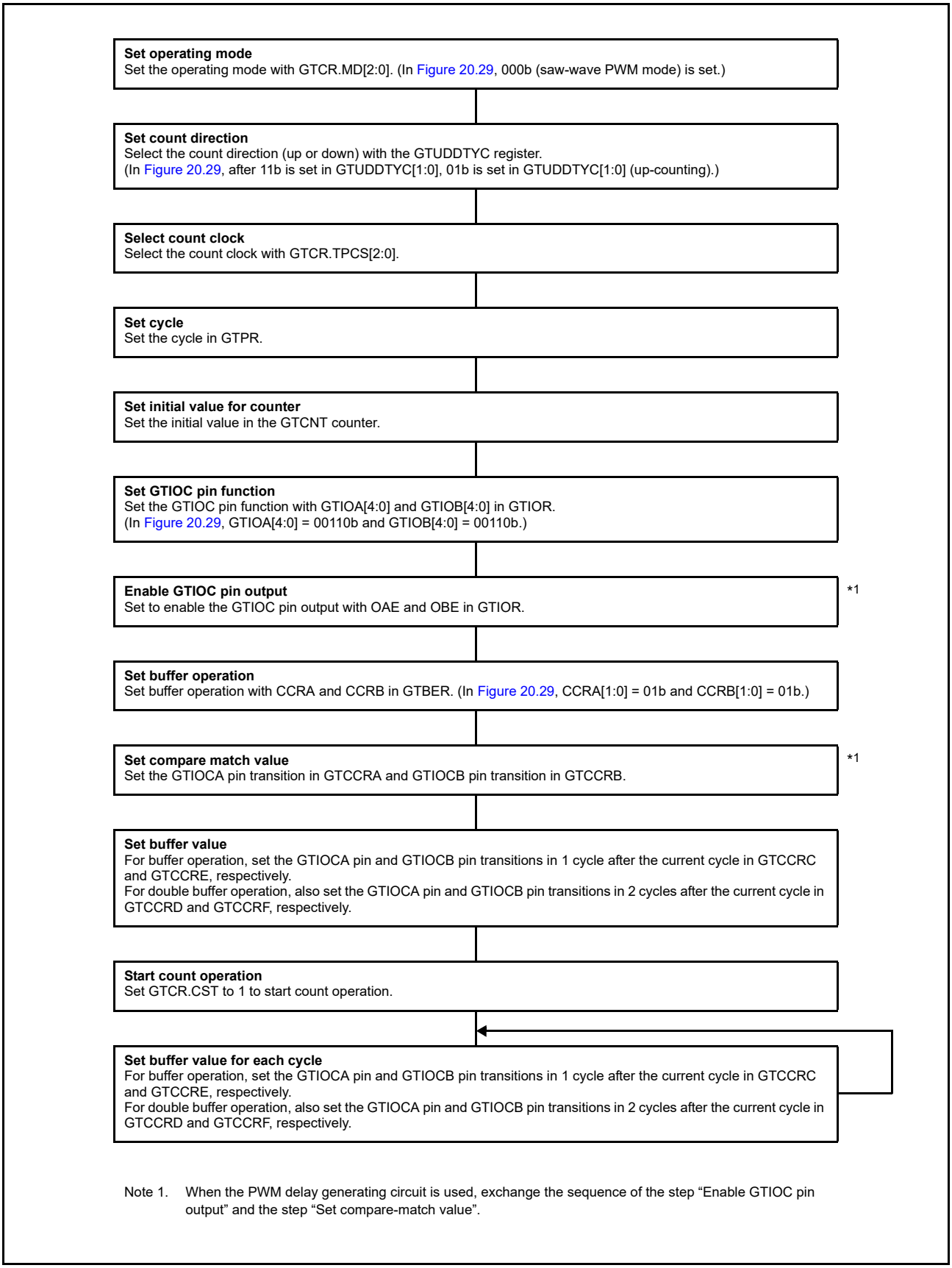


Figure 20.29 Example of saw-wave PWM mode operation with up-counting, buffer operation, high output at GTCCRA/GTCCRB compare match, and low output at cycle end



Note 1. When the PWM delay generating circuit is used, exchange the sequence of the step "Enable GTIOC pin output" and the step "Set compare-match value".

Figure 20.30 Example for setting saw-wave PWM mode

20.3.3.2 Saw-wave one-shot pulse mode

The saw-wave one-shot pulse mode is a mode in which the cycle is set in GTPR, the GTCNT counter performs saw-wave (half-wave) operation and a PWM waveform is output to the GTIOCA or GTIOCB pin at a compare match of GTCCRA or GTCCRB with buffer operation fixed.

Buffer operation in saw-wave one-shot pulse mode is different from the usual buffer operation. Buffer transfer is performed from the following:

- GTCCRC to GTCCRA at the cycle end
- GTCCRE to GTCCRB at the cycle end
- GTCCRD to temporary register A at the cycle end
- GTCCRF to temporary register B at the cycle end
- Temporary register A to GTCCRA at a GTCCRA compare match
- Temporary register B to GTCCRB at a GTCCRB compare match.

The pin output value can be selected from low output, high output, or toggle output separately for a compare match and the cycle end according to the GTIOR setting. When the GTBER.CCRSWT bit is set to 1 while the count operation stops, the buffer is transferred forcibly from the GTCCRD register to temporary register A and from the GTCCRF register to temporary register B. By setting GTDTCR and GTDVU, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 20.31 shows an example of saw-wave one-shot pulse mode operation, and Figure 20.32 shows an example for setting saw-wave one-shot pulse mode.

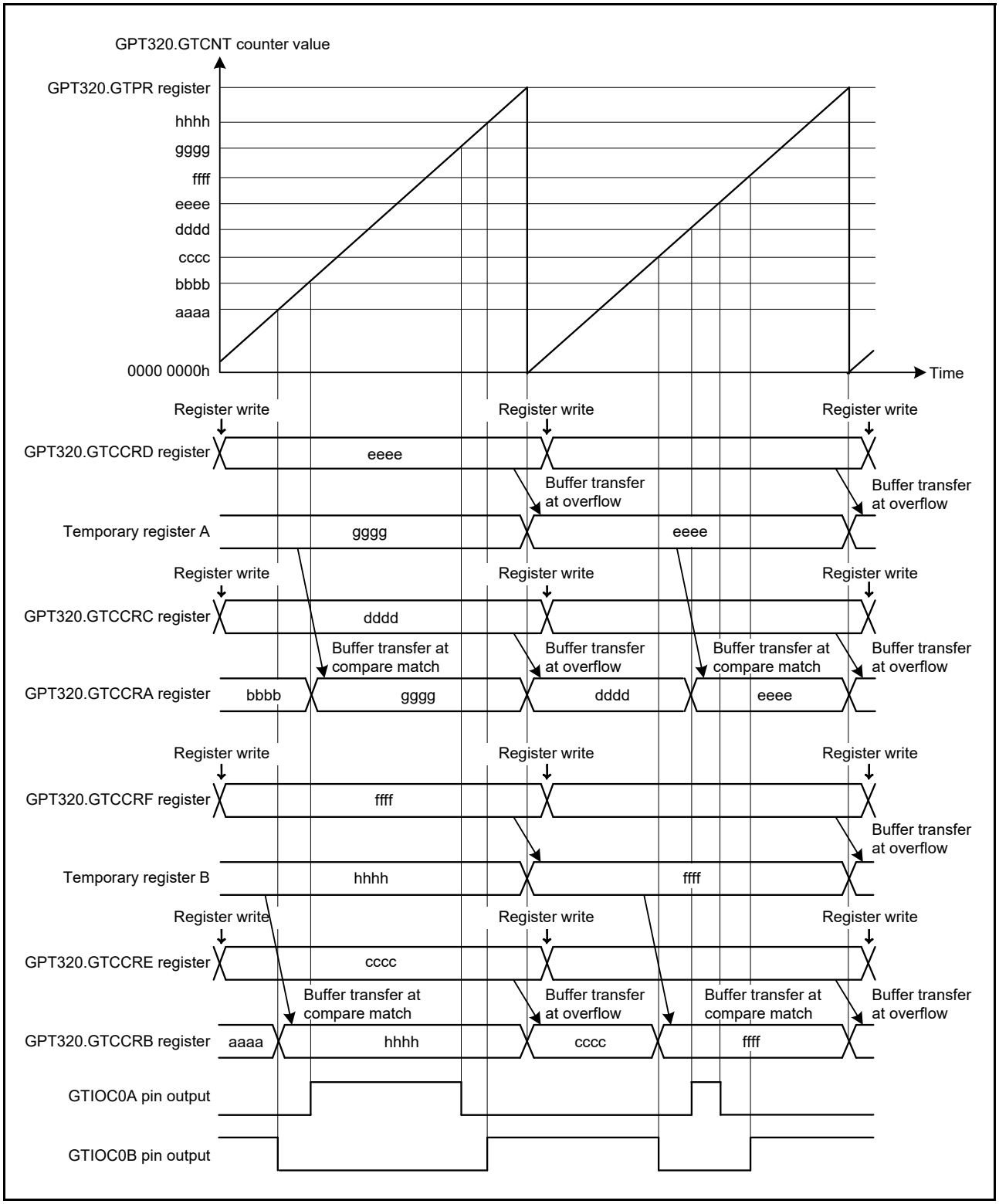
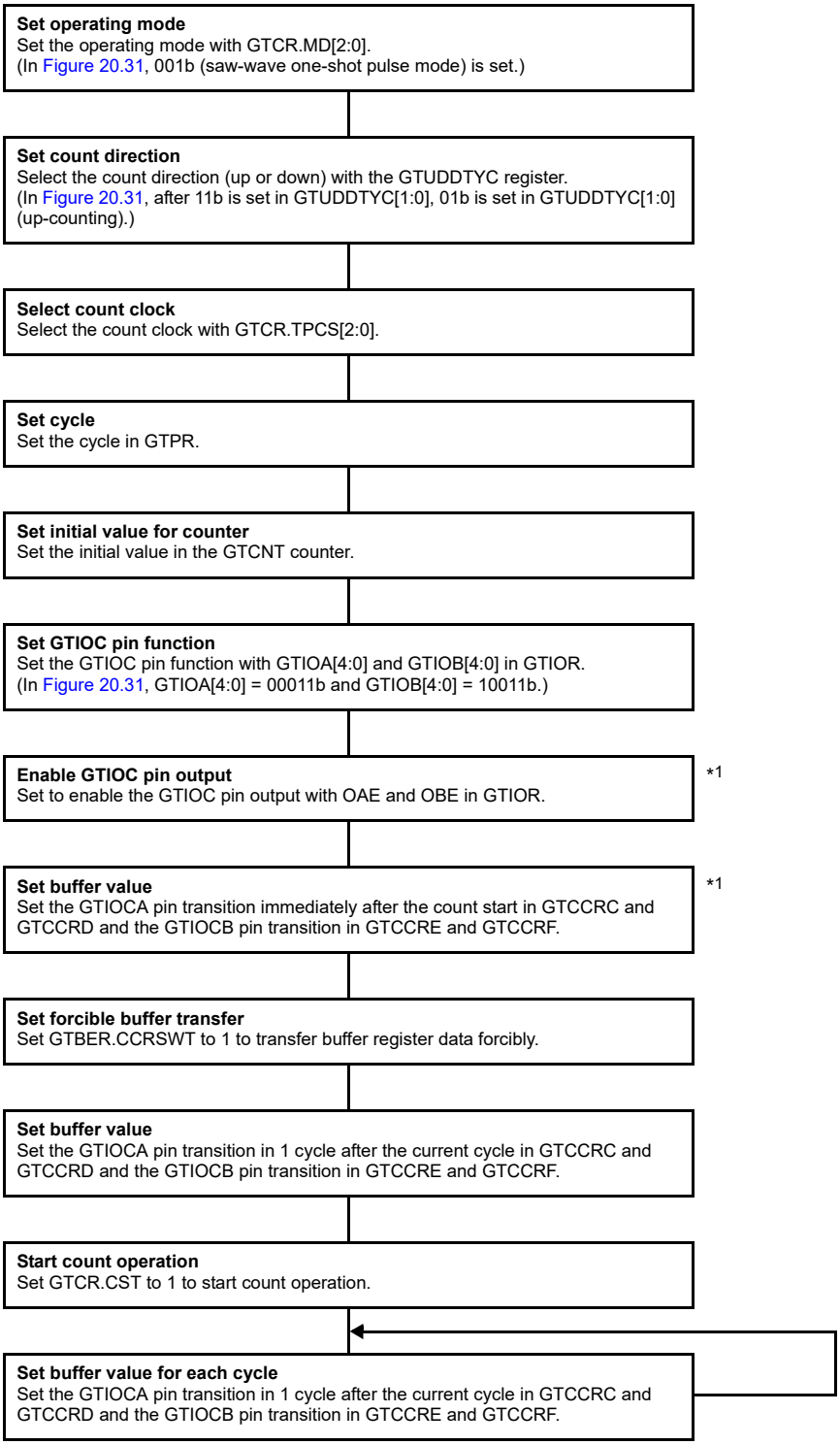


Figure 20.31 **Example of saw-wave one-shot pulse mode operation with up-counting, low output from the GTIOC0A pin and high output from the GTIOC0B pin at count start, output toggled at GTCCRA/ GTCCRB compare match, and output retained at cycle end**



Note 1. When the PWM delay generating circuit is used, exchange the sequence of the step "Enable GTIOC pin output" and the step "Set buffer value".

Figure 20.32 Example for setting saw-wave one-shot pulse mode

20.3.3.3 Triangle-wave PWM mode 1 (32-bit transfer at trough)

The triangle-wave PWM mode 1 is a mode in which the cycle is set in GTPR. The GTCNT counter performs triangle-wave (full-wave) operation, and a PWM waveform is output to the GTIOCA or GTIOCB pin when a GTCCRA or GTCCRB compare match occurs. Buffer transfer is performed at the trough. The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the cycle end according to the GTIOR setting.

By setting GTDTCR and GTDVU, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 20.33 shows an example of a triangle-wave PWM mode 1 operation, and Figure 20.34 shows an example for setting a triangle-wave PWM mode 1.

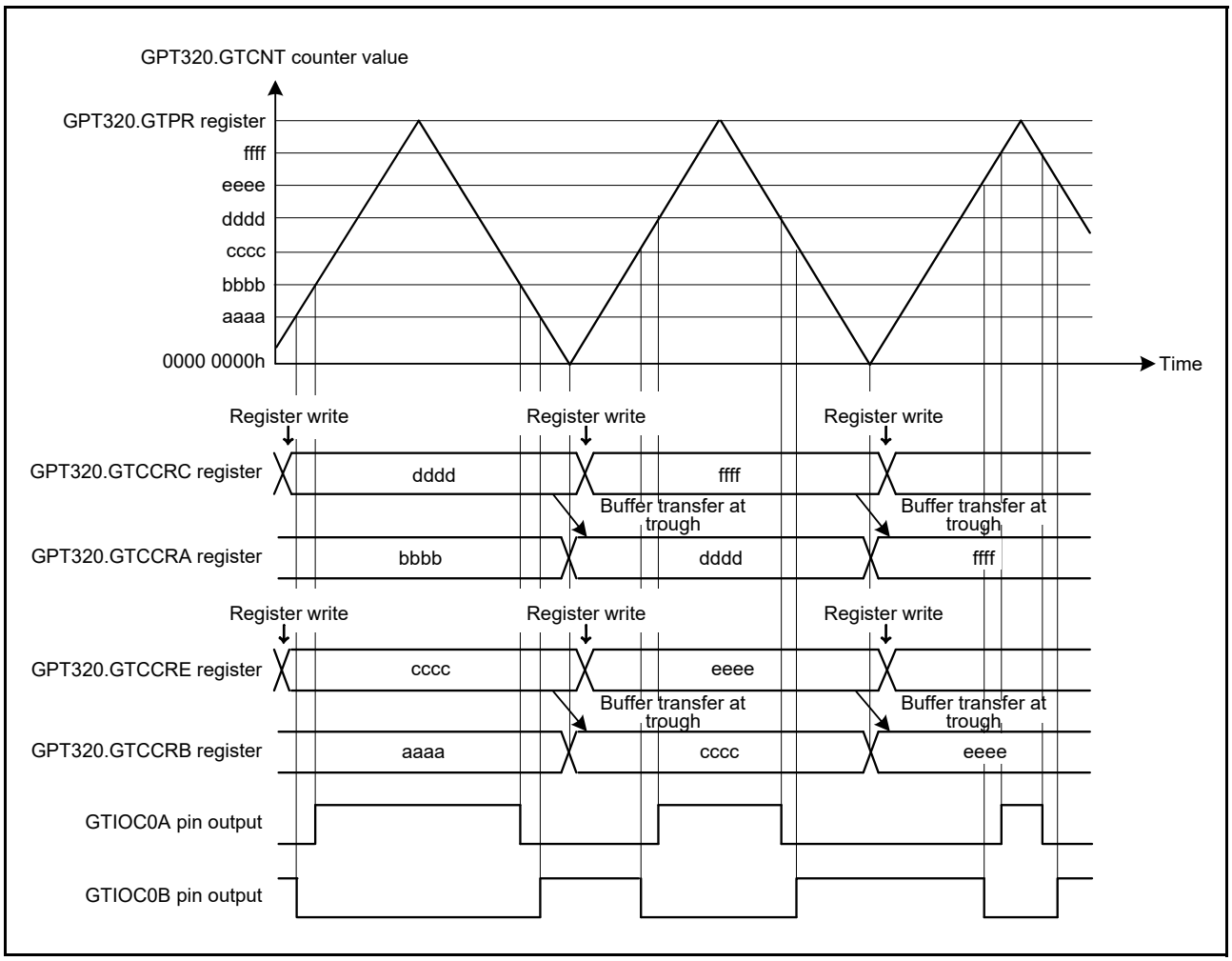
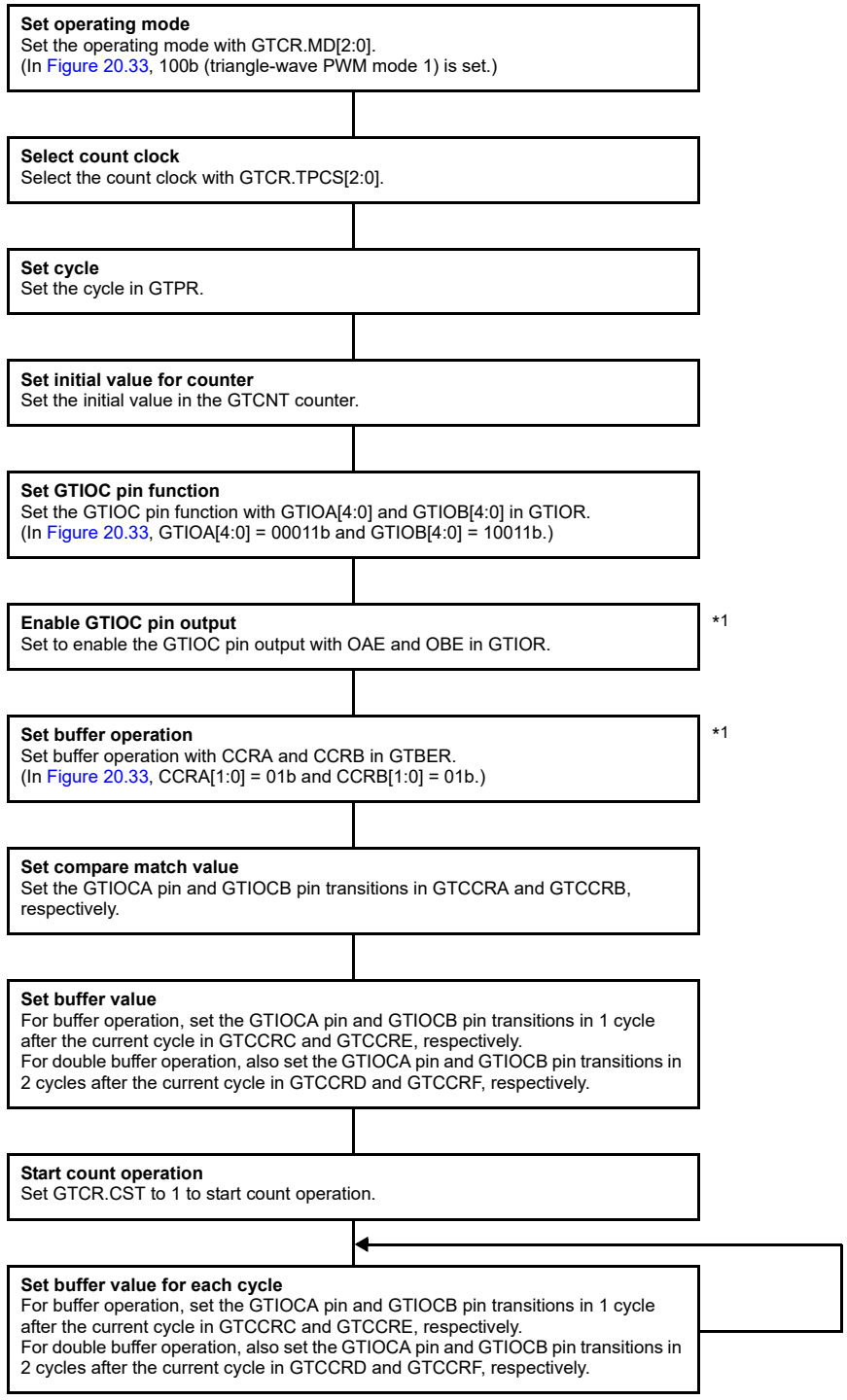


Figure 20.33 Example of triangle-wave PWM mode 1 operation with buffer operation, low output from the GTIOC0A pin and high output from the GTIOC0B pin at count start, output toggled at GTCCRA/ GTCCRB register compare match, and output retained at cycle end



Note 1. When the PWM delay generating circuit is used, exchange the sequence of the step "Enable GTIOC pin output" and the step "Set buffer value".

Figure 20.34 Example for setting triangle-wave PWM mode 1

20.3.3.4 Triangle-wave PWM mode 2 (32-bit transfer at crest and trough)

Similarly to triangle-wave PWM mode 1, in triangle-wave PWM mode 2 the cycle is set in GTPR. The GTCNT counter performs triangle-wave (full-wave) operation, and a PWM waveform is output to the GTIOCA or GTIOCB pin when a GTCCRA or GTCCRB compare match occurs. The buffer transfer is performed at both crests and troughs. The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the cycle end according to the GTIOR setting.

By setting GTDTCR and GTDVU, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 20.35 shows an example of triangle-wave PWM mode 2 operation, and Figure 20.36 shows an example for setting triangle-wave PWM mode 2.

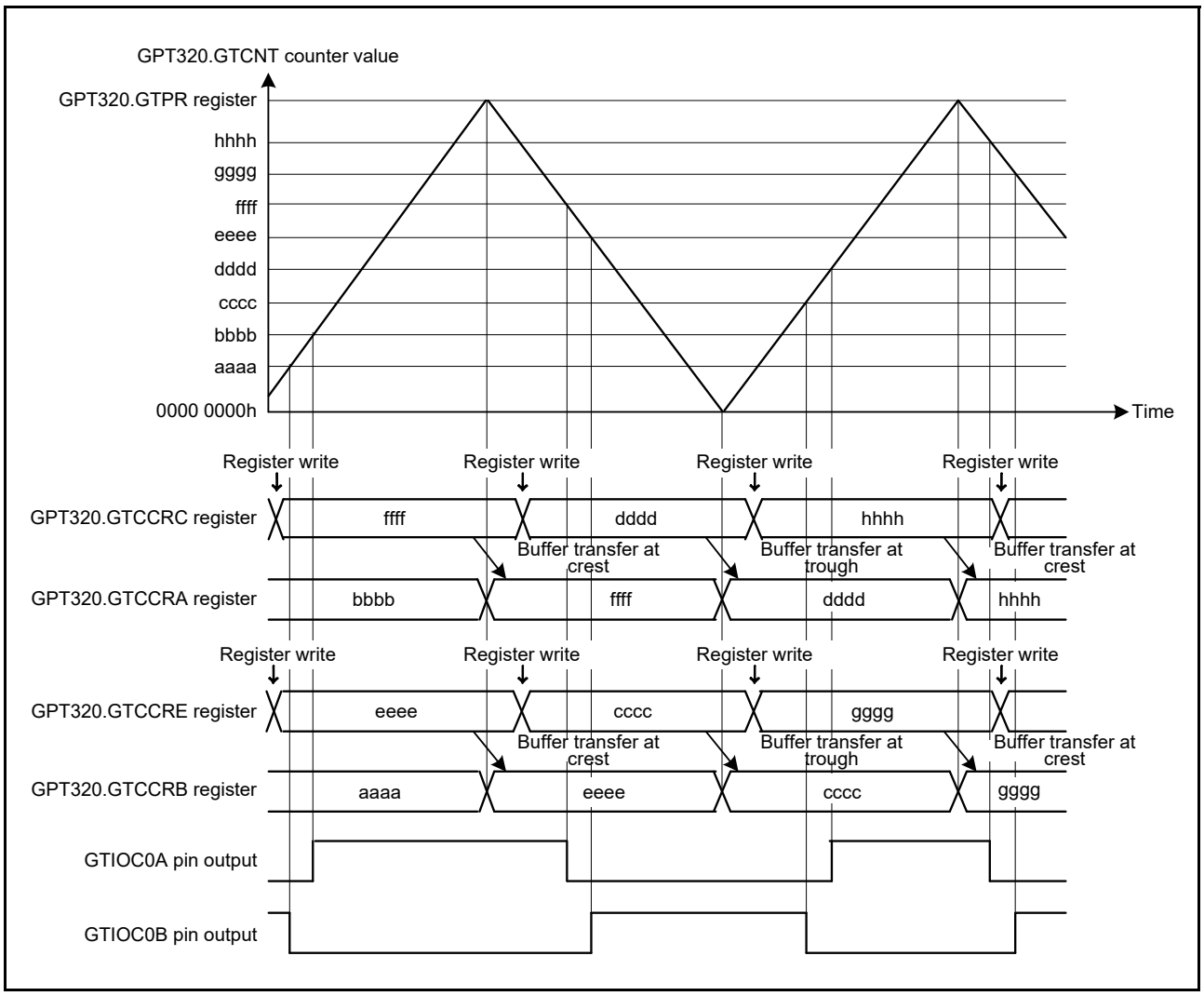
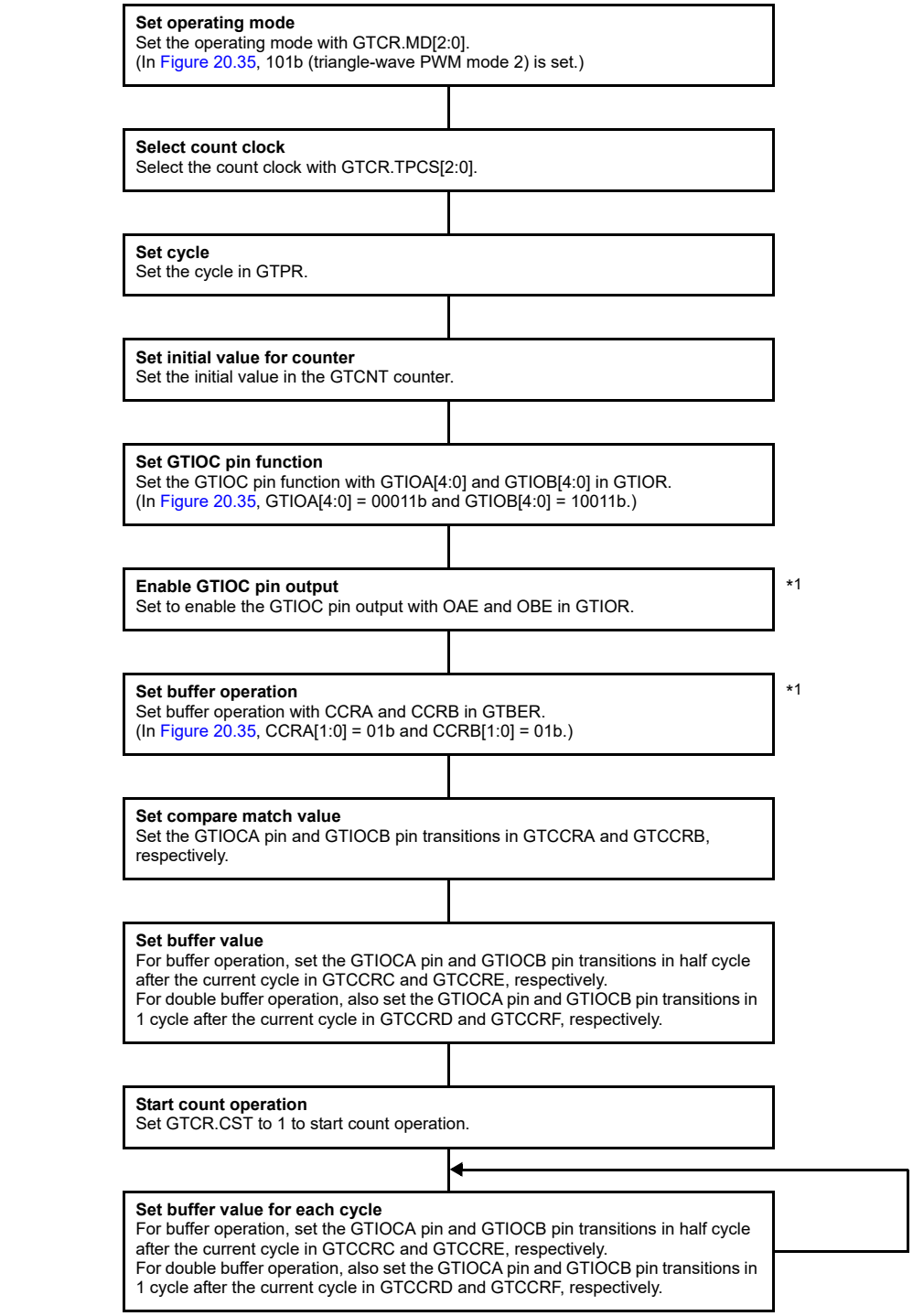


Figure 20.35 Example of triangle-wave PWM mode 2 operation with buffer operation, low output from the GTIOC0A pin and high output from the GTIOC0B pin at count start, output toggled at GTCCRA/ GTCCRB compare match, and output retained at cycle end



Note 1. When the PWM delay generating circuit is used, exchange the sequence of the step "Enable GTIOC pin output" and the step "Set buffer value".

Figure 20.36 Example for setting triangle-wave PWM mode 2

20.3.3.5 Triangle-wave PWM mode 3 (64-bit transfer at trough)

The triangle-wave PWM mode 3 is a mode in which the cycle is set in GTPR. The GTCNT counter performs triangle-wave (full-wave) operation and a PWM waveform is output to the GTIOCA or GTIOCB pin at a compare match of GTCCRA or GTCCRB with buffer operation fixed. Buffer operation in triangle-wave PWM mode 3 is different from the usual buffer operation. Buffer transfer is performed from the following:

- GTCCRC to GTCCRA at the trough
- GTCCRE to GTCCRB at the trough
- GTCCRD to temporary register A at the trough
- GTCCRF to temporary register B at the trough
- Temporary register A to GTCCRA at the crest
- Temporary register B to GTCCRB at the crest.

The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the cycle end according to the GTIOR setting.

By setting GTDTCR and GTDVU, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 20.37 shows an example of triangle-wave PWM mode 3 operation, and Figure 20.38 shows an example for setting triangle-wave PWM mode 3.

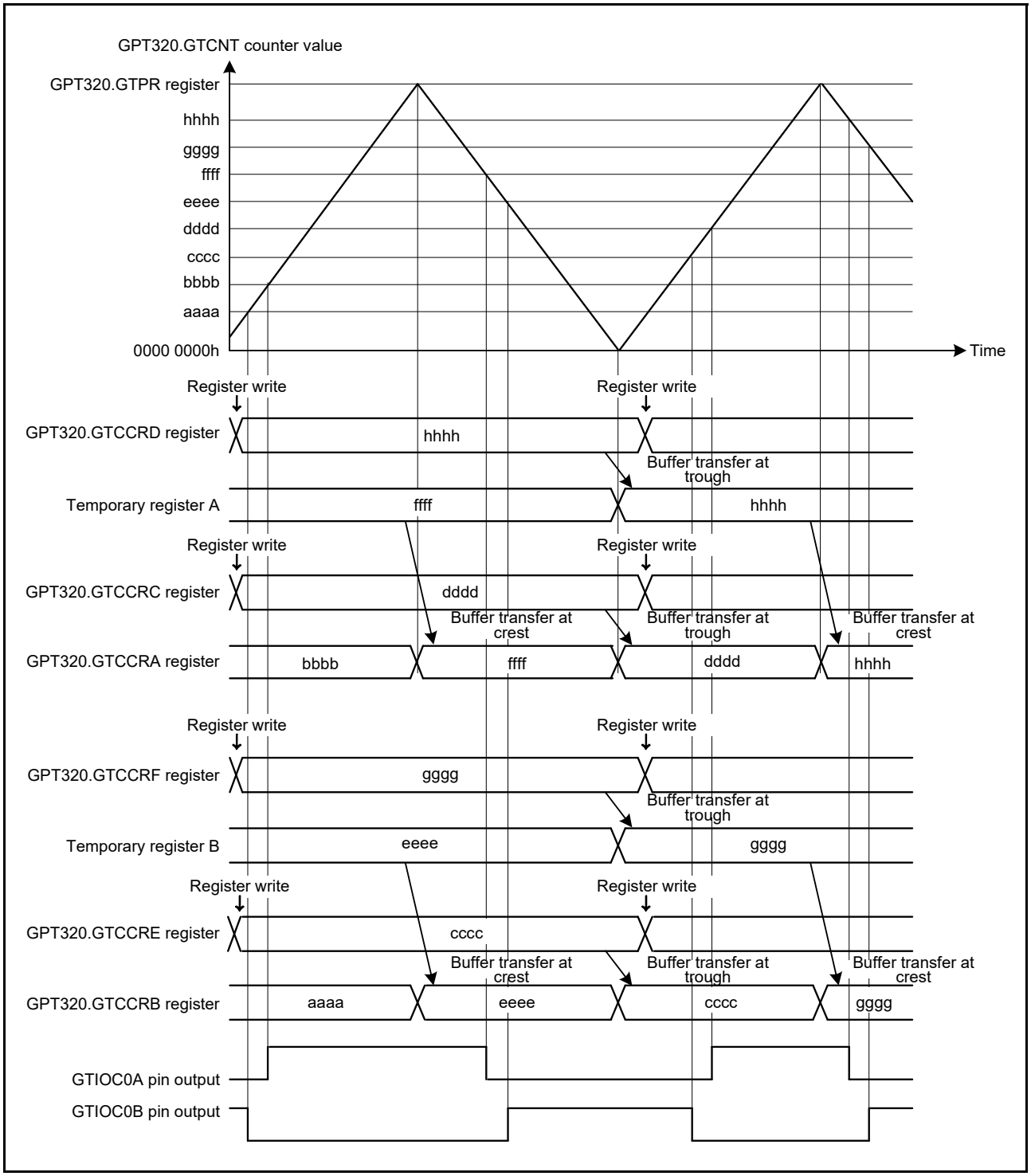


Figure 20.37 **Example of triangle-wave PWM mode 3 operation with low output from the GTIOC0A pin and high output from the GTIOC0B pin at count start, output toggled at GTCCRA/GTCCRB compare match, and output retained at cycle end**

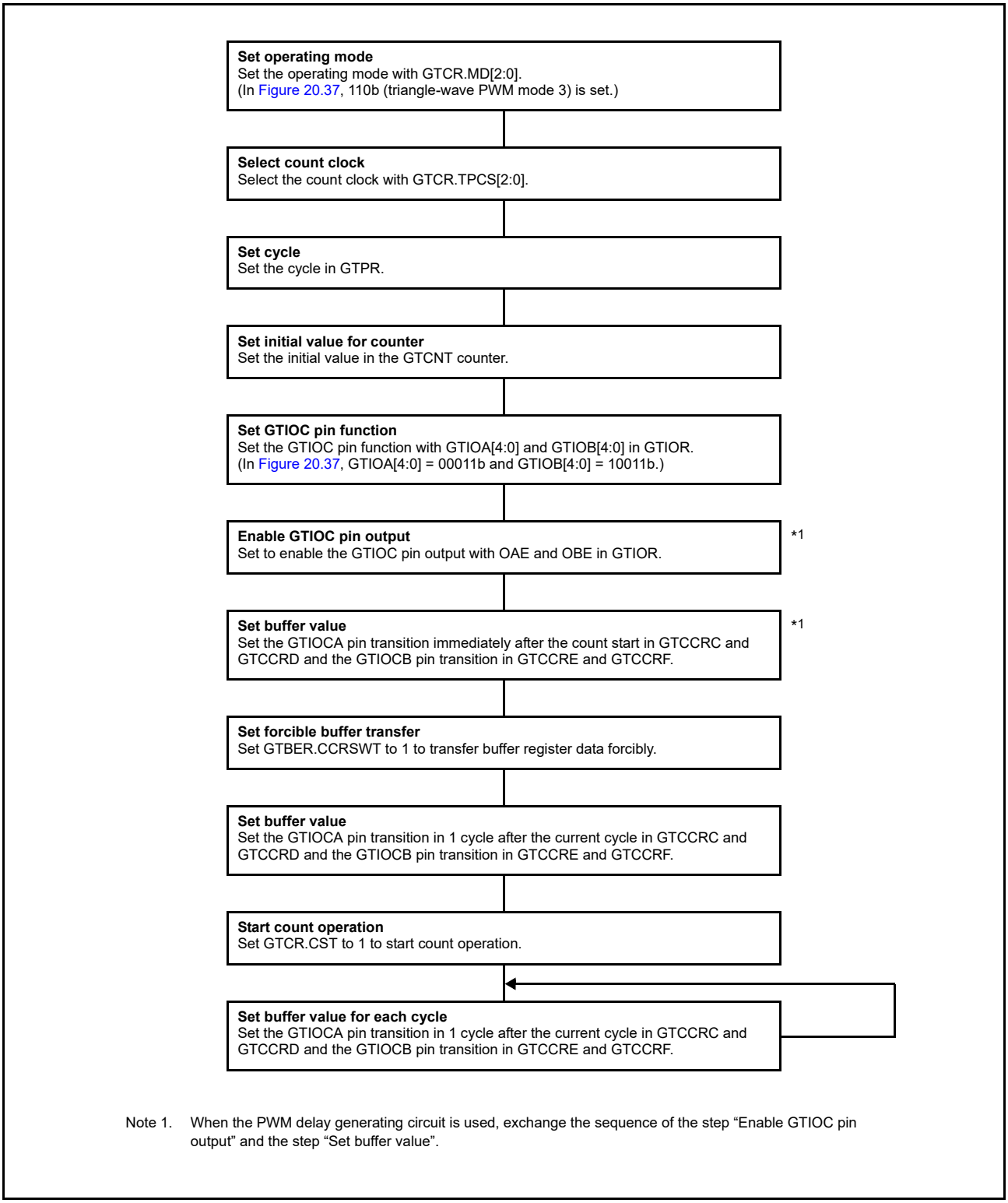


Figure 20.38 Example for setting triangle-wave PWM mode 3

20.3.4 Automatic Dead Time Setting Function

By setting GTDTCR, a compare match value for a negative waveform with dead time obtained by a compare match value for a positive waveform (GTCCRA value) and specified dead time value (GTDVU value) can automatically be set to GTCCRB.

The automatic dead time setting function can be used in saw-wave one-shot pulse mode and all the triangle PWM modes.

Writing to GTCCRB is prohibited when the automatic dead time setting function is used. Dead time setting beyond the cycle is also prohibited. Values for automatic dead time setting can be read from GTCCRB. The automatic dead time value setting to GTCCRB is performed at the next count clock cycle when registers that are used for calculating the automatic dead time value are updated.

Figure 20.39 to Figure 20.42 show examples of automatic dead time setting function operation. Figure 20.43 and Figure 20.44 show the setting examples.

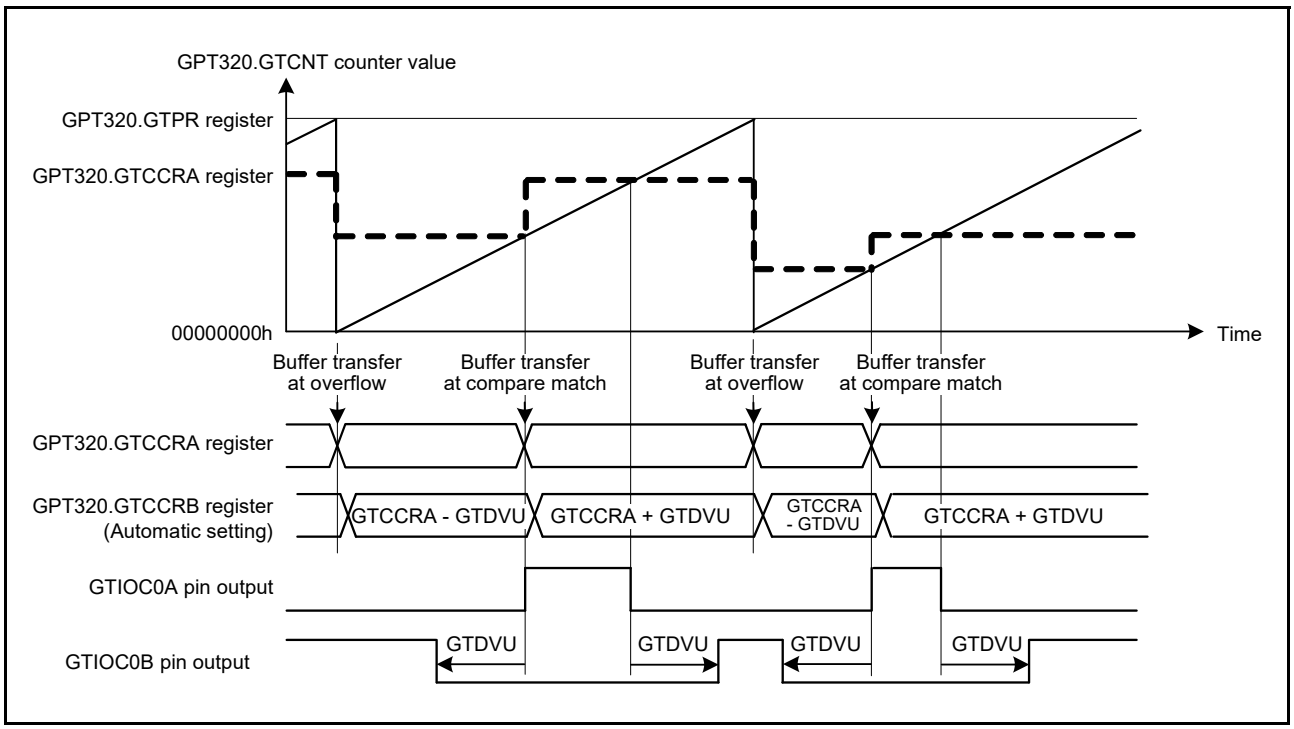


Figure 20.39 Example of automatic dead time setting function operation in saw-wave one-shot pulse mode, up-counting, and active-high

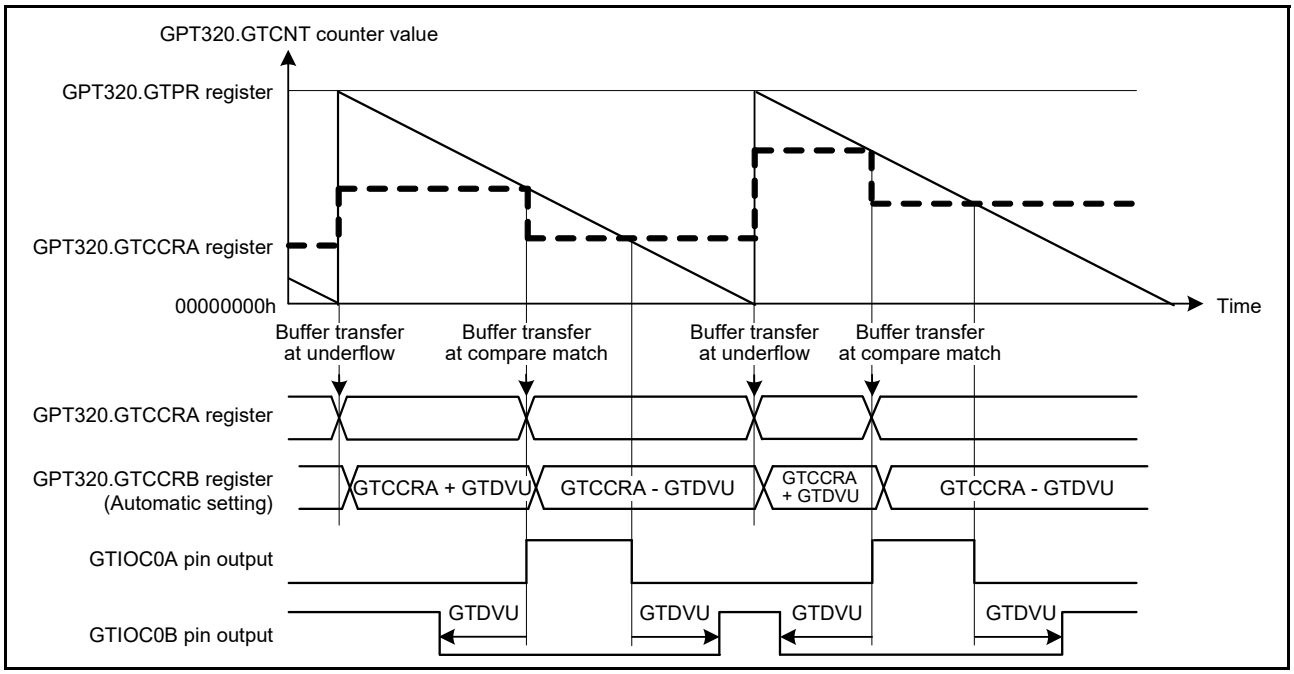


Figure 20.40 Example of automatic dead time setting function operation in saw-wave one-shot pulse mode, down-counting, and active-high

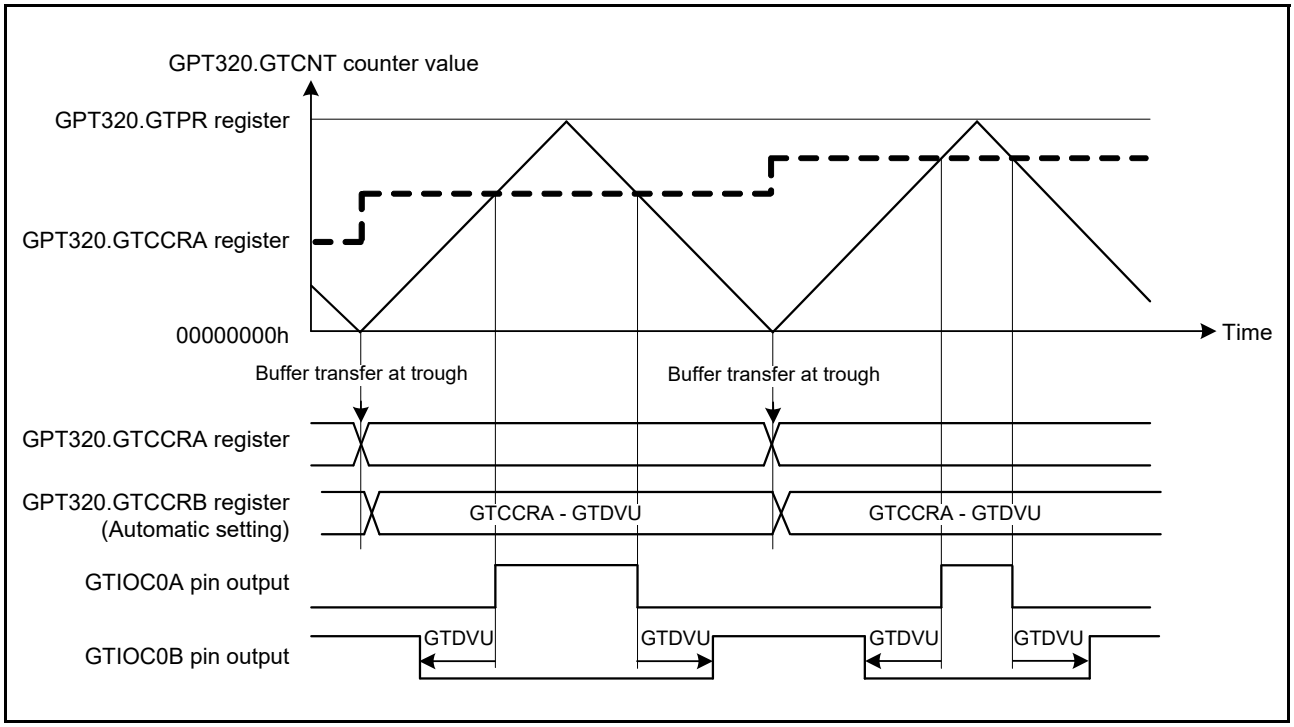


Figure 20.41 Example of automatic compare-match value setting function with dead time in triangle-wave PWM mode 1, and active-high

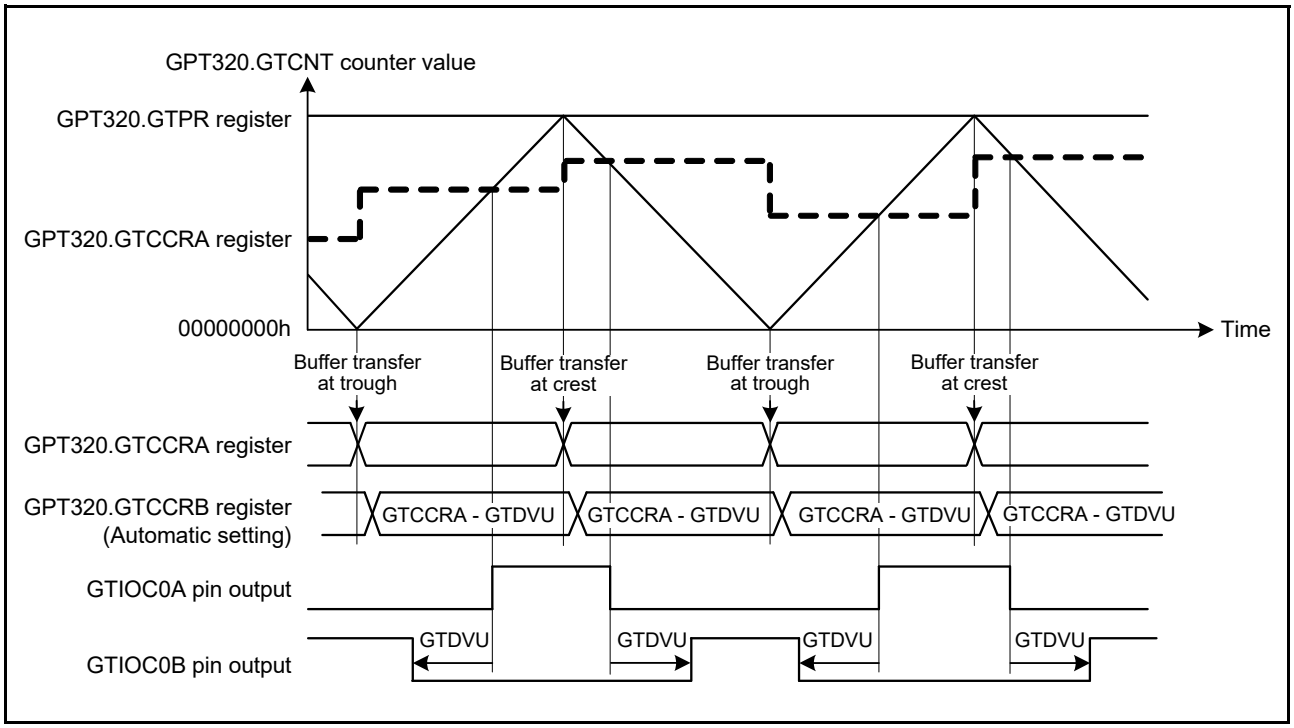


Figure 20.42 Example of automatic compare-match value setting function with dead time in triangle-wave PWM mode 2 or 3, and active-high

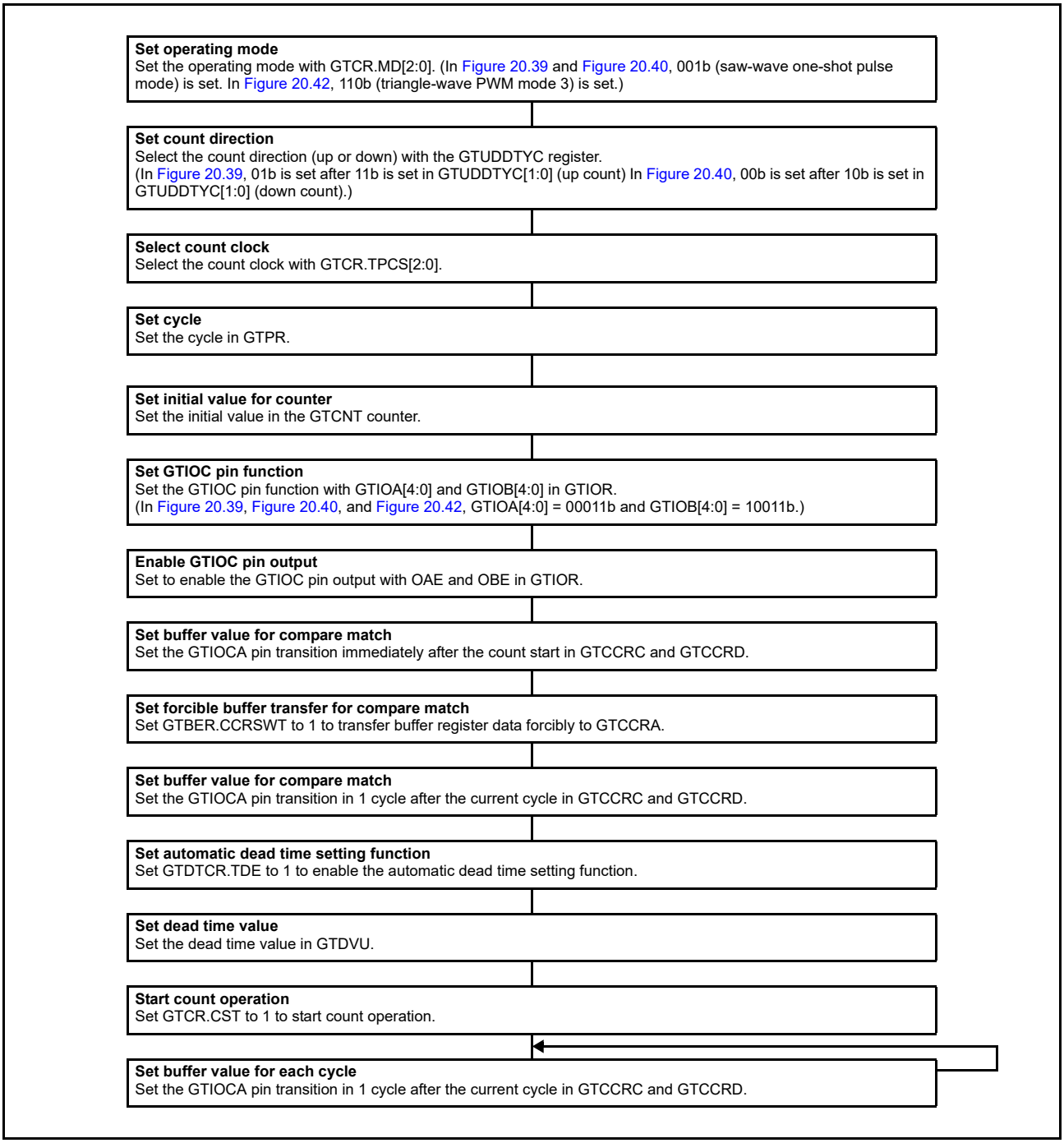


Figure 20.43 Example for setting automatic dead time setting function in saw-wave one-shot pulse mode, and triangle-wave PWM mode 3

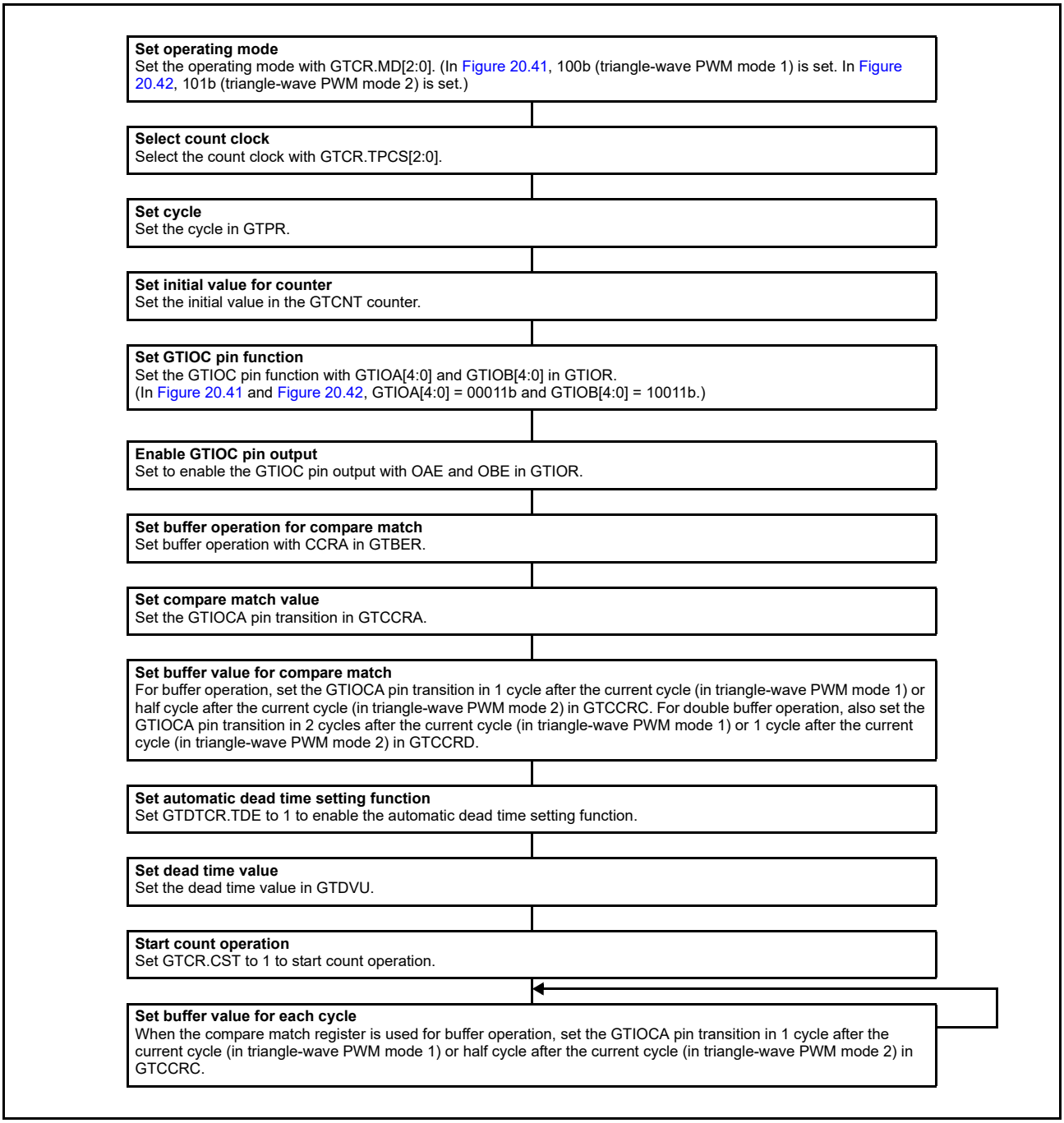


Figure 20.44 Example for setting automatic dead time setting function in triangle-wave PWM mode 1 or 2

20.3.5 Count Direction Changing Function

The count direction of the GTCNT counter can be changed by modifying the UD bit in GTUDDTYC.

In saw-wave mode, if the UD bit in GTUDDTYC is modified during count operation, the count direction is changed at an overflow (when modified during up-counting) or an underflow (when modified during down-counting). If the GTUDDTYC.UD bit is modified while the count operation stops and the GTUDDTYC.UDF bit is 0, the GTUDDTYC.UD bit modification is not reflected at the start of counting and the count direction is changed at an overflow or an underflow. If the UDF bit is set to 1 while the count operation stops, the GTUDDTYC.UD bit value at that time is reflected at the start of counting.

In triangle-wave mode, the count direction does not change even though the UD bit in GTUDDTYC is modified during the count operation. Similarly, even though the GTUDDTYC.UD bit is modified while the count operation stops and

GTUDDTYC.UDF bit is 0, the GTUDDTYC.UD bit value is not reflected to the count operation. If the GTUDDTYC.UDF bit is set to 1 while the count operation stops, the GTUDDTYC.UD bit value at that time is reflected at the start of counting.

If the count direction changes during a saw-wave count operation, the GTPR value after the start of up-counting is reflected in the count cycle during up-counting and the GTPR value before the start of down-counting is reflected during down-counting.

Figure 20.45 shows an example of count direction changing function operation.

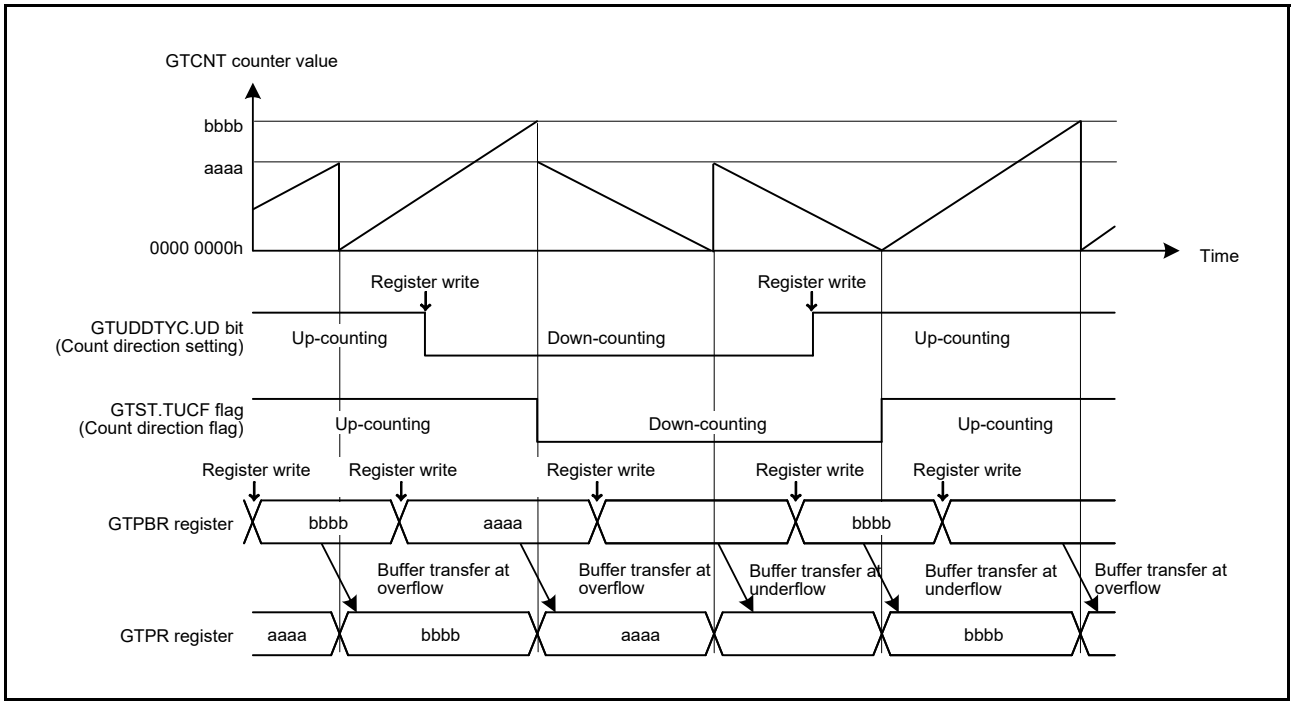


Figure 20.45 Example of a count direction changing function operation during buffer operation

20.3.6 Function of Output Duty 0% and 100%

The output duty of the GTIOCA pin and the GTIOCB pin are set to 0% or 100% by changing the GTUDDTYC.OADTY bit or GTUDDTYC.OBDTY bit.

In saw-wave mode, if the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified during the count operation, the output duty setting is reflected at an overflow (when modified during up-counting) or an underflow (when modified during down-counting). If the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified while the count operation stops and the GTUDDTYC.OADTYF or the GTUDDTYC.OBDTYF bit is 0, the output duty modification is not reflected at the start of counting. The output duty changes at an overflow or an underflow. If the GTUDDTYC.OADTYF or the GTUDDTYC.OBDTYF bit is set to 1 while the count operation stops, the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit value at that time is reflected at the start of counting.

In triangle-wave mode, if the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified during the count operation, the output duty setting is reflected at an underflow.

If the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified while the count operation stops and the GTUDDTYC.OADTYF or the GTUDDTYC.OBDTYF bit is 0, the output duty modification is not reflected at the start of counting. The output duty changes at an underflow. If the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified while the count operation stops and the GTUDDTYC.OADTYF or the GTUDDTYC.OBDTYF bit is 1, the output duty modification is reflected at the start of counting.

In performing 0%/100% duty operation, GPT internally continues to:

- Perform compare match operation
- Set compare match flag

- Output interrupt
- Perform buffer operation.

When the control is changed from 0% or 100% duty setting to compare match, the output value of GTIOCA pin at cycle end is decided by GTIOR.GTIOA[3:2] and GTUDDTYC.OADTYR. The output value of GTIOCB pin at cycle end is decided by GTIOR.GTIOB[3:2] and GTUDDTYC.OBDTYR.

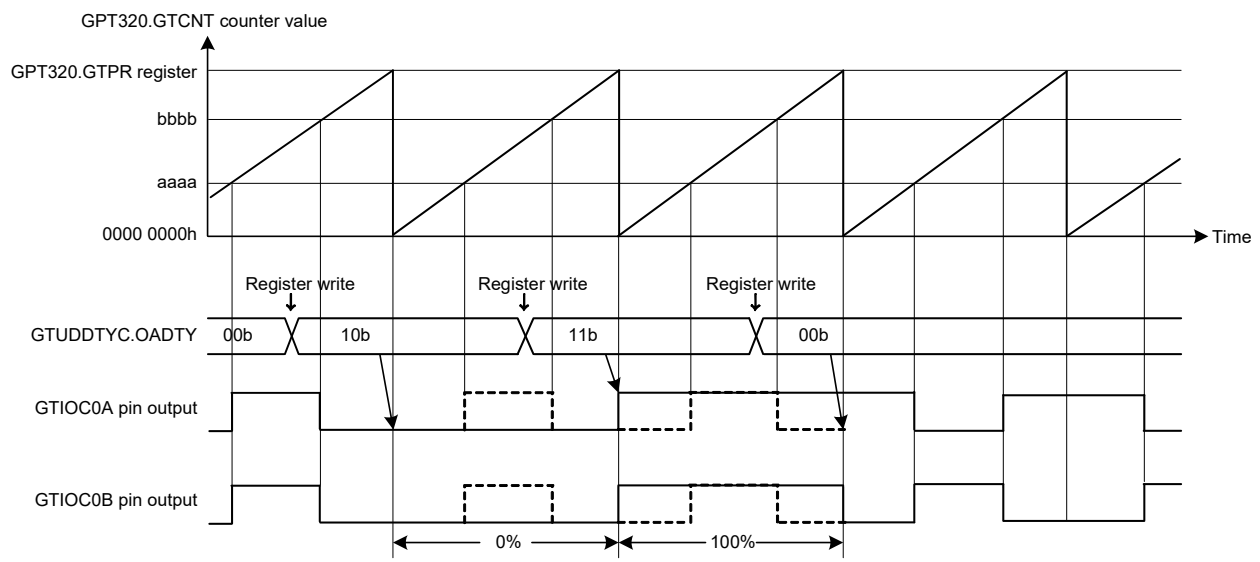
When GTIOR.GTIOA[3:2] and GTIOR.GTIOB[3:2] are set to 01b, the output pins output low at cycle end. When GTIOR.GTIOA[3:2] and GTIOR.GTIOB[3:2] are set to 10b, the output pins output high at cycle end.

GTUDDTYC.OADTYR selects the value that is the object of output retained/toggled at cycle end, when GTIOR.GTIOm[3:2] are set to 00b (output retained at cycle end) or when GTIOR.GTIOm[3:2] are set to 11b (output toggled at cycle end). Table 20.6 shows the values of GTIOCA/GTIOCB pin output at cycle end.

Table 20.6 Output values after releasing 0%/100% duty setting (m = A, B)

GTIOR.GTIOm[3:2]	Compare match value at cycle end masked by 0%/100% duty setting	GTUDDTYC.OmDTYR in duty 0% setting		GTUDDTYC.OmDTYR in duty 100% setting	
		0	1	0	1
00 (Output retained at cycle end)	0	0	0	1	0
	1	0	1	1	1
01 (Low output at cycle end)	—	0	0	0	0
10 (High output at cycle end)	—	1	1	1	1
11 (Output toggled at cycle end)	0	1	1	0	1
	1	1	0	0	0

Figure 20.46 shows an example of output duty 0% and 100% function.



[Setting examples]

GPT320.GTIOR.GTIOA[4:0] bits: 00011b
initial output of low, output toggled at compare match, output retained at cycle end

GPT320.GTUDDTYC.OADTYR bit: 0b
Applied the value of duty 0%/100% output to GTIOA[3:2] bits function after 0%/100% duty setting is released.

GPT320.GTIOR.GTIOB[4:0] bits: 00011b
initial output of low, output toggled at compare match, output retained at cycle end

GPT320.GTUDDTYC.OBDTYR bit: 1
Applied the value of masked compare match output to GTIOB[3:2] bits function after 0%/100% duty setting is released

Figure 20.46 Example of output duty 0% and 100% function

20.3.7 Hardware Count Start/Count Stop and Clear Operation

The GTCNT counter can be started, stopped, or cleared by the following hardware sources:

- External trigger input
- ELC event input
- GTIOCA/GTIOCB pin input.

20.3.7.1 Hardware start operation

The GTCNT counter can be started by selecting a hardware source using GTSSR.

Figure 20.47 shows an example of a count start operation by a hardware source. Figure 20.48 shows the setting example.

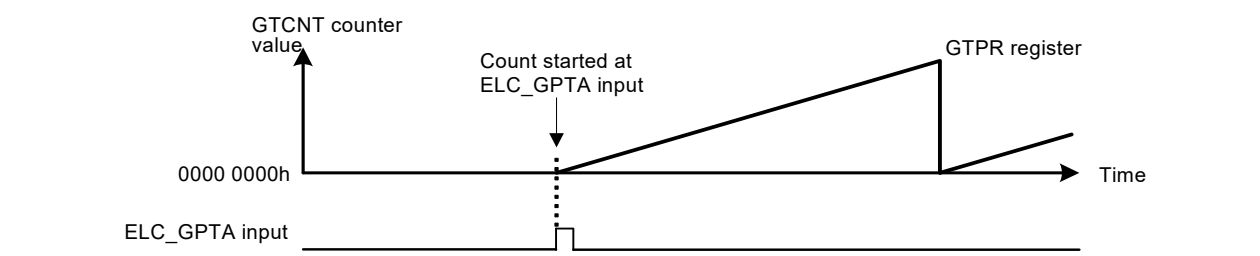


Figure 20.47 Example of count start operation by hardware source started at the input of the signal from the ELC_GPTA

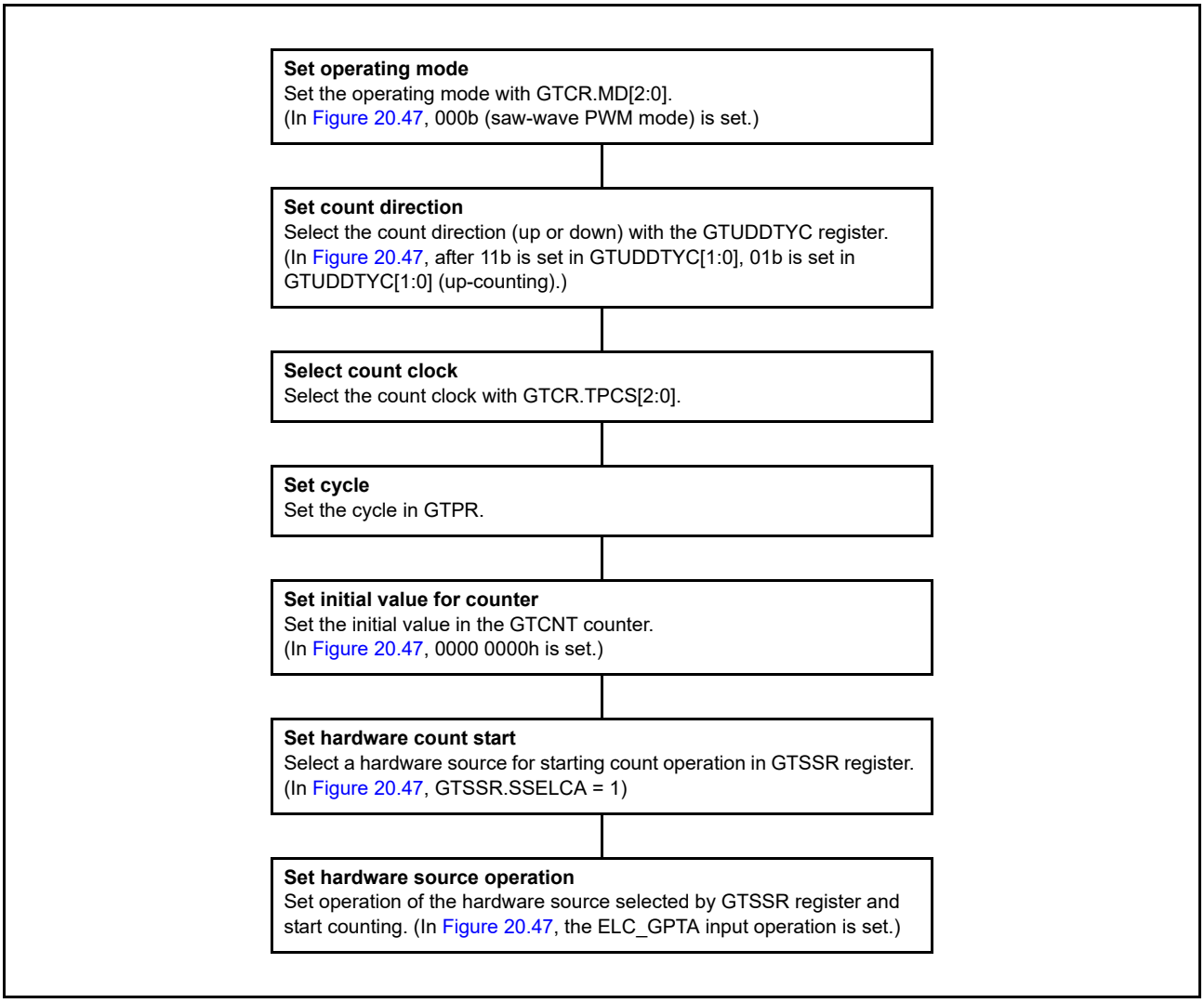


Figure 20.48 Example setting count start operation by hardware source

20.3.7.2 Hardware stop operation

The GTCNT counter can be stopped by selecting a hardware source using GTPSR.

Figure 20.49 shows an example of a count stop operation by a hardware source. Figure 20.50 shows the setting example. In this example, the count operation stops at the edge of the ELC_GPTA input and restarts at the edges of the ELC_GPTB input.

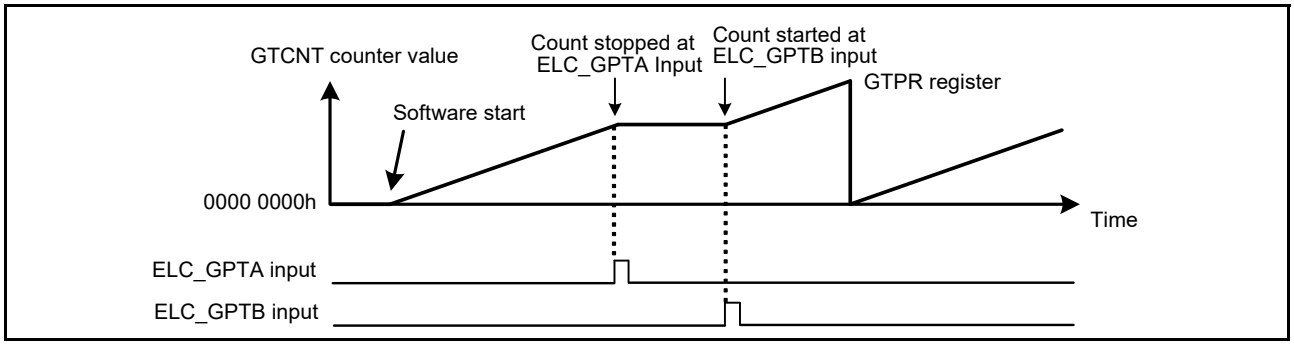


Figure 20.49 Example of count stop operation by hardware source started by software, stopped at ELC_GPTA input, and restarted at ELC_GPTB input

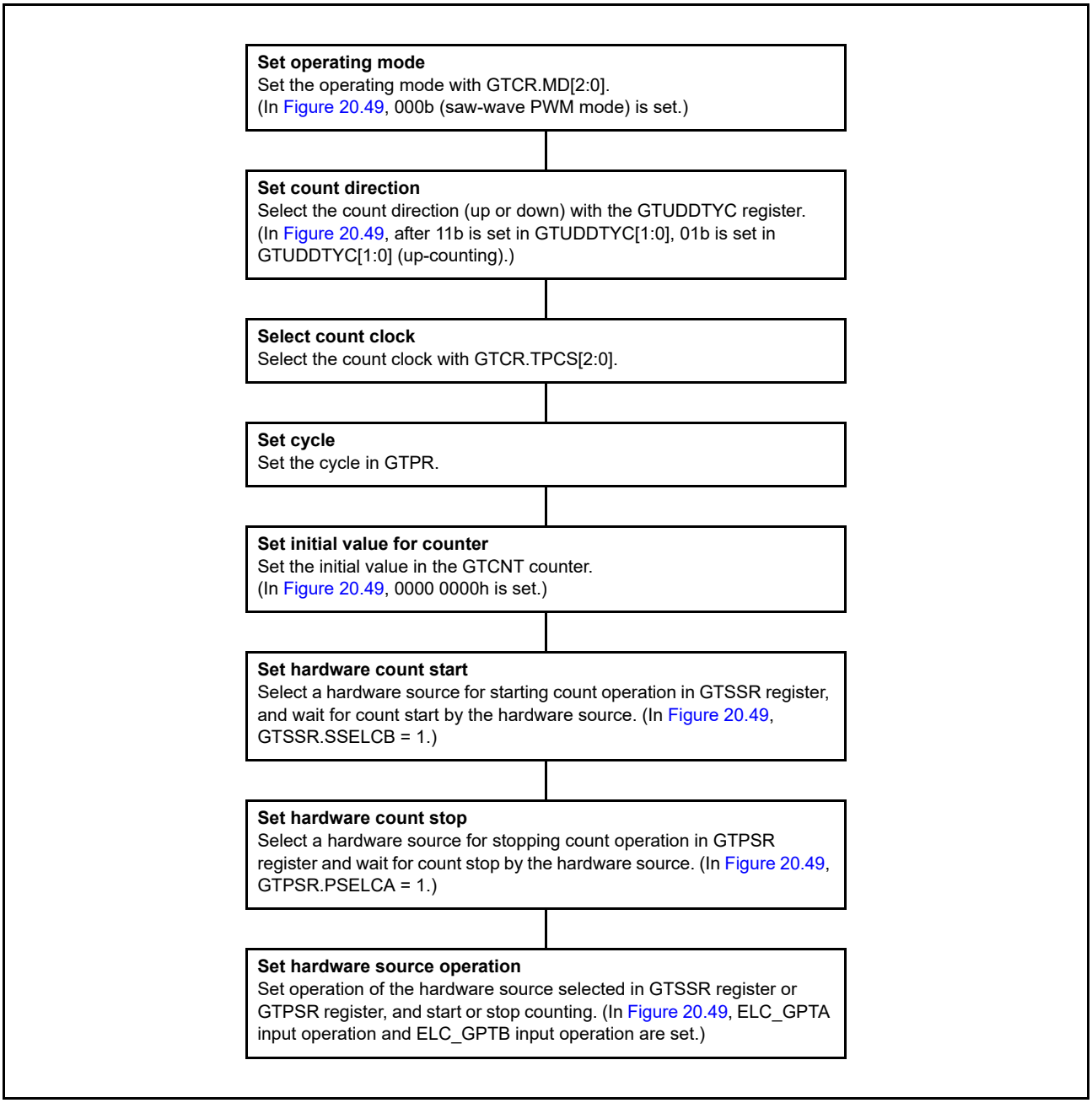


Figure 20.50 Example for setting count stop operation by hardware source

Figure 20.51 shows an example of a count start/stop operation by a hardware source. Figure 20.52 shows the setting example. In this example, the counter operates during the high-level periods of the external trigger input GTETRGA.

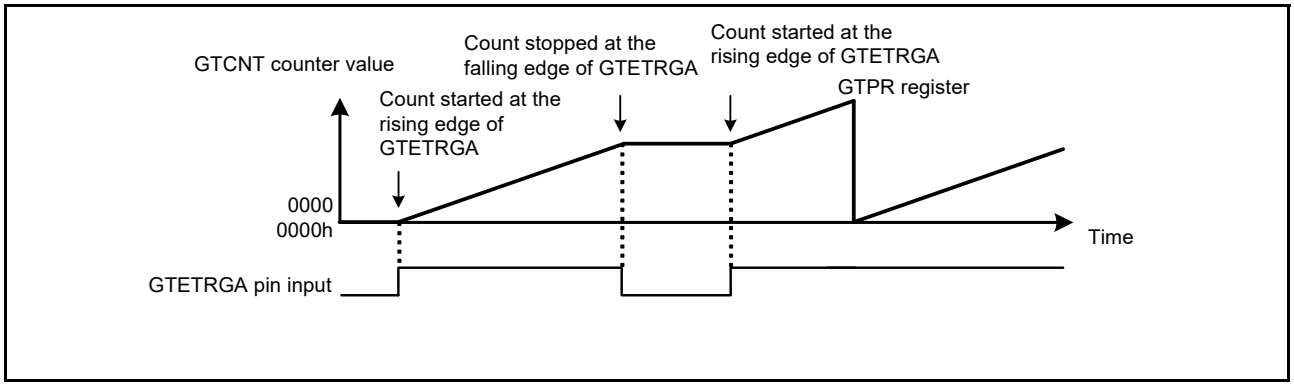


Figure 20.51 Example of count start/stop operation by hardware source started at rising edge of GTETRGA pin input, and stopped at falling edge of GTETRGA pin input

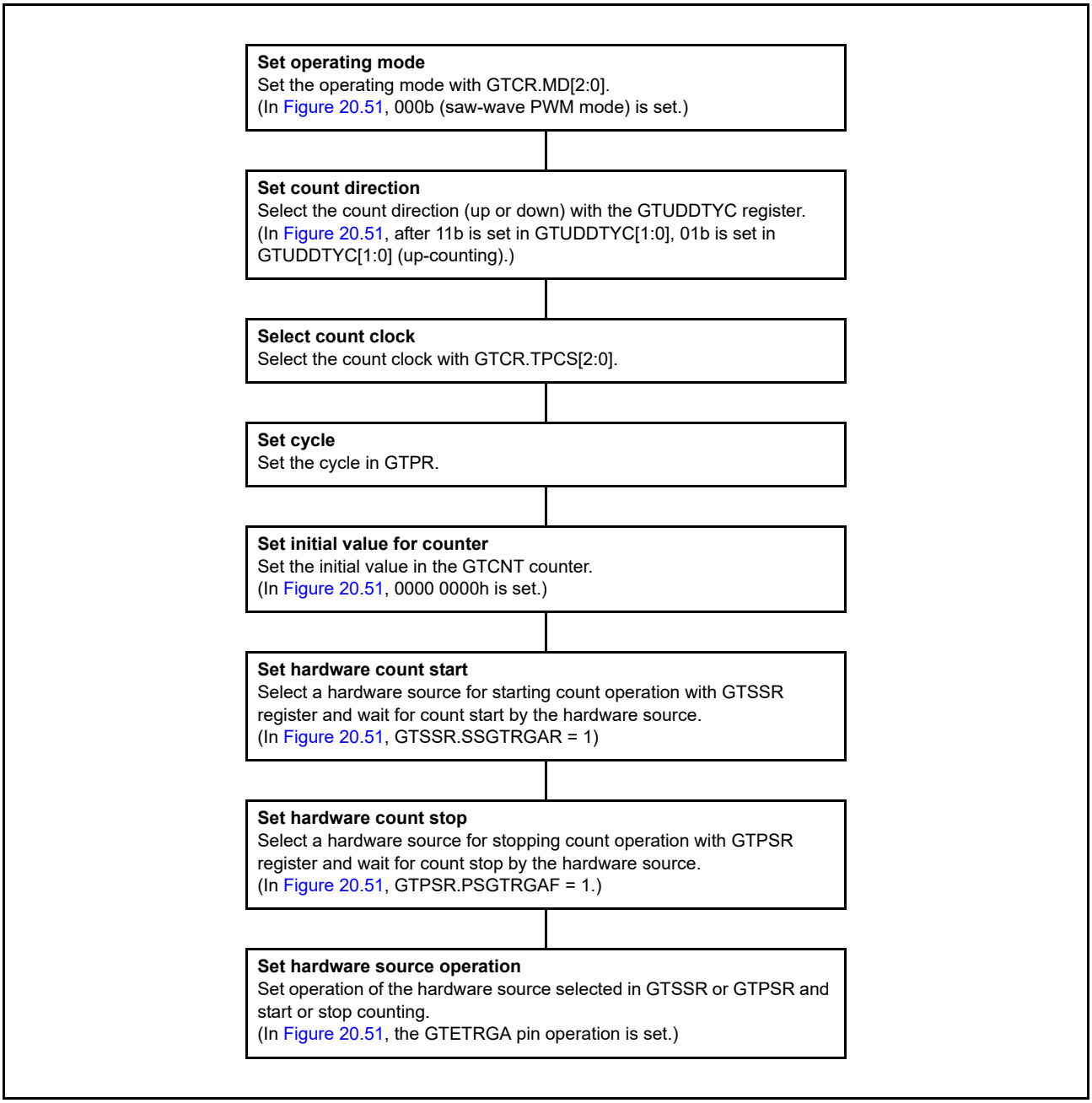


Figure 20.52 Example for setting count start/stop operation by hardware source

20.3.7.3 Hardware clear operation

The GTCNT counter can be cleared by selecting a hardware source using GTCSR.

Note: The GPTn_OVF/GPTn_UDF (n = 0 to 6) interrupt (overflow/underflow interrupt) is not generated when the GTCNT counter is cleared by a hardware source or by software.

Figure 20.53 and Figure 20.54 show examples of the GTCNT counter clearing operation by a hardware source. Figure 20.55 shows the setting example. In this example, the GTCNT counter starts at the edge of the ELC_GPTA input, and the counter stops/clears at the edge of the ELC_GPTB input.

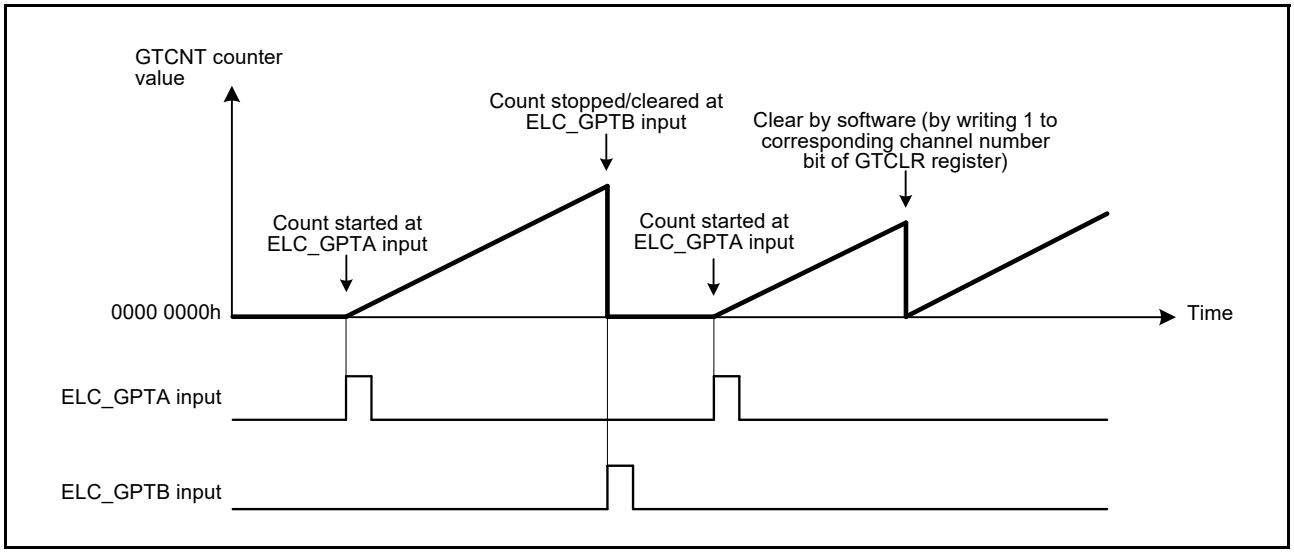


Figure 20.53 Examples of count clearing operation by hardware source in saw wave up-counting, started at ELC_GPTA input, and stopped/cleared at ELC_GPTB input

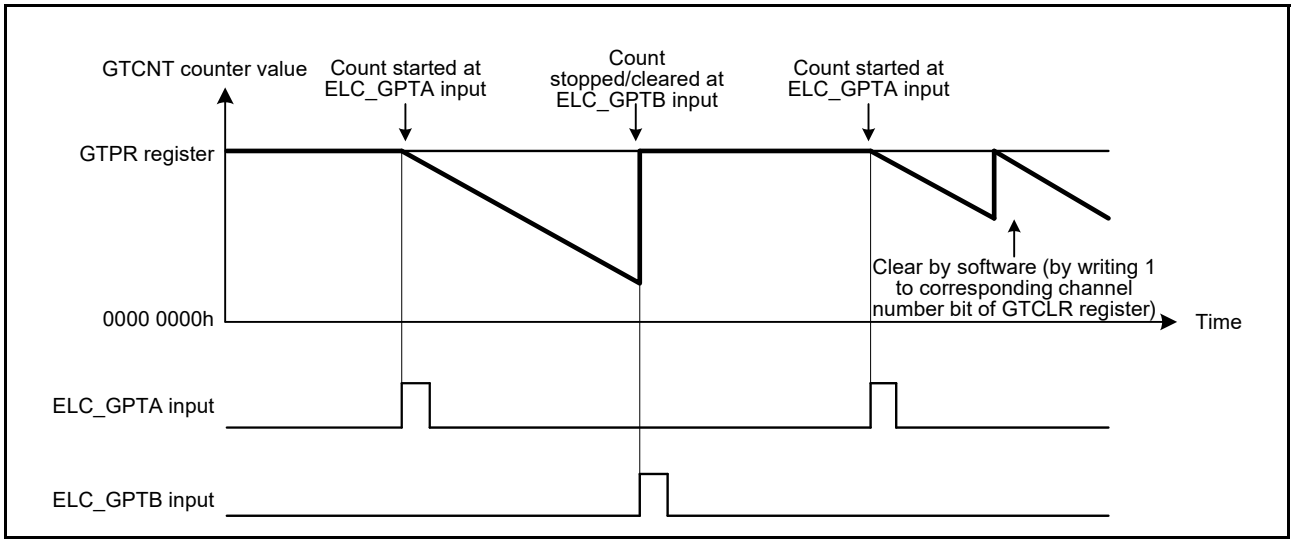


Figure 20.54 Examples of count clearing operation by hardware source in saw wave down-counting, started at ELC_GPTA input, and stopped/cleared at ELC_GPTB input

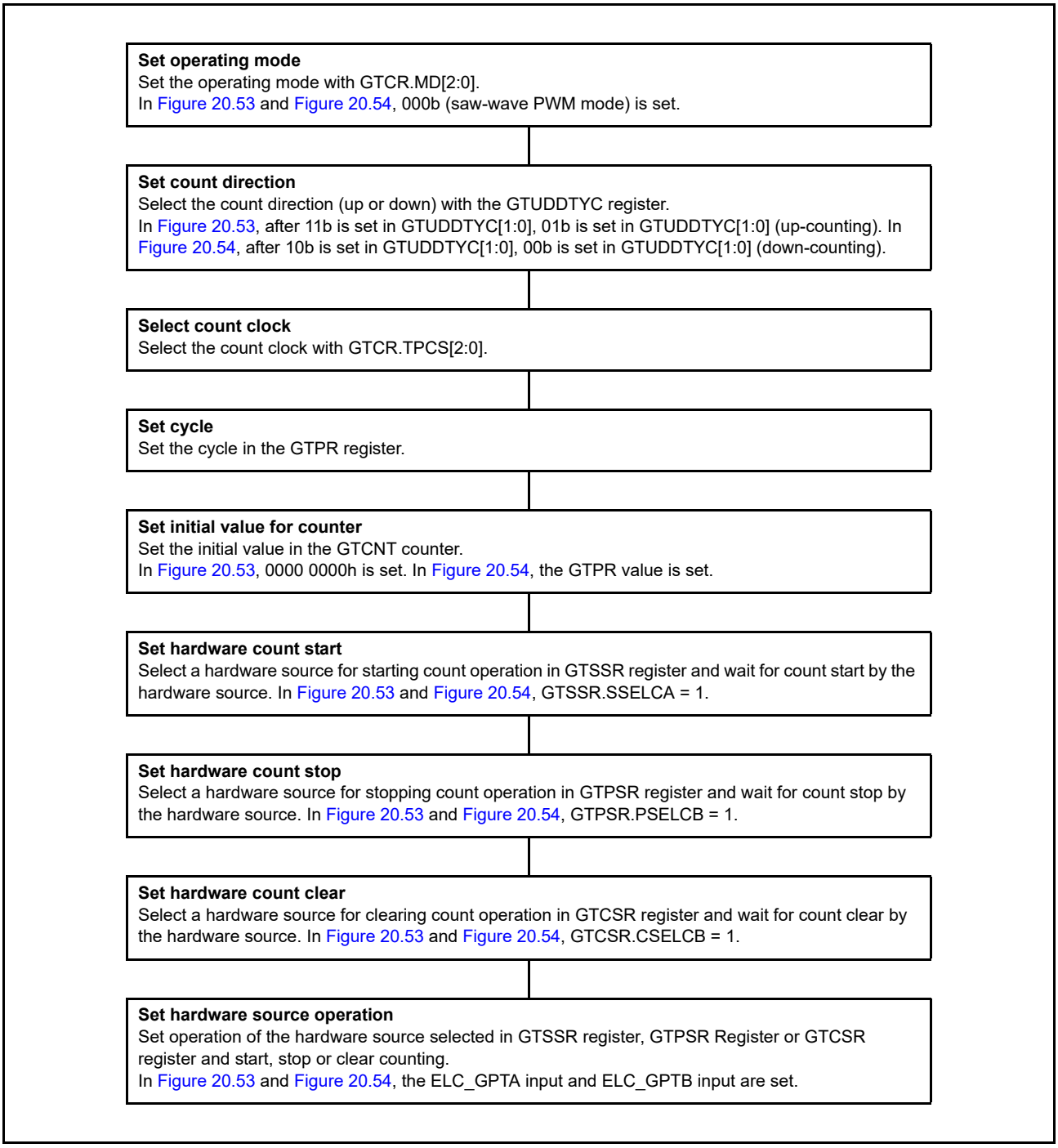


Figure 20.55 Example for setting count clearing operation by hardware source

The GPTn_OVF/GPTn_UDF (n = 0 to 6) interrupt (overflow/underflow interrupt) is not generated when the counter is cleared by a hardware source or by software.

Figure 20.56 shows the relationship between the counter clearing by a hardware source and the GPTn_OVF (n = 0 to 6) interrupt.

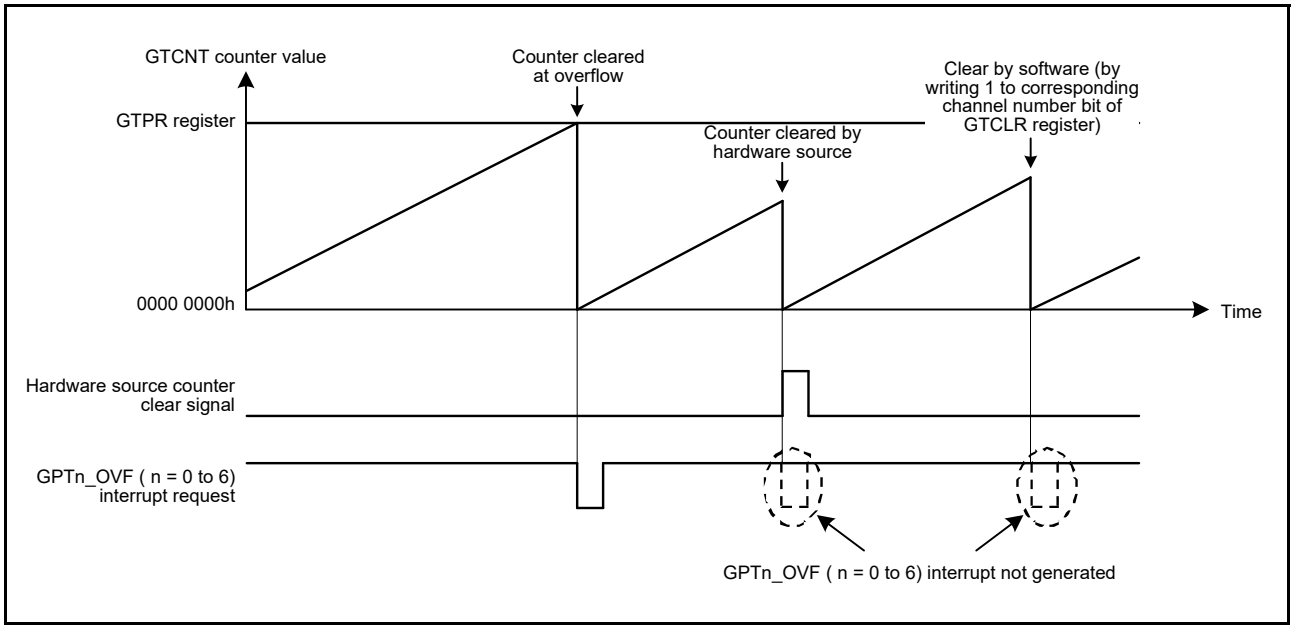


Figure 20.56 Relationship between counter clearing by hardware source and GPTn_OVF (n = 0 to 6) interrupt

20.3.8 Synchronized Operation

Synchronized operation on channels such as a synchronized start, stop and clear operation can be performed.

20.3.8.1 Synchronized operation by software

The GTCNT counters can be started, stopped and cleared on multiple channels by setting the corresponding GTSTR, GTSTP or GTCLR bits simultaneously to 1.

Count start with a phase difference is possible by setting the initial value in the GTCNT counter and setting the corresponding GTSTR bits simultaneously to 1.

Figure 20.57 shows an example of a simultaneous start, stop and clear by software. Figure 20.58 shows an example of phase start operation by software.

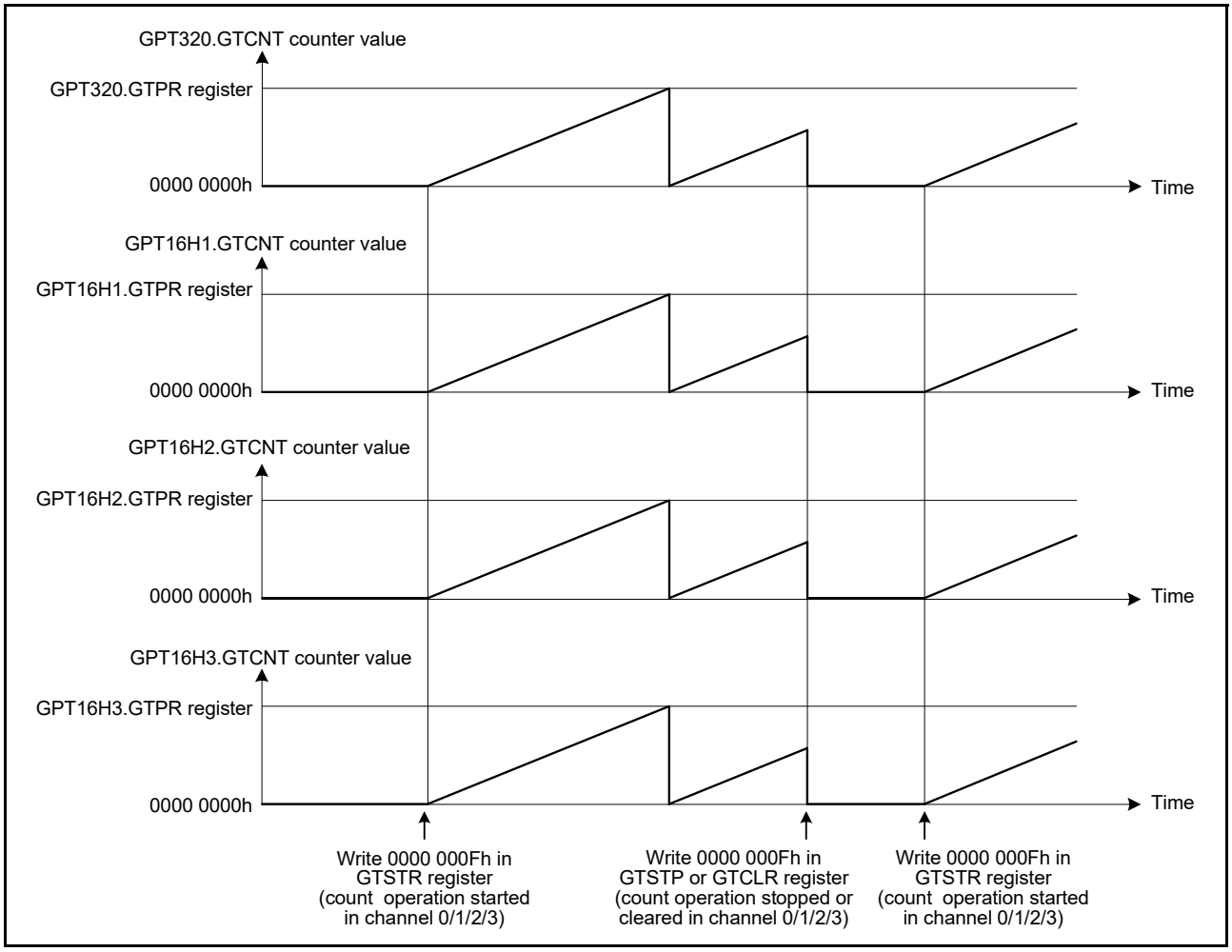


Figure 20.57 Example of a simultaneous start, stop and clear by software with the same count cycle (GTPR register value)

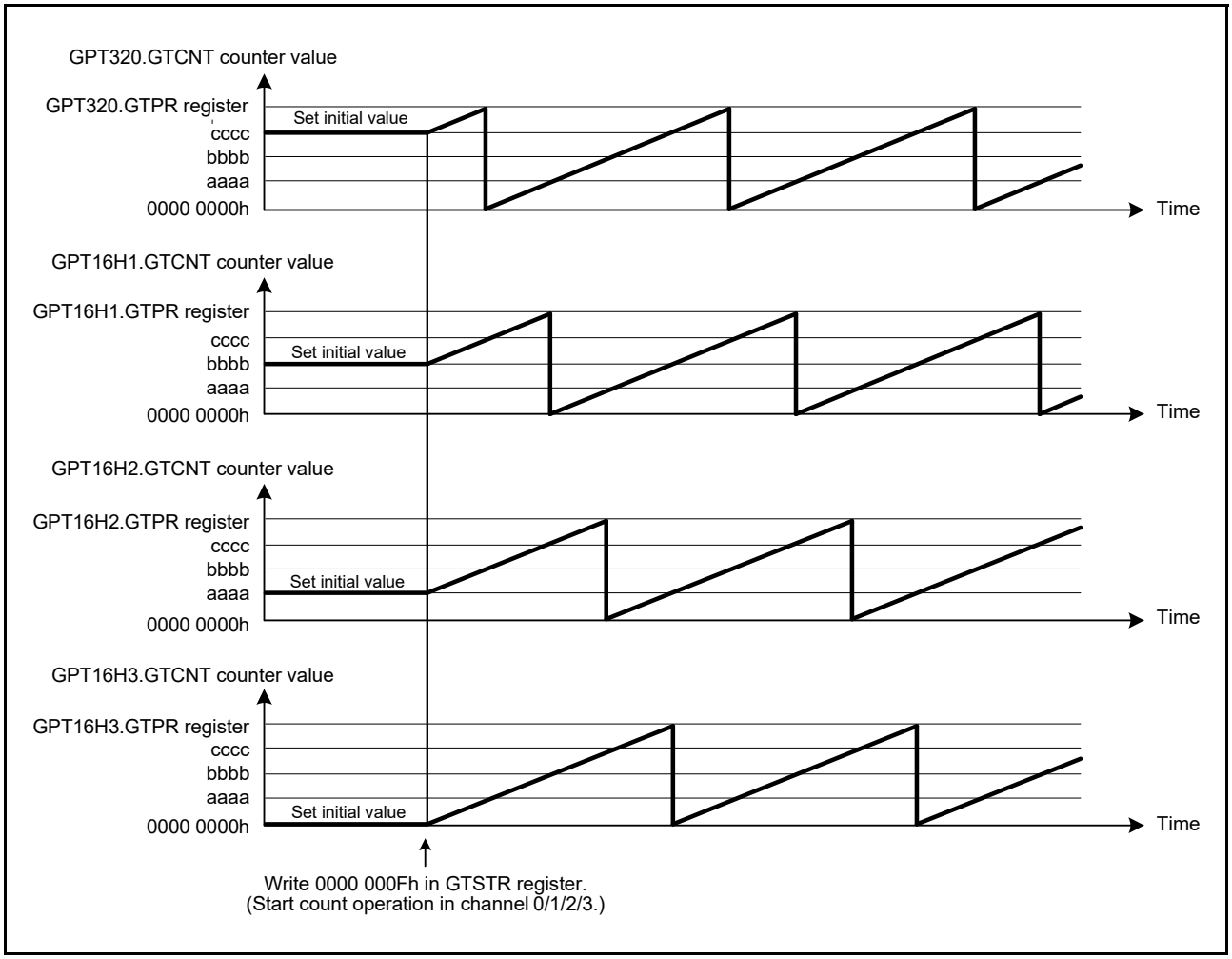


Figure 20.58 Example of software phase start with the same count cycle (GTPR register value)

20.3.8.2 Synchronized operation by hardware

The GTCNT counters can be started simultaneously by the following hardware sources:

- External trigger input
- ELC event input.

Figure 20.59 shows an example of a simultaneous start, stop and clear operation by a hardware source. Figure 20.60 shows the setting example.

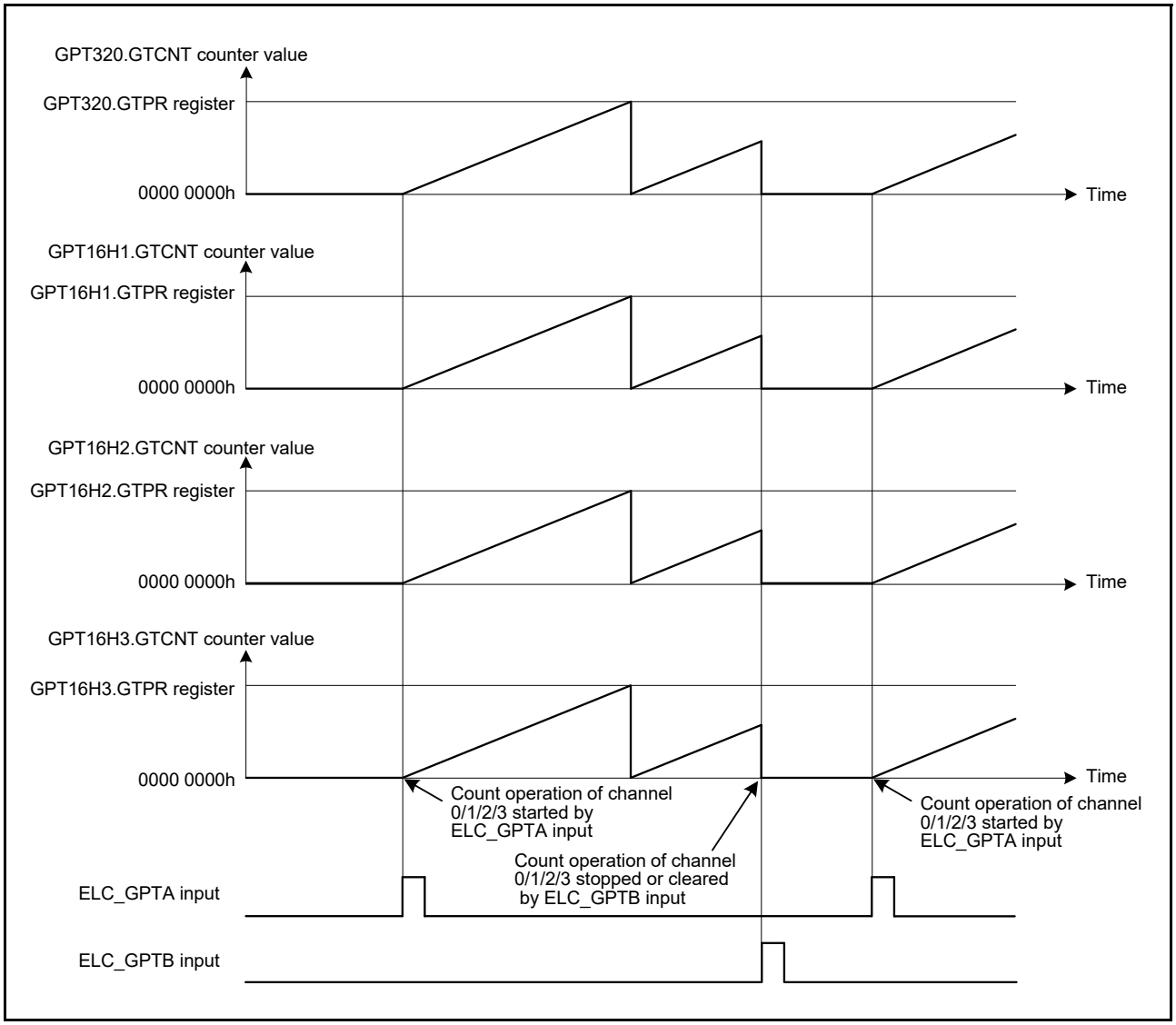


Figure 20.59 Example of a simultaneous start, stop and clear by hardware source with the same count cycle (GTPR register value)

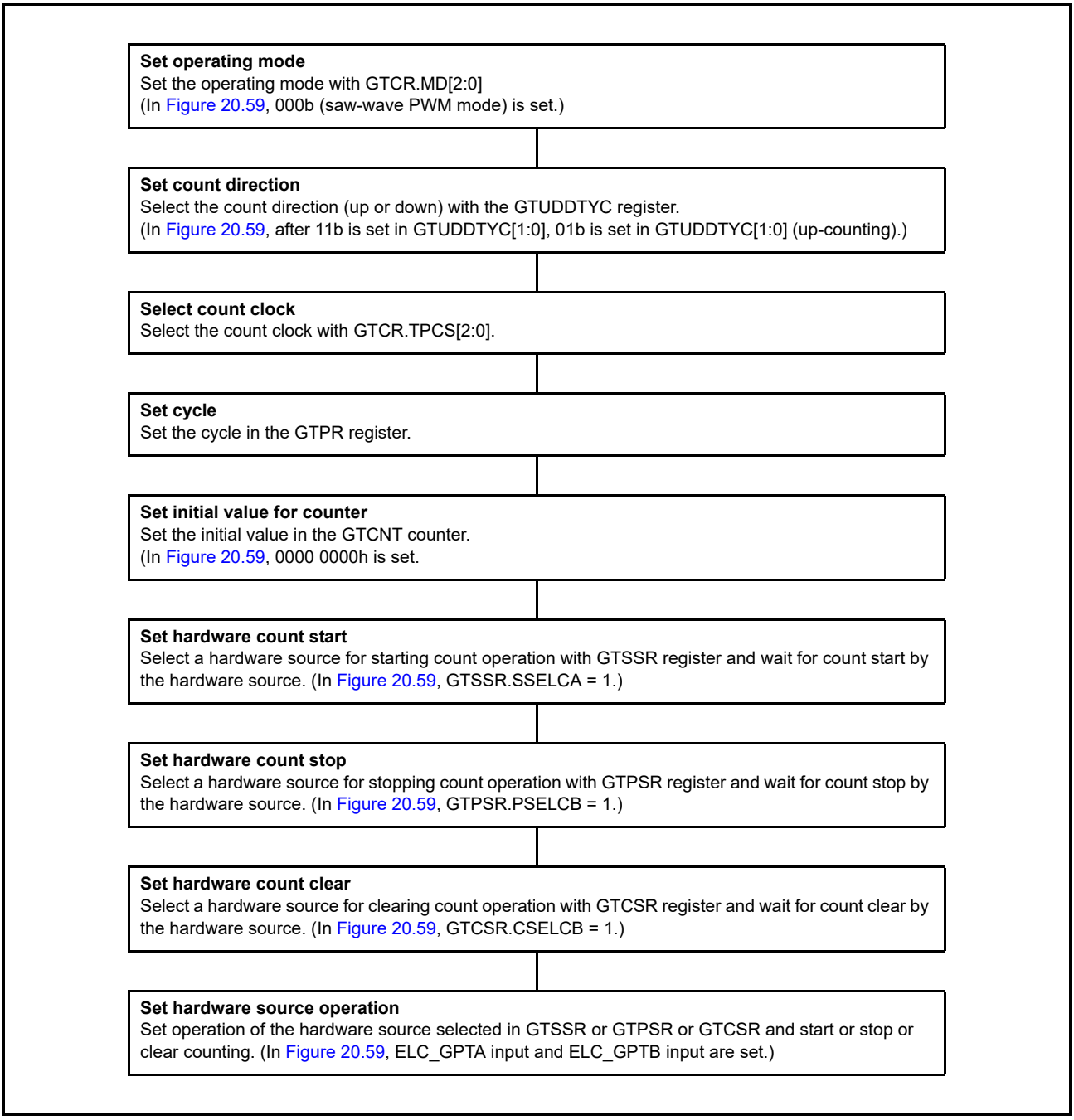


Figure 20.60 Example for setting simultaneous start by hardware source

20.3.9 PWM Output Operation Examples

(1) Synchronized PWM output

The GPT output 14 phases of linked PWM waveforms for a maximum of seven channels by multiple GPTs.

Figure 20.61 shows an example in which four channels perform synchronized operation in saw-wave PWM mode and eight phases of PWM waveforms are output. The GTIOCA is set so that it outputs low as the initial value, high at a GTCCRA compare match, and low at the cycle end. The GTIOCB is set so that it outputs low as the initial value, high at a GTCCRB compare match, and low at the cycle end.

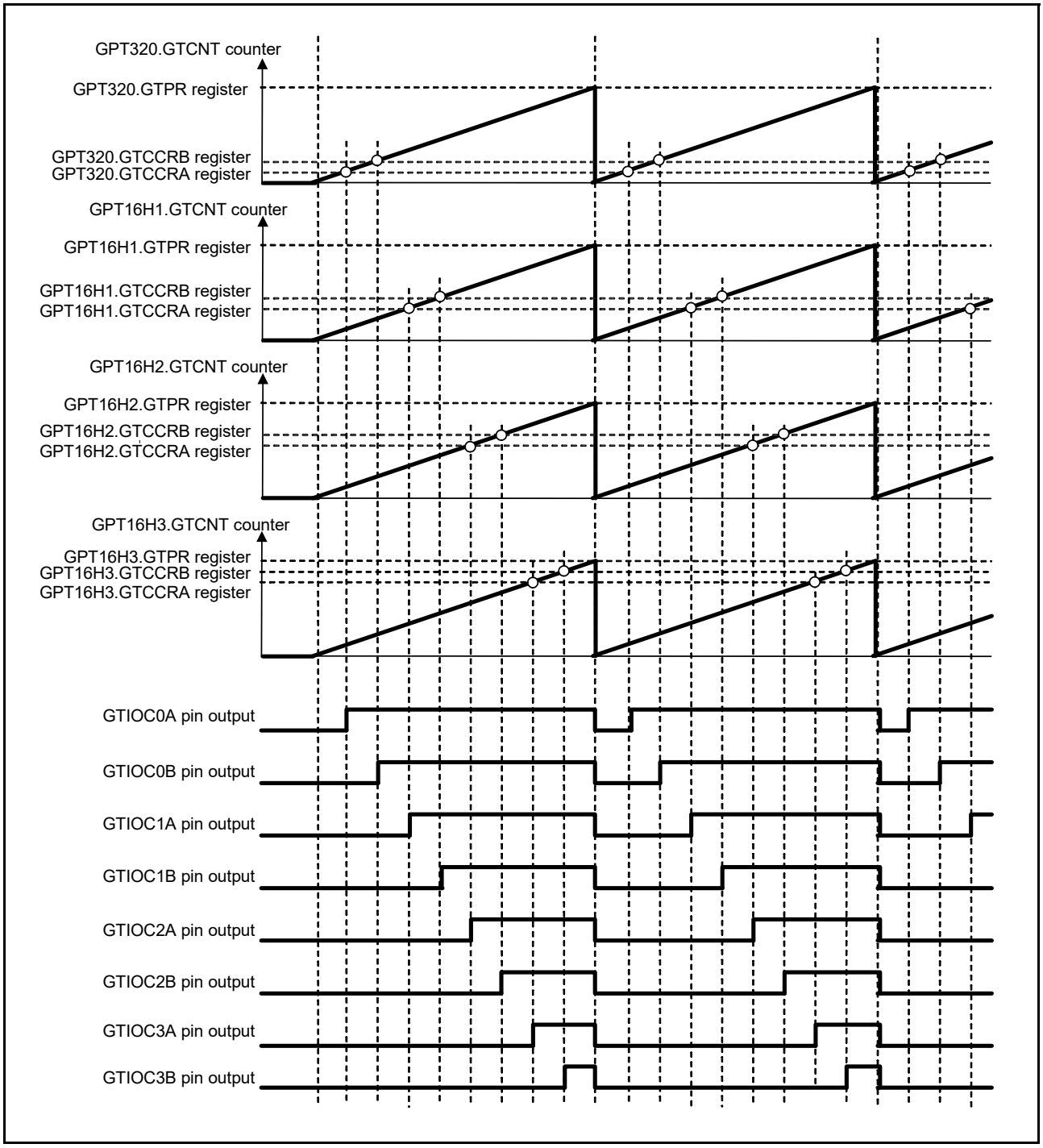


Figure 20.61 Example of synchronized PWM output

(2) 3-phase saw-wave complementary PWM output

Figure 20.62 shows an example in which three channels perform synchronized operation in saw-wave PWM mode and 3-phase complementary PWM waveforms are output. The GTIOCA pin is set so that it outputs low as the initial value, high at a GTCCRA compare match, and low at the cycle end. The GTIOCB pin is set so that it outputs high as the initial value, low at a GTCCRB compare match, and high at the cycle end.

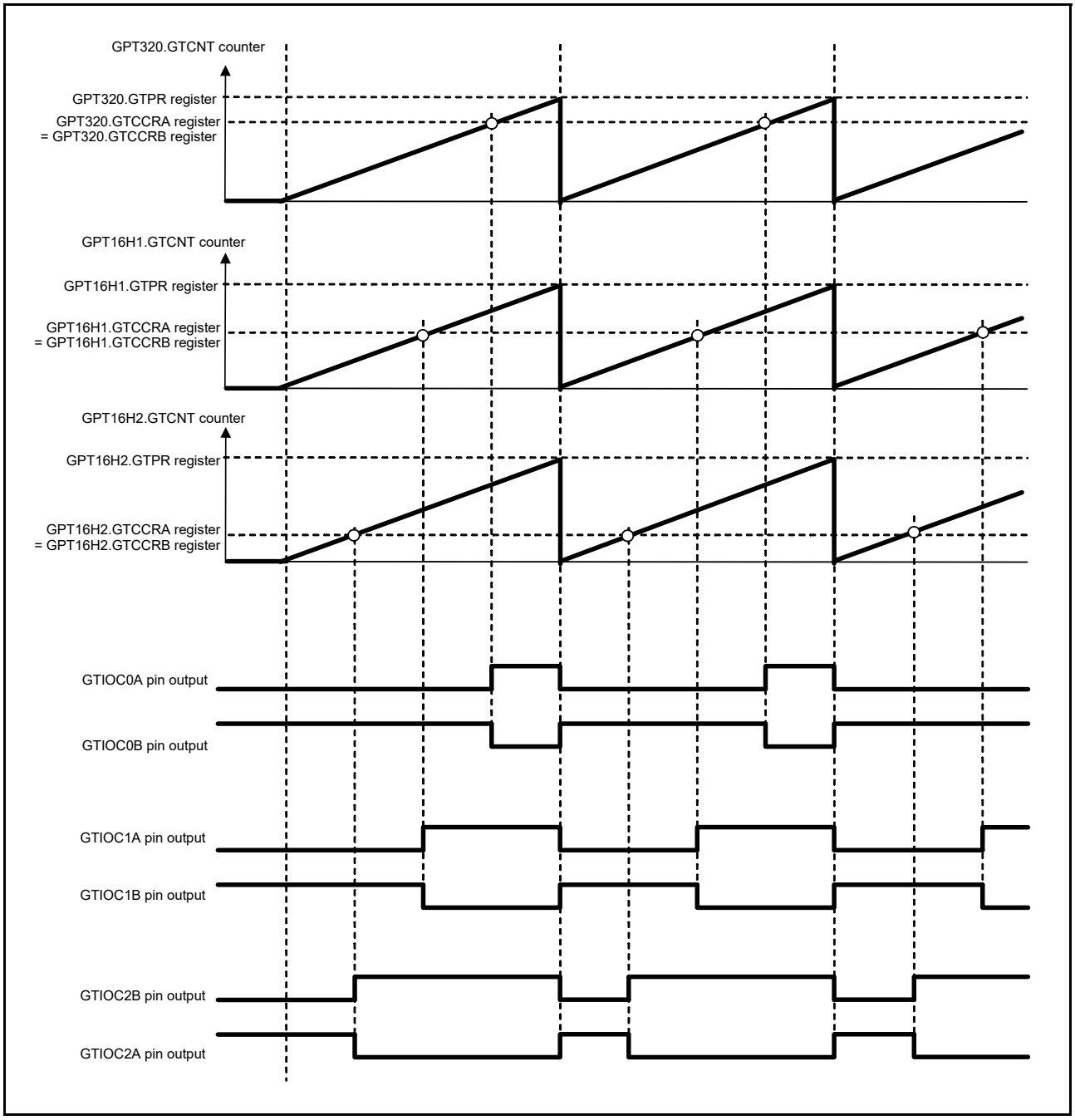


Figure 20.62 Example of 3-phase saw-wave complementary PWM output

(3) 3-phase saw-wave complementary PWM output with automatic dead time setting

Figure 20.63 shows an example in which three channels perform synchronized operation in saw-wave one-shot pulse mode with automatic dead time setting and 3-phase complementary PWM waveforms are output. The GTIOCA pin is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCB pin is set so that it outputs high as the initial value, toggles the output at a GTCCRB compare match, and retains the output at the cycle end.

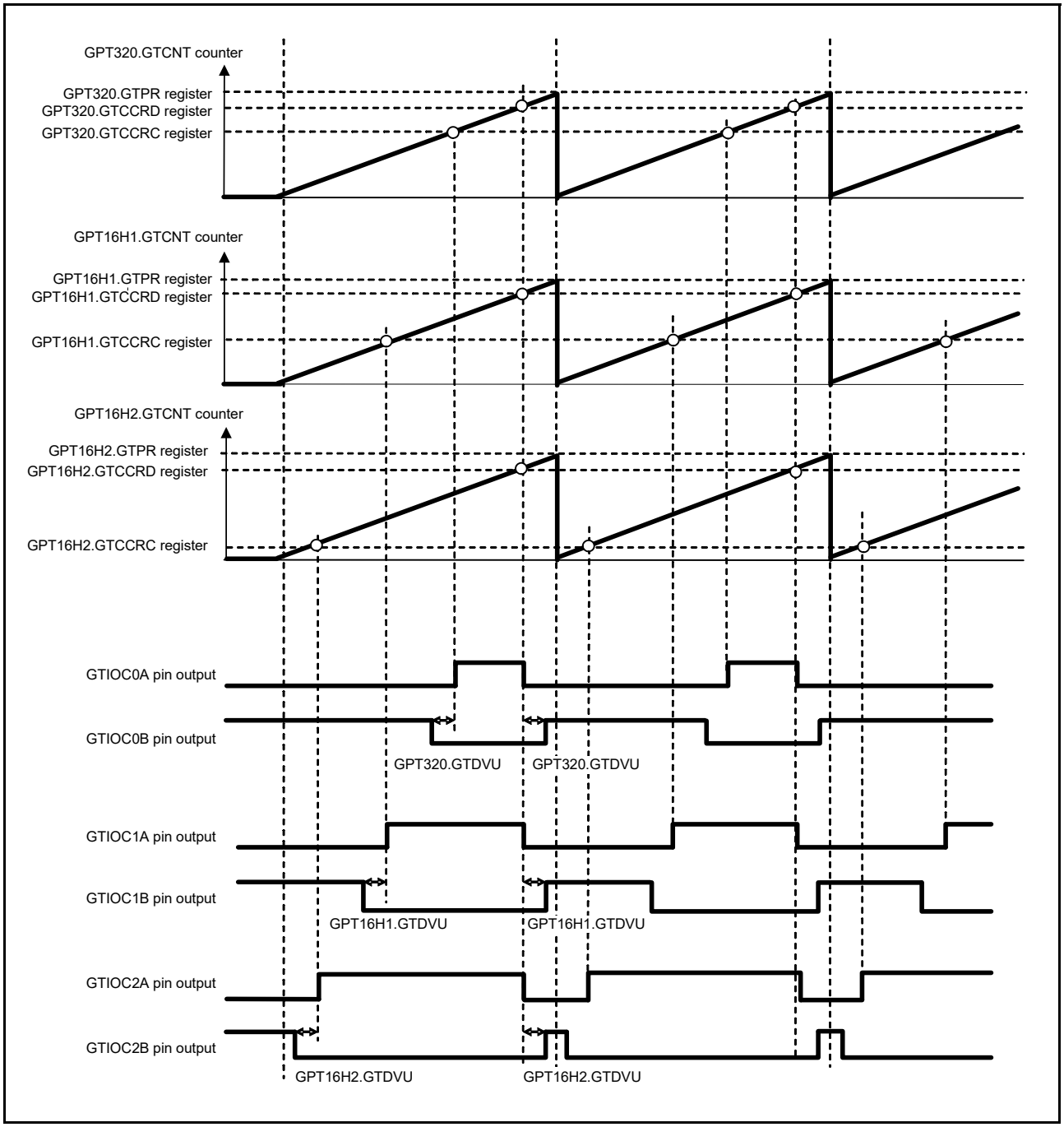


Figure 20.63 Example of 3-phase saw-wave complementary PWM output with automatic dead time setting

(4) 3-phase triangle-wave complementary PWM output

Figure 20.64 shows an example in which three channels perform synchronized operation in triangle-wave PWM mode 1 and 3-phase complementary PWM waveforms are output. The GTIOCA pin is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCB pin is set so that it outputs high as the initial value, toggles the output at a GTCCRB compare match, and retains the output at the cycle end.

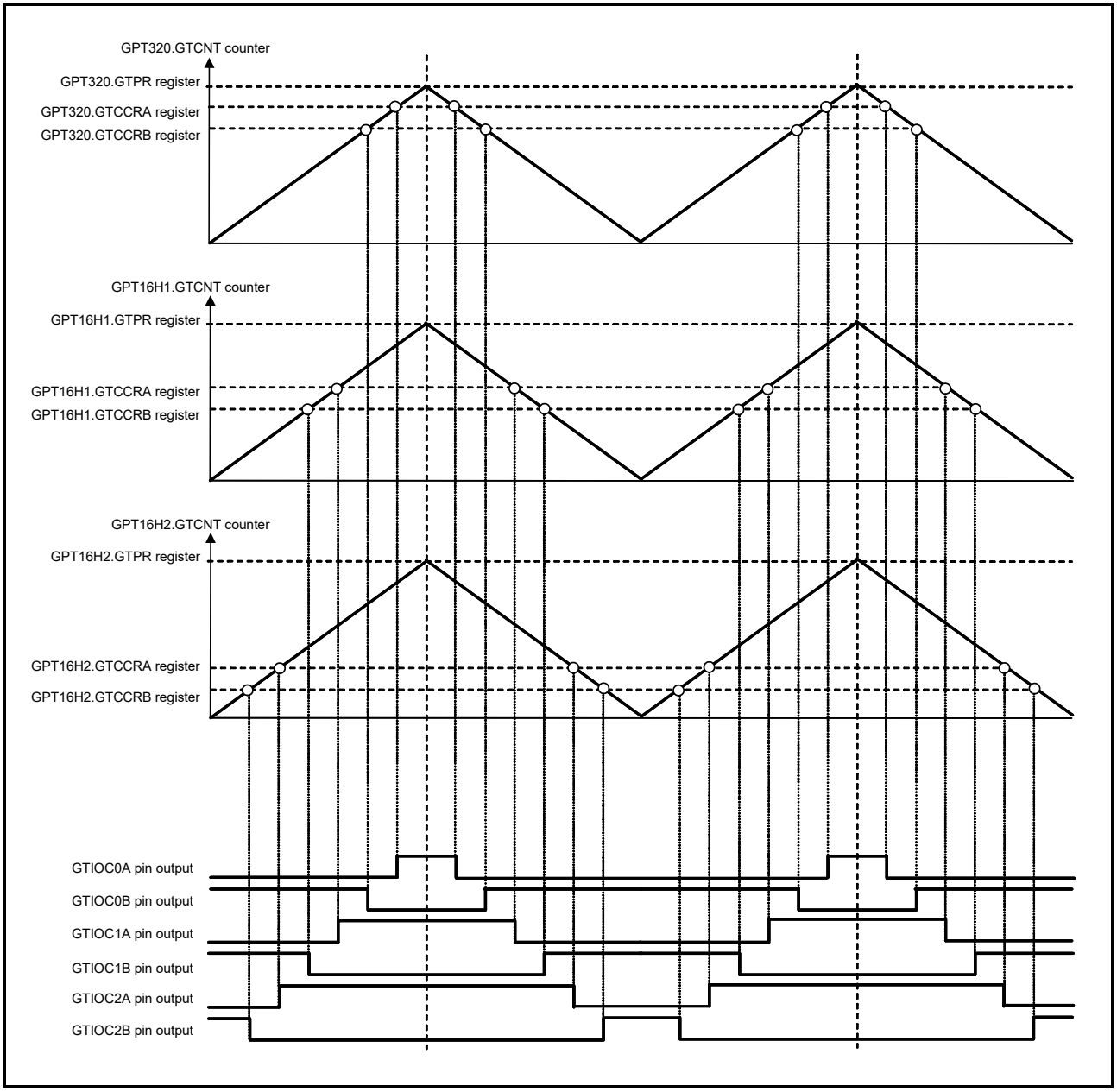


Figure 20.64 Example of 3-phase triangle-wave complementary PWM output

(5) 3-phase triangle-wave complementary PWM output with automatic dead time setting

Figure 20.65 shows an example in which three channels perform synchronized operation in triangle-wave PWM mode 1 with automatic dead time setting and 3-phase complementary PWM waveforms are output. The GTIOCA pin is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCB pin is set so that it outputs high as the initial value, toggles the output at a GTCCRB compare match, and retains the output at the cycle end.

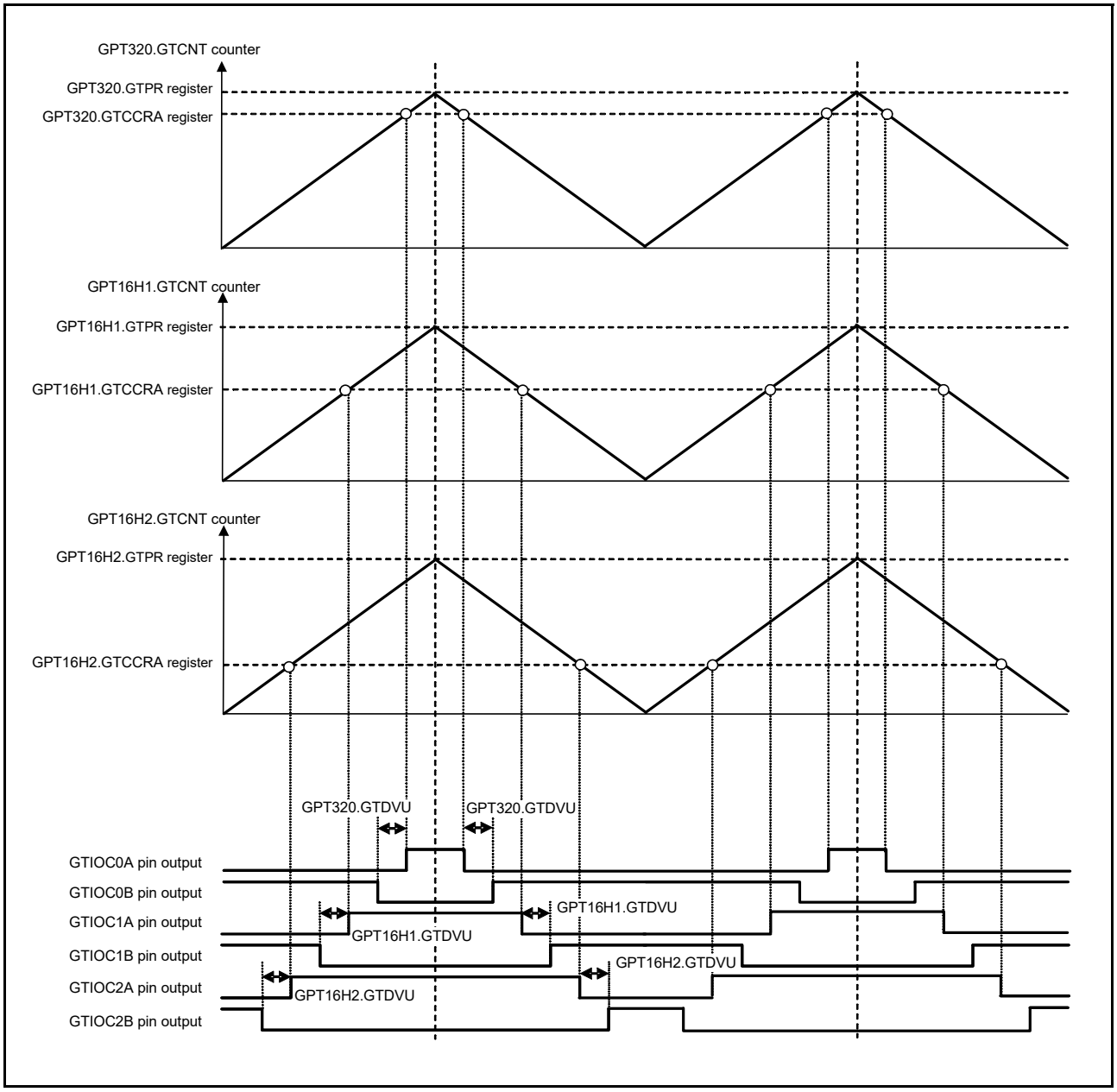


Figure 20.65 Example of 3-phase triangle-wave complementary PWM output with automatic dead time setting

(6) 3-phase asymmetric triangle-wave complementary PWM output with automatic dead time setting

Figure 20.66 shows an example in which three channels perform synchronized operation in triangle-wave PWM mode 3 with automatic dead time setting and 3-phase complementary PWM waveforms are output. The GTIOCA is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCB is set so that it outputs high as the initial value, toggles the output at a GTCCRB compare match, and retains the output at the cycle end.

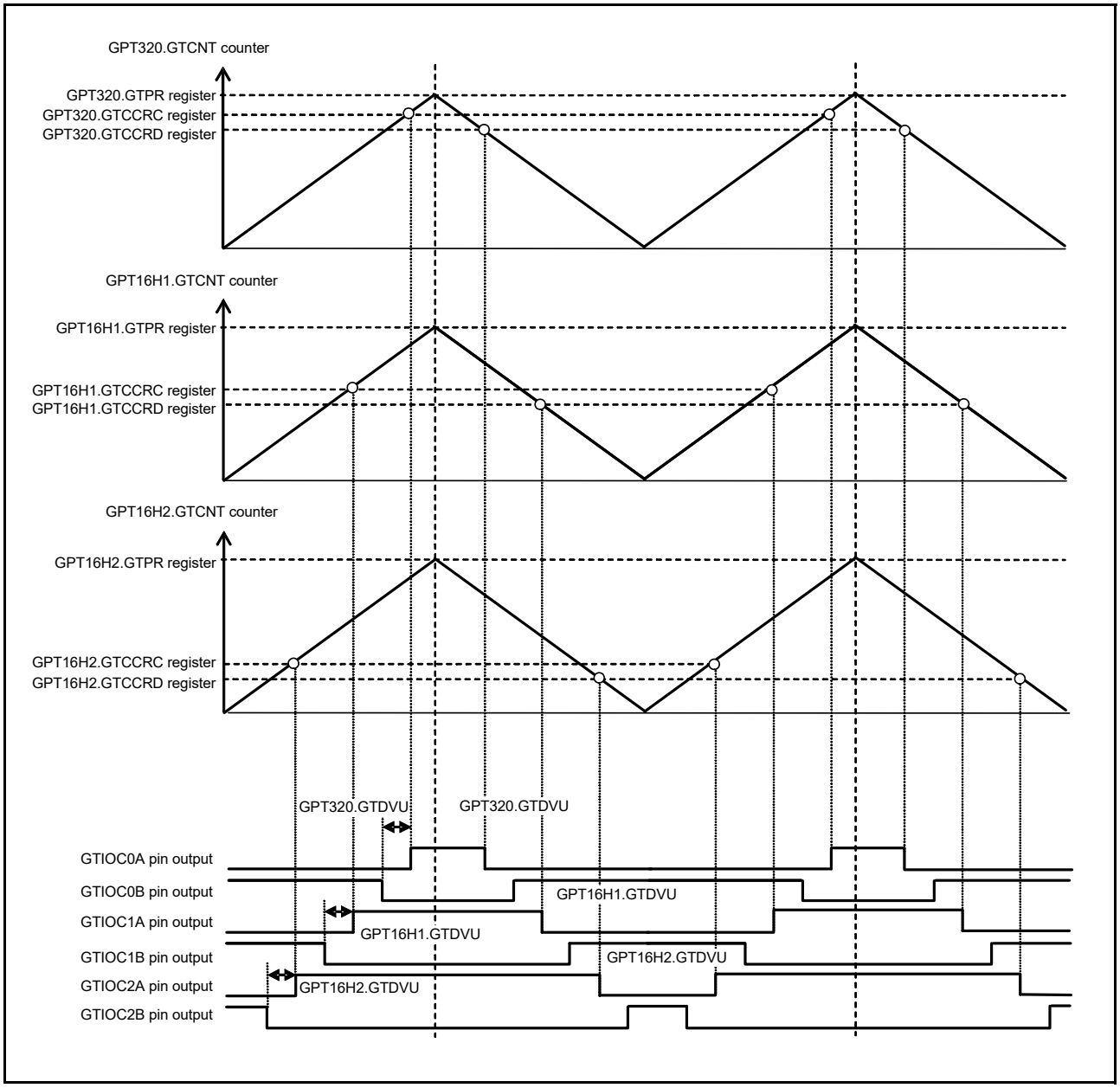


Figure 20.66 Example of 3-phase asymmetric triangle-wave complementary PWM output with automatic dead time setting

20.3.10 Phase Counting Function

The phase difference between the GTIOCA and GTIOCB pin input is detected and the corresponding GTCNT counts up or counts down. The detectable phase difference is available in any combination with the relationship between the edge and the level of GTIOCA pin and GTIOCB pin input being set in the GTUPSR and GTDNSR registers. For details on count operation, see section 20.3.1.1, Counter operation.

Figure 20.67 to Figure 20.76 show phase counting modes 1 to 5. Table 20.7 to Table 20.16 show conditions of up-counting or down-counting and list settings for the GTUPSR and GTDNSR registers.

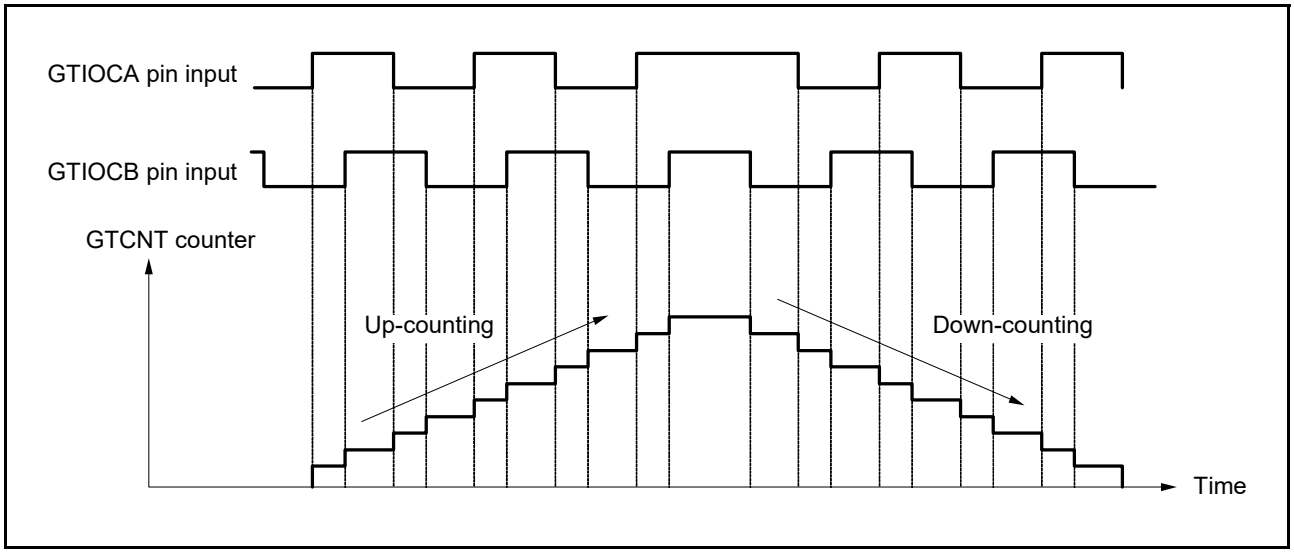


Figure 20.67 Example of phase counting mode 1

Table 20.7 Conditions of up-counting/down-counting in phase counting mode 1

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
High	↑	Up-counting	GTUPSR = 00006900h GTDNSR = 00009600h
Low	↓		
↑	Low		
↓	High		
High	↓	Down-counting	
Low	↑		
↑	High		
↓	Low		

↑ : Rising edge

↓ : Falling edge

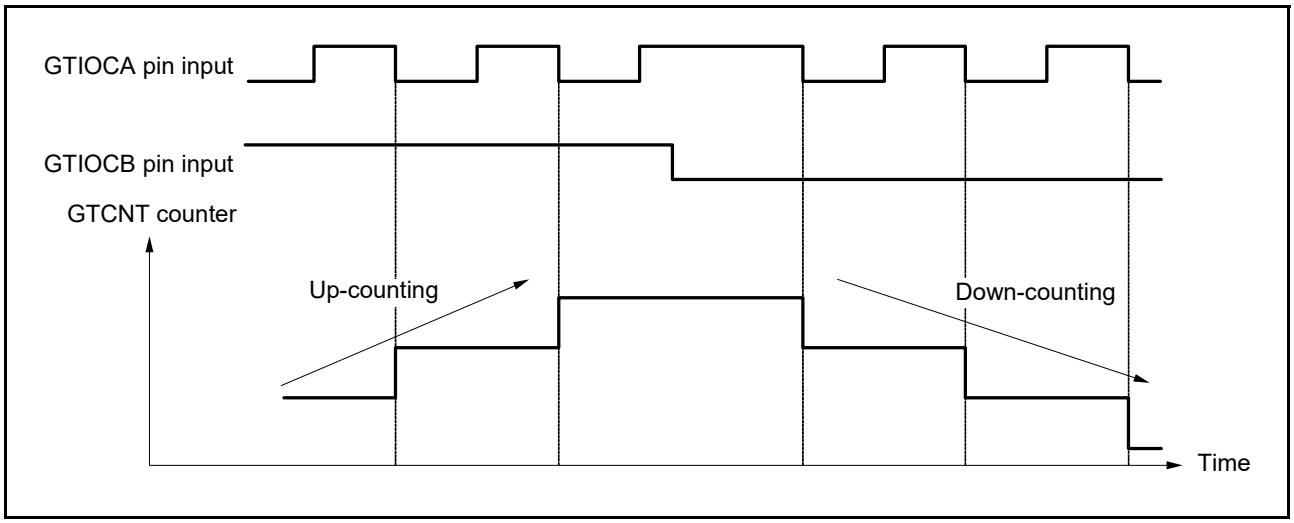


Figure 20.68 Example of phase counting mode 2 (A)

Table 20.8 Conditions of up-counting/down-counting in phase counting mode 2 (A)

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
High	↑	Don't care	GTUPSR = 00000800h GTDNSR = 00000400h
Low	↓		
↑	Low		
↓	High	Up-counting	
High	↓	Don't care	
Low	↑		
↑	High		
↓	Low	Down-counting	

↑ : Rising edge

↓ : Falling edge

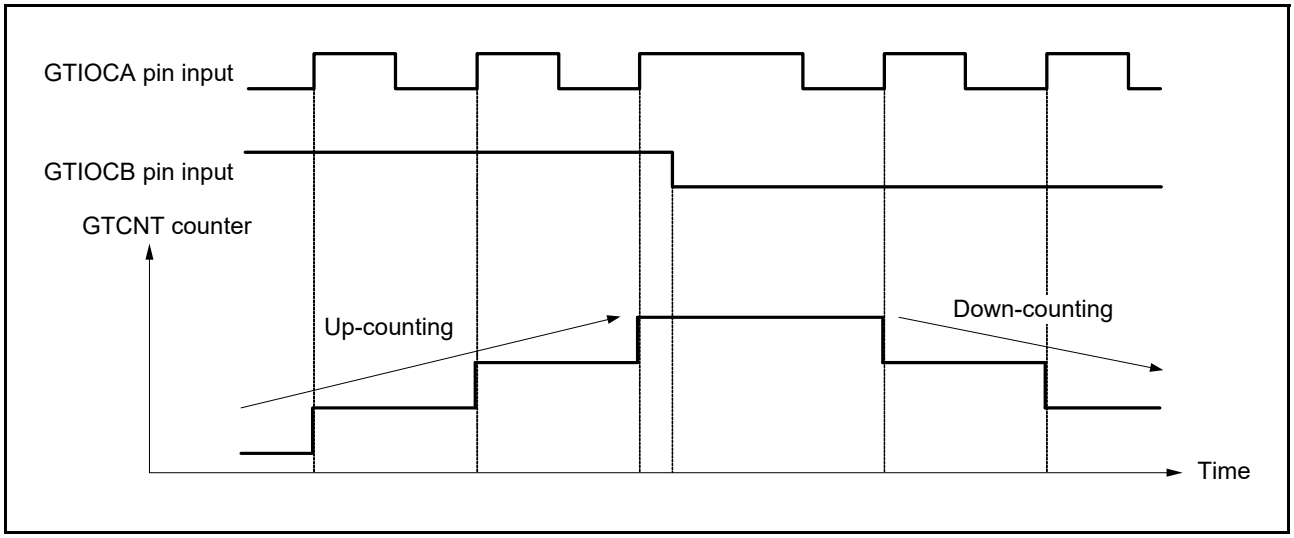


Figure 20.69 Example of phase counting mode 2 (B)

Table 20.9 Conditions of up-counting/down-counting in phase counting mode 2 (B)

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
High	↑	Don't care	GTUPSR = 00000200h GTDNSR = 00000100h
Low	↓		
↑	Low	Down-counting	
↓	High	Don't care	
High	↓		
Low	↑		
↑	High	Up-counting	
↓	Low	Don't care	

↑ : Rising edge

↓ : Falling edge

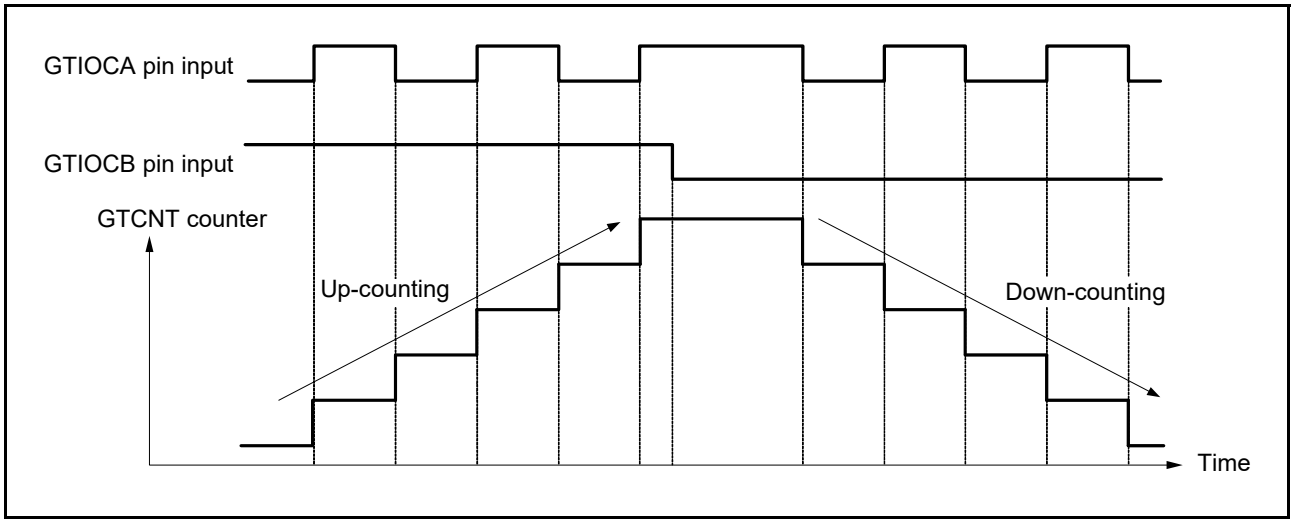


Figure 20.70 Example of phase counting mode 2 (C)

Table 20.10 Conditions of up-counting/down-counting in phase counting mode 2 (C)

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
High	↑	Don't care	GTUPSR = 00000A00h GTDNSR = 00000500h
Low	↓		
↑	Low	Down-counting	
↓	High	Up-counting	
High	↓	Don't care	
Low	↑		
↑	High	Up-counting	
↓	Low	Down-counting	

↑ : Rising edge

↓ : Falling edge

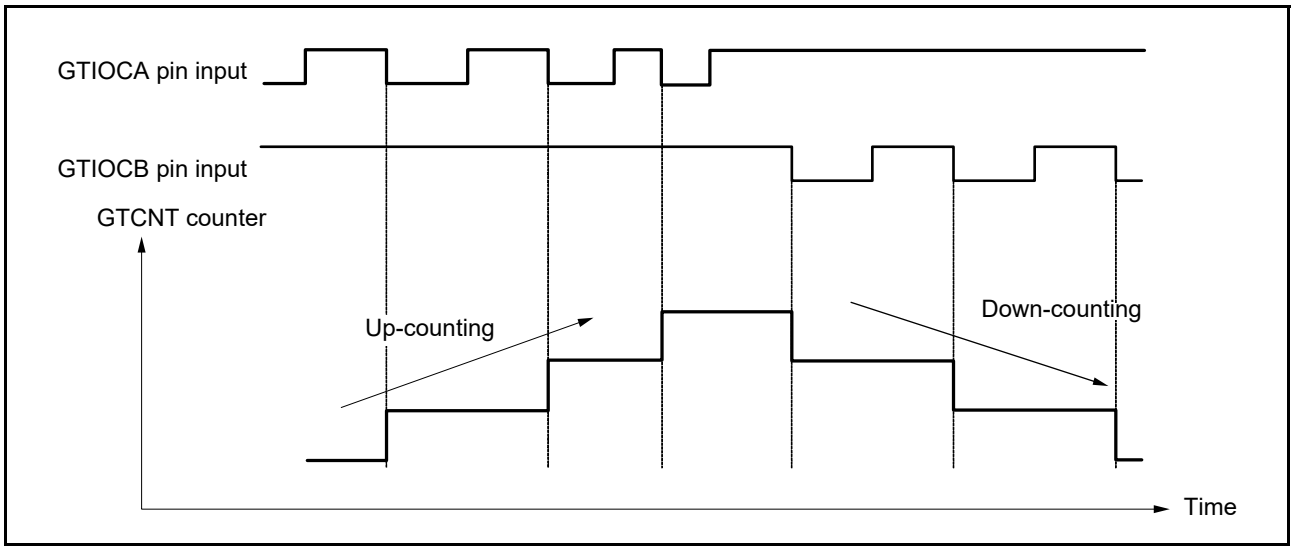


Figure 20.71 Example of phase counting mode 3 (A)

Table 20.11 Conditions of up-counting/down-counting in phase counting mode 3 (A)

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
High	↑	Don't care	GTUPSR = 00000800h GTDNSR = 00008000h
Low	↓		
↑	Low		
↓	High	Up-counting	
High	↓	Down-counting	
Low	↑	Don't care	
↑	High		
↓	Low		

↑ : Rising edge

↓ : Falling edge

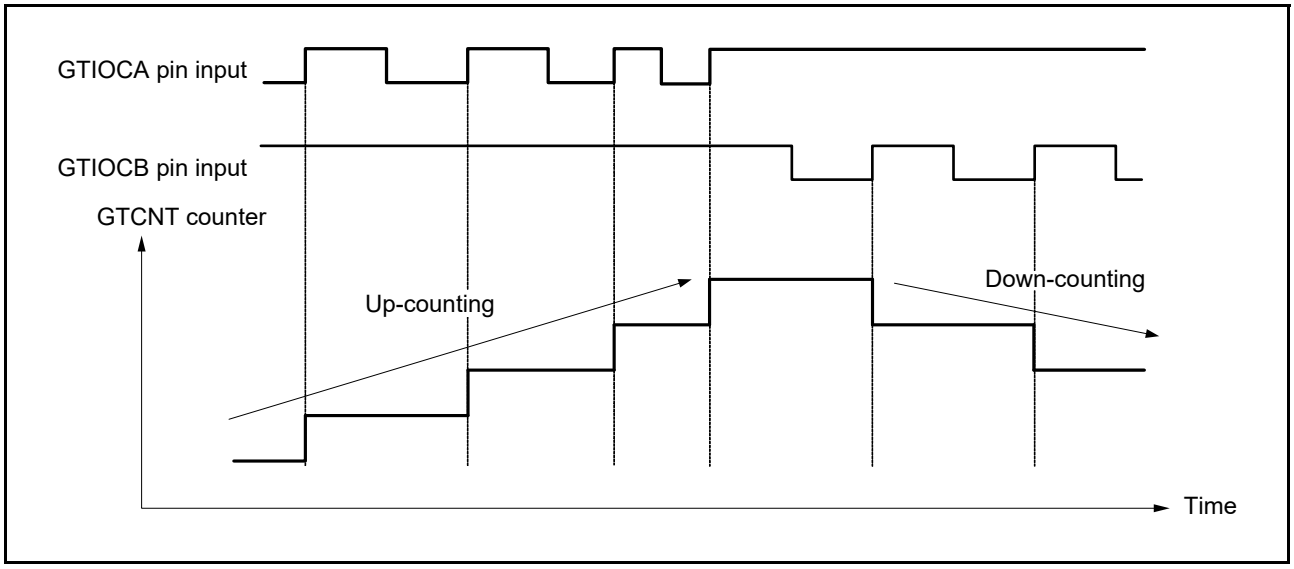


Figure 20.72 Example of phase counting mode 3 (B)

Table 20.12 Conditions of up-counting/down-counting in phase counting mode 3 (B)

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
High	↑	Down-counting	GTUPSR = 00000200h GTDNSR = 00002000h
Low	↓	Don't care	
↑	Low		
↓	High		
High	↓		
Low	↑		
↑	High	Up-counting	
↓	Low	Don't care	

↑ : Rising edge

↓ : Falling edge

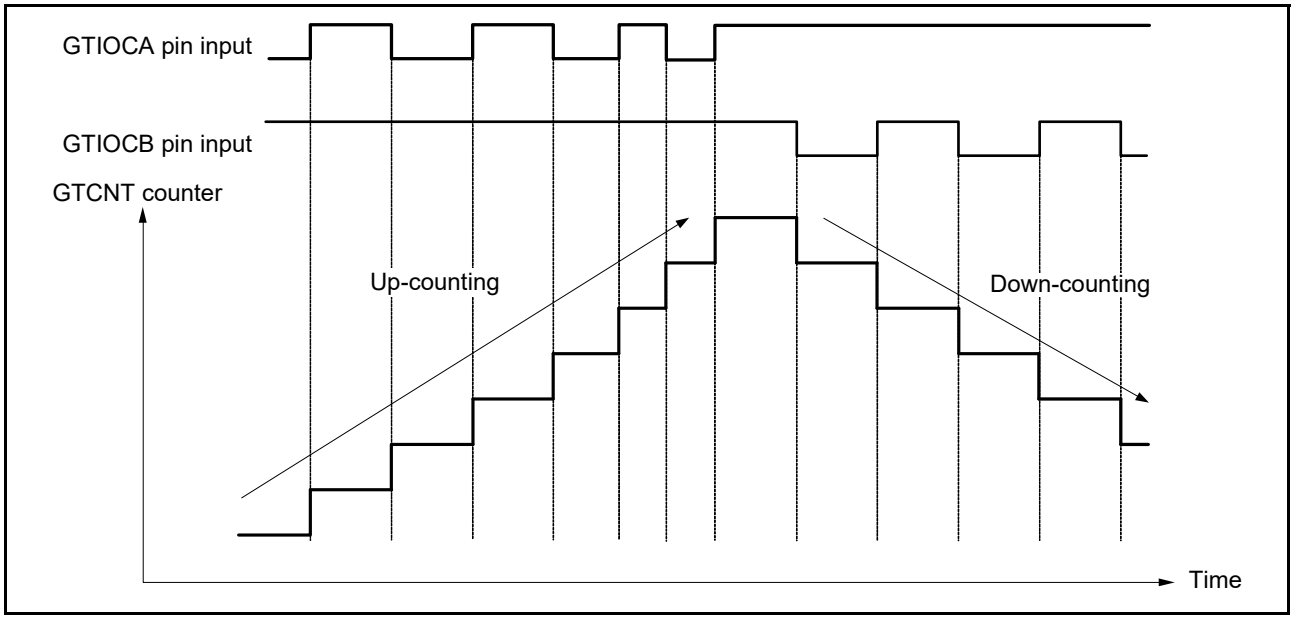


Figure 20.73 Example of phase counting mode 3 (C)

Table 20.13 Conditions of up-counting/down-counting in phase counting mode 3 (C)

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
High	↑	Down-counting	GTUPSR = 00000A00h GTDNSR = 0000A000h
Low	↓	Don't care	
↑	Low		
↓	High	Up-counting	
High	↓	Down-counting	
Low	↑	Don't care	
↑	High	Up-counting	
↓	Low	Don't care	

↑ : Rising edge

↓ : Falling edge

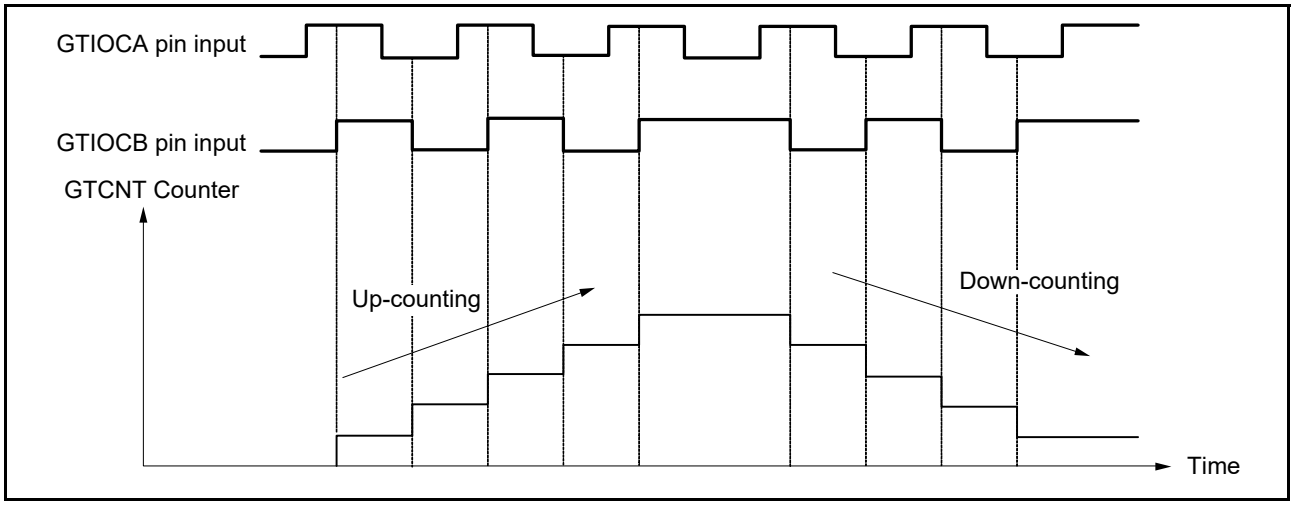


Figure 20.74 Example of phase counting mode 4

Table 20.14 Conditions of up-counting/down-counting in phase counting mode 4

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
High	↑	Up-counting	GTUPSR = 00006000h GTDNSR = 00009000h
Low	↓		
↑	Low	Don't care	
↓	High		
High	↓	Down-counting	
Low	↑		
↑	High	Don't care	
↓	Low		

↑ : Rising edge

↓ : Falling edge

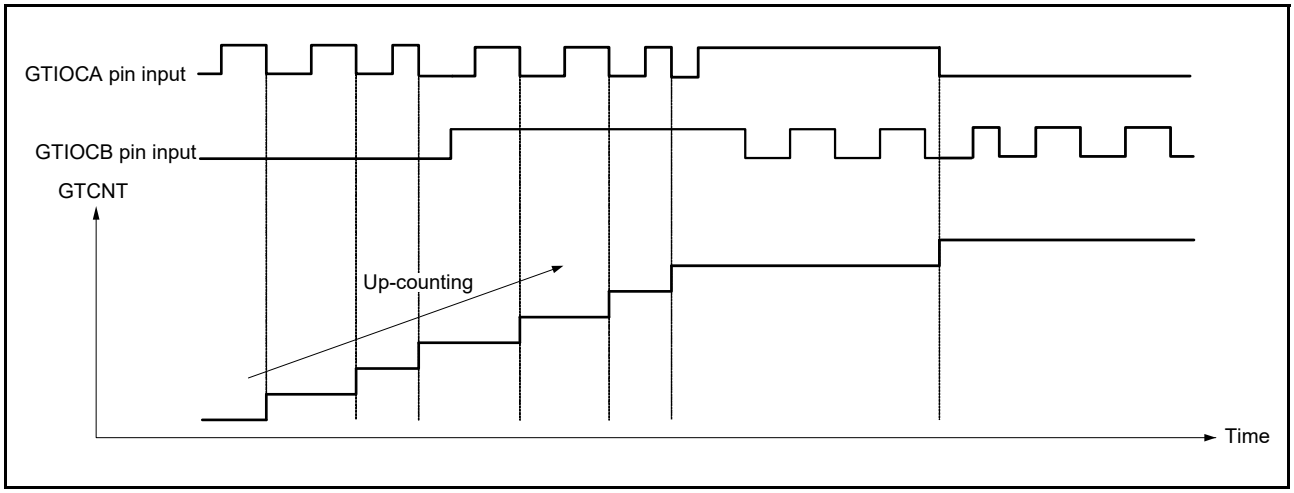


Figure 20.75 Example of phase counting mode 5 (A)

Table 20.15 Conditions of up-counting/down-counting in phase counting mode 5 (A)

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
High	↑	Don't care	GTUPSR = 00000C00h GTDNSR = 00000000h
Low	↓		
↑	Low		
↓	High	Up-counting	
High	↓	Don't care	
Low	↑		
↑	High		
↓	Low	Up-counting	

↑ : Rising edge

↓ : Falling edge

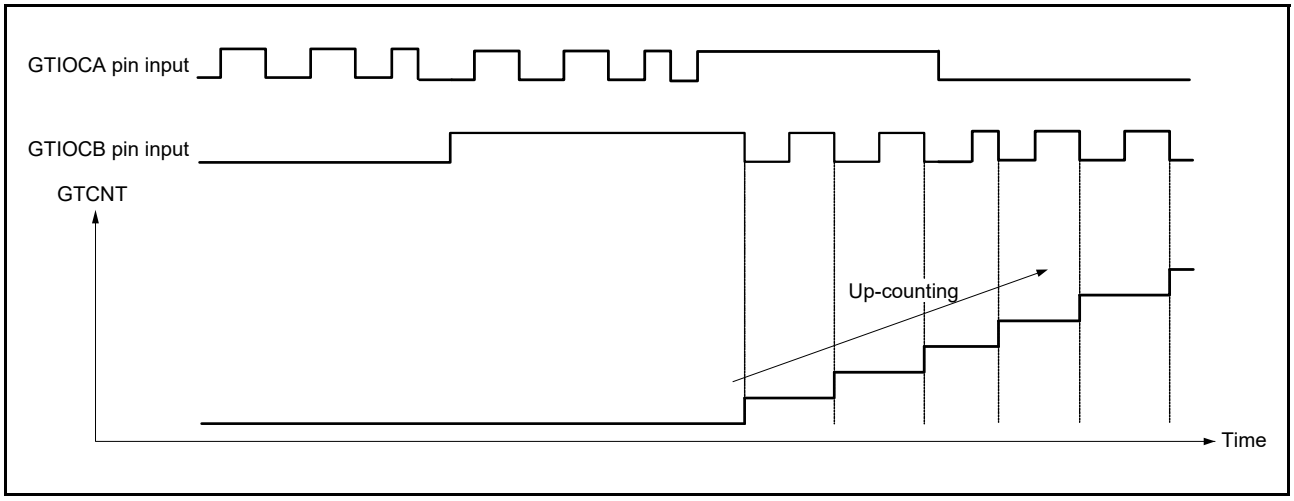


Figure 20.76 Example of phase counting mode 5 (B)

Table 20.16 Conditions of up-counting/down-counting in phase counting mode 5 (B)

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
High	↑	Don't care	GTUPSR = 0000C000h GTDNSR = 00000000h
Low	↓	Up-counting	
↑	Low	Don't care	
↓	High		
High	↓	Up-counting	
Low	↑	Don't care	
↑	High		
↓	Low		

↑ : Rising edge

↓ : Falling edge

20.3.11 Output Phase Switching (GPT_OPS)

GPT_OPS provides a function for easy control of brushless DC motor operation using the Output Phase Switching Control Register (OPSCR).

GPT_OPS outputs a PWM signal to be used for chopper control or level signal for each phase (U-positive phase/negative phase, V-positive phase/negative phase, W-positive phase/negative phase) of the 6-phase motor control. This function uses a soft setting value (OPSCR.UF, VF, WF) set by software or external signals detected by the Hall element, a PWM waveform of GPT16H1.GTIOCA.

Figure 20.77 shows the GPT_OPS control flow conceptual diagram.

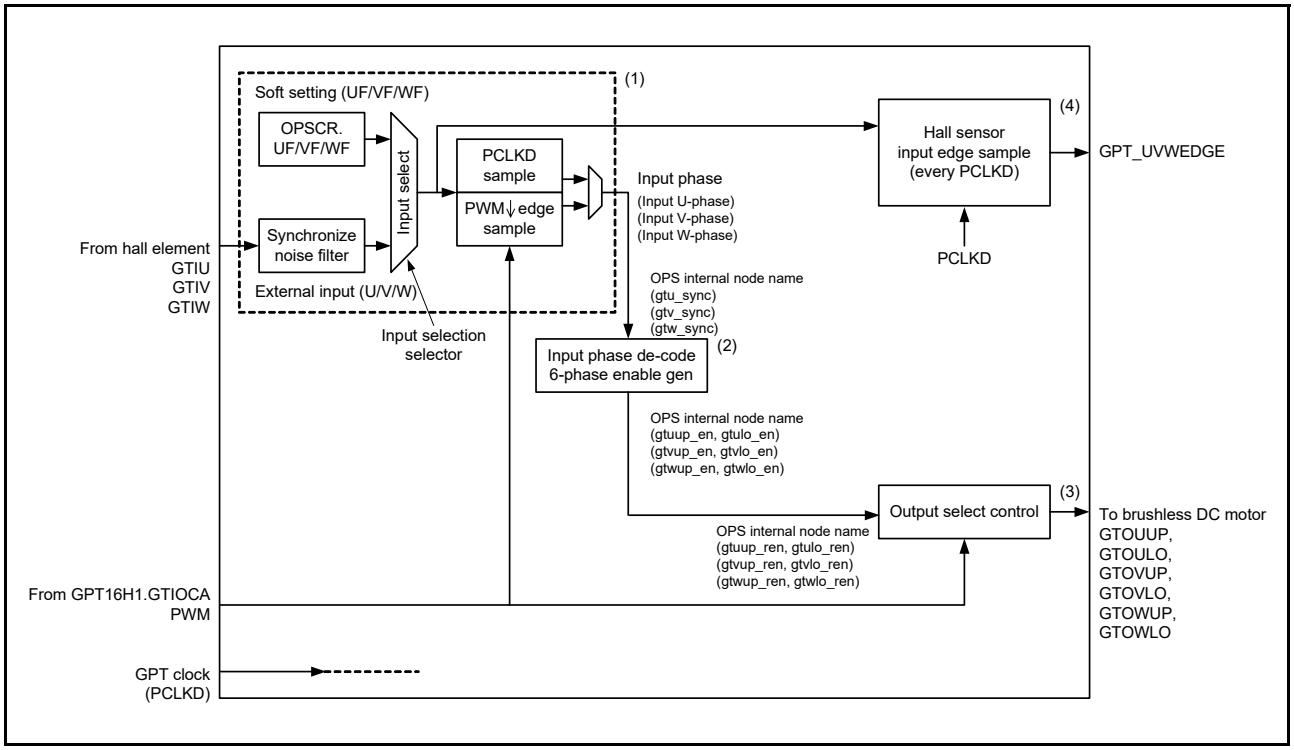


Figure 20.77 GPT_OPS control flow conceptual diagram

Figure 20.78 shows a 6-phase level signals output example of a GPT_OPS operation.

The GPT_UVWEDGE signal in Figure 20.78 is the hall sensor input edge that outputs to the ELC.

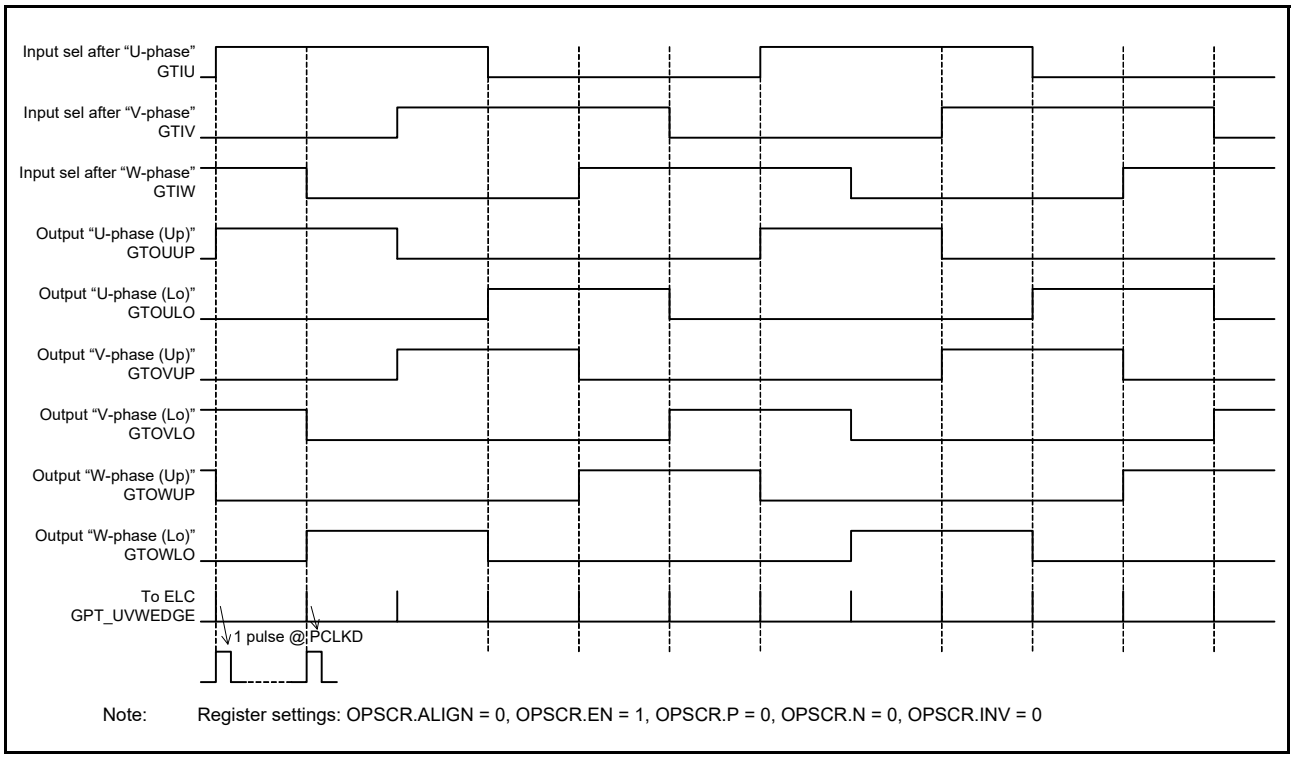


Figure 20.78 6-phase level output operation example

Figure 20.79 shows a 6-phase PWM output example of a GPT_OPS operation with chopper control.

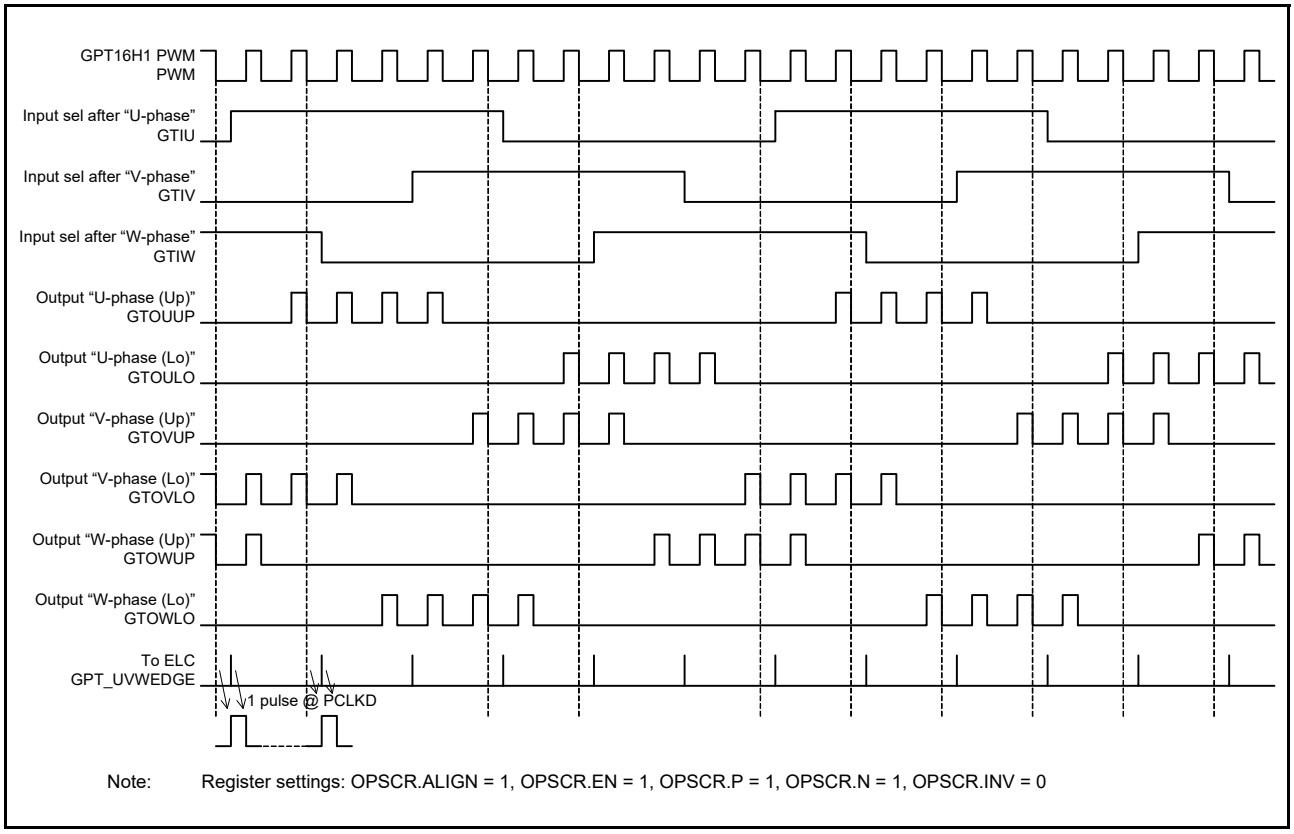


Figure 20.79 6-phase PWM output operation example with chopper control

Figure 20.80 shows an example of output disable control (6-phase PWM output operation).

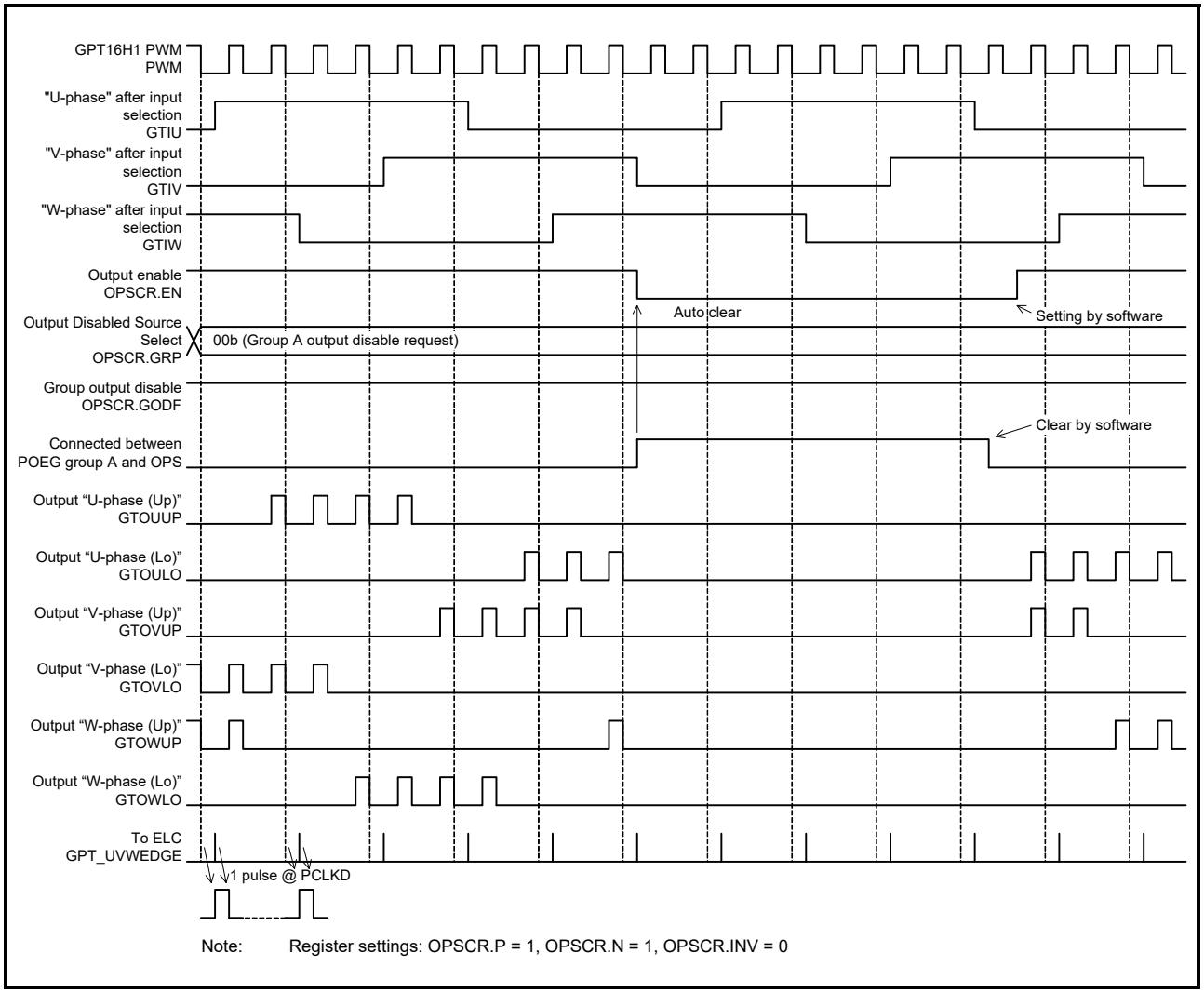


Figure 20.80 Group output disable control operation example

20.3.11.1 Input Selection and Synchronization of External Input Signal

In the GPT_OPS control flow conceptual diagram shown in Figure 20.77, (1) is a selection of input phase from the software settings and external input by the OPSCR.FB bit.

When OPSCR.FB bit is 0, select the external input. Enable the input signal after synchronization with the GPT clock (PCLKD). After carrying out noise filtering (optional), set the external input to the input phase of PWM (PWM of GPT16H1.GTIOCA) using falling edge sampling with OPSCR.ALIGN bit set to 1.

When OPSCR.FB bit is 1, select the soft setting (OPSCR.UF, VF, WF) with the value of the input phase of PWM (PWM of GPT16H1.GTIOCA) using falling edge sampling with OPSCR.ALIGN bit set to 1.

When OPSCR.ALIGN bit is 0, GPT_OPS operates with the input phase of PCLKD synchronization with either OPSCR.FB bit set to 0 or OPSCR.FB bit set to 1. However, there are cases where the PWM pulse width of the output U/V/W phases (PWM output mode) of switch timing (just before/just after) is shortened.

Table 20.17 shows the input selection process and setting of the associated OPSCR bits.

Table 20.17 Input selection processing method

Register OPSCR		Selection of input phase sampling method (U/V/W-phase)	Synchronization input/output selection process (GPT_OPS internal node name)
FB bit	ALIGN bit		
0	1	External Input at PWM Falling Edge Sampling (PCLKD Sync + Falling Edge Sample)	Input Phase Input U-Phase (gtu_sync) Input V-Phase (gtv_sync) Input W-Phase (gtw_sync)
	0	External Input at PCLKD Synchronization Output (PCLKD Sync + Through mode)	
1	1	Software Settings at PWM Falling Edge Sampling (OPSCR.UF, VF, WF of Falling Edge Sample)	
	0	Software Setting Value Selection (= OPSCR.UF/VF/WF value) (= PCLKD Synchronization)	

20.3.11.2 Input sampling

The OPSCR.U, V, W bits indicate the PCLKD, and the sampling results of the input selected by the OPSCR.FB bit.

When OPSCR.FB bit is 0 and after synchronization with the GPT clock (PCLKD) and noise filtering (optional), OPSCR.U, V, W bits have the sampling results of the external input.

When OPSCR.FB bit is 1, OPSCR.U, V, W register is the value (OPSCR.UF, VF, WF) of the soft setting.

20.3.11.3 Input phase decode

In the GPT_OPS control flow conceptual diagram shown in Figure 20.77, (2) enables the 6-phase signals by decoding the input phase selected by the OPSCR.FB bit. The 6-phase enable signal is used for internal processing of GPT_OPS.

Table 20.18 shows the decode table of input phase.

Table 20.18 Decode table of input phase

Input phase (U/V/W) (GPT_OPS internal node name)			6-phase enable {U/V/W (Up/Lo)} by decoding input phase (GPT_OPS internal node name)					
Input U-phase	Input V-phase	Input W-phase	U-phase (Up)	U-phase (Lo)	V-phase (Up)	V-phase (Lo)	W-phase (Up)	W-phase (Lo)
(gtu_sync)	(gtv_sync)	(gtw_sync)	(gtuup_en)	(gtulo_en)	(gtvup_en)	(gtvlo_en)	(gtwup_en)	(gtwlo_en)
1	0	1	1	0	0	1	0	0
1	0	0	1	0	0	0	0	1
1	1	0	0	0	1	0	0	1
0	1	0	0	1	1	0	0	0
0	1	1	0	1	0	0	1	0
0	0	1	0	0	0	1	1	0
0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0

20.3.11.4 Output selection control

In the GPT_OPS control flow conceptual diagram in Figure 20.77, (3) presents the selection of the output waveform by setting the OPSCR register bit.

For output selection, the following bits are relevant:

- The OPSCR.EN bit controls whether to output the 6-phase output, or to stop
- The OPSCR.P bit and OPSCR.N bit can choose from the level signal or PWM signal (chopper output) for the output phase
- The polarity of the output phase can be set to a positive logic or negative logic by the OPSCR. INV bit.

Table 20.19 and Table 20.20 show the output selection control method using the OPSCR register bit.

Table 20.19 Output selection control method (positive phase)

Enable-phase output control	Positive-phase output (P) control	Invert-phase output control	Output port name (positive phase = up) (output selection internal node allocation)	
Register OPSCR.EN	**Register OPSCR.P**	**Register OPSCR.INV**	**GTOUUP GTOVUP GTOWUP**	**Mode**
0	x	x	0	Output Stop (External pin: Hi-Z) GPT_OPS → 0 output
1	0	0	Level signal (gtuup_en) (gtvup_en) (gtwup_en)	Level Output Mode (Positive phase) (Positive logic)
1	0	1	Level signal (~gtuup_en) (~gtvup_en) (~gtwup_en)	Level Output Mode (Positive phase) (Negative logic)
1	1	0	PWM signal (PWM & gtuup_en) (PWM & gtvup_en) (PWM & gtwup_en)	PWM Output Mode (Positive phase) (Positive logic)
1	1	1	PWM signal (~(PWM & gtuup_en)) (~(PWM & gtvup_en)) (~(PWM & gtwup_en))	PWM Output Mode (Positive phase) (Negative logic)

Table 20.20 Output selection control method (negative phase)

Enable-phase output control	Negative-phase output (N) control	Invert-phase output control	Output port name (negative phase = Lo) (output selection internal node allocation)	
Register OPSCR.EN	**Register OPSCR.N**	**Register OPSCR.INV**	**GTOULO GTOVLO GTOWLO**	**Mode**
0	x	x	0	Output Stop (External pin: Hi-Z) GPT_OPS → 0 output
1	0	0	Level signal (gtulo_en) (gtvlo_en) (gtwlo_en)	Level Output Mode (Negative phase) (Positive logic)
1	0	1	Level signal (~gtulo_en) (~gtvlo_en) (~gtwlo_en)	Level Output Mode (Negative phase) (Negative logic)
1	1	0	PWM signal (PWM & gtulo_en) (PWM & gtvlo_en) (PWM & gtwlo_en)	PWM Output Mode (Negative phase) (Positive logic)
1	1	1	PWM signal (~(PWM & gtulo_en)) (~(PWM & gtvlo_en)) (~(PWM & gtwlo_en))	PWM Output Mode (Negative phase) (Negative logic)

20.3.11.5 Output selection control (group output disable function)

When OPSCR.GODF is 1 and the signal value selected by the OPSCR.GRP bit is high (output disable request), the GPT_OPS output pins change to Hi-Z asynchronously and the OPSCR.EN bit is cleared to 0 by the output-disable request signal synchronized with PCLKD.

For the return, after clearing the output-disable request by software, set the OPSCR.EN to 1.

The timing of the OPSCR.EN bit cleared to 0 is 3 PCLKD cycles after generating the output-disable request. To perform output disable control reliably, allow at least 4 PCLKD cycles after generating the output-disable request (by clearing the output-disable request flag in POEG) until the output-disable request is terminated.

For an example of the operation of group output-disable control, see Figure 20.80.

20.3.11.6 Event Link Controller (ELC) output

In the GPT_OPS control flow conceptual diagram shown in Figure 20.77, (4) outputs the hall sensor input signal edge to the event link controller.

The hall sensor input edge signal is the logical OR of the rising and falling edge signals of each U-phase/V-phase/W-phase input sampled at PCLKD. That is, if the high period of each of the U-phase/V-phase/W-phase input is short in duration, the hall sensor edge input signal is not output at that time.

When the OPSCR.FB bit is 0, the hall sensor input edge signal is the logical OR of the edge signals of the external input phase sampled at PCLKD.

When OPSCR.FB bit is 1, the hall sensor input edge signal is the logical OR of the edge of the soft setting (OPSCR.UF, VF, WF) sampled at PCLKD.

See Figure 20.78 to Figure 20.80 for examples of the output signal to the ELC.

20.3.11.7 GPT_OPS start operation setting flow

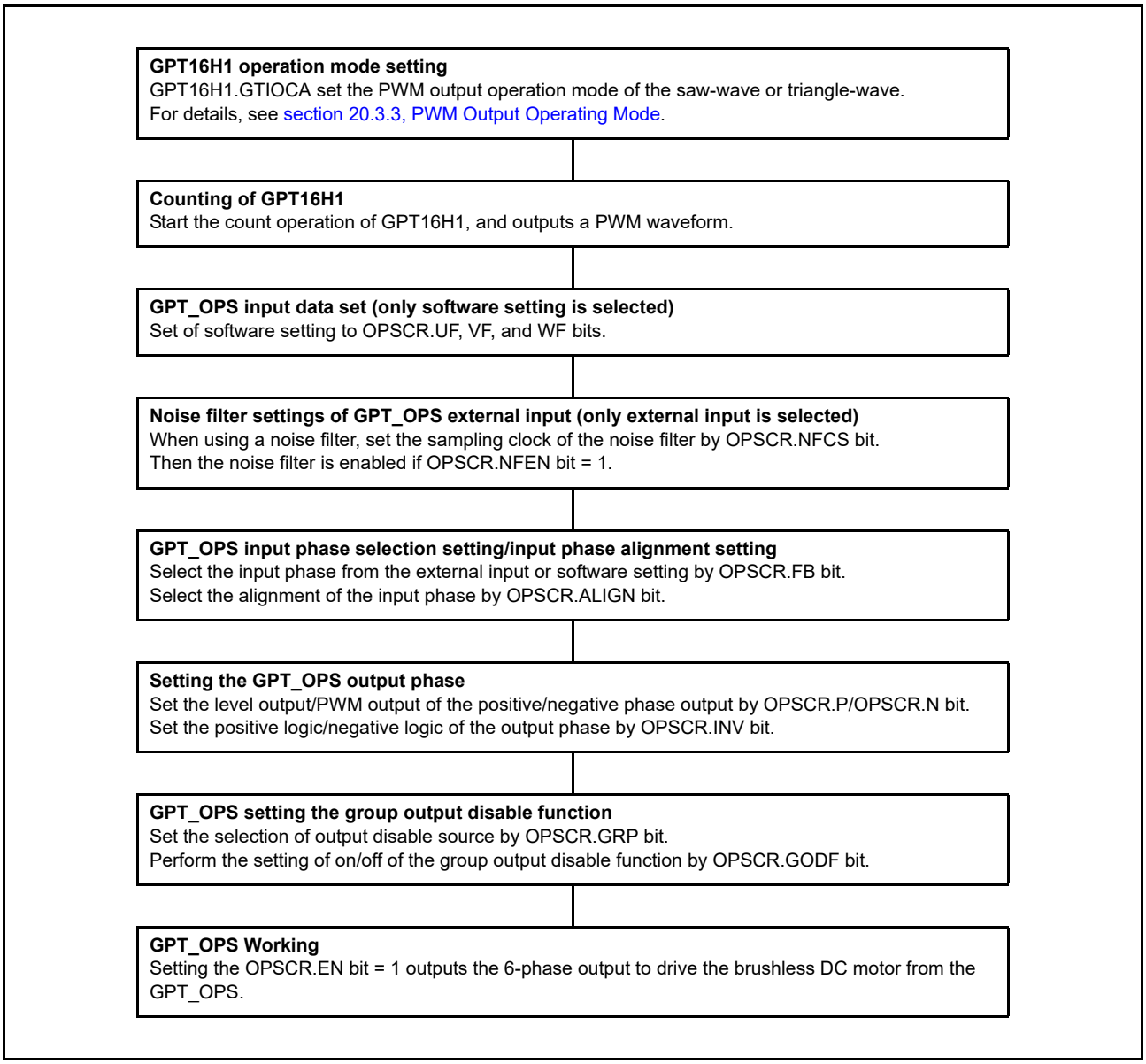


Figure 20.81 Example for setting of GPT_OPS start operation

20.4 Interrupt Sources

20.4.1 Interrupt Sources

The GPT provides the following interrupt sources:

- GTCCR input capture/compare match
- GTCNT counter overflow (GTPR compare match)/underflow.

Each interrupt source has its own status flag. When an interrupt source signal is generated, the corresponding status flag in GTST is set to 1. The corresponding status flag in GTST can be cleared by writing 0. If flag set and flag clear occur at the same time, flag clear takes priority over flag set. Those flags are automatically updated by internal state.

Table 20.21 lists the GPT interrupt sources.

Table 20.21 Interrupt sources

Channel	Name	Interrupt Source	Interrupt Flag	DTC Activation
0	GPT0_CCMPA	GPT320.GTCCRA input capture/compare match	TCFA	Possible
	GPT0_CCMPB	GPT320.GTCCRB input capture/compare match	TCFB	Possible
	GPT0_CMPC	GPT320.GTCCRC compare match	TCFC	Possible
	GPT0_CMPD	GPT320.GTCCRD compare match	TCFD	Possible
	GPT0_OVF	GPT320.GTCNT overflow (GPT320.GTPR compare match)	TCFPO	Possible
	GPT0_UDF	GPT320.GTCNT underflow	TCFPU	Possible
1	GPT1_CCMPA	GPT16H1.GTCCRA input capture/compare match	TCFA	Possible
	GPT1_CCMPB	GPT16H1.GTCCRB input capture/compare match	TCFB	Possible
	GPT1_CMPC	GPT16H1.GTCCRC compare match	TCFC	Possible
	GPT1_CMPD	GPT16H1.GTCCRD compare match	TCFD	Possible
	GPT1_OVF	GPT16H1.GTCNT overflow (GPT16H1.GTPR compare match)	TCFPO	Possible
	GPT1_UDF	GPT16H1.GTCNT underflow	TCFPU	Possible
2	GPT2_CCMPA	GPT16H2.GTCCRA input capture/compare match	TCFA	Possible
	GPT2_CCMPB	GPT16H2.GTCCRB input capture/compare match	TCFB	Possible
	GPT2_CMPC	GPT16H2.GTCCRC compare match	TCFC	Possible
	GPT2_CMPD	GPT16H2.GTCCRD compare match	TCFD	Possible
	GPT2_OVF	GPT16H2.GTCNT overflow (GPT16H2.GTPR compare match)	TCFPO	Possible
	GPT2_UDF	GPT16H2.GTCNT underflow	TCFPU	Possible
3	GPT3_CCMPA	GPT16H3.GTCCRA input capture/compare match	TCFA	Possible
	GPT3_CCMPB	GPT16H3.GTCCRB input capture/compare match	TCFB	Possible
	GPT3_CMPC	GPT16H3.GTCCRC compare match	TCFC	Possible
	GPT3_CMPD	GPT16H3.GTCCRD compare match	TCFD	Possible
	GPT3_OVF	GPT16H3.GTCNT overflow (GPT16H3.GTPR compare match)	TCFPO	Possible
	GPT3_UDF	GPT16H3.GTCNT underflow	TCFPU	Possible
4	GPT4_CCMPA	GPT164.GTCCRA input capture/compare match	TCFA	Possible
	GPT4_CCMPB	GPT164.GTCCRB input capture/compare match	TCFB	Possible
	GPT4_CMPC	GPT164.GTCCRC compare match	TCFC	Possible
	GPT4_CMPD	GPT164.GTCCRD compare match	TCFD	Possible
	GPT4_OVF	GPT164.GTCNT overflow (GPT164.GTPR compare match)	TCFPO	Possible
	GPT4_UDF	GPT164.GTCNT underflow	TCFPU	Possible
5	GPT5_CCMPA	GPT165.GTCCRA input capture/compare match	TCFA	Possible
	GPT5_CCMPB	GPT165.GTCCRB input capture/compare match	TCFB	Possible
	GPT5_CMPC	GPT165.GTCCRC compare match	TCFC	Possible
	GPT5_CMPD	GPT165.GTCCRD compare match	TCFD	Possible
	GPT5_OVF	GPT165.GTCNT overflow (GPT165.GTPR compare match)	TCFPO	Possible
	GPT5_UDF	GPT165.GTCNT underflow	TCFPU	Possible
6	GPT6_CCMPA	GPT166.GTCCRA input capture/compare match	TCFA	Possible
	GPT6_CCMPB	GPT166.GTCCRB input capture/compare match	TCFB	Possible
	GPT6_CMPC	GPT166.GTCCRC compare match	TCFC	Possible
	GPT6_CMPD	GPT166.GTCCRD compare match	TCFD	Possible
	GPT6_OVF	GPT166.GTCNT overflow (GPT166.GTPR compare match)	TCFPO	Possible
	GPT6_UDF	GPT166.GTCNT underflow	TCFPU	Possible

(1) GPTn_CCMPA interrupt (n = 0 to 6)

An interrupt request is generated under the following conditions:

- When the GTCCRA register functions as a compare match register, the GTCNT counter value matches with the GTCCRA register.
- When the GTCCRA register functions as an input capture register, the input-capture signal caused transfer of the GTCNT counter value to the GTCCRA register.

(2) GPTn_CCMPB interrupt (n = 0 to 6)

An interrupt request is generated under the following conditions:

- When the GTCCRB register functions as a compare match register, the GTCNT counter value matches with the GTCCRB register.
- When the GTCCRB register functions as an input capture register, the input-capture signal caused transfer of the GTCNT counter value to the GTCCRB register.

(3) GPTn_CMPC interrupt (n = 0 to 6)

An interrupt request is generated under the following condition:

- When the GTCCRC register functions as a compare match register, the GTCNT counter value matches with the GTCCRC register.

A compare match is not performed and therefore, an interrupt is not requested in the following conditions:

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 01b, 10b, 11b (buffer operation with the GTCCRC register).

(4) GPTn_CMPD interrupt (n = 0 to 6)

An interrupt request is generated under the following condition:

- When the GTCCRD register functions as a compare match register, the GTCNT counter value matches with the GTCCRD register.

A compare match is not performed and therefore, an interrupt is not requested in the following conditions:

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 10b, 11b (buffer operation with the GTCCRD register).

(5) GPTn_OVF interrupt (n = 0 to 6)

An interrupt request is generated in the following conditions:

- In saw-wave mode, interrupt requests are enabled at overflows (when the GTCNT counter value changes from GTPR to 0 during up-counting)
- In triangle-wave mode, interrupt requests are enabled at crests (the GTCNT changes from GTPR to GTPR-1).
- In counting by hardware sources, an overflow (GTCNT changes from GTPR to 0 in up count) has occurred.

(6) GPTn_UDF interrupt (n = 0 to 6)

An interrupt request is generated in the following conditions.

- In saw-wave mode, interrupt requests are enabled at underflows (when the GTCNT counter value changes from 0 to GTPR during down-counting).
- In triangle-wave mode, interrupt requests are enabled at troughs (the GTCNT changes from 0 to 1).
- In counting by hardware sources, underflow (GTCNT changes from 0 to GTPR in down count) has occurred.

Table 20.22 Interrupt signals and interrupt status flags

Interrupt signal	Interrupt status flag
GPTn_UDF	GTST[7] (TCFPU)
GPTn_OVF	GTST[6] (TCFPO)
GPTn_CMPD	GTST[3] (TCFD)
GPTn_CMPC	GTST[2] (TCFC)
GPTn_CCMPB	GTST[1] (TCFB)
GPTn_CCMPA	GTST[0] (TCFA)

n = 0 to 6

20.4.2 DTC Activation

The DTC can be activated by the interrupt in each channel. For details, see section 12, Interrupt Controller Unit (ICU), and section 15, Data Transfer Controller (DTC).

20.5 Operations Linked by ELC

20.5.1 Event Signal Output to ELC

GPT is capable of operation linked with another module set in advance when its interrupt request signal is used as an event signal by the Event Link Controller (ELC).

The GPT has the following ELC event signals:

- Generating of compare match A interrupt (GPTn_CCMPA)
- Generating of compare match B interrupt (GPTn_CCMPB)
- Generating of compare match C interrupt (GPTn_CMPC)
- Generating of compare match D interrupt (GPTn_CMPD)
- Generating of overflow interrupt (GPTn_OVF)
- Generating of underflow interrupt (GPTn_UDF).

Note: n = 0 to 6

20.5.2 Event Signal Inputs from the ELC

The GPT can perform the following operations in response to a maximum of four events from the event link controller (ELC).

- Start counting, stop counting, clear counting
- Up-counting, down counting
- Input capture.

See section 20.3, Operation for detail on hardware resources.

20.6 Noise Filter Function

Each pin for use in input capture and hall sensor input to the GPT is equipped with a noise filter. The noise filter samples input signals at the sampling clock and removes the pulses whose length is less than three sampling cycles.

The noise filter functionality includes enabling and disabling the noise filter for each pin and setting of the sampling clock for each channel.

Figure 20.82 shows the timing of noise filtering.

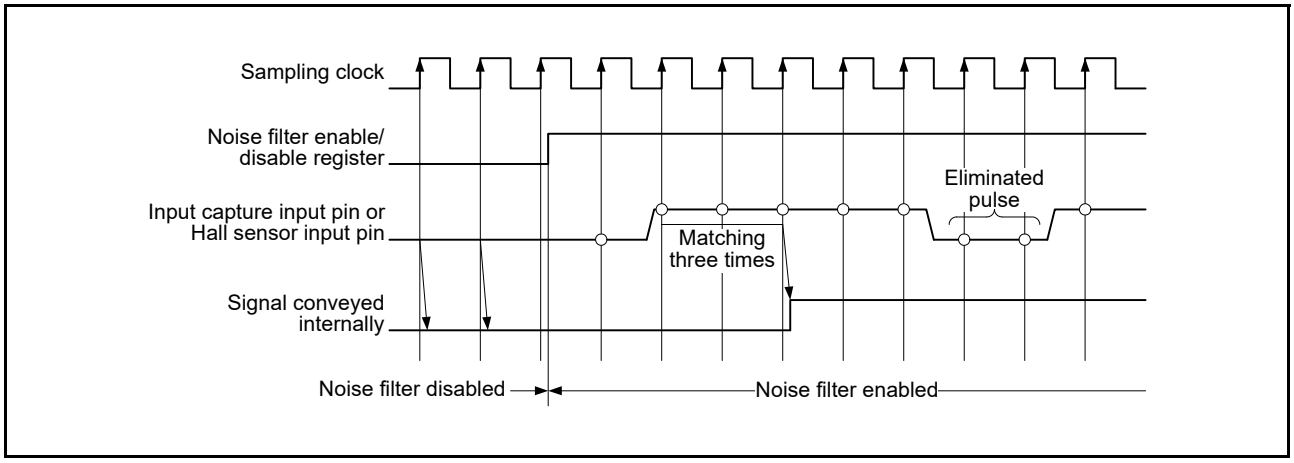


Figure 20.82 Timing of noise filtering

If noise filtering is enabled, the input capture operation or hall sensor input operation is performed on the edges of the noise filtered signal after a delay of a minimum sampling interval × 2 + PCLKD. This is due to the noise filtering for the input capture input or hall sensor input operation.

20.7 Protection Function

20.7.1 Write-Protection for Registers

To prevent registers from being accidentally modified, registers can be write-protected in channel units by setting GTWP.WP. Write-protection can be set for the following registers:

GTSSR, GTPSR, GTCSR, GTUPSR, GTDNSR, GTICASR, GTICBSR, GTCR, GTUDDTYC, GTIOR, GTINTAD, GTST, GTBER, GTCNT, GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, GTCCRF, GTPR, GTPBR, GTDTCR, GTDVU.

20.7.2 Disabling of Buffer Operation

If the timing of the buffer register write is delayed relative to timing for the buffer transfer, buffer operation can be suspended with the GTBER.BD setting. Specifically, buffer transfer can be temporarily disabled, even though a buffer transfer condition is generated during buffer register write, by setting the corresponding GTBER.BD bit to 1 (buffer operation disabled) before buffer register write and clearing the bit to 0 (buffer operation enabled) after completion of writing to all the buffer registers.

Figure 20.83 shows an example of operation for disabling buffer operation.

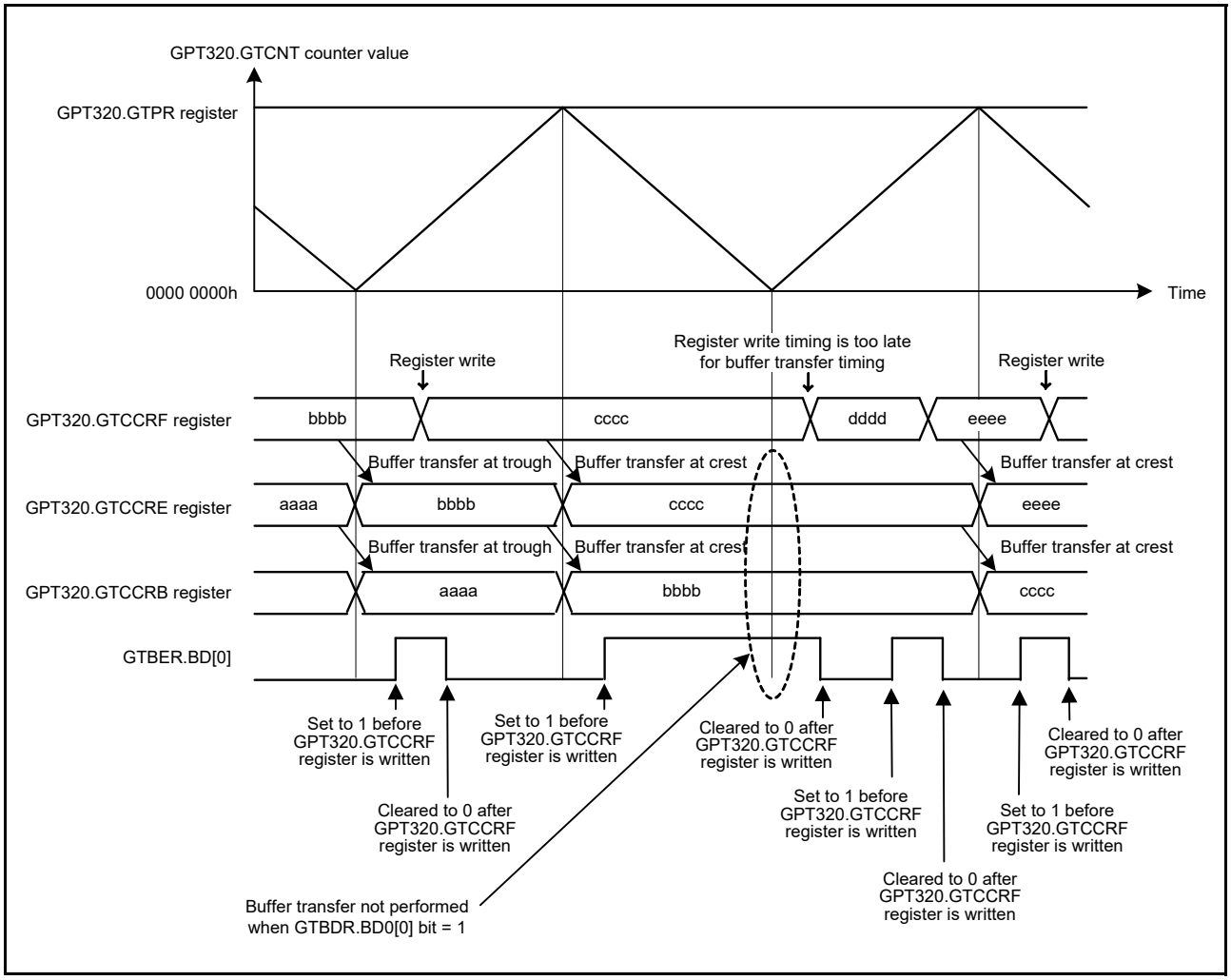


Figure 20.83 Example of operation for disabling buffer operation with triangle waves, double buffer operation, and buffer transfer at both troughs and crests

20.7.3 GTIOC Pin Output Negate Control

For protection from system failure, the output disable control that changes the GTIOC pin output value forcibly is provided for GTIOC pin output by the request of output disable from POEG. When the GTIOCA pin output value is the same as the GTIOCB pin output value, output protection is required. GPT detects such a case and generates output disable requests to POEG according to the setting of output disable request permission bits, such as GTINTAD.GRPABH, GTINTAD.GRPABL. After the POEG receives output disable requests from each channel and calculates external input using an OR operation, the POEG generates output disable requests to GPT.

One output disable signal (representing the common output disable request signal of the GTIOCA pin and the GTIOCB pin) out of two output disable requests generated by the POEG is selected by setting GTINTAD.GRP[1:0]. The status of the selected disable output request is monitored by reading the GTST.ODF bit. The output level during output disable is set in accordance with GTIOR.OADF[1:0] bits for GTIOCA pin and GTIOR.OBDF[1:0] bits for GTIOCB pin.

The change to the output disable state is performed asynchronously by generating the output disable request from the POEG. The release of the output disable state is performed at end of cycle by terminating the output disable request. The timing of release of the output disable state is a minimum of 3 PCLKD cycles after terminating the output disable request. In order to perform output disable control reliably, allow at least 4 PCLKD cycles after generating the output disable request (by clearing the output disable request flag in POEG) until the output disable request is terminated.

When event count is performed or when the output disable state should be released immediately without waiting for end of cycle, GTIOR.OADF[1:0] should be set to 00b (for GTIOCA pin) or GTIOR.OBDF[1:0] should be set to 00b (for GTIOCB pin).

Figure 20.84 shows an example of the GTIOC pin output disable control operation.

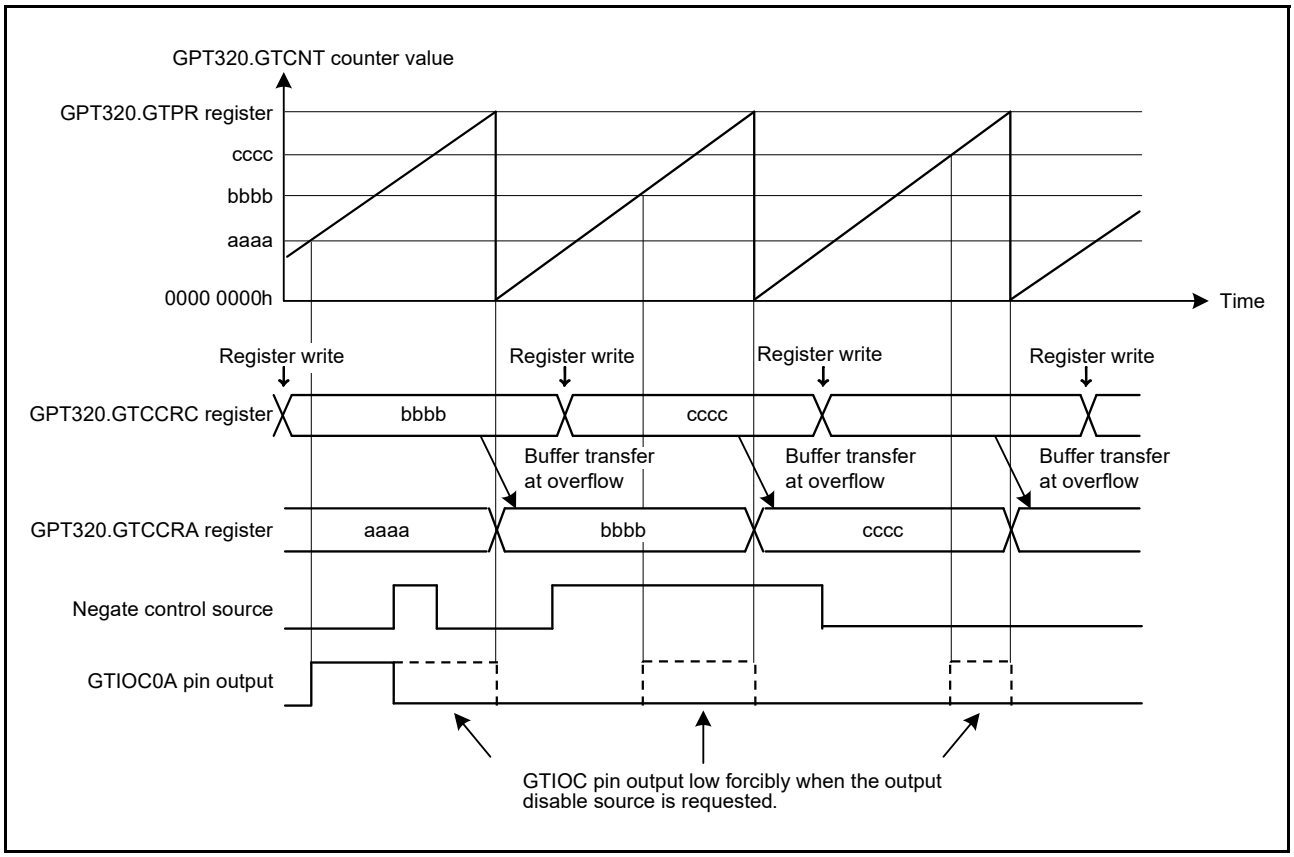


Figure 20.84 Example of GTIOC pin output disable control operation in saw-wave up-counting, buffer operation, active level 1, high output at GTCCRA compare match, low output at cycle end, and low output at output disable

20.8 Initialization Method of Output Pins

20.8.1 Pin Settings after Reset

The GPT registers are initialized at a reset. Start counting after selecting the port pin function with the PmnPFS register, setting GTIOR.OAE and GTIOR.OBE bits, and outputting the GPT function to external pins.

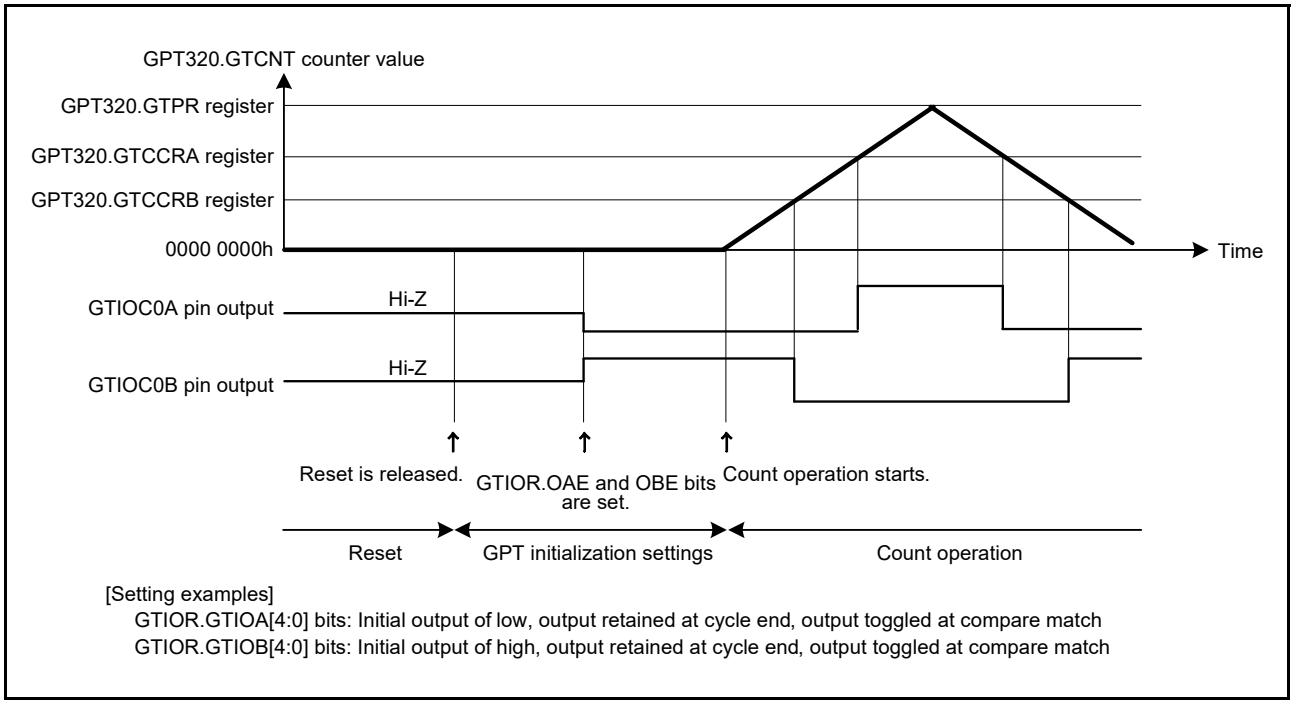


Figure 20.85 Example of pin settings after reset

20.8.2 Pin Initialization Due to Error during Operation

If an error occurs during GPT operation, the following four types of pin processing can be performed before pin initialization:

- Set OAHLD and OBHLD bits in GTIOR to 1 and retain the outputs at count stop
- Set OAHLD and OBHLD bits in GTIOR to 0, specify arbitrary output values at OADFLT and OBDFLT in GTIOR, and output the arbitrary values at count stop
- Set the pin to output an arbitrary value as a general output port by setting the PDR, PODR, and PmnPFS registers of the I/O port in advance. Set the OAE and OBE bits in GTIOR to 0 and the control bit in PmnPFS.PMR that corresponds to the pin to 0 to allow arbitrary values to be output from the pin set as a general output port when an error occurs.
- Drive the output to a high impedance state using the POEG function.

After the automatic dead time setting is made, clear the GTDTCR.TDE bit to 0 after counting stops. When counting stops, only the values of registers that are changed by a GPT external source change. If counting is resumed, operation continues from where it stopped. If counting is stopped, the registers must be initialized before counting starts.

20.9 Usage Notes

20.9.1 Settings for the Module-Stop State

The Module Stop Control Register can enable or disable GPT operation. The GPT is initially stopped after a reset. The registers become accessible on release from the module-stop state. For details, see section 10, Low Power Modes.

20.9.2 Settings of GTCCRn during Compare Match Operation (n = A to F)

(1) When automatic dead time setting is made in triangle-wave PWM mode

The GTCCRA register must satisfy both of the following conditions:

- GTDVU < GTCCRA
- 0 < GTCCRA < GTPR.

(2) When automatic dead time setting is not made in triangle-wave PWM mode

The GTCCRA register must be set within the range of 0 < GTCCRA < GTPR. If GTCCRA = 0 or GTCCRA = GTPR is set, a compare match occurs within the cycle only when GTCCRA is 0 or GTCCRA = GTPR is satisfied. When GTCCRA > GTPR, no compare match occurs.

Similarly, GTCCRB must be set within the range of 0 < GTCCRB < GTPR. If GTCCRB = 0 or GTCCRB = GTPR is set, a compare match occurs within the cycle only when GTCCRB is 0 or GTCCRB = GTPR is satisfied. When GTCCRB > GTPR, no compare match occurs.

(3) When automatic dead time setting is made in saw-wave one-shot pulse mode

The GTCCRC and GTCCRD registers must be set to satisfy the following restrictions. If the restrictions are not satisfied, the correct output waveforms with secured dead time may not be obtained.

- In up-counting — GTCCRC < GTCCRD, GTCCRC > GTDVU, GTCCRD < GTPR - GTDVU
- In down-counting — GTCCRC > GTCCRD, GTCCRC < GTPR - GTDVU, GTCCRD > GTDVU.

(4) When automatic dead time setting is not made in saw-wave one-shot pulse mode

The GTCCRC and GTCCRD registers must be set to satisfy the following restrictions. If the restrictions are not satisfied, two compare matches do not occur and pulse output cannot be performed.

- In up-counting: 0 < GTCCRC < GTCCRD < GTPR
- In down-counting: GTPR > GTCCRC > GTCCRD > 0.

Similarly, GTCCRE and GTCCRF must be set to satisfy the following restrictions. If the restrictions are not satisfied, two compare matches do not occur and pulse output cannot be performed.

- In up-counting: 0 < GTCCRE < GTCCRF < GTPR
- In down-counting: GTPR > GTCCRE > GTCCRF > 0.

(5) In saw-wave PWM mode

The GTCCRA register should be set with the range of 0 < GTCCRA < GTPR. If GTCCRA = 0 or GTCCRA = GTPR is set, a compare match occurs within the cycle only when GTCCRA = 0 or GTCCRA = GTPR is satisfied. If GTCCRA > GTPR is set, no compare match occurs.

Similarly, GTCCRB should be set with the range of 0 < GTCCRB < GTPR. If GTCCRB = 0 or GTCCRB = GTPR is set, a compare match occurs within the cycle only when GTCCRB = 0 or GTCCRB = GTPR is satisfied. If GTCCRB > GTPR is set, no compare match occurs.

20.9.3 Setting the Range for GTCNT Counter

The GTCNT counter register should be set with the range of 0 ≤ GTCNT ≤ GTPR.

20.9.4 GTCNT Counter Start/Stop

The control timing of starting and stopping the GTCNT counter by the GTCR.CST bit synchronizes the count clock that is selected in GTCR.TPCS[2:0]. When GTCR.CST is updated, the GTCNT counter starts/stops after a count clock that is selected in GTCR.TPCS[2:0]. Therefore, an event generated before the GTCNT counter actually starts is ignored, resulting in cases where an event is accepted or an interrupt occurs after GTCR.CST is set to 0.

20.9.5 Priority Order of Each Event

(1) GTCNT register

Table 20.23 shows a priority order of events updating the GTCNT register.

Table 20.23 Priority order of sources updating GTCNT

Source of updating GTCNT	Priority Order
Writing by CPU (writing to GTCNT/GTCLR)	High
Clear by hardware sources set in GTCSR	↑
Count up or down by hardware sources set in GTUPSR/GTDNSR	
Count operation	Low

If up-counting and down-counting by hardware sources occur at the same time, the GTCNT counter value does not change.

When there is a conflict between updating the GTCNT register and reading by the CPU, pre-update data is read.

(2) GTCR.CST bit

When there is a conflict between starting/stopping by hardware sources set in the GTSSR/GTPSR registers and writing by the CPU (writing to GTCR/GTSTR/GTSTP registers), the writing by CPU has a priority over the starting/stopping by hardware sources.

When there is a conflict between starting by hardware sources set in the GTSSR register and stopping by hardware sources set in GTPSR register, the GTCR.CST bit value does not change.

If there is a conflict between updating the GTCR.CST bit and reading by the CPU, pre-update data is read.

(3) GTCCRn registers (n = A to F)

When there is a conflict between input capture/buffer transfer operation and writing to the GTCCRn registers, the writing to GTCCRn registers has a priority over input capture/buffer transfer operation. When there is a conflict between input capture and writing to the counter register by the CPU or updating the counter register by hardware sources, the pre-update counter value is captured.

If there is a conflict between updating the GTCCRn registers and reading by the CPU, pre-update data is read.

(4) GTPR registers

When there is a conflict between buffer transfer operation and the writing to the GTPR register, the writing to GTPR register has a priority over buffer transfer operation.

If there is a conflict between updating GTPR register and reading by the CPU, pre-update data is read.

21. PWM Delay Generation Circuit

21.1 Overview

The MCU has three channel delay circuits that can connect to the General PWM Timer (GPT).

Table 21.1 lists the specifications for the PWM delay generation circuit, Figure 21.1 shows a block diagram, and Table 21.2 lists the I/O pins.

Table 21.1 PWM delay generation circuit specifications

Parameter	Description
Function	The PWM delay generation circuit can control the timing with which signals on the two PWM output pins for channel 1/2/3 rise and fall to an accuracy of up to 1/32 times the period of the GPT clock (PCLKD)

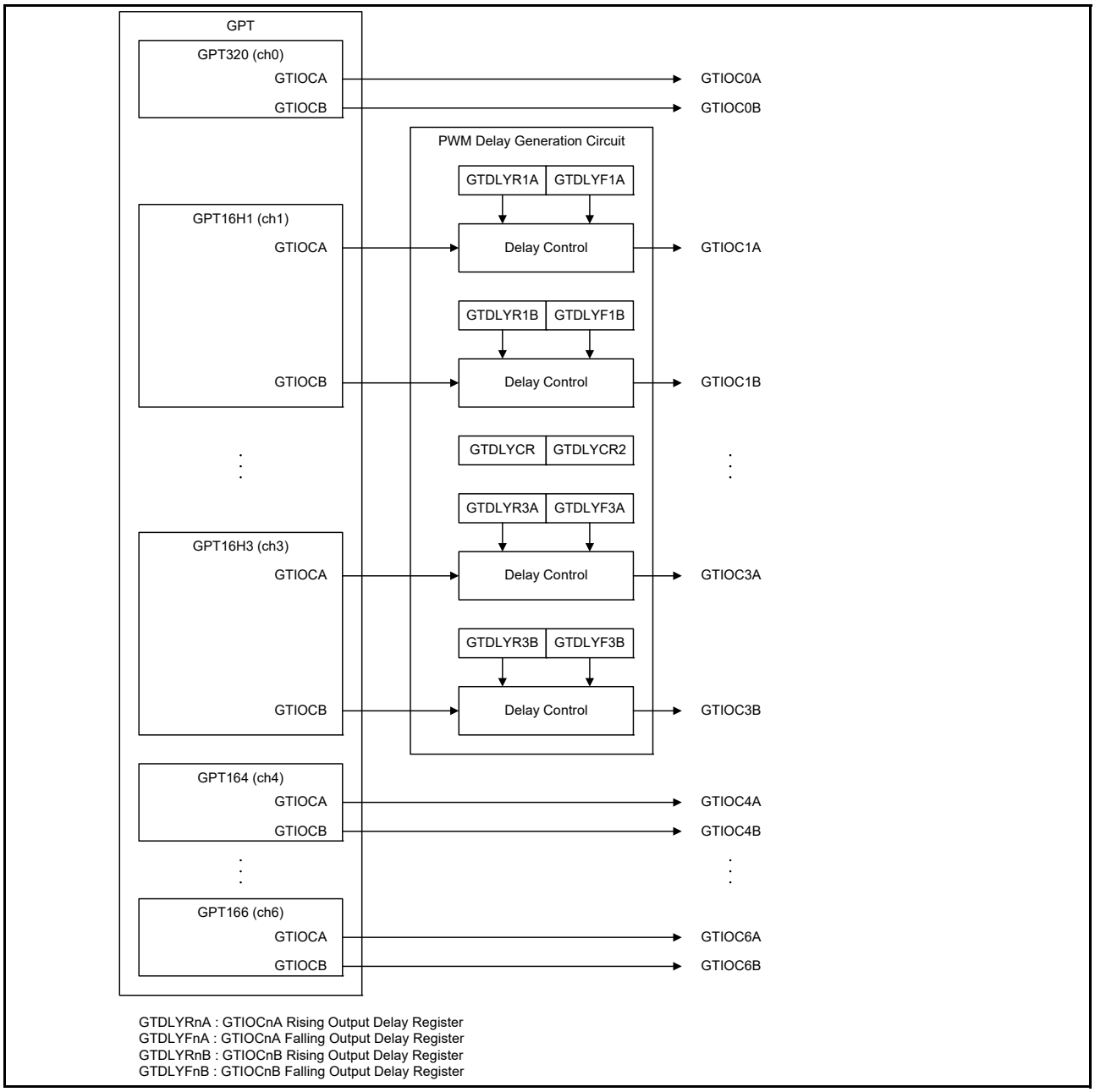


Figure 21.1 PWM delay generation circuit block diagram

Table 21.2 I/O pins of PWM delay generation circuit

I/O pin	I/O	Function
GTIOC1A	Output	Delayed output of GTIOCA pin of GPT channel 1
GTIOC1B	Output	Delayed output of GTIOCB pin of GPT channel 1
GTIOC2A	Output	Delayed output of GTIOCA pin of GPT channel 2
GTIOC2B	Output	Delayed output of GTIOCB pin of GPT channel 2
GTIOC3A	Output	Delayed output of GTIOCA pin of GPT channel 3
GTIOC3B	Output	Delayed output of GTIOCB pin of GPT channel 3

21.2 Register Descriptions

21.2.1 PWM Output Delay Control Register (GTDLYCR)

Address(es): GPT_ODC.GTDLYCR 4007 B000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DLLMOD	—	—	—	—	—	—	DLYRST	DLLEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DLLEN	DLL Operation Enable	0: Disable DLL operation 1: Enable DLL operation.	R/W
b1	DLYRST	PWM Delay Generation Circuit Reset	0: Normal operation 1: Reset.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	DLLMOD	DLL Mode Select	0: 5 bit-mode 1: 4 bit-mode.	R/W
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

GTDLYCR controls the PWM delay generation circuit, which applies delays to the PWM outputs. GTDLYCR register can be written when register write protection is disabled (GPT16H1.GTWP.WP = 0).

DLLEN bit (DLL Operation Enable)

The DLLEN bit selects whether the on-chip DLL in the PWM delay generation circuit is activated or not.

DLYRST bit (PWM Delay Generation Circuit Reset)

The DLYRST bit resets the internal state of the PWM delay generation circuit.

DLLMOD bit (DLL Mode Select)

The DLLMOD bit selects the DLL resolution. When the DLLEN bit is 1, setting this bit is prohibited.

21.2.2 PWM Output Delay Control Register 2 (GTDLYCR2)

Address(es): GPT_ODC.GTDLYCR2 4007 B002h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DLYD ENB3	DLYD ENB2	DLYD ENB1	—	DLYEN 3	DLYEN 2	DLYEN 1	—	—	—	—	—	DLYBS 3	DLYBS 2	DLYBS 1	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b1	DLYBS1	PWM Delay Generation Circuit Bypass for Channel 1	0: Bypass delay generation circuit of channel 1 1: Do not bypass delay generation circuit of channel 1.	R/W
b2	DLYBS2	PWM Delay Generation Circuit Bypass for Channel 2	0: Bypass delay generation circuit of channel 2 1: Do not bypass delay generation circuit of channel 2.	R/W
b3	DLYBS3	PWM Delay Generation Circuit Bypass for Channel 3	0: Bypass delay generation circuit of channel 3 1: Do not bypass delay generation circuit of channel 3.	R/W
b8 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9	DLYEN1	PWM Delay Generation Circuit Enable for Channel 1	0: Enable delay generation circuit of channel 1 1: Disable delay generation circuit of channel 1.	R/W
b10	DLYEN2	PWM Delay Generation Circuit Enable for Channel 2	0: Enable delay generation circuit of channel 2 1: Disable delay generation circuit of channel 2.	R/W
b11	DLYEN3	PWM Delay Generation Circuit Enable for Channel 3	0: Enable delay generation circuit of channel 3 1: Disable delay generation circuit of channel 3.	R/W
b12	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b13	DLYD ENB1	PWM Delay Generation Circuit Disable for GTIOC1B	0: Delay generation circuit of GTIOC1B is based on b9. 1: Disable delay generation circuit of GTIOC1B.	R/W
b14	DLYD ENB2	PWM Delay Generation Circuit Disable for GTIOC2B	0: Delay generation circuit of GTIOC2B is based on b10. 1: Disable delay generation circuit of GTIOC2B.	R/W
b15	DLYD ENB3	PWM Delay Generation Circuit Disable for GTIOC3B	0: Delay generation circuit of GTIOC3B is based on b11. 1: Disable delay generation circuit of GTIOC3B.	R/W

GTDLYCR2 controls each channel of PWM delay generation circuit. The GTDLYCR2 register is writable when register write protection is disabled (GPT16H1.GTWP.WP = 0).

DLYBSn (n = 1 to 3) bits (PWM Delay Generation Circuit Bypass for Channel n)

The DLYBSn bits select whether delays are applied to PWM output signals from the GTIOCnA and GTIOCnB pins (n = 1 to 3) by the PWM delay generation circuit or whether the circuit is bypassed.

A signal delayed in the PWM delay generation circuit is output 3 cycles of GPT operation clock (PCLKD) later than if it bypassed the PWM delay generation circuit.

DLYENn (n = 1 to 3) bits (PWM Delay Generation Circuit Enable for Channel n)

The DLYENn bits select whether the channel n (n = 1 to 3) of PWM delay generation circuit is powered on or off. If the channel n of the PWM delay generation circuit is not used, set to 1.

DLYDENBn (n = 1 to 3) bits (PWM Delay Generation Circuit Disable for GTIOCnB)

The DLYDENBn bits select whether the GTIOCnB pins (n = 1 to 3) of PWM delay generation circuit is powered off. If the GTIOCnB (n = 1 to 3) of PWM delay generation circuit is not used, set to 1.

21.2.3 GTIOCnA Rising Output Delay Register (GTDLYRnA) (n = 1 to 3)

Address(es): GPT_ODC.GTDLYR1A 4007 B01Ch, GPT_ODC.GTDLYR2A 4007 B020h, GPT_ODC.GTDLYR3A 4007 B024h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	DLY[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	DLY[4:0]	GTIOCnA Output Rising Edge Delay Setting	b4 b0 0 0 0 0 0: No delay on rising edges 0 0 0 0 1: Delay of 1/32 times the PCLKD period is applied 0 0 0 1 0: Delay of 2/32 times the PCLKD period is applied 0 0 0 1 1: Delay of 3/32 times the PCLKD period is applied 0 0 1 0 0: Delay of 4/32 times the PCLKD period is applied 0 0 1 0 1: Delay of 5/32 times the PCLKD period is applied 0 0 1 1 0: Delay of 6/32 times the PCLKD period is applied 0 0 1 1 1: Delay of 7/32 times the PCLKD period is applied 0 1 0 0 0: Delay of 8/32 times the PCLKD period is applied 0 1 0 0 1: Delay of 9/32 times the PCLKD period is applied 0 1 0 1 0: Delay of 10/32 times the PCLKD period is applied 0 1 0 1 1: Delay of 11/32 times the PCLKD period is applied 0 1 1 0 0: Delay of 12/32 times the PCLKD period is applied 0 1 1 0 1: Delay of 13/32 times the PCLKD period is applied 0 1 1 1 0: Delay of 14/32 times the PCLKD period is applied 0 1 1 1 1: Delay of 15/32 times the PCLKD period is applied 1 0 0 0 0: Delay of 16/32 times the PCLKD period is applied 1 0 0 0 1: Delay of 17/32 times the PCLKD period is applied 1 0 0 1 0: Delay of 18/32 times the PCLKD period is applied 1 0 0 1 1: Delay of 19/32 times the PCLKD period is applied 1 0 1 0 0: Delay of 20/32 times the PCLKD period is applied 1 0 1 0 1: Delay of 21/32 times the PCLKD period is applied 1 0 1 1 0: Delay of 22/32 times the PCLKD period is applied 1 0 1 1 1: Delay of 23/32 times the PCLKD period is applied 1 1 0 0 0: Delay of 24/32 times the PCLKD period is applied 1 1 0 0 1: Delay of 25/32 times the PCLKD period is applied 1 1 0 1 0: Delay of 26/32 times the PCLKD period is applied 1 1 0 1 1: Delay of 27/32 times the PCLKD period is applied 1 1 1 0 0: Delay of 28/32 times the PCLKD period is applied 1 1 1 0 1: Delay of 29/32 times the PCLKD period is applied 1 1 1 1 0: Delay of 30/32 times the PCLKD period is applied 1 1 1 1 1: Delay of 31/32 times the PCLKD period is applied.	R/W
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

GTDLYRnA register sets a delay to be applied to rising edges of output signals on the GTIOCnA pin. For information about the timing for the transfer of settings, see section 21.3.2, Timing for Transfer of GTDLYRnA, GTLDYRnB, GTDLYFnA, and GTDLYFnB Register Settings.

The GTDLYRnA register is writable when register write protection is disabled (GPT16Hn.GTWP.WP = 0).

When GPT_ODC.GTDLYCR.DLLMOD is 1 (4-bit mode), the bit[0] value in this register is ignored and regarded as 0.

21.2.4 GTIOCnA Falling Output Delay Register (GTDLYFnA) (n = 1 to 3)

Address(es): GPT_ODC.GTDLYF1A 4007 B02Ch, GPT_ODC.GTDLYF2A 4007 B030h, GPT_ODC.GTDLYF3A 4007 B034h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	DLY[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	DLY[4:0]	GTIOCnA Output Falling Edge Delay Setting	b4 b0 0 0 0 0 0: No delay on falling edges 0 0 0 0 1: Delay of 1/32 times the PCLKD period is applied. 0 0 0 1 0: Delay of 2/32 times the PCLKD period is applied. 0 0 0 1 1: Delay of 3/32 times the PCLKD period is applied. 0 0 1 0 0: Delay of 4/32 times the PCLKD period is applied. 0 0 1 0 1: Delay of 5/32 times the PCLKD period is applied. 0 0 1 1 0: Delay of 6/32 times the PCLKD period is applied. 0 0 1 1 1: Delay of 7/32 times the PCLKD period is applied. 0 1 0 0 0: Delay of 8/32 times the PCLKD period is applied. 0 1 0 0 1: Delay of 9/32 times the PCLKD period is applied. 0 1 0 1 0: Delay of 10/32 times the PCLKD period is applied. 0 1 0 1 1: Delay of 11/32 times the PCLKD period is applied. 0 1 1 0 0: Delay of 12/32 times the PCLKD period is applied. 0 1 1 0 1: Delay of 13/32 times the PCLKD period is applied. 0 1 1 1 0: Delay of 14/32 times the PCLKD period is applied. 0 1 1 1 1: Delay of 15/32 times the PCLKD period is applied. 1 0 0 0 0: Delay of 16/32 times the PCLKD period is applied. 1 0 0 0 1: Delay of 17/32 times the PCLKD period is applied. 1 0 0 1 0: Delay of 18/32 times the PCLKD period is applied. 1 0 0 1 1: Delay of 19/32 times the PCLKD period is applied. 1 0 1 0 0: Delay of 20/32 times the PCLKD period is applied. 1 0 1 0 1: Delay of 21/32 times the PCLKD period is applied. 1 0 1 1 0: Delay of 22/32 times the PCLKD period is applied. 1 0 1 1 1: Delay of 23/32 times the PCLKD period is applied. 1 1 0 0 0: Delay of 24/32 times the PCLKD period is applied. 1 1 0 0 1: Delay of 25/32 times the PCLKD period is applied. 1 1 0 1 0: Delay of 26/32 times the PCLKD period is applied. 1 1 0 1 1: Delay of 27/32 times the PCLKD period is applied. 1 1 1 0 0: Delay of 28/32 times the PCLKD period is applied. 1 1 1 0 1: Delay of 29/32 times the PCLKD period is applied. 1 1 1 1 0: Delay of 30/32 times the PCLKD period is applied. 1 1 1 1 1: Delay of 31/32 times the PCLKD period is applied.	R/W
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTDLYFnA register sets a delay to be applied to falling edges of output signals on the GTIOCnA pin. For information about the timing for the transfer of settings, see section 21.3.2, Timing for Transfer of GTDLYRnA, GTLDYRnB, GTDLYFnA, and GTDLYFnB Register Settings. GTDLYFnA is writable when register write protection is disabled (GPT16Hn.GTWP.WP = 0).

When GPT_ODC.GTDLYCR.DLLMOD is 1 (4-bit mode), the bit[0] value in this register is ignored and regarded as 0.

21.2.5 GTIOCnB Rising Output Delay Register (GTDLYRnB) (n = 1 to 3)

Address(es): GPT_ODC.GTDLYR1B 4007 B01Eh, GPT_ODC.GTDLYR2B 4007 B022h, GPT_ODC.GTDLYR3B 4007 B026h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	DLY[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	DLY[4:0]	GTIOCnB Output Rising Edge Delay Setting	b4 b0 0 0 0 0 0: No delay on rising edges 0 0 0 0 1: Delay of 1/32 times the PCLKD period is applied 0 0 0 1 0: Delay of 2/32 times the PCLKD period is applied 0 0 0 1 1: Delay of 3/32 times the PCLKD period is applied 0 0 1 0 0: Delay of 4/32 times the PCLKD period is applied 0 0 1 0 1: Delay of 5/32 times the PCLKD period is applied 0 0 1 1 0: Delay of 6/32 times the PCLKD period is applied 0 0 1 1 1: Delay of 7/32 times the PCLKD period is applied 0 1 0 0 0: Delay of 8/32 times the PCLKD period is applied 0 1 0 0 1: Delay of 9/32 times the PCLKD period is applied 0 1 0 1 0: Delay of 10/32 times the PCLKD period is applied 0 1 0 1 1: Delay of 11/32 times the PCLKD period is applied 0 1 1 0 0: Delay of 12/32 times the PCLKD period is applied 0 1 1 0 1: Delay of 13/32 times the PCLKD period is applied 0 1 1 1 0: Delay of 14/32 times the PCLKD period is applied 0 1 1 1 1: Delay of 15/32 times the PCLKD period is applied 1 0 0 0 0: Delay of 16/32 times the PCLKD period is applied 1 0 0 0 1: Delay of 17/32 times the PCLKD period is applied 1 0 0 1 0: Delay of 18/32 times the PCLKD period is applied 1 0 0 1 1: Delay of 19/32 times the PCLKD period is applied 1 0 1 0 0: Delay of 20/32 times the PCLKD period is applied 1 0 1 0 1: Delay of 21/32 times the PCLKD period is applied 1 0 1 1 0: Delay of 22/32 times the PCLKD period is applied 1 0 1 1 1: Delay of 23/32 times the PCLKD period is applied 1 1 0 0 0: Delay of 24/32 times the PCLKD period is applied 1 1 0 0 1: Delay of 25/32 times the PCLKD period is applied 1 1 0 1 0: Delay of 26/32 times the PCLKD period is applied 1 1 0 1 1: Delay of 27/32 times the PCLKD period is applied 1 1 1 0 0: Delay of 28/32 times the PCLKD period is applied 1 1 1 0 1: Delay of 29/32 times the PCLKD period is applied 1 1 1 1 0: Delay of 30/32 times the PCLKD period is applied 1 1 1 1 1: Delay of 31/32 times the PCLKD period is applied.	R/W
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTDLYRnB register sets a delay to be applied to rising edges of output signals on the GTIOCnB pin. For information about the timing for the transfer of settings, see section 21.3.2, Timing for Transfer of GTDLYRnA, GTLDYRnB, GTDLYFnA, and GTDLYFnB Register Settings. GTDLYRnB is writable when register write protection is disabled (GPT16Hn.GTWP.WP = 0).

When GPT_ODC.GTDLYCR.DLLMOD is 1 (4-bit mode), the bit[0] value in this register is ignored and regarded as 0.

21.2.6 GTIOCnB Falling Output Delay Register (GTDLYFnB) (n = 1 to 3)

Address(es): GPT_ODC.GTDLYF1B 4007 B02Eh, GPT_ODC.GTDLYF2B 4007 B032h, GPT_ODC.GTDLYF3B 4007 B036h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	DLY[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	DLY[4:0]	GTIOCnB Output Falling Edge Delay Setting	b4 b0 0 0 0 0 0: No delay on falling edges 0 0 0 0 1: Delay of 1/32 times the PCLKD period is applied 0 0 0 1 0: Delay of 2/32 times the PCLKD period is applied 0 0 0 1 1: Delay of 3/32 times the PCLKD period is applied 0 0 1 0 0: Delay of 4/32 times the PCLKD period is applied 0 0 1 0 1: Delay of 5/32 times the PCLKD period is applied 0 0 1 1 0: Delay of 6/32 times the PCLKD period is applied 0 0 1 1 1: Delay of 7/32 times the PCLKD period is applied 0 1 0 0 0: Delay of 8/32 times the PCLKD period is applied 0 1 0 0 1: Delay of 9/32 times the PCLKD period is applied 0 1 0 1 0: Delay of 10/32 times the PCLKD period is applied 0 1 0 1 1: Delay of 11/32 times the PCLKD period is applied 0 1 1 0 0: Delay of 12/32 times the PCLKD period is applied 0 1 1 0 1: Delay of 13/32 times the PCLKD period is applied 0 1 1 1 0: Delay of 14/32 times the PCLKD period is applied 0 1 1 1 1: Delay of 15/32 times the PCLKD period is applied 1 0 0 0 0: Delay of 16/32 times the PCLKD period is applied 1 0 0 0 1: Delay of 17/32 times the PCLKD period is applied 1 0 0 1 0: Delay of 18/32 times the PCLKD period is applied 1 0 0 1 1: Delay of 19/32 times the PCLKD period is applied 1 0 1 0 0: Delay of 20/32 times the PCLKD period is applied 1 0 1 0 1: Delay of 21/32 times the PCLKD period is applied 1 0 1 1 0: Delay of 22/32 times the PCLKD period is applied 1 0 1 1 1: Delay of 23/32 times the PCLKD period is applied 1 1 0 0 0: Delay of 24/32 times the PCLKD period is applied 1 1 0 0 1: Delay of 25/32 times the PCLKD period is applied 1 1 0 1 0: Delay of 26/32 times the PCLKD period is applied 1 1 0 1 1: Delay of 27/32 times the PCLKD period is applied 1 1 1 0 0: Delay of 28/32 times the PCLKD period is applied 1 1 1 0 1: Delay of 29/32 times the PCLKD period is applied 1 1 1 1 0: Delay of 30/32 times the PCLKD period is applied 1 1 1 1 1: Delay of 31/32 times the PCLKD period is applied.	R/W
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTDLYFnB register sets a delay to be applied to falling edges of output signals on the GTIOCnB pin. For information about the timing for the transfer of settings, see section 21.3.2, Timing for Transfer of GTDLYRnA, GTLDYRnB, GTDLYFnA, and GTDLYFnB Register Settings. GTDLYFnB is writable when register write protection is disabled (GPT16Hn.GTWP.WP = 0).

When GPT_ODC.GTDLYCR.DLLMOD is 1 (4-bit mode), the bit[0] value in this register is ignored and regarded as 0.

21.3 Operation

21.3.1 Adjustments to the Timing of Rising and Falling Edges in PWM Waveforms

The timing of rising and falling edges in PWM waveforms which are output from the GTIOCnA and GTIOCnB pins, where n = channel number, can be delayed to an accuracy of 1/32 of the GPT operating clock (PCLKD) period.

If the timing of rising or falling edges in PWM waveforms output from the GTIOCnA and GTIOCnB pins must be adjusted, make the initial settings for the PWM generation circuit as shown in the procedure in Figure 21.2.

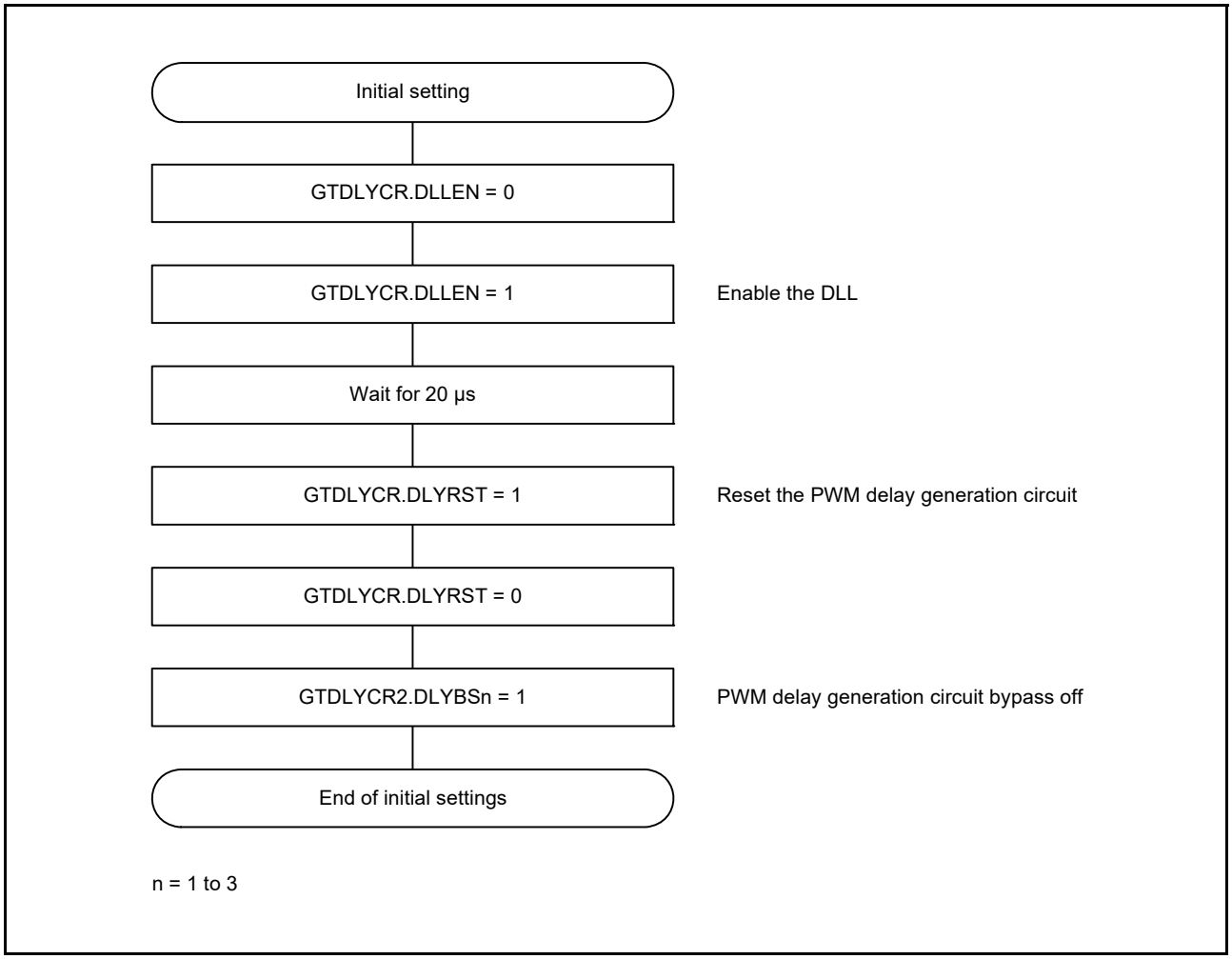


Figure 21.2 Example initialization flow for the PWM delay generation circuit

In the PWM delay generation circuit, delay can be applied to rising and falling edges of the PWM output to an accuracy of 1/32 of the period of the GPT operation clock (PCLKD). This is described in section 20.3.3, PWM Output Operating Mode. Delays associated with the settings are reflected in the PWM output with the timing described in section 21.3.2, Timing for Transfer of GTDLYRnA, GTLDYRnB, GTDLYFnA, and GTDLYFnB Register Settings. Table 21.3 shows the association between the GTDLYRnA, GTLDYRnB, GTDLYFnA, and GTDLYFnB registers and the PWM outputs.

Table 21.3 Association between PWM output pins and delay setting registers

PWM output pin	Rising-edge delay setting register	Falling-edge delay setting register
GTIOC1A	GTDLYR1A	GTDLYF1A
GTIOC1B	GTDLYR1B	GTDLYF1B
GTIOC2A	GTDLYR2A	GTDLYF2A
GTIOC2B	GTDLYR2B	GTDLYF2B
GTIOC3A	GTDLYR3A	GTDLYF3A
GTIOC3B	GTDLYR3B	GTDLYF3B

When the PWM delay generation circuit is in use, the timing with which a PWM output signal rises and falls can be controlled to an accuracy of 1/32 of the period of the GPT operation clock (PCLKD). When this facility is not in use, the period of the PWM output waveform is controlled to an accuracy of one period of the input clock for the timer counter PCLKD. With the PWM delay generation circuit, the output can be controlled to an accuracy 32 times better. Additionally, the delay settings also control the periods at high and low levels for the PWM waveform to the given accuracy. PWM delay generation circuit channels can be individually enabled or disabled.

21.3.2 Timing for Transfer of GTDLYRnA, GTLDYRnB, GTDLYFnA, and GTDLYFnB Register Settings

Settings for the GTDLYRnA, GTLDYRnB, GTDLYFnA, and GTDLYFnB registers are initially transferred to temporary registers and then reflected in the number of delays on the GTIOCnA and GTIOCnB (n = 1 to 3) outputs. Transfer of the settings takes place on overflows (in up-counting) or underflows (in down-counting) for saw waves and in the troughs of triangle waves.

Figure 21.3 and Figure 21.4 show examples of operation of the GTDLYR1A and GTDLYF1A registers.

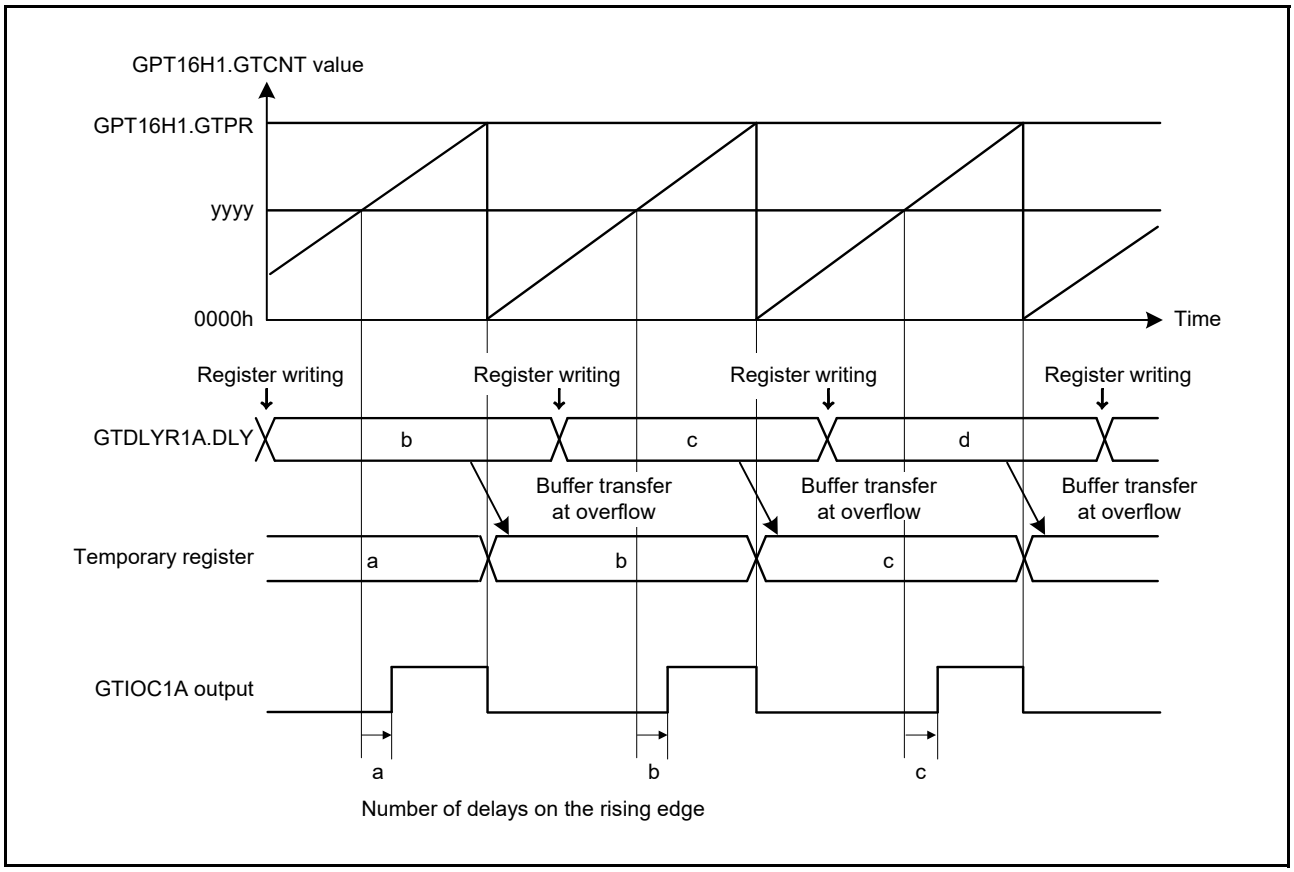


Figure 21.3 Example of GTDLYR1A register operation in PWM saw-wave generation

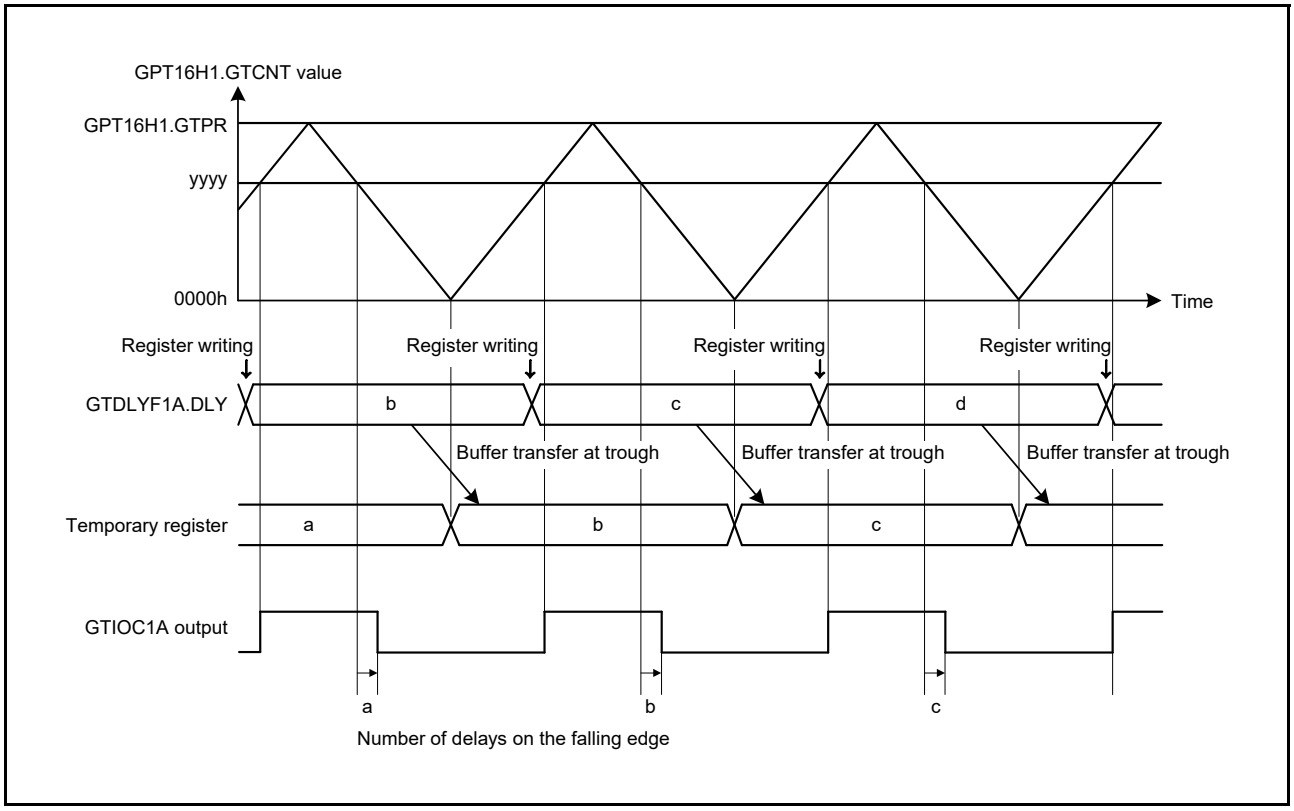


Figure 21.4 Example of GTDLYF1A register operation in PWM triangle-wave generation

21.4 Usage Notes

21.4.1 Module Stop Function Setting

The Module Stop Control Register can disable or enable operation of the PWM delay generation circuit. The PWM delay generation circuit is initially stopped after a reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

21.4.2 Notes on Delay Settings for PWM Delay Generation Circuit

When the PWM delay generation circuit generates delays for a PWM output waveform and the waveform is toggled in response to compare-matches, do not change the settings for delay while the compare-match value is within the ranges listed in Table 21.4. This constraint applies to the GTDLYFnA, GTDLYRnA, GTDLFnB, and GTDLYRnB registers.

Table 21.4 Constraint on delay settings

Mode	Direction of counting	Compare-Match value
Saw-wave mode	Up	GTPR - 2 or above
	Down	2 or below
Triangle-wave mode	Down	2 or below

Figure 21.5 shows an example of how the constraints apply to the timing of setting GTDLYFnA in saw-wave waveform one-shot pulse mode (counting up). Do not change the value set in GTDLYFnA while GTCCRD ≥ GTPR - 2.

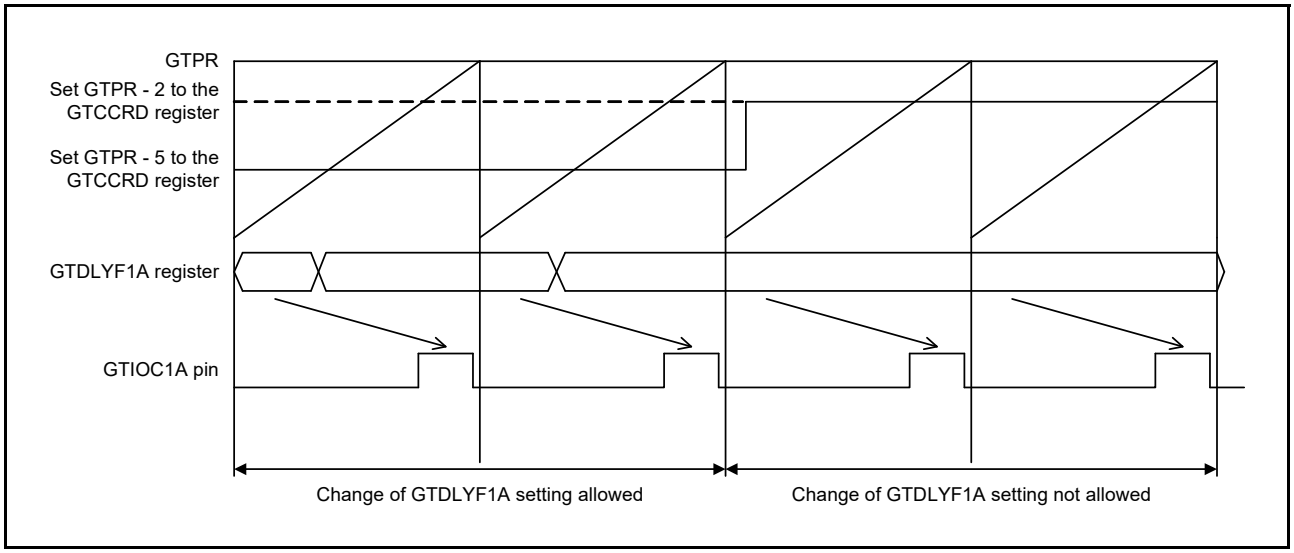


Figure 21.5 Constraint on the timing of GTDLYF1A register settings

Changing the values in the GTDLYFnA, GTDLYRnA, GTDLYFnB, and GTDLYRnB registers during periods where changes to settings are not allowed might lead to faulty output waveforms such as shifts in the timing of output waveform transitions from the expected values.

22. Low Power Asynchronous General Purpose Timer (AGT)

22.1 Overview

The Low Power Asynchronous General Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events.

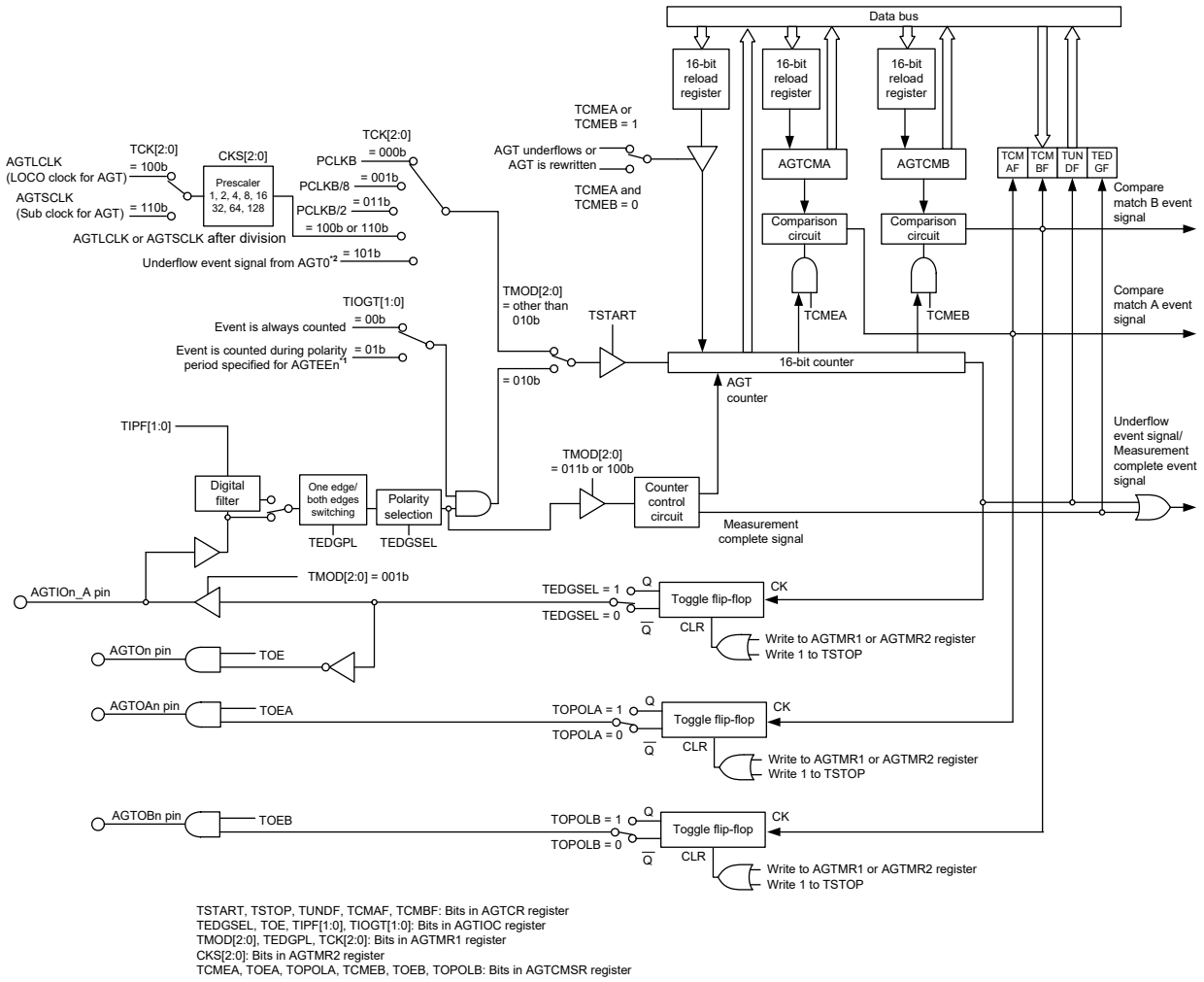
This 16-bit timer consists of a reload register and a down counter. The reload register and the down counter are allocated to the same address, and can be accessed with the AGT register.

Table 22.1 lists the AGT specifications, Figure 22.1 shows a block diagram, and Table 22.2 lists the AGT pin configuration.

Table 22.1 AGT specifications

Parameter		Description
Operating modes	Timer mode	The count source is counted
	Pulse output mode	The count source is counted and the output is inverted at each timer underflow
	Event counter mode	An external event is counted
	Pulse width measurement mode	An external pulse width is measured
	Pulse period measurement mode	An external pulse period is measured
Count source (Operating clock)*2		PCLKB, PCLKB/2, PCLKB/8, AGTLCLK/d, AGTSCLK/d, or underflow signal of AGT0*1 selectable. (d = 1, 2, 4, 8, 16, 32, 64, or 128)
Interrupt/Event link function (Output)		• Underflow event signal or measurement complete event signal – When the counter underflows – When the measurement of the active width of the external input (AGTIOn) completes in pulse width measurement mode – When the set edge of the external input (AGTIOn) is input in pulse period measurement mode. • Compare match A event signal – When the values of AGT and AGTCMA matched (Compare match A function enabled). • Compare match B event signal – When the values of AGT and AGTCMB matched (Compare match B function enabled). • Recovery from Software Standby mode can be performed by an AGT1_AGTI, AGT1_AGTCMAI, or AGT1_AGTCMBI.
Selectable functions		• Compare match function One or two of the compare match A register and compare match B register is selectable.

Note 1. AGT0 cannot use it. AGT1 connects directly with the underflow event signal from the AGT0 timer.
Note 2. Satisfy the frequency of the peripheral module clock (PCLKB) ≥ the frequency of the count source clock.



Note 1. The polarity can be selected by the EEPS bit in the AGTISR register.
Note 2. AGT0 cannot use it. AGT1 uses the underflow of AGT0.

Figure 22.1 AGT block diagram

Table 22.2 AGT I/O pins

Pin name	I/O	Function
AGTEEn	Input	External event input for AGT
AGTIOn	Input/output	External event input and pulse output for AGT
AGTOn	Output	Pulse output for AGT
AGTOAn	Output	Output compare match A output for AGT
AGTOBn	Output	Output compare match B output for AGT

Channel number (n = 0, 1)

22.2 Register Descriptions

22.2.1 AGT Counter Register (AGT)

Address(es): AGT0.AGT 4008 4000h, AGT1.AGT 4008 4100h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Description	Setting Range	R/W
b15 to b0	16-bit counter and reload register *1, *2	0000h to FFFFh	R/W

Note 1. When 1 is written to the TSTOP bit in the AGTCR register, the 16-bit counter is forcibly stopped and set to FFFFh.

Note 2. When the TCK[2:0] bit setting in the AGTMR1 register is a value other than 001b (PCLKB/8) or 011b (PCLKB/2), if the AGT register is set to 0000h, a request signal to the ICU, the DTC and the ELC is generated once immediately after the count starts. The AGTOn and AGTIOn output is toggled.
When the AGT register is set to 0000h in event counter mode, regardless of the value of TCK[2:0] bits, a request signal to the ICU, the DTC and the ELC is generated once immediately after the count starts.
In addition, the AGTOn output toggles even during a period other than the specified count period. When the AGT register is set to 0001h or more, a request signal is generated each time AGT underflows.

AGT is a 16-bit register. The write value is written to the reload register and the read value is read from the counter.

The states of the reload register and the counter change according to the TSTART bit in the AGTCR register and TCMEA/TCMEB bit in the AGTCMSR register. For details, see section 22.3.1, Reload Register and Counter Rewrite Operation. The AGT register can be set by a 16-bit memory manipulation instruction.

22.2.2 AGT Compare Match A Register (AGTCMA)

Address(es): AGT0.AGTCMA 4008 4002h, AGT1.AGTCMA 4008 4102h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Description	Setting range	R/W
b15 to b0	16-bit compare match A data is stored.*1	0000h to FFFFh	R/W

Note 1. Set the AGTCMA register to FFFFh when Compare match A is not used.

The AGTCMA register is a read/write register to set a value for compare match with the AGT counter. The states of the reload register and compare register A change according to the TSTART bit in the AGTCR register. For details, see section 22.3.2, Reload Register and Compare Register A/B Rewrite Operation. The AGTCMA register can be set by a 16-bit memory manipulation instruction.

22.2.3 AGT Compare Match B Register (AGTCMB)

Address(es): AGT0.AGTCMB 4008 4004h, AGT1.AGTCMB 4008 4104h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Description	Setting range	R/W
b15 to b0	16-bit compare match B data is stored.*1	0000h to FFFFh	R/W

Note 1. Set the AGTCMB register to FFFFh when Compare match B is not used.

The AGTCMB register is a read/write register to set a value for compare match with the AGT counter. The states of the reload register and compare register B change according to the TSTART bit in the AGTCR register. For details, see section 22.3.2, Reload Register and Compare Register A/B Rewrite Operation. The AGTCMB register can be set by a 16-bit memory manipulation instruction.

22.2.4 AGT Control Register (AGTCR)

Address(es): AGT0.AGTCR 4008 4008h, AGT1.AGTCR 4008 4108h

	b7	b6	b5	b4	b3	b2	b1	b0
	TCMBF	TCMAF	TUNDF	TEDGF	—	TSTOP	TCSTF	TSTART
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TSTART	AGT count start*2	0: Stop count 1: Start count.	R/W
b1	TCSTF	AGT count status flag*2	0: Count stopped 1: Count in progress.	R
b2	TSTOP	AGT count forced stop*1	0: Invalid (writing is invalid) 1: Force count to stop.	W
b3	—	Reserved	The read value is 0. The write value should be 0.	R/W
b4	TEDGF	Active edge judgment flag	0: No active edge received 1: Active edge received.	R/(W)*3
b5	TUNDF	Underflow flag	0: No underflow 1: Underflow.	R/(W)*3
b6	TCMAF	Compare match A flag	0: No match 1: Match.	R/(W)*3
b7	TCMBF	Compare match B flag	0: No match 1: Match.	R/(W)*3

Note 1. When 1 (count is forcibly stopped) is written to the TSTOP bit, TSTART and TCSTF bits are initialized at the same time. The pulse output level is also initialized. The read value is 0.
Note 2. For information on using the TSTART and TCSTF bits, see section 22.4.1, Count Operation Start and Stop Control.
Note 3. Only 0 can be written to clear the flag.

TSTART bit (AGT count start)

The count operation is started by writing 1 to the TSTART bit and stopped by writing 0. When the TSTART bit is set to 1 (count starts), the TCSTF bit is set to 1 (count in progress) in synchronization with the count source. Also, after 0 is written to the TSTART bit, the TCSTF bit is set to 0 (count stops) in synchronization with the count source. For details, see section 22.4.1, Count Operation Start and Stop Control.

TCSTF flag (AGT count status flag)

The TCSTF flag indicates the AGT count status.

[Setting condition]

- When 1 is written to the TSTART bit (the TCSTF bit is set to 1 in synchronization with the count source).

[Clearing conditions]

- When 0 is written to the TSTART bit (the TCSTF bit is set to 0 in synchronization with the count source)
- When 1 is written to the TSTOP bit.

TSTOP bit (AGT count forced stop)

When 1 is written to the TSTOP bit, the count is forcibly stopped. The read value is 0.

TEDGF flag (Active edge judgment flag)

The TEDGF flag indicates that an active edge was detected.

[Setting condition]

- When the measurement of the active width of the external input (AGTIOn) is complete in pulse width measurement mode
- When the set edge of the external input (AGTIOn) is input in pulse period measurement mode.

[Clearing condition]

- When 0 is written to this bit by software.

TUNDF flag (Underflow flag)

The TUNDF flag indicates that the counter underflowed.

[Setting condition]

- When the counter underflows.

[Clearing condition]

- When 0 is written to this flag by software.

TCMAF flag (Compare match A flag)

The TCMAF flag indicates that compare match A was detected.

[Setting condition]

- When the value in the AGT register matches the value in the AGTCMA register.

[Clearing condition]

- When 0 is written to this flag by software.

TCMBF flag (Compare match B flag)

The TCMBF flag indicates that compare match B was detected.

[Setting condition]

- When the value in the AGT register matches the value in the AGTCMB register.

[Clearing condition]

- When 0 is written to this flag by software.

22.2.5 AGT Mode Register 1 (AGTMR1)

Address(es): AGT0.AGTMR1 4008 4009h, AGT1.AGTMR1 4008 4109h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	TCK[2:0]			TEDGPL	TMOD[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	TMOD[2:0]	Operating mode*3	b2 b0 0 0 0: Timer mode 0 0 1: Pulse output mode 0 1 0: Event counter mode 0 1 1: Pulse width measurement mode 1 0 0: Pulse period measurement mode. Other settings are prohibited.	R/W
b3	TEDGPL	Edge polarity*4	0: Single-edge 1: Both-edge.	R/W
b6 to b4	TCK[2:0]	Count source*1, *2, *5	b6 b4 0 0 0: PCLKB 0 0 1: PCLKB/8 0 1 1: PCLKB/2 1 0 0: Divided clock AGTLCLK specified by CKS[2:0] bits in the AGTMR2 register 1 0 1: Underflow event signal from AGT0*6 1 1 0: Divided clock AGTSCLK specified by CKS[2:0] bits in the AGTMR2 register. Other settings are prohibited.	R/W
b7	—	Reserved	The read value is 0. The write value should be 0.	R/W

Note: Write access to the AGTMR1 register initializes the output from the AGTOn, AGTIOn, AGTOAn and AGTOBn pins of the AGT (n = 0, 1). For details on the output level at initialization, see the description of section 22.2.7, AGT I/O Control Register (AGTIOC).

Note 1. When event counter mode is selected, the external input (AGTIOn) is selected as the count source regardless of the TCK[2:0] bit setting.

Note 2. Do not switch count sources during count operation. Count sources should be switched when both the TSTART and TCSTF bits in the AGTCR register are set to 0 (count stops).

Note 3. The operating mode can only be changed when the count is stopped while both the TSTART and TCSTF bits in the AGTCR register are set to 0 (count stops). Do not change the operating mode during count operation.

Note 4. The TEDGPL bit is only enabled in event counter mode.

Note 5. To run AGT in Software Standby mode or Snooze mode, select AGTLCLK or AGTSCLK.

Note 6. AGT0 cannot use it (setting prohibited). AGT1 uses the AGT0 underflow.

22.2.6 AGT Mode Register 2 (AGTMR2)

Address(es): AGT0.AGTMR2 4008 400Ah, AGT1.AGTMR2 4008 410Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	LPM	—	—	—	—	CKS[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	CKS[2:0]	AGTLCLK or AGTSCLK count source clock frequency division ratio*1, *2, *3	b2 b0 0 0 0: 1/1 0 0 1: 1/2 0 1 0: 1/4 0 1 1: 1/8 1 0 0: 1/16 1 0 1: 1/32 1 1 0: 1/64 1 1 1: 1/128.	R/W
b6 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	LPM	Low Power Mode	0: Normal mode 1: Low power mode.	R/W

Note 1. Do not rewrite the CKS[2:0] bits during count operation. The CKS[2:0] bit should be rewritten when both the TSTART and TCSTF bits in the AGTCR register are set to 0 (count stops).
Note 2. When count source is AGTLCLK or AGTSCLK, CKS[2:0] switch is valid.
Note 3. Do not switch the TCK[2:0] bits in the AGTMR1 register when CKS[2:0] are not 000b. Switch the TCK[2:0] bits in the AGTMR1 register after CKS[2:0] are set to 000b, and wait for 1 cycle of the count source.

LPM bit (Low Power Mode)

The LPM bit selects low power mode, which impacts access to certain AGT registers. Set this bit to 1 to reduce the power consumption when AGT operates in low power mode. When this bit is 1, access to the following registers is prohibited:

- AGT/AGTCMA/AGTCMB/AGTCR.

After this bit is switched from 1 to 0, the first access to the register is constrained as follows:

- AGT: Read AGT register twice. Only the second reading of data is valid.
- AGT, AGTCMA, AGTCMB, and AGTCR: Allow at least 2 cycles of the count source clock when writing to the register.

22.2.7 AGT I/O Control Register (AGTIOC)

Address(es): AGT0.AGTIOC 4008 400Ch, AGT1.AGTIOC 4008 410Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	TIOGT[1:0]		TIPF[1:0]		—	TOE	—	TEDGSEL
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TEDGSEL	I/O polarity switch	Function varies depending on the operating mode (see Table 22.3 and Table 22.4). The TEDGSEL bit switches the AGTOn output polarity and the AGTIOn input/output edge and polarity. In pulse output mode, it only controls polarity of the AGTOn output and AGTIOn output. The AGTOn output and AGTIOn output are initialized when the AGTMR1 register is written and the TSTOP bit of the AGTCR register is written with 1.	R/W

Bit	Symbol	Bit name	Description	R/W
b1	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b2	TOE	AGTOn output enable	0: AGTOn output disabled 1: AGTOn output enabled.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5, b4	TIPF[1:0]	Input filter*3	b5 b4 0 0: No filter 0 1: Filter sampled at PCLKB 1 0: Filter sampled at PCLKB/8 1 1: Filter sampled at PCLKB/32. These bits specifies the sampling frequency of the filter for the AGTIOn input. If the input to the AGTIOn pin is sampled and the value matches three successive times, that value is taken as the input value.	R/W
b7, b6	TIOGT[1:0]	Count control*1, *2	b7 b6 0 0: Event is always counted 0 1: Event is counted during polarity period specified for AGTEEn. Other settings are prohibited.	R/W

Note 1. When AGTEEn pin is used, the polarity to count an event can be selected with the EEPS bit in the AGTISR register.
Note 2. TIOGT[1:0] bits are only enabled in event counter mode.
Note 3. When event counter mode operation is performed during Software Standby mode, the digital filter function cannot be used.

Table 22.3 AGTIOn I/O edge and polarity switching

Operating mode	Function
Timer mode	Not used
Pulse output mode	0: Output is started at high (initialization level: high) 1: Output is started at low (initialization level: low).
Event counter mode	0: Count on rising edge 1: Count on falling edge.
Pulse width measurement mode	0: Low-level width is measured 1: High-level width is measured.
Pulse period measurement mode	0: Measure from one rising edge to the next rising edge 1: Measure from one falling edge to the next falling edge.

Table 22.4 AGTOn output polarity switching

Operating mode	Function
All modes	0: Output is started at low (initialization level: low) 1: Output is started at high (initialization level: high).

22.2.8 AGT Event Pin Select Register (AGTISR)

Address(es): AGT0.AGTISR 4008 400Dh, AGT1.AGTISR 4008 410Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	EEPS	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b2	EEPS	AGTEEn polarity selection	0: An event is counted during the low-level period 1: An event is counted during the high-level period.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

22.2.9 AGT Compare Match Function Select Register (AGTCMSR)

Address(es): AGT0.AGTCMSR 4008 400Eh, AGT1.AGTCMSR 4008 410Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	TOPOLB	TOEB	TCMEB	—	TOPOLA	TOEA	TCMEA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TCMEA	Compare match A register enable*1, *2	0: Disable compare match A register 1: Enable compare match A register.	R/W
b1	TOEA	AGTOAn output enable*1, *2	0: Disable AGTOAn output 1: Enable AGTOAn output.	R/W
b2	TOPOLA	AGTOAn polarity select*1, *2	0: Start AGTOAn output on low 1: Start AGTOAn output on high.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	TCMEB	Compare match B register enable*1, *2	0: Disable compare match B register 1: Enable compare match B register.	R/W
b5	TOEB	AGTOBn output enable*1, *2	0: Disable AGTOBn output 1: Enable AGTOBn output.	R/W
b6	TOPOLB	AGTOBn polarity select*1, *2	0: Start AGTOBn output on low 1: Start AGTOBn output on high.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. Do not rewrite the AGTCMSR register during count operation. Only rewrite the AGTCMSR register when both the TSTART and TCSTF bits in the AGTCR register are set to 0 (count stops).

Note 2. Do not set 1 when in pulse width measurement mode or pulse period measurement mode.

22.2.10 AGT Pin Select Register (AGTIOSEL)

Address(es): AGT0.AGTIOSEL 4008 400Fh, AGT1.AGTIOSEL 4008 410Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	TIES	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	TIES	AGTIOn Input Enable	0: Disable external event input during Software Standby mode 1: Enable external event input during Software Standby mode.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The AGTIOSEL register sets the AGTIOn pin when using the AGTIOn in Software Standby mode. The AGTIOSEL register can be set with an 8-bit memory manipulation instruction.

TIES bit (AGTIOn Input Enable)

The TIES bit enables or disables an external event input.

22.3 Operation

22.3.1 Reload Register and Counter Rewrite Operation

Regardless of the operating mode, the timing of the rewrite operation to the reload register and the counter differs depending on the value of the TSTART bit in the AGTCR register and of the TCMEA/TCMEB bit in the AGTCMSR register. When the TSTART bit is 0 (count stops), the count value is directly written to the reload register and the counter. When the TSTART bit is 1 (count starts) and the TCMEA and TCMEB bits are 0 (compare match A/B register are invalid), the value is written to the reload register in synchronization with the count source, and then to the counter in synchronization with the next count source. When the TSTART bit is 1 (count starts) and the TCMEA bit or the TCMEB bit is 1 (compare match A register or compare match B register is valid), the value is written to the reload register in synchronization with the count source, and then to the counter in synchronization with the underflow of the counter.

Figure 22.2 and Figure 22.3 show the timing of rewrite operation with TSTART bit value and TCMEA/TCMEB bit value.

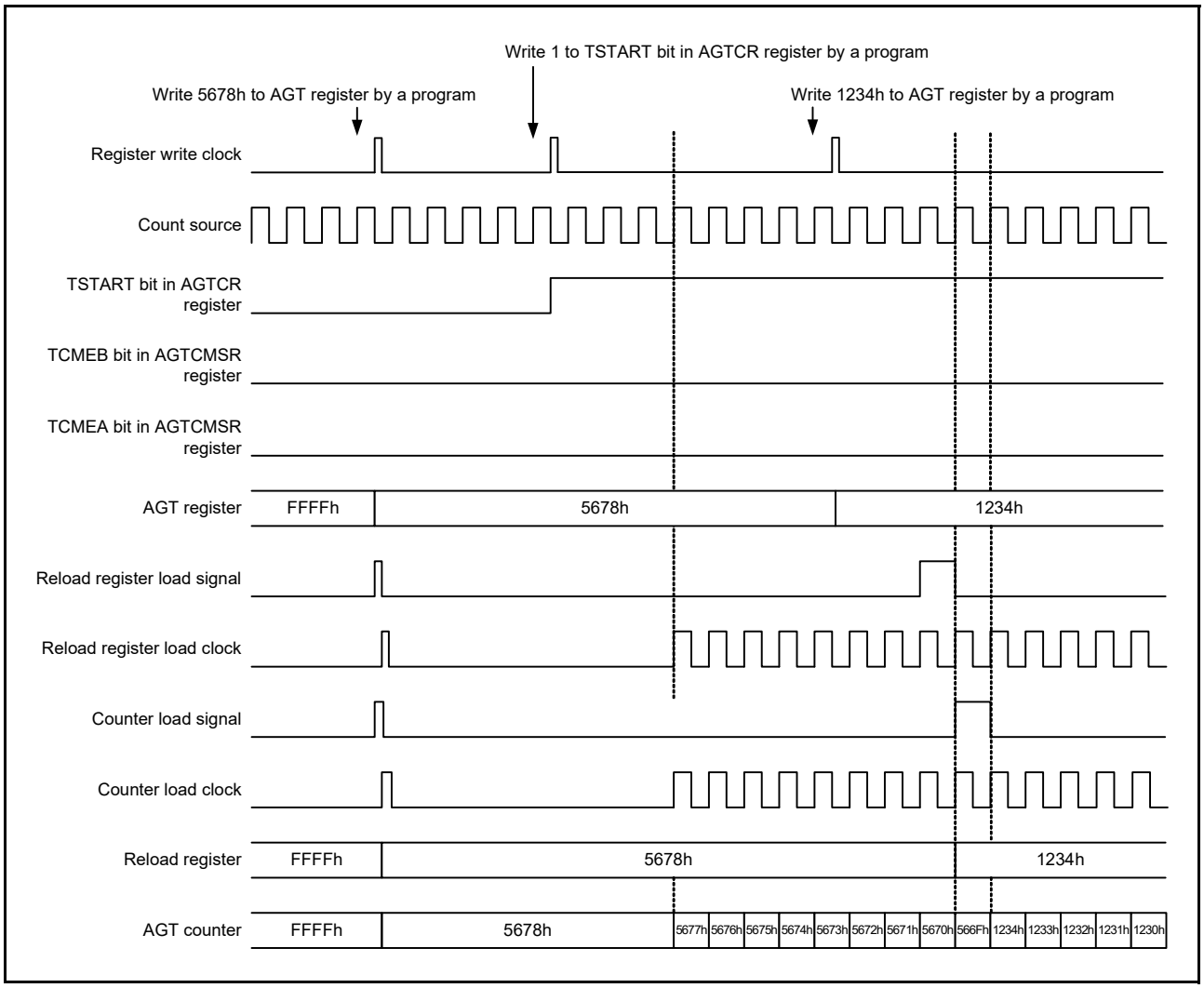


Figure 22.2 Timing of rewrite operation with TSTART, TCMEA and TCMEB bit values when compare match A register and compare match B register are invalid

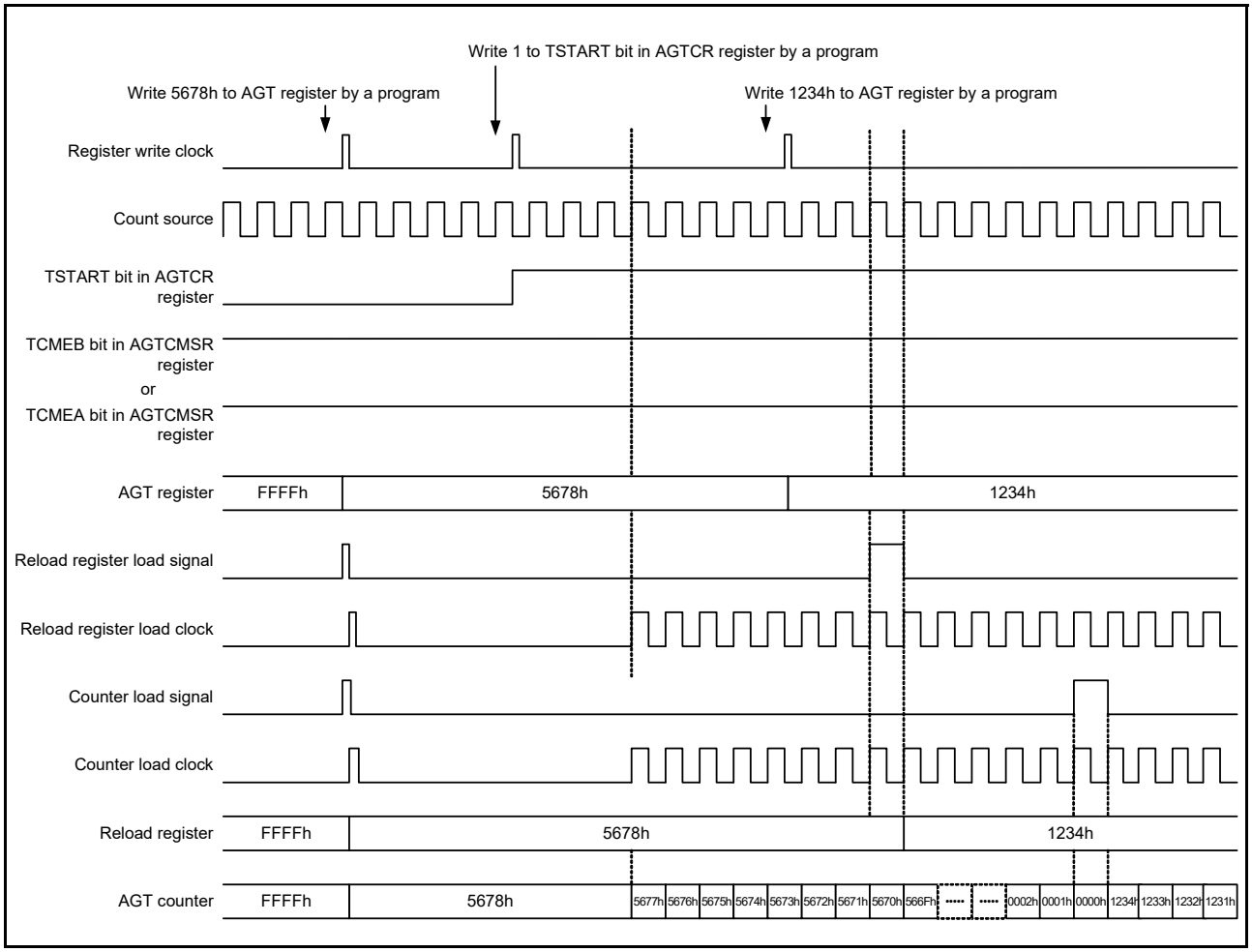


Figure 22.3 Timing of rewrite operation with TSTART and TCMEA or TCMEB bit values when compare match A register or B is valid

22.3.2 Reload Register and Compare Register A/B Rewrite Operation

Regardless of the operating mode, the timing of the rewrite operation to compare register A/B depends on the value of the TSTART bit in the AGTCR register. When the TSTART bit is 0 (count stops), the count value is directly written to the reload register and compare register A/B. When the TSTART bit is 1 (count starts), the value is written to the reload register in synchronization with the count source, and then to the compare register in synchronization with the underflow of the counter.

Figure 22.4 shows the timing of rewrite operation with TSTART bit value for compare register A. Compare register B is of the same timing as compare register A.

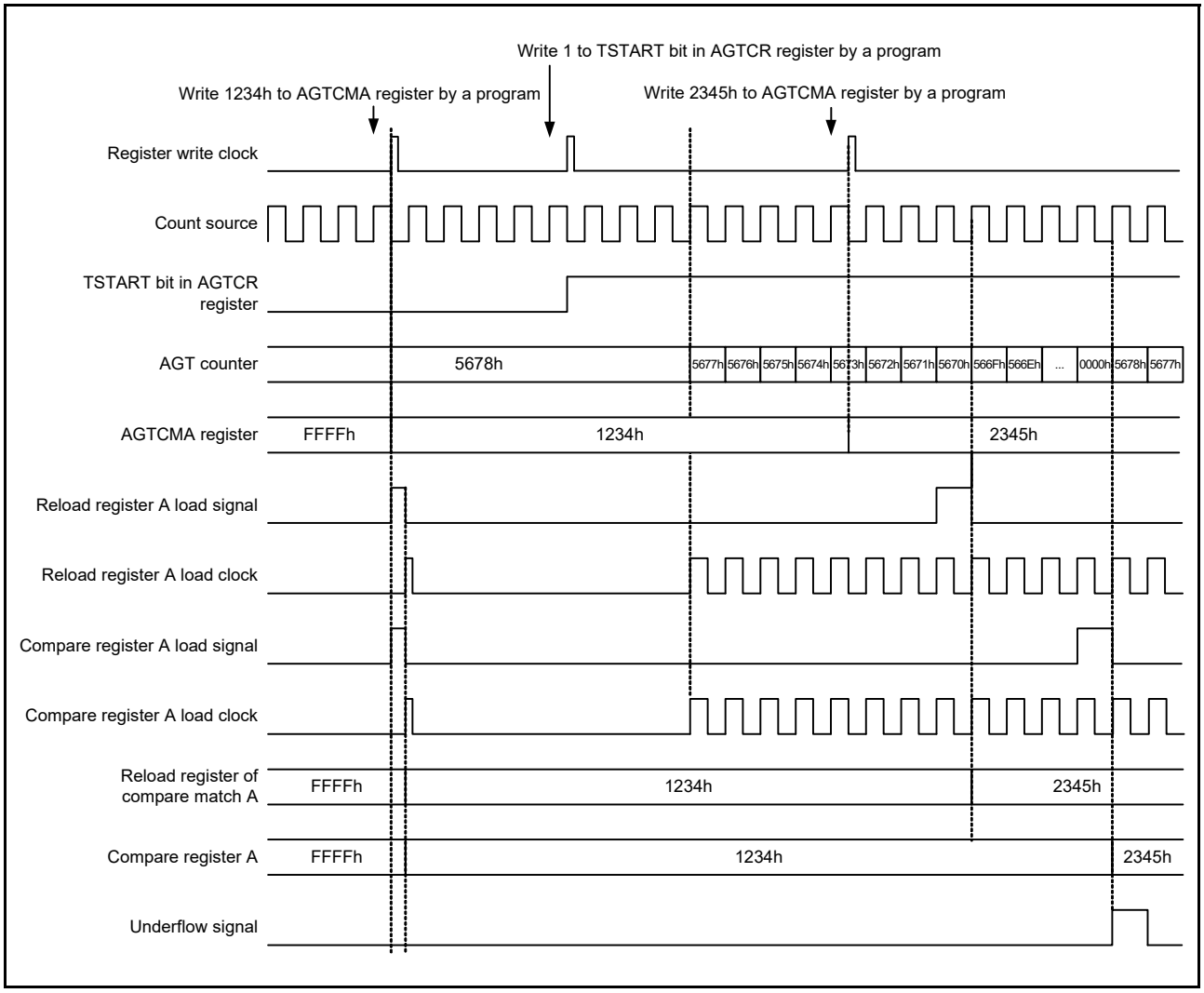


Figure 22.4 Timing of rewrite operation with TSTART bit value for compare register A

22.3.3 Timer Mode

In this mode, the AGT counter is decremented by the count source selected by TCK[2:0] bits in the AGTMR1 register. In timer mode, the count value is decremented by 1 on each rising edge of the count source. When the count value reaches 0000h and the next count source is input, an underflow occurs and an interrupt request is generated.

Figure 22.5 shows the operation example in timer mode.

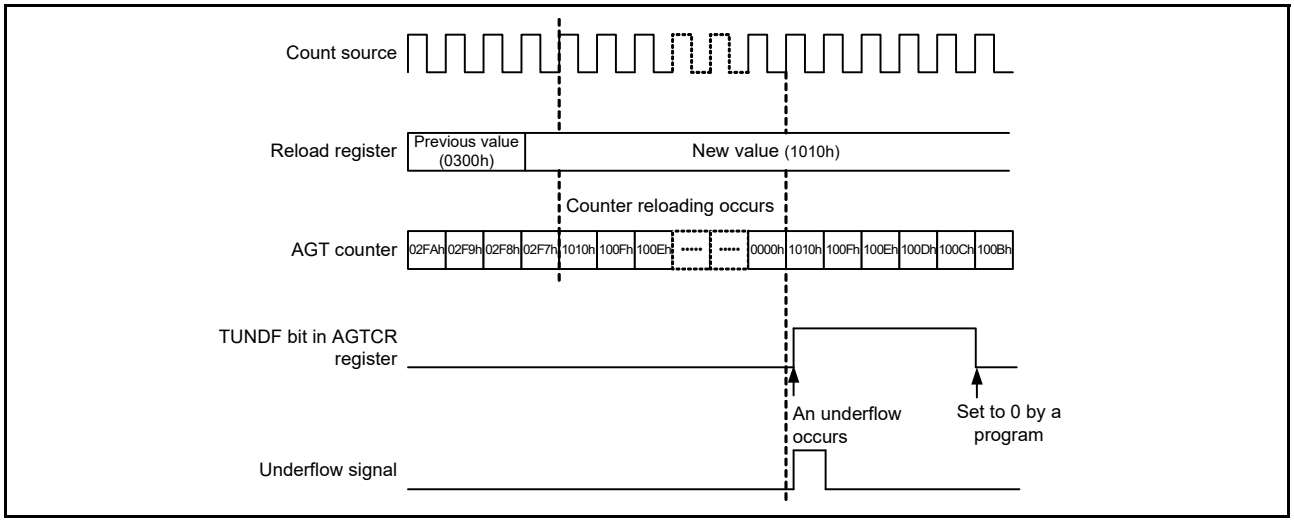


Figure 22.5 Operation example in timer mode

22.3.4 Pulse Output Mode

In this mode, the counter is decremented by the count source selected by TCK[2:0] bits in the AGTMR1 register, and the output level of pins AGTIOn and AGTOn pin is inverted each time an underflow occurs.

In pulse output mode, the count value is decremented by 1 on each rising edge of the count source. When the count value reaches 0000h and the next count source is input, an underflow occurs and an interrupt request is generated. In addition, a pulse can be output from the AGTIOn and AGTOn pins. The output level is inverted each time an underflow occurs. The pulse output from the AGTOn pin can be stopped with the TOE bit in the AGTIOC register. The output level can be selected with the TEDGSEL bit in the AGTIOC register.

Figure 22.6 shows the operation example in pulse output mode.

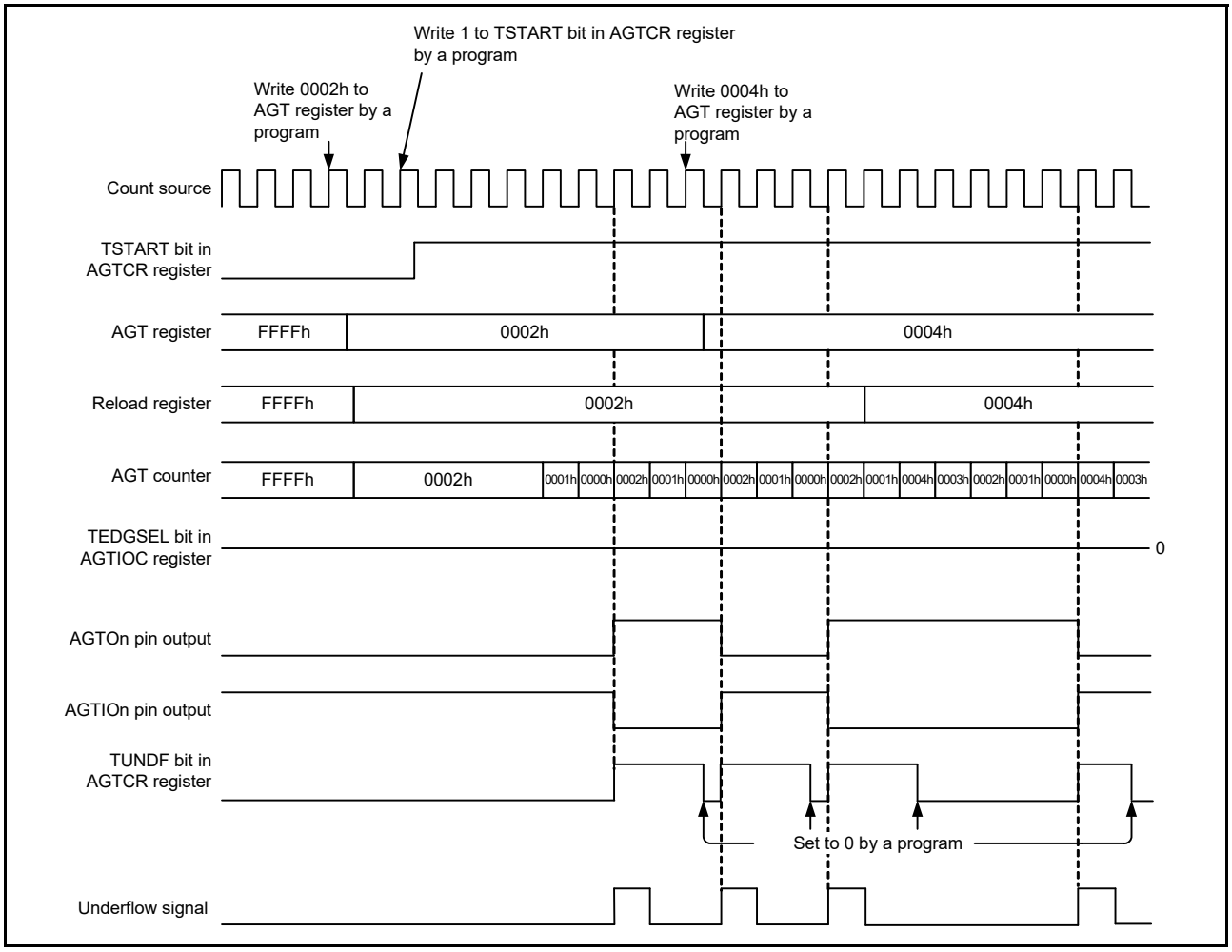


Figure 22.6 Operation example in pulse output mode

22.3.5 Event Counter Mode

In this mode, the counter is decremented by an external event signal (count source) input to the AGTIOn pin. Different periods for counting events can be set with the TIOGT[1:0] bits in the AGTIOC register and the AGTISR register. In addition, the filter function for the AGTIOn input can be specified with bits TIPF[1:0] in the AGTIOC register. The output from the AGTOn pin can be toggled even in event counter mode.

Figure 22.7 shows the operation example in event counter mode.

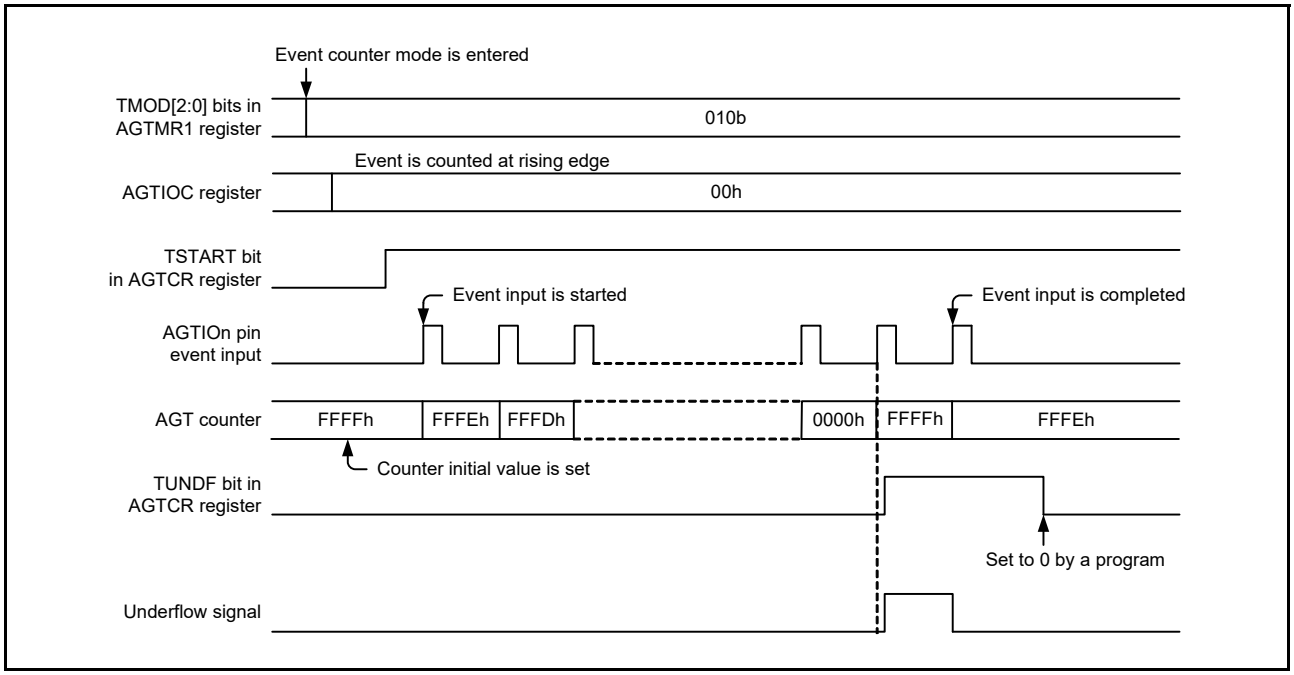


Figure 22.7 Operation example 1 in event counter mode

Figure 22.8 shows an operation example for counting during the specified period in event counter mode (TIOGT[1:0] bits in the AGTIOC register are set to 01b).

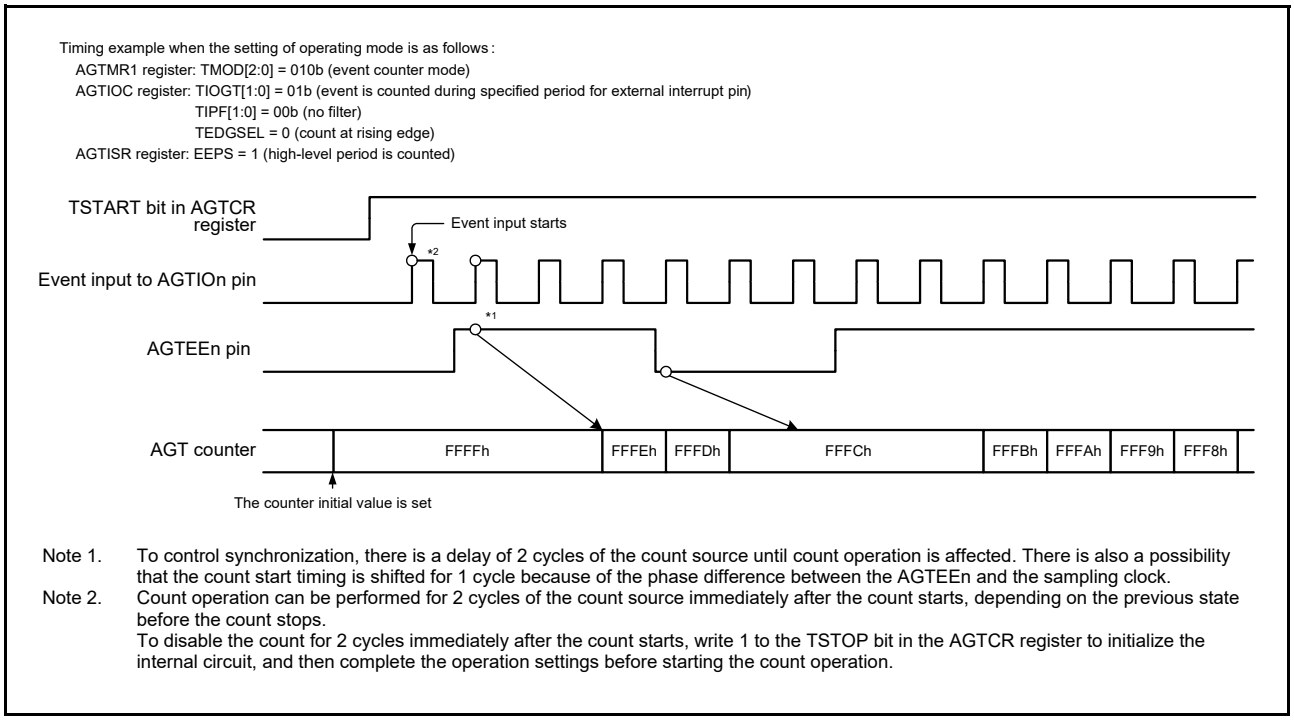


Figure 22.8 Operation example 2 in event counter mode

22.3.6 Pulse Width Measurement Mode

In this mode, the pulse width of an external signal input to the AGTIOn pin is measured. When the level specified by the TEDGSEL bit in the AGTIOC register is input to the AGTIOn pin, the counter is decremented by the count source selected by TCK[2:0] bits in the AGTMR1 register. When the specified level on the AGTIOn pin ends, the counter is stopped, the TEDGF bit in the AGTCR register is set to 1 (active edge received), and an interrupt request is generated. The measurement of pulse width data is performed by reading the count value while the counter is stopped. Also, when

the counter underflows during measurement, the TUNDF bit in the AGTCR register is set to 1 and an interrupt request is generated.

Figure 22.9 shows the operation example in pulse width measurement mode.

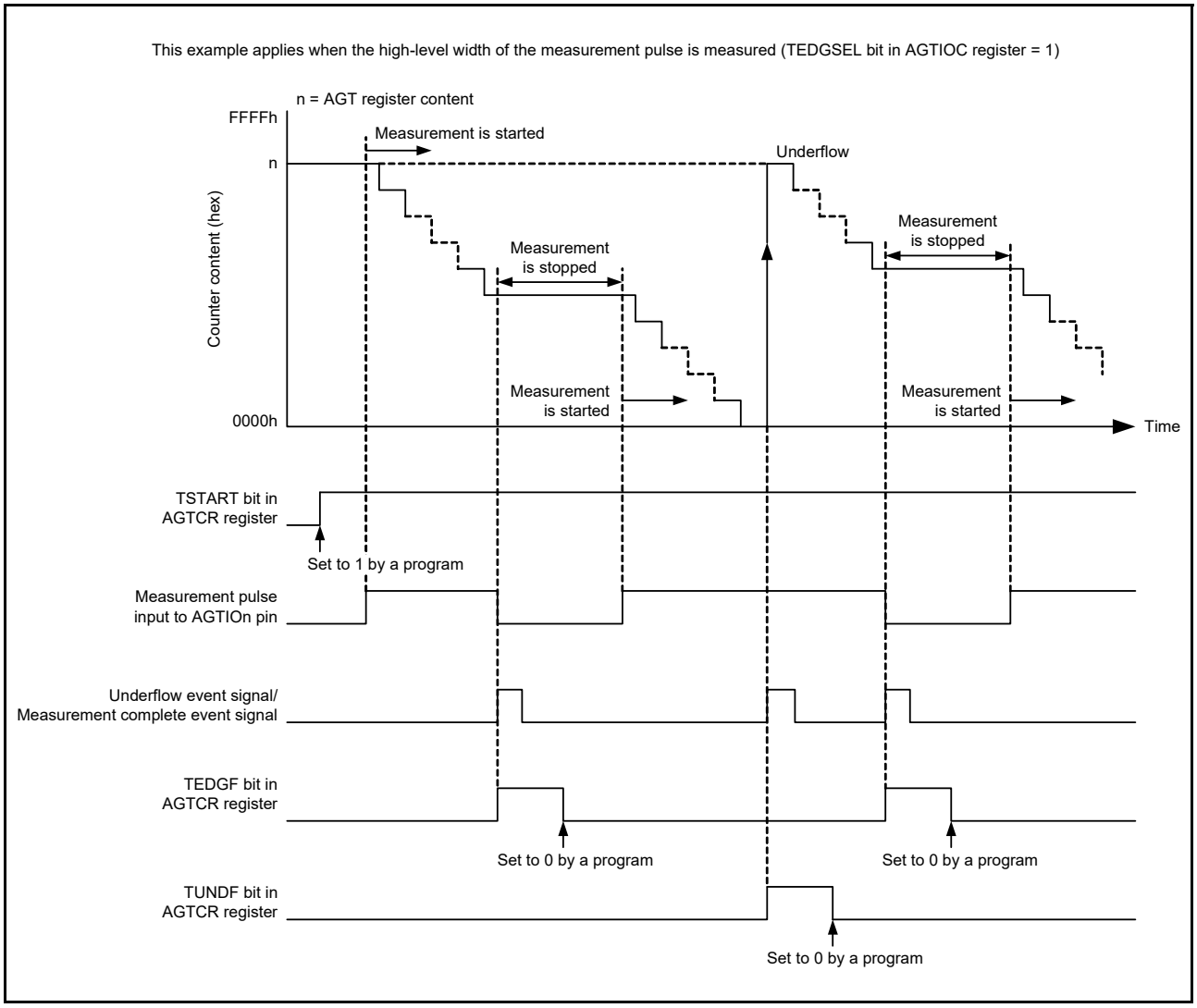


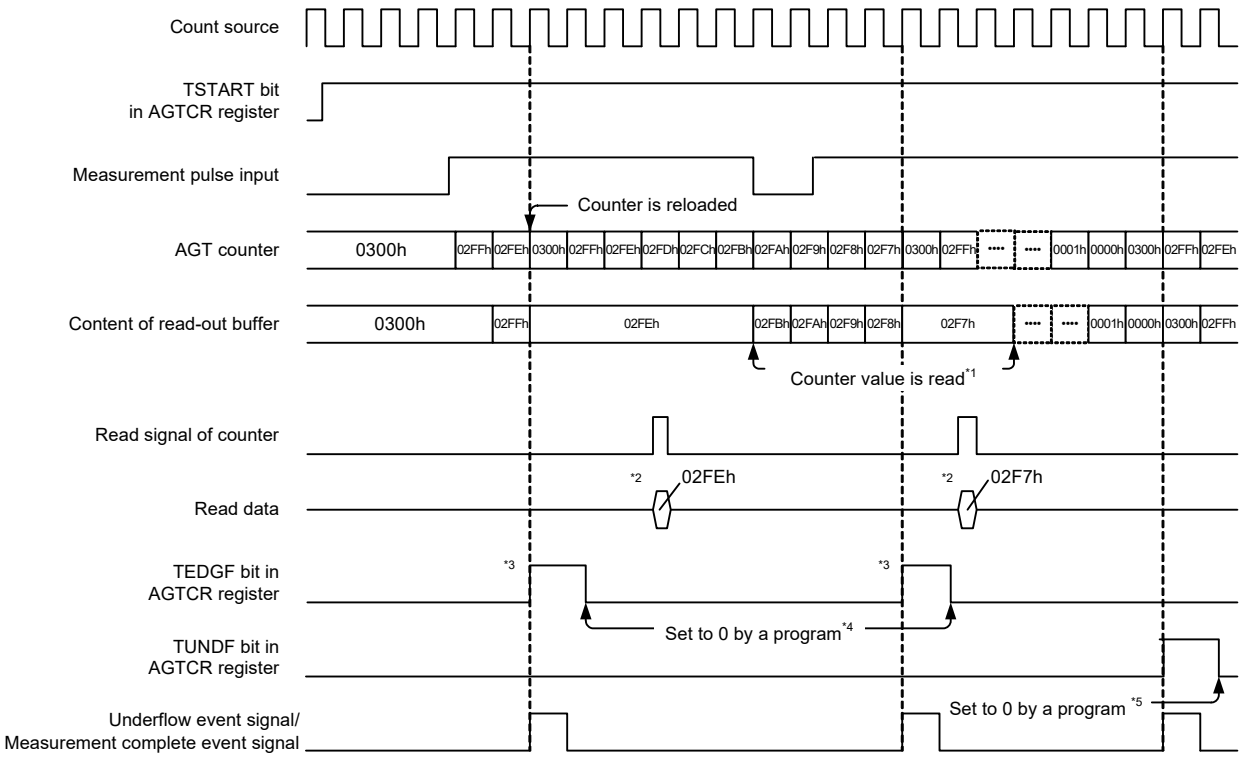
Figure 22.9 Operation example in pulse width measurement mode

22.3.7 Pulse Period Measurement Mode

In this mode, the pulse period of an external signal input to the AGTIOn pin is measured. The counter is decremented by the count source selected with bits TCK[2:0] in the AGTMR1 register. When a pulse with the period specified by the TEDGSEL bit in the AGTIOC register is input to the AGTIOn pin, the count value is transferred to the read-out buffer on the rising edge of the count source. The value in the reload register is loaded to the counter at the next rising edge. Simultaneously, the TEDGF bit in the AGTCR register is set to 1 (active edge received) and an interrupt request is generated. The read-out buffer (AGT register) is read at this time and the difference from the reload value (see section 22.4.5, How to Calculate Event Number, Pulse Width, and Pulse Period) is the period data of the input pulse. The period data is retained until the read-out buffer is read. When the counter underflows, the TUNDF bit in the AGTCR register is set to 1 (underflow) and an interrupt request is generated.

Figure 22.10 shows the operation example in pulse period measurement mode.

Only input pulses with a period longer than twice the period of the count source are measured. Also, the low-level and high-level widths must both be longer than the period of the count source. If a pulse period shorter than these conditions is input, the input might be ignored.



This example applies when the initial value of the AGT register is set to 0300h, the TEDGSEL bit in the AGTIOC register is set to 0, and the period from one rising edge to the next edge of the measurement pulse is measured.

Note 1. Reading from the AGT register must be performed during the period from when the TEDGF bit is set to 1 (active edge received) until the next active edge is input. The content of the read-out buffer is retained until the AGT register is read. If it is not read before the active edge is input, the measurement result of the previous period is retained.
Note 2. When the AGT register is read in pulse period measurement mode, the content of the read-out buffer is read.
Note 3. When the active edge of the measurement pulse is input and then the set edge of an external pulse is input, the TEDGF bit in the AGTCR register is set to 1 (active edge received).
Note 4. To set to 0 with software, write 0 to the TEDGF bit in the AGTCR register using an 8-bit memory manipulation instruction.
Note 5. To set to 0 with software, write 0 to the TUNDF bit in the AGTCR register using an 8-bit memory manipulation instruction.

Figure 22.10 Operation example in pulse period measurement mode

22.3.8 Compare Match function

This function detects matches between the content of the AGTCMA/AGTCMB register and the content of the AGT register. This function is enabled when the TCMEA or TCMEB bit in the AGTCMSR register is 1 (Compare match A register or compare match B register is valid). The counter is decremented by the count source selected with bits TCK[2:0] in the AGTMR1 register, and when the values of AGT and AGTCMA/AGTCMB match, the TCMAF/TCMBF bit in the AGTCR register is set to 1, and an interrupt request is generated.

When the compare match function is enabled, the timing of the rewrite operation to the reload register and the counter differs. See section 22.3.1, Reload Register and Counter Rewrite Operation for details. In addition, the output level of the AGTOAn and AGTOBn pins is inverted by the match and by the underflow. The output level can be selected with the TOPOLA or TOPOLB bit in the AGTCMSR register.

Figure 22.11 shows the operation example in compare match mode.

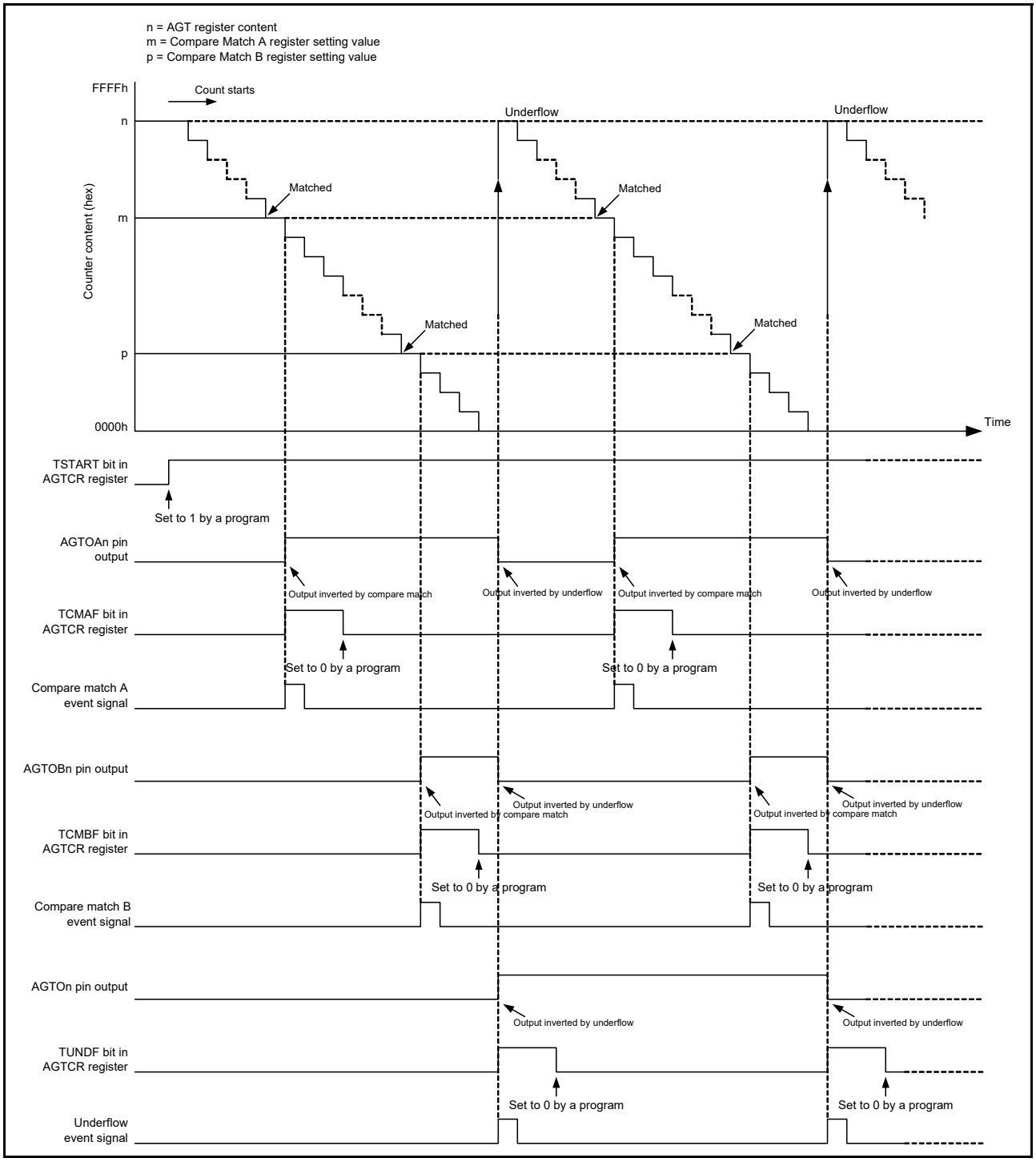


Figure 22.11 Operation example in compare match mode (TOPOLA = 0, TOPOLB = 0)

22.3.9 Output Settings for Each Mode

Table 22.5 to Table 22.8 list the states of pins AGTOn, AGTIOn, AGTOAn, and AGTOBn in each mode.

Table 22.5 AGTOn pin setting

Operating mode	AGTIOC Register		AGTOn pin output
	TOE bit	TEDGSEL bit	
All modes	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled

Table 22.6 AGTIOn pin setting

Operating mode	AGTIOC Register	AGTIOn pin I/O
	TEDGSEL bit	
Timer mode	0 or 1	Input (Not used)
Pulse output mode	1	Normal output
	0	Inverted output
Event counter mode	0 or 1	Input
Pulse width measurement mode		
Pulse period measurement mode		

Table 22.7 AGTOAn pin setting

Operating mode	AGTCMSR Register		AGTOAn pin output
	TOEA bit	TOPOLA bit	
Timer mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (Not used)
Pulse output mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (Not used)
Event counter mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (Not used)
Pulse width measurement mode	0	0	Prohibited
Pulse period measurement mode			

Table 22.8 AGTOBn pin setting (1 of 2)

Operating mode	AGTCMSR Register		AGTOBn pin output
	TOEB bit	TOPOLB bit	
Timer mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (Not used)
Pulse output mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (Not used)

Table 22.8 AGTOBn pin setting (2 of 2)

	AGTCMSR Register		
Operating mode	**TOEB bit**	**TOPOLB bit**	**AGTOBn pin output**
Event counter mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (Not used)
Pulse width measurement mode	0	0	Prohibited
Pulse period measurement mode			

22.3.10 Standby Mode

The AGT can operate in Software Standby mode. Set it to Software Standby mode with count operation start (TSTART = 1, TCSTF = 1).

Table 22.9 and Table 22.10 show the setting that can be used in Software Standby mode.

Table 22.9 Usable settings in Software Standby mode (AGT0)

Operating mode	TCK[2:0] bits of AGTMR1 Register	Operating clock	Resurgence factor of CPU
Timer mode	100b or 110b	AGTLCLK or AGTSCLK	-
Pulse output mode	100b or 110b	AGTLCLK or AGTSCLK	-
Event counter mode	- (invalid)	AGTIOn	-
Pulse width measurement mode	100b or 110b	AGTLCLK or AGTSCLK	-
Pulse period measurement mode	100b or 110b	AGTLCLK or AGTSCLK	-

Table 22.10 Usable settings in Software Standby mode (AGT1)

Operating mode	TCK[2:0] Bits of AGTMR1 register	Operating clock	Resurgence factor of CPU
Timer mode	100b or 110b or 101b *1	AGTLCLK or AGTSCLK or AGT0 underflow	• Underflow • Compare match A/B
Pulse output mode	100b or 110b or 101b *1	AGTLCLK or AGTSCLK or AGT0 underflow	• Underflow • Compare match A/B
Event counter mode	- (invalid)	AGTIOn	• Underflow • Compare match A/B
Pulse width measurement mode	100b or 110b or 101b *1	AGTLCLK or AGTSCLK or AGT0 underflow	• Underflow • Active edge
Pulse period measurement mode	100b or 110b or 101b *1	AGTLCLK or AGTSCLK or AGT0 underflow	• Underflow • Active edge

Note: Release of Software Standby mode is only AGT1.
Note 1. Only when AGT0 operates in Table 22.9.

22.3.11 Interrupt Sources

The AGT has three interrupt sources for channels n (n = 0, 1) as listed in Table 22.11.

Table 22.11 AGT interrupt sources

Name	Interrupt source	DTC activation
AGTn_AGTI	• When the counter underflows • When the measurement of the active width of the external input (AGTIOn) is complete in pulse width measurement mode • When the set edge of the external input (AGTIOn) is input in pulse period measurement mode.	Possible
AGTn_AGTCMAI	• When the values of AGT and AGTCMA match	Possible
AGTn_AGTCMBI	• When the values of AGT and AGTCMB match	Possible

Channel number (n = 0, 1)

22.3.12 Event Signal Output to ELC

The AGT uses the Event Link Controller (ELC) to perform a link operation to a specified module using the interrupt request signal as the event signal. The AGT outputs compare match A, compare match B, and underflow/measurement complete signals as event signals. For details, see section 16, Event Link Controller (ELC).

22.4 Usage Notes

22.4.1 Count Operation Start and Stop Control

- When the operating mode (see Table 22.1) is set to other than the event counter mode, or the count source is set to other than AGT0 underflow (TCK[2:0] = 101b):
  - After 1 (count starts) is written to the TSTART bit in the AGTCR register while the count stops, the TCSTF bit in the AGTCR register remains 0 (count stops) for 3 cycles of the count source. Do not access the registers associated with AGT*1 other than the TCSTF bit until this bit is set to 1 (count in progress).
  - After 0 (count stops) is written to the TSTART bit during a count operation, the TCSTF bit remains 1 for 3 cycles of the count source. When the TCSTF bit is set to 0, the count stops. Do not access the registers associated with AGT*1. other than the TCSTF bit until this bit is set to 0.
  - Clear the interrupt register before changing the TSTART bit from 0 to 1. See section 12, Interrupt Controller Unit (ICU) for details.

Note 1. Registers associated with AGT: AGT, AGTCMA, AGTCMB, AGTCR, AGTMR1, AGTMR2, AGTIOC, AGTISR and AGTCMSR.

- When the operating mode (see Table 22.1) is set to event counter mode, or the count source is set to AGT0 underflow (TCK[2:0] = 101b):
  - After 1 (count starts) is written to the TSTART bit in the AGTCR register while the count stops, the TCSTF bit in the AGTCR register remains 0 (count stops) for 2 PCLKB cycles. Do not access the registers associated with AGT*1 other than the TCSTF bit until this bit is set to 1 (count in progress).
  - After 0 (count stops) is written to the TSTART bit during a count operation, the TCSTF bit remains 1 for 2 PCLKB cycles. When the TCSTF bit is set to 0, the count stops. Do not access the registers associated with AGT*1 other than the TCSTF bit until this bit is set to 0.
  - Clear the interrupt register before changing the TSTART bit from 0 to 1. See section 12, Interrupt Controller Unit (ICU) for details.

Note 1. Registers associated with AGT: AGT, AGTCMA, AGTCMB, AGTCR, AGTMR1, AGTMR2, AGTIOC, AGTISR and AGTCMSR

22.4.2 Access to Counter Register

When the TSTART and TCSTF bits in the AGTCR register are both 1 (count starts), allow at least 3 cycles of the count source clock between writes when writing to the AGT register successively.

22.4.3 When Changing Mode

The registers associated with AGT operating mode (AGTMR1, AGTMR2, AGTIOC, AGTISR and AGTCMSR) can be

changed only when the count is stopped with both the TSTART and TCSTF bits set to 0 (count stops). Do not change these registers during count operation.

When the registers associated with AGT operating mode are changed, the values of TEDGF, TUNDF, TCMAF, and TCMBF bits are undefined. Before starting the count, write 0 to the following bits:

- TEDGF
- TUNDF
- TCMAF
- TCMBF.

22.4.4 Digital Filter

When using the digital filter, do not start the timer operation for 5 cycles of the digital filter clock after setting TIPF[1:0] bits and when the TEDGSEL bit in the AGTIOC register changes.

22.4.5 How to Calculate Event Number, Pulse Width, and Pulse Period

- In event counter mode, event number is expressed mathematically as follows:
  Event number = initial value of counter [AGT register] - counter value of active event end
- In pulse width measurement mode, pulse width is expressed mathematically as follows:
  Pulse width = counter value of stopping measurement - counter value of next stopping measurement
- In pulse period measurement mode, input pulse period is expressed mathematically as follows:
  Period of input pulse = (initial value of counter [AGT register] - reading value of the read-out buffer) + 1

22.4.6 When Count is Forcibly Stopped by TSTOP Bit

After the counter is forcibly stopped by the TSTOP bit in the AGTCR register, do not access the following I/O registers for 1 cycle of the count source:

- AGT
- AGTCMA
- AGTCMB
- AGTCR
- AGTMR1
- AGTMR2.

22.4.7 When Selecting AGT0 Underflow as Count Source

Operate the AGT according to the following procedures when selecting the underflow signal of AGT as the count source.

(1) Procedure for starting operation

1. Set AGT0 and AGT1.
2. Start the count operation of AGT1.
3. Start the count operation of AGT0.

(2) Procedure for stopping operation

1. Stop the count operation of AGT0.
2. Stop the count operation of AGT1.
3. Stop the count source clock of AGT1 (write 000b in AGT1.AGTMR1.TCK[2:0] bits).

22.4.8 Reset of I/O Register

The I/O register of the AGT is not initialized by different types of resets. For details, see section 5, Resets.

22.4.9 When Selecting PCLKB, PCLKB/8, or PCLKB/2 as Count Source

When a reset is generated, the operation of AGT cannot be guaranteed. Set the registers associated with AGT again.

22.4.10 When Selecting AGTLCLK or AGTSCLK as Count Source

The MSTPD2 in MSTPCRD register must be set to 1 except when accessing the AGT1 registers. The MSTPD3 in the MSTPCRD register must be set to 1 except when accessing the AGT0 registers. When a reset occurs while MSTPD2 or MSTPD3 is 0, the operation of AGT1 or AGT0 cannot be guaranteed. Set the registers associated with AGT again.

22.4.11 When Switching Source Clock

When switching a clock source by changing SCKSCR.CKSEL[2:0], the clock output from the selector stops for 4 cycles of the switched clock. Therefore, when using the AGTIOn, AGTEEn, or both input as external event input, the clock source should not be switched. If switching the clock source while using the external event input, extend the input pulse width by 4 clock cycles of the switched source clock cycles.

23. Realtime Clock (RTC)

23.1 Overview

The RTC has two counting modes, calendar count mode and binary count mode, that are used by switching register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar.

The sub-clock oscillator or LOCO can be selected as the count source of the time counters. The RTC uses a 128-Hz clock acquired by dividing the count source by a prescaler. Year, month, date, day-of-week, a.m./p.m. (in 12-hour mode), hour, minute, second, or 32-bit binary is counted by 1/128 second.

Table 23.1 lists the RTC specifications, Figure 23.1 shows a block diagram, and Table 23.2 lists the I/O pins.

Table 23.1 RTC specifications

Parameter	Description
Count mode	Calendar count mode/binary count mode
Count source*1	Sub-clock (XCIN) or LOCO
Clock and calendar functions	• Calendar count mode Year, month, date, day of week, hour, minute, second are counted, BCD display 12 hours/24 hours mode switching function 30 seconds adjustment function (a number less than 30 is rounded down to 00 seconds, and 30 seconds or more are rounded up to 1 minute) Automatic adjustment function for leap years • Binary count mode Count seconds in 32 bits, binary display • Common to both modes Start/stop function The sub-second digit is displayed in binary units (1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, or 64 Hz). Clock error correction function Clock (1-Hz/64-Hz) output.
Interrupts	• Alarm interrupt (RTC_ALM) As an alarm interrupt condition, selectable for comparison with the following: Calendar count mode: Year, month, date, day-of-week, hour, minute, or second can be selected Binary count mode: Each bit of the 32-bit binary counter • Periodic interrupt (RTC_PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second can be selected as an interrupt period. • Carry interrupt (RTC_CUP) An interrupt is generated at either of the following conditions: - When a carry from the 64-Hz counter to the second counter is generated. - When the 64-Hz counter is changed and the R64CNT register is read at the same time. • Return from Software Standby mode can be performed by an alarm interrupt or periodic interrupt
Event link function	Periodic event output (RTC_PRD)

Note 1. Satisfy the frequency of the peripheral module clock (PCLKB) ≥ the frequency of the count source clock.

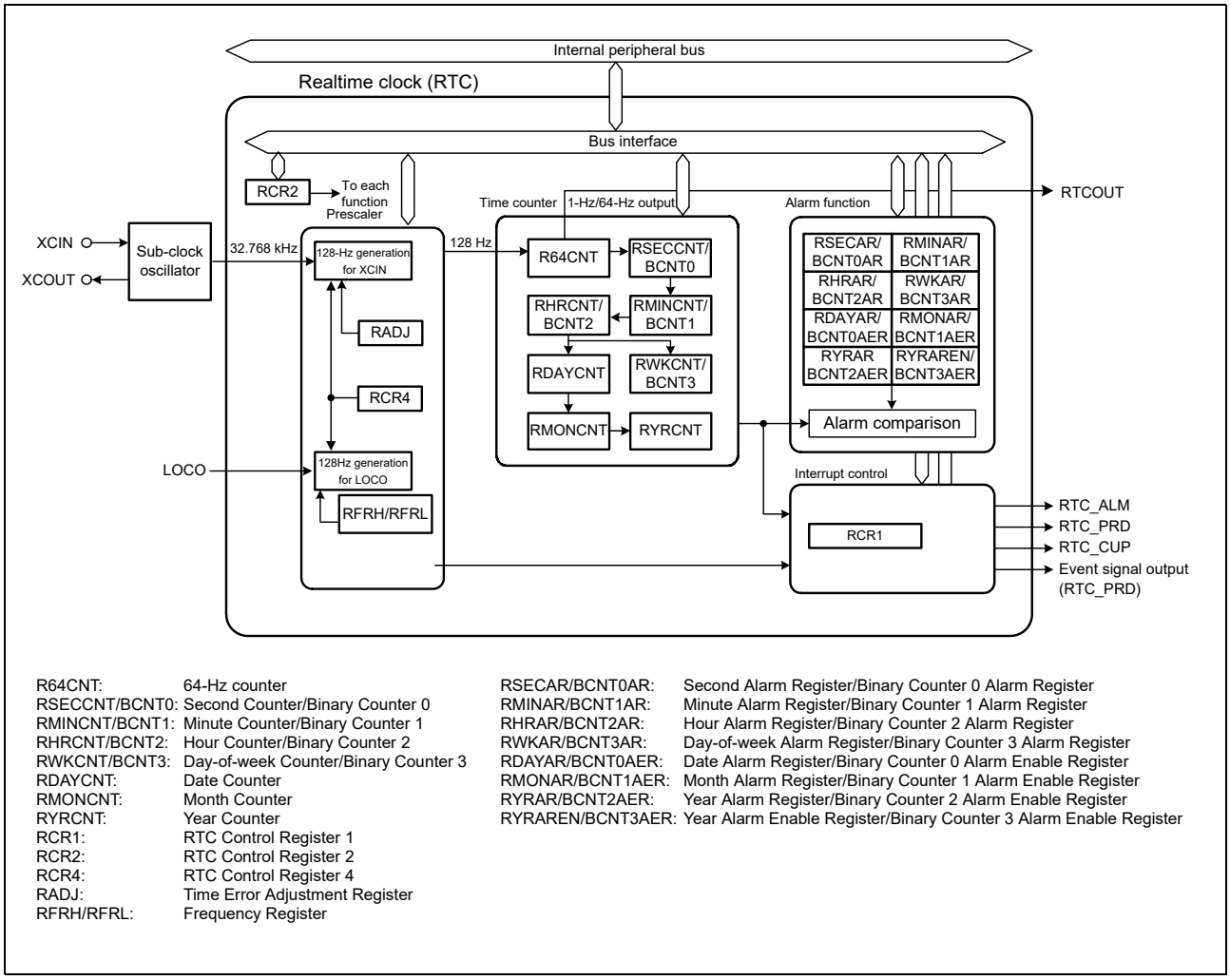


Figure 23.1 RTC block diagram

Table 23.2 RTC I/O pins

Pin name	I/O	Function
XCIN	Input	Connect a 32.768-kHz crystal to these pins
XCOUT	Output	
RTCOUT	Output	This pin is used to output a 1-Hz/64-Hz waveform

23.2 Register Descriptions

Write or read from the RTC registers as described in section 23.6.5, Notes when Writing to and Reading from Registers.

If the value in an RTC register after a reset is given as *x* (undefined bits) in the list, it is not initialized by a reset. When RTC enters the reset state or a low power state during counting operations, for example, while the RCR2.START bit is 1, the year, month, day of the week, date, hours, minutes, seconds, and 64-Hz counters continue to operate.

Note: A reset generated while writing to a register might destroy the register value. In addition, do not allow the MCU to enter Software Standby mode immediately after setting any of these registers. For details, see section 23.6.4, Transitions to Low Power Modes after Setting Registers.

23.2.1 64-Hz Counter (R64CNT)

Address(es): RTC.R64CNT 4004 4000h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	F1HZ	F2HZ	F4HZ	F8HZ	F16HZ	F32HZ	F64HZ
Value after reset:	0	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	F64HZ	64 Hz	These bits indicate the state between 1 Hz and 64 Hz of the sub-second digit	R
b1	F32HZ	32 Hz		R
b2	F16HZ	16 Hz		R
b3	F8HZ	8 Hz		R
b4	F4HZ	4 Hz		R
b5	F2HZ	2 Hz		R
b6	F1HZ	1 Hz		R
b7	—	Reserved	This bit is read as 0	R

The R64CNT counter is used in both calendar count mode and binary count mode. The 64-Hz counter (R64CNT) generates the period for a second by counting up periods of the 128-Hz clock. The state in the sub-second range can be confirmed by reading this counter.

This counter is set to 00h by an RTC software reset or an execution of a 30-second adjustment. To read this counter, follow the procedure in section 23.3.5, Reading 64-Hz Counter and Time.

23.2.2 Second Counter (RSECCNT)/Binary Counter 0 (BCNT0)

(1) In calendar count mode:

Address(es): RTC.RSECCNT 4004 4002h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	SEC10[2:0]			SEC1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	SEC1[3:0]	1-Second Count	Counts from 0 to 9 every second. When a carry is generated, 1 is added to the tens place.	R/W
b6 to b4	SEC10[2:0]	10-Second Count	Counts from 0 to 5 for 60-second counting	R/W
b7	—	Reserved	Set this bit to 0. It is read as the set value.	R/W

The RSECCNT counter is used for setting and counting the BCD-coded second value. It counts carries generated once per second in the 64-Hz counter.

The setting range is decimal 00 to 59. The RTC does not operate normally if any other value is set. Before writing to this register, be sure to stop the count operation using the START bit in RCR2.

To read this counter, follow the procedure in section 23.3.5, Reading 64-Hz Counter and Time.

(2) In binary count mode:

Address(es): RTC.BCNT0 4004 4002h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNT[7:0]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

The BCNT0 counter is a read/write 32-bit binary counter b7 to b0 that performs count operation by a carry generated for each second of the 64-Hz counter. Before writing to this register, be sure to stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 23.3.5, Reading 64-Hz Counter and Time.

23.2.3 Minute Counter (RMINCNT)/Binary Counter 1 (BCNT1)

(1) In calendar count mode:

Address(es): RTC.RMINCNT 4004 4004h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	MIN10[2:0]			MIN1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	MIN1[3:0]	1-Minute Count	Counts from 0 to 9 every minute. When a carry is generated, 1 is added to the tens place.	R/W
b6 to b4	MIN10[2:0]	10-Minute Count	Counts from 0 to 5 for 60-minute counting	R/W
b7	—	Reserved	Set this bit to 0. It is read as the set value	R/W

The RMINCNT counter is used for setting and counting the BCD-coded minute value. It counts the carries generated once per minute in the second counter.

A value from 00 through 59 (in BCD) can be specified. If a value outside this range is specified, the RTC does not operate correctly. Before writing to this register, be sure to stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 23.3.5, Reading 64-Hz Counter and Time.

(2) In binary count mode:

Address(es): RTC.BCNT1 4004 4004h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNT[15:8]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

The BCNT1 counter is a read/write 32-bit binary counter b15 to b8 that performs count operation by a carry generated for each second of the 64-Hz counter. Before writing to this register, be sure to stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 23.3.5, Reading 64-Hz Counter and Time.

23.2.4 Hour Counter (RHRCNT)/Binary Counter 2 (BCNT2)

(1) In calendar count mode:

Address(es): RTC.RHRCNT 4004 4006h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	PM	HR10[1:0]		HR1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	HR1[3:0]	1-Hour Count	Counts from 0 to 9 once per hour. When a carry is generated, 1 is added to the tens place.	R/W
b5, b4	HR10[1:0]	10-Hour Count	Counts from 0 to 2 once per carry from the ones place	R/W
b6	PM	PM	Time Counter Setting for a.m./p.m: 0: a.m. 1: p.m.	R/W
b7	—	Reserved	Set this bit to 0. It is read as the set value.	R/W

The RHRCNT counter is used for setting and counting the BCD-coded hour value. It counts the carries generated once per hour in the minute counter. The specifiable time differs based on the setting in the hours mode bit (RCR2.HR24):

- When the RCR2.HR24 bit is 0 — from 00 to 11 (in BCD)
- When the RCR2.HR24 bit is 1 — from 00 to 23 (in BCD).

If a value outside this range is specified, the RTC does not operate correctly. Before writing to this register, be sure to stop the count operation using the START bit in RCR2. The PM bit is only enabled when the RCR2.HR24 bit is 0. Otherwise, the setting in the PM bit has no effect. To read this counter, follow the procedure in section 23.3.5, Reading 64-Hz Counter and Time.

(2) In binary count mode:

Address(es): RTC.BCNT2 4004 4006h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNT[23:16]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

The BCNT2 counter is a read/write 32-bit binary counter b23 to b16 that performs count operation by a carry generated for each second of the 64-Hz counter. Before writing to this register, be sure to stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 23.3.5, Reading 64-Hz Counter and Time.

23.2.5 Day-of-Week Counter (RWKCNT)/Binary Counter 3 (BCNT3)

(1) In calendar count mode:

Address(es): RTC.RWKCNT 4004 4008h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	DAYW[2:0]		
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b2 to b0	DAYW[2:0]	Day-of-Week Counting	b2 b0 0 0 0: Sunday 0 0 1: Monday 0 1 0: Tuesday 0 1 1: Wednesday 1 0 0: Thursday 1 0 1: Friday 1 1 0: Saturday 1 1 1: Setting prohibited.	R/W
b7 to b3	—	Reserved	Set these bits to 0. They are read as the set value.	R/W

The RWKCNT counter is used for setting and counting in the coded day-of-week value. It counts carries generated once per day in the hour counter. A value from 0 through 6 can be specified. If a value outside of this range is specified, the RTC does not operate correctly. Before writing to this register, be sure to stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 23.3.5, Reading 64-Hz Counter and Time.

(2) In binary count mode:

Address(es): RTC.BCNT3 4004 4008h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNT[31:24]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

The BCNT3 counter is a read/write 32-bit binary counter b31 to b24 that performs count operation by a carry generated for each second of the 64-Hz counter. Before writing to this register, be sure to stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 23.3.5, Reading 64-Hz Counter and Time.

23.2.6 Day Counter (RDAYCNT)

Address(es): RTC.RDAYCNT 4004 400Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	DATE10[1:0]		DATE1[3:0]			
Value after reset:	0	0	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	DATE1[3:0]	1-Day Count	Counts from 0 to 9 once per day. When a carry is generated, 1 is added to the tens place.	R/W
b5, b4	DATE10[1:0]	10-Day Count	Counts from 0 to 3 once per carry from the ones place	R/W

Bit	Symbol	Bit name	Description	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The RDAYCNT counter is used in calendar count mode. RDAYCNT is used for setting and counting the BCD-coded date value. It counts carries generated once per day in the hour counter. The count operation depends on the month and whether the year is a leap year. Leap years are determined according to whether the year counter (RYRCNT) value is divisible by 400, 100, and 4.

A value from 01 through 31 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. When specifying a value, the range of specifiable days depends on the month and whether the year is a leap year. Before writing to this register, be sure to stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 23.3.5, Reading 64-Hz Counter and Time.

23.2.7 Month Counter (RMONCNT)

Address(es): RTC.RMONCNT 4004 400Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	MON10	MON1[3:0]			
Value after reset:	0	0	0	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	MON1[3:0]	1-Month Count	Counts from 0 to 9 once per month. When a carry is generated, 1 is added to the tens place.	R/W
b4	MON10	10-Month Count	Counts from 0 to 1 once per carry from the ones place.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The RMONCNT counter is used in calendar count mode. RMONCNT is used for setting and counting the BCD-coded month value. It counts carries generated once per month in the date counter.

A value from 01 through 12 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. Before writing to this register, be sure to stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 23.3.5, Reading 64-Hz Counter and Time.

23.2.8 Year Counter (RYRCNT)

Address(es): RTC.RYRCNT 4004 400Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	YR10[3:0]				YR1[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	YR1[3:0]	1-Year Count	Counts from 0 to 9 once per year. When a carry is generated, 1 is added to the tens place.	R/W
b7 to b4	YR10[3:0]	10-Year Count	Counts from 0 to 9 once per carry from ones place. When a carry is generated in the tens place, 1 is added to the hundreds place.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The RYRCNT counter is used in calendar count mode. RYRCNT is used for setting and counting the BCD-coded year value. It counts the carries generated once per year in the month counter.

A value from 00 through 99 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. Before writing to this register, be sure to stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 23.3.5, Reading 64-Hz Counter and Time.

23.2.9 Second Alarm Register (RSECAR)/Binary Counter 0 Alarm Register (BCNT0AR)

(1) In calendar count mode:

Address(es): RTC.RSECAR 4004 4010h

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	SEC10[2:0]			SEC1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	SEC1[3:0]	1 Second	Value for the ones place of seconds	R/W
b6 to b4	SEC10[2:0]	10 Seconds	Value for the tens place of seconds	R/W
b7	ENB	ENB	0: The register value is not compared with the RSECCNT counter value 1: The register value is compared with the RSECCNT counter value.	R/W

RSECAR is an alarm register associated with the BCD-coded second counter RSECCNT. When the ENB bit is set to 1, the RSECAR value is compared with the RSECCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the associated counters:

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN.

When all the respective values match, the IR flag associated with the RTC_ALM interrupt is set to 1. The RSECAR values from 00 through 59 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. This register is set to 00h by an RTC software reset.

(2) In binary count mode:

Address(es): RTC.BCNT0AR 4004 4010h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTAR[7:0]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

The BCNT0AR counter is a read/write alarm register associated with the 32-bit binary counter b7 to b0. This register is set to 00h by an RTC software reset.

23.2.10 Minute Alarm Register (RMINAR)/Binary Counter 1 Alarm Register (BCNT1AR)

(1) In calendar count mode:

Address(es): RTC.RMINAR 4004 4012h

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	MIN10[2:0]			MIN1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	MIN1[3:0]	1 Minute	Value for the ones place of minutes	R/W
b6 to b4	MIN10[2:0]	10 Minutes	Value for the tens place of minutes	R/W
b7	ENB	ENB	0: The register value is not compared with the RMINCNT counter value 1: The register value is compared with the RMINCNT counter value	R/W

RMINAR is an alarm register associated with the BCD-coded minute counter RMINCNT. When the ENB bit is set to 1, the RMINAR value is compared with the RMINCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the associated counters:

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN.

When all the respective values match, the IR flag associated with the RTC_ALM interrupt is set to 1. The RMINAR values from 00 through 59 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. This register is set to 00h by an RTC software reset.

(2) In binary count mode:

Address(es): RTC.BCNT1AR 4004 4012h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTAR[15:8]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

The BCNT1AR counter is a read/write alarm register associated with the 32-bit binary counter from b15 to b8. This register is set to 00h by an RTC software reset.

23.2.11 Hour Alarm Register (RHRAR)/Binary Counter 2 Alarm Register (BCNT2AR)

(1) In calendar count mode:

Address(es): RTC.RHRAR 4004 4014h

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	PM	HR10[1:0]		HR1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	HR1[3:0]	1 Hour	Value for the ones place of hours	R/W
b5, b4	HR10[1:0]	10 Hours	Value for the tens place of hours	R/W
b6	PM	PM	Time Alarm Setting for a.m./p.m: 0: a.m. 1: p.m.	R/W
b7	ENB	ENB	0: The register value is not compared with the RHRCNT counter value 1: The register value is compared with the RHRCNT counter value.	R/W

RHRAR is an alarm register associated with the BCD-coded hour counter RHRCNT. When the ENB bit is set to 1, the RHRAR value is compared with the RHRCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the associated counters:

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN.

When all the respective values match, the IR flag associated with the RTC_ALM interrupt is set to 1. The specifiable time differs according to the setting in the hours mode bit (RCR2.HR24):

- When the RCR2.HR24 bit is 0 — From 00 to 11 (in BCD)
- When the RCR2.HR24 bit is 1 — From 00 to 23 (in BCD).

If a value outside of this range is specified, the RTC does not operate correctly. When the RCR2.HR24 bit is 0, be sure to set the PM bit. When the RCR2.HR24 bit is 1, the setting in the PM bit has no effect. This register is set to 00h by an RTC software reset.

(2) In binary count mode:

Address(es): RTC.BCNT2AR 4004 4014h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTAR[23:16]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

The BCNT2AR counter is a read/write alarm register that corresponds to the 32-bit binary counter b23 to b16. This register is set to 00h by an RTC software reset.

23.2.12 Day-of-Week Alarm Register (RWKAR)/Binary Counter 3 Alarm Register (BCNT3AR)

(1) In calendar count mode:

Address(es): RTC.RWKAR 4004 4016h

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	—	—	—	—	DAYW[2:0]		
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b2 to b0	DAYW[2:0]	Day-of-Week Setting	b2 b0 0 0 0: Sunday 0 0 1: Monday 0 1 0: Tuesday 0 1 1: Wednesday 1 0 0: Thursday 1 0 1: Friday 1 1 0: Saturday 1 1 1: Setting prohibited.	R/W
b6 to b3	—	Reserved	Set these bits to 0. They are read as the set value.	R/W
b7	ENB	ENB	0: The register value is not compared with the RWKCNT counter value 1: The register value is compared with the RWKCNT counter value	R/W

RWKAR is an alarm register associated with the coded day-of-week counter RWKCNT. When the ENB bit is set to 1, the RWKAR value is compared with the RWKCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the associated counters:

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN.

When all the respective values all match, the IR flag associated with the RTC_ALM interrupt is set to 1. The RWKAR values from 0 through 6 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. This register is set to 00h by an RTC software reset.

(2) In binary count mode:

Address(es): RTC.BCNT3AR 4004 4016h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTAR[31:24]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

The BCNT3AR counter is a read/write alarm register associated with the 32-bit binary counter b31 to b24. This register is set to 00h by an RTC software reset.

23.2.13 Date Alarm Register (RDAYAR)/Binary Counter 0 Alarm Enable Register (BCNT0AER)

(1) In calendar count mode:

Address(es): RTC.RDAYAR 4004 4018h

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	—	DATE10[1:0]		DATE1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	DATE1[3:0]	1 Day	Value for the ones place of days	R/W
b5, b4	DATE10[1:0]	10 Days	Value for the tens place of days	R/W
b6	—	Reserved	Set this bit to 0. It is read as the set value.	R/W
b7	ENB	ENB	0: The register value is not compared with the RDAYCNT counter value 1: The register value is compared with the RDAYCNT counter value.	R/W

RDAYAR is an alarm register associated with the BCD-coded date counter RDAYCNT. When the ENB bit is set to 1, the RDAYAR value is compared with the RDAYCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the associated counters:

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN.

When all the respective values match, the IR flag associated with the RTC_ALM interrupt is set to 1. The RDAYAR values from 01 through 31 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. This register is set to 00h by an RTC software reset.

(2) In binary count mode:

Address(es): RTC.BCNT0AER 4004 4018h

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB[7:0]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

The BCNT0AER register is a read/write register for setting the alarm enable associated with the 32-bit binary counter b7 to b0. The binary counter (BCNT[31:0]) associated with the ENB[31:0] bits that are set to 1 is compared with the binary alarm register (BCNTAR[31:0]), and when all match, the IR flag associated with the RTC_ALM interrupt becomes 1. This register is set to 00h by an RTC software reset.

23.2.14 Month Alarm Register (RMONAR)/Binary Counter 1 Alarm Enable Register (BCNT1AER)

(1) In calendar count mode:

Address(es): RTC.RMONAR 4004 401Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	—	—	MON10	MON1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	MON1[3:0]	1 Month	Value for the ones place of months	R/W
b4	MON10	10 Months	Value for the tens place of months	R/W
b6, b5	—	Reserved	Set these bits to 0. They are read as the set value.	R/W
b7	ENB	ENB	0: The register value is not compared with the RMONCNT counter value 1: The register value is compared with the RMONCNT counter value.	R/W

RMONAR is an alarm register associated with the BCD-coded month counter RMONCNT. When the ENB bit is set to 1, the RMONAR value is compared with the RMONCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the associated counters:

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN.

When all the respective values match, the IR flag associated with the RTC_ALM interrupt is set to 1. The RMONAR values from 01 through 12 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. This register is set to 00h by an RTC software reset.

(2) In binary count mode:

Address(es): RTC.BCNT1AER 4004 401Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB[15:8]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

The BCNT1AER register is a read/write register for setting the alarm enable associated with the 32-bit binary counter b15 to b8. The binary counter (BCNT[31:0]) associated with the ENB[31:0] bits that are set to 1 is compared with the binary alarm register (BCNTAR[31:0]), and when all match, the IR flag associated with the RTC_ALM interrupt becomes 1. This register is set to 00h by an RTC software reset.

23.2.15 Year Alarm Register (RYRAR)/Binary Counter 2 Alarm Enable Register (BCNT2AER)

(1) In calendar count mode:

Address(es): RTC.RYRAR 4004 401Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	YR10[3:0]				YR1[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	YR1[3:0]	1 Year	Value for the ones place of years	R/W
b7 to b4	YR10[3:0]	10 Years	Value for the tens place of years	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RYRAR is an alarm register associated with the BCD-coded year counter RYRCNT. The RYRAR values from 00 through 99 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. This register is set to 0000h by an RTC software reset.

(2) In binary count mode:

Address(es): RTC.BCNT2AER 4004 401Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	ENB[23:16]							
Value after reset:	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

x: Undefined

The BCNT2AER register is a read/write register for setting the alarm enable associated with the 32-bit binary counter b23 to b16. The binary counter (BCNT[31:0]) associated with the ENB[31:0] bits that are set to 1 is compared with the binary alarm register (BCNTAR[31:0]), and when all match, the IR flag associated with the RTC_ALM interrupt becomes 1. This register is set to 0000h by an RTC software reset.

23.2.16 Year Alarm Enable Register (RYRAREN)/ Binary Counter 3 Alarm Enable Register (BCNT3AER)

(1) In calendar count mode:

Address(es): RTC.RYRAREN 4004 401Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	—	—	—	—	—	—	—
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b6 to b0	—	Reserved	Set these bits to 0. They are read as the set value.	R/W
b7	ENB	ENB	0: The register value is not compared with the RYRCNT counter value 1: The register value is compared with the RYRCNT counter value.	R/W

When the ENB bit in RYRAREN is set to 1, the RYRAR value is compared with the RYRCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the associated counters:

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN.

When all the respective values match, the IR flag associated with the RTC_ALM interrupt is set to 1.This register is set to 00h by an RTC software reset.

(2) In binary count mode:

Address(es): RTC.BCNT3AER 4004 401Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB[31:24]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

The BCNT3AER register is a read/write register for setting the alarm enable associated with the 32-bit binary counter b31 to b24. The binary counter (BCNT[31:0]) associated with the ENB[31:0] bits that are set to 1 is compared with the binary alarm register (BCNTAR[31:0]), and when all match, the IR flag associated with the RTC_ALM interrupt becomes 1. This register is set to 00h by an RTC software reset.

23.2.17 RTC Control Register 1 (RCR1)

Address(es): RTC.RCR1 4004 4022h

	b7	b6	b5	b4	b3	b2	b1	b0
	PES[3:0]				RTCOS	PIE	CIE	AIE
Value after reset:	x	x	x	x	0	x	0	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	AIE	Alarm Interrupt Enable	0: Disable alarm interrupt requests 1: Enable alarm interrupt requests.	R/W
b1	CIE	Carry Interrupt Enable	0: Disable carry interrupt requests 1: Enable carry interrupt requests.	R/W
b2	PIE	Periodic Interrupt Enable	0: Disable periodic interrupt requests 1: Enable periodic interrupt requests.	R/W
b3	RTCOS	RTCOUT Output Select	0: Outputs 1 Hz on RTCOUT 1: Outputs 64 Hz on RTCOUT.	R/W

Bit	Symbol	Bit name	Description	R/W
b7 to b4	PES[3:0]	Periodic Interrupt Select	b7 b4 0 1 1 0: A periodic interrupt is generated every 1/256 second*1 0 1 1 1: A periodic interrupt is generated every 1/128 second 1 0 0 0: A periodic interrupt is generated every 1/64 second 1 0 0 1: A periodic interrupt is generated every 1/32 second 1 0 1 0: A periodic interrupt is generated every 1/16 second 1 0 1 1: A periodic interrupt is generated every 1/8 second 1 1 0 0: A periodic interrupt is generated every 1/4 second 1 1 0 1: A periodic interrupt is generated every 1/2 second 1 1 1 0: A periodic interrupt is generated every 1 second 1 1 1 1: A periodic interrupt is generated every 2 seconds. No periodic interrupts are generated for other settings.	R/W

Note 1. When LOCO is selected (RCR4.RCKSEL = 1) while PES[3:0] = 0110b, a periodic interrupt is generated every 1/128 second.

The RCR1 register is used in both calendar count mode and binary count mode. Bits AIE, PIE, and PES[3:0] are updated synchronously with the count source. When the RCR1 register is modified, check that all the bits are updated before proceeding.

AIE bit (Alarm Interrupt Enable)

The AIE bit enables or disables alarm interrupt requests.

CIE bit (Carry Interrupt Enable)

The CIE bit enables and disables interrupt requests when a carry to the RSECCNT/BCNT0 register occurs, or when a carry to the 64-Hz counter (R64CNT) occurs while reading the 64-Hz counter.

PIE bit (Periodic Interrupt Enable)

The PIE bit enables or disabled a periodic interrupt.

RTCOS bit (RTCOUT Output Select)

The RTCOS bit selects the RTCOUT output period. The RTCOS bit must be rewritten while the count operation is stopped (the RCR2.START bit is 0) and the RTCOUT output is disabled (the RCR2.RTCOE bit is 0). When the RTCOUT is output to an external pin, the RCR2.RTCOE bit must be enabled. For details on controlling I/O ports, see section 17.5.1, Procedure for Specifying Pin Function.

PES[3:0] bits (Periodic Interrupt Select)

The PES[3:0] bits specify the period of the periodic interrupt. A periodic interrupt is generated with the period specified by these bits.

23.2.18 RTC Control Register 2 (RCR2)

(1) In calendar count mode:

Address(es): RTC.RCR2 4004 4024h

	b7	b6	b5	b4	b3	b2	b1	b0
	CNTMD	HR24	AADJP	AADJE	RTCOE	ADJ30	RESET	START
Value after reset:	x	x	x	x	0	0	0	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	START	Start	0: Stop prescaler and time counter 1: Operate prescaler and time counter normally.	R/W

Bit	Symbol	Bit name	Description	R/W
b1	RESET	RTC Software Reset	• In writing: 0: Writing is invalid 1: The prescaler and the target registers for RTC software reset *1 are initialized. • In reading: 0: Normal time operation in progress, or an RTC software reset has completed 1: RTC software reset in progress.	R/W
b2	ADJ30	30-Second Adjustment	• In writing: 0: Writing is invalid 1: 30-second adjustment is executed. • In reading: 0: Normal time operation in progress, or 30-second adjustment has completed 1: 30-second adjustment in progress.	R/W
b3	RTCOE	RTCOUT Output Enable	0: Disable RTCOUT output 1: Enable RTCOUT output.	R/W
b4	AADJE	Automatic Adjustment Enable*2	0: Disable automatic adjustment 1: Enable automatic adjustment.	R/W
b5	AADJP	Automatic Adjustment Period Select*2	0: Adjust RADJ.ADJ[5:0] setting from the count value of the prescaler every minute 1: Adjust RADJ.ADJ[5:0] setting from the count value of the prescaler every 10 seconds.	R/W
b6	HR24	Hours Mode	0: Operate RTC in 12-hour mode 1: Operate RTC in 24-hour mode.	R/W
b7	CNTMD	Count Mode Select	0: Calendar count mode 1: Binary count mode.	R/W

Note 1. R64CNT, RSECAR/BCNT0AR, RMINAR/BCNT1AR, RHRAR/BCNT2AR, RWKAR/BCNT3AR, RDAYAR/BCNT0AER, RMONAR/BCNT1AER, RYRAR/BCNT2AER, RYRAREN/BCNT3AER, RADJ, RCR2.ADJ30, RCR2.AADJE, RCR2.AADJP.
Note 2. When LOCO is selected, the setting of this bit is disabled.

The RCR2 register is related to hours mode, automatic adjustment function, enabling of RTCOUT output, 30-second adjustment, RTC software reset, and controlling count operation.

START bit (Start)

The START bit stops or restarts the prescaler or time counter operation.

The START bit is updated in synchronization with the next cycle of the count source. When the START bit is modified, check that the bit is updated before proceeding.

RESET bit (RTC Software Reset)

The RESET bit initializes the prescaler and registers to be reset by RTC software.

When 1 is written to the RESET bit, initialization starts in synchronization with the count source. When the initialization completes, the RESET bit is automatically set to 0. Check that this bit is set to 0 before proceeding.

ADJ30 bit (30-Second Adjustment)

The ADJ30 bit is for the 30-second adjustment.

When 1 is written to the ADJ30 bit, the RSECCNT value of 30 seconds or less is rounded down to 00 second and the value of 30 seconds or more is rounded up to 1 minute.

The 30-second adjustment is performed in synchronization with the count source. When 1 is written to this bit, the ADJ30 bit is automatically set to 0 after the 30-second adjustment completes. If 1 is written to the ADJ30 bit, check that the bit is set to 0 before proceeding. When the 30-second adjustment is performed, the prescaler and R64CNT are also reset. The ADJ30 bit is set to 0 by an RTC software reset.

RTCOE bit (RTCOUT Output Enable)

The RTCOE bit enables output of a 1-Hz/64-Hz clock signal from the RTCOUT pin.

Use the START bit to stop counting before changing the value of the RTCOE bit. Do not stop counting (write 0 to the

START bit) and change the value of the RTCOE bit at the same time.

When RTCOUT is to be output from an external pin, enable the RTCOE bit and set up the port control for the pin.

AADJE bit (Automatic Adjustment Enable)

The AADJE bit controls (enables or disables) automatic adjustment.

Set the plus-minus bits (RADJ.PMADJ[1:0]) to 00b (adjustment is not performed) before changing the value of the AADJE bit.

The AADJE bit is set to 0 by an RTC software reset.

AADJP bit (Automatic Adjustment Period Select)

The AADJP bit selects the automatic-adjustment period.

Set the plus-minus bits (RADJ.PMADJ[1:0]) to 00b (adjustment is not performed) before changing the value of the AADJP bit.

The AADJP bit is set to 0 by an RTC software reset.

HR24 bit (Hours Mode)

The HR24 bit specifies whether the RTC operates in 12- or 24-hour mode.

Use the START bit to stop counting before changing the value of the HR24 bit. Do not stop counting (write 0 to the START bit) and change the value of the HR24 bit at the same time.

CNTMD bit (Count Mode Select)

The CNTMD bit specifies whether the RTC count mode operates in calendar count mode or in binary count mode.

When setting the count mode, execute an RTC software reset and start again from the initial settings. This bit is updated synchronously with the count source, and its value is fixed before the RTC software reset is complete.

For details on initial settings, see section 23.3.1, Outline of Initial Settings of Registers after Power On.

(2) In binary count mode:

Address(es): RTC.RCR2 4004 4024h

	b7	b6	b5	b4	b3	b2	b1	b0
	CNTMD	—	AADJP	AADJE	RTCOE	—	RESET	START
Value after reset:	x	x	x	x	0	0	0	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	START	Start	0: Stop the 32-bit binary counter, 64-Hz counter, and prescaler 1: Operate 32-bit binary counter, 64-Hz counter, and prescaler normally.	R/W
b1	RESET	RTC Software Reset	• In writing: 0: Writing is invalid. 1: The prescaler and the target registers for RTC software reset*1 are initialized. • In reading: 0: In normal time operation, or an RTC software reset has completed. 1: During an RTC software reset.	R/W
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b3	RTCOE	RTCOUT Output Enable	0: Disable RTCOUT output 1: Enable RTCOUT output.	R/W
b4	AADJE	Automatic Adjustment Enable*2	0: Disable automatic adjustment 1: Enable automatic adjustment.	R/W

Bit	Symbol	Bit name	Description	R/W
b5	AADJP	Automatic Adjustment Period Select*2	0: Add or subtract the RADJ.ADJ[5:0] bits from the prescaler count value every 32 seconds 1: Add or subtract the RADJ.ADJ[5:0] bits from the prescaler count value every 8 seconds.	R/W
b6	—	Reserved	This bit is undefined. The write value should be 0.	R/W
b7	CNTMD	Count Mode Select	0: The calendar count mode 1: The binary count mode.	R/W

Note 1. R64CNT, RSECAR/BCNT0AR, RMINAR/BCNT1AR, RHRAR/BCNT2AR, RWKAR/BCNT3AR, RDAYAR/BCNT0AER, RMONAR/BCNT1AER, RYRAR/BCNT2AER, RYRAREN/BCNT3AER, RADJ, RCR2.ADJ30, RCR2.AADJE, RCR2.AADJP

Note 2. When LOCO is selected, the setting of this bit is disabled.

START bit (Start)

The START bit stops or restarts the prescaler or counter (clock) operation.

The START bit is updated in synchronization with the count source. When the START bit is modified, check that the bit is updated before proceeding.

RESET bit (RTC Software Reset)

The RESET bit initializes the prescaler and registers to be reset by RTC software.

When 1 is written to the RESET bit, initialization starts in synchronization with the count source. When the initialization completes, the RESET bit is automatically set to 0. When 1 is written to the RESET bit, check that the bit is set to 0 before proceeding.

RTCOE bit (RTCOUT Output Enable)

The RTCOE bit enables output of a 1-Hz/64-Hz clock signal from the RTCOUT pin.

Use the START bit to stop counting before changing the value of the RTCOE bit. Do not stop counting (write 0 to the START bit) and change the value of the RTCOE bit at the same time. When an RTCOUT signal is output from an external pin, enable the port control in addition to setting this bit.

AADJE bit (Automatic Adjustment Enable)

The AADJE bit controls (enables or disables) automatic adjustment.

Set the plus-minus bits (RADJ.PMADJ[1:0]) to 00b (adjustment is not performed) before changing the value of the AADJE bit. The AADJE bit is set to 0 by an RTC software reset.

AADJP bit (Automatic Adjustment Period Select)

The AADJP bit selects the automatic-adjustment period.

Correction period can be selected from 32 second units or 8 second units in binary count mode.

Set the plus-minus bits (RADJ.PMADJ[1:0]) to 00b (adjustment is not performed) before changing the value of the AADJP bit. The AADJP bit is set to 0 by an RTC software reset.

CNTMD bit (Count Mode Select)

The CNTMD bit specifies whether the RTC count mode operates in calendar count mode or in binary count mode.

When setting the count mode, execute an RTC software reset and start again from the initial settings. This bit is updated synchronously with the count source, and its value is fixed before the RTC software reset is complete.

For details on initial settings, see section 23.3.1, Outline of Initial Settings of Registers after Power On.

23.2.19 RTC Control Register 4 (RCR4)

Address(es): RTC.RCR4 4004 4028h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	RCKSEL
Value after reset:	0	0	0	0	0	0	0	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	RCKSEL	Count Source Select	0: Sub-clock oscillator is selected. 1: LOCO is selected.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The RCR4 register is used for selecting the count source. This function is used in both calendar count mode and binary count mode. When the RCKSEL bit is set to 0, the time is counted with the sub-clock oscillator. When the bit is set to 1, the time is counted with LOCO.

RCKSEL bit (Count Source Select)

The RCKSEL bit selects the count source from the sub-clock oscillator and LOCO.

The count source must be selected only once before making the initial settings of the RTC registers at power on.

23.2.20 Frequency Register (RFRH/RFRL)

Address(es): RTC.RFRH 4004 402Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RFC16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	RFC16	Reserved	Write 0 before writing to the RFRL register after a cold start	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Address(es): RTC.RFRL 4004 402Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RFC[15:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b15 to b0	RFC[15:0]	Frequency Comparison Value	Write 00FFh to this register when using the LOCO	R/W

RFRL is a register for controlling the prescaler when LOCO is selected.

The RTC time counter operates on a 128-Hz clock signal as the base clock. Therefore, when LOCO is selected, LOCO is

divided by the prescaler to generate a 128-Hz clock signal. Set the frequency comparison value in the RFC[15:0] bits to generate a 128-Hz clock from the LOCO frequency. Before first writing to RFC[15:0] after cold start, write 0000h to the RFRH.

A value from 0007h through 01FFh can be specified as the frequency comparison value. If a value outside of this range is specified, the RTC does not operate correctly. Before writing to this register, be sure to stop the count operation through the setting of the START bit in RCR2. The operating frequency of the peripheral module clock and the LOCO should be such that the peripheral module clock >= LOCO.

Calculation method of frequency comparison value:

RFC[15:0] = (LOCO clock frequency) / 128 - 1

When the LOCO frequency is 32.768 kHz, the RFRL register must be set to 00FFh.

23.2.21 Time Error Adjustment Register (RADJ)

Address(es): RTC.RADJ 4004 402Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	PMADJ[1:0]		ADJ[5:0]					
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b5 to b0	ADJ[5:0]	Adjustment Value	These bits specify the adjustment value from the prescaler	R/W
b7, b6	PMADJ[1:0]	Plus-Minus	b7 b6 0 0: Adjustment is not performed 0 1: Adjustment is performed by the addition to the prescaler 1 0: Adjustment is performed by the subtraction from the prescaler 1 1: Setting prohibited.	R/W

Adjustment is performed by the addition to or subtraction from the prescaler. If the automatic adjustment enable (RCR2.AADJE) bit is 0, adjustment is performed when writing to the RADJ. If the RCR2.AADJE bit is 1, adjustment is performed in the interval specified by the automatic adjustment period select (RCR2.AADJP) bit.

The current adjustment by software (disabling automatic adjustment) might be invalid if the subsequent adjustment value is specified within 320 cycles of the count source after the register setting. To perform adjustment consecutively, wait for 320 cycles or more of the count source after the register setting, then specify the next adjustment value.

RADJ is updated in synchronization with the count source. When RADJ is modified, check that all the bits are updated before continuing with more processing. This register is set to 00h by an RTC software reset. The setting of this register is enabled only when the sub-clock oscillator is selected. When LOCO is selected, adjustment is not performed.

ADJ[5:0] bits (Adjustment Value)

The ADJ[5:0] bits specify the adjustment value (the number of sub-clock cycles) from the prescaler.

PMADJ[1:0] bits (Plus-Minus)

The PMADJ[1:0] bits select whether the clock is set ahead or back depending on the error-adjustment value set in the ADJ[5:0] bits.

23.3 Operation

23.3.1 Outline of Initial Settings of Registers after Power On

On power on, perform the initial settings for the clock setting, count mode setting, time error adjustment, time setting, alarm, and interrupt control register.

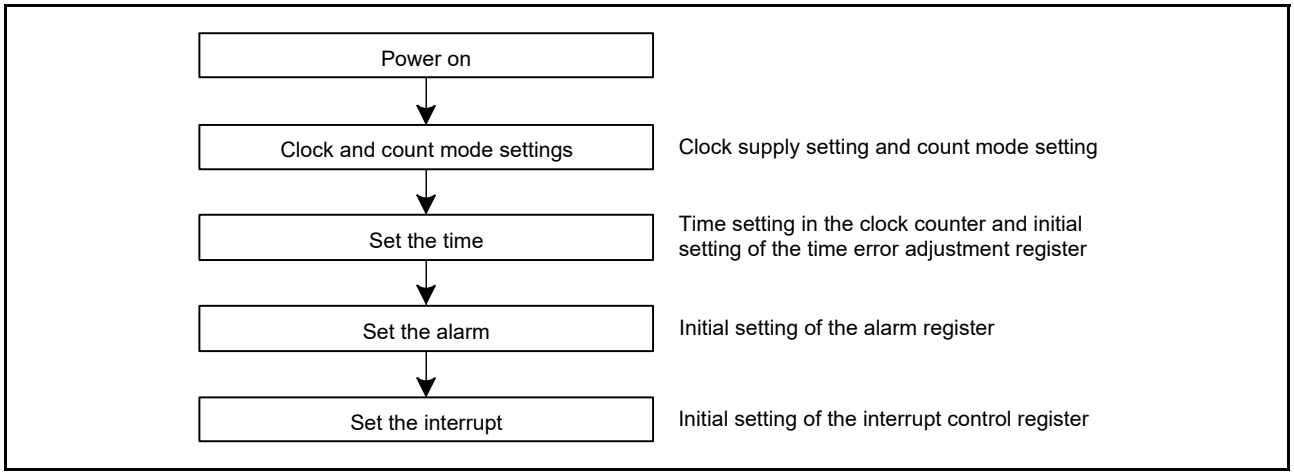


Figure 23.2 Outline of initial settings after a power on

23.3.2 Clock and Count Mode Setting Procedure

Figure 23.3 shows how to set the clock and the count mode.

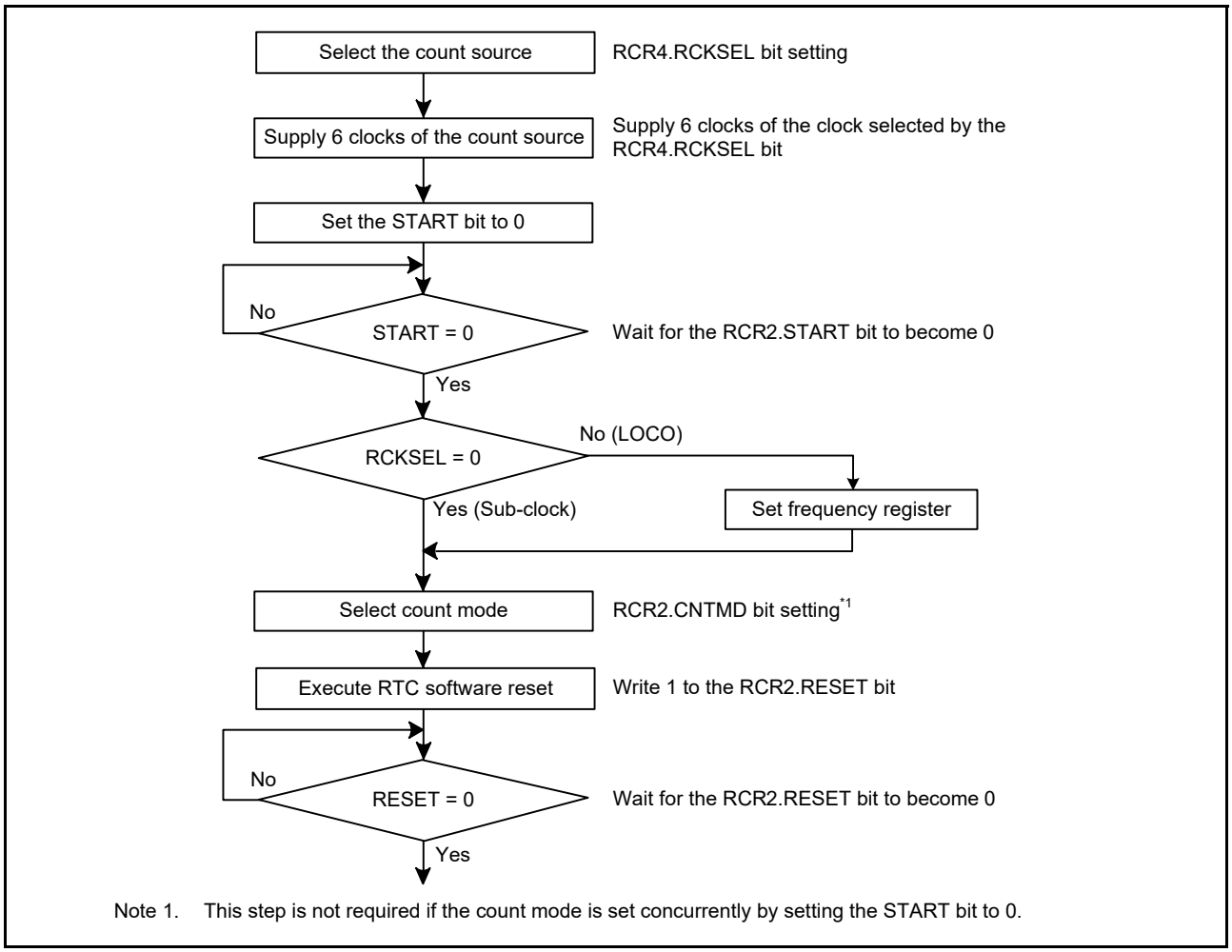


Figure 23.3 Clock and count mode setting procedure

23.3.3 Setting the Time

Figure 23.4 shows how to set the time.

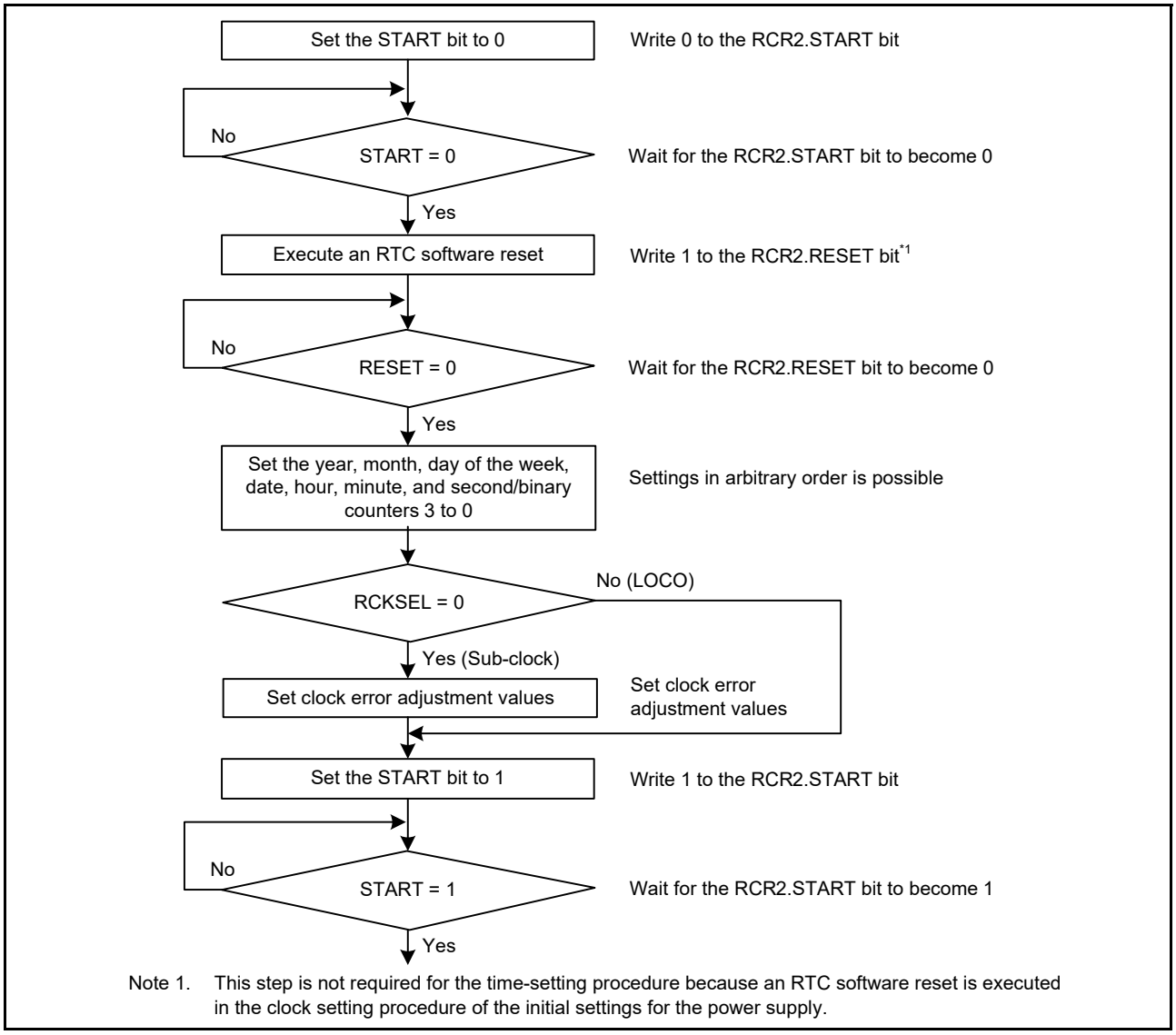


Figure 23.4 Setting the time

23.3.4 30-Second Adjustment

Figure 23.5 shows how to execute a 30-second adjustment.

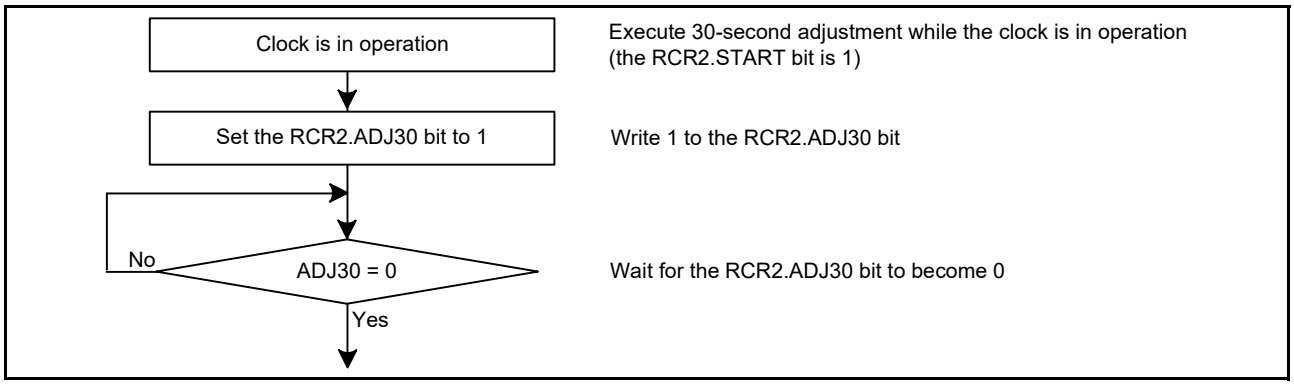


Figure 23.5 30-second adjustment

23.3.5 Reading 64-Hz Counter and Time

Figure 23.6 shows how to read a 64-Hz counter and time.

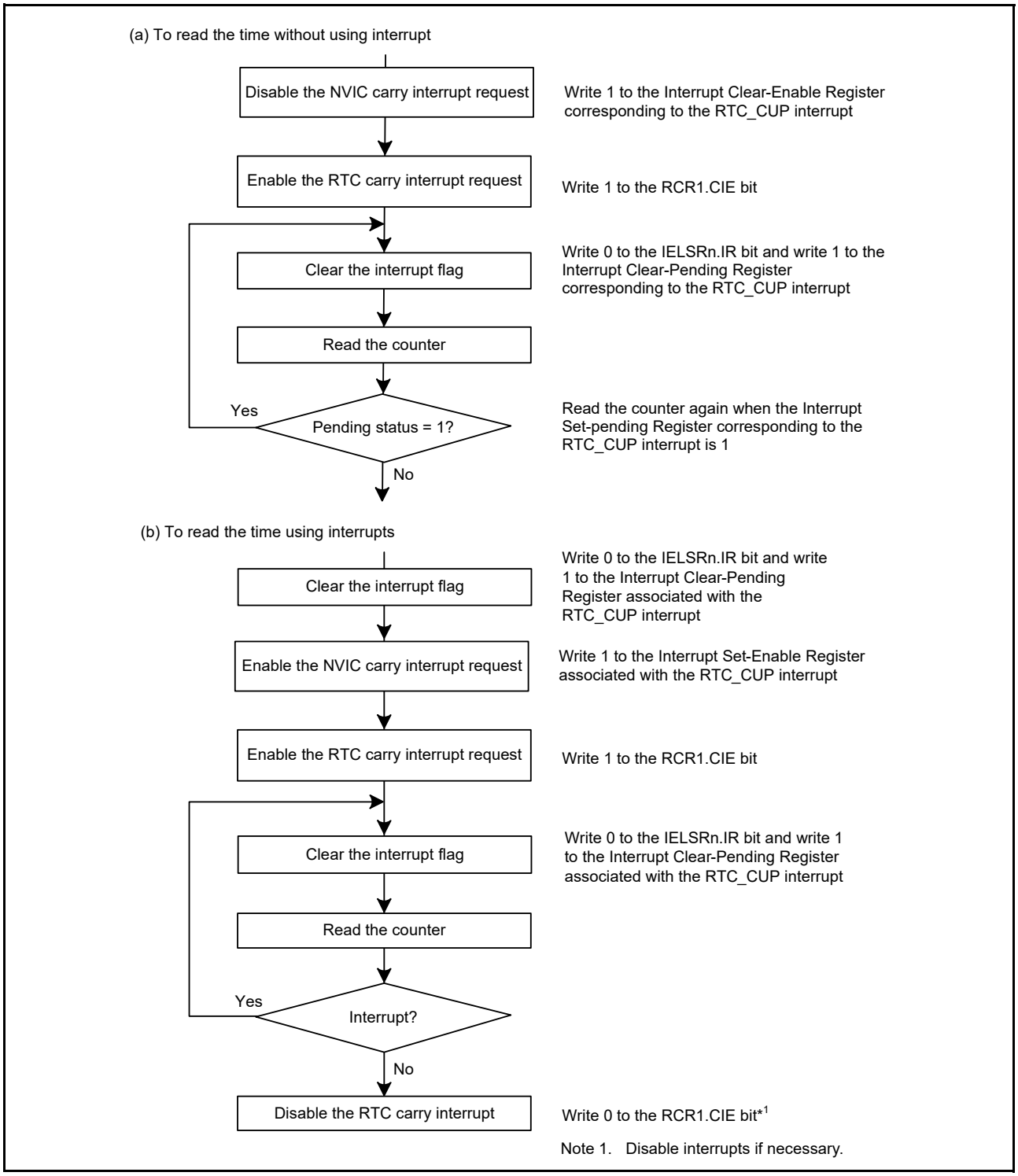


Figure 23.6 Reading time

If a carry occurs while the 64-Hz counter and time are read, the correct time is not obtained, therefore they must be read again. The procedure for reading the time without using interrupts is shown in (a) in Figure 23.6, and the procedure using carry interrupts is shown in (b). To keep the program simple, method (a) should be used in most cases.

23.3.6 Alarm Function

Figure 23.7 shows how to use the alarm function.

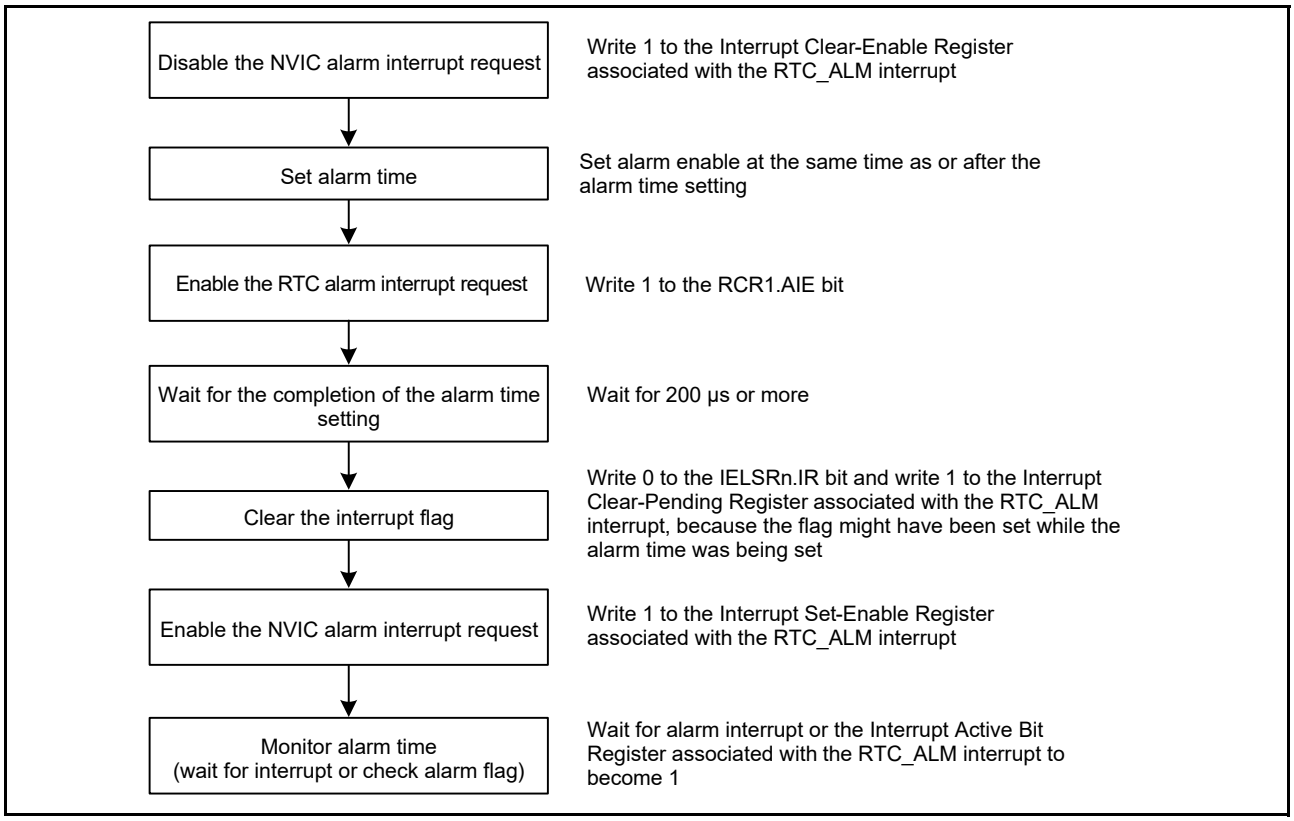


Figure 23.7 Using the alarm function

In calendar count mode, an alarm can be generated by any one of year, month, date, day-of-week, hour, minute or second, or any combination of those. Write 1 to the ENB bit in the alarm registers involved in the alarm setting, and set the alarm time in the lower bits. Write 0 to the ENB bit in registers not involved in the alarm setting.

In binary count mode, an alarm can be generated in any bit combination of 32 bits. Write 1 to the ENB bit of the alarm enable register associated with the target bit of the alarm, and set the alarm time in the alarm register. For bits that are not the target of the alarm, write 0 to the ENB bit of the Alarm Enable register.

When the counter and the alarm time match, the IELSRn.IR bit and Interrupt Set-Pending/Clear-Pending Register associated with the RTC_ALM interrupt are set to 1. Alarm detection can be confirmed by reading the Interrupt Set-Pending Register associated with the RTC_ALM interrupt, but an interrupt should be used in most cases. If 1 is set in the Interrupt Set-Enable Register and Interrupt Active Bit Register associated with the RTC_ALM interrupt, an alarm interrupt is generated in the event of the alarm, enabling the alarm to be detected.

Writing 0 sets the IELSRn.IR bit associated with the RTC_ALM interrupt to 0. If interrupt is enabled, the Interrupt Set-Pending/Clear-Pending Register and Interrupt Active Bit Register associated with the RTC_ALM interrupt is cleared automatically after exiting the interrupt handler. Otherwise, write 1 to the Interrupt Clear-Pending Register associated with the RTC_ALM interrupt to clear it.

When the counter and the alarm time match in a low power state, the MCU returns from the low power state.

23.3.7 Procedure for Disabling Alarm Interrupt

Figure 23.8 shows the procedure for disabling an enabled alarm interrupt request.

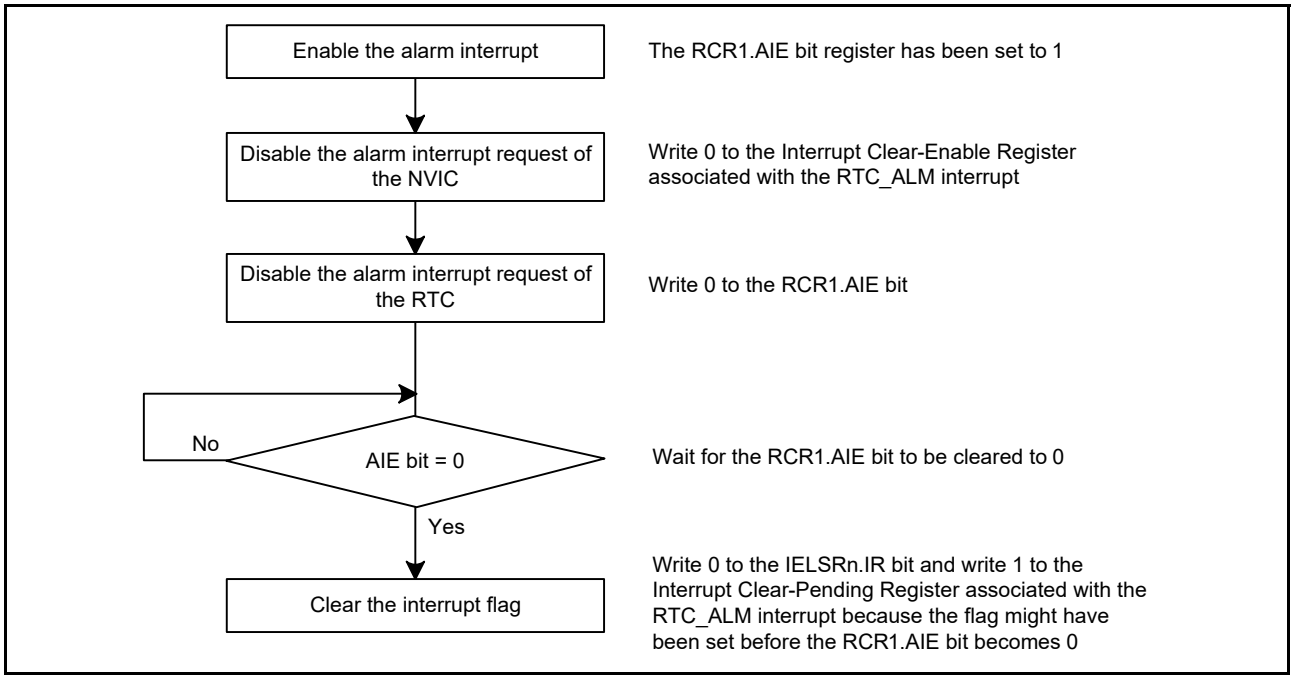


Figure 23.8 Procedure for disabling alarm interrupt request

23.3.8 Time Error Adjustment Function

The time error adjustment function is used to correct errors, running fast or slow, in the time caused by variation in the precision of oscillation by the sub-clock oscillator. Because 32,768 cycles of the sub-clock oscillator constitute 1 second of operation when the sub-clock oscillator is selected, the clock runs fast if the sub-clock frequency is high and slow if the sub-clock frequency is low.

The time error adjustment functions include:

- Automatic adjustment
- Adjustment by software.

Use the RCR2.AADJE bit to select automatic adjustment or adjustment by software.

23.3.8.1 Automatic adjustment

Enable automatic adjustment by setting the RCR2.AADJE bit to 1. Automatic adjustment is the addition or subtraction of the value counted by the prescaler to or from the value in the RADJ register every time the adjustment period selected by the RCR2.AADJP bit elapses.

(1) Example 1 sub-clock oscillator running at 32.769 kHz

(a) Adjustment procedure

When the sub-clock oscillator is running at 32.769 kHz, 1 second elapses in every 32,769 clock cycles. The RTC is meant to run at 32,768 clock cycles, so the clock runs fast by 1 clock cycle every second. The time on the clock is fast by 60 clock cycles per minute, so adjustment can take the form of setting the clock back by 60 cycles every minute.

Register settings when RCR2.CNTMD = 0:

- RCR2.AADJP = 0 (adjustment every minute)
- RADJ.PMADJ[1:0] = 10b (adjustment is performed by the subtraction from the prescaler)
- RADJ.ADJ[5:0] = 60 (3Ch).

(2) Example 2 sub-clock oscillator running at 32.766 kHz

(a) Adjustment procedure

When the sub-clock oscillator runs at 32.766 kHz, 1 second elapses in every 32,766 clock cycles. The RTC is meant to run at 32,768 clock cycles, so the clock runs slow by 2 clock cycles every second. The time on the clock is slow by 20 clock cycles every 10 seconds, so adjustment can take the form of setting the clock forward by 20 cycles every 10 seconds.

Register settings when RCR2.CNTMD is 0 (calendar count mode):

- RCR2.AADJP = 1 (adjustment every 10 seconds)
- RADJ.PMADJ[1:0] = 01b (adjustment is performed by the addition to the prescaler)
- RADJ.ADJ[5:0] = 20 (14h).

(3) Example 3 Sub-clock oscillator running at 32.764 kHz

(a) Adjustment procedure

When the sub-clock oscillator runs at 32.764 kHz, 1 second elapses on 32,764 clock cycles. Because the RTC operates for 32,768 clock cycles as 1 second, the clock is delayed for 4 clock cycles per second. In 8 seconds, the delay is 32 clock cycles, therefore correction can be made by setting the clock for 32 clock cycles every 8 seconds.

Register settings when the RCR2.CNTMD bit is 1 (binary count mode):

- RCR2.AADJP = 1 (adjustment every 8 seconds)
- RADJ.PMADJ[1:0] = 01b (adjustment is performed by the addition to the prescaler)
- RADJ.ADJ[5:0] = 32 (20h).

23.3.8.2 Adjustment by software

Enable adjustment by software by setting the RCR2.AADJE bit to 0. Adjustment by software is the addition or subtraction of the value counted by the prescaler to or from the value in the RADJ register at the time of execution of a write instruction to the RADJ register.

(1) Example 1 sub-clock oscillator running at 32.769 kHz

(a) Adjustment procedure

When the sub-clock oscillator is running at 32.769 kHz, 1 second elapses every 32,769 clock cycles. The RTC is meant to run at 32,768 clock cycles, so the clock runs fast by one clock cycle every second. The time on the clock is fast by one clock cycle per second, so adjustment can take the form of setting the clock back by one cycle every second.

(b) Register settings

- RADJ.PMADJ[1:0] = 10b (adjustment is performed by the subtraction from the prescaler)
- RADJ.ADJ[5:0] = 1 (01h)
  This is written to the RADJ register once per 1-second interrupt.

23.3.8.3 Procedure to change the mode of adjustment

When changing the mode of adjustment, change the value of the AADJE bit in RCR2 after setting the RADJ.PMADJ[1:0] bits to 00b (adjustment is not performed).

To change adjustment by software to automatic adjustment:

1. Set the RADJ.PMADJ[1:0] bits to 00b (adjustment is not performed).
2. Set the RCR2.AADJE bit to 1 (automatic adjustment is enabled).
3. Use the RCR2.AADJP bit to select the period of adjustment.
4. In RADJ, set the PMADJ[1:0] bits for addition or subtraction and the ADJ[5:0] bits to the value for use in time error adjustment.

To change automatic adjustment to adjustment by software:

1. Set the RADJ.PMADJ[1:0] bits to 00b (adjustment is not performed).
2. Set the RCR2.AADJE bit to 0 (adjustment by software is enabled).
3. Proceed with the adjustment by setting the RADJ.PMADJ[1:0] bits for addition or subtraction and the RADJ.ADJ[5:0] bits to the value for use in time error adjustment at the desired time. After that, the time is adjusted every time a value is written to the RADJ register.

23.3.8.4 Procedure to stop adjustment

Stop the adjustment by setting the RADJ.PMADJ[1:0] bits to 00b (adjustment is not performed).

23.4 Interrupt Sources

The RTC has three interrupt sources and are listed in Table 23.3.

Table 23.3 RTC interrupt sources

Name	Interrupt sources
RTC_ALM	Alarm interrupt
RTC_PRD	Periodic interrupt
RTC_CUP	Carry interrupt

(1) Alarm interrupt (RTC_ALM)

This interrupt is generated based on the comparison result between the alarm registers and RTC counters. For details, see section 23.3.6, Alarm Function.

Because there is a possibility that the interrupt flag might be set to 1 when the settings of the alarm registers match the clock counters, wait for the alarm time settings to be confirmed. Clear the IELSRn.IR bit and the Interrupt Set-Pending Register associated with the RTC_ALM interrupt to 0 again after modifying values of the alarm registers. After the interrupt flag for the alarm interrupt is set to 1 and the state is returned to mismatching of the alarm registers and clock counters, the flag does not set again until there is another match or the values of the alarm registers are modified again.

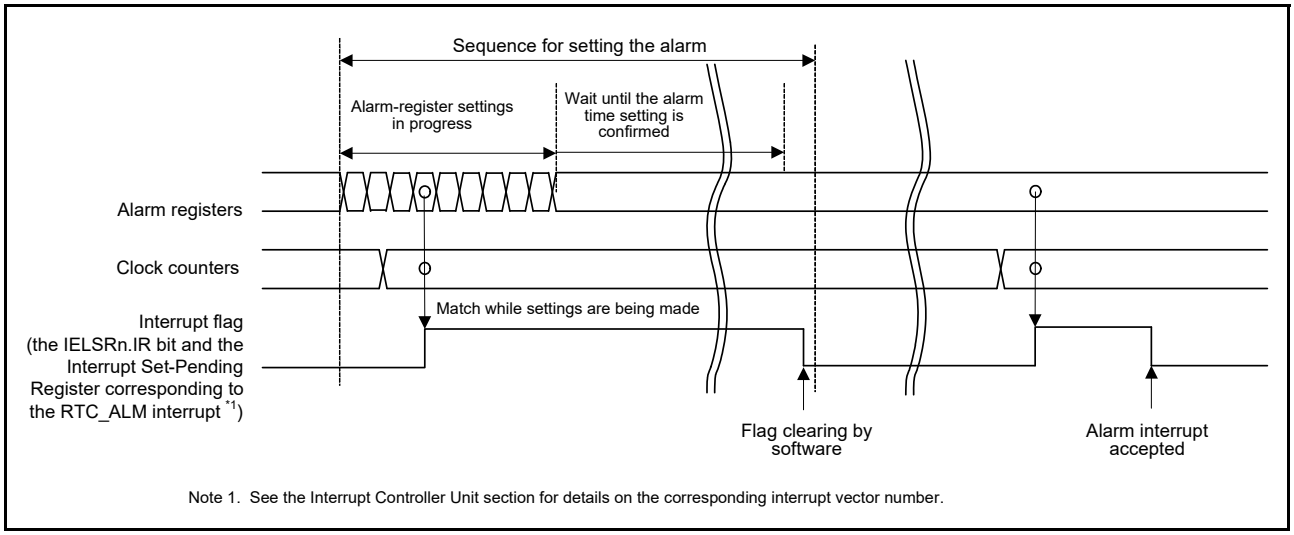


Figure 23.9 Timing for the alarm interrupt (RTC_ALM)

(2) Periodic interrupt (RTC_PRD)

This interrupt is generated at intervals of 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second. The interrupt interval can be selected through the RCR1.PES[3:0] bits.

(3) Carry interrupt (RTC_CUP)

This interrupt is generated when a carry to the second counter/binary counter 0 occurred or a carry to the R64CNT counter occurred during read access to the 64-Hz counter.

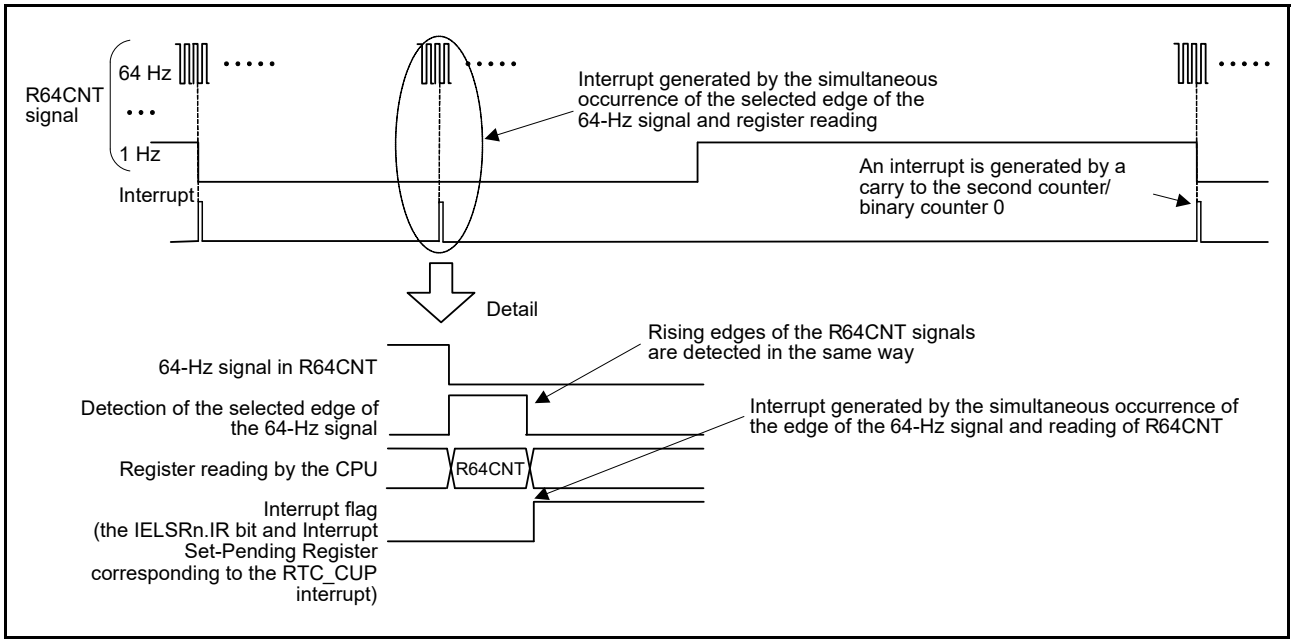


Figure 23.10 Timing for the carry interrupt (RTC_CUP)

23.5 Event Link Output

The RTC generates periodic event output (RTC_PRD) event signal for the ELC that can be used to initiate operations by other modules selected in advance.

The periodic event signal is output at the interval selected from 1/256, 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2, 1, and 2 seconds by setting the RCR1.PES[3:0] bits.

The event generation period immediately after the event generation is selected, is not guaranteed.

Note: If event linking from the RTC is used, only set the ELC after setting the RTC, for example, initialization and time settings. Setting the RTC after the ELC can lead to output of unexpected event signals.

23.5.1 Interrupt Handling and Event Linking

The RTC has a bit to enable or disable periodic interrupts. An interrupt request signal is output for the CPU when an interrupt source is generated while the associated enable bit is enabled.

In contrast, an event link output signal is sent to other modules as an event signal through the ELC when an interrupt source is generated, regardless of the setting of the associated interrupt enable bit.

Note: Although alarm and periodic interrupts can still be output during Software Standby mode, the periodic event signals for the ELC are not output.

23.6 Usage Notes

23.6.1 Register Writing during Counting

The following registers must not be written to during counting, that is, while the RCR2.START bit is 1:

- RSECCNT/BCNT0
- RMINCNT/BCNT1
- RHRCNT/BCNT2

- RDAYCNT
- RWKCNT/BCNT3
- RMONCNT
- RYRCNT
- RCR1.RTCOS
- RCR2.RTCOE
- RCR2.HR24
- RFRL.

The counter must be stopped before writing to any of the these registers.

23.6.2 Use of Periodic Interrupts

The procedure for using periodic interrupts is shown in Figure 23.11.

The generation and period of the periodic interrupt can be changed by setting the RCR1.PES[3:0] bits. However, because the prescaler R64CNT and RSECCNT/BCNT0 are used to generate interrupts, the interrupt period is not guaranteed immediately after setting the RCR1.PES[3:0] bits.

In addition, the stopping/restarting or resetting of the counter operation, reset by RTC software, and the 30-second adjustment by changing the RCR2 value, affects the interrupt period. When the time error adjustment function is used, the interrupt generation period after adjustment is added or subtracted based on the adjustment value.

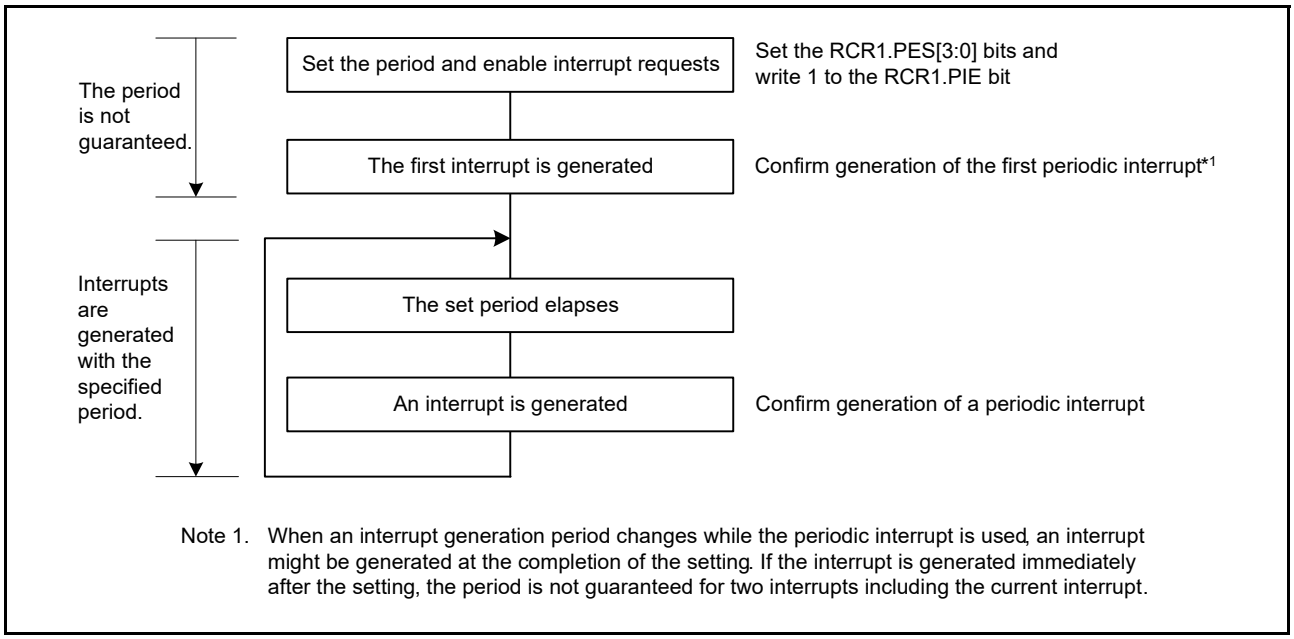


Figure 23.11 Using periodic interrupt function

23.6.3 RTCOUT (1-Hz/64-Hz) Clock Output

Stopping/restarting or resetting the counter operation, reset by RTC software, and the 30-second adjustment by changing the RCR2 value, affects the period of RTCOUT (1-Hz/64-Hz) output. When the time error adjustment function is used, the period of RTCOUT (1-Hz/64-Hz) output after adjustment is added or subtracted based on the adjustment value.

23.6.4 Transitions to Low Power Modes after Setting Registers

A transition to a low power state during a write to an RTC register might corrupt the value of the register. After setting the register, confirm that the setting is in place before initiating a transition to a low power state.

23.6.5 Notes when Writing to and Reading from Registers

- When reading a counter register such as the second counter after writing to the counter register, follow the procedure in section 23.3.5, Reading 64-Hz Counter and Time
- The value written to the count registers, alarm registers, year alarm enable register, bits RCR2.AADJE, AADJP, and HR24, RCR4 register, or frequency register is reflected when four read operations are performed after writing
- The values written to the RCR1.CIE, RCR1.RTCOS, and RCR2.RTCOE bits can be read immediately after writing
- To read the value from the timer counter after returning from a reset or a period in Software Standby mode state, wait for 1/128 second while the clock is operating (RCR2.START bit = 1)
- After a reset is generated, write to the RTC register after 6 cycles of the count source clock have elapsed.

23.6.6 Changing the Count Mode

When changing the count mode (calendar/binary), set the RCR2.START bit to 0, stop the counting operation, then start it again from the initial setting. For details on the initial setting, see section 23.3.1, Outline of Initial Settings of Registers after Power On.

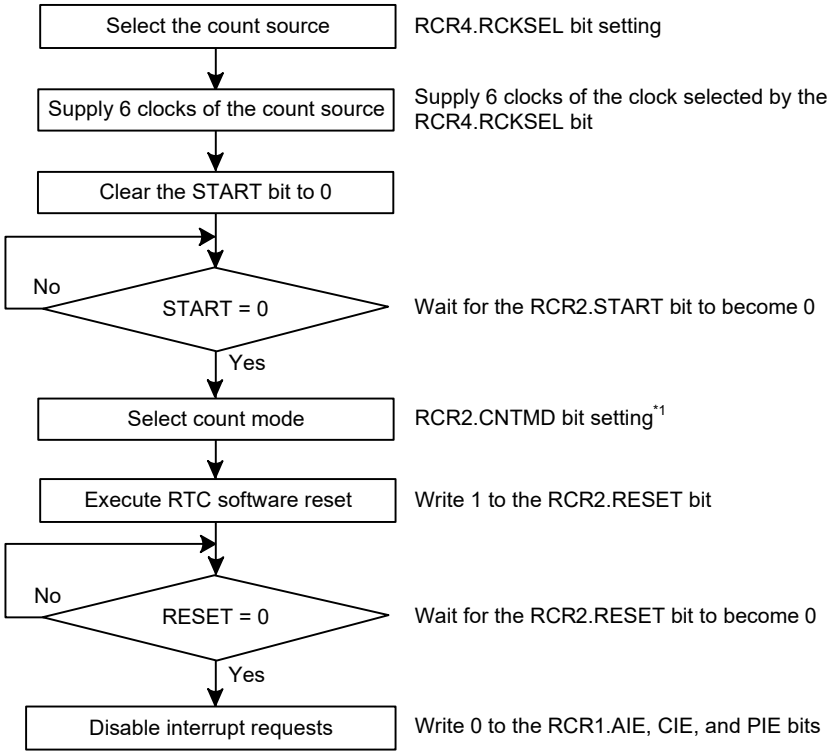
23.6.7 Initialization Procedure when the Realtime Clock is not to be used

Registers in the RTC are not initialized by a reset. Depending on the initial state, the generation of an unintentional interrupt request or operation of the counter might lead to increased power consumption.

For applications that do not require a realtime clock, initialize the registers by following the initialization procedure shown in Figure 23.12.

Alternatively, when the sub-clock oscillator is not used as the system clock or realtime clock, the counter can be stopped by writing 0 (sub-clock oscillator is selected) to the RCR4.RCKSEL bit and stopping the sub-clock oscillator. To stop the sub-clock oscillator, write 1 to the SOSCCR.SOSTP bit.

For details on the setting of the SOSCCR.SOSTP bit, see section 8, Clock Generation Circuit.



Note 1. This step is not required if the count mode is set concurrently by setting the START bit to 0.

Figure 23.12 Initialization procedure

24. Watchdog Timer (WDT)

24.1 Overview

The Watchdog Timer (WDT) is a 14-bit down-counter. It can be used to reset the MCU when the counter underflows because the system has run out of control and become unable to refresh the WDT. In addition, a non-maskable interrupt or an interrupt can be generated by an underflow. The refresh-permitted period can be set to refresh the counter and to detect when the system runs out of control.

Table 24.1 lists the WDT specifications, and Figure 24.1 shows a block diagram.

Table 24.1 WDT specifications

Parameter	Specifications
Count source	Peripheral clock (PCLKB)
Clock division ratio	Divide by 4, 64, 128, 512, 2,048, or 8,192
Counter operation	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Auto start mode: Counting automatically starts after a reset or after an underflow or refresh error occurs • Register start mode: Counting is started by refresh operation (writing to the WDTRR register).
Conditions for stopping the counter	• Reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error is generated.
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Watchdog timer Reset sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error).
Non-maskable interrupt/interrupt sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error).
Reading the counter value	The down-counter value can be read by the WDTSR register.
Event link function (output)	• Down-counter underflow event output • Refresh error event output.
Output signal (internal signal)	• Reset output • Interrupt request output • Sleep mode count stop control output.

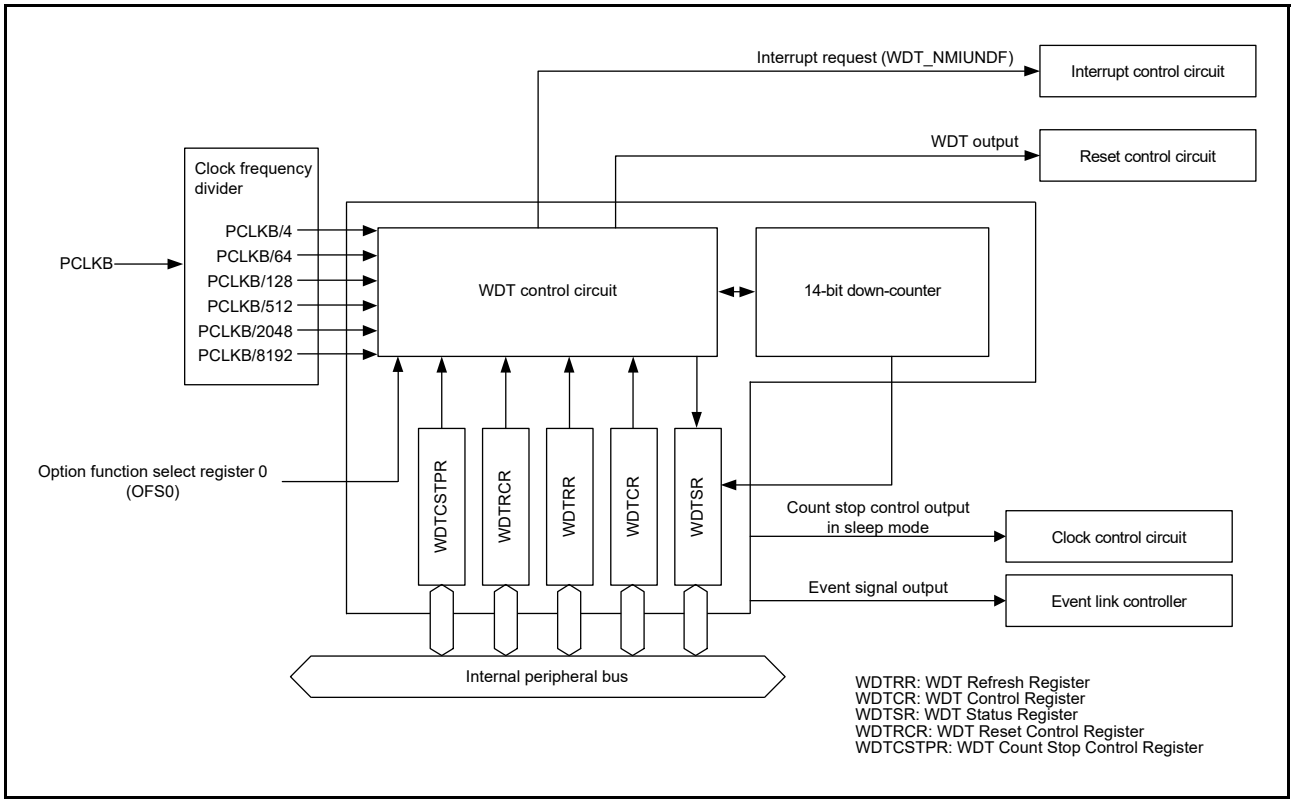


Figure 24.1 WDT block diagram

24.2 Register Descriptions

24.2.1 WDT Refresh Register (WDTRR)

Address(es): WDT.WDTRR 4004 4200h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

Bit	Description	R/W
b7 to b0	The down-counter is refreshed by writing 00h and then writing FFh to this register	R/W

The WDTRR register refreshes the down-counter of the WDT.

The down-counter of the WDT is refreshed by writing 00h and then writing FFh to WDTRR (refresh operation) within the refresh-permitted period.

After the down-counter is refreshed, it starts counting down from the value selected by setting the WDT timeout period select bits (OFS0.WDTTOPS[1:0]) in the Option Function Select Register 0 in auto start mode. In register start mode, counting down starts from the value selected by setting the timeout period selection bits (WDTCR.TOPS[1:0]) in the WDT Control Register.

When 00h is written, the read value is 00h, when a value other than 00h is written, the read value is FFh. For details on the refresh operation, see section 24.3.3, Refresh Operation.

24.2.2 WDT Control Register (WDTCR)

Address(es): WDT.WDTCR 4004 4202h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	RPSS[1:0]		—	—	RPES[1:0]		CKS[3:0]				—	—	TOPS[1:0]	
Value after reset:	0	0	1	1	0	0	1	1	1	1	1	1	0	0	1	1

Bit	Symbol	Bit name	Description	R/W
b1, b0	TOPS[1:0]	Timeout Period Selection	b1 b0 0 0: 1,024 cycles (03FFh) 0 1: 4,096 cycles (0FFFh) 1 0: 8,192 cycles (1FFFh) 1 1: 16,384 cycles (3FFFh).	R/W
b3, b2	—	Reserved	These bits are read as 0 and cannot be modified	R/W
b7 to b4	CKS[3:0]	Clock Division Ratio Selection	b7 b4 0 0 0 1: PCLKB/4 0 1 0 0: PCLKB/64 1 1 1 1: PCLKB/128 0 1 1 0: PCLKB/512 0 1 1 1: PCLKB/2048 1 0 0 0: PCLKB/8192. Other settings are prohibited.	R/W
b9, b8	RPES[1:0]	Window End Position Selection	b9 b8 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0% (window end position is not specified).	R/W
b11, b10	—	Reserved	These bits are read as 0 and cannot be modified	R/W
b13, b12	RPSS[1:0]	Window Start Position Selection	b13 b12 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100% (window start position is not specified).	R/W
b15, b14	—	Reserved	These bits are read as 0 and cannot be modified	R/W

Some restrictions apply to writes to the WDTCR register. For details, see section 24.3.2, Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers.

In auto start mode, the settings in the WDTCR register are disabled, and the settings in the Option Function Select Register 0 (OFS0) are enabled. The settings for the WDTCR register can also be made in the OFS0 register. For details, see section 24.3.7, Association between Option Function Select Register 0 (OFS0) and WDT Registers.

TOPS[1:0] bits (Timeout Period Selection)

The TOPS[1:0] bits select the timeout period, the period until the down-counter underflows, between 1,024, 4,096, 8,192, and 16,384 cycles, taking the divided clock specified in the CKS[3:0] bits as 1 cycle.

After the down-counter is refreshed, the combination of the CKS[3:0] and TOPS[1:0] bits determines the time (number of PCLKB cycles) until the counter underflows.

Table 24.2 lists the relationship between the CKS[3:0] and TOPS[1:0] bit settings, the timeout period, and the number of PCLKB cycles.

Table 24.2 Timeout period settings

CKS[3:0] bits				TOPS[1:0] bits		Clock division ratio	Timeout period (number of cycles)	Cycles of PCLKB clock
b7	b6	b5	b4	b1	b0			
0	0	0	1	0	0	PCLKB/4	1024	4096
				0	1		4096	16384
				1	0		8192	32768
				1	1		16384	65536
0	1	0	0	0	0	PCLKB/64	1024	65536
				0	1		4096	262144
				1	0		8192	524288
				1	1		16384	1048576
1	1	1	1	0	0	PCLKB/128	1024	131072
				0	1		4096	524288
				1	0		8192	1048576
				1	1		16384	2097152
0	1	1	0	0	0	PCLKB/512	1024	524288
				0	1		4096	2097152
				1	0		8192	4194304
				1	1		16384	8388608
0	1	1	1	0	0	PCLKB/2048	1024	2097152
				0	1		4096	8388608
				1	0		8192	16777216
				1	1		16384	33554432
1	0	0	0	0	0	PCLKB/8192	1024	8388608
				0	1		4096	33554432
				1	0		8192	67108864
				1	1		16384	134217728

CKS[3:0] bits (Clock Division Ratio Selection)

The CKS[3:0] bits specify the division ratio of the clock used for the down-counter. The division ratio can be selected from the peripheral clock (PCLKB) divided by 4, 64, 128, 512, 2048, and 8,192. Combined with the TOPS[1:0] bit setting, a count period between 4,096 and 134,217,728 cycles of the PCLKB clock can be selected for the WDT.

RPES[1:0] bits (Window End Position Selection)

The RPES[1:0] bits specify the window end position that indicates the refresh-permitted period. 75%, 50%, 25%, or 0% of the timeout period can be selected for the window end position. The selected window end position should be a value less than the value for the window start position (window start position > window end position). If the window end position is set to a value greater than or equal to the window start position, the window start position setting is enabled and the window end position is set to 0%.

RPSS[1:0] bits (Window Start Position Selection)

The RPSS[1:0] bits specify the window start position that indicates the refresh-permitted period. 100%, 75%, 50%, or 25% of the timeout period can be selected for the window end position. The window start position should be set to a value greater than the value for the window end position. If the window start position is set to a value less than or equal to the window end position, the window start position setting is enable and the window end position is set to 0%.

Table 24.3 lists the counter values for the window start and end positions and Figure 24.2 shows the refresh-permitted period set by the RPSS[1:0], RPES[1:0], and TOPS[1:0] bits.

Table 24.3 Relationship between timeout period and window start and end counter values

TOPS[1:0] bits		Timeout period		Window start and end counter value			
		Cycles	Counter value	100%	75%	50%	25%
0	0	1024	03FFh	03FFh	02FFh	01FFh	00FFh
0	1	4096	0FFFh	0FFFh	0BFFh	07FFh	03FFh
1	0	8192	1FFFh	1FFFh	17FFh	0FFFh	07FFh
1	1	16384	3FFFh	3FFFh	2FFFh	1FFFh	0FFFh

RPSS[1:0] Bits		RPES[1:0] Bits		Window	
b13	b12	b9	b8	Start (%)	End (%)
1	1	1	1	100	0
		1	0		25
		0	1		50
		0	0		75
1	0	1	1	75	0
		1	0		25
		0	1		50
		0	0		75
0	1	1	1	50	0
		1	0		25
		0	1		50
		0	0		75
0	0	1	1	25	0
		1	0		25
		0	1		50
		0	0		75

Note: If window end position setting ≥ window start position setting, the window end position setting is set to 0%.

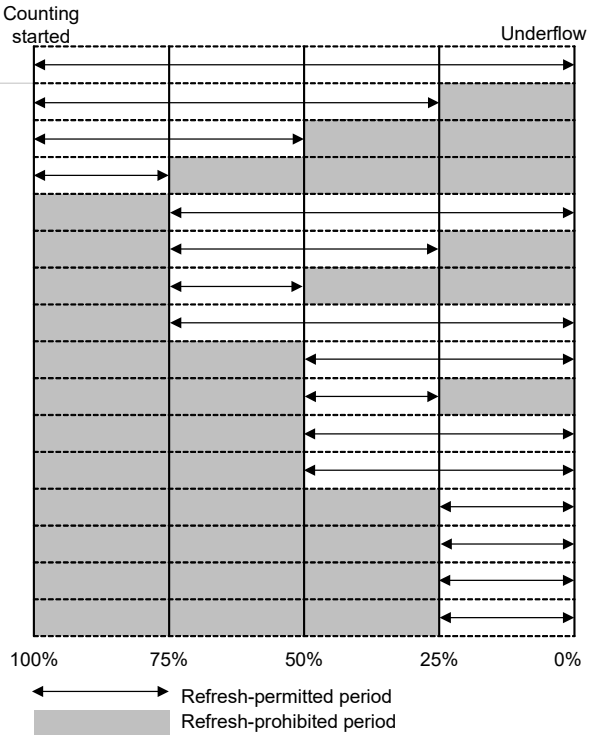


Figure 24.2 RPSS[1:0] and RPES[1:0] bit settings and refresh-permitted period

24.2.3 WDT Status Register (WDTSR)

Address(es): WDT.WDTSR 4004 4204h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	REFEF	UNDFF	CNTVAL[13:0]													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b13 to b0	CNTVAL[13:0]	Down-Counter Value	Value counted by the down-counter	R
b14	UNDFF	Underflow Flag	0: No underflow occurred 1: Underflow occurred.	R(/W) *1
b15	REFEF	Refresh Error Flag	0: No refresh error occurred 1: Refresh error occurred.	R(/W) *1

Note 1. Only 0 can be written to clear the flag.

CNTVAL[13:0] bits (Down-Counter Value)

Read the CNTVAL[13:0] bits to confirm the value of the down-counter, but the read value might differ from the actual count by 1.

UNDFF flag (Underflow Flag)

Read the UNDFF flag to confirm whether an underflow occurred in the down-counter. The value 1 indicates that the down-counter underflowed. Write 0 to the UNDFF flag to set the value to 0. Writing 1 has no effect.

Clearing of the UNDFF flag takes (N+1) PCLKB cycles. In addition, clearing of this flag is ignored for (N+1) PCLKB cycles following an underflow. N is specified in the WDTCR.CKS[3:0] bits as follows:

- When WDTCR.CKS[3:0] = 0001b , N = 4
- When WDTCR.CKS[3:0] = 0100b , N = 64
- When WDTCR.CKS[3:0] = 1111b , N = 128
- When WDTCR.CKS[3:0] = 0110b , N = 512
- When WDTCR.CKS[3:0] = 0111b , N = 2048
- When WDTCR.CKS[3:0] = 1000b , N = 8192.

REFEF flag (Refresh Error Flag)

Read the REFEF flag to confirm whether a refresh error occurred. The value 1 indicates that a refresh error occurred. Write 0 to the REFEF flag to set the value to 0. Writing 1 has no effect.

Clearing of the REFEF flag takes (N+1) PCLKB cycles. In addition, clearing of this flag is ignored for (N+1) PCLKB cycles following a refresh error. N is specified in the WDTCR.CKS[3:0] bits as follows:

- When WDTCR.CKS[3:0] = 0001b , N = 4
- When WDTCR.CKS[3:0] = 0100b , N = 64
- When WDTCR.CKS[3:0] = 1111b , N = 128
- When WDTCR.CKS[3:0] = 0110b , N = 512
- When WDTCR.CKS[3:0] = 0111b , N = 2048
- When WDTCR.CKS[3:0] = 1000b , N = 8192.

24.2.4 WDT Reset Control Register (WDTRCR)

Address(es): WDT.WDTRCR 4004 4206h

	b7	b6	b5	b4	b3	b2	b1	b0
	RSTIRQS	—	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0 and cannot be modified	R/W
b7	RSTIRQS	Reset Interrupt Request Selection	WDT behavior selection 0: Interrupt 1: Reset.	R/W

Some restrictions apply to writes to the WDTRCR register. For details, see section 24.3.2, Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers.

In auto start mode, the WDTRCR register settings are disabled, and the settings in the Option Function Select register 0 (OFS0) are enabled. The settings for the WDTRCR register can also be made for the OFS0 register. For details, see section 24.3.7, Association between Option Function Select Register 0 (OFS0) and WDT Registers.

24.2.5 WDT Count Stop Control Register (WDTCSTPR)

Address(es): WDT.WDTCSTPR 4004 4208h

	b7	b6	b5	b4	b3	b2	b1	b0
	SLCSTP	—	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0 and cannot be modified	R/W
b7	SLCSTP	Sleep-Mode Count Stop Control	0: Count stop is disabled 1: Count is stopped on transition to Sleep mode.	R/W

The WDTCSTPR register controls whether to stop the WDT counter in Sleep mode. Some restrictions apply to writes to the WDTCSTPR register. For details, see section 24.3.2, Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers.

In auto start mode, the WDTCSTPR register settings are disabled, and the settings in the Option Function Select register 0 (OFS0) are enabled. The settings for the WDTCSTPR register can also be made for the OFS0 register. For details, see section 24.3.7, Association between Option Function Select Register 0 (OFS0) and WDT Registers.

SLCSTP bit (Sleep-Mode Count Stop Control)

The SLCSTP bit selects whether to stop counting on transition to Sleep mode.

24.2.6 Option Function Select Register 0 (OFS0)

For details on the OFS0 register, see section 24.3.7, Association between Option Function Select Register 0 (OFS0) and WDT Registers.

24.3 Operation

24.3.1 Count Operation in each Start Mode

The WDT has two start modes:

- Auto start mode, in which counting automatically starts after a release from the reset state
- Register start mode, in which counting is started with a refresh by writing to the register.

In auto start mode, counting automatically starts after a release from the reset state according to the settings in the Option Function Select register 0 (OFS0) in the Flash.

In register start mode, counting is started with a refresh by writing to the register after the respective registers are set after a release from the reset state.

Select auto start mode or register start mode by setting the WDT start mode select bit (OFS0.WDTSTRT) in the OFS0 register.

When the auto start mode is selected, the settings in the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), and WDT Count Stop Control Register (WDTCSTPR) are disabled, and the settings in the OFS0 register are enabled.

When the register start mode is selected, the OFS0 register settings are disabled, and the settings in the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), and WDT Count Stop Control Register (WDTCSTPR) are enabled.

24.3.1.1 Register start mode

When the WDT start mode select bit (OFS0.WDTSTRT) is 1, register start mode is selected, the OFS0 register setting is invalid, and the WDT control register (WDTCR), WDT Reset Control Register (WDTRCR), and WDT Count Stop Control Register (WDTCSTPR) are enabled.

After the reset state is released, set the following:

- Clock division ratio in the WDTCR register
- Window start and end positions in the WDTCR register
- Timeout period in the WDTCR register
- Reset output or interrupt request output in the WDTRCR register
- Counter stop control at transitions to Sleep mode in the WDTCSTPR register.

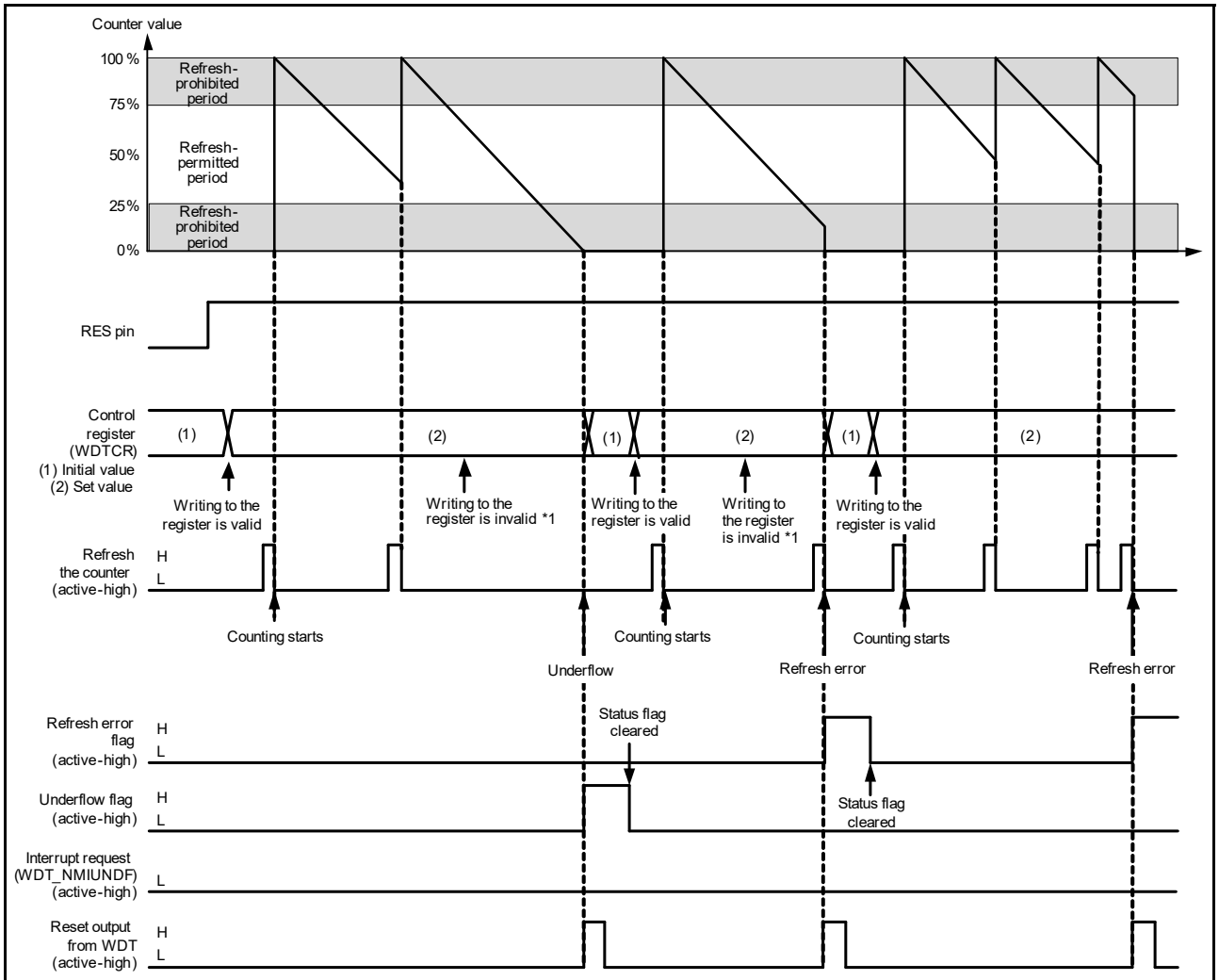
The WDT refresh register (WDTRR) refreshes the down counter.

As a result, the downcount starts at the value set by the timeout period selection bit (WDTCR.TOPS [1: 0]).

After that, as long as the program continues normal operation and the counter is refreshed within the refresh-permitted period, the value in the counter is reset each time the counter is refreshed and down-counting continues. The WDT does not output the reset signal or non-maskable interrupt request/interrupt request as long as the counting continues. However, if the down-counter underflows because the down-counter cannot be refreshed because of a program runaway, of if a refresh error occurs because the counter was refreshed outside the refresh-permitted period, the WDT outputs the reset signal or non-maskable interrupt request/interrupt request (WDT_NMIUNDF). Reset output or interrupt request output can be selected in the WDT Reset Interrupt Request Select bit (WDTRCR.RSTIRQS). The interrupt enable that initiates NMI can be selected with the WDT Underflow/Refresh Error Interrupt Enable bit (NMIER.WDTEN).

Figure 24.3 shows an example of operation under the following conditions:

- Register start mode (OFS0.WDTSTRT = 1)
- Reset output is enabled (WDTRCR.RSTIRQS = 1)
- The window start position is 75% (WDTCR.RPSS[1:0] = 10b)
- The window end position is 25% (WDTCR.RPES[1:0] = 10b).



Note 1. See section 24.3.2, Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers.

Figure 24.3 Operation example in register start mode

24.3.1.2 Auto start mode

When the WDT start mode select bit (OFS0.WDTSTRT) in the Option Function Select register 0 (OFS0) is 0, auto start mode is selected, the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), and WDT Count Stop Control Register (WDTCSTPR) are disabled, and the settings in the OFS0 register are enabled.

Within the reset state, the setting values for the following in the Option Function Select Register 0 (OFS0) are set in the WDT registers:

- Clock division ratio
- Window start and end positions
- Timeout period
- Reset output or interrupt request
- Counter stop control on transitions to Sleep mode.

When the reset state is released, the down-counter automatically starts counting down from the value set in the WDT timeout period select bits (OFS0.WDTTOPS[1:0]).

After that, as long as the program continues normal operation and the counter is refreshed within the refresh-permitted period, the value in the counter is reset each time the counter is refreshed and down-counting continues. The WDT does

not output the reset signal or non-maskable interrupt request/interrupt request as long as the counting continues. However, if the down-counter underflows because the down-counter cannot be refreshed because of a program runaway, of if a refresh error occurs because the counter was refreshed outside the refresh-permitted period, the WDT outputs the reset signal or non-maskable interrupt request/interrupt request (WDT_NMIUNDF).

After the reset signal or non-maskable interrupt request/interrupt request is generated, the counter reloads the timeout period after counting for 1 cycle. The value of the timeout period is set in the down-counter and counting restarts.

Reset output or interrupt request output can be selected in the WDT Reset Interrupt Request Select bit (OFS0.WDTRSTIRQS). The interrupt enable that initiates NMI can be selected with the WDT Underflow/Refresh Error Interrupt Enable bit (NMIER.WDTEN).

Figure 24.4 shows an example of operation (non-maskable interrupt) under the following conditions:

- Auto start mode (OFS0.WDTSTRT = 0)
- WDT behavior selection: interrupt (OFS0.WDTRSTIRQS = 0)
- Non-maskable Interrupt: WDT Underflow/Refresh Error Interrupt Enable (NMIER.WDTEN = 1)
- The window start position is 75% (OFS0.WDTRPSS[1:0] = 10b)
- The window end position is 25% (OFS0.WDTRPES[1:0] = 10b).

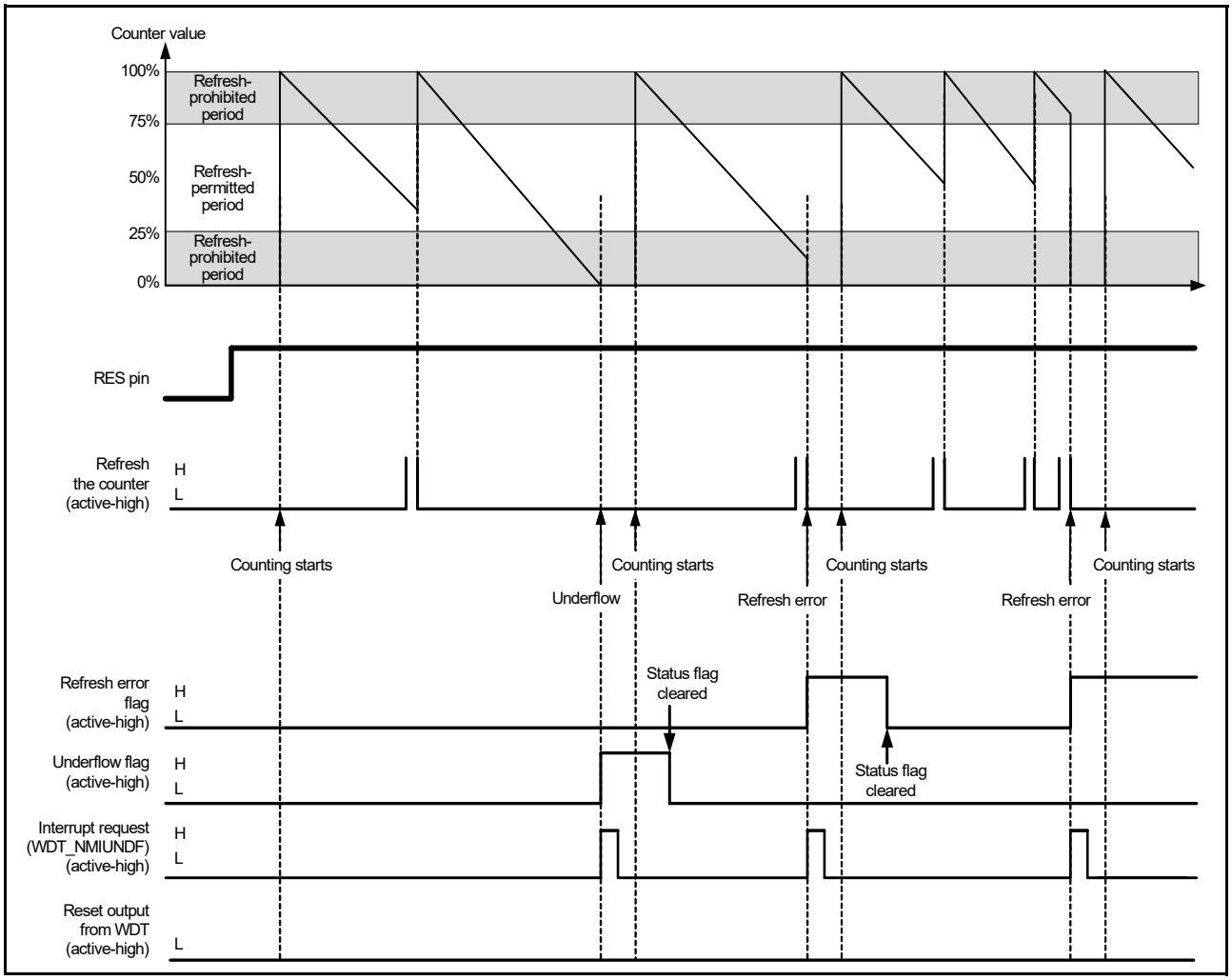


Figure 24.4 Operation example in auto start mode

24.3.2 Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers

Writing to the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), or WDT Count Stop Control Register (WDTCSTPR) is possible once each between the release from the reset state and the first refresh

operation.

After a refresh operation (counting starts) or a write to WDTCR, WDTRCR, or WDTCSTPR, the protection signal in the WDT becomes 1 to protect WDTCR, WDTRCR, and WDTCSTPR against subsequent write attempts. This protection is released by a reset source of the WDT. With other reset sources, the protection is not released.

Figure 24.5 shows control waveforms produced in response to writing to the WDTCR.

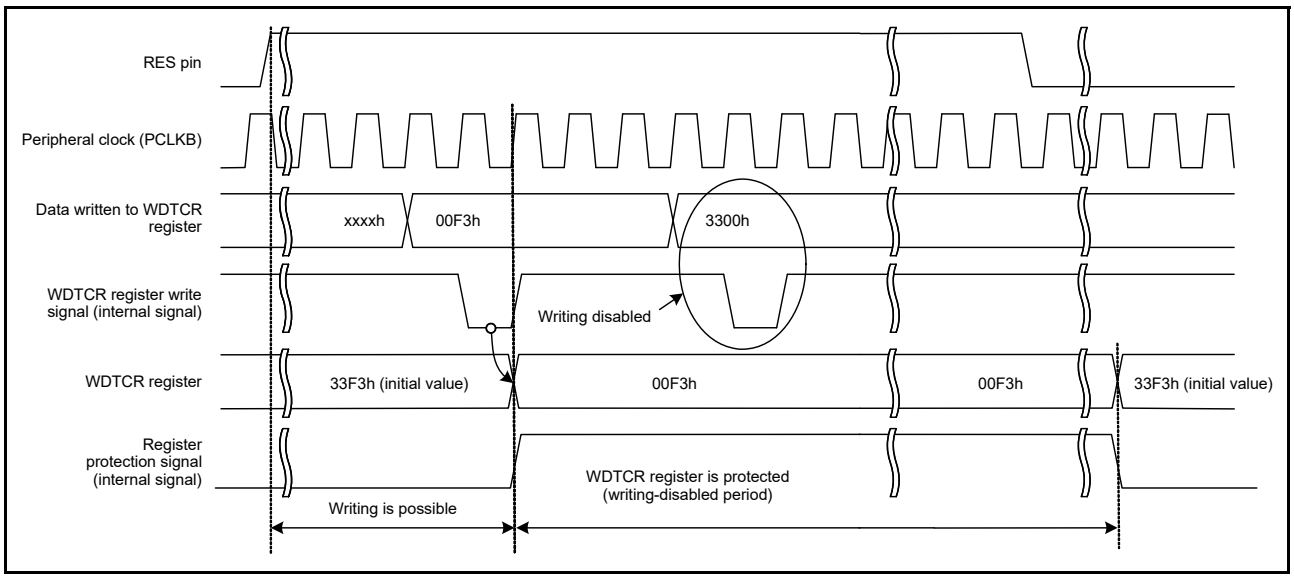


Figure 24.5 Control waveforms produced in response to writes to the WDTCR register

24.3.3 Refresh Operation

The down-counter is refreshed by writing the values 00h and then FFh to the WDT Refresh Register (WDTRR). If a value other than FFh is written after 00h, the down-counter is not refreshed. If an invalid value is written, correct refreshing resumes on a write of 00h and then FFh to the WDTRR register.

Correct refreshing is also performed when a register other than WDTRR is accessed or when WDTRR is read between writing 00h and writing FFh to WDTRR.

Writes to refresh the counter must be made within the refresh-permitted period, and this is determined by writing FFh. For this reason, correct refreshing is performed even when 00h is written outside the refresh-permitted period.

[Example write sequences that are valid for refreshing the counter]

- 00h → FFh
- 00h (n-1-th time) → 00h (nth time) → FFh
- 00h → access to another register or read from WDTRR → FFh.

[Example write sequences that are not valid for refreshing the counter]

- 23h (a value other than 00h) → FFh
- 00h → 54h (a value other than FFh)
- 00h→ AAh (00h and a value other than FFh) → FFh.

After FFh is written to the WDT Refresh Register (WDTRR), refreshing the down-counter requires up to 4 cycles of the signal for counting. To meet this requirement, complete writing FFh to the WDTRR 4 count cycles before the down-counter underflows.

Figure 24.6 shows the WDT refresh operation waveforms when the clock division ratio is PCLKB/64.

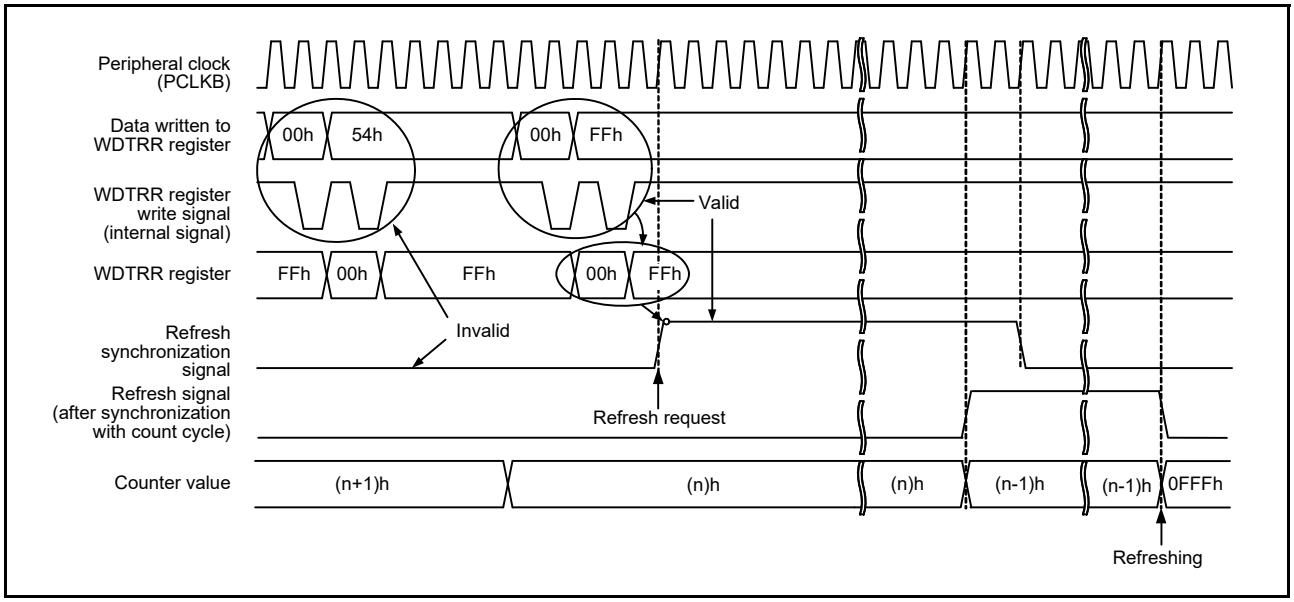


Figure 24.6 WDT refresh operation waveforms when WDTCR.CKS[3:0] = 0100b, WDTCR.TOPS[1:0] = 01b

24.3.4 Reset Output

When the reset interrupt selection bit (WDTRCR.RSTIRQS) is set to 1 in register start mode, or when the WDT reset interrupt request select bit (OFS0.WDTRSTIRQS) in the Option Function Select Register 0 (OFS0) is set to 1 in auto start mode, a reset signal is output for 1 count cycle when an underflow in the down-counter or a refresh error occurs.

In register start mode, the down-counter is initialized (all bits set to 0) and stopped in that state after output of a reset signal. After the reset state is released and the program is restarted, the counter is set up again and counting down starts again with a refresh. In auto start mode, counting down starts automatically after the reset state is released.

24.3.5 Interrupt Sources

When the reset interrupt selection bit (WDTRCR.RSTIRQS) is set to 0 in register start mode or when the WDT reset interrupt request select bit (OFS0.WDTRSTIRQS) in the Option Function Select Register 0 (OFS0) is set to 0 in auto start mode, an interrupt (WDT_NMIUNDF) signal is generated when an underflow in the counter or a refresh error occurs. This interrupt can be used as a non-maskable interrupt or an interrupt. For details, see section 12, Interrupt Controller Unit (ICU).

Table 24.4 WDT interrupt sources

Name	Interrupt source	DTC activation
WDT_NMIUNDF	Down-counter underflow Refresh error	Not possible

24.3.6 Reading the Down-Counter Value

The WDT stores the counter value in the down-counter value bits (WDTSR.CNTVAL[13:0]) of the WDT Status Register. Check these bits to obtain the counter value.

Figure 24.7 shows the processing for reading the WDT down-counter value when the clock division ratio is PCLKB/64.

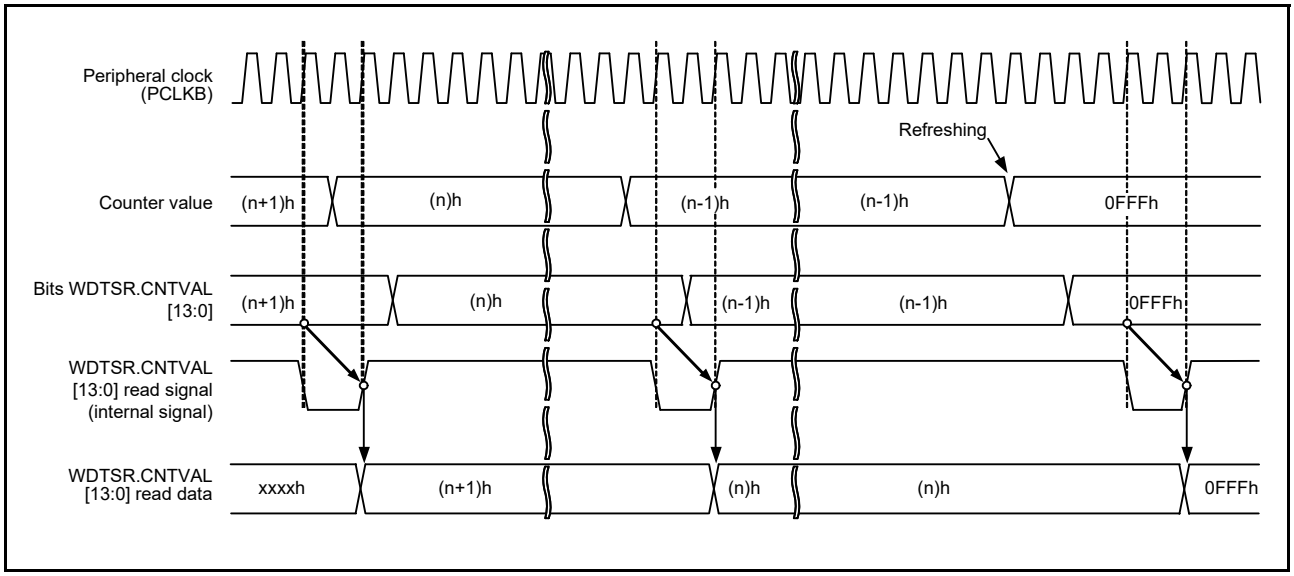


Figure 24.7 Read process for WDT down-counter value when WDTCR.CKS[3:0] = 0100b, WDTCR.TOPS[1:0] = 01b

24.3.7 Association between Option Function Select Register 0 (OFS0) and WDT Registers

Table 24.5 lists the association between the Option Function Select Register 0 (OFS0) used in auto start mode, and the registers used in register start mode. Do not change the OFS0 register setting during WDT operation. For details on the Option Function Select Register 0 (OFS0), see section 6.2.1, Option Function Select Register 0 (OFS0).

Table 24.5 Association between Option Function Select Register 0 (OFS0) and the WDT registers

Control target	Function	OFS0 register (enabled in auto start mode) OFS0.WDTSTRT = 0	WDT registers (enabled in register start mode) OFS0.WDTSTRT = 1
Down-counter	Timeout period selection	OFS0.WDTTOPS[1:0]	WDTCR.TOPS[1:0]
	Clock division ratio selection	OFS0.WDTCKS[3:0]	WDTCR.CKS[3:0]
	Window start position selection	OFS0.WDTRPSS[1:0]	WDTCR.RPSS[1:0]
	Window end position selection	OFS0.WDTRPES[1:0]	WDTCR.RPES[1:0]
Reset output or interrupt request output	Reset interrupt request selection	OFS0.WDTRSTIRQS	WDTRCR.RSTIRQS
Count stop	Sleep mode count stop control	OFS0.WDTSTPCTL	WDTCSTPR.SLCSTP

24.4 Link Operation by ELC

The WDT is capable of link operation for a specified module when interrupt request signal is used as an event signal by the Event Link Controller (ELC). The event signal is output by the counter underflow or refresh error. An event signal is output regardless of the setting of the reset interrupt request selection bit (WDTRCR.RSTIRQS) in register start mode or auto start mode. An event signal can also be output when the next interrupt source is generated while the refresh error flag (WDTSR.REFEF) or underflow flag (WDTSR.UNDFF) is 1. For details, see section 16, Event Link Controller (ELC).

24.5 Usage Notes

24.5.1 ICU Event Link Setting Register n (IELSRn) Setting

Setting 18h to ICU Event Link Setting Register n (IELSRn.IELS[7:0]) is prohibited when enabling the WDT reset assertion (OFS0.WDTRSTIRQS = 1 or WDTRCR.RSTIRQS = 1) or when enabling event link operation (ELSRm.ELS[7:0] =18h).

25. Independent Watchdog Timer (IWDT)

25.1 Overview

The Independent Watchdog Timer (IWDT) consists of a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or an underflow interrupt. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a failsafe mechanism when the system runs out of control. The IWDT can be triggered automatically by a reset, underflow, refresh error, or a refresh of the count value in the registers.

The functions of the IWDT are different from those of the WDT in the following ways:

- The divided IWDT-dedicated clock (IWDTCLK) is used as the count source (not affected by PCLKB)
- IWDT does not support register start mode
- When transitioning to low power mode, the OFS0.IWDTSTPCTL bit can be used to select whether to stop the counter.

Table 25.1 lists the IWDT specifications and Figure 25.1 shows a block diagram.

Table 25.1 IWDT specifications

Parameter	Description
Count source*1	IWDT-dedicated clock (IWDTCLK)
Clock division ratio	Division by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down using a 14-bit down-counter
Condition for starting the counter	• Counting automatically starts after a reset
Conditions for stopping the counter	• Reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error is generated (counting restarts automatically).
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Reset output sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error).
Non-maskable interrupt/interrupt sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error).
Reading the counter value	The down-counter value can be read by the IWDTSR register
Event link function (output)	• Down-counter underflow event output • Refresh error event output.
Output signal (internal signal)	• Reset output • Interrupt request output • Sleep-mode count stop control output.
Auto-start mode	• Selecting the clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to Sleep mode, Software Standby mode, or Snooze mode (OFS0.IWDTSTPCTL bit).

Note 1. Satisfy the frequency of the peripheral module clock (PCLKB) ≥ 4 × (the frequency of the count clock source after division).

To use the IWDT, you must supply the IWDT-dedicated clock (IWDTCLK). The bus interface and registers operate with PCLKB, and the 14-bit counter and control circuits operate with IWDTCLK.

Figure 25.1 shows a block diagram of the IWDT.

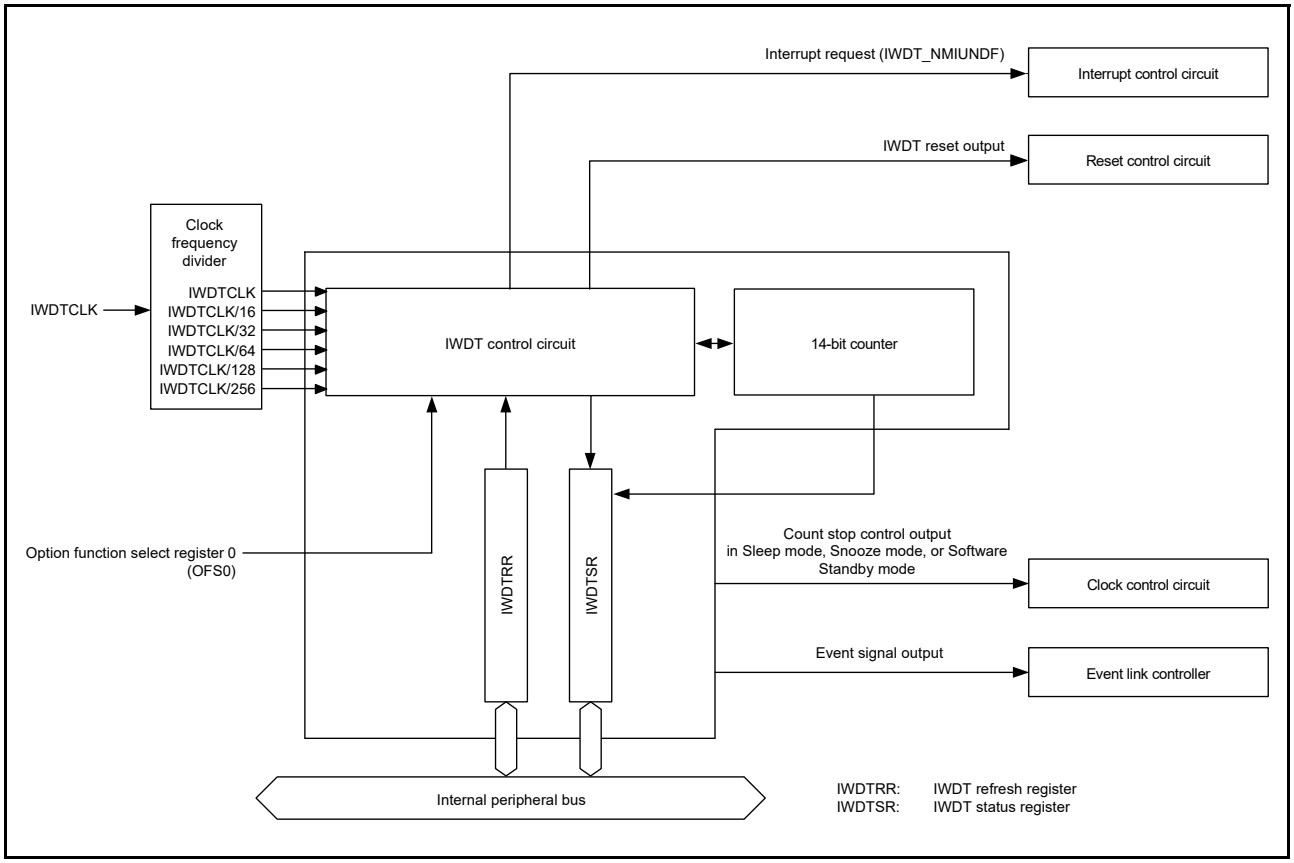


Figure 25.1 IWDT block diagram

25.2 Register Descriptions

25.2.1 IWDT Refresh Register (IWDTRR)

Address(es): IWDT.IWDTRR 4004 4400h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

Bit	Description	R/W
b7 to b0	The counter is refreshed by writing 00h and then writing FFh to this register	R/W

The IWDTRR register refreshes the down-counter of the IWDT. The down-counter of the IWDT is refreshed by writing 00h and then writing FFh to IWDTRR (refresh operation) within the refresh-permitted period. After the down-counter is refreshed, it starts counting down from the value selected in the IWDT timeout period select bits (OFS0.IWDTTOPS[1:0]) in the Option Function Select Register 0 (OFS0).

When 00h is written, the read value is 00h. When a value other than 00h is written, the read value is FFh. For details on the refresh operation, see section 25.3.2, Refresh Operation.

25.2.2 IWDT Status Register (IWDTSR)

Address(es): IWDT.IWDTSR 4004 4404h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	REFEF	UNDFF	CNTVAL[13:0]													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b13 to b0	CNTVAL[13:0]	Counter Value	Value counted by the down-counter	R
b14	UNDFF	Underflow Flag	0: Underflow not occurred 1: Underflow occurred.	R/(W)*1
b15	REFEF	Refresh Error Flag	0: Refresh error not occurred 1: Refresh error occurred.	R/(W)*1

Note 1. Only 0 can be written to clear the flag.

CNTVAL[13:0] bits (Counter Value)

Read the CNTVAL[13:0] bits to confirm the value of the down-counter. The read value might differ from the actual count by 1.

UNDFF flag (Underflow Flag)

Read the UNDFF flag to confirm whether an underflow occurred in the down-counter. The value 1 indicates that the down-counter underflowed. Write 0 to the UNDFF flag to set the value to 0. Writing 1 has no effect.

Clearing of the UNDFF flag takes (N+2) IWDTCLK cycles and 2 PCLKB cycles. In addition, clearing of this flag is ignored for (N+2) IWDTCLK cycles following an underflow. N is specified in the IWDTCKS[3:0] bits as follows:

- When IWDTCKS[3:0] = 0000b , N = 1
- When IWDTCKS[3:0] = 0010b , N = 16
- When IWDTCKS[3:0] = 0011b , N = 32
- When IWDTCKS[3:0] = 0100b , N = 64
- When IWDTCKS[3:0] = 1111b , N = 128
- When IWDTCKS[3:0] = 0101b , N = 256.

REFEF flag (Refresh Error Flag)

Read the REFEF flag to confirm whether a refresh error occurred. The value 1 indicates that a refresh error occurred. Write 0 to the REFEF flag to set the value to 0. Writing 1 has no effect.

Clearing of the REFEF flag takes (N+2) IWDTCLK cycles and 2 PCLKB cycles. In addition, clearing of this flag is ignored for (N+2) IWDTCLK cycles following a refresh error. N is specified in the IWDTCKS[3:0] bits as follows:

- When IWDTCKS[3:0] = 0000b , N = 1
- When IWDTCKS[3:0] = 0010b , N = 16
- When IWDTCKS[3:0] = 0011b , N = 32
- When IWDTCKS[3:0] = 0100b , N = 64
- When IWDTCKS[3:0] = 1111b , N = 128
- When IWDTCKS[3:0] = 0101b , N = 256.

25.2.3 Option Function Select Register 0 (OFS0)

For information on the Option Function Select Register 0 (OFS0), see section 6.2.1, Option Function Select Register 0 (OFS0).

IWDTTOPS[1:0] bits (IWDT Timeout Period Select)

The IWDTTOPS[1:0] bits select the timeout period, the period until the down-counter underflows, from 128, 512, 1024, or 2048 cycles, taking the divided clock specified by the IWDTCKS[3:0] bits as 1 cycle. After the down-counter is refreshed, the combination of the IWDTCKS[3:0] and IWDTTOPS[1:0] bits determines the number of IWDTCLK cycles until the counter underflows.

Table 25.2 lists the relationship between the IWDTCKS[3:0] and IWDTTOPS[1:0] bit settings, the timeout period, and the number of IWDTCLK cycles.

Table 25.2 Timeout period settings

IWDTCKS[3:0] bits				IWDTTOPS[1:0] bits				
b7	b6	b5	b4	b1	b0	Clock division ratio	Timeout period (number of cycles)	Cycles of IWDTCLK
0	0	0	0	0	0	IWDTCLK	128	128
				0	1		512	512
				1	0		1024	1024
				1	1		2048	2048
0	0	1	0	0	0	IWDTCLK/16	128	2048
				0	1		512	8192
				1	0		1024	16384
				1	1		2048	32768
0	0	1	1	0	0	IWDTCLK/32	128	4096
				0	1		512	16384
				1	0		1024	32768
				1	1		2048	65536
0	1	0	0	0	0	IWDTCLK/64	128	8192
				0	1		512	32768
				1	0		1024	65536
				1	1		2048	131072
1	1	1	1	0	0	IWDTCLK/128	128	16384
				0	1		512	65536
				1	0		1024	131072
				1	1		2048	262144
0	1	0	1	0	0	IWDTCLK/256	128	32768
				0	1		512	131072
				1	0		1024	262144
				1	1		2048	524288

IWDTCKS[3:0] bits (IWDT-Dedicated Clock Frequency Division Ratio Select)

The IWDTCKS[3:0] bits specify the division ratio of the clock used for the down-counter. The division ratio can be selected from the IWDT-dedicated clock (IWDTCLK) divided by 1, 16, 32, 64, 128, and 256. Combined with the IWDTTOPS[1:0] bit setting, a count period between 128 and 524288 cycles of the IWDTCLK clock can be selected for the IWDT.

IWDTRPES[1:0] bits (IWDT Window End Position Select)

The IWDTRPES[1:0] bits specify the window end position that indicates the refresh-permitted period. 75%, 50%, 25%, or 0% of the timeout period can be selected for the window end position. The selected window end position should be a

value smaller than the value for the window start position. If the window start position is set to a value less than or equal to the window end position, the window start position setting is enable and the window end position is set to 0%.

IWDTRPSS[1:0] bits (IWDT Window Start Position Select)

The IWDTRPSS[1:0] bits specify the window start position that indicates the refresh-permitted period. 100%, 75%, 50%, or 25% of the timeout period can be selected for the window start position. The window start position should be a value greater than the value for the window end position. If the window start position is smaller than or equal to the window end position, the window end position is set to 0%.

Table 25.3 lists the counter values for the window start and end positions and Figure 25.2 shows the refresh-permitted period set in the IWDTRPSS[1:0], IWDTRPES[1:0], and IWDTTOPS[1:0] bits.

Table 25.3 Relationship between timeout period and window start and end counter values

IWDTTOPS[1:0] bits		Timeout period		Window start and end counter value			
b1	b0	Cycles	Counter value	100%	75%	50%	25%
0	0	128	007Fh	007Fh	005Fh	003Fh	001Fh
0	1	512	01FFh	01FFh	017Fh	00FFh	007Fh
1	0	1024	03FFh	03FFh	02FFh	01FFh	00FFh
1	1	2048	07FFh	07FFh	05FFh	03FFh	01FFh

IWDTRPSS[1:0] bits		IWDTRPES[1:0] bits		Window	
b11	b10	b9	b8	Start (%)	End (%)
1	1	1	1	100	0
		1	0		25
		0	1		50
		0	0		75
1	0	1	1	75	0
		1	0		25
		0	1		50
		0	0		75
0	1	1	1	50	0
		1	0		25
		0	1		50
		0	0		75
0	0	1	1	25	0
		1	0		25
		0	1		50
		0	0		75

Note: If window end position setting ≥ window start position setting, the window end position setting is set to 0%.

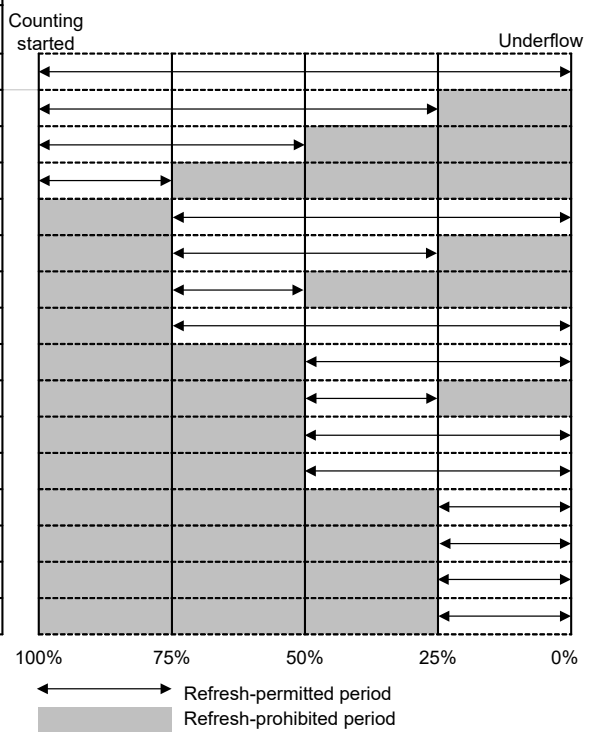


Figure 25.2 IWDTRPSS[1:0] and [IWDTRPES[1:0] bit settings and refresh-permitted period

IWDTRSTIRQS bit (IWDT Reset Interrupt Request Select)

The IWDTRSTIRQS bit specifies the behavior when an underflow or a refresh error occurred. Set this bit to 1 to select reset output. Set this bit to 0 to select interrupt.

IWDTSTPCTL bit (IWDT Stop Control)

The IWDTSTPCTL bit selects whether to stop counting on transition to Sleep mode, Snooze mode, or Software Standby mode.

25.3 Operation

25.3.1 Auto Start Mode

When the IWDT start mode select bit (OFS0.IWDTSTRT) in the Option Function Select Register 0 is 0, auto start mode is selected, otherwise the IWDT is disabled.

Within the reset state, the setting values for the following in the Option Function Select Register 0 (OFS0) are set in the IWDT registers:

- Clock division ratio
- Window start and end positions
- Timeout period
- Reset output or interrupt request
- Counter stop control on transitions to low power mode.

When the reset state is released, the counter automatically starts counting down from the value selected in the IWDT timeout period select bits (OFS0.IWDTTOPS[1:0]).

After that, as long as the program continues normal operation and the counter is refreshed within the refresh-permitted period, the value in the counter is reset each time the counter is refreshed and down-counting continues. The IWDT does not output the reset signal or non-maskable interrupt request/interrupt request as long as the counting continues. However, if the down-counter underflows because the down-counter cannot be refreshed because of a program runaway, of if a refresh error occurs because the counter was refreshed outside the refresh-permitted period, the IWDT outputs the reset signal or non-maskable interrupt request/interrupt request (IWDT_NMIUNDF).

After the reset signal or non-maskable interrupt request/interrupt request is generated, the counter reloads the timeout period after counting for 1 cycle. The value of the timeout period is set in the down-counter and counting restarts.

Reset output or interrupt request output can be selected in the IWDT Reset Interrupt Request Select bit (OFS0.IWDTRSTIRQS). The interrupt enable that initiates NMI can be selected with the IWDT Underflow/Refresh Error Interrupt Enable bit (NMIER.IWDTEN).

Figure 25.3 shows an example of operation under the following conditions:

- Auto start mode (OFS0.IWDTSTRT = 0)
- IWDT behavior selection: interrupt (OFS0.IWDTRSTIRQS = 0)
- Non-maskable Interrupt: IWDT Underflow/Refresh Error Interrupt Enable (NMIER.IWDTEN = 1)
- The window start position is 75% (OFS0.IWDTRPSS[1:0] = 10b)
- The window end position is 25% (OFS0.IWDTRPES[1:0] = 10b).

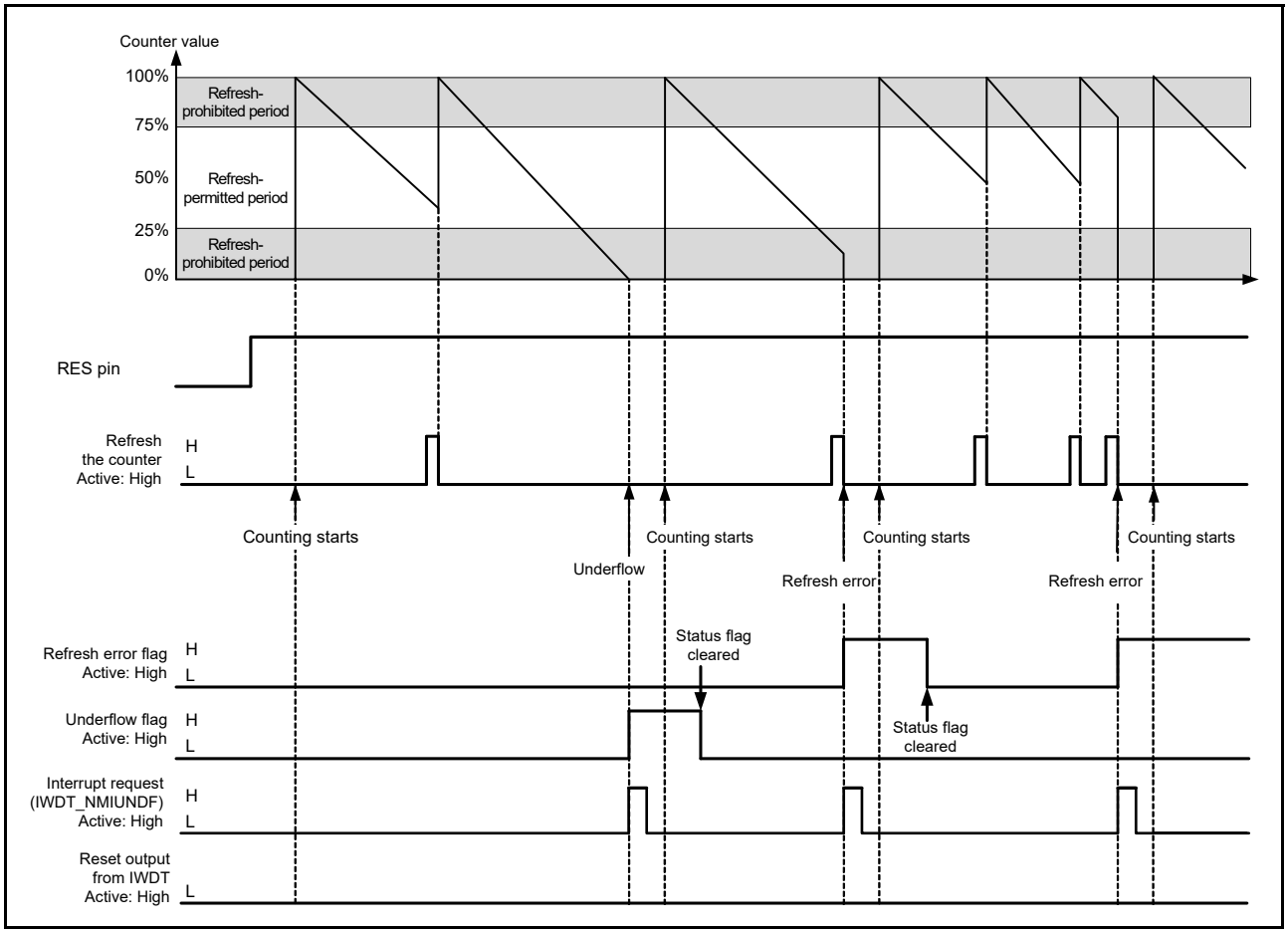


Figure 25.3 Operation example in auto start mode

25.3.2 Refresh Operation

The down-counter is refreshed by writing the values 00h and then FFh to the IWDT Refresh Register (IWDTRR). If a value other than FFh is written after 00h, the down-counter is not refreshed. If an invalid value is written, correct refreshing resumes on a write of 00h and then FFh to the IWDTRR.

When writes are made in the order of 00h (first time) → 00h (second time), and if FFh is written after that, the writing order 00h → FFh is satisfied. Writes of 00h (n-1th time) → 00h (nth time) → FFh are valid, and the refresh is performed correctly. Even when the first value written before 00h is not 00h, correct refreshing is performed as long as the operation contains the write sequence of 00h → FFh.

Correct refreshing is also performed when a register other than IWDTRR is accessed or IWDTRR is read between writing 00h and writing FFh to IWDTRR.

[Example write sequences that are valid to refresh the counter]

- 00h → FFh
- 00h (n-1th time) → 00h (nth time) → FFh
- 00h → access to another register or read from IWDTRR → FFh.

[Example write sequences that are not valid to refresh the counter]

- 23h (a value other than 00h) → FFh
- 00h → 54h (a value other than FFh)
- 00h → AAh (00h and a value other than FFh) → FFh.

When 00h is written to IWDTRR outside the refresh-permitted period and when FFh is written to IWDTRR in the

refresh-permitted period, the writing sequence is valid and refreshing completes.

After FFh is written to the IWDTRR register, refreshing the counter requires up to 4 cycles of the signal for counting (the IWDT-dedicated clock frequency division ratio select bits (OFS0.IWDTCKS[3:0]) to determine how many cycles of the IWDT-dedicated clock (IWDTCLK) make up 1 cycle for counting. To meet this requirement, complete writing FFh to IWDTRR 4 count cycles before the end of the refresh-permitted period or a counter underflow. The value of the counter can be checked using the counter bits (IWDTSR.CNTVAL[13:0]).

[Example refreshing timings]

- When the window start position is set to 01FFh, if 00h is written to IWDTRR before 01FFh is reached (0202h, for example), refreshing occurs if FFh is written to IWDTRR after the value of the IWDTSR.CNTVAL[13:0] bits reaches 01FFh
- When the window end position is set to 01FFh, refreshing occurs if 0203h (4 count cycles before 01FFh) or a greater value is read from the IWDTSR.CNTVAL[13:0] bits immediately after a write of 00h → FFh to IWDTRR
- When the refresh-permitted period continues until count 0000h, refreshing can be performed immediately before an underflow. In this case, if 0003h (4 count cycles before an underflow) or a greater value is read from the IWDTSR.CNTVAL[13:0] bits immediately after a write of 00h → FFh to IWDTRR, no underflow occurs and refreshing is performed.

Figure 25.4 shows the IWDT refresh-operation waveforms when PCLKB > IWDTCLK and the clock division ratio is IWDTCLK.

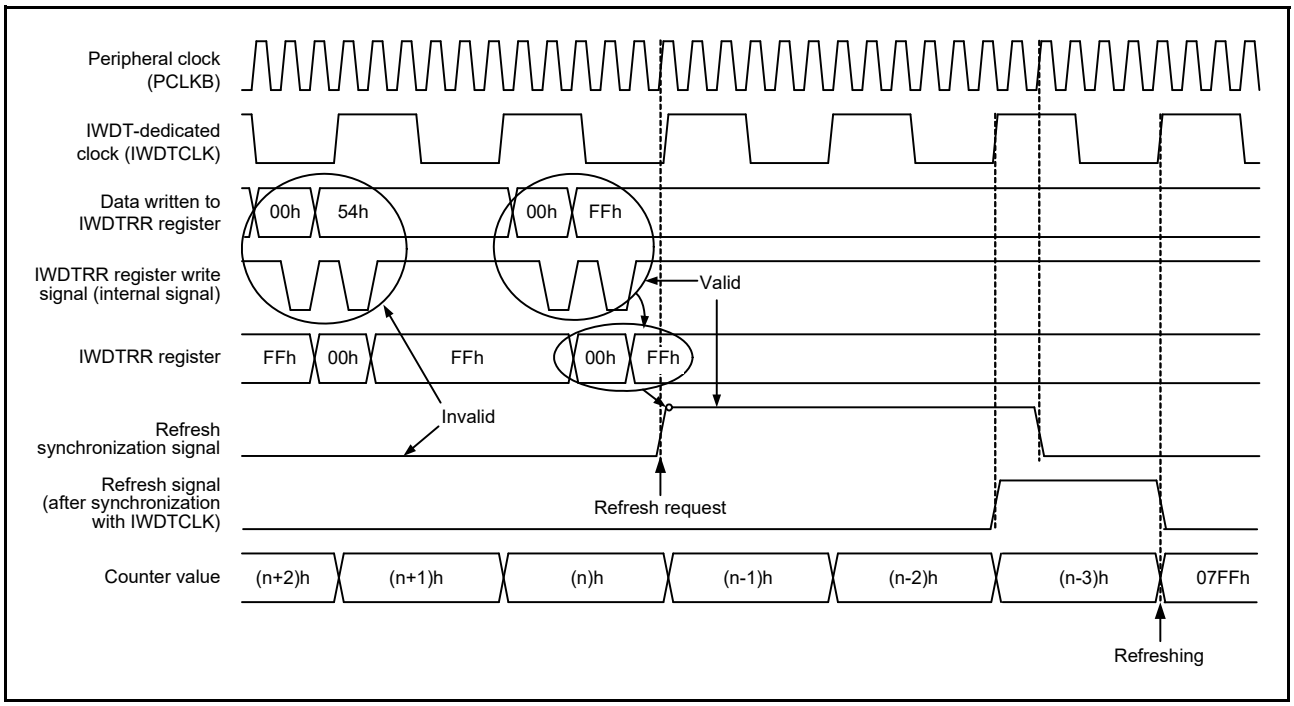


Figure 25.4 IWDT refresh operation waveforms when OFS0.IWDTCKS[3:0] = 0000b, OFS0.IWDTTOPS[1:0] = 11b

25.3.3 Status Flags

The refresh error (IWDTSR.REFEF) and underflow (IWDTSR.UNDFF) flags retain the source of the reset signal output or the source of the interrupt request from the IWDT. Therefore, after a release from the reset state or interrupt request generation, read the IWDTSR.REFEF and UNDFF flags to check for the reset or interrupt source. For each flag, writing 0 clears the bit and writing 1 has no effect.

Leaving the status flags unchanged does not affect operation. If the flags are not cleared at the time of the next reset or interrupt request from the IWDT, the earlier reset or interrupt source is cleared and the new reset or interrupt source is written. After 0 is written to each flag, up to 3 IWDTCLK cycles and 2 PCLKB cycles are required before the value is reflected.

25.3.4 Reset Output

When the IWDT reset interrupt request select bit (OFS0.IWDTRSTIRQS) in the Option Function Select Register 0 (OFS0) is set to 1, a reset signal is output when an underflow in the counter or a refresh error occurs. Counting down starts automatically after the reset output.

25.3.5 Interrupt Sources

When the IWDT reset interrupt request select bit (OFS0.IWDTRSTIRQS) in the Option Function Select Register 0 (OFS0) is set to 0, an interrupt (IWDT_NMIUNDF) signal is generated when an underflow in the counter or a refresh error occurs. This interrupt can be used as a non-maskable interrupt or an interrupt. For details, see section 12, Interrupt Controller Unit (ICU).

Table 25.4 IWDT interrupt source

Name	Interrupt source	DTC activation
IWDT_NMIUNDF	Down-counter underflow Refresh error	Not possible

25.3.6 Reading the Down-counter Value

As the counter in IWDT-dedicated clock (IWDTCLK), the counter value cannot be read directly. The IWDT synchronizes the counter value with the peripheral clock (PCLKB) and stores it in the down-counter value bits (IWDTSR.CNTVAL[13:0]) of the IWDT status register. Check these bits to obtain the counter value indirectly. Reading the counter value requires multiple PCLKB clock cycles (up to 4 clock cycles), and the read counter value might differ from the actual counter value by a value of 1.

Figure 25.5 shows the processing for reading the IWDT counter value when PCLKB > IWDTCLK and the clock division ratio is IWDTCLK.

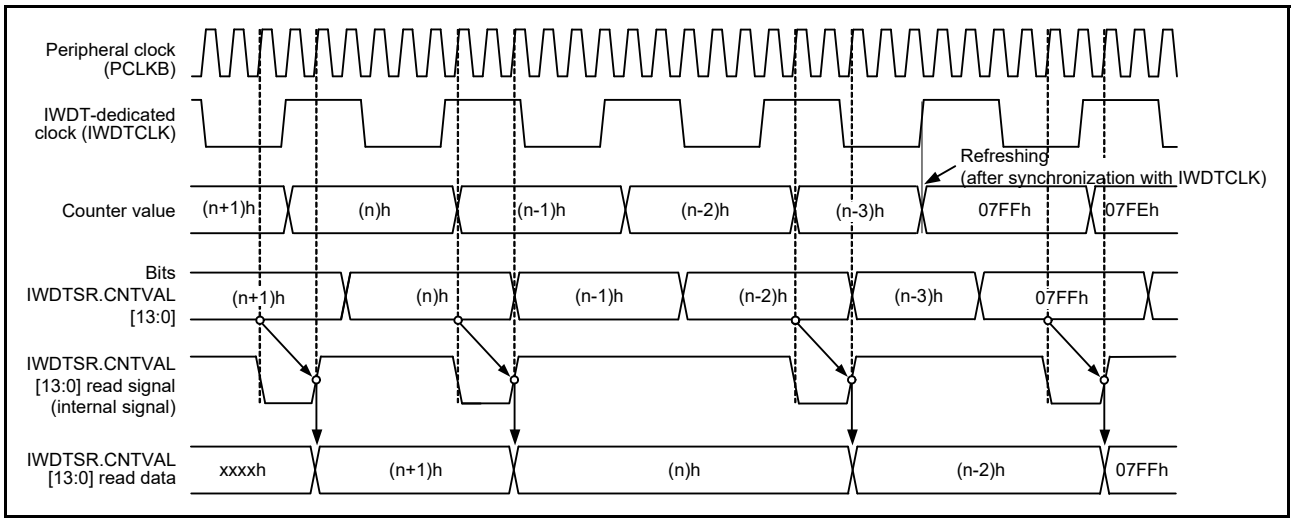


Figure 25.5 Processing for reading IWDT counter value when OFS0.IWDTCKS[3:0] = 0000b, OFS0.IWDTTOPS[1:0] = 11b

25.4 Link Operation by ELC

The IWDT is capable of link operation for a specified module when the interrupt request signal is used as an event signal by the event link controller (ELC). The event signal is output by the counter underflow or refresh error.

An event signal is output regardless of the setting of the OFS0.WDTRSTIRQS bit. An event signal can also be output when the next interrupt source while the refresh error flag (IWDTSR.REFEF) or underflow flag (IWDTSR.UNDFF) is 1. For details, see section 16, Event Link Controller (ELC).

25.5 Usage Notes

25.5.1 Refresh Operations

While configuring the refresh time, consider variations in the range of errors given the accuracy of PCLKB and IWDTCLK. Set values that ensure refreshing is possible.

25.5.2 Clock Division Ratio Setting

Satisfy the frequency of the peripheral module clock (PCLKB) ≥ 4 × (the frequency of the count clock source after division).

26. USB 2.0 Full-Speed Module (USBFS)

26.1 Overview

The MCU incorporates a USB 2.0 Full-Speed module (USBFS) and supports revision 1.2 of the Battery Charging Specification.

The USBFS is a USB controller that operates as a device controller. The module supports full-speed and low-speed transfers as defined in the Universal Serial Bus (USB) 2.0 Specification. The USBFS has an internal USB transceiver and supports control transfers, bulk transfers, and interrupt transfers.

The USBFS has buffer memory for data transfers, providing a maximum of five pipes. PIPE4 to PIPE7 can be assigned any endpoint number based on the peripheral devices or the communication requirements for your system.

Table 26.1 lists the USBFS specifications, Figure 26.1 shows a block diagram, and Table 26.2 lists the I/O pins.

Table 26.1 USBFS specifications

Parameter	Specifications
Features	• USB Device Controller (UDC) and USB 2.0 transceiver supporting device controller (one channel) • Self-power mode or bus power mode can be selected • Revision 1.2 of battery charging specification is supported • The USB LDO regulator is used to power the internal USB transceiver.
	• Full-speed transfer (12 Mbps) and low-speed transfer (1.5 Mbps) are supported • Control transfer stage control function • Device state control function • Auto response function for SET_ADDRESS request • SOF interpolation function.
Communication data transfer type	• Control transfer • Bulk transfer • Interrupt transfer.
Pipe configuration	• Buffer memory for USB communication • Up to five pipes can be selected, including the default control pipe • PIPE4 to PIPE7 can be assigned any endpoint number.
	Transfer conditions that can be set for each pipe: • PIPE0: Control transfer with 64-byte single buffer • PIPE4 and PIPE5: Bulk transfer with 64-byte double buffer • PIPE6 and PIPE7: Interrupt transfer with 64-byte single buffer.
Others	• Reception end function using transaction count • Function that changes the BRDY interrupt event notification timing (BFRE) • NAK setting function for response PID generated on transfer end (SHTNAK) • On-chip pull-up and pull-down resistors of USB_DP/USB_DM • HOCO clock that can be used as USB clock.
Module-stop function	Module-stop state can be set to reduce power consumption

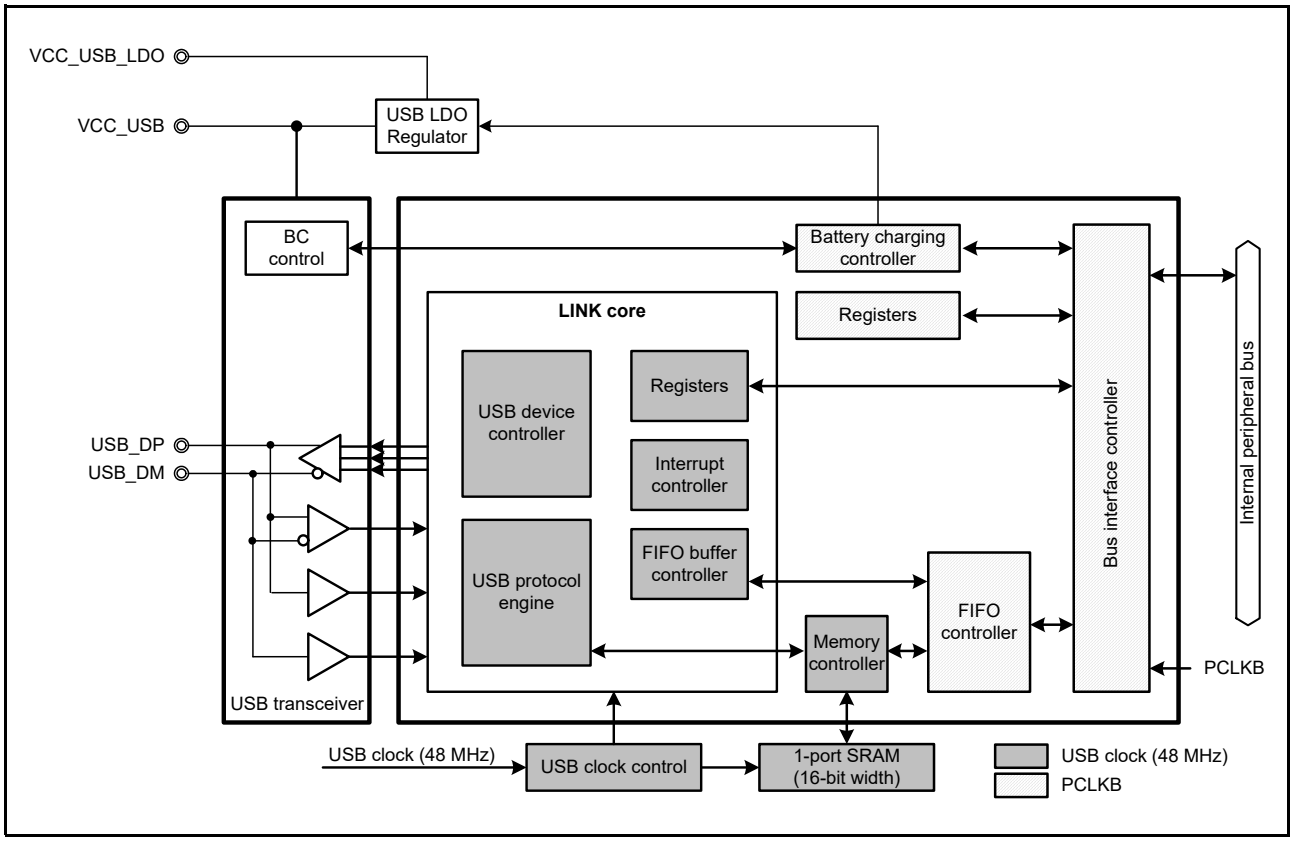


Figure 26.1 USBFS block diagram

Table 26.2 USBFS pin configuration

Port	Pin name	I/O	Function
USBFS	USB_DP	I/O	D+ I/O pin for the USB on-chip transceiver. Must be connected to the D+ pin of the USB bus.
	USB_DM	I/O	D- I/O pin for the USB on-chip transceiver. Must be connected to the D- pin of the USB bus.
	USB_VBUS	Input	USB cable connection monitor pin. Must be connected to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected.*1
Common	VCC_USB	I/O	Input: USB transceiver input supply voltage. Output: USB LDO regulator output supply voltage. This pin must be connected to an external capacitor.
	VCC_USB_LDO	Input	USB LDO regulator input supply voltage
	VSS_USB	Input	USB ground pin

Note 1. P407 is 5-V tolerant.

26.2 Register Descriptions

26.2.1 System Configuration Control Register (SYSCFG)

Address(es): USBFS.SYSCFG 4009 0000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SCKE	—	CNEN	—	—	—	DPRPU	DMRPU	—	—	USBE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	USBE	USBFS Operation Enable	0: USBFS operation disabled 1: USBFS operation enabled.	R/W
b2, b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3	DMRPU	D- Line Resistor Control*1	0: Line pull-up disabled 1: Line pull-up enabled.	R/W
b4	DPRPU	D+ Line Resistor Control*1	0: Line pull-up disabled 1: Line pull-up enabled.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	CNEN	CNEN Single-Ended Receiver Enable	0: Single end receiver operation disabled 1: Single end receiver operation enabled.	R/W
b9	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b10	SCKE	USB Clock Enable*2	0: Stop clock supply to the USB 1: Enable clock supply to the USB.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Do not enable the DMRPU and DPRPU bits at the same time.
Note 2. After writing 1 to the SCKE bit, read it and confirm it is set to 1.

USBE bit (USBFS Operation Enable)

The USBE bit enables or disables operation of the USBFS.

Changing the USBE bit from 1 to 0 initializes the bits listed in Table 26.3. Only change this bit while the SCKE bit is 1.

Table 26.3 Registers initialized by writing 0 to SYSCFG.USBE bit

Register	Bit
SYSSTS0	LNST[1:0]
DVSTCTR0	RHST[2:0]
INTSTS0	DVSQ[2:0]
USBREQ	BREQUEST[7:0], BMREQUESTTYPE[7:0]
USBVAL	WVALUE[15:0]
USBINDX	WINDEX[15:0]
USBLENG	WLENTUH[15:0]

DMRPU bit (D- Line Resistor Control*1)

The DMRPU bit enables or disables pulling up the D- line.

When the DMRPU bit is set to 1, the bit forces a pull-up of the D- line to notify the USB host that it attached as a low-speed device. Changing the DMRPU bit from 1 to 0 allows the USB to release the D- line, thereby notifying the USB host that it detached.

DPRPU bit (D+ Line Resistor Control*1)

The DPRPU bit enables or disables pulling up the D+ line.

When the DPRPU bit is set to 1, the bit forces a pull-up of the D+ line to notify the USB host that it attached. Changing the DPRPU bit from 1 to 0 allows the USB to release the D+ line, thereby notifying the USB host that it detached.

CNEN bit (CNEN Single-Ended Receiver Enable)

Setting the CNEN bit to 1 allows the USBFS to enable the single-ended receiver and set the LNST bit to monitor the status of the D+ and D- lines.

The CNEN bit is used when the USBFS operates as a portable device for battery charging.

SCKE bit (USB Clock Enable*2)

The SCKE bit stops or enables supplying 48-MHz clock signals to the USBFS.

When this bit is 0, only SYSCFG is allowed to be read from and written to. Other USBFS-related registers should not be read from or written to.

26.2.2 System Configuration Status Register 0 (SYSSTS0)

Address(es): USBFS.SYSSTS0 4009 0004h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LNST[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	LNST[1:0]	USB Data Line Status Monitor	Indicates the status of the USB data lines, seeTable 26.4	R
b15 to b2	—	Reserved	These bits are read as 0 and cannot be modified	R

LNST[1:0] bits (USB Data Line Status Monitor)

The LNST[1:0] bits indicate the state of the USB data lines (D+ and D- lines). For details, see Table 26.4.

The LNST[1:0] bits should be read after connection processing (SYSCFG.DPRPU bit = 1).

Table 26.4 Status of USB data bus lines (D+ Line, D- Line)

LNST[1:0] bits	During full-speed operation	During low-speed operation
00b	SE0	SE0
01b	J-State	K-State
10b	K-State	J-State
11b	SE1	SE1

26.2.3 Device State Control Register 0 (DVSTCTR0)

Address(es): USBFS.DVSTCTR0 4009 0008h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	WKUP	—	—	—	—	—	RHST[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	RHST[2:0]	USB Bus Reset Status	b2 b0 0 0 0: Communication speed not determined 0 0 1: USB bus reset in progress or low-speed connection 0 1 0: USB bus reset in progress or full-speed connection.	R
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	WKUP	Wakeup Output	0: Remote wakeup signal is not output 1: Remote wakeup signal is output.	R/W
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RHST[2:0] bits (USB Bus Reset Status)

The RHST[2:0] bits indicate the status of the USB bus reset.

When the USBFS detects a USB bus reset, the RHST[2:0] bits indicate 010b if the DPRPU bit is 1 or 001b if the DMRPU is 1, and a DVST interrupt is generated.

WKUP bit (Wakeup Output)

The WKUP bit enables or disables remote wakeup signals (resume signals) to the USB bus.

The USBFS controls the output timing of the remote wakeup signals. When this bit is set to 1, the USBFS sets this bit to 0 after outputting the K-state for 10 ms. The USB 2.0 specification specifies that the USB bus idle state must be kept for 5 ms or longer before a remote wakeup signal is sent. If the USB writes 1 to this bit immediately after detecting the suspended state, the K-state is output after 2 ms.

Only write 1 to this bit when the device is in the suspended state (INTSTS0.DVSQ[2:0] bits = 1xxb) and the USB host enables the remote wakeup signal. Do not stop the internal clock when this bit is 1, even in the suspended state (SYSCFG.SCKE bit is 1).

26.2.4 CFIFO Port Register (CFIFO/CFIFOL)

(1) When the MBW bit is 1

Address(es): USBFS.CFIFO 4009 0014h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FIFOPORT[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(2) When the MBW bit is 0

Address(es): USBFS.CFIFOL 4009 0014h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	FIFOPORT[15:0]	FIFO Port	The valid bits in a FIFO port register depend on the settings of the MBW bits (CFIFOSEL.MBW) and BIGEND bits (CFIFOSEL.BIGEND) as shown in Table 26.5 and Table 26.6.	R/W

CFIFO is configured with:

- A port register (CFIFO) that handles reading of data from the FIFO buffer and writing of data to the FIFO buffer
- A port select register (CFIFOSEL) that selects the pipe assigned to the FIFO port
- A port control register (CFIFOCTR).

CFIFO has the following constraints:

- Access to the FIFO buffer for DCP control transfers is through the CFIFO port
- There are two FIFO buffer states, one giving access rights to the CPU and the other to the serial interface engine (SIE). When the SIE has access rights, the FIFO buffer cannot be accessed by the CPU.
- The FIFO buffer cannot be accessed by the DTC.

FIFOPORT[15:0] bits (FIFO Port)

When the FIFOPORT[15:0] bit is accessed, the USBFS reads the received data from the FIFO buffer or writes the transmit data to the FIFO buffer.

The CFIFO port register can be accessed only when the FRDY bit in the port control register (CFIFOCTR) is 1. The valid bits in the FIFO port register depend on the MBW and BIGEND settings in the port select register (CFIFOSEL). See Table 26.5 and Table 26.6.

Table 26.5 Endian operation in 16-bit access

CFIFOSEL.BIGEND Bit	Bits 15 to 8	Bits 7 to 0
0	N + 1 data	N + 0 data
1	N + 0 data	N + 1 data

Table 26.6 Endian operation in 8-bit access

CFIFOSEL.BIGEND Bit	Bits 15 to 8	Bits 7 to 0
0	Access prohibited*1	N + 0 data
1	Access prohibited*1	N + 0 data

Note 1. Reading from or writing to an access-prohibited area is not allowed.

26.2.5 CFIFO Port Select Register (CFIFOSEL)

Address(es): USBFS.CFIFOSEL 4009 0020h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RCNT	REW	—	—	—	MBW	—	BIGEND	—	—	ISEL	—	CURPIPE[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	CURPIPE[3:0]	CFIFO Port Access Pipe Specification	b3 b0 0 0 0 0: DCP (Default control pipe) 0 1 0 0: Pipe 4 0 1 0 1: Pipe 5 0 1 1 0: Pipe 6 0 1 1 1: Pipe 7. Other settings are prohibited.	R/W
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5	ISEL	CFIFO Port Access Direction When DCP is Selected	0: Reading from the buffer memory selected 1: Writing to the buffer memory selected.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	BIGEND	CFIFO Port Endian Control	0: Little endian 1: Big endian.	R/W
b9	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b10	MBW	CFIFO Port Access Bit Width	0: 8-bit width 1: 16-bit width.	R/W
b13 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b14	REW	Buffer Pointer Rewind	0: The buffer pointer is not rewound 1: The buffer pointer is rewound.	R/W*1
b15	RCNT	Read Count Mode	0: The DTLN[8:0] bits are cleared when all received data is read from the CFIFO. In double buffer mode, the DTLN[8:0] bit value is cleared when all data is read from only a single plane. 1: The DTLN[8:0] bits are decremented each time the received data is read from the CFIFO.	R/W

Note 1. Only 0 can be read.

CURPIPE[3:0] bits (CFIFO Port Access Pipe Specification)

The CURPIPE[3:0] bits specify the pipe number to use for reading or writing data through the CFIFO port. After writing to these bits, read them to check that the written value agrees with the read value before proceeding to the next process.

During FIFO buffer access, even when an attempt is made to change the CURPIPE[3:0] setting, the current access setting is retained until access is complete. The modification then becomes effective, therefore enabling continuous access.

ISEL bit (CFIFO Port Access Direction When DCP is Selected)

After writing a new value to the ISEL bit with the DCP as a selected pipe, read this bit to check that the written value agrees with the read value before proceeding to the next process. Set this bit and the CURPIPE[3:0] bits simultaneously.

MBW bit (CFIFO Port Access Bit Width)

The MBW bit specifies the bit width for accessing the CFIFO port.

When the selected pipe is receiving, set the CURPIPE[3:0] bits and MBW bits simultaneously. After a write to these bits starts a data read from the FIFO buffer, do not change the bits until all the data is read. When you read the FIFO buffer, read with the access size set in MBW.

When the selected pipe is transmitting, the bit width cannot be changed from 8-bit width to 16-bit width while data is written to the buffer memory.

An odd number of bytes can also be written through byte-access control even when 16-bit width is selected.

REW bit (Buffer Pointer Rewind)

The REW bit specifies whether or not to rewind the buffer pointer.

When the selected pipe is receiving, setting the REW bit to 1 while the FIFO buffer is being read allows re-reading of the FIFO buffer from the first data. In double buffering mode, this setting enables re-reading of the currently-read FIFO buffer plane from the first entry.

Do not set the REW bit to 1 while simultaneously changing the CURPIPE[3:0] bits. Before setting the REW bit to 1, be sure to check that the FRDY bit is 1.

To rewrite to the FIFO buffer from the first data for the transmitting pipe, use the BCLR bit.

26.2.6 CFIFO Port Control Register (CFIFOCTR)

Address(es): USBFS.CFIFOCTR 4009 0022h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BVAL	BCLR	FRDY	—	—	—	—	DTLN[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b8 to b0	DTLN[8:0]	Receive Data Length	Indicate the length of the received data. These bits indicate different values depending on the setting of the RCNT bit in the port select register. For details, see the description of the DTLN[8:0] bits shown in this section.	R
b12 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13	FRDY	FIFO Port Ready	0: FIFO port access disabled 1: FIFO port access enabled.	R
b14	BCLR	CPU Buffer Clear	0: Does not operate 1: Clears the buffer memory on the CPU side.	R/W*1
b15	BVAL	Buffer Memory Valid Flag	0: Invalid 1: Writing ended.	R/W

Note 1. Only 0 can be read.

DTLN[8:0] bits (Receive Data Length)

The DTLN[8:0] bits indicate the length of the received data.

While the FIFO buffer is being read, the DTLN[8:0] bits indicate different values depending on the CFIFOSEL.RCNT bit (n = 0, 1) value as follows:

- RCNT = 0:
  The USBFS sets the DTLN[8:0] bits to indicate the length of the received data until the CPU has read all the received data from a single FIFO buffer plane.
  While the PIPECFG.BFRE bit = 1, these bits retain the length of the received data until the BCLR bit is set to 1 even after all the data is read.
- RCNT = 1:
  The USBFS decrements the value indicated in the DTLN[8:0] bits each time data is read from the FIFO buffer. The value is decremented by 1 when the MBW bit = 0, and by 2 when the MBW bit = 1.
  The USBFS sets these bits to 0 when all the data is read from one FIFO buffer plane. However, in double buffer mode, if data is received in one FIFO buffer plane before all the data is read from the other plane, the USBFS sets these bits to indicate the length of the received data in the former plane when all the data is read from the latter plane.

FRDY bit (FIFO Port Ready)

The FRDY bit indicates whether the FIFO port can be accessed by the CPU.

In the following cases, the USBFS sets the FRDY bit to 1 but data cannot be read by the FIFO port because there is no data to be read. In these cases, set the BCLR bit to 1 to clear the FIFO buffer, and enable transmission and reception of the next data.

- A zero-length packet is received when the FIFO buffer assigned to the selected pipe is empty
- A short packet is received and the data is completely read while the PIPECFG.BFRE bit = 1.

BCLR bit (CPU Buffer Clear)

Set the BCLR bit to 1 to clear the FIFO buffer on the CPU side for the selected pipe.

When double buffer mode is set for the FIFO buffer assigned to the selected pipe, the USBFS clears only one plane of the FIFO buffer even when both planes are read-enabled.

When the DCP is the selected pipe, setting the BCLR bit to 1 allows the USBFS to clear the FIFO buffer regardless of whether the CPU or SIE has access rights. To clear the buffer when the SIE has access rights, set the DCPCTR.PID[1:0] bits to 00b (NAK response) before setting the BCLR bit to 1.

When the selected pipe is transmitting, if 1 is written to the BVAL flag and the BCLR bit simultaneously, the USBFS clears the data that is already written, enabling transmission of a zero-length packet.

When the selected pipe is not the DCP, only write 1 to the BCLR bit while the FRDY bit in the FIFO port control register is 1 (set by the USBFS).

BVAL flag (Buffer Memory Valid Flag)

Set the BVAL flag to 1 when data is completely written to the FIFO buffer on the CPU for the pipe selected in CURPIPE[3:0].

When the selected pipe is transmitting, set the BVAL flag to 1 in the following cases:

- To transmit a short packet, set this flag to 1 after data is written
- To transmit a zero-length packet, set this flag to 1 before data is written to the FIFO buffer.

The USBFS then switches the FIFO buffer from the CPU to the SIE, enabling transmission.

When data of the maximum packet size is written for the pipe in continuous transfer mode, the USBFS sets the BVAL flag to 1 and switches the FIFO buffer from the CPU to the SIE, enabling transmission.

Only write 1 to the BVAL flag while the FRDY bit is 1 (set by the USBFS). When the selected pipe is receiving, do not set the BVAL flag to 1.

26.2.7 Interrupt Enable Register 0 (INTENB0)

Address(es): USBFS.INTENB0 4009 0030h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	VBSE	RSME	SOFE	DVSE	CTRE	BEMPE	NRDYE	BRDYE	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	BRDYE	Buffer Ready Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b9	NRDYE	Buffer Not Ready Response Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled.	R/W

Bit	Symbol	Bit name	Description	R/W
b10	BEMPE	Buffer Empty Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b11	CTRE	Control Transfer Stage Transition Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b12	DVSE	Device State Transition Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b13	SOFE	Frame Number Update Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b14	RSME	Resume Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b15	VBSE	VBUS Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled.	R/W

When a status flag in the INTSTS0 register is set to 1 and the associated interrupt request enable bit setting in the INTENB0 register is 1, the USBFS issues a USBFS interrupt request.

Regardless of the INTENB0 register setting, the status flag in the INTSTS0 register is set to 1 in response to a state change that satisfies the associated condition.

When an interrupt request enable bit in the INTENB0 register is switched from 0 to 1 while the associated status flag in the INTSTS0 register is set to 1, a USBFS interrupt is requested.

26.2.8 BRDY Interrupt Enable Register (BRDYENB)

Address(es): USBFS.BRDYENB 4009 0036h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	PIPE7BRDYE	PIPE6BRDYE	PIPE5BRDYE	PIPE4BRDYE	—	—	—	PIPE0BRDYE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PIPE0BRDYE	BRDY Interrupt Enable for PIPE0	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	PIPE4BRDYE	BRDY Interrupt Enable for PIPE4	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b5	PIPE5BRDYE	BRDY Interrupt Enable for PIPE5	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b6	PIPE6BRDYE	BRDY Interrupt Enable for PIPE6	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b7	PIPE7BRDYE	BRDY Interrupt Enable for PIPE7	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

BRDYENB enables or disables the INTSTS0.BRDY bit to be set to 1 when the BRDY interrupt is detected for each pipe.

On detecting the BRDY interrupt for the pipe associated with the bit in BRDYENB to which 1 is set by software, the USBFS sets 1 to the associated BRDYSTS.PIPEnBRDY bit (n = 0, 4 to 7) and the INTSTS0.BRDY bit. If INTENB0.BRDYE = 1 at this time, the USBFS generates the BRDY interrupt request.

While at least one PIPEnBRDY bit indicates 1, the USBFS generates the BRDY interrupt request when the corresponding interrupt enable bit in BRDYENB is modified from 0 to 1 by software.

26.2.9 NRDY Interrupt Enable Register (NRDYENB)

Address(es): USBFS.NRDYENB 4009 0038h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	PIPE7NRDYE	PIPE6NRDYE	PIPE5NRDYE	PIPE4NRDYE	—	—	—	PIPE0NRDYE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PIPE0NRDYE	NRDY Interrupt Enable for PIPE0	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	PIPE4NRDYE	NRDY Interrupt Enable for PIPE4	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b5	PIPE5NRDYE	NRDY Interrupt Enable for PIPE5	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b6	PIPE6NRDYE	NRDY Interrupt Enable for PIPE6	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b7	PIPE7NRDYE	NRDY Interrupt Enable for PIPE7	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

NRDYENB enables or disables the INTSTS0.NRDY bit to be set to 1 when the NRDY interrupt is detected for each pipe.

On detecting the NRDY interrupt for the pipe associated with the bit in NRDYENB to which 1 is set by software, the USBFS sets 1 to the associated NRDYSTS.PIPEnNRDY bit (n = 0, 4 to 7) and the INTSTS0.NRDY bit. If INTENB0.NRDYE is 1 at this time, the USBFS generates the NRDY interrupt request.

While at least one PIPEnNRDY bit indicates 1, the USBFS generates the NRDY interrupt request when the associated interrupt enable bit in NRDYENB is modified from 0 to 1 by software.

26.2.10 BEMP Interrupt Enable Register (BEMPENB)

Address(es): USBFS.BEMPENB 4009 003Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	PIPE7BEMPE	PIPE6BEMPE	PIPE5BEMPE	PIPE4BEMPE	—	—	—	PIPE0BEMPE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PIPE0BEMPE	BEMP Interrupt Enable for PIPE0	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	PIPE4BEMPE	BEMP Interrupt Enable for PIPE4	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b5	PIPE5BEMPE	BEMP Interrupt Enable for PIPE5	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b6	PIPE6BEMPE	BEMP Interrupt Enable for PIPE6	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b7	PIPE7BEMPE	BEMP Interrupt Enable for PIPE7	0: Interrupt output disabled 1: Interrupt output enabled.	R/W

Bit	Symbol	Bit name	Description	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

BEMPENB enables or disables the INTSTS0.BEMP bit to be set to 1 when the BEMP interrupt is detected for each pipe.

On detecting the BEMP interrupt for the pipe associated with the bit in BEMPENB to which 1 is set by software, the USBFS sets 1 to the associated BEMPSTS.PIPEnBEMP bit (n = 0, 4 to 7) and the INTSTS0.BEMP bit. If INTENB0.BEMPE = 1 at this time, the USBFS generates the BEMP interrupt request.

While at least one PIPEnBEMP bit in BEMPSTS indicates 1, the USBFS generates the BEMP interrupt request when the associated interrupt enable bit in BEMPENB is modified from 0 to 1 by software.

26.2.11 SOF Output Configuration Register (SOFCFG)

Address(es): USBFS.SOFCFG 4009 003Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	BRDYM	—	EDGESTS	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	EDGESTS	Edge Interrupt Output Status Monitor*1	Indicates 1 when the edge interrupt output signal is in the middle of edge processing.	R
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	BRDYM	BRDY Interrupt Status Clear Timing	0: Software clears the status 1: The USBFS clears the status when data is read from the FIFO buffer or data is written to the FIFO buffer.	R/W
b15 to b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Confirm that this bit is 0 before stopping the clock supply to the USBFS.

EDGESTS bit (Edge Interrupt Output Status Monitor)

The EDGESTS bit indicates 1 when the edge interrupt output signal is in the middle of edge processing. Confirm that this bit is 0 before stopping the clock supply to the USBFS.

BRDYM bit (BRDY Interrupt Status Clear Timing)

The BRDYM bit specifies the timing for clearing the BRDY interrupt status for each pipe.

26.2.12 Interrupt Status Register 0 (INTSTS0)

Address(es): USBFS.INTSTS0 4009 0040h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	VBINT	RESM	SOFR	DVST	CTRT	BEMP	NRDY	BRDY	VBSTS	DVSQ[2:0]			VALID	CTSQ[2:0]		
Value after reset:	0	0	0	0/1*1	0	0	0	0	0*2	0*3	0*3	0/1*3	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	CTSQ[2:0]	Control Transfer Stage	b2 b0 0 0 0: Idle or setup stage 0 0 1: Control read data stage 0 1 0: Control read status stage 0 1 1: Control write data stage 1 0 0: Control write status stage 1 0 1: Control write (no data) status stage 1 1 0: Control transfer sequence error.	R
b3	VALID	USB Request Reception	0: Setup packet is not received 1: Setup packet is received.	R/W*4
b6 to b4	DVSQ[2:0]	Device State	b6 b4 0 0 0: Powered state 0 0 1: Default state 0 1 0: Address state 0 1 1: Configured state 1 x x: Suspended state.	R
b7	VBSTS	VBUS Input Status	0: USB_VBUS pin is low 1: USB_VBUS pin is high.	R
b8	BRDY	Buffer Ready Interrupt Status	0: BRDY interrupts are not generated 1: BRDY interrupts are generated.	R
b9	NRDY	Buffer Not Ready Interrupt Status	0: NRDY interrupts are not generated 1: NRDY interrupts are generated.	R
b10	BEMP	Buffer Empty Interrupt Status	0: BEMP interrupts are not generated 1: BEMP interrupts are generated.	R
b11	CTRT	Control Transfer Stage Transition Interrupt Status	0: Control transfer stage transition interrupts are not generated 1: Control transfer stage transition interrupts are generated.	R/W*4
b12	DVST	Device State Transition Interrupt Status	0: Device state transition interrupts are not generated 1: Device state transition interrupts are generated.	R/W*4
b13	SOFR	Frame Number Refresh Interrupt Status	0: SOF interrupts are not generated 1: SOF interrupts are generated.	R/W*4
b14	RESM	Resume Interrupt Status*5	0: Resume interrupts are not generated 1: Resume interrupts are generated.	R/W*4
b15	VBINT	VBUS Interrupt Status*5	0: VBUS interrupts are not generated 1: VBUS interrupts are generated.	R/W*4

x: Don't care

Note 1. The value is 0 when the MCU is reset and 1 after a USB bus reset.
Note 2. The value is 1 when the USB_VBUS pin is high and 0 when the USB_VBUS pin is low.
Note 3. The value is 000b when the MCU is reset and 001b after a USB bus reset.
Note 4. To clear the VBINT, RESM, SOFR, DVST, CTRT, or VALID bit, write 0 only to the bits to be cleared. Write 1 to the other bits. Do not write 0 to the status bits indicating 0.
Note 5. A change in the status indicated by the VBINT and RESM bits can be detected even while the clock supply is stopped (SYSCFG.SCKE bit is 0), and the interrupts are output when the corresponding interrupt enable bits are enabled. Clear the status through software after enabling the clock supply.

DVSQ[2:0] bits (Device State)

The DVSQ[2:0] bits are initialized by a USB bus reset.

BRDY bit (Buffer Ready Interrupt Status)

The BRDY bit indicates the BRDY interrupt status.

The USBFS sets the BRDY bit to 1 when at least one PIPEnBRDY bit (n = 0, 4 to 7) is set to 1 from the PIPEBRDY bits. These bits correspond to the BRDYENB.PIPEnBRDYE bits (n = 0, 4 to 7) to which 1 is set when the USBFS detects the BRDY interrupt status in at least one pipe in the pipes for which the BRDY interrupt output is enabled by software.

For the conditions for PIPEnBRDY status assertion, see section 26.3.3.1, BRDY interrupt.

The USBFS sets the BRDY bit to 0 when 0 is written by software to all the PIPEnBRDY bits associated with the PIPEnBRDYE bits that are set to 1. The BRDY bit cannot be set to 0 even if 0 is written to this bit by software.

NRDY bit (Buffer Not Ready Interrupt Status)

The USBFS sets the NRDY bit to 1 when at least one PIPEnNRDY bit (n = 0, 4 to 7) is set to 1 from the PIPENRDY bits. These bits correspond to the PIPEnNRDYE bits (n = 0, 4 to 7) to which 1 is set when the USBFS detects the NRDY interrupt status in at least one pipe in the pipes for which software enables the NRDY interrupt output.

For the conditions for PIPEnNRDY status assertion, see section 26.3.3.2, NRDY interrupt.

The USBFS sets the NRDY bit to 0 when 0 is written by software to all the PIPEnNRDY bits that correspond to the PIPEnNRDYE bits that are set to 1. The NRDY bit cannot be set to 0 even if 0 is written to this bit by software.

BEMP bit (Buffer Empty Interrupt Status)

The USBFS sets the BEMP bit to 1 when at least one PIPEnBEMP bit (n = 0, 4 to 7) is set to 1 in the PIPEnBEMP bits. These bits correspond to the PIPEnBEMPE bits (n = 0, 4 to 7) to which 1 is set when the USBFS detects the BEMP interrupt status in at least one pipe from the pipes for which the BEMP interrupt output is enabled by software.

For the conditions for PIPEnBEMP status assertion, see section 26.3.3.3, BEMP interrupt.

The USBFS sets the BEMP bit to 0 when 0 is written by software to all the PIPEnBEMP bits that correspond to the PIPEnBEMPE bits that are set to 1. The BEMP bit cannot be set to 0 even if 0 is written to this bit by software.

CTRT bit (Control Transfer Stage Transition Interrupt Status)

The USBFS updates the value of the CTSQ[2:0] bits and sets the CTRT bit to 1 when detecting a change in the control transfer stage.

When a control transfer stage transition interrupt is generated, clear the status before the USBFS detects the next control transfer stage transition.

DVST bit (Device State Transition Interrupt Status)

The USBFS updates the DVSQ[2:0] value and sets the DVST bit to 1 when detecting a change in the device state.

When a device state transition interrupt is generated, clear the status before the USBFS detects the next device state transition.

SOFR bit (Frame Number Refresh Interrupt Status)

The USBFS sets the SOFR bit to 1 when updating the frame number. A frame number refresh interrupt is detected every 1 ms.

The USBFS can detect an SOFR interrupt through the internal interpolation function even when a damaged SOF packet is received from the USB host.

RESM bit (Resume Interrupt Status)

The USBFS sets the RESM bit to 1 when detecting the falling edge of the signal on the USB_DP pin in the suspended state (DVSQ[2:0] = 1xxb).

VBINT bit (VBUS Interrupt Status)

The USBFS sets the VBINT bit to 1 when detecting a level change (high to low or low to high) in the USB_VBUS pin input value. The USBFS sets the VBSTS bit to indicate the USB_VBUS pin input value. When the VBUS interrupt is generated, use software to repeat the reading of the VBSTS bit until the same value is read three or more times to eliminate chattering.

26.2.13 BRDY Interrupt Status Register (BRDYSTS)

Address(es): USBFS.BRDYSTS 4009 0046h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	PIPE7BRDY	PIPE6BRDY	PIPE5BRDY	PIPE4BRDY	—	—	—	PIPE0BRDY
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PIPE0BRDY	BRDY Interrupt Status for PIPE0*2	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	PIPE4BRDY	BRDY Interrupt Status for PIPE4*2	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b5	PIPE5BRDY	BRDY Interrupt Status for PIPE5*2	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b6	PIPE6BRDY	BRDY Interrupt Status for PIPE6*2	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b7	PIPE7BRDY	BRDY Interrupt Status for PIPE7*2	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. When the SOFCFG.BRDYM bit is set to 0, to clear the status indicated by the bits in BRDYSTS, write 0 only to the bits to be cleared. Write 1 to the other bits.

Note 2. When the SOFCFG.BRDYM bit is set to 0, clear the BRDY Interrupts before accessing the FIFO.

26.2.14 NRDY Interrupt Status Register (NRDYSTS)

Address(es): USBFS.NRDYSTS 4009 0048h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	PIPE7NRDY	PIPE6NRDY	PIPE5NRDY	PIPE4NRDY	—	—	—	PIPE0NRDY
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PIPE0NRDY	NRDY Interrupt Status for PIPE0	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	PIPE4NRDY	NRDY Interrupt Status for PIPE4	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b5	PIPE5NRDY	NRDY Interrupt Status for PIPE5	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b6	PIPE6NRDY	NRDY Interrupt Status for PIPE6	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b7	PIPE7NRDY	NRDY Interrupt Status for PIPE7	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. To clear the status indicated by the bits in NRDYSTS, write 0 only to the bits to be cleared. Write 1 to the other bits.

26.2.15 BEMP Interrupt Status Register (BEMPSTS)

Address(es): USBFS.BEMPSTS 4009 004Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	PIPE7BEMP	PIPE6BEMP	PIPE5BEMP	PIPE4BEMP	—	—	—	PIPE0BEMP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PIPE0BEMP	BEMP Interrupt Status for PIPE0	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	PIPE4BEMP	BEMP Interrupt Status for PIPE4	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b5	PIPE5BEMP	BEMP Interrupt Status for PIPE5	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b6	PIPE6BEMP	BEMP Interrupt Status for PIPE6	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b7	PIPE7BEMP	BEMP Interrupt Status for PIPE7	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. To clear the status indicated by the bits in BEMPSTS, write 0 only to the bits to be cleared. Write 1 to the other bits.

26.2.16 Frame Number Register (FRMNUM)

Address(es): USBFS.FRMNUM 4009 004Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	FRNM[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b10 to b0	FRNM[10:0]	Frame Number	Latest frame number	R
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

FRNM[10:0] bits (Frame Number)

The FRNM[10:0] bits indicate the latest frame number for the USBFS after issuing of an SOF packet every 1 ms or writing to the FRNM[10:0] bits at the SOF packet reception.

26.2.17 USB Request Type Register (USBREQ)

Address(es): USBFS.USBREQ 4009 0054h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BREQUEST[7:0]								BMREQUESTTYPE[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	BMREQUESTTYPE[7:0]	Request Type	These bits store the USB request bmRequestType value	R
b15 to b8	BREQUEST[7:0]	Request	These bits store the USB request bRequest value	R

USBREQ stores setup requests for control transfers. The received values of bRequest and bmRequestType are stored.

USBREQ is initialized by a USB bus reset.

BMREQUESTTYPE[7:0] bits (Request Type)

The BMREQUESTTYPE[7:0] bits hold the value of the bmRequestType field of a USB request.

These bits indicate the value of the USB request data in the setup transactions for reception. Writing to these bits has no effect.

BREQUEST[7:0] bits (Request)

The BREQUEST[7:0] bits store the bRequest value of the USB request.

These bits indicate the value of the USB request data in setup transactions for reception. Writing to these bits has no effect.

26.2.18 USB Request Value Register (USBVAL)

Address(es): USBFS.USBVAL 4009 0056h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	WVALUE[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	WVALUE[15:0]	Value	These bits store the USB request wValue value	R

The received value of wValue is stored in USBVAL. USBVAL is initialized by a USB bus reset.

WVALUE[15:0] bits (Value)

The WVALUE[15:0] bits store the wValue value of the USB request.

These bits indicate the value of the wValue field in USB requests received in setup transactions for reception. Writing to the WVALUE[15:0] bits has no effect.

26.2.19 USB Request Index Register (USBINDX)

Address(es): USBFS.USBINDX 4009 0058h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	WINDEX[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	WINDEX[15:0]	Index	These bits store the USB request wIndex value	R

USBINDX stores setup requests for control transfers. The received value of wIndex is stored.

USBINDX is initialized by a USB bus reset.

WINDEX[15:0] bits (Index)

The WINDEX[15:0] bits hold the value of the wIndex field of a USB request.

These bits indicate the value of the wIndex field in USB requests received in setup transactions for reception. Writing to the WINDEX[15:0] bits has no effect.

26.2.20 USB Request Length Register (USBLENG)

Address(es): USBFS.USBLENG 4009 005Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	WLENTUH[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	WLENTUH[15:0]	Length	These bits store the USB request wLength value	R

USBLENG stores setup requests for control transfers. The received value of wLength is stored.

USBLENG is initialized by a USB bus reset.

WLENTUH[15:0] bits (Length)

The WLENTUH[15:0] bits hold the value of the wLength field of a USB request.

These bits indicate the value of the wLength field in USB requests received in setup transactions for reception. Writing to the WLENTUH[15:0] bits has no effect.

26.2.21 DCP Configuration Register (DCPCFG)

Address(es): USBFS.DCPCFG 4009 005Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	SHTNAK	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit name	Description	R/W
b7	SHTNAK	Pipe Disabled at End of Transfer*1	0: Pipe continued at the end of transfer 1: Pipe disabled at the end of transfer.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Modify this bit while PID is NAK. Before changing this bit after modifying the DCPCTR.PID[1:0] bits for the DCP from BUF to NAK, check that the DCPCTR.PBUSY bit is 0. However, if the USB changes the PID[1:0] bits to NAK, checking the PBUSY bit through software is not required.

SHTNAK bit (Pipe Disabled at End of Transfer)

The SHTNAK bit specifies whether to modify PID to NAK on the transfer end when the selected pipe is receiving.

The SHTNAK bit is valid when the selected pipe is receiving.

When the SHTNAK bit is set to 1, the USBFS modifies the DCPCTR.PID[1:0] bits for the DCP to NAK on determining that a transfer has ended. The USB determines that the transfer has ended on the following condition:

- A short packet (including a zero-length packet) is successfully received.

26.2.22 DCP Maximum Packet Size Register (DCPMAXP)

Address(es): USBFS.DCPMAXP 4009 005Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	MXPS[6:0]						
Value after reset:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b6 to b0	MXPS[6:0]	Maximum Packet Size*1	These bits set the maximum amount of data (maximum packet size) in payloads for the DCP. b6 b0 0 0 0 1 0 0 0: 8 bytes 0 0 1 0 0 0 0: 16 bytes 0 0 1 1 0 0 0: 24 bytes 0 1 0 0 0 0 0: 32 bytes 0 1 0 1 0 0 0: 40 bytes 0 1 1 0 0 0 0: 48 bytes 0 1 1 1 0 0 0: 56 bytes 1 0 0 0 0 0 0: 64 bytes 1 0 0 1 0 0 0: 72 bytes 1 0 1 0 0 0 0: 80 bytes 1 0 1 1 0 0 0: 88 bytes 1 1 0 0 0 0 0: 96 bytes 1 1 0 1 0 0 0: 104 bytes 1 1 1 0 0 0 0: 112 bytes 1 1 1 1 0 0 0: 120 bytes. Other settings are prohibited.	R/W
b15 to b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Modify the MXPS[6:0] bits while PID is NAK. Before changing these bits after modifying the DCPCTR.PID[1:0] bits for the DCP from BUF to NAK, check that the DCPCTR.PBUSY bit is 0. However, if the USB changes the PID[1:0] bits to NAK, checking the PBUSY bit through software is not required. After modifying the MXPS[6:0] bits and the DCP is set to the CURPIPE[3:0] bits in the port select register, clear the buffer by setting the BCLR bit in the port control register to 1.

MXPS[6:0] bits (Maximum Packet Size*1)

The MXPS[6:0] bits specify the maximum amount of data (maximum packet size) in payloads for the DCP. The initial value of the bits is 40h (64 bytes).

Ensure that the setting of the MXPS[6:0] bits is in compliance with the USB 2.0 Specification. Do not write to the FIFO buffer or set PID = BUF while the setting of the MXPS[6:0] bits is 0.

26.2.23 DCP Control Register (DCPCTR)

Address(es): USBFS.DCPCTR 4009 0060h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BSTS	—	—	—	—	—	—	SQCLR	SQSET	SQMON	PBUSY	—	—	CCPL	PID[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	PID[1:0]	Response PID	b1 b0 0 0: NAK response 0 1: BUF response (depending on the buffer state) 1 0: STALL response 1 1: STALL response.	R/W
b2	CCPL	Control Transfer End Enable	0: Invalid 1: Completion of control transfer is enabled.	R/W
b4, b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	PBUSY	Pipe Busy	0: DCP is not used for the transaction 1: DCP is used for the transaction.	R
b6	SQMON	Sequence Toggle Bit Monitor	0: DATA0 1: DATA1.	R
b7	SQSET	Sequence Toggle Bit Set*2	0: Invalid 1: Specifies DATA1.	R/W*1
b8	SQCLR	Sequence Toggle Bit Clear*2	0: Invalid 1: Specifies DATA0.	R/W*1
b14 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	BSTS	Buffer Status	0: Buffer access is disabled 1: Buffer access is enabled.	R

Note 1. This bit is read as 0.
Note 2. Write 1 to the SQSET and SQCLR bits while PID is NAK. Before changing these bits after modifying the PID[1:0] bits for the DCP from BUF to NAK, check that the PBUSY bit is 0. However, if the USB changes the PID[1:0] bits to NAK, checking the PBUSY bit through software is not required.

PID[1:0] bits (Response PID)

The PID[1:0] bits control the response type of the USBFS during control transfer.

The USBFS modifies the setting of the PID[1:0] bits as follows:

- The USBFS modifies the PID[1:0] bits to NAK on receiving the setup packet. The USBFS sets the INTSTS0.VALID bit to 1. The setting of the PID[1:0] bits cannot be modified until the VALID bit is set to 0 by software.
- The USBFS sets PID to STALL (11b) on receiving data of a size that exceeds the maximum packet size when the PID[1:0] bits are set to BUF by software
- The USBFS sets PID to STALL (1xb) on detecting the control transfer sequence error
- The USBFS sets PID to NAK on detecting the USB bus reset.

The USBFS does not check the setting of the PID[1:0] bits while the SET_ADDRESS request is processed.

The PID[1:0] bits are initialized by a USB bus reset.

CCPL bit (Control Transfer End Enable)

Setting the CCPL bit to 1 enables the status stage of the control transfer to be completed.

When the CCPL bit is set to 1 by software while the corresponding PID[1:0] bits are set to BUF, the USBFS completes the control transfer status stage.

During control read transfer, the USBFS transmits the ACK handshake in response to the OUT transaction from the USB host, and transmits the zero-length packet in response to the IN transaction from the USB host during control write or no-data control transfer. However, on detecting the SET_ADDRESS request, the USBFS operates in auto response mode from the setup stage up to status stage completion, irrespective of the setting of the CCPL bit.

The USBFS modifies the CCPL bit from 1 to 0 on receiving a new setup packet. A value of 1 cannot be written to the CCPL bit by software while the INTSTS0.VALID bit is 1. The CCPL bit is initialized by a USB bus reset.

PBUSY bit (Pipe Busy)

The PBUSY bit indicates whether DCP is used for the transaction when the USB changes the PID[1:0] bits from BUF to NAK.

The USBFS modifies the PBUSY bit from 0 to 1 at the start of the USB transaction for the selected pipe, and modifies the PBUSY bit from 1 to 0 on completion of one transaction.

Reading the PBUSY bit after PID is set to NAK by software allows you to check whether modification of the pipe settings is possible.

For details, see section 26.3.4.1, Pipe control register switching procedures.

SQMON bit (Sequence Toggle Bit Monitor)

The SQMON bit indicates the expected value of the sequence toggle bit for the next transaction during the DCP transfer.

The USBFS allows the SQMON bit to toggle on successful completion of the transaction. However, the SQMON bit is not allowed to toggle when a DATA-PID mismatch occurs during the transfer in the receiving direction.

The USBFS sets the SQMON bit to 1 (specifies DATA1 as the expected value) on successful reception of the setup packet.

The USBFS does not reference the SQMON bit during the IN/OUT transaction of the status stage, and does not allow the SQMON bit to toggle on normal completion.

SQSET bit (Sequence Toggle Bit Set*2)

The SQSET bit specifies DATA1 as the expected value of the sequence toggle bit for the next transaction during the DCP transfer.

Do not set the SQCLR and SQSET bits to 1 simultaneously.

SQCLR bit (Sequence Toggle Bit Clear*2)

The SQCLR bit specifies DATA0 as the expected value of the sequence toggle bit for the next transaction during the DCP transfer. The SQCLR bit indicates 0.

Do not set the SQCLR and SQSET bits to 1 simultaneously.

BSTS bit (Buffer Status)

The BSTS bit indicates whether DCP FIFO buffer access is enabled or disabled.

The meaning of the BSTS bit varies as follows depending on the CFIFOSEL.ISEL setting:

- When the ISEL bit = 0, the BSTS bit indicates whether the received data can be read from the buffer
- When the ISEL bit = 1, the BSTS bit indicates whether the data to be transmitted can be written to the buffer.

26.2.24 Pipe Window Select Register (PIPESEL)

Address(es): USBFS.PIPESEL 4009 0064h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	PIPESEL[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	PIPESEL[3:0]	Pipe Window Select	b3 b0 0 0 0 0: No pipe selected 0 1 0 0: PIPE4 0 1 0 1: PIPE5 0 1 1 0: PIPE6 0 1 1 1: PIPE7. Other settings are prohibited.	R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Set PIPE4 to PIPE7 using PIPESEL, PIPECFG, PIPEMAXP, PIPEnCTR, PIPEnTRE, and PIPEnTRN.

After selecting the pipe with the PIPESEL register, set the pipe functions using PIPECFG and PIPEMAXP. The PIPEnCTR, PIPEnTRE, and PIPEnTRN registers can be set independently of the pipe selection in the PIPESEL register.

PIPESEL[3:0] bits (Pipe Window Select)

The PIPESEL[3:0] bits select the pipe number associated with PIPECFG and PIPEMAXP that are used for data writing and reading.

Selecting a pipe number through the PIPESEL[3:0] bits allows writing to and reading from PIPECFG and PIPEMAXP associated with the selected pipe number.

When PIPESEL[3:0] = 0000b, 0 is read from all of the bits in PIPECFG and PIPEMAXP. Writing to these bits is invalid.

26.2.25 Pipe Configuration Register (PIPECFG)

Address(es): USBFS.PIPECFG 4009 0068h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TYPE[1:0]		—	—	—	BFRE	DBLB	—	SHTNAK	—	—	DIR	EPNUM[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	EPNUM[3:0]	Endpoint Number*1	These bits specify the endpoint number for the selected pipe. Setting 0000b means an unused pipe.	R/W
b4	DIR	Transfer Direction*2 *3	0: Receiving direction 1: Transmitting direction.	R/W
b6, b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	SHTNAK	Pipe Disabled at End of Transfer*1	0: Pipe assignment continued at transfer end 1: Pipe assignment disabled at transfer end.	R/W
b8	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b9	DBLB	Double Buffer Mode*2 *3	0: Single buffer 1: Double buffer.	R/W
b10	BFRE	BRDY Interrupt Operation Specification*2 *3	0: BRDY interrupt on transmitting or receiving data 1: BRDY interrupt on completion of reading data.	R/W

Bit	Symbol	Bit name	Description	R/W
b13 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15, b14	TYPE[1:0]	Transfer Type*1	• PIPE4 and PIPE5 b15 b14 0 0: Pipe not used 0 1: Bulk transfer 1 0: Setting prohibited 1 1: Setting prohibited. • PIPE6 and PIPE7 b15 b14 0 0: Pipe not used 0 1: Setting prohibited 1 0: Interrupt transfer 1 1: Setting prohibited.	R/W

Note 1. Only set the TYPE[1:0], SHTNAK, and EPNUM[3:0] bits while PID is NAK. Before setting these bits, check that the PIPEnCTR.PBUSY bit is 0, then change the PIPEnCTR.PID[1:0] bits for the selected pipe from BUF to NAK. If the USB changes the PID[1:0] bits to NAK, checking the PBUSY bit through software is not required.

Note 2. Only set the BFRE, DBLB, and DIR bits while PID is NAK and before the pipe is selected in the CURPIPE[3:0] bits in the port select register. Before setting these bits, check that the PIPEnCTR.PBUSY bit is 0, then change the PIPEnCTR.PID[1:0] bits for the selected pipe from BUF to NAK. If the USB changes the PID[1:0] bits to NAK, checking the PIPEnCTR.PBUSY bit through software is not required.

Note 3. To change the BFRE, DBLB, and DIR bits after completing USB communication on the selected pipe, write 1 and then 0 to the PIPEnCTR.ACLRM bit continuously through software to clear the FIFO buffer assigned to the selected pipe while the PID and CURPIPE[3:0] bits are in the state described in Note 2.

PIPECFG specifies the transfer type, buffer memory access direction, and endpoint numbers for PIPE4 to PIPE7. It also selects single or double buffer mode, and whether to continue or disable pipe operation at the end of transfer.

EPNUM[3:0] bits (Endpoint Number*1)

The EPNUM[3:0] bits specify the endpoint number for the selected pipe. Setting 0000b indicates an unused pipe. Set these bits so that the combination of the DIR and EPNUM[3:0] settings is different for two or more pipes (EPNUM[3:0] bits can be set to 0000b for all pipes).

DIR bit (Transfer Direction*2 *3)

The DIR bit specifies the transfer direction for the selected pipe. When the DIR bit is set to 0 by software, the USBFS uses the selected pipe in the receiving direction, and when software set the DIR bit to 1, the USBFS uses the selected pipe in the transmitting direction.

SHTNAK bit (Pipe Disabled at End of Transfer*1)

The SHTNAK bit specifies whether to modify PID to NAK on the end of transfer when the selected pipe is in the receiving direction. The SHTNAK bit is valid when the selected pipe is PIPE4 and PIPE5 in the receiving direction.

When the SHTNAK bit is set to 1 by software for the selected pipe in the receiving direction, the USBFS modifies the PIPEnCTR.PID[1:0] bits associated with the selected pipe to NAK on determining the end of the transfer. The USBFS determines that the transfer has ended on any of the following conditions:

- A short packet (including a zero-length packet) is successfully received
- The transaction counter is used and the number of packets specified by the counter are successfully received.

DBLB bit (Double Buffer Mode*2 *3)

The DBLB bit selects either single or double buffer mode for the FIFO buffer used by the selected pipe. The DBLB bit is valid when PIPE4 and PIPE5 are selected.

BFRE bit (BRDY Interrupt Operation Specification*2 *3)

The BFRE bit specifies the BRDY interrupt generation timing from the USBFS to the CPU for the selected pipe.

When the BFRE bit is set to 1 by software and the selected pipe is receiving, the USBFS detects the transfer completion and generates the BRDY interrupt after reading the relevant packet.

When the BRDY interrupt is generated as specified, write 1 to the BCLR bit in the port control register with software. The FIFO buffer assigned to the selected pipe is not enabled for reception until 1 is written to the BCLR bit.

When the BFRE bit is set to 1 by software and the selected pipe is transmitting, the USBFS does not generate the BRDY interrupt. For details, see section 26.3.3.1, BRDY interrupt.

TYPE[1:0] bits (Transfer Type*1)

The TYPE[1:0] bits select the transfer type for the pipe selected in the PIPESEL.PIPESEL[3:0] bits.

Before setting PID to BUF for the selected pipe (before starting USB communication using the selected pipe), set the TYPE[1:0] bits to a value other than 00b.

26.2.26 Pipe Maximum Packet Size Register (PIPEMAXP)

Address(es): USBFS.PIPEMAXP 4009 006Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	MXPS[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0/1 *1	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b8 to b0	MXPS[8:0]	Maximum Packet Size*2	• PIPE4 and PIPE5: 8 bytes (008h), 16 bytes (010h), 32 bytes (020h), 64 bytes (040h) (Bits [8:7] and [2:0] are not provided.) • PIPE6 and PIPE7: 1 byte (001h) to 64 bytes (040h) (Bits [8:7] are not provided.)	R/W
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The value of these bits is 000h when no pipe is selected in the PIPESEL.PIPESEL[3:0] bits and 040h when a pipe is selected.
Note 2. Only set the MXPS[8:0] bits while PID is NAK and before the pipe is selected in the CURPIPE[3:0] bits in the port select register. Before setting these bits, check that the PIPEnCTR.PBUSY bit is 0, then change the PIPEnCTR.PID[1:0] bits for the selected pipe from BUF to NAK. If the PID[1:0] bits are changed to NAK by the USB, checking the PBUSY bit through software is not required.

PIPEMAXP specifies the maximum packet size for PIPE4 to PIPE7.

MXPS[8:0] bits (Maximum Packet Size*2)

The MXPS[8:0] bits specify the maximum data payload (maximum packet size) for the selected pipe.

These bits must be set to the appropriate value for each transfer type based on the USB 2.0 Specification. When MXPS[8:0] = 0, do not write to the FIFO buffer or set PID to BUF.

26.2.27 PIPEn Control Registers (PIPEnCTR) (n = 4 to 7)

PIPEnCTR (n = 4 and 5)

Address(es): USBFS.PIPE4CTR 4009 0076h, USBFS.PIPE5CTR 4009 0078h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BSTS	INBUFM	—	—	—	ATREPM	ACLRM	SQCLR	SQSET	SQMON	PBUSY	—	—	—	PID[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	PID[1:0]	Response PID	b1 b0 0 0: NAK response 0 1: BUF response (depending on the buffer state) 1 0: STALL response 1 1: STALL response.	R/W
b4 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	PBUSY	Pipe Busy	0: The selected pipe is not used for the transaction 1: The selected pipe is used for the transaction.	R
b6	SQMON	Sequence Toggle Bit Confirmation	0: DATA0 1: DATA1.	R
b7	SQSET	Sequence Toggle Bit Set*2	0: Write disabled 1: Specifies DATA1.	R/W*1
b8	SQCLR	Sequence Toggle Bit Clear*2	0: Write disabled 1: Specifies DATA0.	R/W*1
b9	ACLRM	Auto Buffer Clear Mode*3	0: Disabled 1: Enabled (all buffers are initialized).	R/W
b10	ATREPM	Auto Response Mode*2	0: Auto response is disabled 1: Auto response is enabled.	R/W
b13 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b14	INBUFM	Transmit Buffer Monitor	0: There are no data to be transmitted in the buffer memory. 1: There is data to be transmitted in the buffer memory.	R
b15	BSTS	Buffer Status	0: Buffer access by the CPU is disabled 1: Buffer access by the CPU is enabled.	R

Note 1. Only 0 can be read.
Note 2. Only set the ATREPM bit or write 1 to the SQCLR or SQSET bit while PID is NAK. Before setting these bits, check that the PBUSY bit is 0, then change the PID[1:0] bits for the selected pipe from BUF to NAK. If the USB changes the PID[1:0] bits to NAK, checking the PBUSY bit through software is not required.
Note 3. Only set the ACLRM bit while PID[1:0] is NAK and before the pipe is selected in the CURPIPE[3:0] bits in the port select register. Before setting this bit, check that the PBUSY bit is 0, then change the PID[1:0] bits for the selected pipe from BUF to NAK. If the USB changes the PID[1:0] bits to NAK, checking the PBUSY bit through software is not required.

PIPEnCTR can be set for any pipe selection in the PIPESEL register.

PID[1:0] bits (Response PID)

The PID[1:0] bits specify the response type for the next transaction on the selected pipe. The default setting of the PID[1:0] bits is NAK. Modify the setting of the PID[1:0] bits to BUF to use the associated pipe for USBFS transfer. Table 26.7 shows the basic operation of the USBFS (when there are no errors in the communication packets) based on the PID[1:0] bit setting.

After changing the PID[1:0] setting from BUF to NAK through software during USBFS communication on the selected pipe, check that the PBUSY bit is 1 to determine if USBFS transfer on the selected pipe has actually entered the NAK state. If the USBFS changes the PID[1:0] bits to NAK, checking the PBUSY bit through software is not required.

The USBFS changes the PID[1:0] setting in the following cases:

- The USBFS sets PID to NAK on recognizing completion of the transfer when the selected pipe is receiving and the PIPECFG.SHTNAK bit for the selected pipe is set to 1 by software

- The USBFS sets PID to STALL (11b) on receiving a data packet with a payload exceeding the maximum packet size of the selected pipe
- The USBFS sets PID to NAK on detecting a USB bus reset.

To specify the response type, set the PID[1:0] bits as follows:

- To transition from NAK (00b) to STALL, set 10b
- To transition from BUF (01b) to STALL, set 11b
- To transition from STALL (11b) to NAK, set 10b and then 00b
- To transition from STALL to BUF, transition to NAK and then BUF.

PBUSY bit (Pipe Busy)

The PBUSY bit indicates whether the selected pipe is currently used for the transaction.

The USBFS modifies the PBUSY bit from 0 to 1 at the start of the USBFS transaction for the selected pipe, and modifies the PBUSY bit from 1 to 0 on completion of one transaction.

Reading the PBUSY bit with software after PID is set to NAK allows you to check whether changing the pipe settings is possible. For details, see section 26.3.4.1, Pipe control register switching procedures.

SQMON bit (Sequence Toggle Bit Confirmation)

The SQMON bit indicates the expected value of the sequence toggle bit for the next transaction of the selected pipe. The SQMON bit is not allowed to toggle when a DATA-PID mismatch occurs during the transfer in the receiving direction.

SQSET bit (Sequence Toggle Bit Set*2)

Setting the SQSET bit to 1 through software allows the USB to set DATA1 as the expected value of the sequence toggle bit for the next transaction of the selected pipe. The USBFS sets the SQSET bit to 0.

SQCLR bit (Sequence Toggle Bit Clear*2)

Setting the SQCLR bit to 1 through software allows the USBFS to set DATA0 as the expected value of the sequence toggle bit for the next transaction of the selected pipe. The USBFS sets the SQCLR bit to 0.

ACLRM bit (Auto Buffer Clear Mode*3)

The ACLRM bit enables or disables auto buffer clear mode for the selected pipe.

To completely delete the information in the FIFO buffer assigned to the selected pipe, write 1 and then 0 to the ACLRM bit consecutively.

Table 26.8 shows the information cleared by writing 1 and 0 to the ACLRM bit consecutively and the cases in which clearing the information is required.

ATREPM bit (Auto Response Mode*2)

The ATREPM bit enables or disables auto response mode for the selected pipe.

This bit can be set to 1 when the selected pipe is for bulk transfer. When the ATREPM bit is set to 1, the USBFS responds to the token from the USB host as follows:

- When the selected pipe is set for Bulk IN transfers (PIPECFG.TYPE[1:0] = 01b and PIPECFG.DIR bit = 1):
  - When the ATREPM bit = 1 and PID = BUF, the USB transmits a zero-length packet in response to the IN token
  - The USB updates the sequence toggle bit (DATA-PID) each time the USB receives ACK from the USB host. In a single transaction, the IN token is received, a zero-length packet is transmitted, and ACK is received). The USB does not generate the BRDY or BEMP interrupt.
- When the selected pipe is for Bulk OUT transfer (PIPECFG.TYPE[1:0] = 01b and PIPECFG.DIR = 0):
  - When the ATREPM bit = 1 and PID = BUF, the USB returns NAK in response to the OUT token and generates an NRDY interrupt.

For USB communication in auto response mode, set the ATREPM bit to 1 while the FIFO buffer is empty. Do not write

to the FIFO buffer during USBFS communication in auto response mode.

INBUFM bit (Transmit Buffer Monitor)

The INBUFM bit indicates the FIFO buffer status for the selected pipe in the transmitting direction.

When the selected pipe is transmitting (PIPECFG.DIR = 1), the USBFS sets this bit to 1 when the CPU completes writing data to at least one FIFO buffer plane.

The USBFS sets the INBUFM bit to 0 when it completes transmitting the data from the FIFO buffer plane to which all the data is written. In double buffer mode (PIPECFG.DBLB = 1), the USBFS sets the INBUFM bit to 0 when it completes transmitting the data from the two FIFO buffer planes before the CPU completes writing data to one FIFO buffer plane.

The INBUFM bit indicates the same value as the BSTS bit when the selected pipe is receiving (PIPECFG.DIR = 0).

BSTS bit (Buffer Status)

The BSTS bit indicates the FIFO buffer status for the selected pipe.

The meaning of the BSTS bit depends on the settings of PIPECFG.DIR and PIPECFG.BFRE as shown in Table 26.9.

Table 26.7 Operation of USBFS based on PID[1:0] bit setting

Bits PID[1:0]	Transfer type	Transfer direction (DIR bit)	Operation of USBFS
00b (NAK)	Bulk or interrupt	Operation does not depend on the setting	Returns NAK in response to the token from the USB host
01b (BUF)	Bulk	Receiving direction (DIR bit = 0)	Receives data and returns ACK in response to the OUT token from the USB host if the FIFO buffer associated with the selected pipe is ready for reception
	Interrupt	Receiving direction (DIR bit = 0)	Receives data and returns ACK in response to the OUT token from the USB host if the FIFO buffer associated with the selected pipe is ready for reception
	Bulk or interrupt	Transmitting direction (DIR bit = 1)	Transmits data in response to the token from the USB host if the associated FIFO buffer is ready for transmission. Returns NAK if not ready.
10b (STALL) or 11b (STALL)	Bulk or interrupt	Operation does not depend on the setting	Returns STALL in response to the token from the USB host

Table 26.8 Information cleared by USBFS by setting ACLRM = 1

No.	Information cleared by ACLRM bit manipulation	Cases in which clearing information is required
1	All the information in the FIFO buffer assigned to the selected pipe (both FIFO buffer planes are cleared when double buffer mode is selected)	When the pipe is to be initialized
2	Internal flags of the PIPECFG.BFRE bit	When the PIPECFG.BFRE setting is modified
3	FIFO buffer toggle control	When the PIPECFG.DBLB setting is modified
4	Internal flags of the transaction count	When the transaction count function is forcibly terminated

Table 26.9 Operation of BSTS bit

DIR bit	BFRE bit	BSTS bit function
0	0	The received data can be read from the FIFO buffer. The received data is completely read from the FIFO buffer.
	1	The received data that can be read from the FIFO buffer is set to 1 by software after the received data is completely read from the FIFO buffer
1	0	The transmit data can be written to the FIFO buffer. The transmit data is completely written to the FIFO buffer.
	1	Setting prohibited

PIPEnCTR (n = 6 and 7)

Address(es): USBFS.PIPE6CTR 4009 007Ah, USBFS.PIPE7CTR 4009 007Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BSTS	—	—	—	—	—	ACLRM	SQCLR	SQSET	SQMON	PBUSY	—	—	—	PID[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	PID[1:0]	Response PID	b1 b0 0 0: NAK response 0 1: BUF response (depending on the buffer state) 1 0: STALL response 1 1: STALL response.	R/W
b4 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	PBUSY	Pipe Busy	0: The selected pipe is not used at the USB bus 1: The selected pipe is used at the USB bus.	R
b6	SQMON	Sequence Toggle Bit Confirmation	0: DATA0 1: DATA1.	R
b7	SQSET	Sequence Toggle Bit Set*2	0: Invalid 1: Specifies DATA1.	R/W *1
b8	SQCLR	Sequence Toggle Bit Clear*2	0: Invalid 1: Specifies DATA0.	R/W *1
b9	ACLRM	Auto Buffer Clear Mode*2,*3	0: Auto buffer clear mode is disabled 1: Auto buffer clear mode is enabled (all buffers are initialized).	R/W
b14 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	BSTS	Buffer Status	0: Buffer access is disabled 1: Buffer access is enabled.	R

Note 1. Only 0 can be read. Only 1 can be written.

Note 2. Only write 1 to the SQCLR or SQSET bit while PID is NAK. Before setting these bits, check that the PBUSY bit is 0, and then change the PID[1:0] bits for the selected pipe from BUF to NAK. If the USB changes the PID[1:0] bits to NAK, checking the PBUSY bit through software is not required.

Note 3. Only set the ACLRM bit while PID is NAK and before the pipe is selected in the CURPIPE[3:0] bits in the port select register. Before setting this bit, check that the PBUSY bit is 0, then change the PID[1:0] bits for the selected pipe from BUF to NAK. If the USB changes the PID[1:0] bits to NAK, checking the PBUSY bit through software is not required.

PID[1:0] bits (Response PID)

The PID[1:0] bits specify the response type for the next transaction of the selected pipe.

The default setting of the PID[1:0] bits is NAK. Change the PID[1:0] setting to BUF to use the selected pipe for USBFS transfer. Table 26.7 shows the basic operation (when there are no errors in the transmitted and received packets) of the USB depending on the PID[1:0] setting.

After changing the PID[1:0] setting from BUF to NAK through software during USBFS communication on the selected pipe, check that the PBUSY bit is 1 to determine if USBFS transfer on the selected pipe has actually entered the NAK state. If the USBFS changes the PID[1:0] bits to NAK, checking the PBUSY bit through software is not required.

The USBFS changes the PID[1:0] setting in the following cases:

- The USBFS sets PID to NAK on completion of the transfer when the selected pipe is receiving and the PIPECFG.SHTNAK bit for the selected pipe is set to 1 by software
- The USBFS sets PID to STALL (11b) on receiving a data packet with a payload exceeding the maximum packet size of the selected pipe
- The USBFS sets PID to NAK on detecting a USB bus reset.

To specify each response type, set the PID[1:0] bits as follows:

- To transition from NAK (00b) to STALL, set 10b

- To transition from BUF (01b) to STALL, set 11b
- To transition from STALL (11b) to NAK, set 10b and then 00b
- To transition from STALL to BUF, transition to NAK and then BUF.

PBUSY bit (Pipe Busy)

The PBUSY bit indicates whether the selected pipe is currently used for the transaction.

The USBFS changes the PBUSY bit from 0 to 1 at the start of the USBFS transaction for the selected pipe, and changes the PBUSY bit from 1 to 0 on completion of one transaction. Reading the PBUSY bit by software after PID is set to NAK allows you to check whether changing the pipe setting is possible.

SQMON bit (Sequence Toggle Bit Confirmation)

The SQMON bit indicates the expected value of the sequence toggle bit for the next transaction of the selected pipe. The USBFS toggles the SQMON bit on successful completion of the transaction. However, the USBFS does not toggle the SQMON bit when a DATA-PID mismatch occurs during the transfer in the receiving direction.

SQSET bit (Sequence Toggle Bit Set)

Setting the SQSET bit to 1 through software allows the USBFS to set DATA1 as the expected value of the sequence toggle bit for the next transaction of the selected pipe. The USBFS sets the SQSET bit to 0.

SQCLR bit (Sequence Toggle Bit Clear)

Setting the SQCLR bit to 1 through software allows the USB to set DATA0 as the expected value of the sequence toggle bit for the next transaction of the selected pipe. The USB sets the SQCLR bit to 0.

ACLRM bit (Auto Buffer Clear Mode)

The ACLRM bit enables or disables auto buffer clear mode for the selected pipe. To completely clear the data in the FIFO buffer assigned to the selected pipe, write 1 and then 0 to the ACLRM bit continuously.

Table 26.10 shows the information cleared by writing 1 and 0 to the ACLRM bit continuously and the cases in which this processing is required.

BSTS bit (Buffer Status)

The BSTS bit indicates the FIFO buffer status for the selected pipe. The meaning of the BSTS bit depends on the PIPECFG.DIR and PIPECFG.BFRE settings, as shown in Table 26.9.

Table 26.10 Information cleared by USB by setting ACLRM bit to 1

No.	Information cleared by ACLRM bit manipulation	Cases in which clearing information is required
1	All the information in the FIFO buffer assigned to the selected pipe	When the pipe is initialized
2	Internal flags of the PIPECFG.BFRE bit	When the PIPECFG.BFRE setting is modified
3	Internal flags of the transaction count	When the transaction count function is forcibly terminated

26.2.28 PIPEn Transaction Counter Enable Register (PIPEnTRE) (n = 4 and 5)

Address(es): USBFS.PIPE4TRE 4009 009Ch, USBFS.PIPE5TRE 4009 00A0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	TRENB	TRCLR	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit name	Description	R/W
b8	TRCLR	Transaction Counter Clear	0: Invalid 1: The current counter value is cleared.	R/W
b9	TRENB	Transaction Counter Enable	0: Transaction counter disabled 1: Transaction counter enabled.	R/W
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Only change each bit in PIPEnTRE while PID is NAK. Before setting these bits, check that the PIPEnCTR.PBUSY bit is 0, then change the PIPEnCTR.PID[1:0] bits for the selected pipe from BUF to NAK. If the USB changes the PID[1:0] bits to NAK, checking the PBUSY bit through software is not required.

TRCLR bit (Transaction Counter Clear)

When the TRCLR bit is set to 1, the USBFS clears the current value of the transaction counter associated with the selected pipe and then sets the TRCLR bit to 0.

TRENB bit (Transaction Counter Enable)

The TRENB bit enables or disables the transaction counter.

For the pipe in the receiving direction, setting the TRENB bit to 1 after setting the total number of the packets to be received in the PIPEnTRN.TRNCNT[15:0] bits through software allows the USBFS to control hardware as follows, on having received the number of packets equal to the TRNCNT[15:0] setting.

- While the PIPECFG.SHTNAK bit is 1, the USBFS changes the PID bits to NAK for the associated pipe on having received the number of packets equal to the TRNCNT[15:0] setting
- While the PIPECFG.BFRE bit is 1, the USBFS asserts the BRDY interrupt on having received the number of packets equal to the TRNCNT[15:0] setting and then reading the last received data.

For the transmitting pipe, set the TRENB bit to 0. When the transaction counter is not used, set the TRENB bit to 0. When the transaction counter is used, set the TRNCNT[15:0] bits before setting the TRENB bit to 1. Set the TRENB bit to 1 before receiving the first packet to be counted by the transaction counter.

26.2.29 PIPEn Transaction Counter Register (PIPEnTRN) (n = 4 and 5)

Address(es): USBFS.PIPE4TRN 4009 009Eh, USBFS.PIPE5TRN 4009 00A2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TRNCNT[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	TRNCNT[15:0]	Transaction Counter	• When written to: Specifies the total number of packets (number of transactions) to be received in the associated PIPE. • When read from: Indicates the specified number of transactions if the PIPEnTRE.TRENB bit is 0. Indicates the number of currently counted transactions if the PIPEnTRE.TRENB bit is 1.	R/W

The PIPEnTRN registers retain their current setting during a USB bus reset.

TRNCNT[15:0] bits (Transaction Counter)

The USBFS increments the value of the TRNCNT[15:0] bits by 1 when all of the following conditions are satisfied on receiving the packet:

- The PIPEnTRE.TRENB bit is 1
- (TRNCNT[15:0] set value ≠ current counter value + 1) on receiving the packet

- The payload of the received packet aligns with the PIPEMAXP.MXPS[8:0] setting.

The USBFS sets the value of the TRNCNT[15:0] bits to 0 when any of the following conditions are satisfied:

- All of the following conditions are satisfied:
  - The PIPEnTRE.TRENB bit is 1
  - (TRNCNT[15:0] set value = current counter value + 1) on receiving the packet
  - The payload of the received packet aligns with the PIPEMAXP.MXPS[8:0] setting.
- All of the following conditions are satisfied:
  - The PIPEnTRE.TRENB bit is 1
  - The USBFS has received a short packet.
- All of the following conditions are satisfied:
  - The PIPEnTRE.TRENB bit is 1
  - The PIPEnTRE.TRCLR bit is set to 1 by software.

For the transmitting pipe, set the TRNCNT[15:0] bits to 0. When the transaction counter is not used, set the TRNCNT[15:0] bits to 0.

Setting the number of transactions to be transferred to the TRNCNT[15:0] bits is only enabled when the PIPEnTRE.TRENB bit is 0. To set the number of transactions to be transferred, set the TRCLR bit to 1 to clear the current counter value before setting the PIPEnTRE.TRENB bit to 1.

26.2.30 USB Module Control Register (USBMC)

Address(es): USBFS.USBMC 4009 00CCh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	VDCEN	—	—	—	—	—	—	VDDUSBE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit	Symbol	Bit name	Description	R/W
b0	VDDUSBE	USB Reference Power Supply Circuit On/Off Control	0: USB reference power supply circuit off 1: USB reference power supply circuit on.	R/W
b1	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b6 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	VDCEN	USB Regulator On/Off Control	0: USB regulator off 1: USB regulator on.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

VDDUSBE bit (USB Reference Power Supply Circuit On/Off Control)

The USB reference power supply circuit generates the reference voltage for battery charging. Set this bit to 1 when using the battery charging function.

VDCEN bit (USB Regulator On/Off Control)

The VDCEN bit controls the USB regulator circuit. Set this bit to 1 when using the USB regulator circuit.

26.2.31 BC Control Register 0 (USBBCCTRL0)

Address(es): USBFS.USBBCCTRL0 4009 00B0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PDDETSTS0	CHGDETSTS0	BATCHGE0	—	VDMSRCE0	IDPSINKE0	VDPSRCE0	IDMSINKE0	IDPSRCE0	RPDME0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RPDME0	D- Pin Pull-Down Control	0: Pull-down off 1: Pull-down on.	R/W
b1	IDPSRCE0	D+ Pin IDPSRC Output Control	0: Stop 1: 10 μA output.	R/W
b2	IDMSINKE0	D- Pin 0.6 V Input Detection (Comparator and Sink) Control	0: Detection off 1: Detection on (comparator and sink current on).	R/W
b3	VDPSRCE0	D+ Pin VDPSRC (0.6 V) Output Control	0: Stop 1: 0.6 V output.	R/W
b4	IDPSINKE0	D+ Pin 0.6 V Input Detection (Comparator and Sink) Control	0: Detection off 1: Detection on (comparator and sink current on).	R/W
b5	VDMSRCE0	D- Pin VDMSRC (0.6 V) Output Control	0: Stop 1: 0.6 V output.	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	BATCHGE0	BC (Battery Charger) Function Ch0 General Enable Control	0: Disabled 1: Enabled.	R/W
b8	CHGDETSTS0	D- Pin 0.6 V Input Detection Status*1	0: Not detected 1: Detected.	R
b9	PDDETSTS0	D+ Pin 0.6 V Input Detection Status*2	0: Not detected 1: Detected.	R
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Valid when IDMSINKE0 = 1.
Note 2. Valid when IDPSINKE0 = 1.

RPDME0 bit (D- Pin Pull-Down Control)

When using the battery charging function, set this bit to 1 to control the pull-down resistor of the D- pin.

IDPSRCE0 bit (D+ Pin IDPSRC Output Control)

When the IDPSRCE0 bit is set to 1, the current output is enabled on detection of the data pin connection and D+ pin pull-up.

IDMSINKE0 bit (D- Pin 0.6 V Input Detection (Comparator and Sink) Control)

When the IDMSINKE0 bit is set to 1, the USBFS detects whether VDMSRC (0.6 V), output from the host to D- on primary detection, is connected, or VDPSRC (0.6 V), output from the device to D+, is connected to D- by the host of the device.

VDPSRCE0 bit (D+ Pin VDPSRC (0.6 V) Output Control)

When the VDPSRCE0 bit set to 1, output is enabled on primary detection and VDPSRC (0.6 V) is applied to D+.

IDPSINKE0 bit (D+ Pin 0.6 V Input Detection (Comparator and Sink) Control)

When the IDPSINKE0 bit is set to 1, the USBFS detects whether VDMSRC (0.6 V), output from the device to D- is connected to D+ (DCP) by the host of the device.

VDMSRCE0 bit (D- Pin VDMSRC (0.6 V) Output Control)

When the VDMSRCE0 bit set to 1, output is enabled on secondary detection and VDMSRC (0.6 V) is applied to D-.

CHGDETSTS0 flag (D- Pin 0.6 V Input Detection Status*1)

The CHGDETSTS0 flag is set to 1 if the USBFS detects whether VDMSRC (0.6 V), output from the host to D- during primary detection, is connected, or VDPSRC (0.6 V), output from the device to D+, is connected to D- by the host of the device.

PDDETSTS0 flag (D+ Pin 0.6 V Input Detection Status*2)

The PDDETSTS0 flag is set to 1 if the USBFS detects whether VDMSRC (0.6 V) that is output from the device to D- during secondary detection is connected to D+ (DCP) by the host of the device.

26.2.32 USB Clock Selection Register (UCKSEL)

Address(es): USBFS.UCKSEL 4009 00C4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UCKSELC
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	UCKSELC	USB Clock Selection*1	0: High-speed on-chip oscillator clock (HOCO) not selected as USB clock 1: High-speed on-chip oscillator clock (HOCO) selected as USB clock.	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. When UCKSELC = 1, the user trimming function cannot be used. For information on the user trimming function, see section 8, Clock Generation Circuit.

26.3 Operation

26.3.1 System Control

This section describes the register settings required for initializing the USBFS module and controlling power consumption.

26.3.1.1 Setting data to USBFS-related registers

Setting the SYSCFG.USBE bit to 1 after starting the clock supply to the USB (SYSCFG.SCKE bit is 1) enables and starts USBFS operation.

26.3.1.2 Controlling USBFS data bus registers

The USBFS has pull-up resistors for the D+ and D- lines. Pull up these lines by setting the SYSCFG.DPRPU and SYSCFG.DMRPU bits.

Confirm that connection to the USB host is made, then set the SYSCFG.DPRPU bit to 1 and pull up the D+ line (during full-speed) or set SYSCFG.DMRPU bit to 1 to pull up D- line (during low-speed).

When the SYSCFG.DPRPU (during full-speed) or SYSCFG.DMRPU (during low-speed) bit is set to 0 during communication with the system, the USBFS disables the pull-up resistor of the USB data line, thereby notifying the USBFS host of the disconnection.

Table 26.11 Control settings for the USBFS data bus resistors

SYSCFG register settings				
DPRPU bit	**DMRPU bit**	**D-**	**D+**	**Function**
0	0	Open	Open	Not in use
1	0	Open	Pull-up	Full-speed

Table 26.11 Control settings for the USBFS data bus resistors

SYSCFG register settings				
DPRPU bit	**DMRPU bit**	**D-**	**D+**	**Function**
0	1	Pull-up	Open	Low-speed
Other settings		—	—	Setting prohibited

26.3.1.3 Example of USBFS Power Supply Connection

Figure 26.2 shows an example of power supply connection when the USB regulator is not used. Figure 26.3 and Figure 26.4 show examples of power supply connection when the USB regulator is used.

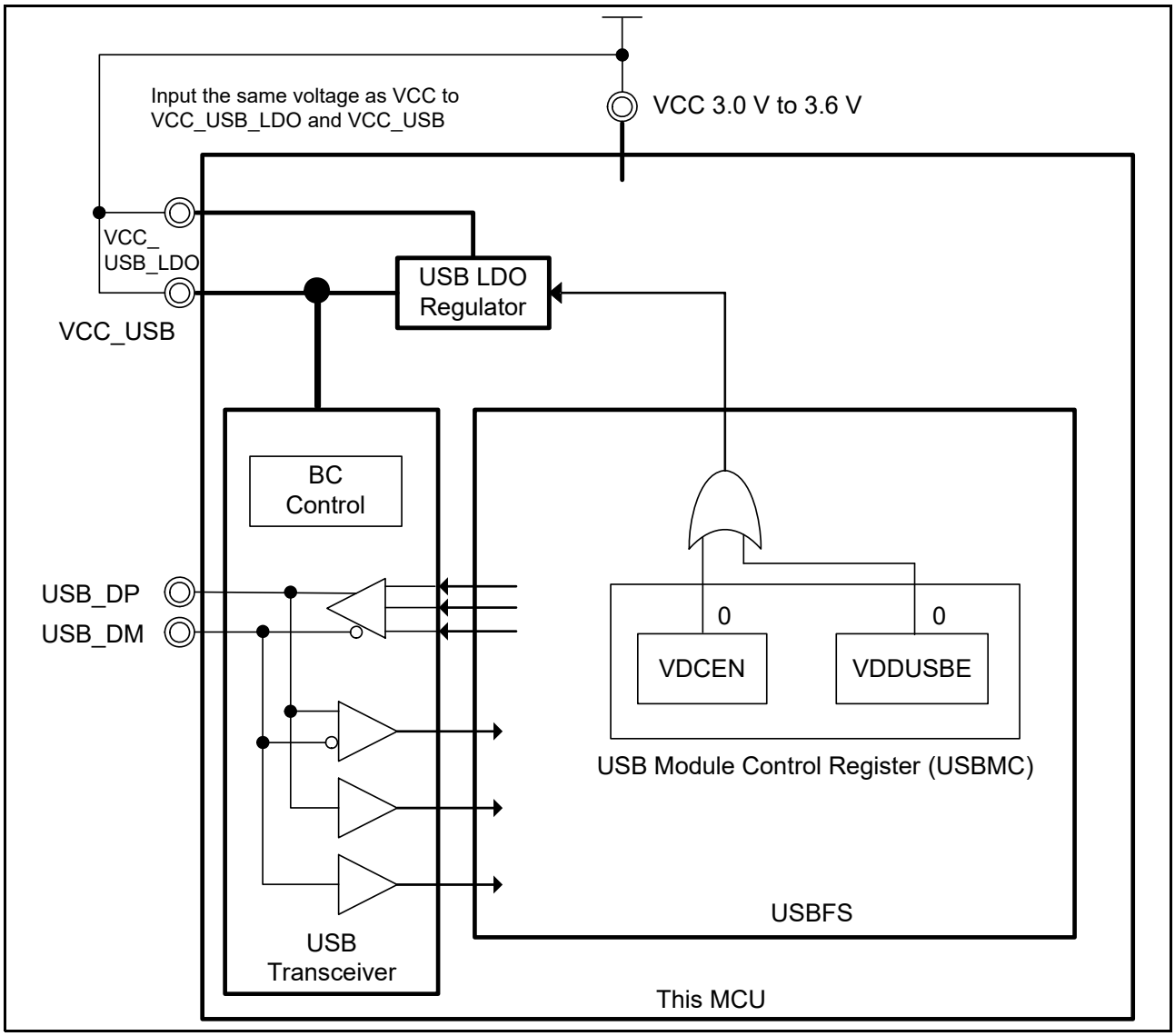
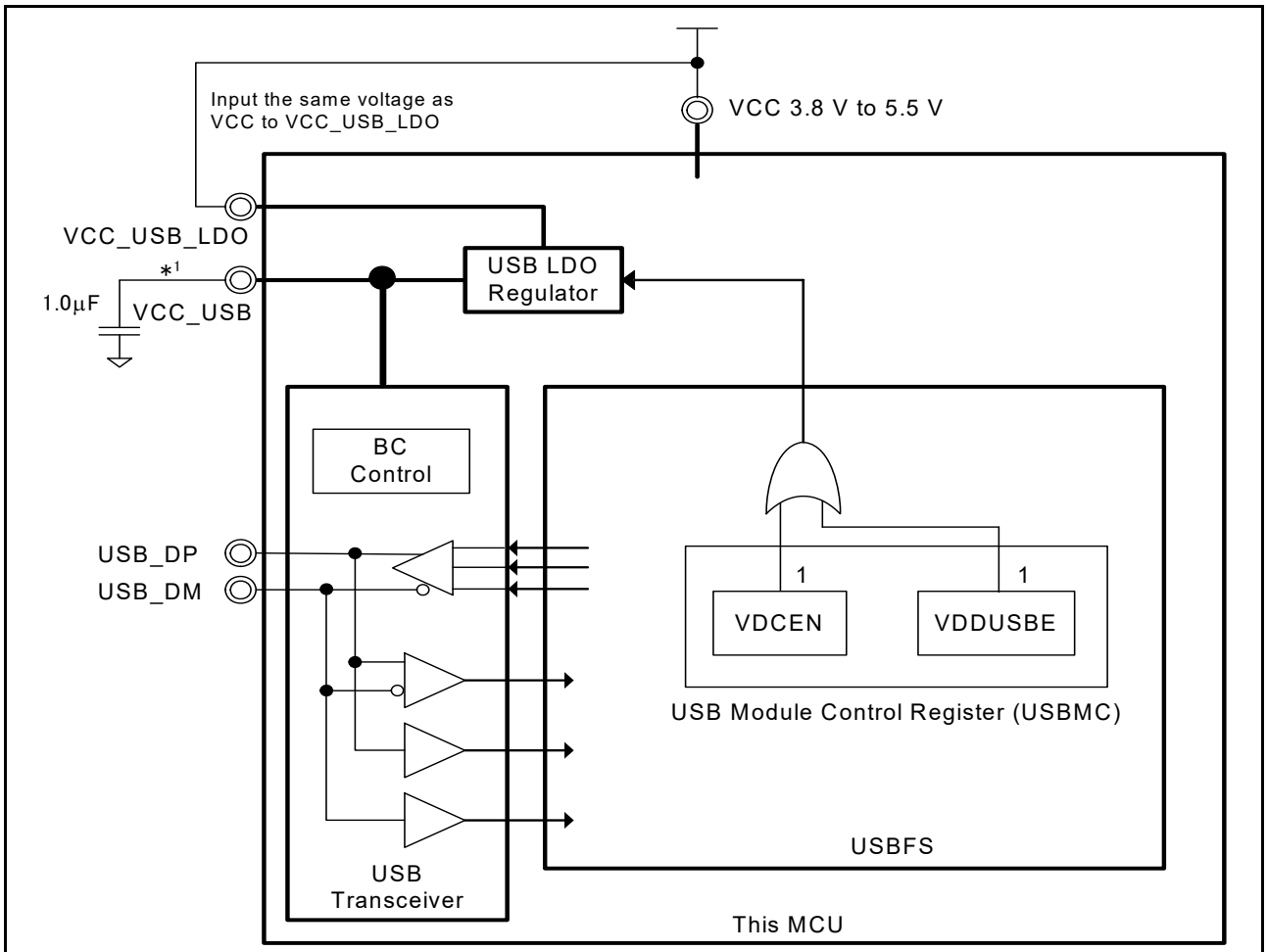
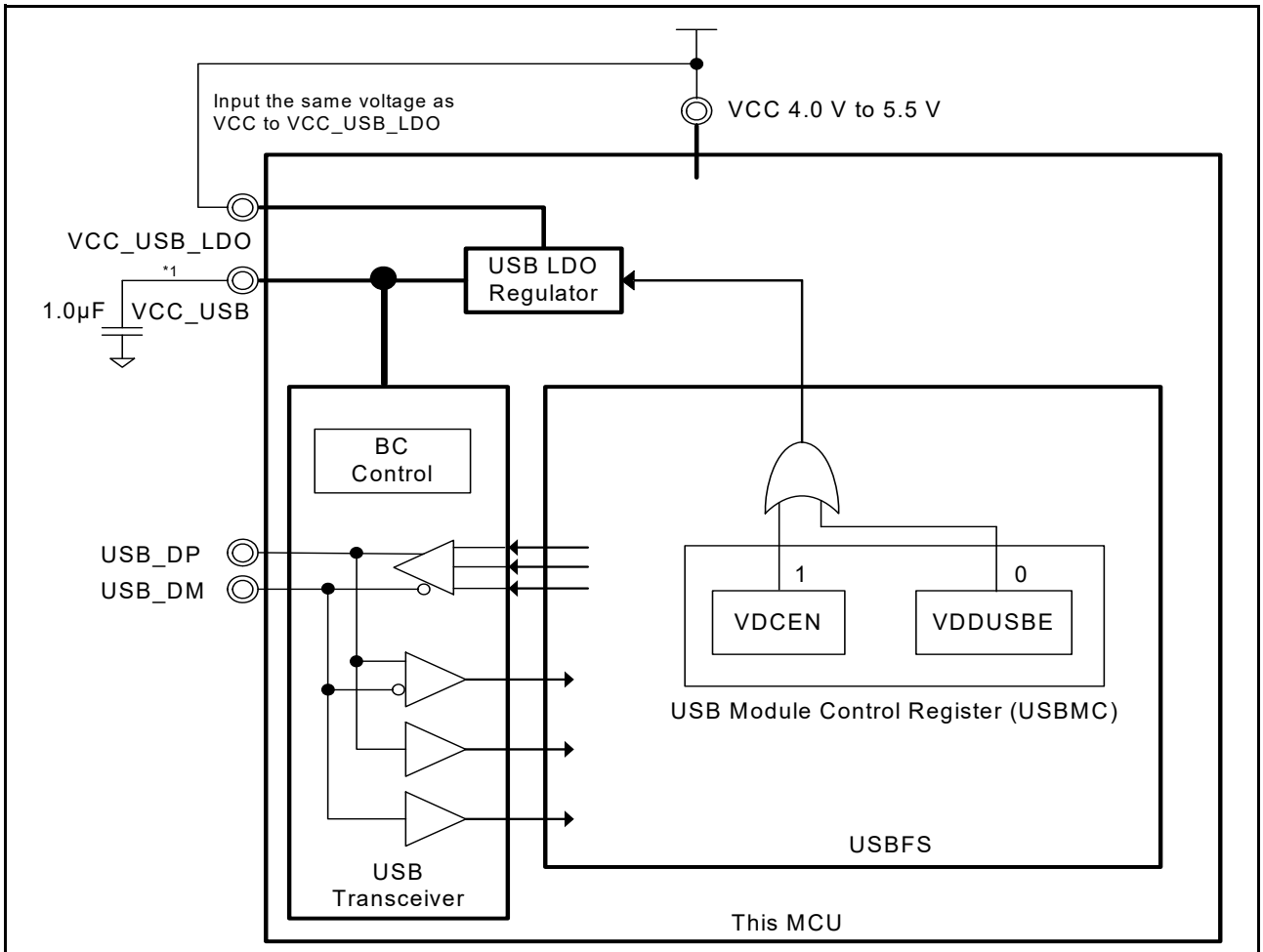


Figure 26.2 Example of power supply connection when the USB LDO regulator is not used



Note 1. Make sure that the resistance of the connected wiring is 0.5 Ω or less to connect a capacitor of ESR ≤ 1 Ω.

Figure 26.3 Example of power supply connection when the USB LDO regulator is used (BC used)



Note 1. Make sure that the resistance of the connected wiring is 0.5 Ω or less to connect a capacitor of ESR ≤ 1 Ω.

Figure 26.4 Example of power supply connection when the USB LDO regulator is used (BC not used)

26.3.1.4 Example of USB external connection circuit

The host recognizes a USB device when one of the data lines is pulled up. The MCU can use switching of the internal pull-up resistor for this. Also, bus-powered devices do not require external regulators because the MCU incorporates a power supply in the USB-PHY. Figure 26.6 and Figure 26.8 show examples of external circuits for USB connection.

Figure 26.5 shows an example of functional connection of the USB connector in the self-powered state.

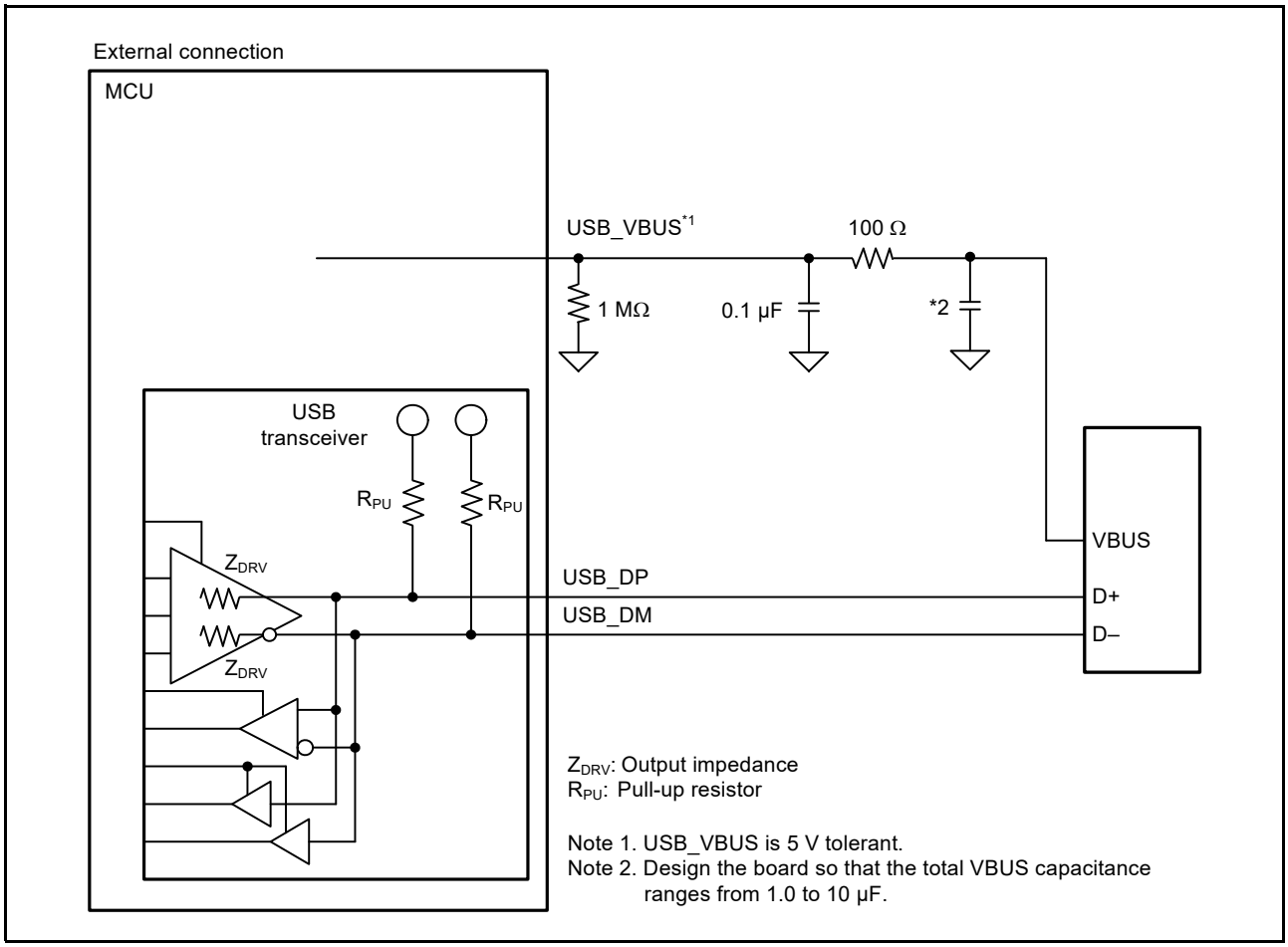


Figure 26.5 Example device connection in self-powered state

Figure 26.6 shows an example of functional connection of the USB connector in bus-powered state.

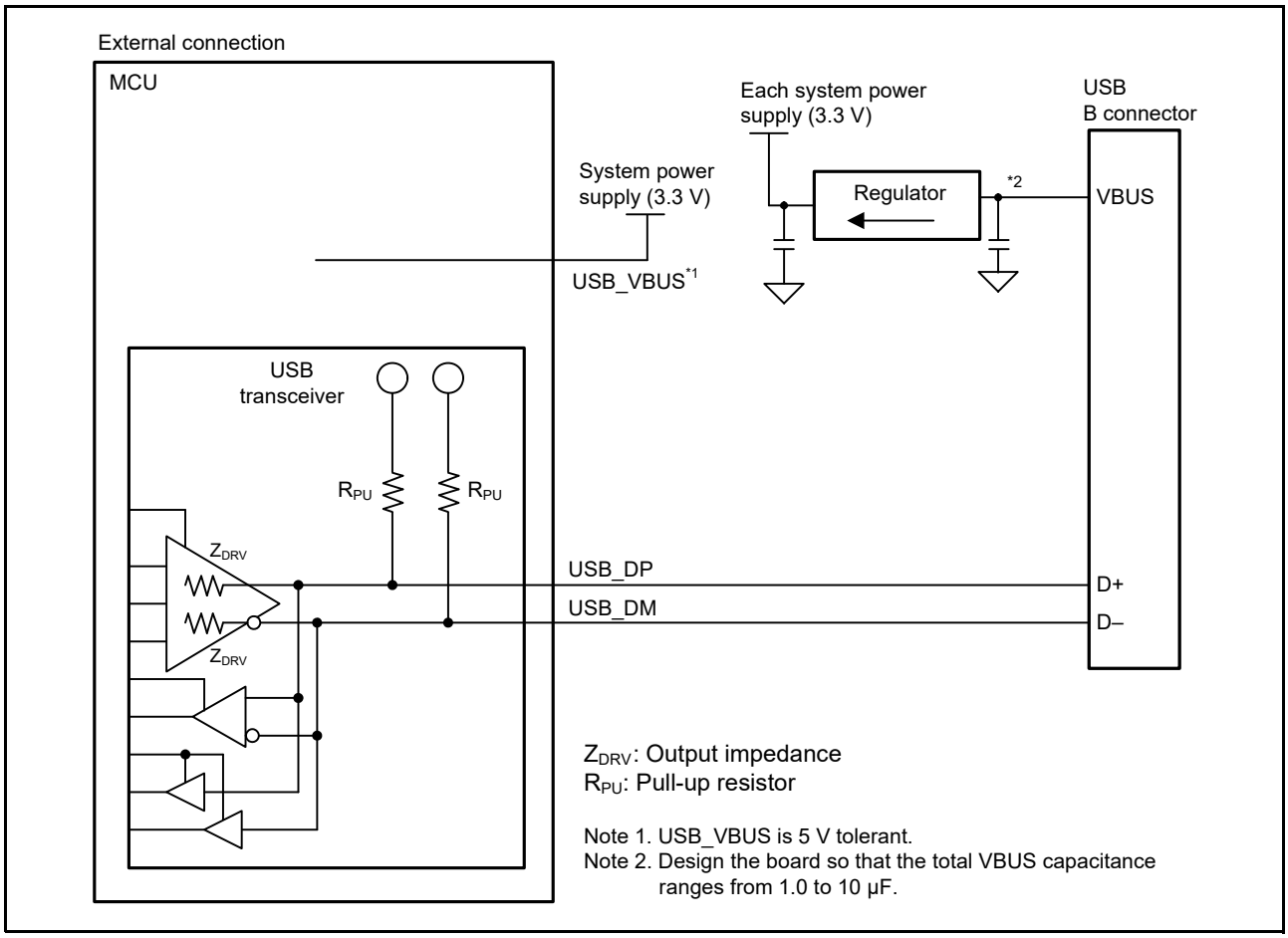


Figure 26.6 Example device connection in bus-powered state 1

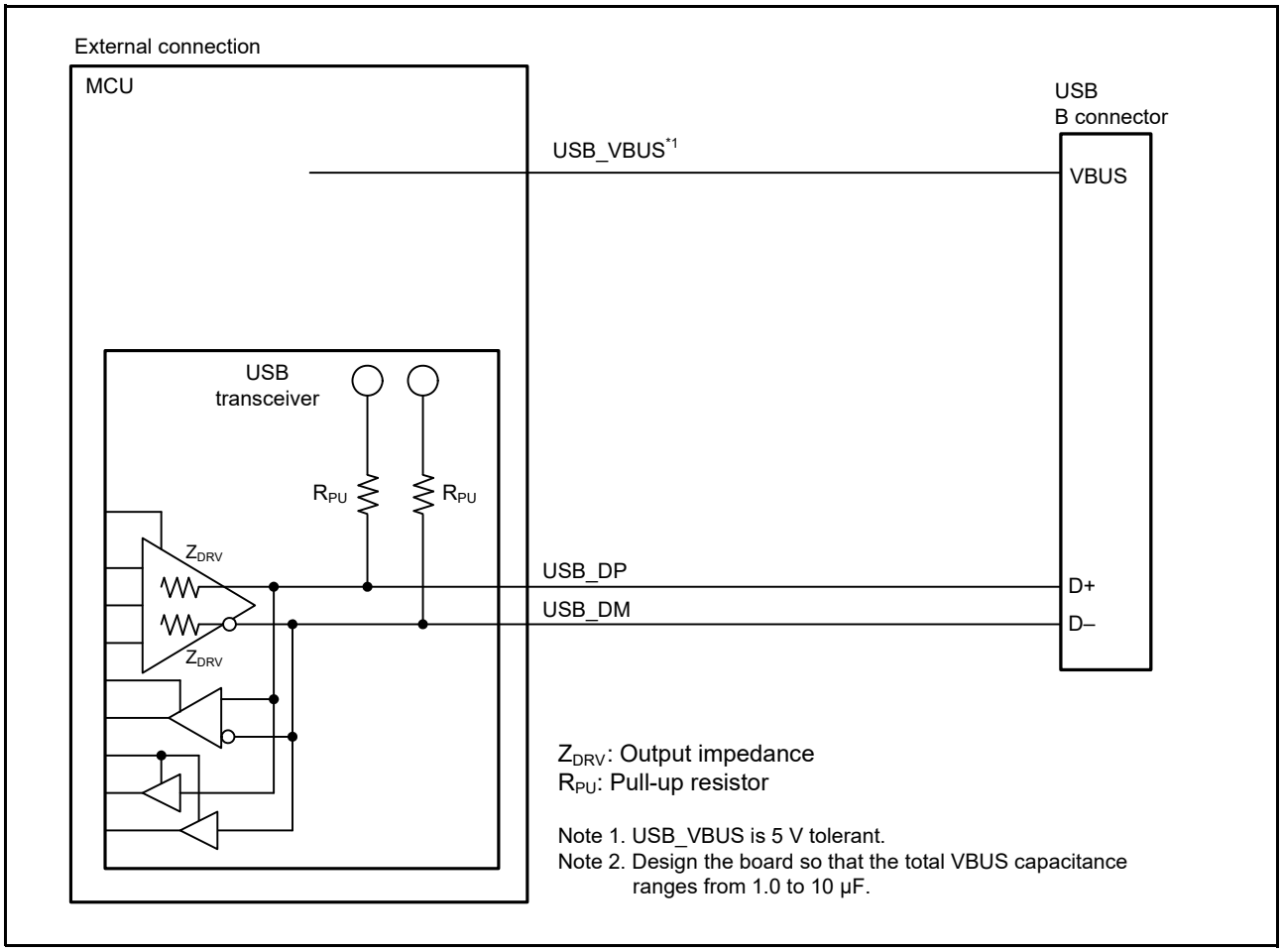


Figure 26.7 Example device connection in bus-powered state 2

The examples of external circuits given in this section are simplified circuits, and their operation in every system is not guaranteed.

Figure 26.8 shows an example of functional connection of the USB connector with Battery Charging Rev 1.2 supported.

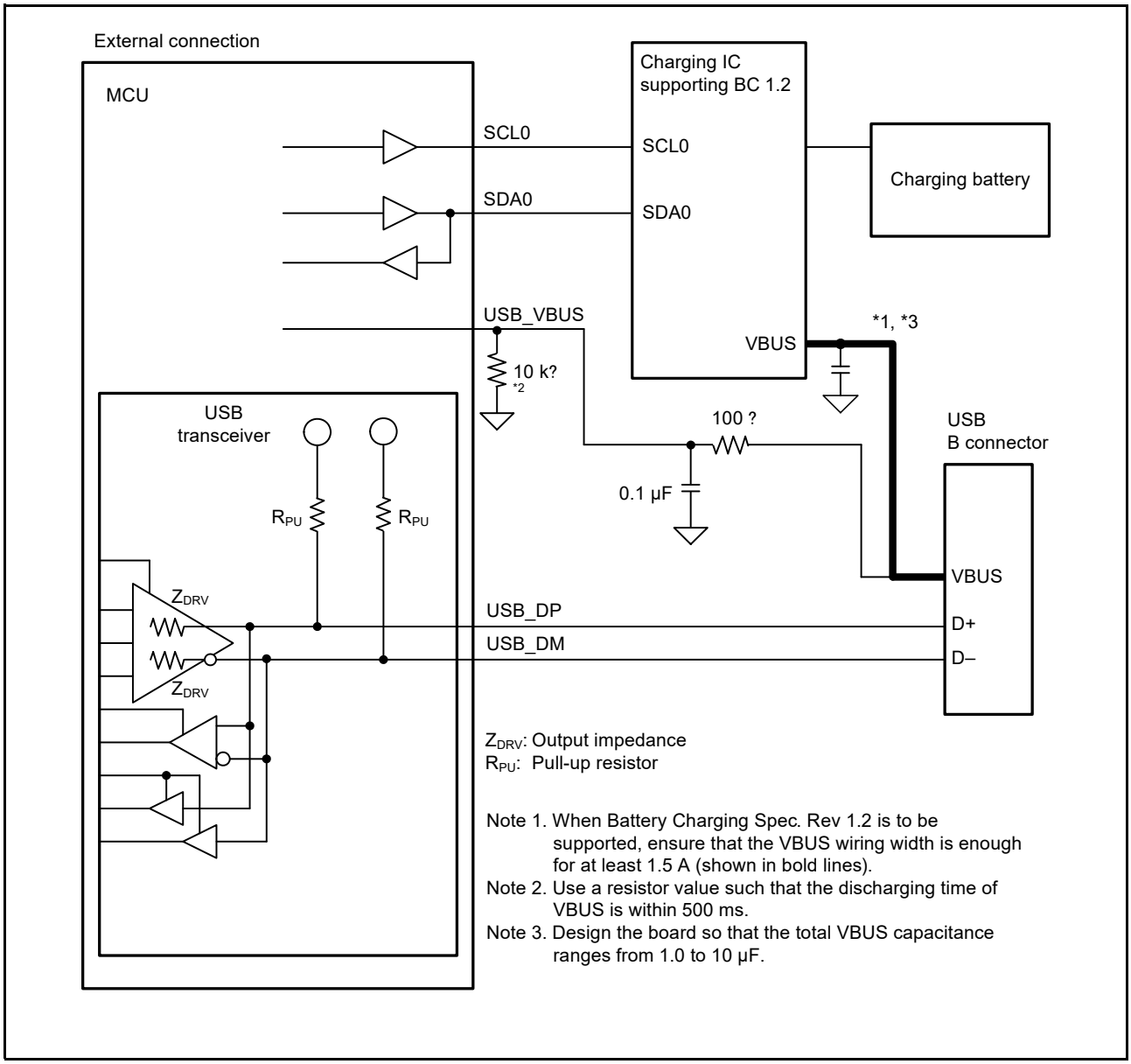


Figure 26.8 Functional connection sample of USB connector with Battery Charging Rev 1.2 supported

26.3.2 Interrupt Sources

Table 26.12 lists the interrupt sources in the USBFS.

When an interrupt generation condition is satisfied and the interrupt output is enabled using the associated interrupt enable register, a USB interrupt request is issued to the Interrupt Controller Unit and a USB interrupt is generated. See section 12, Interrupt Controller Unit (ICU).

Table 26.12 Interrupt sources

Bit to be set	Name	Interrupt source	Status flag
VBINT	VBUS interrupt	• When a change in the state of the USB_VBUS input pin is detected (low to high or high to low).	INTSTS0.VBSTS
RESM	Resume interrupt	• When a change in the state of the USB bus is detected in the suspended state (J-state to K-state or J-state to SE0).	—
SOFR	Frame number update interrupt	• When an SOF packet with a different frame number is received.	—

Table 26.12 Interrupt sources

Bit to be set	Name	Interrupt source	Status flag
DVST	Device state transition interrupt	• When a device state transition is detected with any of the following conditions: - A USB bus reset detected - Suspended state detected - SET_ADDRESS request received - SET_CONFIGURATION request received.	INTSTS0.DVSQ[2:0]
CTRT	Control transfer stage transition interrupt	• When a stage transition is detected in control transfer with any of the following conditions: - Setup stage completed - Control write transfer status stage transition - Control read transfer status stage transition - Control transfer completed - A control transfer sequence error occurred.	INTSTS0.CTSQ[2:0]
BEMP	Buffer empty interrupt	• When transmission of all data in the buffer memory is complete and the buffer becomes empty • When a packet larger than the maximum packet size is received.	BEMPSTS.PIPEnBEMP
NRDY	Buffer not ready interrupt	• When NAK is returned for an IN or OUT token while the PID bit = BUF.	NRDYSTS.PIPEnNRDY
BRDY	Buffer ready interrupt	• When the buffer becomes ready (reading or writing is enabled).	BRDYSTS.PIPEnBRDY

Figure 26.9 shows the circuits related to the interrupts in the USBFS.

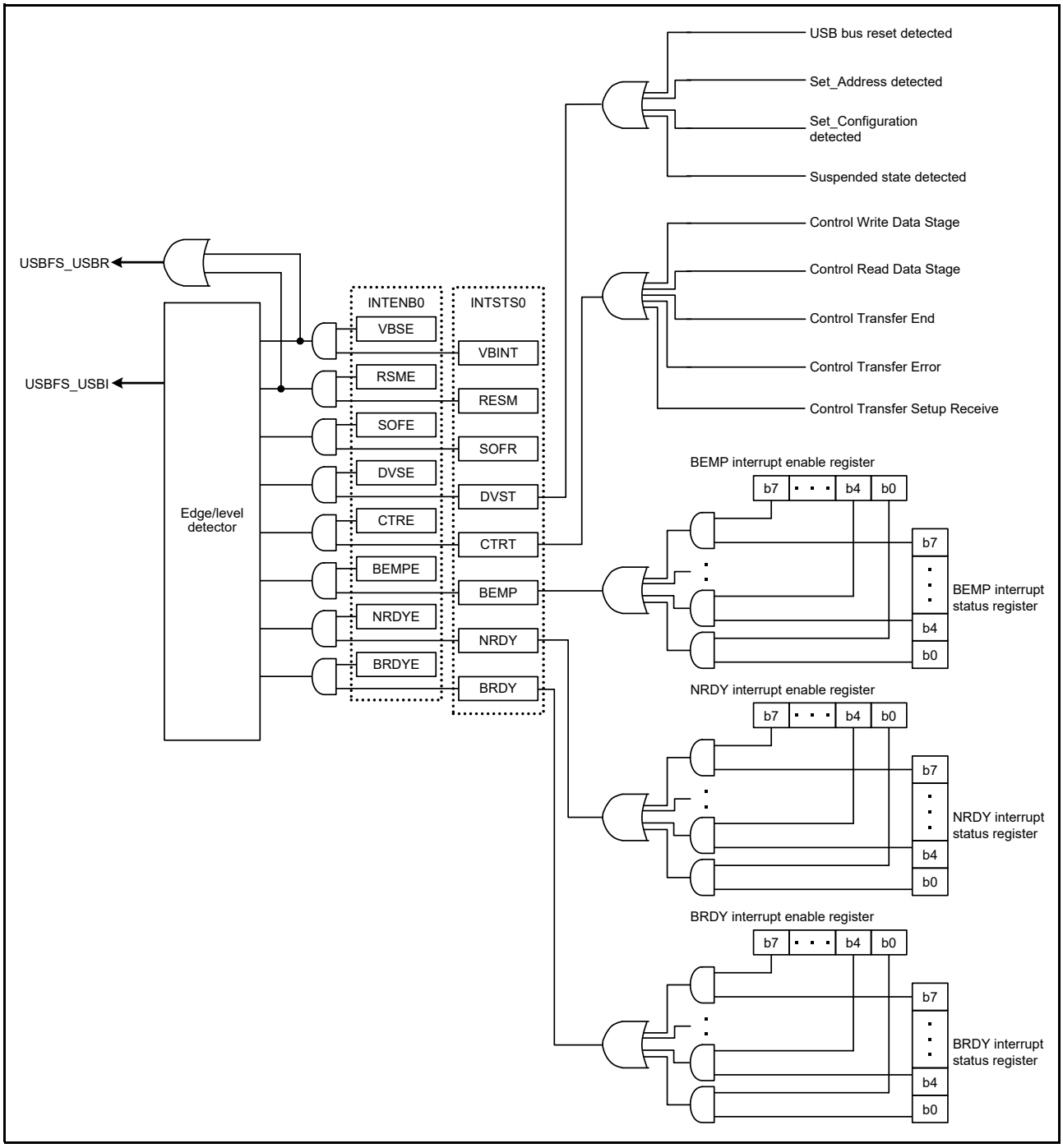


Figure 26.9 Circuits related to interrupts in USBFS

Table 26.13 shows the interrupts generated in the USBFS.

Table 26.13 USBFS Interrupts

Interrupt name	Interrupt status flag	DTC activation
USBFS_USBI	VBUS interrupt, resume interrupt, frame number update interrupt, device state transition interrupt, control transfer stage transition interrupt, buffer empty interrupt, buffer not ready interrupt, buffer ready interrupt.	Not possible
USBFS_USBR	VBUS interrupt, resume interrupt.	Not possible

26.3.3 Interrupt Descriptions

26.3.3.1 BRDY interrupt

The following sections describe the conditions in which the USBFS sets 1 to a corresponding bit in BRDYSTS. For this condition, the USBFS generates a BRDY interrupt if software sets 1 to the BRDYENB.PIPEnBRDYE bit that corresponds to the pipe and 1 to the INTENB0.BRDYE bit.

The conditions for generating and clearing the BRDY interrupt depend on the settings of the SOFCFG.BRDYM bit and PIPECFG.BFRE bit for each pipe as described in the following sections:

(1) When the SOFCFG.BRDYM bit = 0 and the PIPECFG.BFRE bit = 0

With these settings, the BRDY interrupt indicates that the FIFO port is accessible.

On any of the following conditions, the USBF generates an internal BRDY interrupt request trigger and sets 1 to the BRDYSTS.PIPEnBRDY bit associated with the selected pipe.

(a) For the transmitting pipe:

- When the DIR bit is changed from 0 to 1 by software
- When packet transmission is complete using the selected pipe while write-access from the CPU to the FIFO buffer for the selected pipe is disabled (when the BSTS bit is read as 0)
- When one FIFO buffer is empty on completion of writing data to the other FIFO buffer in double buffer mode
- No request trigger is generated until completion of writing data to the currently-written FIFO buffer even if transmission to the other FIFO buffer is complete
- When 1 is written to the PIPEnCTR.ACLRM bit, that causes the FIFO buffer to transition from the write-disabled to write-enabled state.

  No request trigger is generated for the DCP during data transmission for control transfers.

(b) For the receiving pipe:

- When packet reception completes successfully therefore, enabling the FIFO buffer to be read while read-access from the CPU to the FIFO buffer for the selected pipe is disabled (when the BSTS bit is read as 0).
  No request trigger is generated for the transaction in which DATA-PID mismatch occurred.
- When one FIFO buffer is read-enabled on completion of reading data from the other FIFO buffer in double buffer mode.
  No request trigger is generated until completion of reading data from the currently-read FIFO buffer even when reception by the other FIFO buffer completes.

The BRDY interrupt is not generated in the status stage of control transfers.

The PIPEnBRDY interrupt status of the selected pipe can be set to 0 by writing 0 to the corresponding PIPEnBRDY bit through software. In this case, write 1 to the PIPEnBRDY bits for the other pipes.

Clear the BRDY status before accessing the FIFO buffer.

(2) When the SOFCFG.BRDYM bit = 0 and the PIPECFG.BFRE bit = 1

With these settings, the USB generates a BRDY interrupt on completion of reading all data for a single transfer using the pipe in the receiving direction, and sets 1 to the bit in BRDYSTS associated with the selected pipe.

On any of the following conditions, the USBFS determines that the last data for a single transfer is received.

- When a short packet including a zero-length packet is received
- When the PIPEn transaction counter register (PIPEnTRN) is used and the number of packets specified by the PIPEnTRN.TRNCNT[15:0] bits are completely received.

When the pertinent data is completely read after any of the specified conditions is satisfied, the USBFS determines that all data for a single transfer is completely read.

When a zero-length packet is received while the FIFO buffer is empty, the USBFS determines that all data for a single

transfer is completely read when the FRDY bit in the FIFO port control register is 1 and the DTLN[8:0] bits are 0. In this case, to start the next transfer, write 1 to the BCLR bit in the associated port control register through software. With these settings, the USBFS does not detect a BRDY interrupt for the transmitting pipe.

The PIPEnBRDY interrupt status of the selected pipe can be set to 0 by writing 0 to the corresponding BRDYSTS.PIPEnBRDY bit through software. In this case, write 1 to the PIPEnBRDY bits for the other pipes.

In this mode, do not modify the PIPECFG.BFRE bit setting until all data for a single transfer is processed. When modification to the PIPECFG.BFRE bit is required before processing completes, clear all FIFO buffers for the selected pipe with the PIPEnCTR.ACLRM bit.

(3) When the SOFCFG.BRDYM bit = 1 and the PIPECFG.BFRE bit = 0

With these settings, the BRDYSTS.PIPEnBRDY values are linked to the BSTS bit setting for each pipe, that is, the BRDY interrupt status bits (PIPEnBRDY) are set to 1 or 0 by the USBFS depending on the FIFO buffer status.

(a) For the transmitting pipe

The BRDY interrupt status bits are set to 1 when the FIFO buffer is ready for write access, and are set to 0 when it is not ready. However, the BRDY interrupt is not generated even when the DCP in the transmitting direction is ready for write access.

(b) For the receiving pipe

The BRDY interrupt status bits are set to 1 when the FIFO buffer is ready for read access, and are set to 0 when all data are read (not ready for read access). When a zero-length packet is received while the FIFO buffer is empty, the selected bit is set to 1 and the BRDY interrupt is continuously generated until BCLR = 1 is written by software.

With this setting, the PIPEnBRDY bit cannot be set to 0 by software. When the SOFCFG.BRDYM bit is set to 1, set all PIPECFG.BFRE bits for all pipes to 0.

Figure 26.10 shows the timing of BRDY interrupt generation.

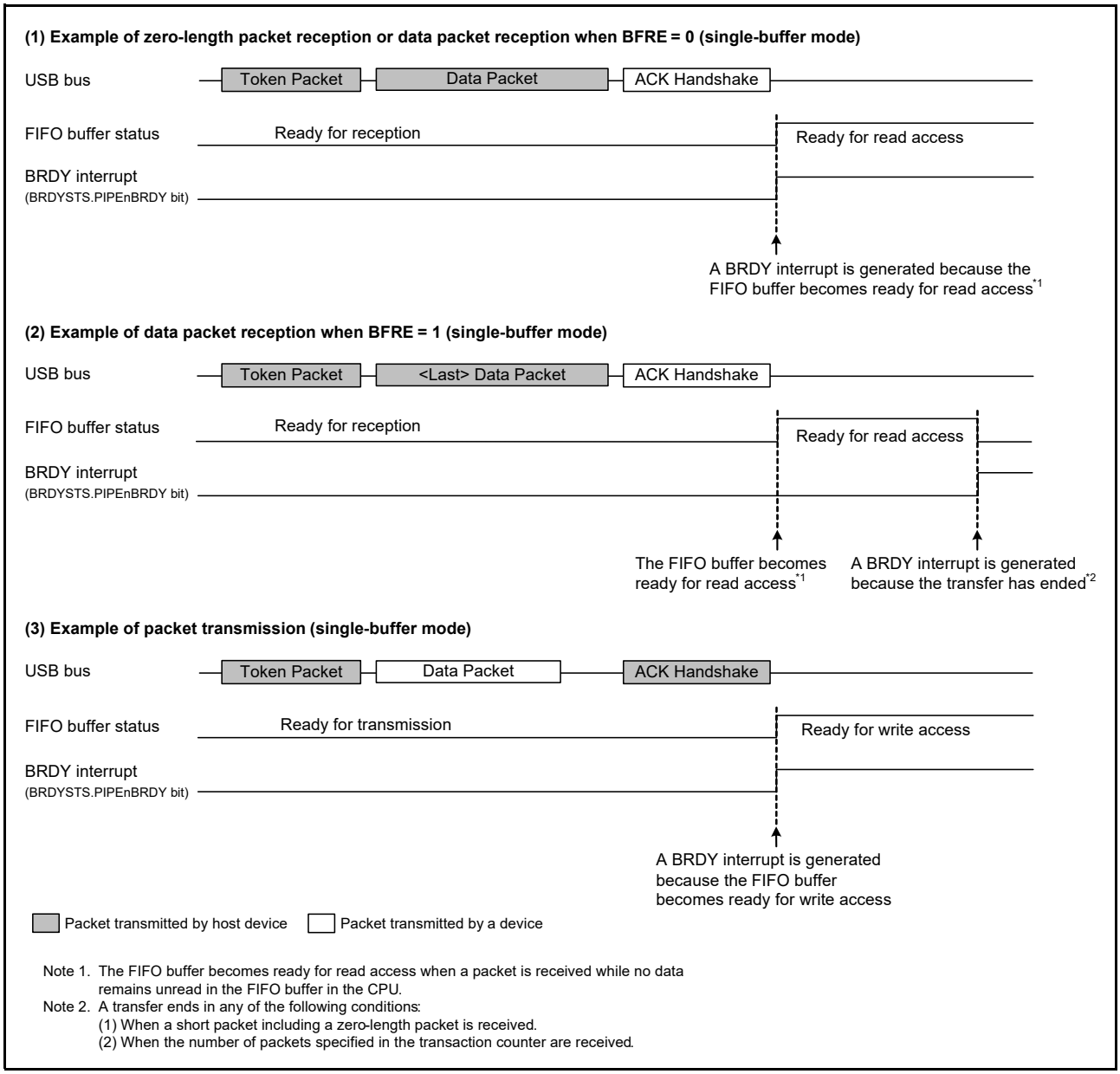


Figure 26.10 Timing of BRDY interrupt generation

The condition for which the USBFS clears the INTSTS0.BRDY bit depends on the SOFCFG.BRDYM bit setting. Table 26.14 shows the condition for clearing the BRDY bit.

Table 26.14 Condition for clearing BRDY bit

BRDYM bit	Condition for clearing BRDY bit
0	When all bits in BRDYSTS are set to 0 by software
1	When the BSTS bits for all pipes become 0

26.3.3.2 NRDY interrupt

On generating an internal NRDY interrupt request for the pipe whose PID bits are set to BUF by software, the USBFS sets the associated PIPEnNRDY bit in NRDYSTS to 1. If the associated bit in NRDYENB is set to 1 by software, the USBFS sets the INTSTS0.NRDY bit to 1 and generates a USB interrupt.

This section describes the conditions in which the USBFS generates the internal NRDY interrupt request for a given pipe.

The internal NRDY interrupt request is not generated during status stage execution of the control transfer.

(a) For the transmitting pipe

When an IN token is received while there is no data to be transmitted in the FIFO buffer, the USBFS generates a NRDY interrupt request on reception of the IN token and sets the NRDYSTS.PIPEnNRDY bit to 1.

(b) For the receiving pipe

When an OUT token is received while there is no space available in the FIFO buffer.

For transfer pipes in which an interrupt is generated, the USBFS generates an NRDY interrupt request when an NAK handshake is transferred after the data following the OUT token is received, and sets the PIPEnNRDY bit to 1.

However, during retransmission (due to DATA-PID mismatch), the NRDY interrupt request is not generated. In addition, if an error occurs in the DATA packet, the NRDY interrupt request is not generated.

Figure 26.11 shows the timing of NRDY interrupt generation.

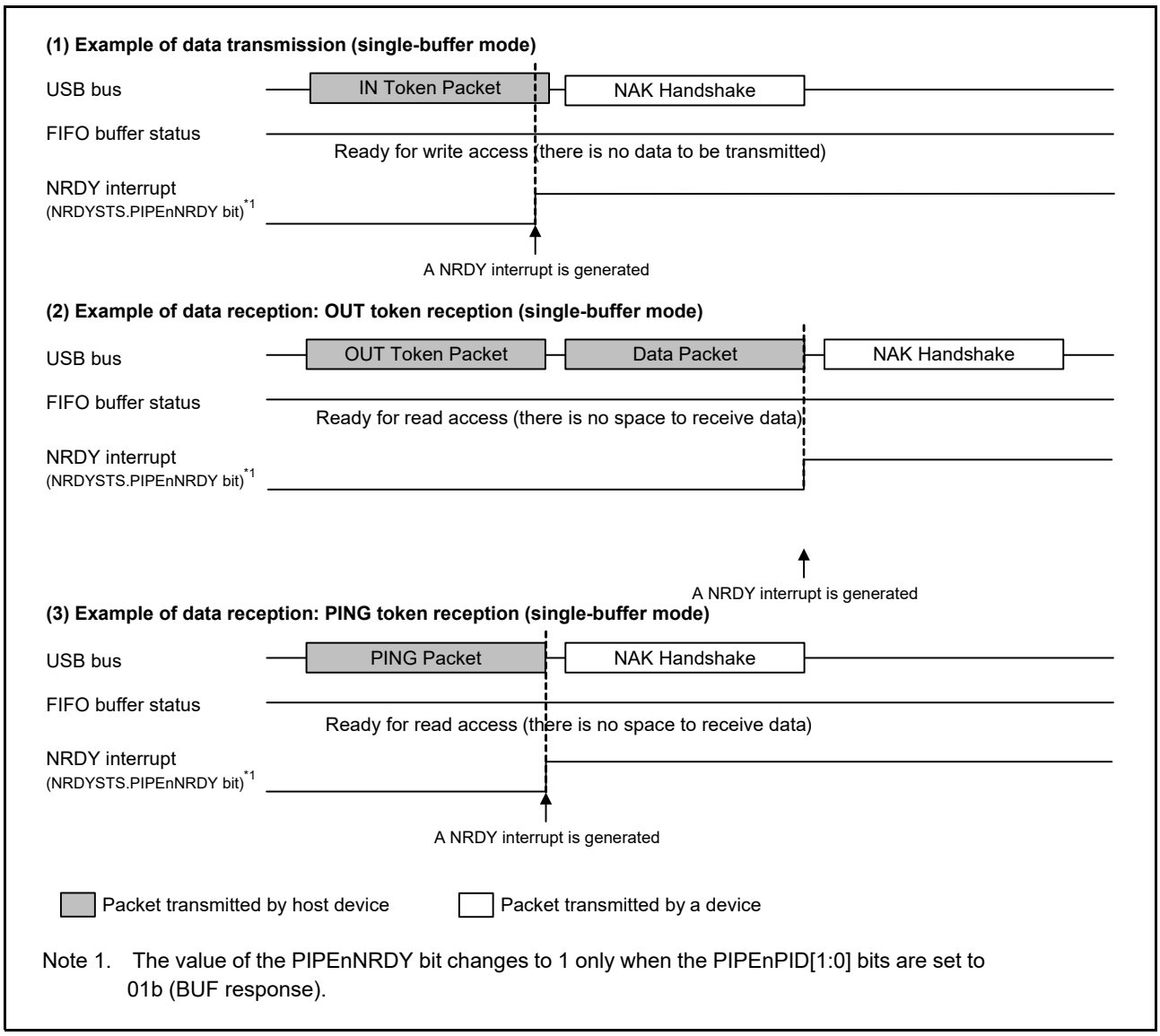


Figure 26.11 Timing of NRDY interrupt generation

26.3.3.3 BEMP interrupt

On detecting a BEMP interrupt for the pipe whose PID bits are set to BUF by software, the USBFS sets the associated BEMPSTS.PIPEnBEMP bit to 1. If the associated bit in BEMPENB is set to 1 by software, the USBFS sets the

INTSTS0.BEMP bit to 1 and generates a USB interrupt.

The following sections describe the conditions in which the USBFS generates an internal BEMP interrupt request.

(1) For the transmitting pipe

When the FIFO buffer of the associated pipe is empty on completion of transmission (including zero-length packet transmission).

In single buffer mode, an internal BEMP interrupt request is generated simultaneously with the BRDY interrupt for the pipe other than DCP.

The internal BEMP interrupt request is not generated on any of the following conditions:

- When the CPU writes data to the FIFO buffer of the CPU on completion of transmitting data from one FIFO buffer in double buffer mode
- When the buffer is cleared by setting the PIPEnCTR.ACLRM or the BCLR bit in the port control register to 1
- When IN transfer (zero-length packet transmission) is performed during the control transfer status stage.

(2) For the receiving pipe

When a successfully-received data packet size exceeds the specified maximum packet size. In this case, the USBFS generates a BEMP interrupt request, sets the associated BEMPSTS.PIPEnBEMP bit to 1, discards the received data, and changes the associated PID[1:0] setting for the pipe to STALL (11b). The USBFS returns STALL response.

The internal BEMP interrupt request is not generated on any of the following conditions:

- When a CRC error or a bit stuffing error is detected in the received data
- When a setup transaction is performed:
  - Writing 0 to the BEMPSTS.PIPEnBEMP bit clears the status
  - Writing 1 to the BEMPSTS.PIPEnBEMP bit has no effect.

Figure 26.12 shows the timing of BEMP interrupt generation.

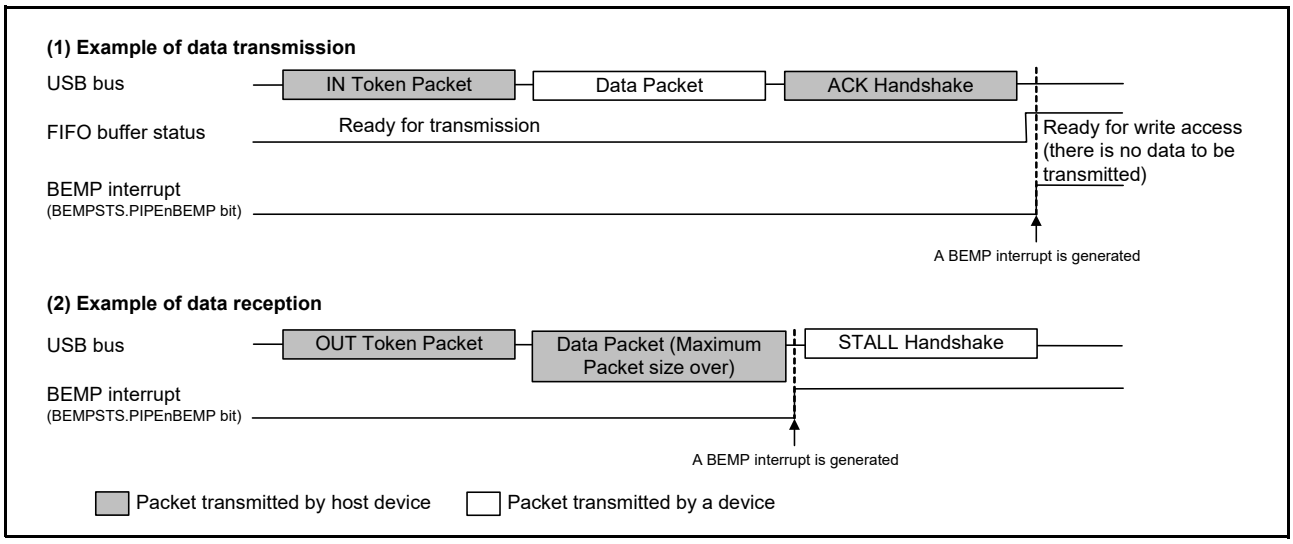


Figure 26.12 Timing of BEMP interrupt generation

26.3.3.4 Device state transition interrupt

Figure 26.13 is a diagram of device state transitions in the USB. The USBFS controls device state and generates device state transition interrupts. However, recovery from the suspended state (resumed signal detection) is detected by means of the resumed interrupt. The device state transition interrupts can be enabled or disabled individually using INTENB0. The device state to which a transition is made can be confirmed using the INTSTS0.DVSQ[2:0] bits.

When a transition is made to the default state, a device state transition interrupt is generated after a USB bus reset is

detected.

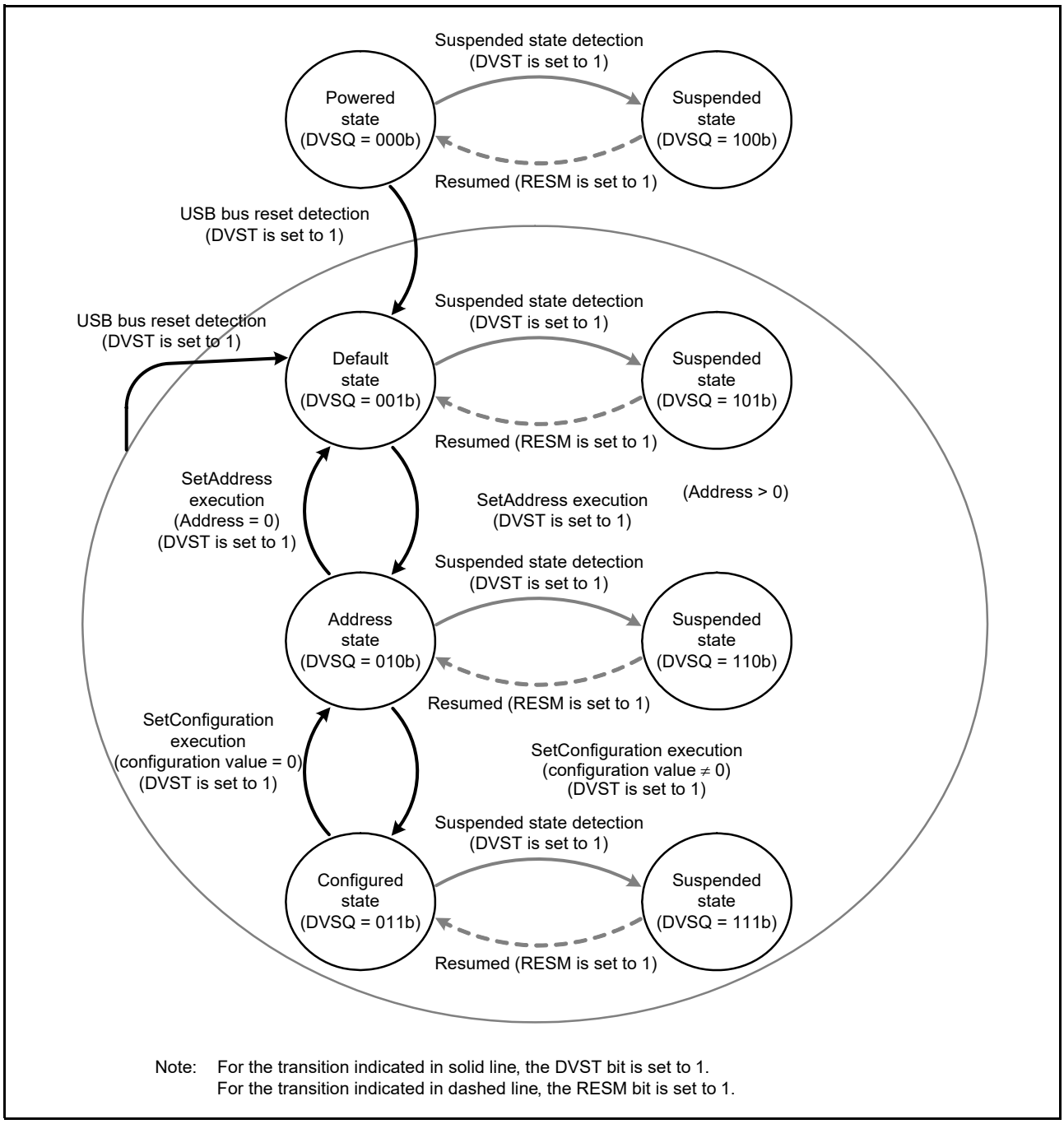


Figure 26.13 Device state transitions

26.3.3.5 Control transfer stage transition interrupt

Figure 26.14 is a diagram of control transfer stage transitions in the USB. The USB controls the control transfer sequence and generates control transfer stage transition interrupts. The control transfer stage transition interrupts can be enabled or disabled individually using INTENB0. The transfer stage to which a transition is made can be confirmed using the INTSTS0.CTSQ[2:0] bits. Control transfer stage transition interrupts are generated.

This section describes control transfer sequence errors. When an error occurs, the DCPCTR.PID[1:0] bits are set to 1xb (STALL response).

(1) Control read transfer errors

- An OUT token is received but no data is transferred in response to the IN token at the data stage
- An IN token is received at the status stage
- A data packet with DATAPID = DATA0 is received at the status stage.

(2) Control write transfer errors

- An IN token is received but no ACK is returned in response to the OUT token at the data stage
- A data packet with DATAPID = DATA0 is received as the first data packet at the data stage
- An OUT token is received at the status stage.

(3) No data control transfers

- An OUT token is received at the status stage.

At the control write transfer data stage, if the received data length exceeds the wLength value of the USB request, it cannot be recognized as a control transfer sequence error. At the control read transfer status stage, packets other than zero-length packets are received by an ACK response and the transfer ends normally.

When a CTRT interrupt occurs in response to a sequence error (INTSTS0.CTRT = 1), the CTSQ[2:0] = 110b value is saved until the CTRT bit = 0 is written from the system (the interrupt status is cleared). While CTSQ[2:0] = 110b is being held, the CTRT interrupt that ends the setup stage is not generated even when a new USB request is received. The USBFS saves the setup stage completion status, and generates a CTRT interrupt after software clears the interrupt status.

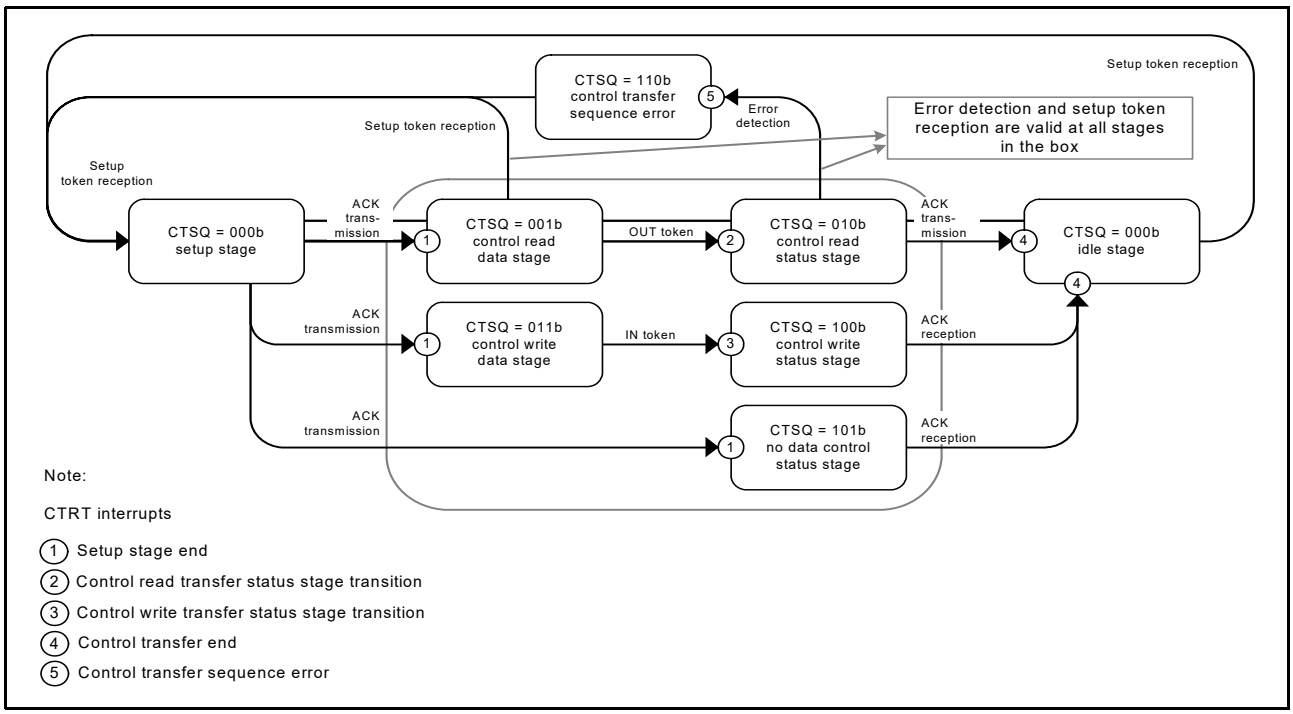


Figure 26.14 Control transfer stage transitions

26.3.3.6 Frame update interrupt

The USBFS updates the frame number and generates an SOFR interrupt if it detects a new SOF packet during full-speed operation.

26.3.3.7 VBUS interrupt

When the USB_VBUS pin level changes, a VBUS interrupt is generated. The level of the USB_VBUS pin can be checked with the INTSTS0.VBSTS bit. Whether the host controller is connected or disconnected can be confirmed using the VBUS interrupt. If the system is activated with the host controller connected, the first VBUS interrupt is not

generated because there is no change in the USB_VBUS pin level.

26.3.3.8 Resumed interrupt

A resumed interrupt is generated when the device state is the suspended state and the USB bus state has changed from J-state to K-state, or from J-state to SE0. Recovery from the suspended state is detected by means of the resumed interrupt.

26.3.4 Pipe Control

Table 26.15 lists the pipe settings for the USBFS. USBFS data transfer is performed through pipes that software has associated with the endpoint. The USBFS has 5 pipes for data transfer.

Set each pipe appropriately based on your system specifications.

Table 26.15 Pipe settings

Register name	Bit name	Setting	Remarks
DCPCFG PIPECFG	TYPE	Specify the transfer type	PIPE4 to PIPE7: Can be set
	BFRE	Select the BRDY interrupt mode	PIPE4 and PIPE5: Can be set
	DBLB	Select double buffer mode	PIPE4 and PIPE5: Can be set
	DIR	Select transfer direction	IN or OUT can be set
	EPNUM	Endpoint number	PIPE4 to PIPE7: Can be set Set a value other than 0000b when the pipe is used.
	SHTNAK	Select disabled state for pipe when transfer ends	PIPE4 and PIPE5: Can be set
DCPMAXP PIPEMAXP	MXPS	Maximum packet size	Compliant with USB 2.0 Specification
DCPCTR PIPEnCTR	BSTS	Buffer status	For the DCP, receive buffer status and transmit buffer status are switched with the ISEL bit
	INBUFM	IN buffer monitor	Available only for PIPE4 and PIPE5
	ATREPM	Auto response mode	PIPE4 and PIPE5: Can be set
	ACLRM	Auto buffer clear	PIPE4 to PIPE7: Can be set
	SQCLR	Sequence clear	Clear the data toggle bit
	SQSET	Sequence set	Set the data toggle bit
	SQMON	Sequence monitor	Monitor the data toggle bit
	PBUSY	Pipe busy status	-
	PID	Response PID	See section 26.3.4.6, Response PID
PIPEnTRE	TRENB	Transaction counter enable	PIPE4 and PIPE5: Can be set
	TRCLR	Current transaction counter clear	PIPE4 and PIPE5: Can be set
PIPEnTRN	TRNCNT	Transaction counter	PIPE4 and PIPE5: Can be set

26.3.4.1 Pipe control register switching procedures

Do not modify the following bits in the pipe control registers when USB communication is enabled (PID = BUF):

- Bits in DCPCFG and DCPMAXP
- SQCLR and SQSET bits in DCPCTR
- Bits in PIPECFG and PIPEMAXP
- ATREPM, ACLRM, SQCLR, and SQSET bits in PIPEnCTR
- Bits in PIPEnTRE and PIPEnTRN.

To modify those bits when USB communication is enabled (PID = BUF), use the following procedure:

1. When a request to modify bits in the pipe control register occurs, modify the PID[1:0] bits associated with the pipe to NAK.

2. Wait until the corresponding PBUSY bit is set to 0.
3. Modify the bits in the pipe control register.

The following bits in the pipe control registers can be modified only when the selected pipe information is not set by the CURPIPE[3:0] bits in CFIFOSEL:

- Bits in DCPCFG and DCPMAXP
- Bits in PIPECFG and PIPEMAXP.

To change pipe information, set the CURPIPE[3:0] bits in the port select registers to a pipe other than the one to be modified. For DCP, clear the buffer with the BCLR bit in the Port Control Register after the pipe information is changed.

26.3.4.2 Transfer types

The PIPECFG.TYPE[1:0] bits specify the following transfer types for each pipe:

- DCP — No setting is required (fixed at control transfer)
- PIPE4 and PIPE5 — Set to bulk transfer
- PIPE6 and PIPE7 — Set to interrupt transfer.

26.3.4.3 Endpoint number

The PIPECFG.EPNUM[3:0] bits set the endpoint number for each pipe. The DCP is fixed at endpoint 0. The other pipes can be set from endpoint 1 to 15:

- DCP — No setting is required (fixed at endpoint 0)
- PIPE4 to PIPE7 — Select and set the endpoint numbers from 1 to 15 so that the combination of the PIPECFG.DIR and EPNUM[3:0] bits is unique.

26.3.4.4 Maximum packet size setting

The DCPMAXP.MXPS[6:0] and PIPEMAXP.MXPS[8:0] bits specify the maximum packet size for each pipe. DCP, PIPE4 and PIPE5 can be set to any of the maximum pipe sizes defined in the USB 2.0 Specification. For PIPE6 and PIPE7, the maximum packet size is 64 bytes. Set the maximum packet size as follows before starting a transfer (PID = BUF):

- DCP — Set to 8, 16, 32, or 64
- PIPE4 and PIPE5 — Set to 8, 16, 32, or 64 for bulk transfers
- PIPE6 and PIPE7 — Set to a value between 1 and 64.

26.3.4.5 Transaction counter for PIPE4 and PIPE5 in the receiving direction

When the specified number of transactions is complete in the data packet receiving direction, the USBFS recognizes that the transfer has ended. Two transaction counters are provided:

- The PIPEnTRN register that specifies the number of transactions to be executed
- The current counter that internally counts the number of executed transactions.

With the PIPECFG.SHTNAK bit set to 1, when the current counter value matches the specified number of transactions, the associated PIPEnCTR.PID[1:0] bits are set to NAK and the subsequent transfer is disabled. The transactions can be counted again from the beginning by initializing the current counter of the transaction counter function through the PIPEnTRE.TRCLR bit. The data read from PIPEnTRN differs depending on the PIPEnTRE.TRENB setting as follows:

- The TRENB bit = 0 — the specified transaction counter value can be read
- The TRENB bit = 1 — the current counter value that indicates the internally counted number of executed transactions can be read.

When working with the TRCLR bit, the following constraints apply:

- If the transactions are counted and PID = BUF, the current counter cannot be cleared

- If there is any data left in the buffer, the current counter cannot be cleared.

26.3.4.6 Response PID

The PID[1:0] bits in DCPCTR and PIPEnCTR set the response PID for each pipe.

The following sections describe the USBFS operation with different response PID settings.

(1) Response PID settings

The response PID specifies the response to transactions from the host:

- NAK setting — the NAK response is returned in response to the generated transaction
- BUF setting — the responses are made to transactions according to the status of the buffer memory
- STALL setting — the STALL response is returned in response to the generated transaction.

Note: For setup transactions, an ACK response is returned regardless of the PID[1:0] setting, and the USB request is stored in the register.

The USBFS can write to the PID[1:0] bits, depending on the results of the transaction as described in the following section.

(2) When the response PID is set by hardware

- NAK setting — PID = NAK is set and NAK is returned in response to the following transactions:
  - When the SETUP token is received normally (DCP only)
  - If the transaction counting ends or a short packet is received when the PIPECFG.SHTNAK bit is set to 1 for bulk transfer.
- BUF setting — there is no BUF writing by the USB
- STALL setting — PID = STALL is set and STALL is returned in response to the following transactions:
  - When a received data packet exceeds the maximum packet size
  - When a control transfer sequence error is detected (DCP only).

26.3.4.7 Data PID sequence bit

The USBFS automatically toggles the sequence bit in the data PID when data is transferred successfully in the control transfer data stage, bulk transfer, and interrupt transfer. The sequence bit of the next data PID to be transmitted can be confirmed with the SQMON bit in DCPCTR and PIPEnCTR. When data is transmitted, the sequence bit toggles on ACK handshake reception. When data is received, the sequence bit toggles on ACK handshake transmission. The SQCLR and SQSET bits in DCPCTR and PIPEnCTR registers can be used to change the data PID sequence bit.

When the control transfer is used, the USBFS automatically sets the sequence bit for stage transitions. DATA1 is returned when the setup stage ended. The sequence bit is not referenced and PID = DATA1 is returned in the status stage. Therefore, software settings are not required.

For ClearFeature requests for transmission or reception, software should set the data PID sequence bit.

26.3.4.8 Response PID = NAK function

The USBFS provides a function that disables pipe operation (PID response = NAK) when the final data packet of a transaction is received. The USBFS automatically distinguishes this based on reception of a short packet or the transaction counter. Enable this function by setting the PIPECFG.SHTNAK bit to 1.

When the double buffer mode is used for the buffer memory, this function enables reception of data packets in transfer units. If pipe operation is disabled, software should set the pipe to the enabled state again (PID response = BUF).

The response PID = NAK function can only be used for bulk transfers.

26.3.4.9 Auto response mode

For bulk transfer PIPE4 and PIPE5, when the PIPEnCTR.ATREPM bit is set to 1, a transition is made in auto response

mode. During an OUT transfer (PIPECFG.DIR bit is 0), OUT-NAK mode is entered, and during an IN transfer (DIR bit is 1), null auto response mode is entered.

26.3.4.10 OUT-NAK mode

For bulk OUT transfer pipes, NAK is returned in response to an OUT token and an NRDY interrupt is output when the PIPEnCTR.ATREPM bit is set to 1. To make a transition from normal mode to OUT-NAK mode, specify OUT-NAK mode while pipe operation is disabled (response PID = NAK) before enabling pipe operation (response PID = BUF). After pipe operation is enabled, OUT-NAK mode becomes valid. If an OUT token is received immediately before pipe operation is disabled, the token data is received and an ACK is returned to the host.

To transition from OUT-NAK mode to normal mode, cancel OUT-NAK mode while pipe operation is disabled (response PID = NAK) before enabling pipe operation (response PID = BUF). In normal mode, reception of OUT data is enabled.

26.3.4.11 Null auto response mode

For bulk IN transfer pipes, zero-length packets are continuously transmitted when the PIPEnCTR.ATREPM bit is set to 1.

To transition from normal mode to null auto response mode, specify null auto response mode while pipe operation is disabled (response PID = NAK) before enabling pipe operation (response PID = BUF). After pipe operation is enabled, null auto response mode becomes valid. Before setting null auto response mode, check that PIPEnCTR.INBUFM = 0 because the mode can only be set when the buffer is empty. If the INBUFM bit is 1, empty the buffer with the PIPEnCTR.ACLRM bit. Do not write data from the FIFO port while a transition to null auto response mode is made.

To transition from null auto response mode to normal mode, keep pipe operation disabled (response PID = NAK) for the period of zero-length packet transmission (about 10 µs) before canceling the null auto response mode. In normal mode, data can be written from the FIFO port so packet transmission to the host is enabled by enabling pipe operation (response PID = BUF).

26.3.5 FIFO Buffer Memory

The USBFS has FIFO buffer memory for data transfers and it manages the memory area used for each pipe. The FIFO buffer memory has two states depending on whether the access right is assigned to the system (CPU side) or the USB (SIE side).

(1) Buffer status

Table 26.16 and Table 26.17 show the buffer status in the USBFS. The buffer memory status can be confirmed with the BSTS bit in DCPCTR and INBUFM bit in PIPEnCTR. The transfer direction for the buffer memory can be specified in either PIPECFG.DIR bit or CFIFOSEL.ISEL bit (when DCP is selected). The INBUFM bit is valid for PIPE4 and PIPE5 in the transmitting direction.

When a transmitting pipe uses the double buffer configuration, software can read the BSTS bit to monitor the buffer memory status on the CPU side and the INBUFM bit to monitor the buffer memory status on the SIE side. When the BEMP interrupt does not show the buffer empty status because write access to the FIFO port by the CPU is slow, software can use the INBUFM bit to confirm the end of transmission.

Table 26.16 Buffer status indicated by BSTS bit

ISEL or DIR	BSTS	Buffer memory status
0 (receiving direction)	0	There is no received data or data is being received. Reading from the FIFO port is disabled.
0 (receiving direction)	1	There is received data, or a zero-length packet is received. Reading from the FIFO port is allowed. Note: When a zero-length packet is received, reading is not possible and the buffer must be cleared.
1 (transmitting direction)	0	The transmission is not complete. Writing to the FIFO port is disabled.
1 (transmitting direction)	1	The transmission is complete. CPU write is allowed.

Table 26.17 Buffer status indicated by INBUFM bit

DIR	INBUFM	Buffer memory status
0 (receiving direction)	Invalid	Invalid
1 (transmitting direction)	0	The transmission is complete. There is no waiting data to be transmitted.
1 (transmitting direction)	1	The FIFO port has written data to the buffer. There is data to be transmitted.

26.3.6 FIFO Buffer Clearing

Table 26.18 shows methods for clearing the FIFO buffer memory by the USBFS. The buffer memory can be cleared using the BCLR in the Port Control Register, or PIPEnCTR.ACLRM bit.

Single or double buffer configuration can be selected for PIPE4 and PIPE5, using the PIPECFG.DBLB bit.

Table 26.18 Buffer clearing methods

FIFO buffer clearing mode	Clearing buffer memory on CPU side	Auto buffer clear mode for discarding all received packets
Register used	CFIFOCTR	PIPEnCTR
Bit used	BCLR	ACLRM
Clearing condition	Cleared by writing 1	1: Mode valid 0: Mode invalid

(1) Auto buffer clear mode function

The USB discards all received data packets if the PIPEnCTR.ACLRM bit is set to 1. If a correct data packet is received, the ACK response is returned to the host controller. The auto buffer clear mode function can only be set in the buffer memory reading direction.

Setting the ACLRM bit to 1 and then to 0 clears the buffer memory of the selected pipe regardless of the access direction. An access cycle of at least 100 ns is required for the internal hardware sequence processing time between ACLRM = 1 and ACLRM = 0.

26.3.7 FIFO Port Functions

Table 26.19 shows the settings for the FIFO port functions of the USB. In write access, writing data until the maximum packet size is reached automatically enables transmission of the data. To enable transmission before the maximum packet size is reached, set the BVAL bit in the port control register to end writing. To send a zero-length packet, use the BCLR bit to clear the buffer and set the BVAL bit to end writing.

In reading, reception of new packets is automatically enabled when all data is read. Data cannot be read when a zero-length packet is received (the DTLN[8:0] bits = 0) therefore, use the BCLR bit to clear the buffer. The length of the received data can be confirmed with the DTLN[8:0] bits in the port control register.

Table 26.19 FIFO port function settings (1 of 2)

Register name	Bit name	Description
CFIFOSEL	RCNT	Selects DTLN[8:0] read mode
	REW	Buffer memory rewind (re-read, rewrite)
	MBW	FIFO port access bit width
	BIGEND	Selects FIFO port endian
	ISEL	FIFO port access direction (only for DCP)
	CURPIPE	Selects the current pipe

Table 26.19 FIFO port function settings (2 of 2)

Register name	Bit name	Description
CFIFOCTR	BVAL	Ends writing to the buffer memory
	BCLR	Clears the buffer memory on the CPU side
	DTLN	Checks the length of received data

(1) FIFO Port Selection

Table 26.20 shows the pipes that can be selected with the different FIFO ports. The pipe to be accessed must be selected with the CURPIPE[3:0] bits in the port select register. After a pipe is selected, software must check whether the written value can be correctly read from the CURPIPE[3:0] bits (if the previous pipe number is read, it indicates that the USBFS is modifying the pipe). Next, the software checks that the FRDY bit in the port control register is 1.

In addition, software must specify the bus width to be accessed using the MBW bit in the port select register. The buffer memory access direction conforms to the PIPECFG.DIR setting. Only for the DCP that the ISEL bit in the port select register determines the direction.

Table 26.20 FIFO port access by pipe

Pipe	Access method	Port that can be used
DCP	CPU access	CFIFO port register
PIPE4 to PIPE7	CPU access	CFIFO port register

(2) REW bit

It is possible to temporarily stop access to a pipe currently being accessed, access a different pipe, and then continue to process the first pipe again. Use the REW bit in the port select register for this processing.

If a pipe is selected in the CURPIPE[3:0] bits in the port select register with the REW bit set to 1, the pointer used for reading from and writing to the buffer memory is reset. Reading or writing can be carried out from the first byte. If a pipe is selected with 0 set for the REW bit, data can be read and written in continuation from the previous selection, without the pointer being reset. To access the FIFO port, software must check that the FRDY bit in the port control register is 1 after selecting a pipe.

26.3.8 Control Transfers Using DCP

In the data stage of control transfers, data is transferred using the default control pipe (DCP).

The DCP buffer memory is a 64-byte single buffer and is a fixed area that is shared for both control reading and control writing. The buffer memory can only be accessed through the CFIFO port.

26.3.8.1 Control transfers

(1) Setup stage

The USBFS sends an ACK response for the correct setup packet targeted to the USBFS. The USBFS operation in the setup stage is described as follows:

When receiving a new setup packet, the USBFS sets the following bits:

- INTSTS0.VALID bit to 1
- DCPCTR.PID[1:0] bits to NAK
- DCPCTR.CCPL bit to 0.

When receiving a data packet after the setup packet, the USBFS stores the request parameters in USBREQ, USBVAL, USBINDX, and USBLENG. Perform response processing with respect to the control transfer after setting the VALID bit to 0. When the VALID bit is 1, PID = BUF cannot be set, and the data stage cannot be terminated.

Using the function of the VALID bit, the USBFS can suspend the current processing request when receiving a new request during a control transfer. The USBFS can then send a response to the newest request.

Additionally, the USBFS automatically detects the direction bit, bit [8] of bmRequestType, and the request data length

(wLength) of the received request. The USBFS also automatically distinguishes between control read transfer, control write transfer, no-data control transfer, and control stage transitions. For an incorrect sequence, the sequence error of the control transfer stage transition interrupt is generated, and software is notified of the error. For the stage control of the USBFS, see Figure 26.14.

(2) Data stage

Data transfers associated with received USB requests are performed using the DCP. Before accessing the DCP buffer memory, specify the access direction using the CFIFOSEL.ISEL bit. If the transfer data is larger than the size of the DCP buffer memory, perform data transfer using the BRDY interrupt for control write transfers and the BEMP interrupt for control read transfers.

(3) Status stage

Control transfers are terminated by setting the DCPCTR.CCPL bit to 1 while the DCPCTR.PID[1:0] bits are set to BUF.

After the specified settings are made, the USBFS automatically executes the status stage according to the data transfer direction determined at the setup stage. The procedure is as follows:

- For control read transfers:
  A zero-length packet is received from the USB host and an ACK response is sent.
- For control write transfers and no-data control transfers:
  A zero-length packet is transmitted and an ACK response is received from the USB host.

(4) Control transfer auto response function

The USBFS automatically responds to a correct SET_ADDRESS request. If any of the following errors occurs in the SET_ADDRESS request, a response from software is required:

- bmRequestType is not 00h — any transfer other than a control write transfer
- wIndex is not 00h — request error
- wLength is not 00h — any transfer other than a no-data control transfer
- wValue is larger than 7Fh — request error
- INTSTS0.DVSQ[2:0] are 011b (Configured state) — control transfer of a device state error.

For all requests other than the SET_ADDRESS request, a response is required from the associated software.

26.3.9 Bulk Transfers (PIPE4 and PIPE5)

The buffer memory usage (single or double buffer setting) can be selected for bulk transfers. The USBFS provides the following functions for bulk transfers:

- BRDY interrupt function (PIPECFG.BFRE bit, see section 26.3.3.1, (2) When the SOFCFG.BRDYM bit = 0 and the PIPECFG.BFRE bit = 1)
- Transaction count function (PIPEnTRE.TRENB, TRCLR, and PIPEnTRN.TRNCNT[15:0] bits, see section 26.3.4.5, Transaction counter for PIPE4 and PIPE5 in the receiving direction)
- Response PID = NAK function (PIPECFG.SHTNAK bit, see section 26.3.4.8, Response PID = NAK function)
- Auto response mode (PIPEnCTR.ATREPM bit, see section 26.3.4.9, Auto response mode).

26.3.10 Interrupt Transfers (PIPE6 and PIPE7)

The USBFS performs interrupt transfers based on the timing controlled by the host controller.

26.3.11 Pipe Schedule

26.3.11.1 Transfer schedule

This section describes the transfer scheduling within a frame of the USBFS. After the USBFS sends an SOF, the transfer is performed in the sequence as described in this section.

1. Execution of periodic transfers

A pipe is searched in the order of PIPE6 → PIPE7, if there is a pipe for which an interrupt transfer transaction can be generated, the transaction is generated.

2. Setup transactions for control transfers
   The DCP is checked and if a setup transaction is possible, it is sent.
3. Execution of bulk transfers, control transfer data stages, and control transfer status stages
   A pipe is searched in the order of DCP → PIPE4 → PIPE5, if there is a pipe for which a transaction is for a bulk transfer, a control transfer data stage, or a control transfer status stage, the transaction is generated.
   When a transaction is generated, processing moves to the next transaction pipe regardless of whether the response from the peripheral device is ACK or NAK. If there is time for transfer within the frame, this step is repeated.

26.3.12 Battery Charging Detection Processing

It is possible to control the processing for data contact detection (D+ line contact check), primary detection (charger detection), and secondary detection (charger verification), which are defined in the Battery Charging Specification. This section describes the required operations for a function device and a host device, individually.

26.3.12.1 Processing

The following processing is required when operating the USBFS module as a portable device for battery charging:

1. Detect when the data lines (D+ and D-) made contact and start the processing for primary detection.
2. After primary detection starts, wait 40 ms for masking, then check the D- voltage level to confirm the primary detection result.
3. If the charger is detected during primary detection, start the secondary detection.
4. After the secondary detection starts, wait 40 ms for masking, then check the D+ voltage level to confirm the secondary detection result.

For step 1., after VBUS is detected using the VBINT bit and the VBSTS bit, wait for 300 to 900 ms by software, then set the VDPSRCE0 and IDMSINKE0 bits in the USBBCCTRL0 register. You can also set the IDPSRCE0 bit and after a change from high to low on the D+ line is detected using the LNST bits, clear the IDPSRCE0 bit and set the VDPSRCE0 and IDMSINKE0 bits. Set the VDPSRCE0 and IDMSINKE0 bits at the same time.*1

For step 2., set the VDPSRCE0 and IDMSINKE0 bits and wait 40 ms by software, and then use the CHGDETSTS0 bit to verify the primary detection result.*2

For step 3., if the CHGDETSTS0 bit is set in step 2., verify that the charger is detected, then clear the VDPSRCE0 and IDMSINKE0 bits, and set the VDMSRCE0 and IDPSINKE0 bits.

For step 4., set the VDMSRCE0 and IDPSINKE0 bits and wait for 40 ms by software, then use the PDDETSTS0 bit to verify the secondary detection result.

Figure 26.15 shows the process flow.

Note 1. The Battery Charging Specification describes two ways to process data contact detection (D+/D- line contact check). One method is to detect a change to logic low due to the pull-down resistor of the host device when the D+ and D- lines make contact with the target, while the D+ line is held at logic high by applying a current of 7 to 13μA on the D+ line. The other method is to wait for 300 to 900 ms after VBUS is detected.

Note 2. During primary detection, when the voltage on the D- line is detected to be 0.25 to 0.4 V or above and 0.8 to 2.0 V or below, the target device is recognized as the host device for battery charging, that is, charging downstream port. When using a PHY in which the CHGDETSTS0 bit only indicates that the voltage on the D- line is 0.25 to 0.4 V or above, add the processing to check that the voltage on D- line is 0.8 V to 2.0 V or below using the LNST bits, as necessary.

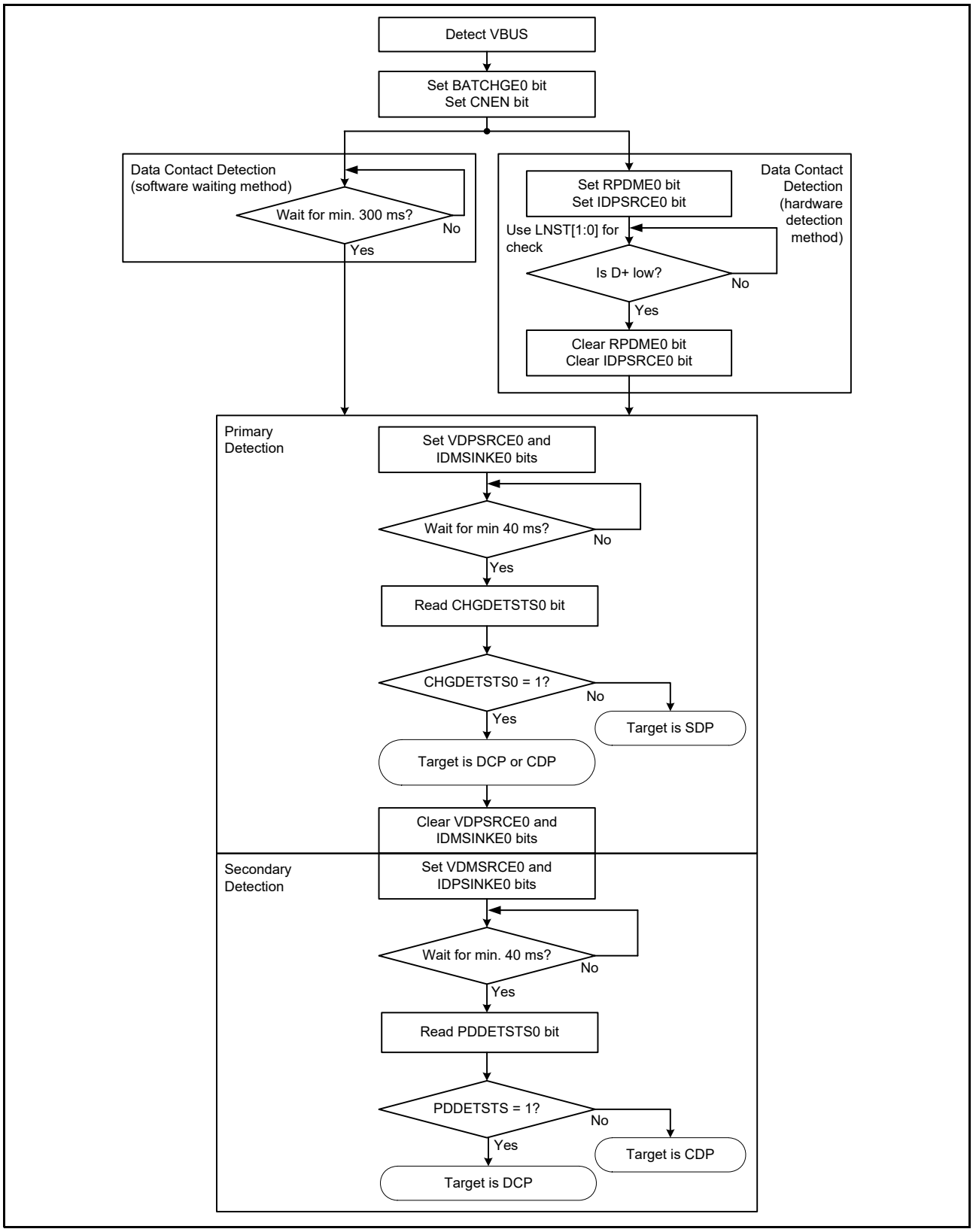


Figure 26.15 Process flow for operating as portable device

26.4 Usage Note

26.4.1 Settings for the Module-Stop State

The Module Stop Control Register B (MSTPCRB) can enable or disable USBFS operation. The USBFS is stopped after a reset. The registers become accessible on release from the module-stop state. For details, see section 10, Low Power Modes.

26.4.2 Clear of Interrupt Status Register after Software Standby mode

When the following conditions are met at the same time, the unexpected interrupt might occur because the input buffer is always enabled in the Software Standby mode:

- Enable the interrupt when the MCU is Normal mode
- Prohibit the interrupt when the MCU is Software Standby mode
- When the input level of pin which cancels the software standby is changed in Software Standby mode.

The interrupt flag is set to the interrupt status register in the specified condition. After canceling the Software Standby mode, the unexpected interrupt can be propagated to the interrupt controller. Therefore, in the canceling sequence, the INTSTS0 and INTSTS1 registers must be cleared.

26.4.3 Clear of Interrupt Status Register after Setting the Port Function

The input buffer is disabled before setting the port (PmnPFS.PSEL and PmnPFS.PMR) so the internal signal is fixed to high or low. Therefore, the input buffer is enabled after setting the port, so the external pin state is propagated into the chip. At this time, an unexpected interrupt might occur and the interrupt status such as INTSTS0 is set to 1, especially the VBINT bit. To avoid malfunction, the INTSTS0 register must be cleared after setting the port.

27. Serial Communications Interface (SCI)

27.1 Overview

The Serial Communications Interface (SCI) is configurable to five asynchronous and synchronous serial interfaces:

- Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA))
- 8-bit clock synchronous interface
- Simple IIC (master-only)
- Simple SPI
- Smart card interface.

The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. SCI0 has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator.

Table 27.1 lists the SCI specifications, Figure 27.1 shows a block diagram, and Table 27.2 lists the pin configuration of the SCI for the individual modes.

Table 27.1 SCI specifications (1 of 2)

Parameter	Description
Serial communication modes	• Asynchronous • Clock synchronous • Smart card interface • Simple IIC • Simple SPI.
Transfer speed	Bit rate specifiable with the on-chip baud rate generator
Full-duplex communications	Transmitter: Continuous transmission possible using double-buffering Receiver: Continuous reception possible using double-buffering
I/O pins	See Table 27.2
Data transfer	Selectable as LSB-first or MSB-first transfer
Interrupt sources	Transmit end, transmit data empty, receive data full, receive error, receive data ready, and address match Completion of generation of a start condition, restart condition, or stop condition (for simple IIC mode)
Module-stop function	Module-stop state can be set for each channel
Snooze end request	SCI0 address mismatch (SCI0_DCUF)

Table 27.1 SCI specifications (2 of 2)

Parameter		Description
Asynchronous mode	Data length	7, 8, or 9 bits
	Transmission stop bit	1 or 2 bits
	Parity	Even parity, odd parity, or no parity
	Receive error detection	Parity, overrun, and framing errors
	Hardware flow control	CTSn_RTSn pin can be used in controlling transmission/reception
	Transmission/Reception	Selectable as either 1 stage register or 16 stage FIFO (only SCI0 supports FIFO)
	Address match	The interrupt request/event output can be issued when detecting a match between received data and the value of compare match register
	Address mismatch (SCI0 only) receive data	The snooze end request can be issued when detecting the mismatch between the received data and the value of the Compare Match Register
	Start-bit detection	Low level or falling edge is selectable
	Break detection	Break detectable on framing error with SPTR register read
	Clock source	An internal or external clock can be selected
	Double-speed mode	Baud rate generator double-speed mode is selectable
	Multi-processor communications function	Serial communication between multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters
Clock synchronous mode	Data length	8 bits
	Receive error detection	Overrun error
	Clock source	An internal clock (Master mode) or external clock (Slave mode) can be selected
	Hardware flow control	CTSn_RTSn pin can be used in controlling transmission/reception
	Transmission/Reception	Selectable as either 1 stage register or 16 stage FIFO (only SCI0 supports FIFO)
Smart card interface mode	Error processing	An error signal can be automatically transmitted when detecting a parity error during reception
		Data can be automatically retransmitted when receiving an error signal during transmission
	Data type	Both direct convention and inverse convention are supported
Simple IIC mode	Transfer format	I^2C bus format (MSB-first only)
	Operating mode	Master (single-master operation only)
	Transfer rate	Up to 400 kbps
	Noise cancellation	The signal paths from input on the SCLn and SDAn pins incorporate digital noise filters, and provide an adjustable interval for noise cancellation
Simple SPI mode	Data length	8 bits
	Detection of errors	Overrun error
	Clock source	An internal clock (Master mode) or external clock (Slave mode) can be selected
	SS input pin function	Applying the high level to the SSn pin can cause the output pins to enter the high impedance state
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable
Bit rate modulation function		Correction of outputs from the on-chip baud rate generator can reduce errors
Event link function		Error (receive error or error signal detection) event output (SCIn_ERI*1)
		Receive data full event output (SCIn_RXI*1, *2)
		Transmit data empty event output (SCIn_TXI*1, *2)
		Transmit end event output (SCIn_TEI*1, *2)
		Address match event output (SCIn_AM*1)

Note 1. Channel number (n = 0, 1, 9)

Note 2. Using this event link function is prohibited when the FIFO is selected in asynchronous mode.

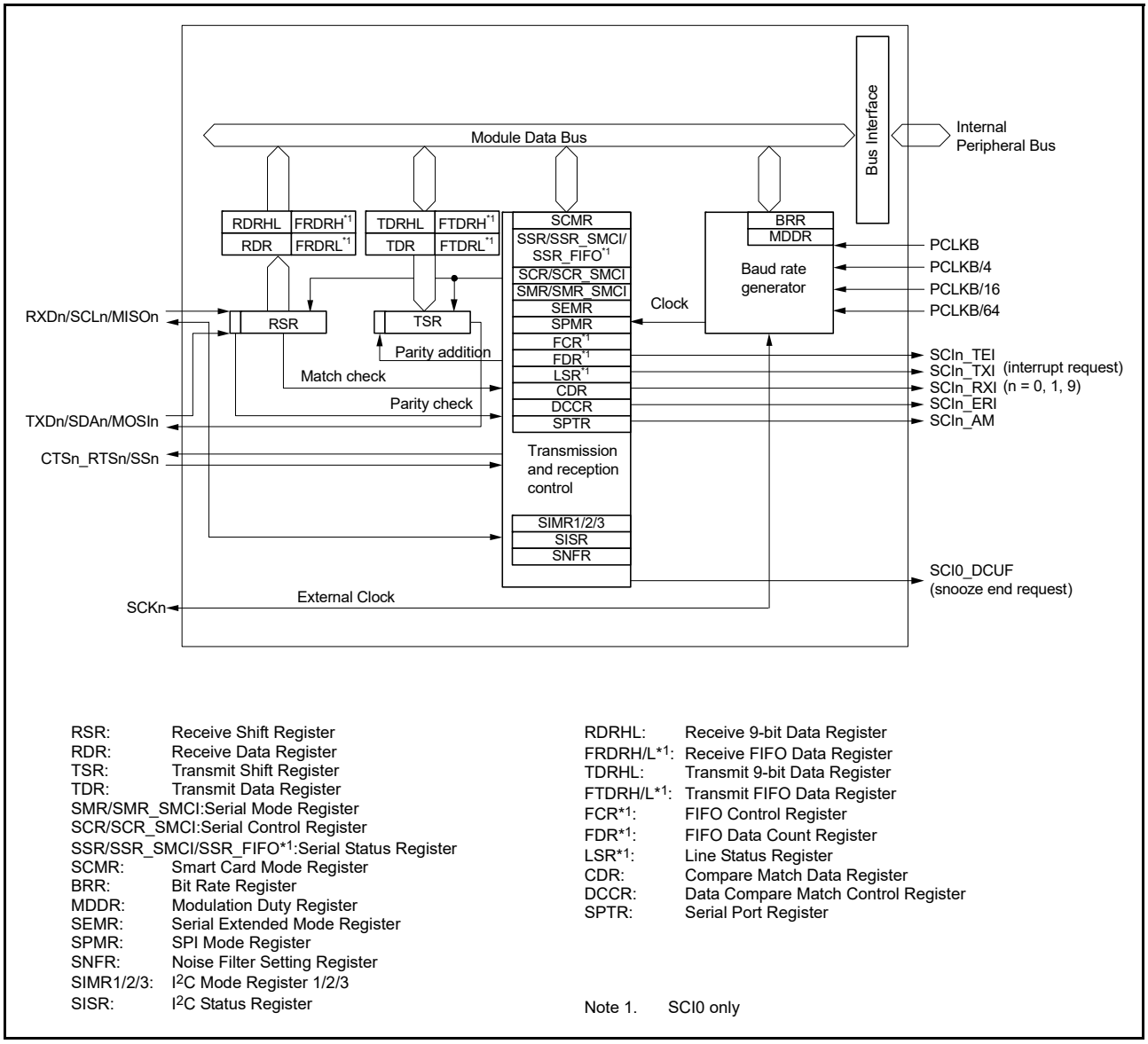


Figure 27.1 SCI block diagram

Table 27.2 SCI I/O pins (1 of 2)

Channel	Pin name	Input/Output	Function
SCI0	SCK0	Input/Output	SCI0 clock input/output
	RXD0/SCL0/ MISO0	Input/Output	SCI0 receive data input SCI0 IIC clock input/output SCI0 slave transmit data input/output
	TXD0/SDA0/ MOSI0	Input/Output	SCI0 transmit data output SCI0 IIC data input/output SCI0 master transmit data input/output
	SS0/CTS0_RTS0	Input/Output	SCI0 chip select input, active-low SCI0 transfer start control input/output, active-low

Table 27.2 SCI I/O pins (2 of 2)

Channel	Pin name	Input/Output	Function
SCI1	SCK1	Input/Output	SCI1 clock input/output
	RXD1/SCL1/ MISO1	Input/Output	SCI1 receive data input SCI1 IIC clock input/output SCI1 slave transmit data input/output
	TXD1/SDA1/ MOSI1	Input/Output	SCI1 transmit data output SCI1 IIC data input/output SCI1 master transmit data input/output
	SS1/CTS1_RTS1	Input/Output	SCI1 chip select input, active-low SCI1 transfer start control input/output, active-low
SCI9	SCK9	Input/Output	SCI9 clock input/output
	RXD9/SCL9/ MISO9	Input/Output	SCI9 receive data input SCI9 IIC clock input/output SCI9 slave transmit data input/output
	TXD9/SDA9/ MOSI9	Input/Output	SCI9 transmit data output SCI9 IIC data input/output SCI9 master transmit data input/output
	SS9/CTS9_RTS9	Input/Output	SCI9 chip select input, active-low SCI9 transfer start control input/output, active-low

27.2 Register Descriptions

27.2.1 Receive Shift Register (RSR)

RSR is a shift register that receives serial data input from the RXDn pin and converts it into parallel data. When one frame of data is received, it is automatically transferred to the RDR register, RDRHL register, or receive FIFO. The RSR register cannot be directly accessed by the CPU.

27.2.2 Receive Data Register (RDR)

Address(es): SCI0.RDR 4007 0005h, SCI1.RDR 4007 0025h, SCI9.RDR 4007 0125h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0

RDR is an 8-bit register that stores received data. When one frame of serial data is received, it is transferred from RSR to RDR, and the RSR register can receive more data. Because RSR and RDR function as a double buffer, continuous received operations can be performed.

Read the RDR only once after a receive data full interrupt (SCIn_RXI) occurs.

Note: If the next one frame of data is received before reading the received data from RDR, an overrun error occurs. The CPU cannot write to the RDR.

27.2.3 Receive 9-bit Data Register (RDRHL)

Address(es): SCI0.RDRHL 4007 0010h, SCI1.RDRHL 4007 0030h, SCI9.RDRHL 4007 0130h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RDRHL is a 16-bit register that stores received data. Use this register when asynchronous mode and 9-bit data length are selected.

The lower 8 bits of RDRHL are the shadow register of RDR, for example access to RDRHL affects the RDR register. Access to the RDRHL register is prohibited if 7-bit or 8-bit data length is selected.

After one frame of data is received, the received data is transferred from the RSR register to these registers, therefore allowing the RSR register to receive more data.

The RSR and RDRHL registers have a double-buffered construction to enable continuous reception. RDRHL should only be read when a receive data full interrupt (SCIn_RXI) request is issued. An overrun error occurs when the next frame of data is received before the received data is read from RDRHL. The CPU cannot write to the RDRHL register. Bits [15:9] are fixed to 0. These bits are read as 0. The write value should be 0.

27.2.4 Receive FIFO Data Register H, L, HL (FRDRH, FRDRL, FRDRHL)

Receive FIFO Data Register H (FRDRH)

Address(es): SCI0.FRDRH 4007 0010h

Receive FIFO Data Register L (FRDRL)

Address(es): SCI0.FRDRL 4007 0011h

Receive FIFO Data Register HL (FRDRHL)

Address(es): SCI0.FRDRHL 4007 0010h

	SCI0.FRDRHL															
	SCI0.FRDRH								SCI0.FRDRL							
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	RDF	ORER	FER	PER	DR	MPB	RDAT[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b8 to b0	RDAT[8:0]	Serial Receive Data	Valid only in asynchronous mode, including multi-processor or clock synchronous mode, and with FIFO selected. It can read serial receive data.	R
b9	MPB	Multi-Processor Bit Flag	Valid only in asynchronous mode with SMR.MP = 1 and FIFO selected. It can read multi-processor bit associated with serial receive data (RDAT[8:0]): 0: Data transmission cycles 1: ID transmission cycles.	R
b10	DR	Receive Data Ready Flag	This flag is the same as SSR_FIFO.DR: 0: Receiving is in progress, or no received data remains in FRDRH and FRDRL after a normal completion of received data 1: Next receive data is not received for a period after a normal completion of received data.	R*1
b11	PER	Parity Error Flag	0: No parity error occurred at the first data of FRDRH and FRDRL 1: A parity error occurred at the first data of FRDRH and FRDRL.	R
b12	FER	Framing Error Flag	0: No framing error occurred at the first data of FRDRH and FRDRL 1: A framing error occurred at the first data of FRDRH and FRDRL.	R
b13	ORER	Overrun Error Flag	It is same as SSR_FIFO.ORER: 0: No overrun error occurred 1: An overrun error occurred.	R*1

Bit	Symbol	Bit name	Description	R/W
b14	RDF	Receive FIFO Data Full Flag	It is same as SSR_FIFO.RDF: 0: The amount of received data written in FRDRH and FRDRL is below the specified received triggering number 1: The amount of received data written in FRDRH and FRDRL is equal to or greater than the specified received triggering number.	R*1
b15	—	Reserved	This bit is read as 0.	R

Note 1. If this flag is read, it is the same as a read of the SSR_FIFO register. Write 0 to the SSR_FIFO register to clear the flag.

FRDRHL is a 16-bit register that consists of FRDRL and FRDRH.

FRDRH and FRDRL constitute a 16-stage FIFO register that stores serial receive data and related status information. Software can read serial receive data and related status information. This register is only valid in asynchronous mode, including multi-processor mode or clock synchronous mode.

The SCI completes a reception of one frame of serial data by transferring the received data from the Receive Shift Register (RSR) into FRDRH and FRDRL for storage. Continuous reception is executed until 16 stages are stored. If data is read when there is no received data in FRDRH and FRDRL, the value is undefined. When FRDRH and FRDRL are full of received data, subsequent serial receive data is lost. The CPU can read from FRDRH and FRDRL but cannot write to them.

Reading 1 from the RDF, ORER, or DR flags of the FRDRH register is the same as reading those bits from the SSR_FIFO register. When writing 0 to clear the flag in the SSR_FIFO register after reading the FRDRH register, write 0 only in the cleared flag and write 1 otherwise.

When reading both the FRDRH and FRDRL registers, read in the order from FRDRH to FRDRL. The FRDRHL register can be accessed in 16-bit units.

27.2.5 Transmit Data Register (TDR)

Address(es): SCI0.TDR 4007 0003h, SCI1.TDR 4007 0023h, SCI9.TDR 4007 0123h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

TDR is an 8-bit register that stores transmit data.

When the SCI detects that TSR is empty, it transfers the transmit data written in TDR to TSR and starts transmission.

The double-buffered structures of TDR and TSR enable continuous serial transmission. If the next transmit data is already written to TDR when one frame of data is transmitted, the SCI transfers the written data to TSR to continue transmission.

The CPU can read from or write to TDR at any time. Only write transmit data to TDR once after each instance of the transmit data empty interrupt (SCIn_TXI).

27.2.6 Transmit 9-Bit Data Register (TDRHL)

Address(es): SCI0.TDRHL 4007 000Eh, SCI1.TDRHL 4007 002Eh, SCI9.TDRHL 4007 012Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

TDRHL is a 16-bit register that stores transmit data. Use this register when asynchronous mode and 9-bit data length are selected.

The lower 8 bits of TDRHL are the shadow register of TDR for example, access to TDRHL affects the TDR register.

Access to the TDRHL register is prohibited if 7-bit or 8-bit data length is selected.

When empty space is detected in the TSR register, the transmit data stored in the TDRHL registers is transferred to TSR and transmission is started.

The TSR and TDRHL registers have a double-buffered structure to support continuous transmission. When the next data to be transmitted is stored in TDRHL after one frame of data is transmitted, the transmitting operation continues by transferring to the TSR register.

The CPU can read and write to the TDRHL register. Bits [15:9] in TDRHL are fixed to 1. These bits are read as 1. The write value should be 1.

Writing transmit data to the TDRHL register should be performed only once when a transmit data empty interrupt (SCIn_TXI) request is issued.

27.2.7 Transmit FIFO Data Register H, L, HL (FTDRH, FTDRL, FTDRHL)

Transmit FIFO Data Register H (FTDRH)

Address(es): SCI0.FTDRH 4007 000Eh

Transmit FIFO Data Register L (FTDRL)

Address(es): SCI0.FTDRL 4007 000Fh

Transmit FIFO Data Register HL (FTDRHL)

Address(es): SCI0.FTDRHL 4007 000Eh

	SCI0.FTDRHL															
	SCI0.FTDRH								SCI0.FTDRL							
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	MPBT	TDAT[8:0]								
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b8 to b0	TDAT[8:0]	Serial Transmit Data	Valid only in asynchronous mode including multi-processor or clock synchronous mode, and with FIFO selected. It can write serial transmit data.	W
b9	MPBT	Multi-Processor Transfer Bit Flag	Valid only in asynchronous mode and SMR.MP = 1 and FIFO selected. Value of the multi-processor bit in the transmission frame: 0: Data transmission cycles 1: ID transmission cycles.	W
b15 to b10	—	Reserved	The write value should be 1.	W

FTDRHL is a 16-bit register that consists of FTDRH and FTDRL.

FTDRH and FTDRL constitute a 16-stage FIFO register that stores data for serial transmission and multi-processor transfer bit. This register is valid only in asynchronous mode, including multi-processor mode or clock synchronous mode.

When the SCI detects that the Transmit Shift Register (TSR) is empty, it transmits data written in the FTDRH and FTDRL into TSR and starts serial transmission. Continuous serial transmission is executed until no transmit data is left in FTDRH and FTDRL. When FTDR is full of transmit data, no more data can be written. If writing new data is attempted, the data is ignored. The CPU can write to FTDRH and FTDRL but cannot read them.

When writing to both the FTDRH and FTDRL registers, write in the order from FTDRH to FTDRL.

MPBT bit (Multi-Processor Transfer Bit Flag)

Selects the multi-processor bit of the transmit frame.

When FCR.FM = 1, SSR.MPBT is not valid.

27.2.8 Transmit Shift Register (TSR)

TSR is a shift register that transmits serial data. To perform serial data transmission, the SCI first automatically transfers transmit data from TDR, TDRHL, or transmit FIFO to TSR, then sends the data to the TXDn pin. The CPU cannot directly access the TSR.

27.2.9 Serial Mode Register (SMR) for Non-Smart Card Interface mode (SCMR.SMIF = 0)

Address(es): SCI0.SMR 4007 0000h, SCI1.SMR 4007 0020h, SCI9.SMR 4007 0120h

	b7	b6	b5	b4	b3	b2	b1	b0
	CM	CHR	PE	PM	STOP	MP	CKS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	CKS[1:0]	Clock Select	b1 b0 0 0: PCLKB clock (n = 0)*1 0 1: PCLKB/4 clock (n = 1)*1 1 0: PCLKB/16 clock (n = 2)*1 1 1: PCLKB/64 clock (n = 3)*1.	R/W*4
b2	MP	Multi-Processor Mode	Valid only in asynchronous mode: 0: Multi-processor communications function is disabled 1: Multi-processor communications function is enabled.	R/W*4
b3	STOP	Stop Bit Length	Valid only in asynchronous mode: 0: 1 stop bit 1: 2 stop bits.	R/W*4
b4	PM	Parity Mode	Valid only when the PE bit is 1: 0: Selects even parity 1: Selects odd parity.	R/W*4
b5	PE	Parity Enable	Valid only in asynchronous mode: • When transmitting: 0: Parity bit addition is not performed 1: The parity bit is added. • When receiving: 0: Parity bit checking is not performed 1: The parity bit is checked.	R/W*4
b6	CHR	Character Length	Valid only in asynchronous mode*2. Selects in combination with the CHR1 bit in SCMR. CHR1CHR 0 0: Transmit/receive in 9-bit data length 0 1: Transmit/receive in 9-bit data length 1 0: Transmit/receive in 8-bit data length (initial value) 1 1: Transmit/receive in 7-bit data length*3.	R/W*4
b7	CM	Communication Mode	0: Asynchronous mode or simple IIC mode 1: Clock synchronous mode or simple SPI mode.	R/W*4

Note 1. n is the decimal notation of the value of n in BRR, see section 27.2.17, Bit Rate Register (BRR).
Note 2. In other than asynchronous mode, this bit setting is invalid and a fixed data length of 8 bits is used.
Note 3. LSB-first is fixed and the MSB bit [7] in TDR is not transmitted in transmission.
Note 4. Writable only when TE in SCR = 0 and RE in SCR = 0 (both serial transmission and reception are disabled).

The SMR register sets the communication format and clock source for the on-chip baud rate generator.

CKS[1:0] bits (Clock Select)

The CKS[1:0] bits select the clock source for the on-chip baud rate generator.

For the relationship between the settings of these bits and the baud rate, see section 27.2.17, Bit Rate Register (BRR).

MP bit (Multi-Processor Mode)

The MP bit disables or enables the multi-processor communications function. The settings of the PE bit and PM bit are invalid in multi-processor mode.

STOP bit (Stop Bit Length)

The STOP bit selects the stop bit length in transmission.

In reception, only the first stop bit is checked regardless of this bit setting. If the second stop bit is 0, it is treated as the start bit of the next transmit frame.

PM bit (Parity Mode)

The PM bit selects the parity mode (even or odd) for transmission and reception.

The setting of the PM bit is invalid in multi-processor mode.

PE bit (Parity Enable)

When the PE bit is set to 1, the parity bit is added to transmit data, and the parity bit is checked in reception.

Irrespective of the setting of the PE bit, the parity bit is not added or checked in multi-processor format.

CHR bit (Character Length)

The CHR bit selects the data length for transmission and reception in combination with the CHR1 bit in SCMR.

In modes other than asynchronous mode, a fixed data length of 8 bits is used.

CM bit (Communication Mode)

The CM bit selects the communication mode:

- Asynchronous mode or simple IIC mode
- Clock synchronous mode or simple SPI mode.

27.2.10 Serial Mode Register for Smart Card Interface Mode (SMR_SMCI) (SCMR.SMIF = 1)

Address(es): SCI0.SMR_SMCI 4007 0000h, SCI1.SMR_SMCI 4007 0020h, SCI9.SMR_SMCI 4007 0120h

	b7	b6	b5	b4	b3	b2	b1	b0
	GM	BLK	PE	PM	BCP[1:0]		CKS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	CKS[1:0]	Clock Select	b1 b0 0 0: PCLKB clock (n = 0)*1 0 1: PCLKB/4 clock (n = 1)*1 1 0: PCLKB/16 clock (n = 2)*1 1 1: PCLKB/64 clock (n = 3)*1.	R/W*2
b3, b2	BCP[1:0]	Base Clock Pulse	Selects the number of base clock cycles in combination with the BCP2 bit in SCMR. Table 27.3 lists the combinations of the SCMR.BCP2 bit and SMR.BCP[1:0] bits.	R/W*2
b4	PM	Parity Mode	Valid only when the PE bit is 1: 0: Selects even parity 1: Selects odd parity.	R/W*2

Bit	Symbol	Bit name	Description	R/W
b5	PE	Parity Enable	When this bit is set to 1, a parity bit is added to transmit data, and the parity of received data is checked. Set this bit to 1 in smart card interface mode.	R/W*2
b6	BLK	Block Transfer Mode	0: Non-block transfer mode operation 1: Block transfer mode operation.	R/W*2
b7	GM	GSM Mode	0: Normal mode operation 1: Non-GSM mode operation.	R/W*2

Note 1. n is the decimal notation of the value of n in BRR, see section 27.2.17, Bit Rate Register (BRR).
Note 2. Writable only when TE in SCR_SMCI = 0 and RE in SCR_SMCI = 0 (both serial transmission and reception are disabled).

The SMR_SMCI register sets the communication format and clock source for the on-chip baud rate generator.

CKS[1:0] bits (Clock Select)

The CKS[1:0] bits select the clock source for the on-chip baud rate generator.

For the relationship between the settings of these bits and the baud rate, see section 27.2.17, Bit Rate Register (BRR).

BCP[1:0] bits (Base Clock Pulse)

The BCP[1:0] bits select the number of base clock cycles in a 1-bit data transfer time in smart card interface mode.

Set these bits in combination with the BCP2 bit in SCMR.

For details, see section 27.6.4, Receive Data Sampling Timing and Reception Margin.

Table 27.3 Combinations of SCMR.BCP2 bit and SMR_SMCI.BCP[1:0] bits

SCMR.BCP2 bit	SMR_SMCI.BCP[1:0] bits		Number of base clock cycles for 1-bit transfer period
0	0	0	93 clock cycles (S = 93)*1
0	0	1	128 clock cycles (S = 128)*1
0	1	0	186 clock cycles (S = 186)*1
0	1	1	512 clock cycles (S = 512)*1
1	0	0	32 clock cycles (S = 32)*1 (Initial Value)
1	0	1	64 clock cycles (S = 64)*1
1	1	0	372 clock cycles (S = 372)*1
1	1	1	256 clock cycles (S = 256)*1

Note 1. S is the value of S in BRR (see section 27.2.17, Bit Rate Register (BRR)).

PM bit (Parity Mode)

The PM bit selects the parity mode for transmission and reception (even or odd).

For details on the usage of this bit in smart card interface mode, see section 27.6.2, Data Format (Except in Block Transfer Mode).

PE bit (Parity Enable)

Set the PE bit to 1.

The parity bit is added to transmit data before transmission, and the parity bit is checked in reception.

BLK bit (Block Transfer Mode)

Setting the BLK bit to 1 enables block transfer mode operation.

For details, see section 27.6.3, Block Transfer Mode.

GM bit (GSM Mode)

Setting the GM bit to 1 enables GSM mode operation.

In GSM mode, the SSR_SMCI.TEND flag set timing is moved forward to 11.0 ETU (elementary time unit = 1-bit

transfer time) from the start and the clock output control function is appended. For details, see section 27.6.6, Serial Data Transmission (Except in Block Transfer Mode) and section 27.6.8, Clock Output Control.

27.2.11 Serial Control Register (SCR) for Non-Smart Card Interface Mode (SCMR.SMIF = 0)

Address(es): SCI0.SCR 4007 0002h, SCI1.SCR 4007 0022h, SCI9.SCR 4007 0122h

	b7	b6	b5	b4	b3	b2	b1	b0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	CKE[1:0]	Clock Enable	Asynchronous mode: b1 b0 0 0: On-chip baud rate generator. The SCKn pin is available for use as an I/O port according to the I/O port settings. 0 1: On-chip baud rate generator. The clock with the same frequency as the bit rate is output from the SCKn pin. 1 x: External clock. • The clock with a frequency 16 times the bit rate should be input from the SCKn pin (when SEMR.ABCS bit is 0). Input a clock signal with a frequency eight times the bit rate when the SEMR.ABCS bit is 1. Clock synchronous mode: b1 b0 0 x: Internal clock. The SCKn pin functions as the clock output pin. 1 x: External clock. The SCKn pin functions as the clock input pin.	R/W*1
b2	TEIE	Transmit End Interrupt Enable	0: An SCIn_TEI interrupt request is disabled 1: An SCIn_TEI interrupt request is enabled.	R/W
b3	MPIE	Multi-Processor Interrupt Enable	Valid in asynchronous mode when SMR.MP = 1: 0: Non-multiprocessor reception 1: When data with the multi-processor bit set to 0 is received, the data is not read, and setting the status flags RDRF, RDF, ORER, and FER in SSR to 1 is disabled. When data with the multiprocessor bit set to 1 is received, the MPIE bit is automatically cleared to 0, and non-multiprocessor reception.	R/W*3
b4	RE	Receive Enable	0: Serial reception is disabled 1: Serial reception is enabled.	R/W*2
b5	TE	Transmit Enable	0: Serial transmission is disabled 1: Serial transmission is enabled.	R/W*2
b6	RIE	Receive Interrupt Enable	0: SCIn_RXI and SCIn_ERI interrupt requests are disabled 1: SCIn_RXI and SCIn_ERI interrupt requests are enabled.	R/W
b7	TIE	Transmit Interrupt Enable	0: An SCIn_TXI interrupt request is disabled 1: An SCIn_TXI interrupt request is enabled.	R/W

x: Don't care

Note 1. Writable only when TE = 0 and RE = 0.
Note 2. 1 can only be written when TE = 0 and RE = 0, while the SMR.CM bit is 1. After setting TE or RE to 1, only 0 can be written in TE and RE. While the SMR.CM bit is 0 and the SIMR1.IICM bit is 0, writing is enabled under any condition.
Note 3. When writing a new value to a bit other than the MPIE bit of this register during multi-processor mode (SMR.MP bit = 1), write 0 to MPIE bit using the store instruction to avoid accidentally setting the MPIE bit to 1 by read modify write when using a bit manipulation instruction.

SCR sets control and the clock source selection for transmission and reception.

CKE[1:0] bits (Clock Enable)

The CKE[1:0] bits select the clock source and SCKn pin function.

TEIE bit (Transmit End Interrupt Enable)

The TEIE bit enables or disables an SCIn_TEI interrupt request.

An SCIn_TEI interrupt request is disabled by setting the TEIE bit to 0.

In simple IIC mode, the SCIn_TEI is allocated to the interrupt on completion of issuing a start, restart, or stop condition (STIn). In this case, the TEIE bit can be used to enable or disable the STI.

MPIE bit (Multi-Processor Interrupt Enable)

When the MPIE bit is set to 1 and data with the multi-processor bit set to 0 is received, the data is not read and setting the status flags RDRF, RDF, ORER, and FER in SSR/SSR_FIFO to 1 is disabled. When data with the multi-processor bit set to 1 is received, the MPIE is automatically cleared to 0, and non-multiprocessor reception resumes. For details, see section 27.4, Multi-Processor Communications Function.

When the received data includes the MPB bit in the SSR is set to 0, the received data is not transferred from the RSR to the RDR, a receive error is not detected, and setting the flags ORER and FER to 1 is disabled.

When the received data includes the MPB bit is set to 1, the MPIE bit is automatically cleared to 0, the SCIn_RXI and SCIn_ERI interrupt requests are enabled (if the RIE bit in SCR is set to 1), and the setting of the ORER and FER flags to 1 is enabled.

MPIE should be set to 0 if the multi-processor communications function is not used.

RE bit (Receive Enable)

The RE bit enables or disables serial reception.

When this bit is set to 1, serial reception starts by detecting the start bit in asynchronous mode or the synchronous clock input in clock synchronous mode. SMR should be set prior to setting the RE bit to 1 to designate the reception format.

When reception is halted by setting the RE bit to 0, the RDRF, ORER, FER, and PER flags in SSR are not affected and the previous value is retained when non-FIFO is selected. When reception is halted by setting the RE bit to 0, the RDF, ORER, FER, PER, and DR flags in SSR_FIFO are not affected and the previous value is retained when FIFO selected.

TE bit (Transmit Enable)

The TE bit enables or disables serial transmission.

When this bit is set to 1, serial transmission starts by writing transmit data to TDR.

Note: SMR should be set prior to setting the TE bit to 1 to designate the transmission format.

RIE bit (Receive Interrupt Enable)

The RIE bit enables or disables SCIn_RXI and SCIn_ERI interrupt requests.

Setting the RIE bit to 0 disables SCIn_RXI and SCIn_ERI interrupt requests.

To cancel an SCIn_ERI interrupt request, read 1 from the ORER, FER, or PER flag in SSR/SSR_FIFO, then set the flag to 0, or set the RIE bit to 0.

TIE bit (Transmit Interrupt Enable)

The TIE bit enables or disables SCIn_TXI interrupt request.

SCIn_TXI interrupt requests are disabled by setting the TIE bit to 0.

Note: To switch the TIE bit value from 0 to 1 in FIFO mode, set the TIE and TE bits to 1 simultaneously or set the TIE bit to 1 when TE = 1. When TE = 0 in FIFO mode, setting the TIE bit to 1 is prohibited.

27.2.12 Serial Control Register for Smart Card Interface Mode (SCR_SMCI) (SCMR.SMIF = 1)

Address(es): SCI0.SCR_SMCI 4007 0002h, SCI1.SCR_SMCI 4007 0022h, SCI9.SCR_SMCI 4007 0122h

	b7	b6	b5	b4	b3	b2	b1	b0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	CKE[1:0]	Clock Enable	• When GM in SMR_SMCI = 0: b1 b0 0 0: Output disabled. The SCKn pin is available for use as an I/O port according to the I/O port settings. 0 1: Clock output 1 x: Setting prohibited. • When GM in SMR_SMCI = 1 b1 b0 0 0: Output fixed low x 1: Clock output 1 0: Output fixed high.	R/W*1
b2	TEIE	Transmit End Interrupt Enable	This bit should be 0 in smart card interface mode	R/W
b3	MPIE	Multi-Processor Interrupt Enable	This bit should be 0 in smart card interface mode	R/W
b4	RE	Receive Enable	0: Serial reception is disabled 1: Serial reception is enabled.	R/W*2
b5	TE	Transmit Enable	0: Serial transmission is disabled 1: Serial transmission is enabled.	R/W*2
b6	RIE	Receive Interrupt Enable	0: SCIn_RXI and SCIn_ERI interrupt requests are disabled 1: SCIn_RXI and SCIn_ERI interrupt requests are enabled.	R/W
b7	TIE	Transmit Interrupt Enable	0: An SCIn_TXI interrupt request is disabled 1: An SCIn_TXI interrupt request is enabled.	R/W

x: Don't care

Note 1. Writable only when TE = 0 and RE = 0.
Note 2. 1 can be written only when TE = 0 and RE = 0. After setting TE or RE to 1, only 0 can be written in TE and RE.

SCR_SMCI sets transmission control, interrupt control and reception and clock source selection for transmission and reception.

For details on interrupt requests, see section 27.10, Interrupt Sources.

CKE[1:0] bits (Clock Enable)

The CKE[1:0] bits control the clock output from the SCKn pin.

In GSM mode, clock output can be dynamically switched. For details, see section 27.6.8, Clock Output Control.

TEIE bit (Transmit End Interrupt Enable)

The TEIE bit should be 0 in smart card interface mode.

RE bit (Receive Enable)

The RE bit enables or disables serial reception.

When this bit is set to 1, serial reception starts by detecting the start bit.

Note: SMR_SMCI should be set prior to setting the RE bit to 1 to designate the reception format.

When reception is halted by setting the RE bit to 0, the ORER, FER, and PER flags in SSR_SMCI are not affected and the previous value is retained.

TE bit (Transmit Enable)

The TE bit enables or disables serial transmission.

When this bit is set to 1, serial transmission starts by writing transmit data to TDR.

Note: SMR_SMCI should be set prior to setting the TE bit to 1 to designate the transmission format.

RIE bit (Receive Interrupt Enable)

The RIE bit enables or disables SCIn_RXI and SCIn_ERI interrupt requests.

Setting the RIE bit to 0 disables SCIn_RXI and SCIn_ERI interrupt requests.

To cancel an SCIn_ERI interrupt request, read 1 from the ORER, FER, or PER flag in SSR_SMCI, then set the flag to 0, or set the RIE bit to 0.

TIE bit (Transmit Interrupt Enable)

The TIE bit enables or disables SCIn_TXI interrupt request.

SCIn_TXI interrupt requests are disabled by setting the TIE bit to 0.

27.2.13 Serial Status Register (SSR) for Non-Smart Card Interface and Non-FIFO Mode (SCMR.SMIF = 0 and FCR.FM = 0)

Address(es): SCI0.SSR 4007 0004h, SCI1.SSR 4007 0024h, SCI9.SSR 4007 0124h

	b7	b6	b5	b4	b3	b2	b1	b0
	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
Value after reset:	1	0	0	0	0	1	0	0

Bit	Symbol	Bit name	Description	R/W
b0	MPBT	Multi-Processor Bit Transfer	Sets the multi-processor bit to add to the transmission frame: 0: Data transmission cycles 1: ID transmission cycles.	R/W
b1	MPB	Multi-Processor	Value of the multi-processor bit in the reception frame: 0: Data transmission cycles 1: ID transmission cycles.	R
b2	TEND	Transmit End Flag	0: A character is transmitted 1: Character transfer is complete.	R
b3	PER	Parity Error Flag	0: No parity error occurred 1: A parity error occurred.	R/W*1
b4	FER	Framing Error Flag	0: No framing error occurred 1: A framing error occurred.	R/W*1
b5	ORER	Overrun Error Flag	0: No overrun error occurred 1: An overrun error occurred.	R/W*1
b6	RDRF	Receive Data Full Flag	0: No received data is in RDR register 1: Received data is in RDR register.	R/W*1
b7	TDRE	Transmit Data Empty Flag	0: Transmit data is in TDR register 1: No transmit data is in TDR register.	R/W*1

Note 1. Only 0 can be written to clear the flag after reading 1.

The SSR register provides the SCI status flag and transmission/reception multi-processor bits.

MPBT bit (Multi-Processor Bit Transfer)

The MPBT bit selects the multi-processor bit of the transmit frame.

MPB bit (Multi-Processor)

The MPB bit holds the value of the multi-processor bit in the reception frame. This bit does not change when the SCR.RE bit is 0.

TEND flag (Transmit End Flag)

The TEND flag indicates completion of transmission.

[Setting conditions]

- When the SCR.TE bit is set to 0 (serial transmission is disabled) and the FCR.FM bit is set to 0 (non-FIFO selected)
- When the SCR.TE bit is set to 1, the TEND flag is not affected and retains the value 1
- When the TDR register is not updated at the time of transmission of the tail-end bit of a character being transmitted.

[Clearing conditions]

- When transmit data are written to the TDR register while the SCR.TE bit is 1
- When 0 is written to TDRE after reading TDRE = 1 while the SCR.TE bit is 1.

PER flag (Parity Error Flag)

The PER flag indicates that a parity error occurred during reception in asynchronous mode and the reception ends abnormally.

[Setting condition]

- When a parity error is detected during reception in asynchronous mode and the state of address match function is invalid (DCCR.DCME = 0).

  Although received data when the parity error occurs is transferred to RDR, no SCIn_RXI interrupt request occurs. When the PER flag is set to 1, the subsequent received data is not transferred to RDR.

[Clearing condition]

- When 0 is written to PER after reading PER = 1 (after writing 0 to it, read the PER bit to verify that its value is 0).

When the RE bit in SCR is set to 0 (serial reception is disabled), the PER flag is not affected and retains its previous value.

FER flag (Framing Error Flag)

The FER flag indicates that a framing error occurs during reception in asynchronous mode and the reception ends abnormally.

[Setting condition]

- When 0 is sampled as the stop bit during reception in asynchronous mode and the state of address match function is invalid (DCCR.DCME = 0).

  In 2-stop-bit mode, only the first stop bit is checked if it is 1 but the second stop bit is not checked. Although received data when the framing error occurs is transferred to RDR, no SCIn_RXI interrupt request occurs. In addition, when the FER flag is set to 1, the subsequent received data is not transferred to RDR.

[Clearing condition]

- When 0 is written to FER after reading FER = 1 (after writing 0 to it, read the FER bit to verify that its value is 0).

When the RE bit in SCR is set to 0, the FER flag is not affected and retains its previous value.

ORER flag (Overrun Error Flag)

The ORER flag indicates that an overrun error occurs during reception and the reception ends abnormally.

[Setting condition]

- When the next data is received before receive data is read from RDR that does not have a parity error and a framing error.

  In RDR, received data prior to an overrun error occurrence is retained, but data received after the overrun error occurrence is lost. When the ORER flag is set to 1, reception data is not forwarded to RDR register. In clock synchronous mode, serial transmission and reception are stopped.

[Clearing condition]

- When 0 is written to ORER after reading ORER = 1 (after writing 0 to it, read the ORER bit to verify that its value is 0).

When the RE bit in SCR is set to 0, the ORER flag is not affected and retains its previous value.

RDRF flag (Receive Data Full Flag)

The RDRF flag indicates the presence of received data in the RDR register.

[setting condition]

- When the reception ends normally, and receive data is forwarded from the RSR register to the RDR register.

[Clearing conditions]

- When it is set to 0 after 1 is read
- When data is read from the RDR register.

Note: Do not clear the RDRF flag by accessing the RDRF bit in SSR register unless communication is aborted.

TDRE flag (Transmit Data Empty Flag)

The TDRE flag indicates the presence of transmit data in the TDR register.

[setting conditions]

- When the SCR.TE bit is 0
- When data is transmitted from the TDR register to the TSR register.

[Clearing conditions]

- When it is set to 0 after 1 is read
- When the SCR.TE bit is 1, data is forwarded to the TDR register.

Note: Do not clear the TDRE flag by accessing the TDRE bit in SSR register unless communication is aborted.

27.2.14 Serial Status Register for Non-Smart Card Interface and FIFO Mode (SSR_FIFO) (SCMR.SMIF = 0 and FCR.FM = 1)

Address(es): SCI0.SSR_FIFO 4007 0004h

	b7	b6	b5	b4	b3	b2	b1	b0
	TDFE	RDF	ORER	FER	PER	TEND	—	DR
Value after reset:	1	0	0	0	0	0	x	0

Bit	Symbol	Bit name	Description	R/W
b0	DR	Receive Data Ready Flag	0: Receiving is in progress, or no received data remains in FRDRHL after a normal completion of received data (receive FIFO is empty) 1:The next received data is not received for a period after a normal completion of received data, and when the amount of data stored in the FIFO is equal to or less than the received triggering number.	R/W*1
b1	—	Reserved	The read value is undefined. The write value should be 1.	R/W
b2	TEND	Transmit End Flag	0: A character is transmitted 1: Character transfer is complete.	R/W*1
b3	PER	Parity Error Flag	0: No parity error occurred 1: A parity error occurred.	R/W*1
b4	FER	Framing Error Flag	0: No framing error occurred 1: A framing error occurred.	R/W*1
b5	ORER	Overrun Error Flag	0: No overrun error occurred 1: An overrun error occurred.	R/W*1
b6	RDF	Receive FIFO Data Full Flag	0: The amount of received data written in FRDRHL falls below the specified receive triggering number 1: The amount of received data written in FRDRHL is equal to or greater than the specified receive triggering number.	R/W*1
b7	TDFE	Transmit FIFO Data Empty Flag	0: The amount of transmit data written in FTDRHL exceeds the specified transmit triggering number 1: The amount of transmit data written in FTDRHL is equal to or less than the specified transmit triggering number.	R/W*1

Note 1. Only 0 can be written to clear the flag after reading 1.

The SSR_FIFO register provides SCI with FIFO mode status flags.

DR flag (Receive Data Ready Flag)

The DR flag indicates that the amount of data stored in the receive FIFO data register (FRDRHL) falls below the specified receive triggering number, and that no subsequent data is received yet after the elapse of 15 ETUs (Element Time Unit) from the last stop bit in asynchronous mode. This flag is valid only in asynchronous mode, including multi-processor mode, and when FIFO is selected.

In clock synchronous mode, this flag is not set to 1.

[Setting condition]

- DR is set to 1 when FRDRHL contains less data than the specified receive triggering number, and no subsequent data is received yet after the elapse of 15 ETUs*1 from the last stop bit and SSR_FIFO.FER and SSR_FIFO.PER flags are 0.

[Clearing conditions]

- When 1 is read from DR and 0 is written after all received data are read
- When the FCR.FM bit switches from 0 to 1.

Note 1. This is equivalent to one and a half (1.5) frames in the 8-bit format with one stop bit (ETU).
Only when FIFO is selected in asynchronous mode including multi-processor mode, the DR flag becomes 1 but not 1 in other operation modes.

TEND flag (Transmit End Flag)

The TEND flag indicates that FTDRHL does not contain valid data when transmitting the last bit of a serial character, therefore transmission is halted.

[Setting condition]

- TEND is set to 1 when FTDRHL does not contain transmit data when the last bit of a 1-byte serial character is transmitted.

[Clearing conditions]

- When transmit data is written in FTDRHL while the SCR.TE bit is 1
- When 0 is written in TEND after 1 is read from TEND while the SCR.TE bit is 1
- When the FCR.FM bit switches from 0 to 1.

PER flag (Parity Error Flag)

The PER flag indicates whether there is a parity error in the data read from the receive FIFO data register (FRDRHL) in asynchronous mode when the address match function is disabled (DCCR.DCME = 0).

[Setting condition]

- PER is set to 1 when data is received and a parity error is detected in the state of address match function that is disabled (DCCR.DCME = 0).

[Clearing condition]

- When 0 is written to PER after reading PER = 1.

The receive operation is continuous when received data is stored to the FRDRHL register even when a parity error occurs while data is received.

When the SCR.RE bit is cleared, the PER flag is not affected and the previous state is kept.

FER flag (Framing Error Flag)

The FER flag indicates whether there is a framing error in the data read from the receive FIFO data register (FRDRHL) in asynchronous mode and that the state of the address match function is disabled (DCCR.DCME = 0).

[Setting condition]

- FER is set to 1 when 0 is sampled as the stop bit during reception in the state of the address match function that is disabled (DCCR.DCME = 0).

[Clearing condition]

- When 0 is written to FER after reading FER = 1.

The receive operation is continuous when received data is stored to the FRDRHL register even when a framing error occurs while data is received.

When the SCR.RE bit is cleared, the FER flag is not affected and the previous state is kept.

ORER flag (Overrun Error Flag)

The ORER flag indicates that receive operation abnormally stops due to occurrence of an overrun error.

[Setting condition]

- ORER is set to 1 when the next serial reception completes while the receive FIFO is full of 16-byte received data.

[Clearing condition]

- When 0 is written after 1 is read from ORER.

Clearing the RE bit to 0 in the Serial Control Register (SCR) does not affect the ORER flag, which retains its previous state.

RDF flag (Receive FIFO Data Full Flag)

The RDF flag indicates that received data is transferred to the receive FIFO data register (FRDRHL), and the amount of data in FRDRHL equals or exceeds the specified receive triggering number. However, when RTRG is set to 0, the RDF flag is not set even when the amount of data in the receive FIFO is equal to 0.

[Setting condition]

- RDF is set to 1 when the amount of received data that is equal to or greater than the specified receive triggering number are stored in FRDRHL*1 and FIFO is not empty.

[Clearing conditions]

- After 1 is read from RDF and 0 is written
- When FRDRHL is read by the DTC but only when block transfer is the last transmission
- When the setting condition and clearing condition occur at the same time, the RDF flag is 0. After that, when the amount of data stored in FRDRHL register is the same or greater than the RTRG value, RDF is set to 1 after 1 PCLKB.

Note: Do not clear the RDF flag by accessing the RDF bit in SSR register before reading receive data unless communication is aborted.

Note 1. Because the FRDRHL is a 16-stage FIFO register, the maximum amount of data that can be read when RDF is 1 is equivalent to the specified receive triggering number. If an attempt is made to read after all the data in FRDRHL is read, the data is undefined.

TDFE flag (Transmit FIFO Data Empty Flag)

The TDFE flag indicates that data is transferred from the Transmit FIFO Data Register (FTDRHL) into the Transmit Shift Register (TSR), the amount of data in FTDRHL has fallen below the specified transmit triggering number, and writing of transmit data to FTDRHL is enabled.

[Setting conditions]

- TDFE is set to 1 when the TE bit in SCR is 0
- TDFE is set to 1 when the amount of transmit data written in FTDRHL is equal to or less than the specified transmit triggering number*1.

[Clearing conditions]

- When writing to FTDRHL is executed on the last transmission while the DTC is activated
- When 0 is written in the TDFE flag after reading TDFE = 1.
  The setting conditions is given priority at TE = 0. When the setting condition and clearing condition occur at the same time, the TDFE flag is 0. Thereafter, when the amount of data stored in the FTDRHL register is the same as or greater than the TTRG value, TDFE is set to 1 after 1 PCLKB.

Note: Do not clear the TDFE flag by accessing the TDFE bit in the SSR register before writing transmit data unless communication is aborted.

Note 1. Because the FTDRHL register is a 16-stage FIFO register, the maximum amount of data that can be written when the TDFE flag is set to 1 is indicated in "16 - FDR.T[4:0]". If more data is written, data is discarded.

27.2.15 Serial Status Register for Smart Card Interface Mode (SSR_SMCI) (SCMR.SMIF = 1)

Address(es): SCI0.SSR_SMCI 4007 0004h, SCI1.SSR_SMCI 4007 0024h, SCI9.SSR_SMCI 4007 0124h

	b7	b6	b5	b4	b3	b2	b1	b0
	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT
Value after reset:	1	0	0	0	0	1	0	0

Bit	Symbol	Bit name	Description	R/W
b0	MPBT	Multi-Processor Bit Transfer	This bit should be 0 in smart card interface mode	R/W
b1	MPB	Multi-Processor	This bit should be 0 in smart card interface mode	R
b2	TEND	Transmit End Flag	0: A character is being transmitted 1: Character transfer is complete.	R
b3	PER	Parity Error Flag	0: No parity error occurred 1: A parity error occurred.	R/W*1
b4	ERS	Error Signal Status Flag	0: Low error signal not responded 1: Low error signal responded.	R/W*1
b5	ORER	Overrun Error Flag	0: No overrun error occurred 1: An overrun error occurred.	R/W*1
b6	RDRF	Receive Data Full Flag	0: No received data is in RDR register 1: Received data is in RDR register.	R/W*1
b7	TDRE	Transmit Data Empty Flag	0: Transmit data is in TDR register 1: No transmit data is in TDR register.	R/W*1

Note 1. Only 0 can be written to clear the flag after reading 1.

The SSR_SMCI register provides SCI with smart card interface mode status flags.

TEND flag (Transmit End Flag)

With no error signal from the receiving side, the TEND flag is set to 1 when additional transfer data is ready to be transferred to the TDR register.

[Setting conditions]

- When the SCR_SMCI.TE bit = 0 (serial transmission is disabled).

  When the SCR_SMCI.TE bit changes from 0 to 1, the TEND flag is not affected and retains the value 1.
- When a specified period has elapsed after the latest transmission of 1 byte, the ERS flag is 0, and the TDR register is not updated.

  The set timing is determined by register settings as follows:
  - When SMR_SMCI.GM = 0 and SMR_SMCI.BLK = 0, 12.5 ETU after the start of transmission
  - When SMR_SMCI.GM = 0 and SMR_SMCI.BLK = 1, 11.5 ETU after the start of transmission
  - When SMR_SMCI.GM = 1 and SMR_SMCI.BLK = 0, 11.0 ETU after the start of transmission
  - When SMR_SMCI.GM = 1 and SMR_SMCI.BLK = 1, 11.0 ETU after the start of transmission.

[Clearing conditions]

- When transmit data is written to the TDR register while the SCR_SMCI.TE bit is 1
- When 0 is written to TDRE after reading TDRE = 1 while the SCR_SMCI.TE bit is 1.

PER flag (Parity Error Flag)

The PER flag indicates that a parity error occurred during reception in asynchronous mode and the reception ends

abnormally.

[Setting condition]

- When a parity error is detected during reception.

  Although received data when the parity error occurs is transferred to RDR, no SCIn_RXI interrupt request occurs. When the PER flag is set to 1, the subsequent receive data is not transferred to RDR.

[Clearing condition]

- When 0 is written to PER after reading PER = 1. After writing 0 to the PER flag, read it to verify that its value is 0.

When the RE bit in SCR_SMCI is set to 0 (serial reception is disabled), the PER flag is not affected and retains its previous value.

ERS flag (Error Signal Status Flag)

[Setting condition]

- When a low error signal is sampled.

[Clearing condition]

- When 0 is written to ERS after reading ERS = 1.

ORER flag (Overrun Error Flag)

The ORER flag indicates that an overrun error occurred during reception and the reception ends abnormally.

[Setting condition]

- When the next data is received before received data is read from RDR that does not have a parity error. In RDR, the data received before an overrun error occurred is saved, but data received after the error is lost.

[Clearing condition]

- When 0 is written to ORER after reading ORER = 1. After writing 0 to the ORER flag, read it to verify that its value is 0).

When the RE bit in SCR_SMCI is set to 0, the ORER flag is not affected and retains its previous value.

RDRF flag (Receive Data Full Flag)

The RDRF flag indicates the presence of received data in the RDR register.

[setting condition]

- When the reception ends normally, and received data is forwarded from the RSR register to the RDR register.

[Clearing conditions]

- When it is set to 0 after 1 is read
- When data is read from the RDR register.

Note: Do not clear the RDRF flags by accessing the RDRF bit in the SSR register unless communication is aborted.

TDRE flag (Transmit Data Empty Flag)

The TDRE flag indicates the presence of transmit data in the TDR register.

[setting conditions]

- When the SCR_SMCI.TE bit is 0
- When data is transmitted from the TDR register to the TSR register.

[Clearing conditions]

- When it is set to 0 after 1 is read
- When the SCR_SMCI.TE bit is 1 and it forwards data to the TDR register.

Note: Do not clear the TDRE flags by accessing the TDRE bit in the SSR register unless communication is aborted.

27.2.16 Smart Card Mode Register (SCMR)

Address(es): SCI0.SCMR 4007 0006h, SCI1.SCMR 4007 0026h, SCI9.SCMR 4007 0126h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCP2	—	—	CHR1	SDIR	SINV	—	SMIF
Value after reset:	1	1	1	1	0	0	1	0

Bit	Symbol	Bit name	Description	R/W
b0	SMIF	Smart Card Interface Mode Select	0: Non-smart card interface mode (asynchronous mode, clock synchronous mode, simple SPI mode, or simple IIC mode) 1: Smart card interface mode.	R/W*1
b1	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b2	SINV	Transmitted/Received Data Invert	0: TDR contents are transmitted as they are. Received data is stored as received in the RDR. 1: TDR contents are inverted before being transmitted. Received data is stored in inverted form in the RDR. This bit can be used in the following modes: • Smart card interface mode • Asynchronous mode (multi-processor mode) • Clock synchronous mode • Simple SPI mode. Set this bit to 0 if operation is in simple IIC mode.	R/W*1
b3	SDIR	Transmitted/Received Data Transfer Direction	0: Transfer with LSB first 1: Transfer with MSB first. This bit can be used in the following modes: • Smart card interface mode • Asynchronous mode (multi-processor mode) • Clock synchronous mode • Simple SPI mode. Set this bit to 1 if operation is in simple IIC mode.	R/W*1
b4	CHR1	Character Length 1	Only valid in asynchronous mode*2. Selects in combination with the CHR bit in SMR. CHR1 CHR 0 0: Transmit/receive in 9-bit data length 0 1: Transmit/receive in 9-bit data length 1 0: Transmit/receive in 8-bit data length (initial value) 1 1: Transmit/receive in 7-bit data length*3.	R/W*1
b6, b5	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b7	BCP2	Base Clock Pulse 2	Selects the number of base clock cycles in combination with the SMR_SMCI.BCP[1:0] bits. Table 27.4 lists the combinations of the SCMR.BCP2 bit and SMR_SMCI.BCP[1:0] bits.	R/W*1

Note 1. Writable only when TE in SCR/SCR_SMCI = 0 and RE in SCR/SCR_SMCI = 0 (both serial transmission and reception are disabled).
Note 2. The setting is invalid and a fixed data length of 8 bits is used in modes other than asynchronous mode.
Note 3. LSB-first should be selected and the value of MSB bit [7] in TDR cannot be transmitted.

The SCMR register selects the smart card interface and communication format.

SMIF bit (Smart Card Interface Mode Select)

Setting the SMIF bit to 1 selects the smart card interface mode. Setting it to 0 selects all other modes:

- Asynchronous mode, including multi-processor mode
- Clock synchronous mode
- Simple SPI mode

- Simple IIC mode.

SINV bit (Transmitted/Received Data Invert)

The SINV bit inverts the transmit/receive data logic level. This bit does not affect the logic level of the parity bit. To invert the parity bit, invert the PM bit in SMR or SMR_SMCI.

CHR1 bit (Character Length 1)

The CHR1 bit selects the data length of transmit/receive data in combination with the CHR bit in SMR.

A fixed data length of 8 bits is used in modes other than asynchronous mode.

BCP2 bit (Base Clock Pulse 2)

The BCP2 bit selects the number of base clock cycles in a 1-bit data transfer time in smart card interface mode. Set this bit in combination with the SMR_SMCI.BCP[1:0] bits.

Table 27.4 Combinations of SCMR.BCP2 bit and SMR_SMCI.BCP[1:0] bits

SCMR.BCP2 bit	SMR_SMCI.BCP[1:0] bits		Number of base clock cycles for 1-bit transfer period
0	0	0	93 clock cycles (S = 93)*1
0	0	1	128 clock cycles (S = 128)*1
0	1	0	186 clock cycles (S = 186)*1
0	1	1	512 clock cycles (S = 512)*1
1	0	0	32 clock cycles (S = 32)*1 (Initial Value)
1	0	1	64 clock cycles (S = 64)*1
1	1	0	372 clock cycles (S = 372)*1
1	1	1	256 clock cycles (S = 256)*1

Note 1. S is the value of S in the Bit Rate Register (BRR), see section 27.2.17, Bit Rate Register (BRR).

27.2.17 Bit Rate Register (BRR)

Address(es): SCI0.BRR 4007 0001h, SCI1.BRR 4007 0021h, SCI9.BRR 4007 0121h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

BRR is an 8-bit register that adjusts the bit rate.

As each SCI channel has independent baud rate generator control, different bit rates can be set for each. Table 27.5 shows the relationship between the setting (N) in the BRR and the bit rate (B) for asynchronous mode, multiprocessor transfer, clock synchronous mode, smart card interface mode, simple SPI mode, and simple IIC mode.

The initial value of BRR is FFh. BRR can be read by the CPU, but can only be written to when the TE and RE bits in SCR/SCR_SMCI are 0.

Table 27.5 Relationship between N setting in BRR and bit rate B

Mode	SEMR settings			BRR setting	Error
	BGDM bit	ABCS bit	ABCSE bit		
Asynchronous, multi-processor transfer	0	0	0	$N = \frac{PCLKB \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \{ \frac{PCLKB \times 10^6}{B \times 64 \times 2^{2n-1} \times (N + 1)} - 1 \} \times 100$
	1	0	0	$N = \frac{PCLKB \times 10^6}{32 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \{ \frac{PCLKB \times 10^6}{B \times 32 \times 2^{2n-1} \times (N + 1)} - 1 \} \times 100$
	0	1	0		
	1	1	0	$N = \frac{PCLKB \times 10^6}{16 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \{ \frac{PCLKB \times 10^6}{B \times 16 \times 2^{2n-1} \times (N + 1)} - 1 \} \times 100$
	Don't care	Don't care	1	$N = \frac{PCLKB \times 10^6}{12 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \{ \frac{PCLKB \times 10^6}{B \times 12 \times 2^{2n-1} \times (N + 1)} - 1 \} \times 100$
Clock synchronous, simple SPI				$N = \frac{PCLKB \times 10^6}{8 \times 2^{2n-1} \times B} - 1$	
Smart card interface				$N = \frac{PCLKB \times 10^6}{S \times 2^{2n+1} \times B} - 1$	$Error\ (\%) = \{ \frac{PCLKB \times 10^6}{B \times S \times 2^{2n+1} \times (N + 1)} -1 \} \times 100$
Simple IIC*1				$N = \frac{PCLKB \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	

B: Bit rate (bps).
N: BRR setting for on-chip baud rate generator ($0 \leq N \leq 255$).
PCLKB: Operating frequency (MHz).
n and S: Determined by the settings of the SMR/SMR_SMCI and SCMR registers as listed in Table 27.7 and Table 27.8.

Note 1. Adjust the bit rate so that the widths at high and low level of the SCLn output in simple IIC mode satisfy the I^2C standard.

Table 27.6 Calculating widths at high and low level for SCL

Mode	SCL	Formula (result in seconds)
IIC	Width at high level (minimum value)	$(N+1) \times 4 \times 2^{2n-1} \times 7 \times \frac{1}{PCLKB \times 10^6}$
	Width at low level (minimum value)	$(N+1) \times 4 \times 2^{2n-1} \times 8 \times \frac{1}{PCLKB \times 10^6}$

Table 27.7 Clock source settings

SMR or SMR_SMCI.CKS[1:0] bit setting		
CKS[1:0] bits	**Clock source**	**n**
0 0	PCLKB clock	0
0 1	PCLKB/4 clock	1
1 0	PCLKB/16 clock	2
1 1	PCLKB/64 clock	3

Table 27.8 Base clock settings in smart card interface mode

SCMR.BCP2 bit setting	SMR_SMCI.BCP[1:0] bit setting		
BCP2 bit	**BCP[1:0] bits**	**Base clock cycles for 1-bit period**	**S**
0	0 0	93 clock cycles	93
0	0 1	128 clock cycles	128
0	1 0	186 clock cycles	186
0	1 1	512 clock cycles	512
1	0 0	32 clock cycles	32
1	0 1	64 clock cycles	64
1	1 0	372 clock cycles	372
1	1 1	256 clock cycles	256

Table 27.9 and Table 27.10 list examples of BRR (N) settings in asynchronous mode. Table 27.11 lists the maximum bit rate selectable for each operating frequency. Table 27.15 lists examples of BRR (N) settings in smart card interface mode. Table 27.17 lists examples of BRR (N) settings in simple IIC mode.

In smart card interface mode, the number of base clock cycles S in a 1-bit data transfer time can be selected. For details, see section 27.6.4, Receive Data Sampling Timing and Reception Margin. Table 27.12 and Table 27.14 list the maximum bit rates with external clock input.

When either the asynchronous mode base clock select bit (ABCS) or the baud rate generator double-speed mode select bit (BGDM) in the Serial Extended Mode Register (SEMR) is set to 1 in asynchronous mode, the bit rate becomes twice that listed in Table 27.16. When both of those registers are set to 1, the bit rate becomes four times the listed value.

Table 27.9 Examples of BRR settings for different bit rates in asynchronous mode (1)

Bit rate (bps)	Operating frequency PCLKB (MHz)														
	8			9.8304			10			12			12.288		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	141	0.03	2	174	-0.26	2	177	-0.25	2	212	0.03	2	217	0.08
150	2	103	0.16	2	127	0.00	2	129	0.16	2	155	0.16	2	159	0.00
300	1	207	0.16	1	255	0.00	2	64	0.16	2	77	0.16	2	79	0.00
600	1	103	0.16	1	127	0.00	1	129	0.16	1	155	0.16	1	159	0.00
1200	0	207	0.16	0	255	0.00	1	64	0.16	1	77	0.16	1	79	0.00
2400	0	103	0.16	0	127	0.00	0	129	0.16	0	155	0.16	0	159	0.00
4800	0	51	0.16	0	63	0.00	0	64	0.16	0	77	0.16	0	79	0.00
9600	0	25	0.16	0	31	0.00	0	32	-1.36	0	38	0.16	0	39	0.00
19200	0	12	0.16	0	15	0.00	0	15	1.73	0	19	-2.34	0	19	0.00
31250	0	7	0.00	0	9	-1.70	0	9	0.00	0	11	0.00	0	11	2.40
38400	—	—	—	0	7	0.00	0	7	1.73	0	9	-2.34	0	9	0.00

Bit rate (bps)	Operating frequency PCLKB (MHz)														
	14			16			17.2032			18			19.6608		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	248	-0.17	3	70	0.03	3	75	0.48	3	79	-0.12	3	86	0.31
150	2	181	0.16	2	207	0.16	2	223	0.00	2	233	0.16	2	255	0.00
300	2	90	0.16	2	103	0.16	2	111	0.00	2	116	0.16	2	127	0.00
600	1	181	0.16	1	207	0.16	1	223	0.00	1	233	0.16	1	255	0.00
1200	1	90	0.16	1	103	0.16	1	111	0.00	1	116	0.16	1	127	0.00
2400	0	181	0.16	0	207	0.16	0	223	0.00	0	233	0.16	0	255	0.00
4800	0	90	0.16	0	103	0.16	0	111	0.00	0	116	0.16	0	127	0.00

Bit rate (bps)	Operating frequency PCLKB (MHz)														
	14			16			17.2032			18			19.6608		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	45	-0.93	0	51	0.16	0	55	0.00	0	58	-0.69	0	63	0.00
19200	0	22	-0.93	0	25	0.16	0	27	0.00	0	28	1.02	0	31	0.00
31250	0	13	0.00	0	15	0.00	0	16	1.20	0	17	0.00	0	19	-1.70
38400	—	—	—	0	12	0.16	0	13	0.00	0	14	-2.34	0	15	0.00

Note: In this example, SEMR.ABCS = 0, SEMR.ABCSE = 0, and SEMR.BGDM = 0. When either ABCS bit or BGDM bit is set to 1, the bit rate doubles. When both ABCS = 1 and BGDM = 1, the bit rate increases four times.

Table 27.10 Examples of BRR settings for various bit rates in asynchronous mode (2)

Bit rate (bps)	Operating frequency PCLKB (MHz)		
	20		
	n	N	Error (%)
110	3	88	-0.25
150	3	64	0.16
300	2	129	0.16
600	2	64	0.16
1200	1	129	0.16
2400	1	64	0.16
4800	0	129	0.16
9600	0	64	0.16
19200	0	32	-1.36
31250	0	19	0.00
38400	0	15	1.73

Note: In this example, SEMR.ABCS = 0, SEMR.ABCSE = 0, and SEMR.BGDM = 0. When either ABCS bit or BGDM bit is set to 1, the bit rate doubles. When both ABCS = 1 and BGDM = 1, the bit rate increases four times.

Table 27.11 Maximum bit rate for each operating frequency in asynchronous mode (1 of 2)

PCLKB (MHz)	SEMR settings					Maximum bit rate (bps)	PCLKB (MHz)	SEMR settings					Maximum bit rate (bps)
	BGDM bit	ABCS bit	ABCSE bit	n	N			BGDM bit	ABCS bit	ABCSE bit	n	N	
8	0	0	0	0	0	250000	17.2032	0	0	0	0	0	537600
		1	0	0	0	500000			1	0	0	0	1075200
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1000000			1	0	0	0	2150400
	Don't care	Don't care	1	0	0	1333333		Don't care	Don't care	1	0	0	2867200
9.8304	0	0	0	0	0	307200	18	0	0	0	0	0	562500
		1	0	0	0	614400			1	0	0	0	1125000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1228800			1	0	0	0	2250000
	Don't care	Don't care	1	0	0	1638400		Don't care	Don't care	1	0	0	3000000

Table 27.11 Maximum bit rate for each operating frequency in asynchronous mode (2 of 2)

PCLKB (MHz)	SEMR settings BGDM bit	ABCS bit	ABCSE bit	n	N	Maximum bit rate (bps)	PCLKB (MHz)	SEMR settings BGDM bit	ABCS bit	ABCSE bit	n	N	Maximum bit rate (bps)
10	0	0	0	0	0	312500	19.6608	0	0	0	0	0	614400
		1	0	0	0	625000			1	0	0	0	1228800
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1250000			1	0	0	0	2457600
	Don't care	Don't care	1	0	0	1666666		Don't care	Don't care	1	0	0	3276800
12	0	0	0	0	0	375000	20	0	0	0	0	0	625000
		1	0	0	0	750000			1	0	0	0	1250000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1500000			1	0	0	0	2500000
	Don't care	Don't care	1	0	0	2000000		Don't care	Don't care	1	0	0	3333333
12.288	0	0	0	0	0	384000							
		1	0	0	0	768000							
	1	0	0	0	0								
		1	0	0	0	1536000							
	Don't care	Don't care	1	0	0	2048000							
14	0	0	0	0	0	437500							
		1	0	0	0	875000							
	1	0	0	0	0								
		1	0	0	0	1750000							
	Don't care	Don't care	1	0	0	2333333							
16	0	0	0	0	0	500000							
		1	0	0	0	1000000							
	1	0	0	0	0								
		1	0	0	0	2000000							
	Don't care	Don't care	1	0	0	2666666							

Table 27.12 Maximum bit rate with external clock input in asynchronous mode

PCLKB (MHz)	External input clock (MHz)	Maximum bit rate (bps) SEMR.ABCS bit = 0	SEMR.ABCS bit = 1
8	2.0000	125000	250000
9.8304	2.4576	153600	307200
10	2.5000	156250	312500
12	3.0000	187500	375000
12.288	3.0720	192000	384000
14	3.5000	218750	437500
16	4.0000	250000	500000
17.2032	4.3008	268800	537600
18	4.5000	281250	562500
19.6608	4.9152	307200	614400
20	5.0000	312500	625000

Table 27.13 BRR settings for different bit rates in clock synchronous and simple SPI modes

	Operating Frequency PCLKB (MHz)							
	8		10		16		20	
Bit rate (bps)	n	N	n	N	n	N	n	N
110								
250	3	124	—	—	3	249		
500	2	249	—	—	3	124	—	—
1 k	2	124	—	—	2	249	—	—
2.5 k	1	199	1	249	2	99	2	124
5 k	1	99	1	124	1	199	1	249
10 k	0	199	0	249	1	99	1	124
25 k	0	79	0	99	0	159	0	199
50 k	0	39	0	49	0	79	0	99
100 k	0	19	0	24	0	39	0	49
250 k	0	7	0	9	0	15	0	19
500 k	0	3	0	4	0	7	0	9
1 M	0	1			0	3	0	4
2.5 M			0	0*1			0	1
5 M							0	0*1
7.5 M								

Space: Setting prohibited.
—: Can be set, but an error occurs.

Note 1. Continuous transmission or reception is impossible. After transmitting or receiving one frame of data, a 1-bit period elapses before starting transmitting or receiving the next frame of data. The output of the synchronization clock stops for a 1-bit period. For this reason, it takes 9 bits worth of time to transfer one frame (8 bits) of data, and the average transfer rate is 8/9 times the bit rate.

Table 27.14 Maximum bit rate with external clock input in clock synchronous and simple SPI modes

PCLKB (MHz)	External input clock (MHz)	Maximum bit rate (Mbps)
8	1.3333	1.3333333
10	1.6667	1.6666667
12	2.0000	2.0000000
14	2.3333	2.3333333
16	2.6667	2.6666667
18	3.0000	3.0000000
20	3.3333	3.3333333

Table 27.15 BRR settings for different bit rates in smart card interface mode, n = 0, S = 372

	Operating frequency PCLKB (MHz)											
	7.1424			10.00			10.7136			13.00		
bit rate (bps)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	0	0.00	0	1	-30	0	1	-25	0	1	-8.99

	Operating frequency PCLKB (MHz)											
	14.2848			16.00			18.00			20.00		
bit rate (bps)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	1	0.00	0	1	12.01	0	2	-15.99	0	2	-6.66

Table 27.16 Maximum bit rate for each operating frequency in smart card interface mode, S = 32

PCLKB (MHz)	Maximum bit rate (bps)	n	N
10.00	156250	0	0
10.7136	167400	0	0
13.00	203125	0	0
16.00	250000	0	0
18.00	281250	0	0
20.00	312500	0	0

Table 27.17 BRR settings for different bit rates in simple IIC mode

	Operating frequency PCLKB (MHz)								
	8			10			16		
Bit rate (bps)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
10 k	0	24	0.0	0	30	0.8	1	12	-3.8
25 k	0	9	0.0	0	12	-3.8	1	4	0.0
50 k	0	4	0.0	0	5	4.2	1	2	-16.7
100 k*1	0	2	-16.7	0	3	-21.9	0	4	0.0
250 k	0	0	0.0	0	0	25	0	1	0.0
350 k	—	—	—	—	—	—	—	—	—
400 k*1	—	—	—	—	—	—	—	—	—

	Operating frequency PCLKB (MHz)		
	20		
Bit rate (bps)	n	N	Error (%)
10 k	1	15	-2.3
25 k	1	5	4.2
50 k	1	2	4.2
100 k*1	0	6	-10.7
250 k	0	2	-16.7
350 k	0	1	-10.7
400 k*1	0	1	-21.9

Note 1. The bit rate of 100 kbps and 400 kbps indicates the set value at which the error is on the minus side.
Note 2. The minimum value of low width is smaller than 1.3 us which is the standard value of fast mode.

Table 27.18 Minimum widths at high and low level for SCL at different bit rates in simple IIC mode

	Operating frequency PCLKB (MHz)								
	8			10			16		
Bit rate (bps)	n	N	Min. Widths at High/Low Level for SCL (μs)	n	N	Min. Widths at High/Low Level for SCL (μs)	n	N	Min. Widths at High/Low Level for SCL (μs)
10 k	0	24	43.75/50.00	0	30	43.40/49.60	1	12	45.5/52.00
25 k	0	9	17.50/20.00	0	12	18.2/20.80	1	4	17.50/20.00
50 k	0	4	8.75/10.00	0	5	8.40/9.60	1	2	10.50/12.00
100 k	0	2	5.25/6.00	0	3	5.60/6.40	0	4	4.38/5.00
250 k	0	0	1.75/2.00	0	0	1.40/1.60	0	1	1.75/2.00
350 k	—	—	—	—	—	—	—	—	—
400 k	—	—	—	—	—	—	—	—	—

Bit rate (bps)	Operating frequency PCLKB (MHz)		
	20		
	n	N	Min. Widths at High/Low Level for SSL (μs)
10 k	1	15	44.80/51.20
25 k	1	5	16.80/19.20
50 k	1	2	8.40/9.60
100 k	0	6	4.90/5.60
250 k	0	2	2.10/2.40
350 k	0	1	1.40/1.60
400 k	0	1	1.40/1.60

Note 1. The minimum value of low width is smaller than 1.3 us which is the standard value of fast mode. The setting values are the same as in Table 27.17.

27.2.18 .Modulation Duty Register (MDDR)

Address(es): SCI0.MDDR 4007 0012h, SCI1.MDDR 4007 0032h, SCI9.MDDR 4007 0132h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

MDDR corrects the bit rate adjusted by the BRR register.

When the BRME bit in SEMR is set to 1, the bit rate generated by the on-chip baud rate generator is evenly corrected according to the settings of MDDR (M/256). Table 27.19 lists the relationship between the MDDR setting (M) and the bit rate (B).

The initial value of MDDR is FFh. Bit [7] in this register is fixed to 1.

The CPU can read the MDDR register, but this register is only writable when the TE and RE bits in SCR/SCR_SMCI are 0.

Table 27.19 Relationship between MDDR setting (M) and bit rate (B) when bit rate modulation function is used

Mode	SEMR settings			BRR setting	Error
	BGDM bit	ABCS bit	ABCSE bit		
Asynchronous, multi-processor transfer	0	0	0	$N = \frac{PCLKB \times 10^6}{64 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error\ (\%) = \{ \frac{PCLKB \times 10^6}{B \times 64 \times 2^{2n-1} \times (256/M) \times (N + 1)} - 1 \} \times 100$
	1	0	0	$N = \frac{PCLKB \times 10^6}{32 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error\ (\%) = \{ \frac{PCLKB \times 10^6}{B \times 32 \times 2^{2n-1} \times (256/M) \times (N + 1)} - 1 \} \times 100$
	0	1	0		
	1	1	0	$N = \frac{PCLKB \times 10^6}{16 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error\ (\%) = \{ \frac{PCLKB \times 10^6}{B \times 16 \times 2^{2n-1} \times (256/M) \times (N + 1)} - 1 \} \times 100$
	Don't care	Don't care	1	$N = \frac{PCLKB \times 10^6}{12 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error\ (\%) = \{ \frac{PCLKB \times 10^6}{B \times 12 \times 2^{2n-1} \times (256/M) \times (N + 1)} - 1 \} \times 100$
Clock synchronous, simple SPI*1				$N = \frac{PCLKB \times 10^6}{8 \times 2^{2n-1} \times (256/M) \times B} - 1$	

Table 27.19 Relationship between MDDR setting (M) and bit rate (B) when bit rate modulation function is used

Mode	SEMR settings			BRR setting	Error
	BGDM bit	ABCS bit	ABCSE bit		
Smart card interface				$N = \frac{PCLKB \times 10^6}{S \times 2^{2n+1} \times (256/M) \times B} - 1$	$Error\ (\%) = \{ \frac{PCLKB \times 10^6}{B \times S \times 2^{2n+1} \times (256/M) \times (N + 1)} - 1 \} \times 100$
Simple IIC*2				$N = \frac{PCLKB \times 10^6}{64 \times 2^{2n-1} \times (256/M) \times B} - 1$	

B: Bit rate (bps).
M: MDDR setting (128 ≤ MDDR ≤ 255).
N: BRR setting for baud rate generator (0 ≤ N ≤ 255).
PCLKB: Operating frequency (MHz).
n and S: Determined by the settings of the SMR/SMR_SMCI and SCMR registers as listed in Table 27.8 and Table 27.9.
Bit Rate Register (BRR).

Note 1. Do not use this function in clock synchronous mode and in the highest speed settings in simple SPI mode (SMR.CKS[1:0] = 00b, SCR.CKE[1] = 0, and BRR = 0).
Note 2. Adjust the bit rate so that the widths at high and low level of the SCLn output in simple IIC mode satisfy the I^2C standard.

Table 27.20 and Table 27.21 list examples of N settings in BRR and M settings in MDDR in asynchronous mode.

Table 27.20 Examples of BRR and MDDR settings for different bit rates in asynchronous mode (1)

Bit rate (bps)	Operating frequency PCLKB (MHz)														
	8					9.8304					10				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	5	236	0	0.03	0	7	(256)*1	0	0.00	0	10	173	1	-0.01
57600	0	3	236	0	0.03	0	4	240	0	0.00	0	4	236	0	0.03
115200	0	1	236	0	0.03	0	1	192	0	0.00	0	4	236	1	0.03
230400	0	0	236	0	0.03	0	0	192	0	0.00	0	1	189	1	0.14
460800	0	0	236	1	0.03	0	0	192	1	0.00	0	0	189	1	0.14

Bit rate (bps)	Operating frequency PCLKB (MHz)														
	12					12.288					14				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	8	236	0	0.03	0	9	(256)*1	0	0.00	0	16	191	1	0.00
57600	0	5	236	0	0.03	0	4	192	0	0.00	0	13	236	1	0.03
115200	0	2	236	0	0.03	0	4	192	1	0.00	0	6	236	1	0.03
230400	0	2	236	1	0.03	0	2	230	1	-0.17	0	2	202	1	-0.11
460800	0	0	157	1	-0.18	0	0	154	1	0.26	0	0	135	1	0.14

Bit rate (bps)	Operating frequency PCLKB (MHz)														
	16					17.2032					18				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	11	236	0	0.03	0	13	(256)*1	0	0.00	0	18	166	1	-0.01
57600	0	7	236	0	0.03	0	6	192	0	0.00	0	18	249	1	-0.01
115200	0	3	236	0	0.03	0	6	192	1	0.00	0	8	236	1	0.03
230400	0	1	236	0	0.03	0	3	219	1	-0.20	0	1	210	0	0.14
460800	0	1	236	1	0.03	0	1	219	1	-0.20	0	0	210	0	0.14

Note 1. In this example, the ABCS and ABCSE in SEMR are 0. SEMR.BRME = 0 (M = 256) disables the bit rate modulation function.

Table 27.21 Examples of BRR and MDDR settings for different bit rates in asynchronous mode (2)

	Operating frequency PCLKB (MHz)									
	19.6608					20				
Bit Rate (bps)	n	N	M	BGDMbit	Error (%)	n	N	M	BGDMbit	Error (%)
38400	0	15	(256)*1	0	0.00	0	10	173	0	-0.01
57600	0	9	240	0	0.00	0	9	236	0	0.03
115200	0	4	240	0	0.00	0	4	236	0	0.03
230400	0	1	192	0	0.00	0	4	236	1	0.03
460800	0	0	192	0	0.00	0	0	189	0	0.14

Note 1. In this example, the ABCS and ABCSE in SEMR are 0. SEMR.BRME = 0 (M = 256) disables the bit rate modulation function.

27.2.19 Serial Extended Mode Register (SEMR)

Address(es): SCI0.SEMR 4007 0007h, SCI1.SEMR 4007 0027h, SCI9.SEMR 4007 0127h

	b7	b6	b5	b4	b3	b2	b1	b0
	RXDESEL	BGDM	NFEN	ABCS	ABCSE	BRME	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0, b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b2	BRME	Bit Rate Modulation Enable	0: Bit rate modulation function is disabled 1: Bit rate modulation function is enabled.	R/W*1
b3	ABCSE	Asynchronous Mode Extended Base Clock Select 1	Valid only in asynchronous mode and SCR.CKE[1] = 0: 0: Clock cycles for 1-bit period is decided with a combination between BGDM and ABCS in SEMR 1: Baud rate is 6 base clock cycles for 1-bit period.	R/W*1
b4	ABCS	Asynchronous Mode Base Clock Select	Valid only in asynchronous mode: 0: Selects 16 base clock cycles for 1-bit period 1: Selects 8 base clock cycles for 1-bit period.	R/W*1
b5	NFEN	Digital Noise Filter Function Enable	In asynchronous mode: 0: Noise cancellation function for the RXDn input signal is disabled 1: Noise cancellation function for the RXDn input signal is enabled. In simple IIC mode: 0: Noise cancellation function for the SCLn and SDAn input signals is disabled 1: Noise cancellation function for the SCLn and SDAn input signals is enabled. The NFEN bit should be 0 in any mode other than above.	R/W*1
b6	BGDM	Baud Rate Generator Double-Speed Mode Select	Valid only in asynchronous mode and SCR.CKE[1] = 0: 0: Baud rate generator outputs the clock with basic frequency 1: Baud rate generator outputs the clock with doubled frequency.	R/W*1
b7	RXDESEL	Asynchronous Start Bit Edge Detection Select	Valid only in asynchronous mode: 0: The low level on the RXDn pin is detected as the start bit 1: A falling edge on the RXDn pin is detected as the start bit.	R/W*1

Note 1. Writable only when TE in SCR/SCR_SMCI = 0 and RE in SCR/SCR_SMCI = 0 (both serial transmission and reception are disabled).

SEMR selects the clock source for 1-bit period in asynchronous mode.

BRME bit (Bit Rate Modulation Enable)

The BRME bit enables or disables the bit rate modulation function. The bit rate generated by the on-chip baud rate

generator is evenly corrected when this function is enabled.

ABCSE bit (Asynchronous Mode Extended Base Clock Select 1)

The pulse number for a base clock at 1-bit period is 6 and the double-frequency clock is output from the baud rate generator. When the bit rate is set to 6 while dividing the bus clock frequency, use this bit and set SMR.CKS[1:0] to 00b and BRR to 0. Set this bit to 0 except in asynchronous mode.

ABCS bit (Asynchronous Mode Base Clock Select)

The ABCS bit selects the clock cycles for 1-bit period. Set this bit to 0 except in asynchronous mode.

NFEN bit (Digital Noise Filter Function Enable)

The NFEN bit enables or disables the digital noise filter function.

When the function is enabled, noise cancellation is applied to the RXDn input signal in asynchronous mode, and noise cancellation is applied to the SDAn and SCLn input signals in simple IIC mode. In any mode other those specified, set the NFEN bit to 0 to disable the digital noise filter function. When the function is disabled, input signals are transferred as received, and as internal signals.

BGDM bit (Baud Rate Generator Double-Speed Mode Select)

The BGDM bit selects the cycle of output clock for the baud rate generator.

This bit is valid when the on-chip baud rate generator is selected as the clock source (SCR.CKE[1] = 0) in asynchronous mode (SMR.CM = 0). For the clock output from the baud rate generator, either single or doubled frequency can be selected. The base clock is generated by the clock output from the baud rate generator. When the BGDM bit is set to 1, the base clock cycle is halved and the bit rate is doubled.

Set this bit to 0 in modes other than asynchronous mode.

RXDESEL bit (Asynchronous Start Bit Edge Detection Select)

The RXDESEL bit selects the detection method of the start bit for reception in asynchronous mode. When a break occurs, data receiving operation depends on the settings of this bit. Set this bit to 1 when reception must be stopped while a break occurs or when reception must be started without retaining the RXDn pin input at high level for the period of one data frame or longer after completion of the break.

Set this bit to 0 in modes other than asynchronous mode.

27.2.20 Noise Filter Setting Register (SNFR)

Address(es): SCI0.SNFR 4007 0008h, SCI1.SNFR 4007 0028h, SCI9.SNFR 4007 0128h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	NFCS[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	NFCS[2:0]	Noise Filter Clock Select	In asynchronous mode, the standard setting for the base clock is as follows: b2 b0 0 0 0: The clock signal divided by 1 is used with the noise filter. In simple IIC mode, the standard settings for the clock source of the on-chip baud rate generator selected by the SMR.CKS[1:0] bits are given as follows: b2 b0 0 0 1: The clock signal divided by 1 is used with the noise filter 0 1 0: The clock signal divided by 2 is used with the noise filter 0 1 1: The clock signal divided by 4 is used with the noise filter 1 0 0: The clock signal divided by 8 is used with the noise filter. Other settings are prohibited.	R/W*1
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Writing to these bits is only possible when the RE and TE bits in the SCR/SCR_SMCI are 0 (serial reception and transmission disabled).

The SNFR register sets the digital noise filter clock.

NFCS[2:0] bits (Noise Filter Clock Select)

The NFCS[2:0] bits select the sampling clock for the digital noise filter. To use the noise filter in asynchronous mode, set these bits to 000b. In simple IIC mode, set the bits to a value in the range from 001b to 100b.

27.2.21 I²C Mode Register 1 (SIMR1)

Address(es): SCI0.SIMR1 4007 0009h, SCI1.SIMR1 4007 0029h, SCI9.SIMR1 4007 0129h

	b7	b6	b5	b4	b3	b2	b1	b0
	IICDL[4:0]					—	—	IICM
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	IICM	Simple IIC Mode Select	SMIF IICM 0 0: Asynchronous mode, multi-processor mode, clock synchronous mode 0 1: Simple IIC mode 1 0: Smart card interface mode 1 1: Setting prohibited.	R/W*1
b2, b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit name	Description	R/W
b7 to b3	IICDL[4:0]	SDA Delay Output Select	The following cycles are of the clock signal from the on-chip baud rate generator: b7 b3 0 0 0 0 0: No output delay 0 0 0 0 1: 0 to 1 cycle 0 0 0 1 0: 1 to 2 cycles 0 0 0 1 1: 2 to 3 cycles 0 0 1 0 0: 3 to 4 cycles 0 0 1 0 1: 4 to 5 cycles 1 1 1 1 0: 29 to 30 cycles 1 1 1 1 1: 30 to 31 cycles.	R/W*1

Note 1. Writing to these bits is only possible when the RE and TE bits in the SCR are 0 (both serial transmission and reception are disabled).

SIMR1 is used to select simple IIC mode and the number of delay stages for the SDAn output.

IICM bit (Simple IIC Mode Select)

In combination with the SMIF bit in SCMR, the IICM bit selects the operating mode.

IICDL[4:0] bits (SDA Delay Output Select)

The IICDL[4:0] bits are used to set a delay for output on the SDAn pin relative to the falling edge of the output on the SCLn pin.

The available delay settings range from no delay to 31 cycles, with the clock signal from the on-chip baud rate generator as the base. The signal obtained by frequency-dividing PCLKB by the divisor set in SMR.CKS[1:0], is supplied as the clock signal from the on-chip baud rate generator. Set these bits to 00000b unless operation is in simple IIC mode. In simple IIC mode, set the bits to a value in the range from 00001b to 11111b.

27.2.22 I2C Mode Register 2 (SIMR2)

Address(es): SCI0.SIMR2 4007 000Ah, SCI1.SIMR2 4007 002Ah, SCI9.SIMR2 4007 012Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	IICACKT	—	—	—	IICCSC	IICINTM
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	IICINTM	IIC Interrupt Mode Select	0: Use ACK/NACK interrupts 1: Use reception and transmission interrupts.	R/W*1
b1	IICCSC	Clock Synchronization	0: No synchronization with the clock signal 1: Synchronization with the clock signal.	R/W*
b4 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	IICACKT	ACK Transmission Data	0: ACK transmission 1: NACK transmission and reception of ACK/NACK.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Writing to these bits is only possible when the RE and TE bits in the SCR are 0 (serial reception and transmission disabled).

SIMR2 is used to select how reception and transmission are controlled in simple IIC mode.

IICINTM bit (IIC Interrupt Mode Select)

The IICINTM bit selects the sources of interrupt requests in simple IIC mode.

IICCSC bit (Clock Synchronization)

Set the IICCSC bit to 1 if the internally generated SCL clock signal is to be synchronized when the SCLn pin is placed at the low level for a wait inserted by other device, for example.

The SCL clock signal is not synchronized if the IICCSC bit is 0. The SCLn clock signal is generated according to the rate selected in the BRR regardless of the level being input on the SCLn pin.

Set the IICCSC bit to 1 except during debugging.

IICACKT bit (ACK Transmission Data)

The IICACKT bit transmits data that contains ACK bits. Set this bit to 1 when ACK and NACK bits are received.

27.2.23 I²C Mode Register 3 (SIMR3)

Address(es): SCI0.SIMR3 4007 000Bh, SCI1.SIMR3 4007 002Bh, SCI9.SIMR3 4007 012Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	IICSCLS[1:0]		IICSDAS[1:0]		IICSTIF	IICSTPREQ	IICRSTAREQ	IICSTAREQ
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	IICSTAREQ	Start Condition Generation	0: A start condition is not generated 1: A start condition is generated.*1, *3, *5, *6	R/W
b1	IICRSTAREQ	Restart Condition Generation	0: A restart condition is not generated 1: A restart condition is generated.*2, *3, *5, *6	R/W
b2	IICSTPREQ	Stop Condition Generation	0: A stop condition is not generated 1: A stop condition is generated.*2, *3, *5, *6	R/W
b3	IICSTIF	Issuing of Start, Restart, or Stop Condition Completed Flag	0: There are no requests for generating conditions or a condition is being generated 1: A start, restart, or stop condition is completely generated. When 0 is written to IICSTIF, it is cleared to 0.*4	R/W*4
b5, b4	IICSDAS[1:0]	SDA Output Select	b5 b4 0 0: Serial data output 0 1: Generate a start, restart, or stop condition 1 0: Output the low level on the SDAn pin 1 1: Place the SDAn pin in the high-impedance state.	R/W
b7, b6	IICSCLS[1:0]	SCL Output Select	b7 b6 0 0: Serial clock output 0 1: Generate a start, restart, or stop condition 1 0: Output the low level on the SCLn pin 1 1: Place the SCLn pin in the high-impedance state.	R/W

Note 1. Only generate a start condition after checking the bus state and confirming that it is free.
Note 2. Generate a restart or stop condition after checking the bus state and confirming that it is busy.
Note 3. Do not set more than one of the IICSTAREQ, IICRSTAREQ, and IICSTPREQ bits to 1 at a given time.
Note 4. Write only 0. When 1 is written, the value is ignored.
Note 5. Execute the generation of a condition after the value of the IICSTIF flag is 0.
Note 6. Do not write 0 to this bit while it is 1. Generation of a condition is suspended by writing 0 to this bit while it is 1.

IICSTAREQ bit (Start Condition Generation)

When a start condition is to be generated, set both the IICSDAS[1:0] and IICSCLS[1:0] bits to 01b in addition to setting the IICSTAREQ bit to 1.

[Setting condition]

- Writing 1 to the bit.

[Clearing condition]

- Completion of the start condition generation.

IICRSTAREQ bit (Restart Condition Generation)

When a restart condition is to be generated, set both the IICSDAS[1:0] and IICSCLS[1:0] bits to 01b in addition to setting the IICRSTAREQ bit to 1.

[Setting condition]

- Writing 1 to the bit.

[Clearing condition]

- Completion of the restart condition generation.

IICSTPREQ bit (Stop Condition Generation)

When a stop condition is to be generated, set both the IICSDAS[1:0] and IICSCLS[1:0] bits to 01b in addition to setting the IICSTPREQ bit to 1.

[Setting condition]

- Writing 1 to the bit.

[Clearing condition]

- Completion of the stop condition generation.

IICSTIF flag (Issuing of Start, Restart, or Stop Condition Completed Flag)

After generating a condition, the IICSTIF flag indicates that the generation is complete. When using the IICSTAREQ, IICRSTAREQ, or IICSTPREQ bit to cause generation of a condition, do so after setting the IICSTIF flag to 0.

When the IICSTIF flag is 1 while an interrupt request is enabled by setting the SCR.TEIE bit, an STI request is output.

[Setting condition]

- Completion of the start, restart, or stop condition generation. If this conflicts with any of the clearing conditions for the flag, the other condition takes precedence.

[Clearing conditions]

- Writing 0 to the bit (after that, confirm that the IICSTIF flag is 0)
- Writing 0 to the SIMR1.IICM bit when operation is not in simple IIC mode
- Writing 0 to the SCR.TE bit.

IICSDAS[1:0] bits (SDA Output Select)

The IICSDAS[1:0] bits control output from the SDAn pin.

Set the IICSDAS[1:0] and IICSCLS[1:0] bits to the same value.

IICSCLS[1:0] bits (SCL Output Select)

The IICSCLS[1:0] bits control output from the SCLn pin.

Set the IICSCLS[1:0] and IICSDAS[1:0] bits to the same value.

27.2.24 I²C Status Register (SISR)

Address(es): SCI0.SISR 4007 000Ch, SCI1.SISR 4007 002Ch, SCI9.SISR 4007 012Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	IICACKR
Value after reset:	0	0	x	x	0	x	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	IICACKR	ACK Reception Data Flag	0: ACK received 1: NACK received.	R
b1	—	Reserved	This bit is read as 0	R
b2	—	Reserved	The read value is undefined	R

Bit	Symbol	Bit name	Description	R/W
b3	—	Reserved	This bit is read as 0	R
b5, b4	—	Reserved	The read values are undefined	R
b7, b6	—	Reserved	These bits are read as 0	R

SISR is used to monitor state in simple IIC mode.

IICACKR flag (ACK Reception Data Flag)

Received ACK and NACK bits can be read from the IICACKR flag. This flag is updated on the rising edge of the SCL clock for the ACK/NACK receiving bit.

27.2.25 SPI Mode Register (SPMR)

Address(es): SCI0.SPMR 4007 000Dh, SCI1.SPMR 4007 002Dh, SCI9.SPMR 4007 012Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	CKPH	CKPOL	—	MFF	—	MSS	CTSE	SSE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SSE	SSn Pin Function Enable	0: SSn pin function is disabled 1: SSn pin function is enabled.	R/W*1
b1	CTSE	CTS Enable	0: CTS function is disabled (RTS output function is enabled) 1: CTS function is enabled.	R/W*1
b2	MSS	Master Slave Select	0: Transmission is through the TXDn pin and reception is through the RXDn pin (master mode) 1: Reception is through the TXDn pin and transmission is through the RXDn pin (slave mode).	R/W*1
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	MFF	Mode Fault Flag	0: No mode fault error 1: Mode fault error.	R/W*2
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	CKPOL	Clock Polarity Select	0: Clock polarity is not inverted 1: Clock polarity is inverted.	R/W*1
b7	CKPH	Clock Phase Select	0: Clock is not delayed 1: Clock is delayed.	R/W*1

Note 1. Writing to these bits is only possible when the RE and TE bits in the SCR are 0 (both serial transmission and reception are disabled).
Note 2. Only write 0 to these bits to clear the flag.

SPMR is used to select the extension settings in asynchronous and clock synchronous modes.

SSE bit (SSn Pin Function Enable)

Set the SSE bit to 1 if the SSn pin is used to control transmission and reception (in simple SPI mode). Set this bit to 0 in any other mode. Additionally, for usage in simple SPI mode, the SSn pin on the master side is not required to control reception and transmission when master mode (SCR.CKE[1:0] = 00b and MSS = 0) is selected and there is a single master. Therefore, the setting of the SSE bit is 0. Do not set both the SSE and CTSE bits to enabled as operation is the same as that when these bits are set to 0.

CTSE bit (CTS Enable)

Set the CTSE bit to 1 if the SSn pin is used to input the CTS control signal to control transmission and reception. The RTS signal is output when this bit is set to 0. Set this bit to 0 in smart card interface mode, simple SPI mode, and simple IIC mode. Do not set both the CTSE and SSE bits to enabled as operation is the same as that when these bits are set to 0.

MSS bit (Master Slave Select)

The MSS bit selects between master and slave operation in simple SPI mode. The functions of the TXDn and RXDn pins are reversed when the MSS bit is set to 1, so that data is received through the TXDn pin and transmitted through the RXDn pin. Set this bit to 0 in modes other than simple SPI mode.

MFF flag (Mode Fault Flag)

The MFF flag indicates mode fault errors.

In a multi-master configuration, determine the mode fault error occurrence by reading the MFF flag.

[Setting condition]

- Input on the SSn pin is at the low level during master operation in simple SPI mode (SSE bit = 1 and MSS bit = 0).

[Clearing condition]

- Writing 0 to the flag after it is read as 1.

CKPOL bit (Clock Polarity Select)

The CKPOL bit selects the polarity of the clock signal output through the SCKn pin. See Figure 27.70 for details.

Set this bit to 0 in other than simple SPI mode and clock synchronous mode.

CKPH bit (Clock Phase Select)

The CKPH bit selects the phase of the clock signal output through the SCKn pin. See Figure 27.70 for details.

Set this bit to 0 in other than simple SPI mode and clock synchronous mode.

27.2.26 FIFO Control Register (FCR)

Address(es): SCI0.FCR 4007 0014h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RSTRG[3:0]				RTRG[3:0]				TTRG[3:0]				DRES	TFRST	RFRST	FM
Value after reset:	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	FM	FIFO Mode Select	Valid only in asynchronous mode including multi-processor or clock synchronous mode: 0: Non-FIFO mode. Selects TDR/RDR or TDRHL/RDRHL for communication. 1: FIFO mode. Selects FTDRHL/FRDRHL for communication.	R/W*1
b1	RFRST	Receive FIFO Data Register Reset	Valid only in FCR.FM = 1: 0: Not reset to FRDRHL 1: Reset to FRDRHL.	R/W
b2	TFRST	Transmit FIFO Data Register Reset	Valid only in FCR.FM = 1: 0: Not reset to FTDRHL 1: Reset to FTDRHL.	R/W
b3	DRES	Receive Data Ready Error Select Bit	When detecting a reception data ready, the interrupt request is selected: 0: Receive data full interrupt (SCIn_RXI) 1: Receive error interrupt (SCIn_ERI).	R/W
b7 to b4	TTRG[3:0]	Transmit FIFO Data Trigger Number	Valid only in asynchronous mode including multi-processor or clock synchronous mode: 0000: Trigger number 0 1111: Trigger number 15.	R/W

Bit	Symbol	Bit name	Description	R/W
b11 to b8	RTRG[3:0]	Receive FIFO Data Trigger Number	Valid only in asynchronous mode including multi-processor or clock synchronous mode 0000: Trigger number 0 1111: Trigger number 15.	R/W
b15 to b12	RSTRG[3:0]	RTS Output Active Trigger Number Select	Valid only in asynchronous mode including multi-processor or clock synchronous mode, while FCR.FM = 1, SPMR.CTSE = 0, and SPMR.SSE = 0: 0000: Trigger number 0 1111: Trigger number 15.	R/W

Note 1. Writable only when TE = 0 and RE = 0.

FCR is a register for setting FIFO mode selection, reset of FTDRHL/FRDRHL, FIFO data trigger number of transmission/reception, and RTS output active trigger number.

FM bit (FIFO Mode Select)

When the FM bit is set to 1, FTDRHL and FRDRHL are selected for communication. When the FM bit is set to 0, TDR and RDR or TDRHL and RDRHL are selected for communication.

RFRST bit (Receive FIFO Data Register Reset)

The FRDRHL register is reset when the RFRST bit is set to 1, and the number of receive data is reset to 0. After writing 1, this bit is set to 0 after 1 PCLKB.

TFRST bit (Transmit FIFO Data Register Reset)

The FTDRHL register is reset when the TFRST bit is set to 1, and the number of transmit data is reset to 0. After writing 1, this bit is set to 0 after 1 PCLKB.

DRES bit (Receive Data Ready Error Select Bit)

When the DRES bit is set to 1, receive error interrupt (SCIn_ERI) is selected. When the DRES bit is set to 0, receive data full interrupt is selected.

When starting DTC and reading the FRDRH and FRDRL registers, set DRES to 1.

TTRG[3:0] bits (Transmit FIFO Data Trigger Number)

The TDFE flag is set to 1 when the amount of transmit data in the Transmit FIFO Data Register (FTDRHL) is equal to or less than the specified transmit triggering number, and software can write data to FTDRHL. If SCR.TIE = 1, SCIn_TXI interrupt request occurred.

RTRG[3:0] bits (Receive FIFO Data Trigger Number)

The RDF flag is set to 1 when the amount of receive data in the Receive FIFO Data Register (FRDRHL) is equal to or greater than the specified receive triggering number, and software can read data from FRDRHL. If SCR.RIE = 1, SCIn_RXI interrupt request occurred. But, when RTRG is set to 0, the RDF flag is not set even when the amount of the data in receive FIFO is equal to 0. Additionally, an SCIn_RXI interrupt does not occur.

RSTRG[3:0] bits (RTS Output Active Trigger Number Select)

When the amount of receive data stored in the Receive FIFO Data Register (FRDRHL) is equal to or greater than the specified receive triggering number, the RTSn signal is high. But, when RSTRG is set to 0, the RTSn signal is not high even when the quality of the data in receive FIFO is equal to 0.

27.2.27 FIFO Data Count Register (FDR)

Address(es): SCI0.FDR 4007 0016h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	T[4:0]					—	—	—	R[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	R[4:0]	Receive FIFO Data Count	Valid only in asynchronous mode, including multi-processor or clock synchronous mode, while FCR.FM = 1. Indicate the amount of receive data stored in FRDRHL.	R
b7 to b5	—	Reserved	These bits are read as 0	R
b12 to b8	T[4:0]	Transmit FIFO Data Count	Valid only in asynchronous mode, including multi-processor or clock synchronous mode, while FCR.FM = 1. Indicate the amount of non-transmit data stored in FTDRHL.	R
b15 to b13	—	Reserved	These bits are read as 0	R

This register indicates the amount of data stored in FRDRHL/FTDRHL.

R[4:0] bits (Receive FIFO Data Count)

The R[4:0] bits indicate the amount of receive data stored in FRDRHL. A value of 00h means no receive data, and 10h means that the maximum received data is stored in FRDRHL.

T[4:0] bits (Transmit FIFO Data Count)

The T[4:0] bits indicate the amount of non-transmitted data stored in FTDRHL. A value of 00h means no transmit data, and 10h means that all (maximum count) of the data to be transmitted is stored in FTDRHL.

27.2.28 Line Status Register (LSR)

Address(es): SCI0.LSR 4007 0018h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PNUM[4:0]					—	FNUM[4:0]					—	ORER
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ORER	Overrun Error Flag	Valid only in asynchronous mode, including multi-processor or clock synchronous mode, and FIFO selected: 0: No overrun error occurred 1: An overrun error occurred.	R*1
b1	—	Reserved	This bit is read as 0	R
b6 to b2	FNUM[4:0]	Framing Error Count	Indicates the amount of data with a framing error among the receive data stored in the receive FIFO data register (FRDRHL)	R
b7	—	Reserved	This bit is read as 0	R
b12 to b8	PNUM[4:0]	Parity Error Count	Indicates the amount of data with a parity error among the receive data stored in the receive FIFO data register (FRDRHL).	R
b15 to b13	—	Reserved	These bits are read as 0	R

Note 1. If this flag is read, it is not complete to the read of SSR_FIFO register. If 1 is read, write 0 to SSR_FIFO.ORER to clear the flag.

The LSR register indicates the status of receive error.

ORER bit (Overrun Error Flag)

The ORER bit reflects the value in SSR_FIFO.ORER.

FNUM[4:0] bits (Framing Error Count)

The FNUM[4:0] value indicates the amount of data stored in the FRDRHL register with a framing error.

PNUM[4:0] bits (Parity Error Count)

The PNUM[4:0] value indicates the amount of data stored in the FRDRHL register with a parity error.

27.2.29 Compare Match Data Register (CDR)

Address(es): SCI0.CDR 4007 001Ah, SCI1.CDR 4007 003Ah, SCI9.CDR 4007 013Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CMPD[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b8 to b0	CMPD[8:0]	Compare Match Data	Compare data pattern for address match wakeup function	R/W
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The CDR register sets the address match function.

CMPD[8:0] bits (Compare Match Data)

The CMPD[8:0] bits set the data to be compared to receive data for the address match function when address match function is enabled (DCCR.DCME = 1).

Three bit lengths are available:

- MPD[6:0] with 7-bit length
- CMPD[7:0] with 8-bit length
- CMPD[8:0] with 9-bit length.

27.2.30 Data Compare Match Control Register (DCCR)

Address(es): SCI0.DCCR 4007 0013h, SCI1.DCCR 4007 0033h, SCI9.DCCR 4007 0133h

	b7	b6	b5	b4	b3	b2	b1	b0
	DCME	IDSEL	—	DFER	DPER	—	—	DCMF
Value after reset:	0	1	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DCMF	Data Compare Match Flag	0: Not matched 1: Matched.	R/W*1
b2, b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3	DPER	Data Compare Match Parity Error Flag	0: No parity error occurred 1: A parity error occurred.	R/W*1
b4	DFER	Data Compare Match Framing Error Flag	0: No framing error occurred 1: A framing error occurred.	R/W*1
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit name	Description	R/W
b6	IDSEL	ID Frame Select	Valid only in asynchronous mode, including multi-processor mode: 0: Always compare data regardless of the MPB bit value 1: Compare data when the MPB bit is 1 (ID frame) only.	R/W
b7	DCME	Data Compare Match Enable	Valid only in asynchronous mode including multi-processor mode: 0: Address match function is disabled 1: Address match function is enabled.	R/W

Note 1. Only 0 can be written to clear the flag after reading 1.

DCCR sets control of the address match function.

DCMF flag (Data Compare Match Flag)

The DCMF flag indicates that the SCI detected a receive data match with the comparison data (CDR.CMPD).

[Setting condition]

- Matched to the comparison data (CDR.CMPD) with the receive data when DCCR.DCME = 1.

[Clearing condition]

- When 0 is written after 1 is read from DCMF.

Clearing the RE bit to 0 in the Serial Control Register (SCR) does not affect the DCMF flag, which retains its previous state.

DPER flag (Data Compare Match Parity Error Flag)

The DPER flag indicates that a parity error occurred on address match detection (reception data match detection).

[Setting condition]

- When a parity error is detected by the frame in which an address match is detected.

[Clearing conditions]

- When 0 is written after 1 is read from DPER.
- When the RE bit in SCR is set to 0 (serial reception is disabled), the DPER flag is not affected and retains its previous value.

DFER flag (Data Compare Match Framing Error Flag)

The DFER flag indicates that a framing error occurs on address match detection (receive data match detection).

[Setting conditions]

- When a stop bit of the frame in which an address match is detected is 0
- When in 2-stop mode, only the 1st bit of the stop bits is checked for a value of 1 (the second bit is not checked).

[Clearing conditions]

- When 0 is written after 1 is read from DFER
- When the RE bit in SCR is set to 0 (serial reception is disabled), the DFER flag is not affected and retains its previous value.

IDSEL bit (ID Frame Select)

The ISDEL bit selects whether to compare data regardless of the MPB bit value or to compare data only when MPB = 1 (ID frame) when the address match function is enabled. Set the time for address match function selection to choose at the same time.

DCME bit (Data Compare Match Enable)

The DCME bit enables or disables the address match function (data compare match function).

If the SCI detects a match to the comparison data (CDR.CMPD) with the receive data, DCME is cleared automatically, after which, SCI operation mode is receive mode without the data compare match function. See section 27.3.6, Address Match (Receive Data Match Detection) Function.

The write value should be 0 for any mode other than asynchronous mode.

27.2.31 Serial Port Register (SPTR)

Address(es): SCI0.SPTR 4007 001Ch, SCI1.SPTR 4007 003Ch, SCI9.SPTR 4007 013Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SPB2IO	SPB2DT	RXDMON
Value after reset:	0	0	0	0	0	0	1	1

Bit	Symbol	Bit name	Description	R/W
b0	RXDMON	Serial Input Data Monitor	The state of the RXDn pin: 0: RXDn pin is at the Low level 1: RXDn pin is at the High level.	R
b1	SPB2DT	Serial Port Break Data Select	The output level of TXDn pin is selected when SCR.TE = 0: 0: Low level is output in TXDn pin 1: High level is output in TXDn pin.	R/W
b2	SPB2IO	Serial Port Break I/O	Selects whether the value of SPB2DT is output to TXDn pin: 0: The value of SPB2DT bit is not output in TXDn pin 1: The value of SPB2DT bit is output in TXDn pin.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The SPTR register provides confirmation of serial reception pin (RXDn pin) status and sets transmission pin (TXDn pin) status.

This register can only be used in asynchronous mode.

The TXDn pin status is determined by the combination of SCR.TE, SPTR.SPB2IO, and SPTR.SPB2DT settings, as shown in Table 27.22.

Table 27.22 TXDn pin status

Value of SCR.TE	Value of SPTR.SPB2IO	Value of SPTR.SPB2DT	TXDn pin status
0	0	x	Hi-Z (initial value)
0	1	0	Low level output
0	1	1	High level output
1	x	x	Serial transmission data is output

x: Don't care.

Note: Use the SPTR register in asynchronous mode only. Using this register in any other mode is not guaranteed.

27.3 Operation in Asynchronous Mode

Figure 27.2 shows the general format for asynchronous serial communications. One frame consists of a start bit (low level), transmit/receive data, a parity bit, and stop bits (high level).

In asynchronous serial communications, the communications line is held in the mark state (high level) when not communicating.

The SCI monitors the communications line. When the SCI detects a low, it regards that as a start bit and starts serial communication.

Inside the SCI, the transmitter and receiver are independent units, enabling full-duplex communications. Both the transmitter and the receiver have a double-buffered structure in addition to FIFO mode, so that data can be read or written during transmission or reception, enabling continuous data transmission and reception.

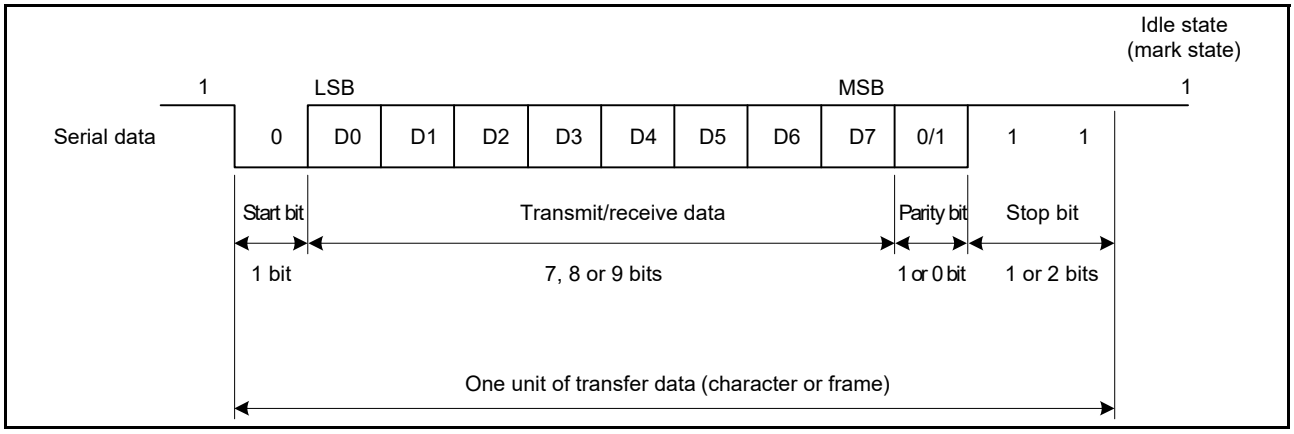


Figure 27.2 Data format in asynchronous serial communications with 8-bit data, parity, and 2 stop bits

27.3.1 Serial Data Transfer Format

Table 27.23 lists the serial data transfer formats that can be used in asynchronous mode. Any of the 18 transfer formats can be selected according to the SMR and SCMR settings. For details on the multi-processor function, see section 27.4, Multi-Processor Communications Function.

Table 27.23 Serial transfer formats in asynchronous mode (1 of 2)

SCMR setting	SMR setting				Serial transfer format and frame length												
					1	2	3	4	5	6	7	8	9	10	11	12	13
CHR1	CHR	PE	MP	STOP													
0	0	0	0	0	S	9-bit data									STOP		
0	0	0	0	1	S	9-bit data									STOP	STOP	
0	0	1	0	0	S	9-bit data									P	STOP	
0	0	1	0	1	S	9-bit data									P	STOP	STOP
1	0	0	0	0	S	8-bit data								STOP			
1	0	0	0	1	S	8-bit data								STOP	STOP		
1	0	1	0	0	S	8-bit data								P	STOP		

Table 27.23 Serial transfer formats in asynchronous mode (2 of 2)

SCMR setting	SMR setting				Serial transfer format and frame length												
					1	2	3	4	5	6	7	8	9	10	11	12	13
CHR1	CHR	PE	MP	STOP													
1	0	1	0	1	S	8-bit data								P	STOP	STOP	
1	1	0	0	0	S	7-bit data							STOP				
1	1	0	0	1	S	7-bit data							STOP	STOP			
1	1	1	0	0	S	7-bit data							P	STOP			
1	1	1	0	1	S	7-bit data							P	STOP	STOP		
0	0	—	1	0	S	9-bit data									MPB	STOP	
0	0	—	1	1	S	9-bit data									MPB	STOP	STOP
1	0	—	1	0	S	8-bit data								MPB	STOP		
1	0	—	1	1	S	8-bit data								MPB	STOP	STOP	
1	1	—	1	0	S	7-bit data							MPB	STOP			
1	1	—	1	1	S	7-bit data							MPB	STOP	STOP		

S: Start bit
STOP: Stop bit
P: Parity bit
MPB: Multi-processor bit

27.3.2 Receive Data Sampling Timing and Reception Margin in Asynchronous Mode

In asynchronous mode, the SCI operates on a base clock with a frequency of 16 times*1 the bit rate.

In reception, the SCI samples the falling edge of the start bit using the base clock, and performs internal synchronization.

Because receive data is sampled on the rising edge of the 8th pulse*1 of the base clock, data is latched at the middle of each bit, as shown in Figure 27.3. Therefore, the reception margin in asynchronous mode is determined by the following formula (1):

$$M = \left| (0.5 - \frac{1}{2N}) - (L - 0.5)\ F - \frac{\lfloor D - 0.5 \rfloor}{N}\ (1 + F) \right| \times 100\ [\%] \cdots \text{Formula (1)}$$

M: Reception margin
N: Ratio of bit rate to clock
N = 16 when ABCSE in SEMR = 0 and ABCS in SEMR = 0
N = 8 when ABCS in SEMR = 1, N = 6 when ABCSE in SEMR = 1
D: Duty cycle of clock (D = 0.5 to 1.0)
L: Frame length (L = 9 to 13)
F: Absolute value of clock frequency deviation

Assuming the values of F = 0 and D = 0.5 in formula (1), the reception margin is determined by the following formula:

$$M = \{0.5 - 1/(2 \times 16)\} \times 100\ (\%) = 46.875\%$$

This represents the computed value, and a margin of 20% to 30% should be allowed in system design.

Note 1. In this example, the ABCS bit in SEMR is 0 and ABCSE bit in SEMR is 0. When the ABCS bit is 1, and the ABCSE bit is 0, a frequency of 8 times the bit rate is used as a base clock, and receive data is sampled on the rising edge of the 4th pulse of the base clock.
When the ABCSE bit is 1, a sextuple frequency of a bit rate is used as a base clock, and receive data is sampled on the rising edge of the 3rd pulse of the base clock.

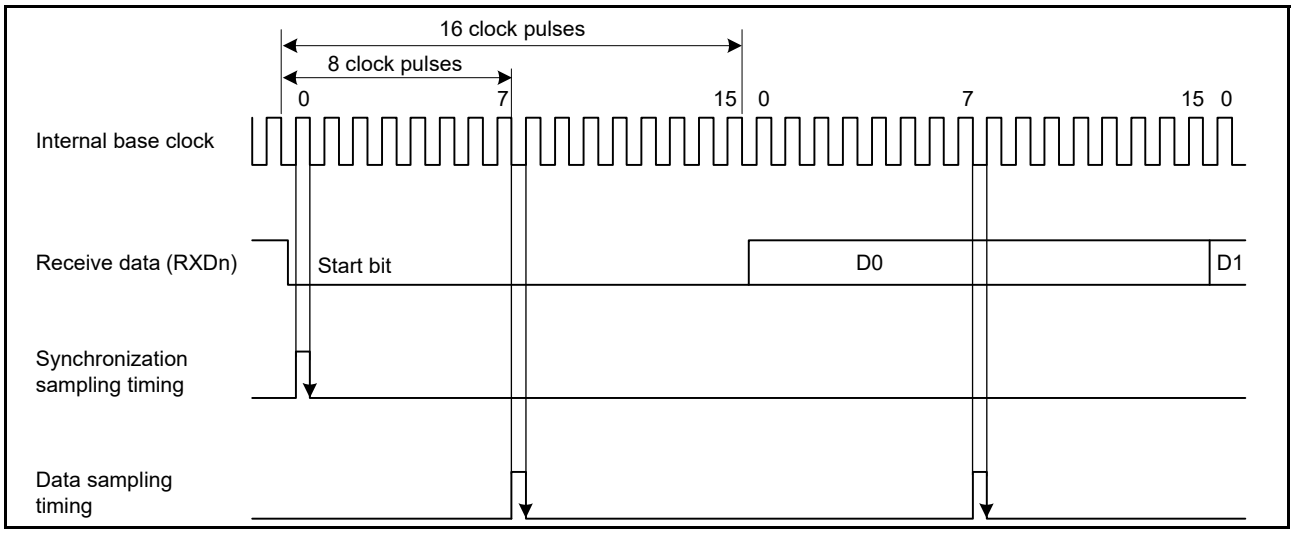


Figure 27.3 Receive data sampling timing in asynchronous mode

27.3.3 Clock

Either an internal clock generated by the on-chip baud rate generator or an external clock input to the SCKn pin can be selected as the transfer clock of the SCI, based on the CM bit in SMR and the CKE[1:0] bits in SCR.

When an external clock is input to the SCKn pin, the clock frequency must be 16 times the bit rate (when ABCS in SEMR = 0) or 8 times the bit rate (when ABCS in SEMR = 1).

When the SCI uses its internal clock, the clock can be output from the SCKn pin. The frequency of the clock output in this case is equal to the bit rate, and the phase is configured so that the rising edge of the clock is in the middle of the

transmit data, as Figure 27.4 shows.

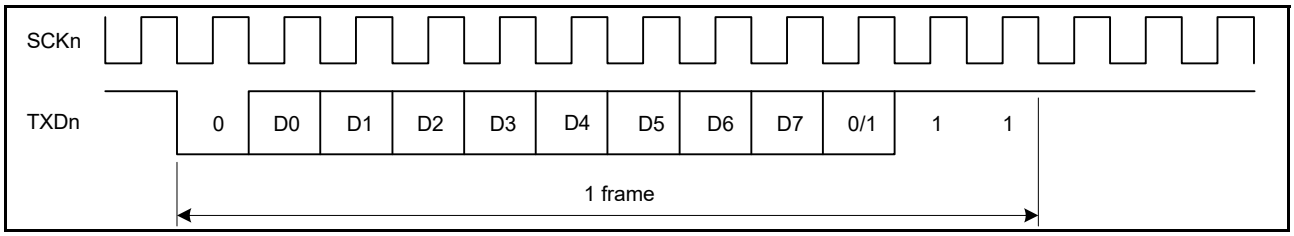


Figure 27.4 Phase relationship between output clock and transmit data in asynchronous mode when SMR.CHR = 0, PE = 1, MP = 0, STOP = 1

27.3.4 Double-Speed Operation and Frequency of 6 Times the Bit Rate

When the ABCS bit in SEMR is set to 1 and 8 pulses of the base clock for a 1-bit period is selected, the SCI operates on the bit rate twice that when ABCS is set to 0. When the BGDM bit in SEMR is set to 1, the cycle of the base clock is half and the bit rate is double that when BGDM is set to 0. When the CKE[1] bit in SCR is set to 0 and the on-chip baud rate generator is selected, setting the ABCS and BGDM bits to 1 allows the SCI to operate on a bit rate 4 times that when the ABCS and BGDM bits are set to 0. When the ABCSE bit in SEMR is set to 1, the number of basic clock pulses are 6 during a period of 1 bit, and the SCI operates at 16/3 times that when SEMR.ABCS, SEMR.BGDM, and SMER.ABCSE are 0.

As shown by Formula (1) in section 27.3.2, Receive Data Sampling Timing and Reception Margin in Asynchronous Mode, the reception margin decreases when the ABCS bit in SEMR is set to 1 or ABCSE bit in SEMR is set to 1. Therefore, if the target bit rate can be obtained with ABCS or ABCSE set to 0, it is recommended that you use the SCI with ABCSE and ABCS set to 0.

27.3.5 CTS and RTS Functions

The CTS function uses input on the CTSn_RTSn pin in transmission control. Setting the SPMR.CTSE bit to 1 enables the CTS function. When the CTS function is enabled, placing the low level on the CTSn_RTSn pin causes transmission to start.

Applying the high level to the CTSn_RTSn pin while transmission is in progress does not affect transmission of the current frame.

In the RTS function that uses output on the CTSn_RTSn pin, a low level is output when reception becomes possible. Conditions for output of the low and high level are shown in this section.

[Conditions for low-level output]

(a) Non-FIFO selected when all of the following conditions are satisfied

- The value of the RE bit in the SCR is 1
- Reception is not in progress
- There is no receive data yet to be read
- The ORER, FER, and PER flags in the SSR are all 0.

(b) FIFO selected when all of the following conditions are satisfied

- The value of the RE bit in the SCR is 1
- When the amount of receive data written in FRDRHL is equal to or less than the specified receive triggering number
- The ORER in the SSR_FIFO (ORER in the FRDRH) is 0.

[Condition for high-level output]

(a) Non-FIFO selected

- The conditions for low-level output are not satisfied.
- When reception is terminated with SCR.RE = 0 without reading the RDR register after reception is complete, RTS

remains high. At this time, read the SCR register for dummy values after writing 0 to SCR.RE.

(b) FIFO selected

- The conditions for low-level output are not satisfied.

27.3.6 Address Match (Receive Data Match Detection) Function

The address match function can be used only in asynchronous mode.

If the DCCR.DCME is set to 1*4, when one frame of data is received, SCI compares that received data with the data set in CDR.CMPD. If SCI detects a match to the comparison data (CDR.CMPD*3) with the received data, SCI can issue the SCIn_RXI interrupt request.

If the SMR.MP bit is set to 0, comparison occurs only for valid data in receive format. In multi-processor mode (SMR.MP bit = 1), if DCCR.IDSEL bit is set to 1, receive data where the MPB bit is 1 is subject to comparison for address match. Receive data where the MPB bit is 0 is always treated as a mismatch.

If DCCR.IDSEL bit is set to 0, SCI performs address match or mismatch regardless the value of the MPB bit of the received data.

Until SCI detects a match to the comparison data (CDR.CMPD*3) with receive data, received data is skipped (discarded), and SCI cannot detect parity error or framing error.

When SCI detects the match, the DCCR.DCME is automatically cleared, and DCCR.DCMF is set to 1.

If DCCR.IDSEL bit is set to 1 at this time, SCR.MPIE bit is automatically cleared, and if DCCR.IDSEL bit is set to 0 at this time, the value of SCR.MPIE bit is retained. At the same time, if SCR.RIE is set to 1, SCI issues an SCIn_RXI interrupt request. If SCI detects a framing error in the receive data for which a match is detected, DCCR.DFER is set to 1, and if SCI detects a parity error in that frame, DCCR.DPER is set to 1. The compared receive data is not stored in the RDR register*1, and SSR.RDRF remains 0.*2

After SCI detects a match, and the DCCR.DCME is automatically cleared, it receives the next data continuously based on the current register setting.

When the DCCR.DFER flag or DCCR.DPER flag is set, the address match is not performed. Before enabling the address match function, set DCCR.DFER and DCCR.DPER flag to 0.

An example of the address match function is shown in Figure 27.5 and Figure 27.6.

Note 1. When FCR.FM = 1, this refers to the FRDRHL register.
Note 2. When FCR.FM = 1, this refers to the SSR_FIFO.RDF flag.
Note 3. This comparative target can select one length of 3 types: CMPD[6:0] with 7-bit length, CMPD[7:0] with 8-bit length, and CMPD[8:0] with 9-bit length.
Note 4. Set the DCCR.DCME bit to 1 before receiving the start bit of the received frame that performs address matching.

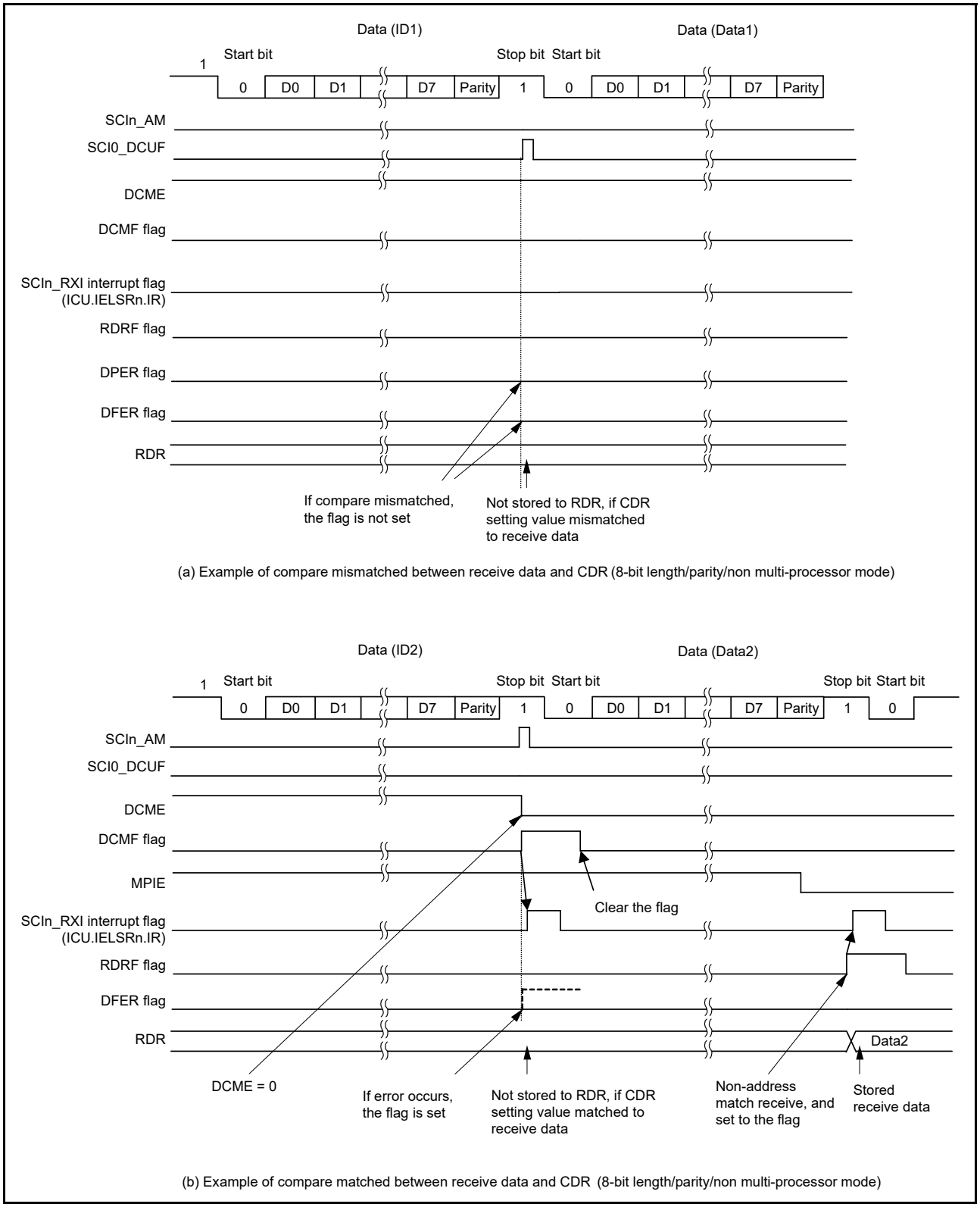


Figure 27.5 Example of address match (1) non multi-processor mode

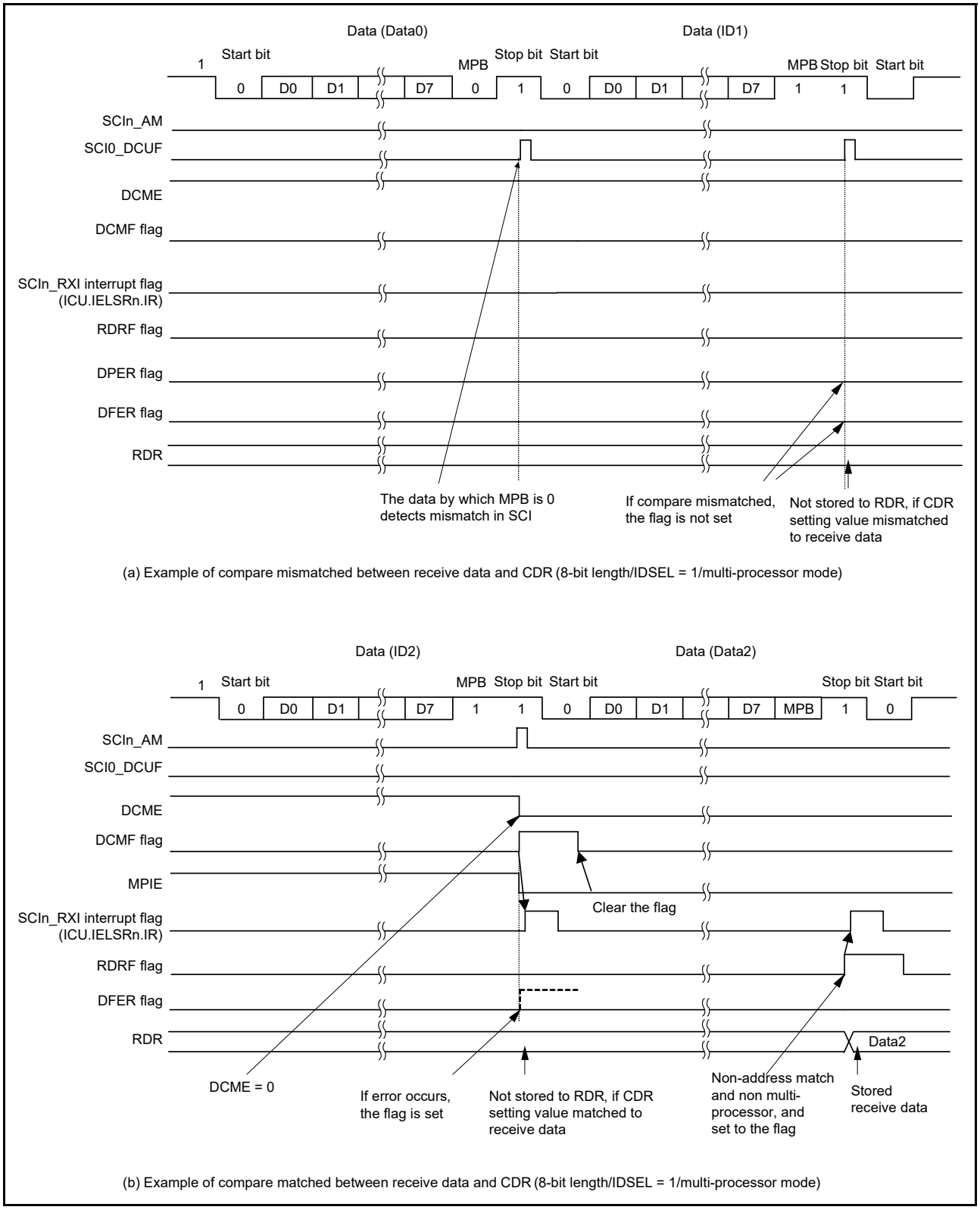


Figure 27.6 Example of address match (2) multi-processor mode

27.3.7 SCI Initialization in Asynchronous Mode

Before transmitting and receiving data, start by writing the initial value 00h to SCR and then continue through the SCI procedure (select non-FIFO or FIFO) shown in Figure 27.7 and Figure 27.8. Whenever the operating mode or transfer format is to be changed, SCR must be initialized before the change is made.

When the external clock is used in asynchronous mode, ensure that the clock signal is supplied during initialization.

Note: Setting the SCR.RE bit to 0 initializes neither the ORER, FER, RDRF, RDF, PER and DR flags in SSR/SSR_FIFO nor RDR and RDRHL. When the TE bit is set to 0, the TEND flag for the selected FIFO buffer is not initialized.

Note: In non-FIFO mode, switching the value of the SCR.TE bit from 1 to 0 or 0 to 1 while the SCR.TIE bit is 1 leads to the generation of an SCIn_TXI interrupt request.

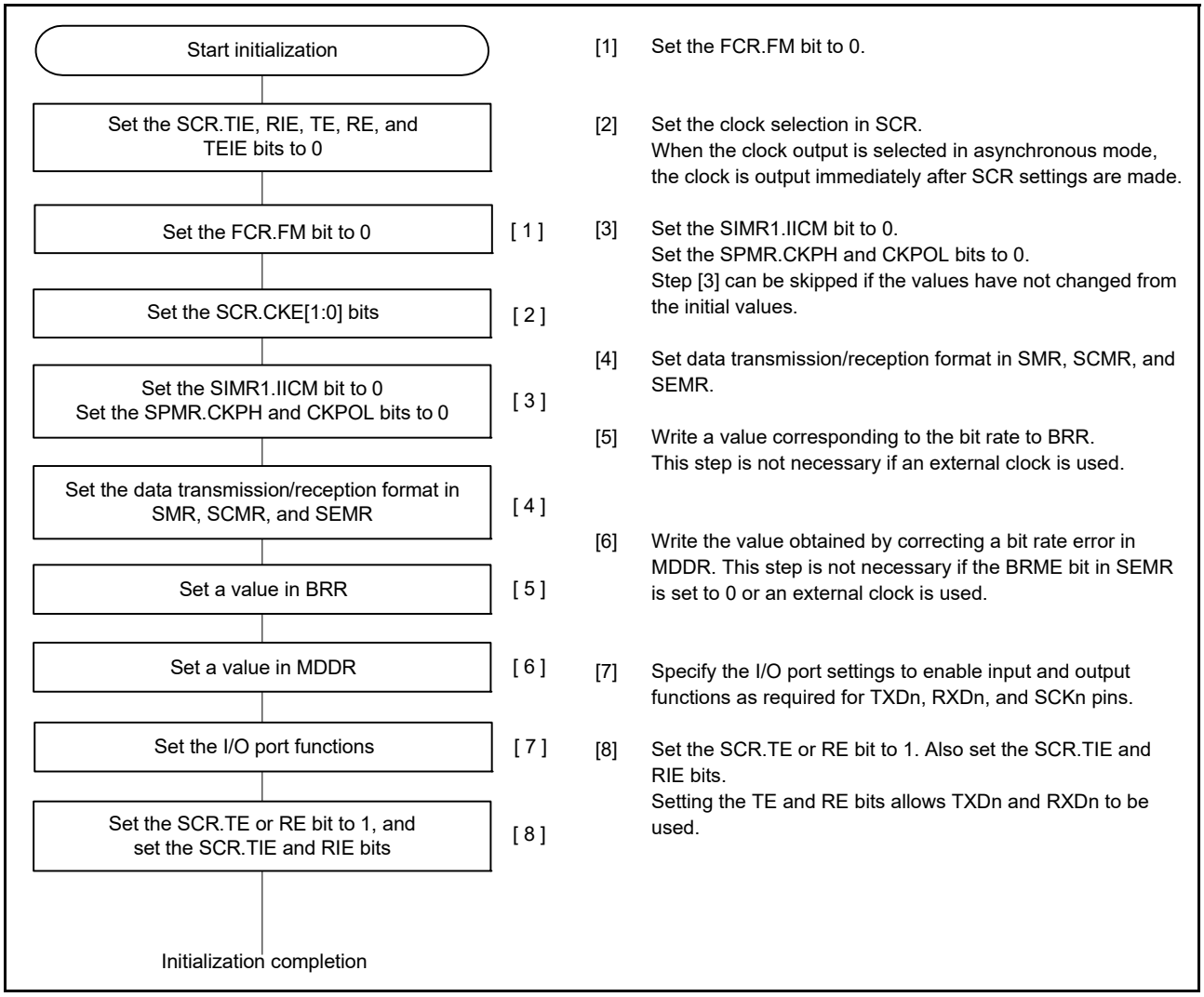


Figure 27.7 Example SCI initialization flow in asynchronous mode with non-FIFO selected

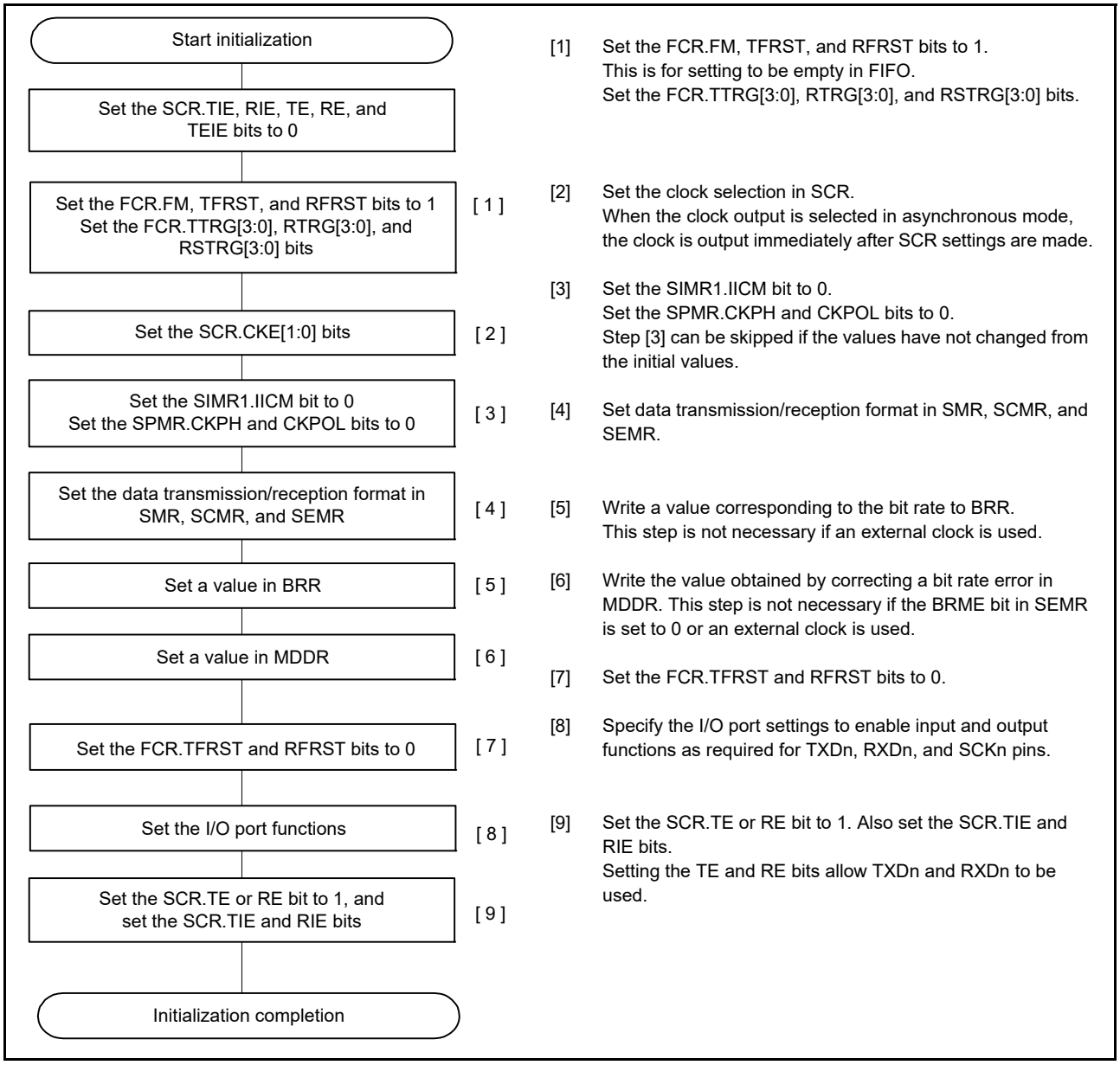


Figure 27.8 Example SCI initialization flow in asynchronous mode with FIFO selected

27.3.8 Serial Data Transmission in Asynchronous Mode

(1) Non-FIFO selected

Figure 27.9, Figure 27.10, and Figure 27.11 show examples of serial transmission in asynchronous mode.

In serial transmission, the SCI operates as described in this section. When the TE bit is set to 1, the high level for one frame (preamble) is output to TXD.

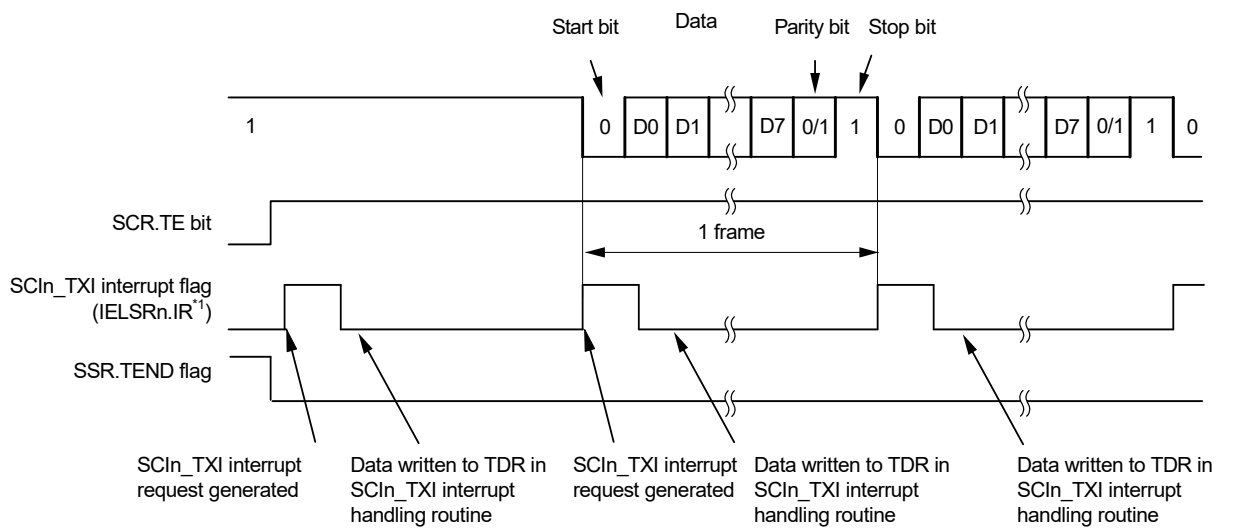
1. The SCI transfers data from TDR*1 to TSR when data is written to TDR*1 in the SCIn_TXI interrupt handling routine.
   The SCIn_TXI interrupt request at the beginning of transmission is generated when the TE and TIE bits in the SCR are set to 1 simultaneously by a single instruction.
2. Transmission starts after the CTSE bit in SPMR is set to 0 (CTS function is disabled) or a low level on the CTSn_RTSn pin causes data transfer from TDR*1 to TSR. If the TIE bit in SCR is 1 at this time, an SCIn_TXI interrupt request is generated. Continuous transmission is possible by writing the next transmit data to TDR*1 in the SCIn_TXI interrupt handling routine before transmission of the current transmit data is complete. When SCIn_TEI

interrupt requests are in use, set the SCR.TIE bit to 0 (an SCIn_TXI interrupt request is disabled) and the SCR.TEIE bit to 1 (an SCIn_TEI interrupt request is enabled) after the last of the data to be transmitted is written to the TDR*1 from the handling routine for SCIn_TXI requests.

3. Data is sent from the TXDn pin in the following order:
   - Start bit
   - Transmit data
   - Parity bit or multi-processor bit (can be omitted depending on the format)
   - Stop bit.
4. The SCI checks for update of the TDR at the time of the output of the stop bit.
5. When TDR is updated, setting the CTSE bit in SPMR to 0 (CTS function is disabled) or a low-level input on the CTSn_RTSn pin cause transfer of the next transmit data from TDR*1 to TSR and transmission of the stop bit, after which serial transmission of the next frame starts.
6. If TDR is not updated, the TEND flag in SSR is set to 1, the stop bit is sent, and the mark state enters where 1 is output. If the TEIE bit in SCR is 1 at this time, the TEND flag in SSR is set to 1 and SCIn_TEI interrupt request is generated.

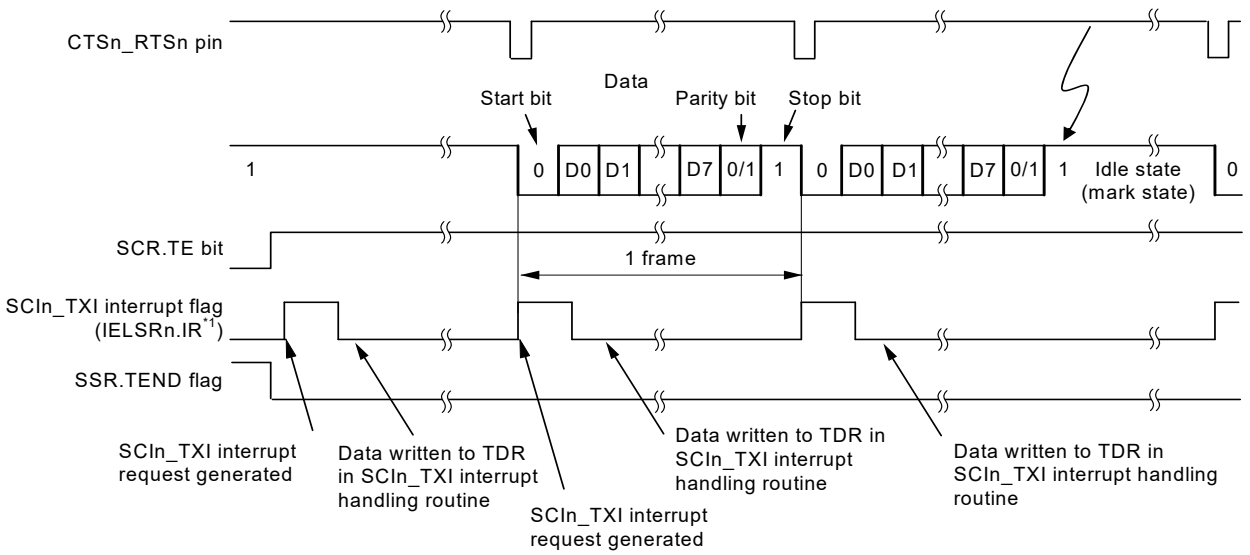
Note 1. Only write data to the TDRHL register when 9-bit data length is selected.

Figure 27.9, Figure 27.10, and Figure 27.11 show a sample flowchart for serial transmission in asynchronous mode.



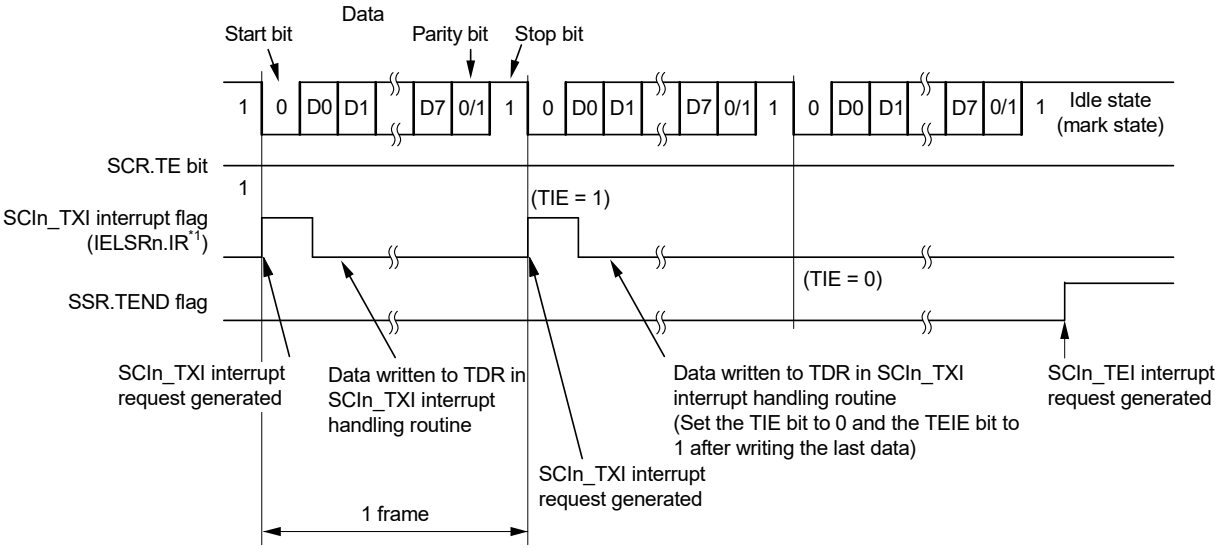
Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 27.9 Example of operation for serial transmission in asynchronous mode (1) with 8-bit data, parity, 1 stop bit, CTS function not used, at the beginning of transmission



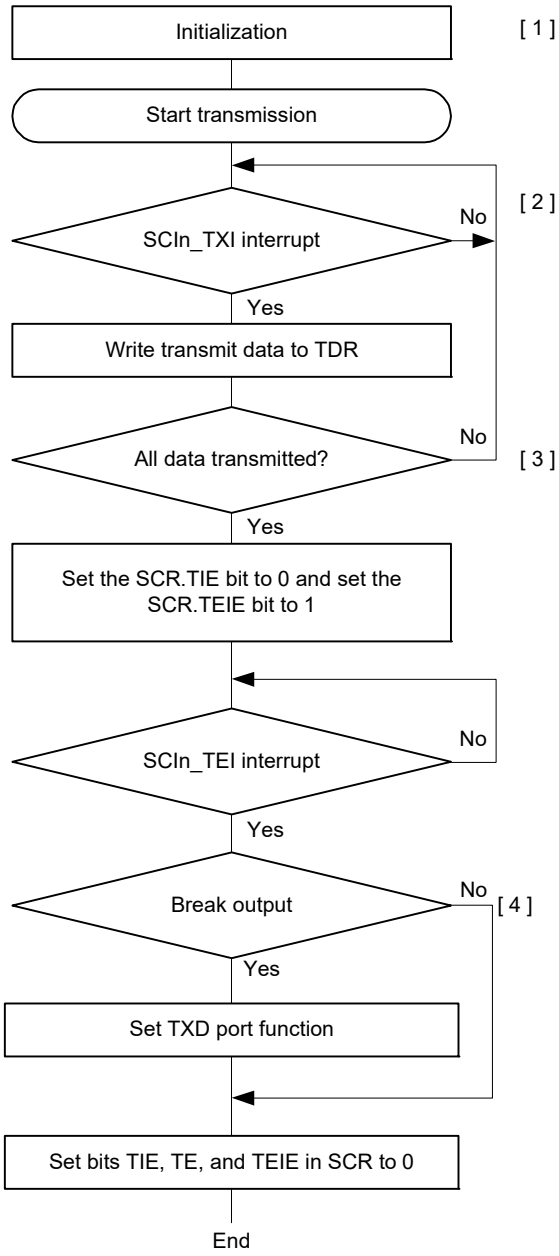
Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 27.10 Example of operation for serial transmission in asynchronous mode (2) with 8-bit data, parity, 1 stop bit, CTS function used, at the beginning of transmission



Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 27.11 Example of operation for serial transmission in asynchronous mode (3) with 8-bit data, parity, 1 stop bit, CTS function not used, from the middle of transmission until transmission completion



[1] SCI Initialization:
Set data transmission.
After the TE bit in SCR is set to 1, 1 is output for a frame (preamble), and transmission is enabled.

[2] Transmit data write to TDR by an SCIn_TXI interrupt request:
When transmit data is transferred from TDR to TSR, a transmit data empty interrupt (SCIn_TXI) request is generated.
Write transmit data to TDR once in the SCIn_TXI interrupt processing routine.

[3] Serial transmission continuation procedure:
To continue serial transmission write transmit data to TDR once using an SCIn_TXI interrupt request.
Transmit data can also be written to TDR by activating the DTC.
When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted are written to the TDR.

[4] Break output at the end of serial transmission:
To output a break in serial transmission, after setting the output state (Low level output) of TXDn pin by SPTR.SPB2IO and SPTR.SPB2DT bits, set the SCR.TE bit to 0.

Note: The TDR register becomes the TDRHL register when 9-bit data length is selected.

Figure 27.12 Example of serial transmission flowchart in asynchronous mode with non-FIFO selected

(2) FIFO selected

Figure 27.13 shows an example of a data format that is written to FTDRH and FTDRL in asynchronous mode.

Data is set to FTDRH and FTDRL that corresponds to the data length. Write 0 for unused bits. Write in the order from FTDRH to FTDRL.

Data Length	Register Setting		Transmit data in FTDRH, FTDRL															
			FTDRHL															
			FTDRH								FTDRL							
	SCMR. CHR1	SMR. CHR	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	—	—	—	—	—	—	—	—	7-bit transmit data						
8 bits	1	1	—	—	—	—	—	—	—	—	8-bit transmit data							
9 bits	0	Don't care	—	—	—	—	—	—	—	9-bit transmit data								

—: Invalid. The write value should be 0.

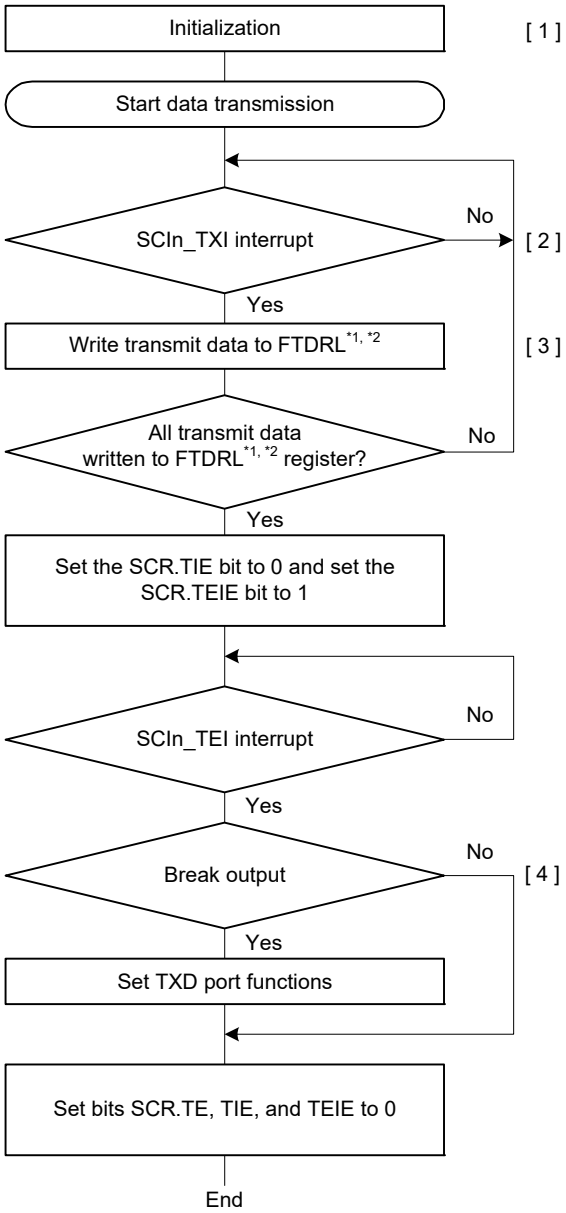
Figure 27.13 Data format written to FTDRH and FTDRL with FIFO selected

In serial transmission, the SCI operates as described in this section. When the TE bit is set to 1, the high level for one frame (preamble) is output to TXD.

1. The SCI transfers data from FTDRL*1 to TSR when data is written to FTDRL*1 in the SCIn_TXI interrupt handling routine.
   The amount of data that can be written to FTDRL is 16 minus FDR.T[4:0] bytes. The SCIn_TXI interrupt request at the beginning of transmission is generated when the TE and TIE bits in the SCR are set to 1 simultaneously by a single instruction.
2. Transmission starts after the CTSE bit in SPMR is set to 0 (CTS function is disabled) and a low level on the CTSn_RTSn pin causes data transfer from FTDRL*1 to TSR. When the amount of transmit data written in FTDRL is equal to or less than the specified transmit triggering number, SSR_FIFO.TDFE is set to 1. If the TIE bit in SCR is 1 at this time, an SCIn_TXI interrupt request is generated. Continuous transmission is possible by writing the next transmit data to FTDRL*1 in the SCIn_TXI interrupt handling routine before transmission of the current transmit data is complete. When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 (an SCIn_TXI interrupt request is disabled) and the SCR.TEIE bit to 1 (an SCIn_TEI interrupt request is enabled) after the last of the data to be transmitted is written to the FTDRL*1 *2 from the handling routine for SCIn_TXI requests.
3. Data is sent from the TXDn pin in the following order:
   a. Start bit
   b. Transmit data
   c. Parity bit or multi-processor bit (can be omitted depending on the format)
   d. Stop bit.
4. The SCI checks whether non-transmitted data remains in FTDRL*3 or not at the time of the stop bit output.
5. When data is set to FTDRL*3, setting of the CTSE bit in SPMR to 0 (CTS function is disabled) or a low-level input on the CTSn_RTSn pin causes transfer of the next transmit data from FTDRL*1 to TSR and transmission of the stop bit, after which serial transmission of the next frame starts.
6. If data is not set in FTDRL*3, the TEND flag in SSR_FIFO is set to 1, the stop bit is sent, and the mark state is entered in which 1 is output. If the TEIE bit in SCR is 1 at this time, the TEND flag in SSR_FIFO is set to 1 and an SCIn_TEI interrupt request is generated.

Note 1. Write data to the FTDRH and FTDRL registers when 9-bit data length is selected.
Note 2. Write data in order from FTDRH to FTDRL when 9-bit data length is selected.
Note 3. The SCI only checks for update to the FTDRL register and not the FTDRH register when 9-bit data length is selected.

Figure 27.14 shows an example flow of serial transmission in asynchronous mode with FIFO selected.



[1] SCI initialization:
Set data transmission.
After the TE bit in SCR is set to 1, 1 is output for a frame (preamble), and transmission is enabled.

[2] Transmit data write to FTDRL*1 by an SCIn_TXI interrupt request:
When transmit data is transferred from FTDRL to TSR, when the amount of transmit data written in FTDRL is equal to or less than the specified transmit triggering number, a transmit data FIFO empty interrupt (SCIn_TXI) request is generated. Write transmit data to FTDRL*1, *2 once in the SCIn_TXI interrupt handling routine.

[3] Serial transmission continuation procedure:
To continue serial transmission, write all transmit data to FTDRL using an SCIn_TXI interrupt request and clear the SSR_FIFO.TDFE flag to 0. The number of transmission data it is possible to write in is 16 - (the number of stored transmit FIFO data).
Transmit data can also be written to FTDRL by activating the DTC. When writing the data to FTDRL by DTC, the TDFE flag is cleared automatically, so do not write to the TDFE flag.
When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted are written to the FTDRL.

[4] Break output at the end of serial transmission:
To output a break in serial transmission, after setting the output state (low-level output) of TXDn pin by SPTR.SPB2IO and SPTR.SPB2DT bits, set the SCR.TE bit to 0.

Note 1. When data length is 9 bits, this refers to FTDRH and FTDRL registers.
Note 2. When data length is 9 bits, write in order from FTDRH to FTDRL.

Figure 27.14 Example flow of serial transmission in asynchronous mode with FIFO selected

27.3.9 Serial Data Reception in Asynchronous Mode

(1) Non-FIFO selected

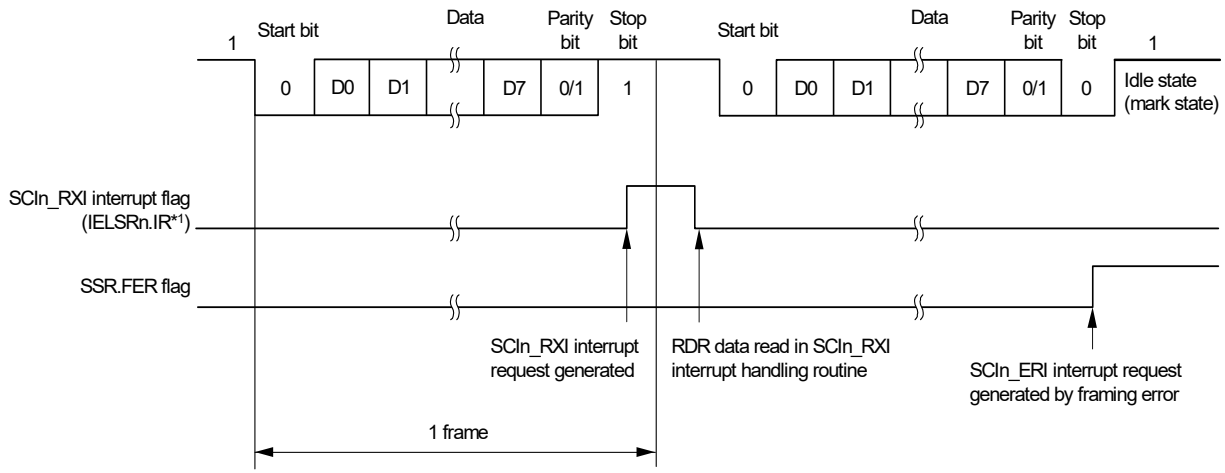
Figure 27.15 and Figure 27.16 show an example of the operation for serial data reception in asynchronous mode.

In serial data reception, the SCI operates as follows:

1. When the value of the RE bit in SCR becomes 1, the output signal on the CTSn_RTSn pin goes low.
2. When the SCI monitors the communications line and detects a start bit, it performs internal synchronization, stores receive data in RSR, and checks the parity bit and stop bit.
3. If an overrun error occurs, the ORER flag in SSR is set to 1. If the RIE bit in SCR is 1, an SCIn_ERI interrupt request is generated. Receive data is not transferred to RDR*1.
4. If a parity error is detected, the PER bit in SSR is set to 1 and receive data is transferred to RDR*1. If the RIE bit in SCR is 1, an SCIn_ERI interrupt request is generated.

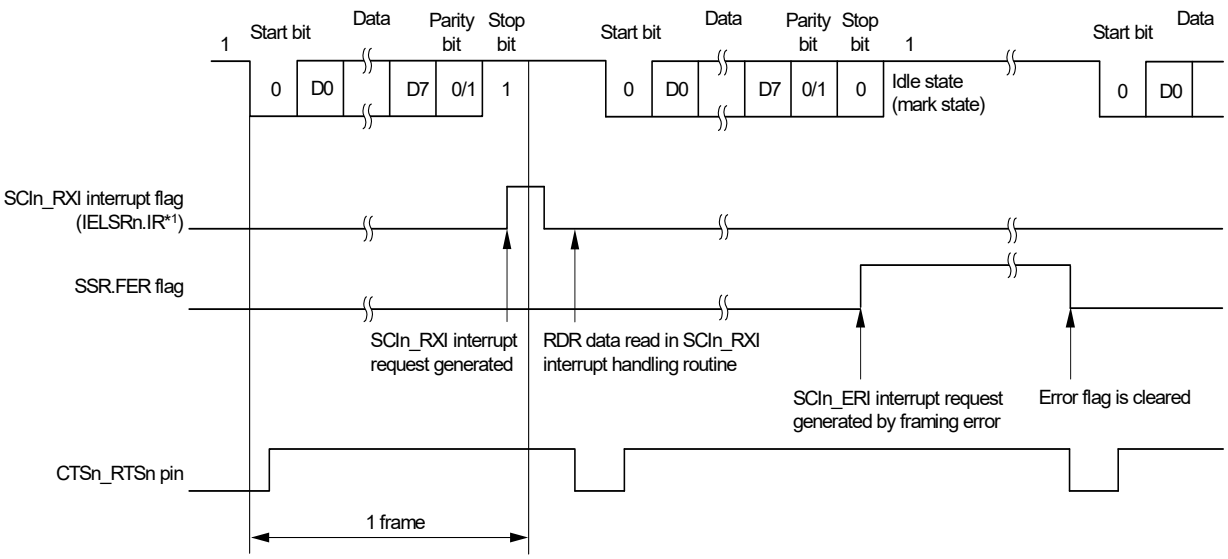
5. If a frame error is detected, the FER bit in the SSR is set to 1 and receive data is transferred to RDR*1. If the RIE bit in the SCR is 1, an SCIn_ERI interrupt request is generated.
6. When reception finishes successfully, receive data is transferred to RDR*1. If the RIE bit in the SCR is 1, an SCIn_RXI interrupt request is generated. Continuous reception is enabled by reading the receive data transferred to RDR in this SCIn_RXI interrupt handling routine before reception of the next receive data completes. Reading the received data that is transferred to RDR causes the CTSn_RTSn pin to output low.

Note 1. Only read data in the RDRHL register when 9-bit data length is selected.



Note 1. See section 12, Interrupt Controller Unit (ICU) for details on the associated interrupt event number.

Figure 27.15 Example of SCI operation with 8-bit data, parity, and 1 stop bit for serial reception in asynchronous mode (1) when RTS function is not used



Note 1. See section 12, Interrupt Controller Unit (ICU) for details on the associated interrupt event number.

Figure 27.16 Example of SCI operation with 8-bit data, parity, and 1 stop bit for serial reception in asynchronous mode (2) when RTS function is used

Table 27.24 lists the states of the flags in the SSR status register and receive data handling when a receive error is detected.

If a receive error is detected, an SCIn_ERI interrupt request is generated but an SCIn_RXI interrupt request is not generated. Data reception cannot be resumed while the receive error flag is 1. Accordingly, set the ORER, FER, and PER bits to 0 before resuming reception. In addition, be sure to read the RDR or the RDRHL during overrun error processing. When a reception is forced to terminate by setting the SCR.RE bit to 0 during operation, read the RDR or RDRHL register because received data that is not read might be left in the RDR or RDRHL.

Figure 27.17 and Figure 27.18 show example flows for serial data reception.

Table 27.24 Flags in SSR Status Register and receive data handling

Flags in the SSR Status Register				
ORER	**FER**	**PER**	**Receive data**	**Receive error type**
1	0	0	Lost	Overrun error
0	1	0	Transferred to RDR*1	Framing error
0	0	1	Transferred to RDR*1	Parity error
1	1	0	Lost	Overrun error + framing error
1	0	1	Lost	Overrun error + parity error
0	1	1	Transferred to RDR*1	Framing error + parity error
1	1	1	Lost	Overrun error + framing error + parity error

Note 1. Only read data in the RDRHL register when 9-bit data length is selected.

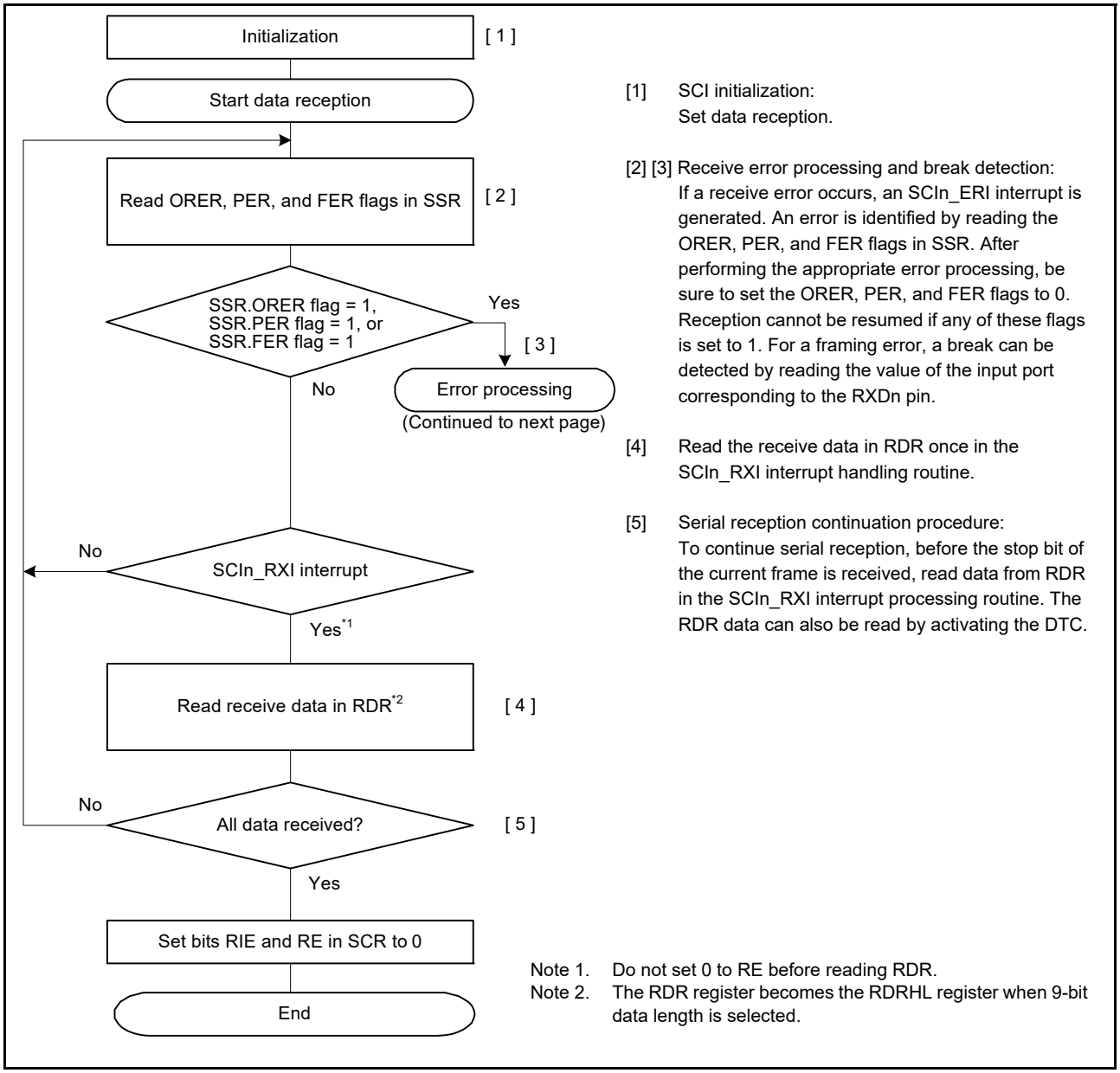


Figure 27.17 Example flow of serial reception in asynchronous mode with non-FIFO selected (1)

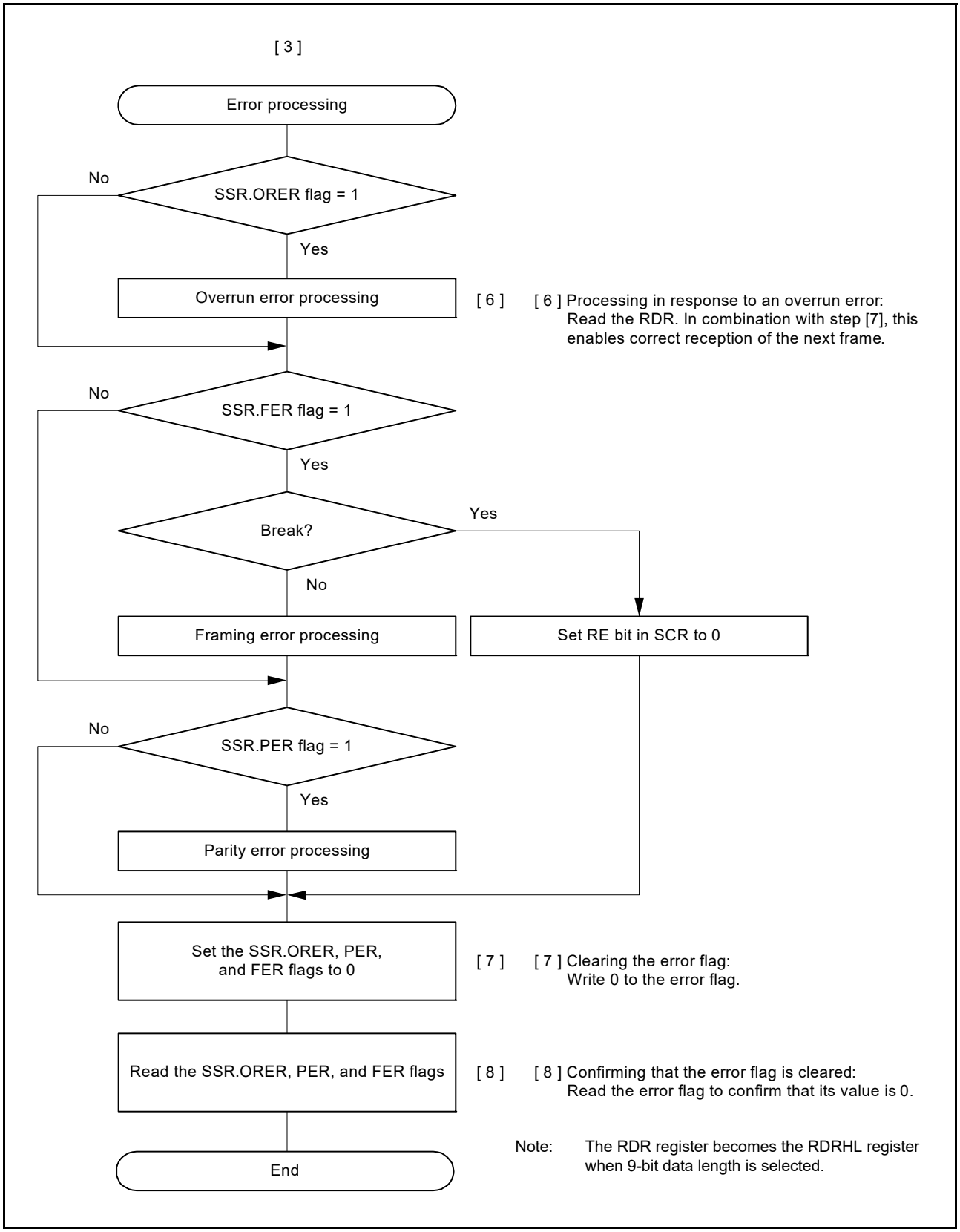


Figure 27.18 Example flow of serial reception in asynchronous mode with non-FIFO selected (2)

(2) FIFO selected

Figure 27.19 shows an example of a data format that is written to FRDRH and FRDRL in asynchronous mode.

In asynchronous mode, 0 is written to the MPB flag in FRDRH. Data that corresponds to the data length is written to FRDRH and FRDR. Unused bits are written as 0. Read in order from FRDRH to FRDRL. If software reads FRDRL, SCI updates FER, PER and receive data (RDAT[8:0]) in FRDRL with the next data. The RDF, ORER, and DR flags in FRDRH always reflect the corresponding flags in the SSR_FIFO register.

Data Length	Register Setting		Receive data in FRDRH, FRDRL															
			FRDRHL															
			FRDRH								FRDRL							
	SCMR. CHR1	SMR. CHR	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	RDF	ORER	FER	PER	DR	0	0	0	7-bit receive data						
8 bits	1	1	—	RDF	ORER	FER	PER	DR	0	0	8-bit receive data							
9 bits	0	Don't care	—	RDF	ORER	FER	PER	DR	0	9-bit receive data								

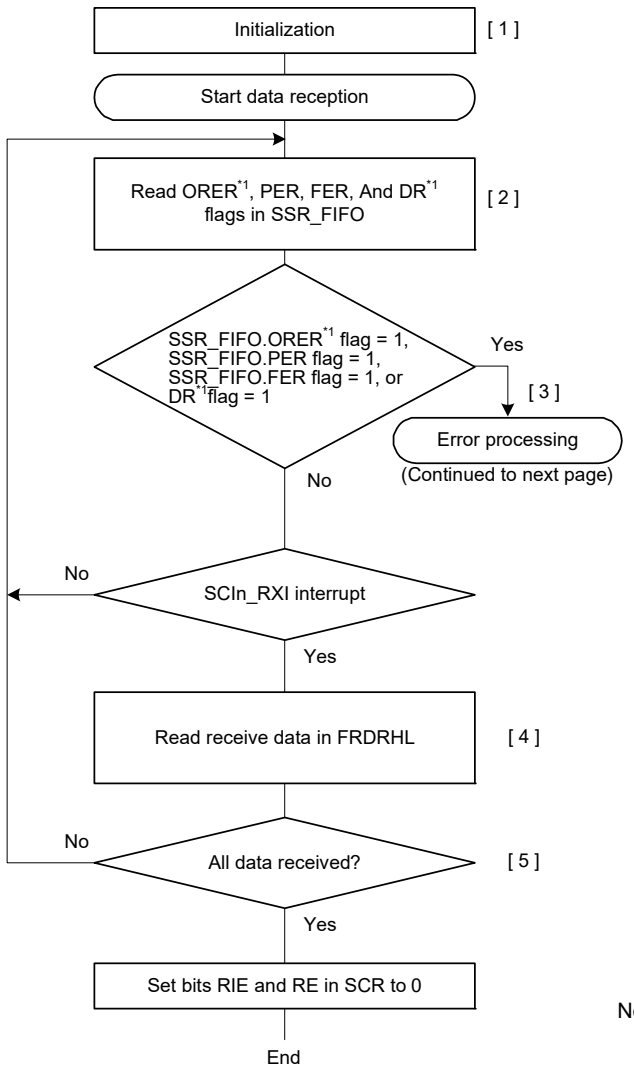
Note: 0 is always read for MPB flag (FRDRH[1])
When data length is 7 bits, 0 is always read for FRDRH[0] and FRDRL[7]
When data length is 8 bits, 0 is always read for FRDRH[0]
FRDRH[7] bit is read as an indefinite value.

Figure 27.19 Data format stored in FRDRH and FRDRL with FIFO selected

In serial data reception, the SCI operates as follows:

1. When the value of the RE bit in SCR becomes 1, the output signal on the CTSn_RTSn pin goes low.
2. When the SCI monitors the communications line and detects a start bit, it performs internal synchronization, stores receive data in RSR, and checks the parity bit and stop bit.
3. If an overrun error occurs, the ORER flag in SSR_FIFO is set to 1. When the RIE bit in SCR is 1, an SCIn_ERI interrupt request is generated. Receive data is not transferred to FRDRL*1.
4. If a parity error is detected, the PER flag and receive data are transferred to FRDRL*1. When the RIE bit is set to 1, an SCIn_ERI interrupt request is generated.
5. If a frame error is detected, the FER flag and receive data are transferred to FRDRL*1. When a RIE bit is set to 1, an SCIn_ERI interrupt request is generated.
6. After a frame error is detected and when SCI detects that the continuous receive data is for one frame, reception stops.
7. When the amount of data stored in the receive FIFO data register (FRDRL) falls below the specified receive triggering number, and the next data has not been received after the elapse of 15 ETUs from the last stop bit in asynchronous mode, SSR_FIFO.DR is set to 1. When the RIE bit is 1 and the FCR.DRES bit is 0, SCI generates an SCIn_RXI interrupt request. When the FCR.DRES bit is 1, SCI generates an SCIn_ERI interrupt request.
8. When reception finishes successfully, receive data is transferred to FRDRL*1. RDF is set to 1 when the amount of receive data written to FRDRHL is equal to or greater than the specified receive triggering number. When the RIE bit in SCR is 1, an SCIn_RXI interrupt request is generated. Continuous reception is enabled by reading the receive data transferred to FRDRL*2 in this SCIn_RXI interrupt handling routine, before an overrun error occurs. If the received data that is transferred to FRDRL*3 is less than the RTS trigger number, the CTSn_RTSn pin outputs low.

Note 1. Only read data in the FRDRH and FRDRL registers when 9-bit data length is selected.
Note 2. Read data in order from FRDRH to FRDRL when 9-bit data length is selected.
Note 3. The SCI only checks for update to the FRDRL register and not to the FRDRH register when 9-bit data length is selected.



[1] SCI initialization:
Set data reception.

[2] [3] Receive error processing and break detection:
If a receive error occurs, an SCIn_ERI interrupt is generated. A break can be detected by reading the SPTR.RXDMON bit. An error is identified by reading the ORER*1, PER, DR*1, and FER flags in SSR_FIFO. After performing the appropriate error processing, be sure to set the ORER*1 flag to 0. Reception cannot be resumed if ORER*1 flag is set to 1. The reception operation is continuous, even when FER = 1 or PER = 1 or DR*1 = 1.

[4] Read the receive data in FRDRHL in the SCIn_RXI interrupt handling routine. The reception data stored in the FRDRHL register is read until the number of stored data is at least below the FCR.RTRG value. Confirm the number of the reception data in the FIFO with the FDR.R bits.

[5] Serial reception continuation procedure:
To continue serial reception, before an overrun error occurs, read data from FRDRHL in the SCIn_RXI interrupt handling routine and clear RDF flag and DR flag to 0.
The FRDRHL data can also be read by activating the DTC. The RDF flag is cleared automatically in this case, so do not write to the RDF flag.

Note 1. Can be read by the FRDRHL.ORER and DR flags.

Figure 27.20 Example flow of serial reception in asynchronous mode with FIFO selected (1)

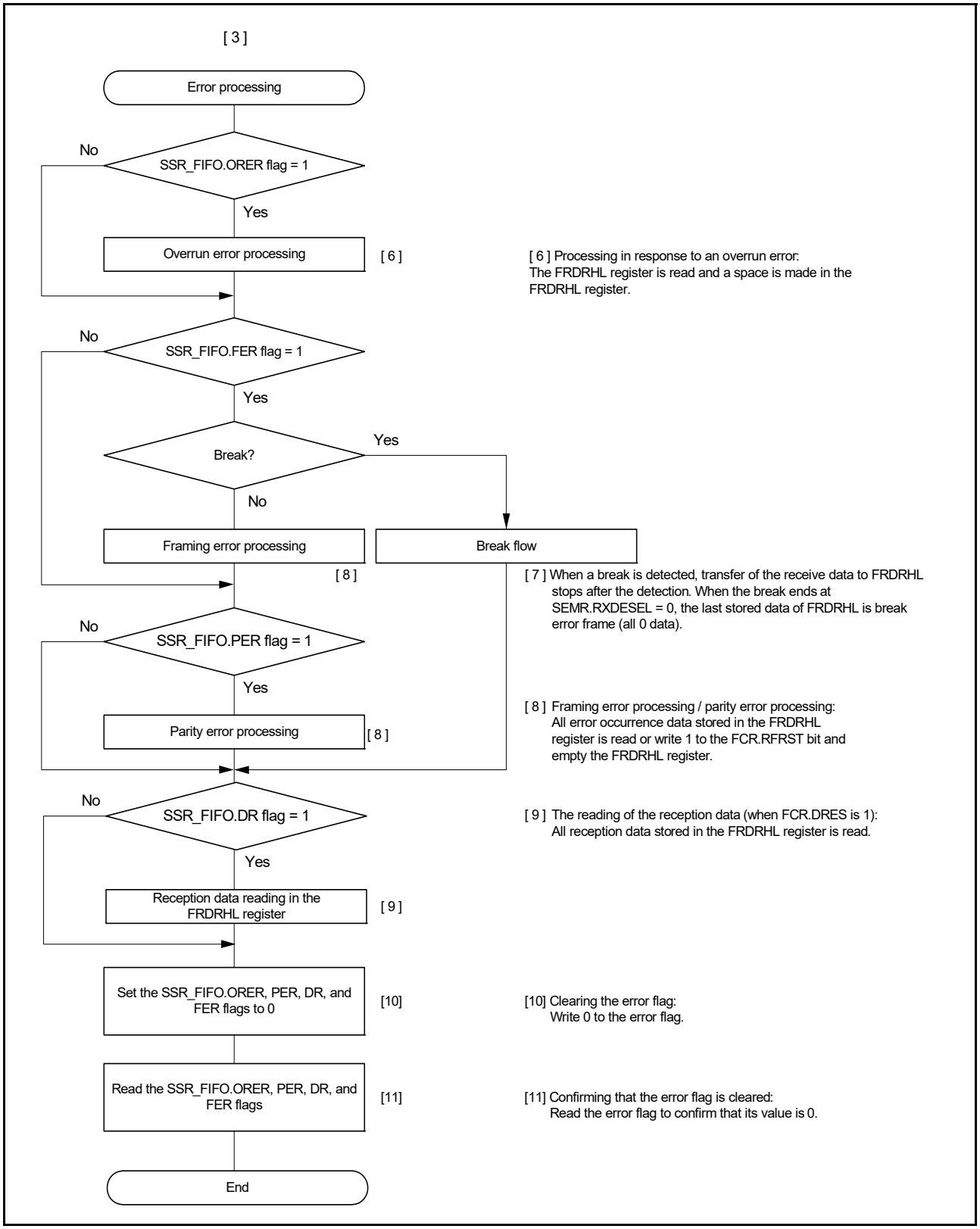


Figure 27.21 Example flow of serial reception in asynchronous mode with FIFO selected (2)

27.4 Multi-Processor Communications Function

The multi-processor communication function enables the SCI to transmit and receive data between multiple processors by sharing an asynchronous serial communication line that has an added multiple-processor bit. In multi-processor

communication, a unique ID code is allocated to each receiving station. Serial communication cycles consist of an ID transmission cycle to specify the receiving station and a data transmission cycle to transmit data to the specified receiving station.

The multi-processor bit is used to distinguish between the ID transmission cycle and the data transmission cycle:

- When the multi-processor bit is set to 1, the transmission cycle is the ID transmission cycle
- When the multi-processor bit is set to 0, the transmission cycle is the data transmission cycle.

Figure 27.22 shows an example of communication between processors using a multi-processor format. First, a transmitting station transmits communication data in which the multi-processor bit set to 1, is added to the ID code of the receiving station. Next, the transmitting station transmits communication data in which the multi-processor bit set to 0, is added to the transmit data. After receiving communication data with the multi-processor bit set to 1, the receiving station compares the received ID with the ID of the receiving station itself. If the two match, the receiving station receives communication data that is subsequently transmitted. If the received ID does not match with the ID of the receiving station, the receiving station skips the communication data until it receives the data again in which the multi-processor bit is set to 1.

(1) Non-FIFO selected

To support this function, the SCI provides the MPIE bit in the SCR. When the MPIE bit is set to 1, the following are disabled until the reception of data in which the multi-processor bit is set to 1:

- Transfer of receive data from the RSR to the RDR (the RDRHL register when 9-bit data length is selected)
- Detection of a receive error
- Setting of the respective status flags RDRF, ORER and FER in SSR.

On receiving a reception character in which the multi-processor bit is set to 1, the MPBT bit in SSR is set to 1 and the MPIE bit in SCR is automatically cleared, therefore returning to a non multi-processor reception operation. During this time, an SCIn_RXI interrupt is generated if the RIE bit in SCR is set.

When the multi-processor format is specified, specification of the parity bit is disabled. Apart from this, there is no difference from operation in non multi-processor asynchronous mode. The clock used for the multi-processor communication is the same as the clock used in non multi-processor asynchronous mode.

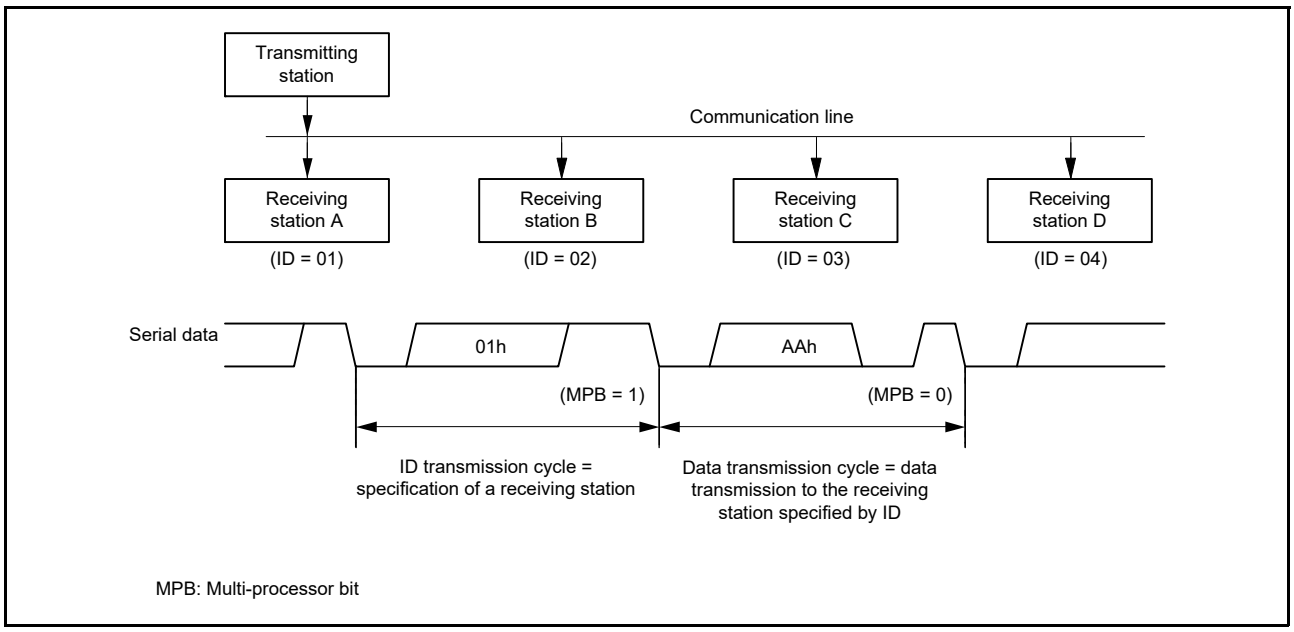


Figure 27.22 Example of communication using multi-processor format for transmission of data AAh to receiving station A

(2) FIFO selected

For data transmission, software must write data to FTDRHL.MPBT that corresponds to transmit data in FTDRHL.TDAT. For data reception, the multi-processor bit that is part of the receive data is written to FRDRHL.MPB and receive data is written to FRDRL.

When the MPIE bit is set to 1, the following are disabled until reception of data in which the multi-processor bit is set to 1:

- Transfer of receive data from RSR to FRDRHL
- Detection of a receive error
- Break
- Setting of the respective RDF, ORER, and FER status flags in SSR_FIFO.

On receiving an 8-bit character in which the multi-processor bit is set to 1, the MPB bit in FRDRHL is set to 1 and receive data is written to FRDRHL.RDAT. The MPIE bit in SCR is automatically cleared, therefore returning to non multi-processor reception operation. During this time, an SCIn_RXI interrupt is generated if the RIE bit in SCR is set.

When the multi-processor format is specified, specification of the parity bit is disabled. Apart from this, there is no difference from operation in non multi-processor asynchronous mode and non-FIFO selected.

27.4.1 Multi-Processor Serial Data Transmission

(1) Non-FIFO selected

Figure 27.23 shows an example flow of multi-processor data transmission. In the ID transmission cycle, the ID must be transmitted with the MPBT bit in the SSR set to 1. In the data transmission cycle, the data must be transmitted with the MPBT bit set to 0. The rest of the operations are the same as operations in asynchronous mode.

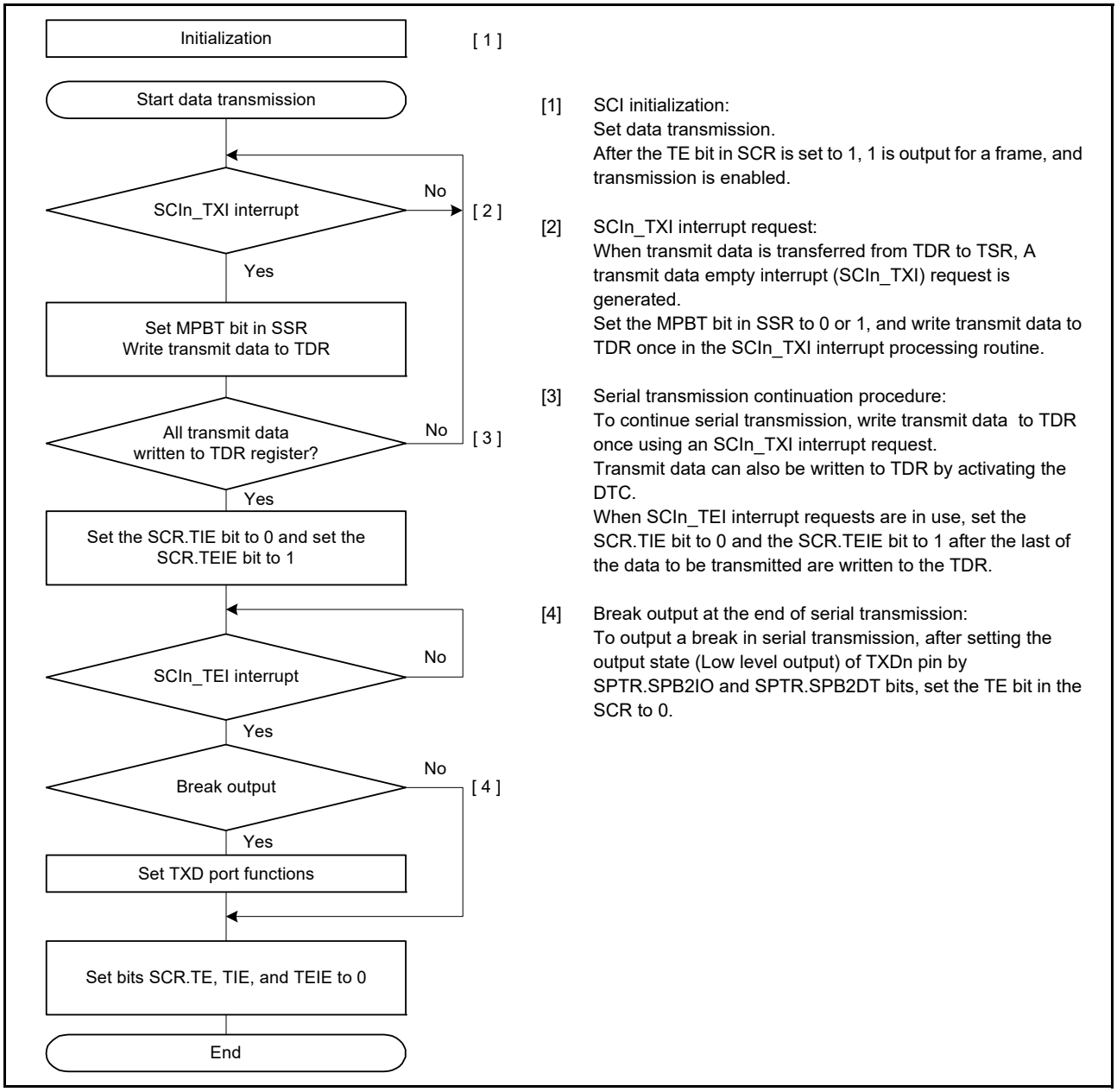


Figure 27.23 Example flow of multi-processor serial transmission with non-FIFO selected

(2) FIFO selected

Figure 27.24 shows an example of data format that is written to FTDRH and FTDRL in multi-processor mode.

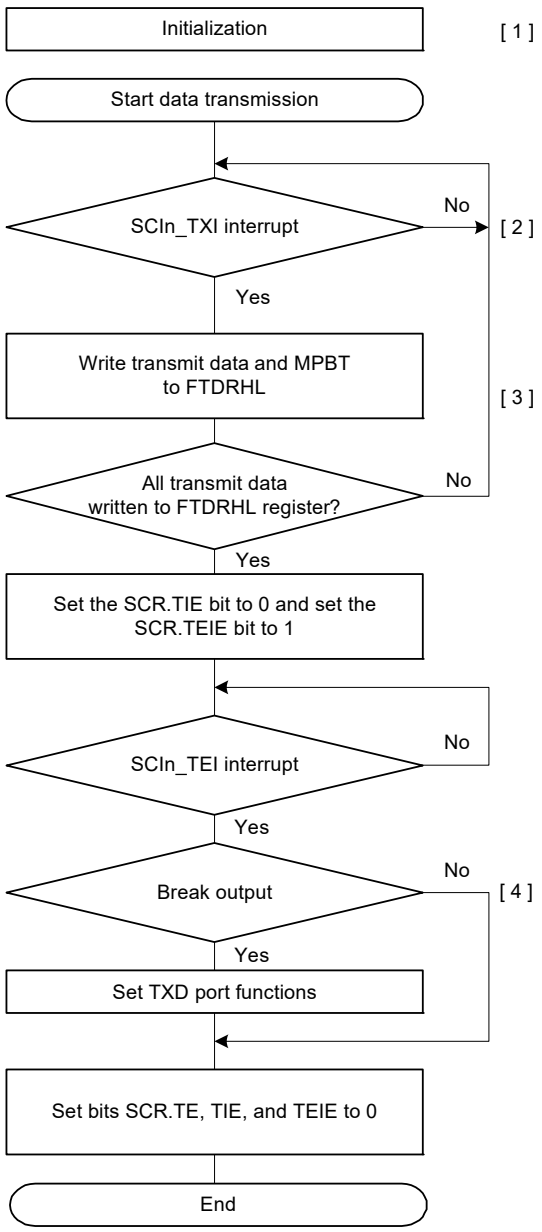
MPBT is set to 1 in FTDRH. Data is set to FTDRH and FTDRL associated with the data length. Write 0 for unused bits. Write in order from FTDRH to FTDRL.

Data Length	Register Setting		Transmit data in FTDRH, FTDRL															
			FTDRHL															
			FTDRH								FTDRL							
	SCMR. CHR1	SMR. CHR	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	—	—	—	—	—	MPBT	—	—	7-bit transmit data						
8 bits	1	1	—	—	—	—	—	—	MPBT	—	8-bit transmit data							
9 bits	0	Don't care	—	—	—	—	—	—	MPBT	9-bit transmit data								

—: Invalid. The write value should be 0.

Figure 27.24 Data format written to FTDRH and FTDRL in multi-processor mode with FIFO selected

Figure 27.25 shows an example flow for multi-processor data transmission with FIFO selected. In the ID transmission cycle, the ID must be transmitted with the MPBT bit in FTDRH set to 1. In the data transmission cycle, the data must be transmitted with the MPBT bit set to 0. The rest of the operations are the same as operations in asynchronous mode with non-FIFO selected.



[1] SCI initialization:
Set data transmission.
After the TE bit in SCR is set to 1, 1 is output for a frame, and transmission is enabled.

[2] Transmit data write to FTDRHL by an SCIn_TXI interrupt request:
When transmit data is transferred from FTDRHL to TSR, when the amount of receive data written in FTDRHL is equal to or less than the specified transmit triggering number, a transmit data FIFO empty interrupt (SCIn_TXI) request is generated.

[3] Serial transmission continuation procedure:
To continue serial transmission, write transmit data and MPBT to FTDRHL once using an SCIn_TXI interrupt request.
Transmit data can also be written to FTDRHL by activating the DTC.
When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted are written to the FTDRHL.

[4] Break output at the end of serial transmission:
To output a break in serial transmission, after setting the output state (Low level output) of TXDn pin by SPTR.SPB2IO and SPTR.SPB2DT bits, set the TE bit in the SCR to 0.

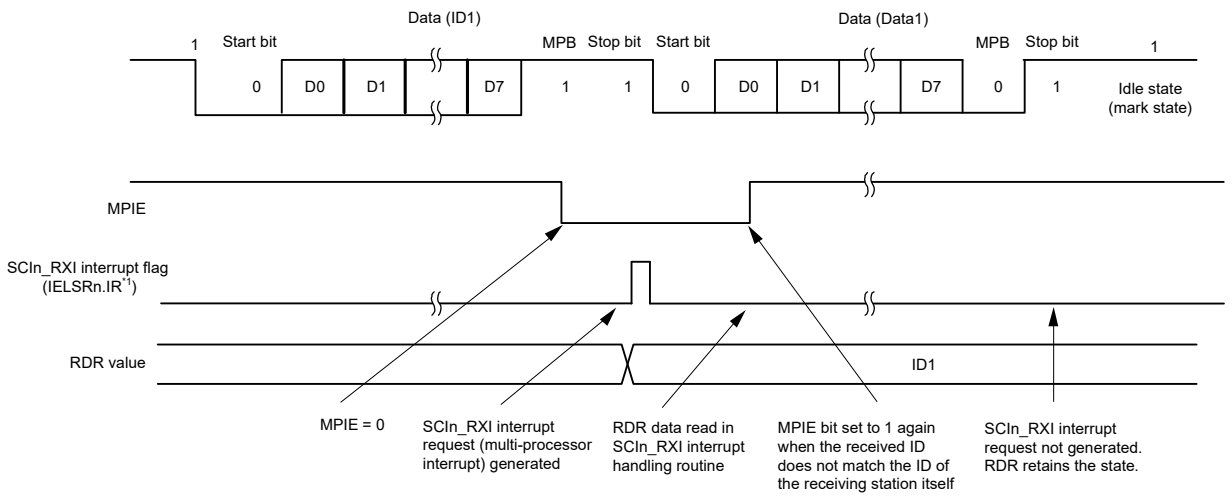
Figure 27.25 Example flow of serial transmission in multi-processor mode with FIFO selected

27.4.2 Multi-Processor Serial Data Reception

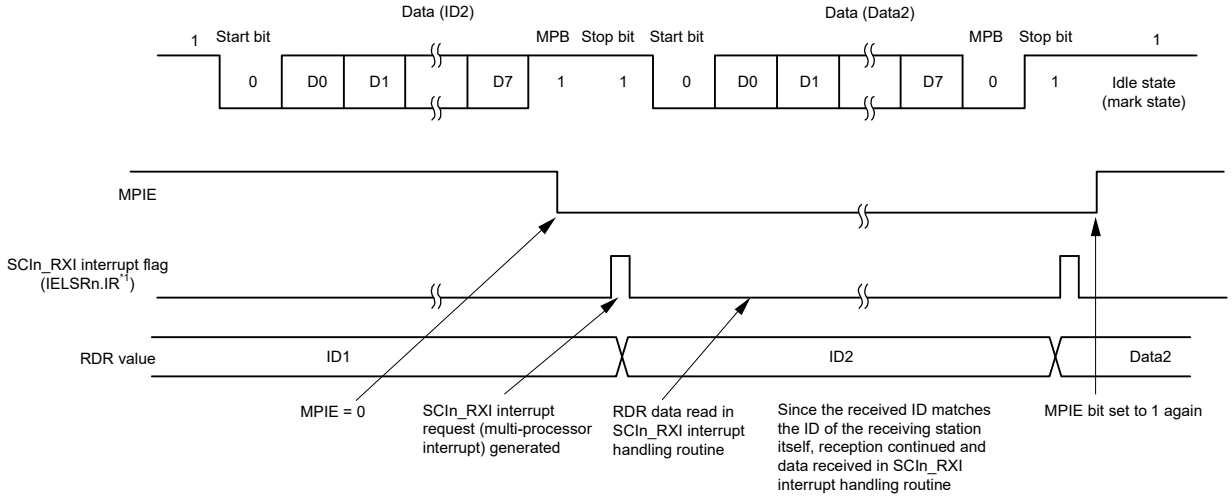
(1) Non-FIFO selected

Figure 27.27 and Figure 27.28 are example flows of multi-processor data reception. When the MPIE bit in SCR is set to 1, reading communication data is skipped until reception of communication data in which the multi-processor bit is set to 1. When communication data in which the multi-processor bit is set to 1 is received, the received data is transferred to RDR (the RDRHL register when 9-bit data length is selected). During this time, the SCIn_RXI interrupt request is generated. The rest of the operations are the same as operations in asynchronous mode.

Figure 27.26 shows an example operation for data reception.



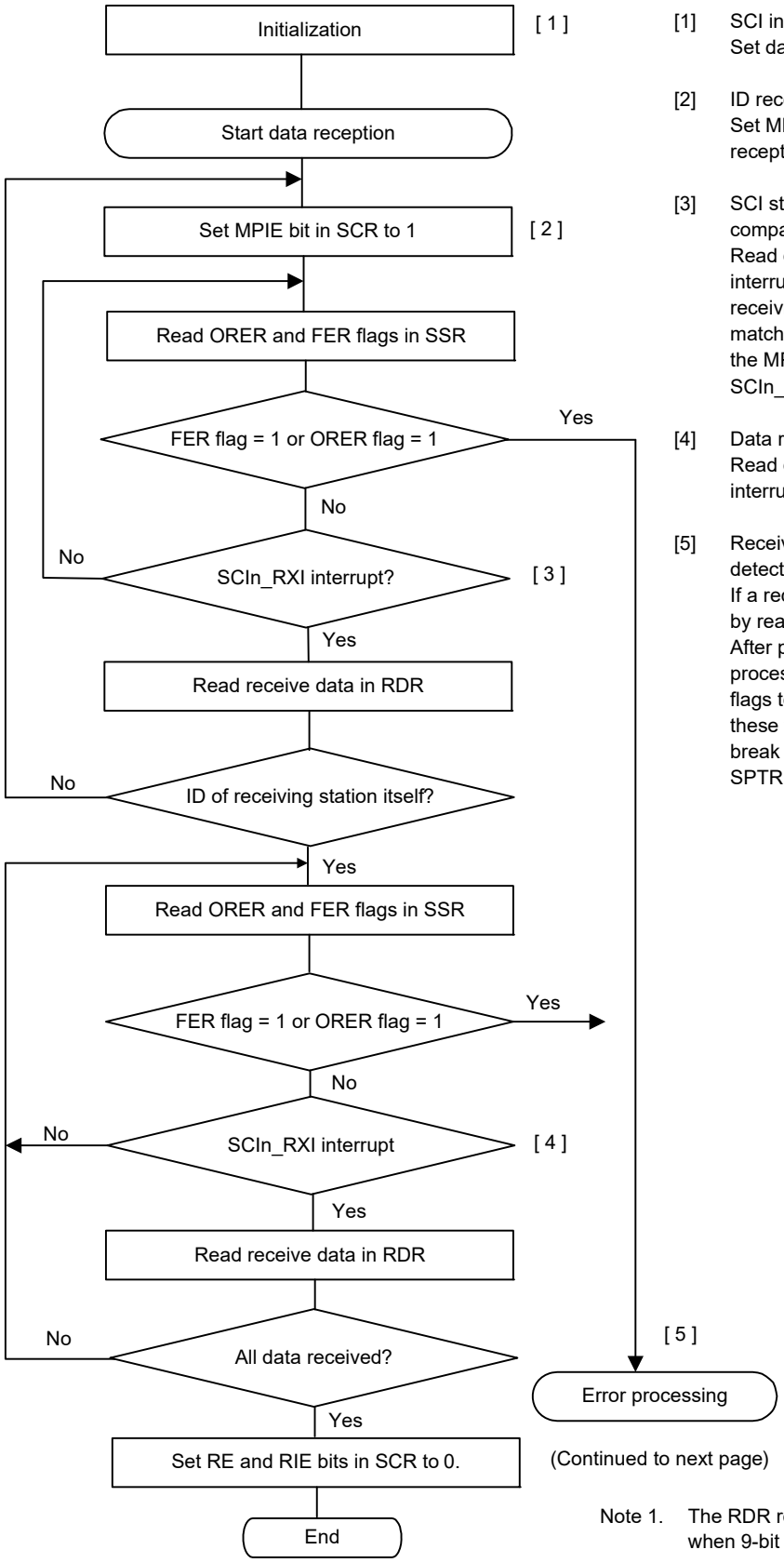
(a) When the received ID does not match the ID of the receiving station itself



(b) When the received ID matches the ID of the receiving station itself

Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 27.26 Example of SCI reception with 8-bit data, multi-processor bit, and 1 stop bit



[1] SCI initialization:
Set data reception.

[2] ID reception cycle:
Set MPIE bit in SCR to 1 and wait for ID reception.

[3] SCI status confirmation and reception and comparison of ID:
Read data in RDR*1 at the first SCIn_RXI interrupt and compare it with the ID of the receiving station itself. If the ID does not match the ID of the receiving station itself, set the MPIE bit to 1 again, and wait for another SCIn_RXI interrupt request.

[4] Data reception at an SCIn_RXI interrupt:
Read data in RDR*1 once in the SCIn_RXI interrupt routine.

[5] Receive error processing and break detection:
If a receive error occurs, an error is identified by reading ORER and FER flags in SSR. After performing the appropriate error processing be sure to set ORER and FER flags to 0. Reception cannot resume if any of these flags is set to 1. For a framing error, a break can be detected by reading SPTR.RXDMON bit.

(Continued to next page)

Note 1. The RDR register becomes the RDRHL register when 9-bit data length is selected.

Figure 27.27 Example flow of multi-processor serial reception with non-FIFO selected (1)

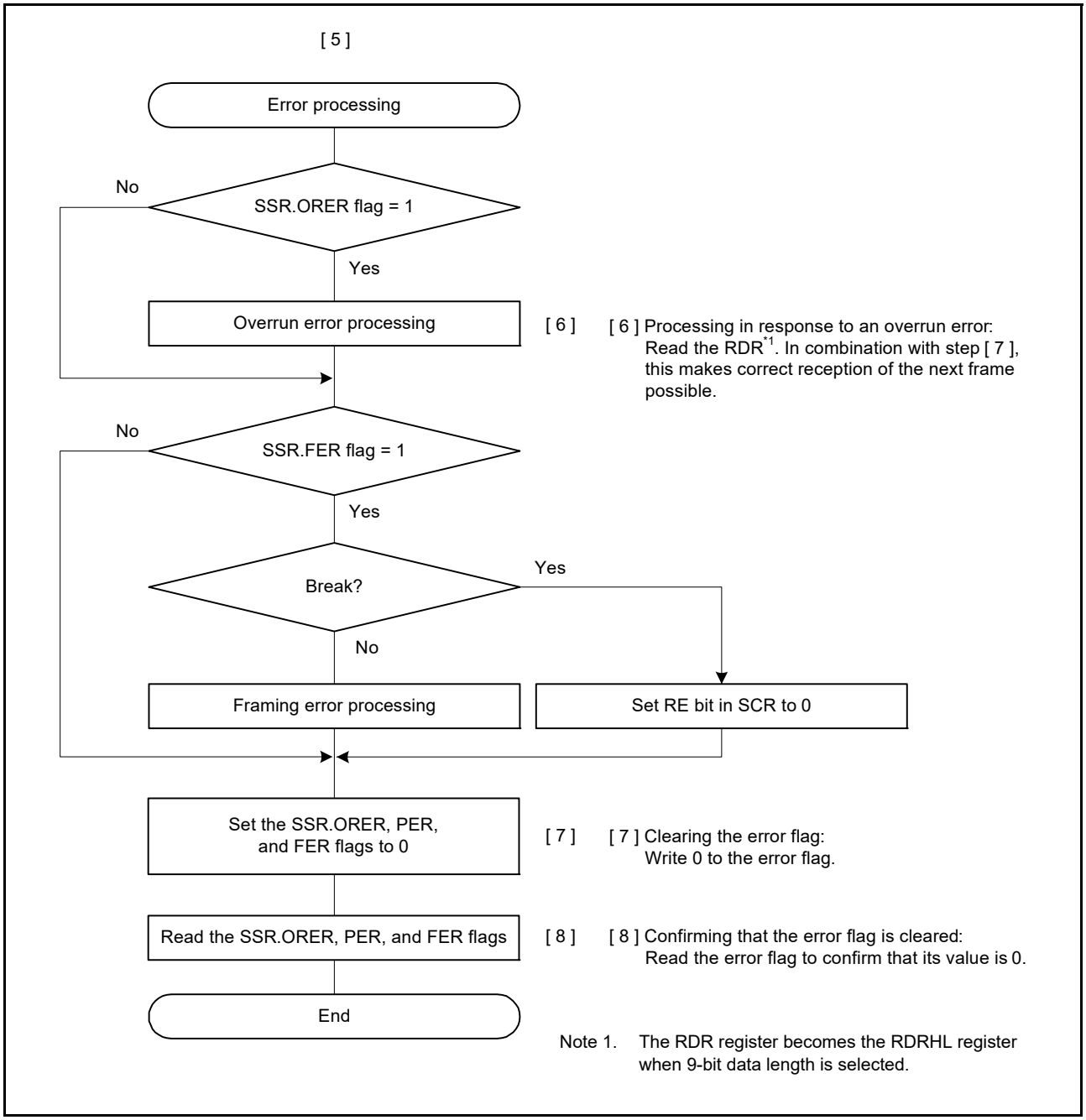


Figure 27.28 Example flow of multi-processor serial reception with non-FIFO selected (2)

(2) FIFO selected

Figure 27.29 shows an example of a data format that is written to FRDRH and FRDRL in multi-processor mode.

In multi-processor mode, the MPB value that is a part of the receive data is written to the MPB flag (FRDRH[1]) in FRDRH. A value of 0 is written to the PER flag (FRDRH[3]) in FRDRH. Data is written to FRDRH and FRDRL associated with the data length. Unused bits are written with 0. Read in order from FRDRH to FRDRL. If software reads FRDRL, SCI updates FER, MPB and receive data (RDAT[8:0]) in FRDRL with the next data. The flags RDF, ORER and DR in FRDRH always reflect the associated flags in the SSR_FIFO register.

Data Length	Register Setting		Receive data in FRDRH, FRDRL															
			FRDRHL															
			FRDRH								FRDRL							
	SCMR. CHR1	SMR. CHR	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	RDF	ORER	FER	0	DR	MPB	0	0	7-bit receive data						
8 bits	1	1	—	RDF	ORER	FER	0	DR	MPB	0	8-bit receive data							
9 bits	0	Don't care	—	RDF	ORER	FER	0	DR	MPB	9-bit receive data								

Note: When data length is 7 bits, 0 is always read for FRDRH[0] and FRDRL[7].
When data length is 8 bits, 0 is always read for FRDRH[0].
FRDRH[7] bit is read as an indefinite value.

Figure 27.29 Data format stored to FRDRH and FRDRL in multi-processor mode with FIFO selected

Figure 27.30 shows an example flow for multi-processor data reception with FIFO selected. When the MPIE bit in SCR is set to 1, reading communication data is skipped until reception of communication data in which the multi-processor bit is set to 1. When communication data in which the multi-processor bit is set to 1 is received, the received data, MPB and associated errors are transferred to FRDRHL. The MPIE bit in SCR is automatically cleared, and non multi-processor reception continues.

If a frame error occurs and the SSR_FIFO.FER flag is set to 1, SCI continues data reception. The rest of the operations are the same as those in asynchronous mode with non-FIFO selected.

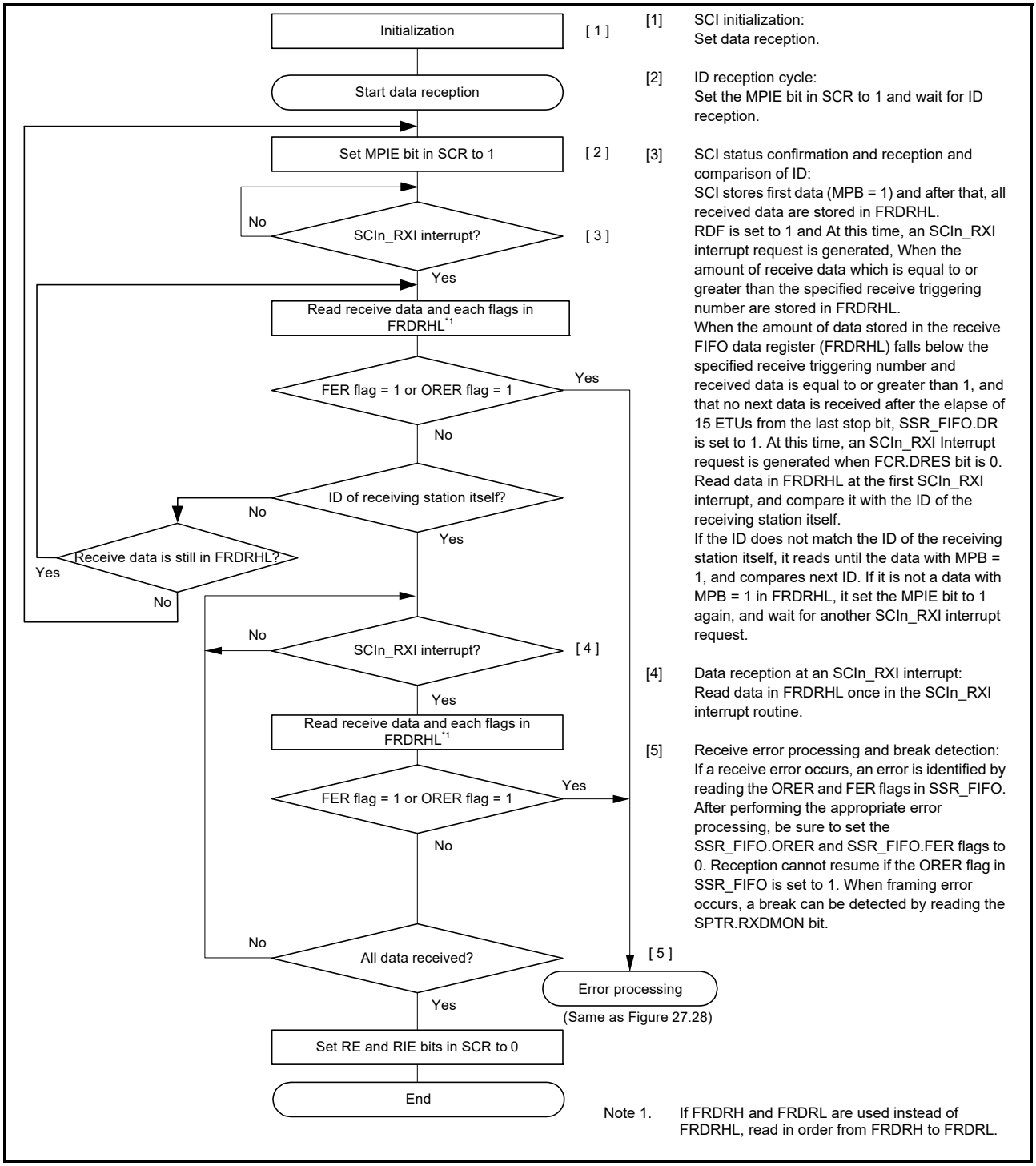


Figure 27.30 Example flow of serial reception in multi-processor mode with FIFO selected

27.5 Operation in Clock Synchronous Mode

Figure 27.31 shows the data format for clock synchronous serial data communications.

In clock synchronous mode, data is transmitted or received in synchronization with clock pulses. One character in transfer data consists of 8-bit data. In clock synchronous mode, no parity bit can be added.

In data transmission, the SCI outputs data from one falling edge of the synchronization clock to the next. In data reception, the SCI receives data in synchronization with the rising edge of the synchronization clock. After 8-bit data is output, the transmission line holds the last bit as output state. When SPMR.CKPH is 1 in slave mode, it holds the first bit output state.

Within the SCI, the transmitter and receiver are independent units, enabling full-duplex communications by using a common clock. Both the transmitter and the receiver also have a double-buffered structure, so that the next transmit data can be written during transmission or the previous receive data can be read during reception, enabling continuous data transfer.

However, it is not possible to do continuous transfer in the fastest bit rate setting (BRR = 00h and SMR.CKS[1:0] = 00b), therefore when the FIFO is selected, this setting (BRR = 00h and SMR.CKS[1:0] = 00b) is not available.

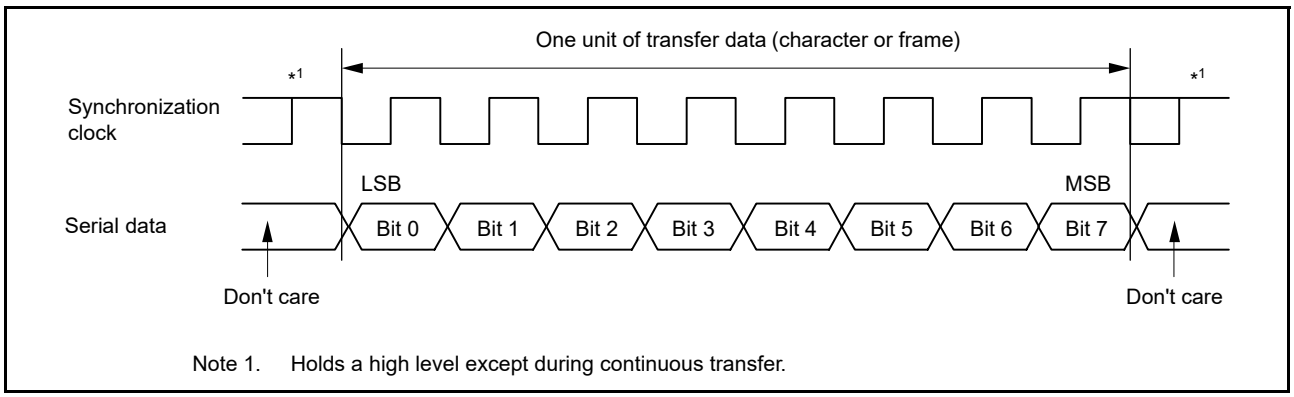


Figure 27.31 Data format in clock synchronous serial communications with LSB-first

27.5.1 Clock

Either an internal clock generated by the on-chip baud rate generator or an external synchronization clock input at the SCKn pin can be selected according to the setting of the SCR.CKE[1:0] bits.

When the SCI operates on an internal clock, the synchronization clock is output from the SCKn pin. Eight synchronization clock pulses are output in the transfer of one character. When no transfer is performed the clock is held high. However, when only data reception is performed while the CTS function is disabled, the synchronization clock output starts at the same time when the SCR.RE bit is set to 1. The synchronization clock stops when it goes high*1 and when an overrun error occurs or the SCR.RE bit is set to 0.

When only data reception is performed and the CTS function is enabled, the clock output does not start when the SCR.RE bit set to 1 and the CTSn_RTSn pin input is high. The synchronization clock output starts when the SCR.RE bit is set to 1 and the CTSn_RTSn pin input is low. Following that, when the CTSn_RTSn pin input is high on completion of the frame reception, the synchronization clock output stops when it goes high. If the CTSn_RTSn pin input continues to be low, the synchronization clock stops when it goes high*1 and when an overrun error occurs or the SCR.RE bit is set to 0.

Note 1. The signal is held high while (SPMR.CKPH bit = 0 && SPMR.CKPOL bit = 0) or (SPMR.CKPH bit = 1 && SPMR.CKPOL bit = 1). It is held low while (SPMR.CKPH bit = 0 && SPMR.CKPOL bit = 1) or (SPMR.CKPH bit = 1 && SPMR.CKPOL bit = 0).

27.5.2 CTS and RTS Functions

In the CTS function, the CTSn_RTSn pin input controls the start of data reception or transmission when the clock source is the internal clock. Setting the SPMR.CTSE bit to 1 enables the CTS function. When the CTS function is enabled, setting the CTSn_RTSn pin low causes data reception or transmission to start.

Setting the CTSn_RTSn pin high while the data transmission or reception is in progress does not affect transmission or reception of the current frame.

In the RTS function, the CTSn_RTSn pin output is used to request the start of data reception or transmission when the clock source is an external synchronizing clock. Low is output when serial communication becomes possible. Conditions for output of the low and high are shown as follows:

[Conditions for low-level output]

(a) Non-FIFO selected when all of the following conditions are satisfied

- The value of the RE or TE bit in the SCR is 1
- When serial communication is enabled
- There is no received data available to be read when the SCR.RE bit is 1
- Transmit data is written when the SCR.TE bit is 1 and SCR.CKE[1] bit is 0
- ORER flag in SSR is 0.

(b) FIFO selected when all of the following conditions are satisfied

- The value of the RE or TE bit in the SCR is 1
- When serial communication is enabled
- When the amount of receive data written in FRDRHL is less than the specified CTSn_RTSn output triggering number when SCR.RE = 1
- Data that has not been transmitted in FTDRHL is available when SCR.TE bit is 1 and SCR.CKE[1] bit is 0
- Data is available before transmission in the TSR register when SCR.TE bit is 1 and SCR.CKE[1] bit is 1
- The ORER in the SSR_FIFO is 0.

[Condition for high-level output]

(a) Non-FIFO selected

- The conditions for low-level output are not satisfied
- When reception is terminated with SCR.RE = 0 without reading the RDR register after reception is complete, RTS remains high. At this time, read the SCR register for dummy values after writing 0 to SCR.RE.

(b) FIFO selected

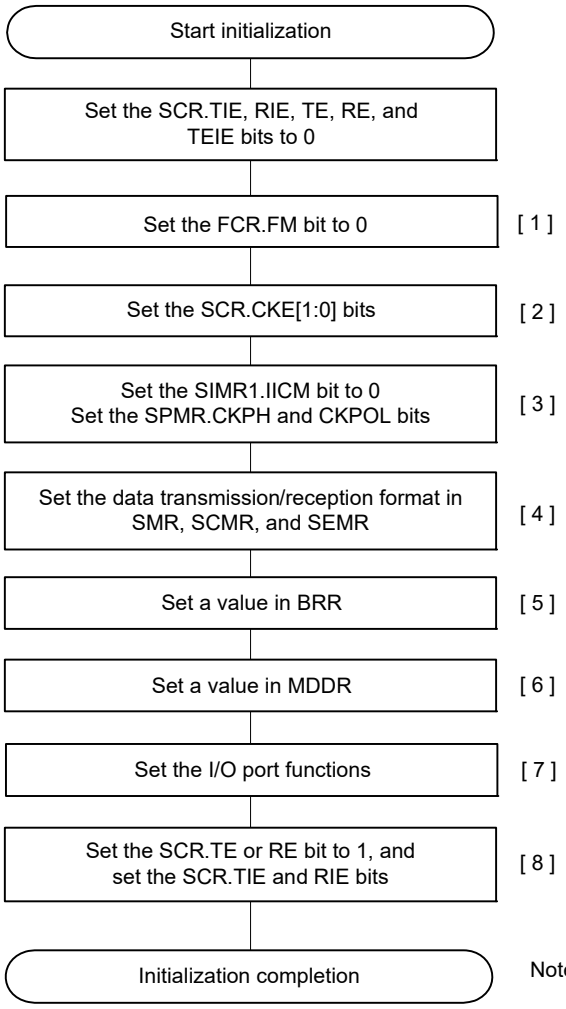
- The conditions for low-level output are not satisfied.

27.5.3 SCI Initialization in Clock Synchronous Mode

Before transmitting and receiving data, start by writing the initial value 00h to the SCR then continue through the SCI initialization procedure given in the Non-FIFO selected or FIFO selected sections in section 27.5.2, CTS and RTS Functions. Anytime the operating mode or transfer format is to be changed, the SCR must be initialized before the change can be made.

Note 1. Setting the SCR.RE bit to 0 initializes neither the ORER, FER, RDRF, RDF, PER and DR flags in SSR/SSR_FIFO nor the RDR and RDRHL. When the TE bit is set to 0, the TEND flag for the selected FIFO buffer is not initialized.

Note 2. Switching the value of the SCR.TE bit from 1 to 0 or 0 to 1 when the SCR.TIE bit is 1 generates an SCIn_TXI interrupt request.



[1] Set the FCR.FM bit to 0.

[2] Set the clock selection in SCR.

[3] Set the SIMR1.IICM bit to 0.
Set the SPMR.CKPH and CKPOL bits.
Step [3] can be skipped if the values have not changed from the initial values.

[4] Set data transmission/reception format in SMR, SCMR, and SEMR.

[5] Write a value corresponding to the bit rate to BRR.
This step is not necessary if an external clock is used.

[6] Write the value obtained by correcting a bit rate error in MDDR. This step is not necessary if the BRME bit in SEMR is set to 0 or an external clock is used.

[7] Specify the I/O port settings to enable input and output functions as required for the TXDn, RXDn, and SCKn pins.

[8] Set the SCR.TE or RE bit to 1. Set the SCR.TIE and RIE bits also.
Setting the TE and RE bits allows TXDn and RXDn to be used.

Note: In simultaneous transmit and receive operations, the TE and RE bits in SCR must both be set to 0 or set to 1 simultaneously.

Figure 27.32 Example flow of SCI initialization in clock synchronous mode with non-FIFO selected

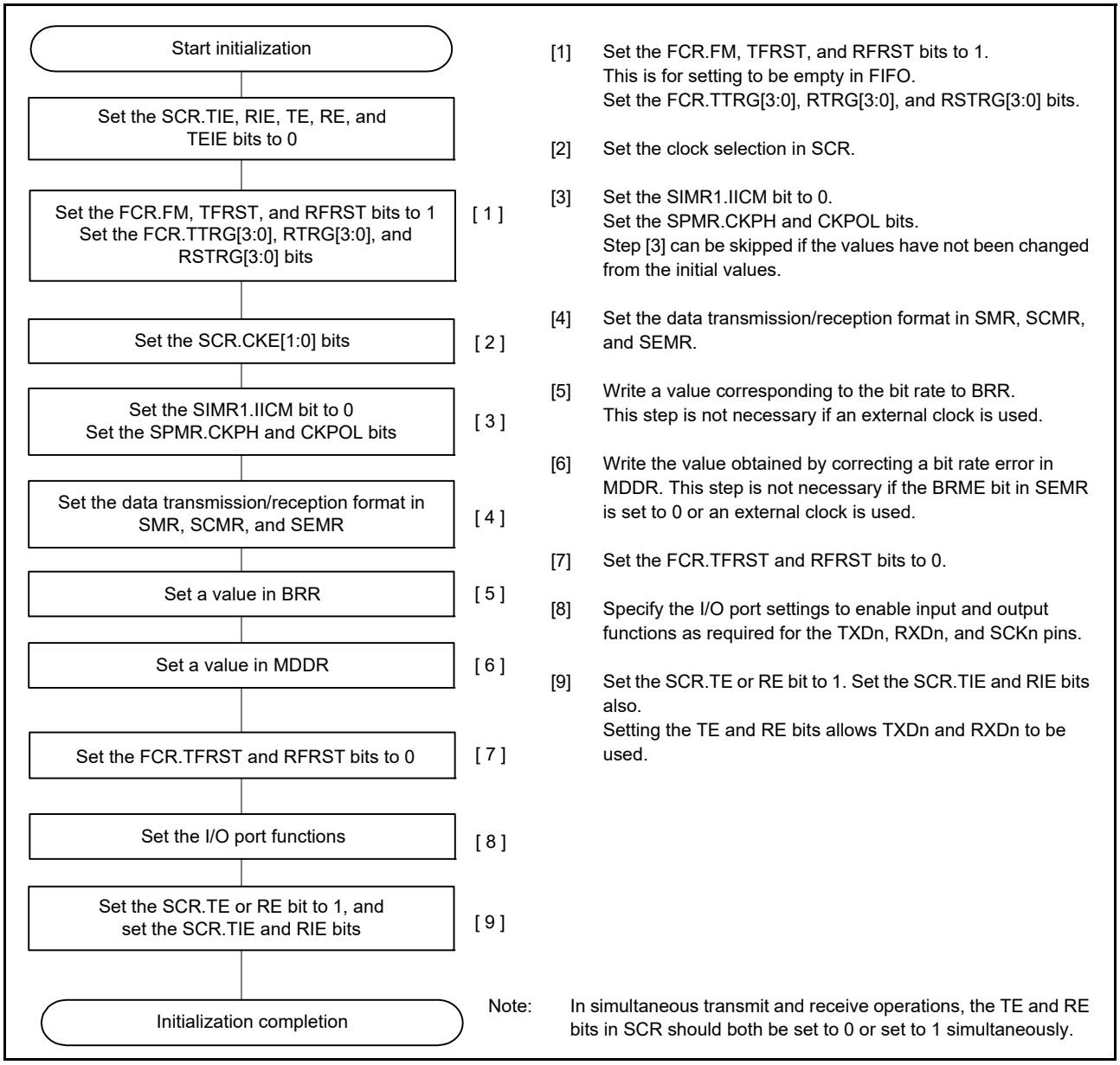


Figure 27.33 Example flow of SCI initialization in clock synchronous mode with FIFO selected

27.5.4 Serial Data Transmission in Clock Synchronous Mode

(1) Non-FIFO selected

Figure 27.34, Figure 27.35, and Figure 27.36 show examples of serial transmission in clock synchronous mode.

In serial data transmission, the SCI operates as follows:

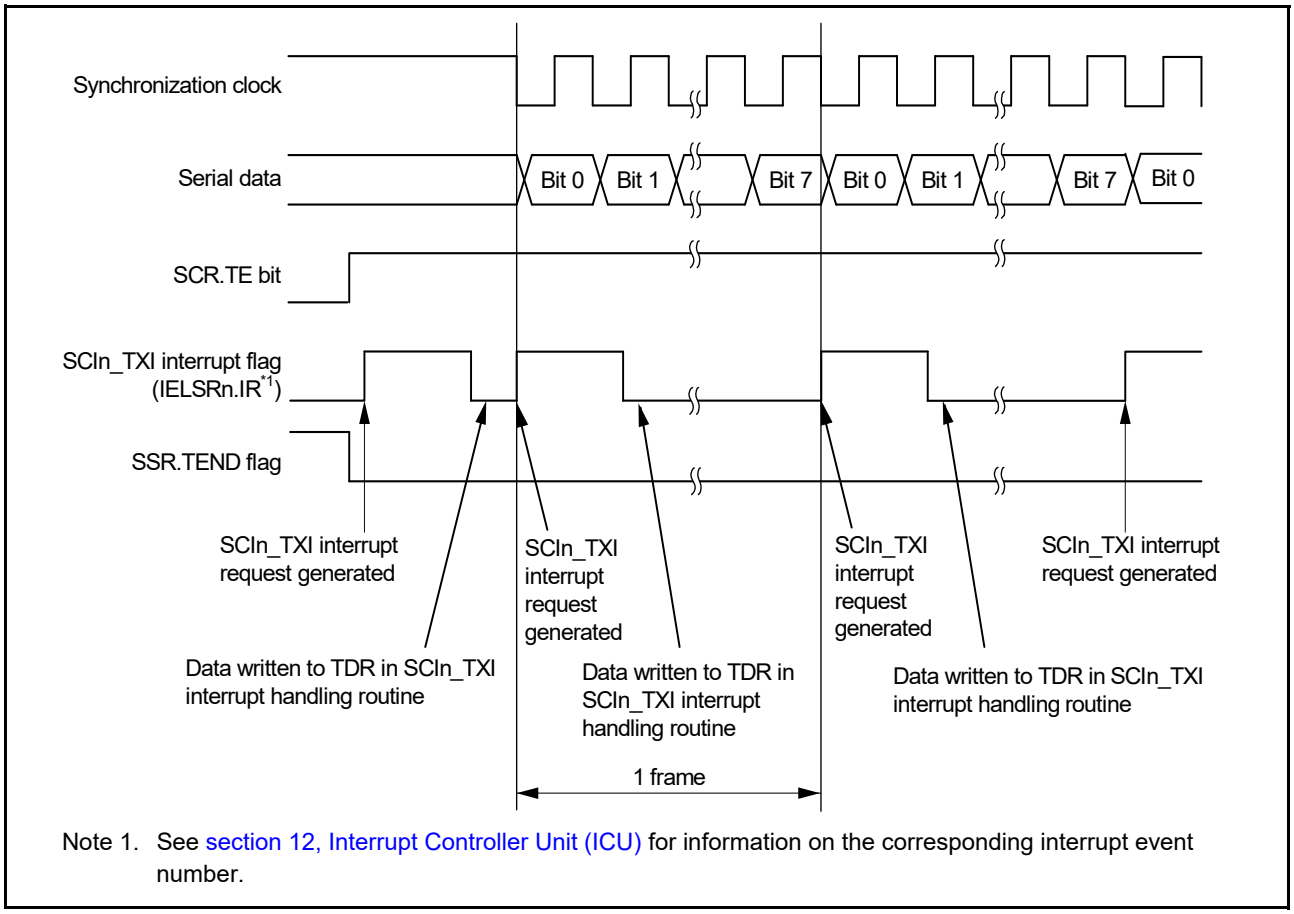
1. The SCI transfers data from TDR to TSR when data is written to TDR in the SCIn_TXI interrupt handling routine. The SCIn_TXI interrupt request at the beginning of transmission is generated when the TE bit is set to 1 but only after the TIE bits in the SCR are also set to 1 or when these two bits are set to 1 simultaneously by a single instruction.
2. After transferring data from TDR to TSR, the SCI starts transmission. When the SCR.TIE bit is set to 1, an SCIn_TXI interrupt request is generated. Continuous transmission is enabled by writing the next transmit data to TDR in this SCIn_TXI interrupt handling routine before transmission of the current transmit data finished. When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to the TDR from the handling routine for SCIn_TXI requests.

3. 8-bit data is sent from the TXDn pin in synchronization with the output clock when the clock output mode is specified and in synchronization with the input clock when the use of an external clock is specified. Output of the clock signal is suspended until the input CTS signal is low while the CTSE bit in SPMR is 1.
4. The SCI checks for update to the TDR on output of the last bit.
5. When TDR is updated, the next transmit data is transferred from TDR to TSR, and serial transmission of the next frame starts.
6. If TDR is not updated, set the SSR.TEND flag to 1. The TXDn pin retains the output state of the last bit. If the TEIE bit in SCR is 1, an SCIn_TEI interrupt request is generated and the SCKn pin is held high.

Figure 27.34 shows an example flow of serial data transmission.

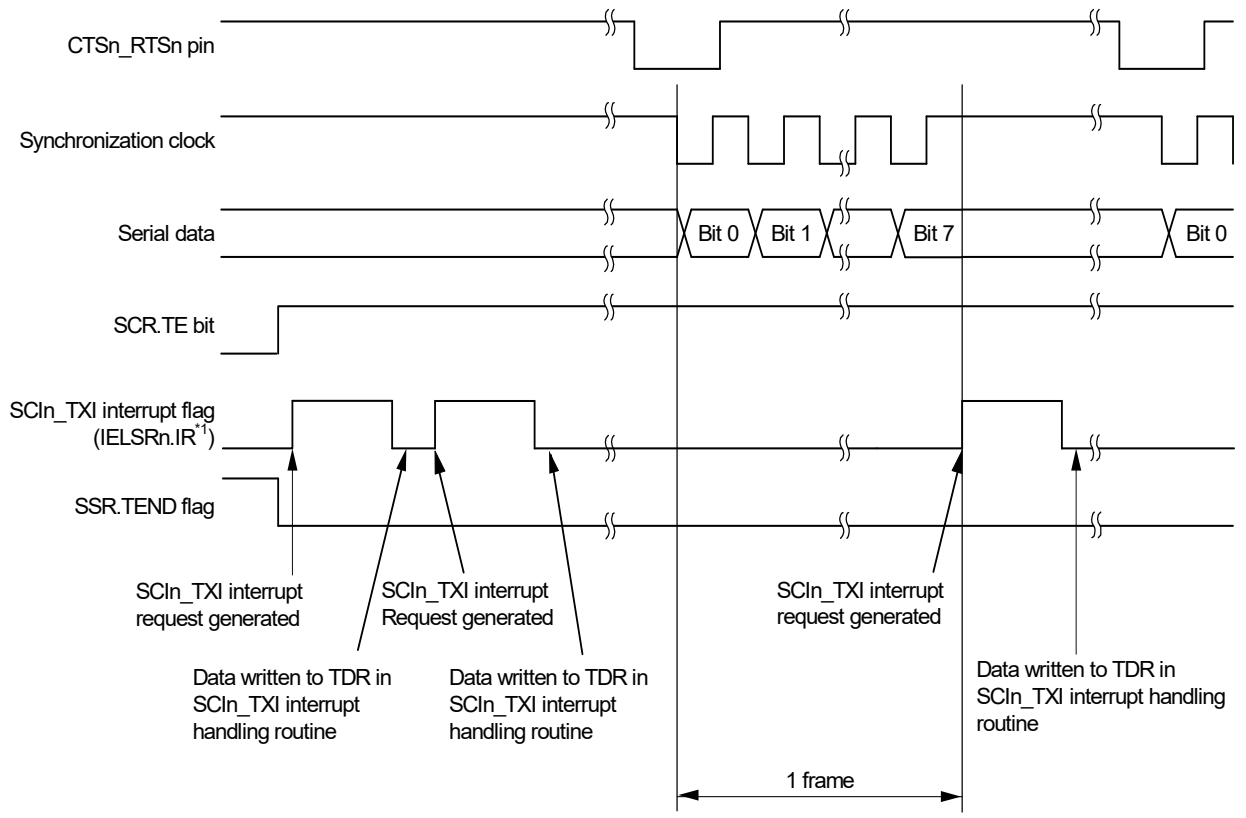
Transmission does not start while a receive error flag (ORER, FER, or PER in SSR) is set to 1. Be sure to set the receive error flags to 0 before starting transmission.

Note: Setting the RE bit in SCR to 0 does not clear the receive error flags.



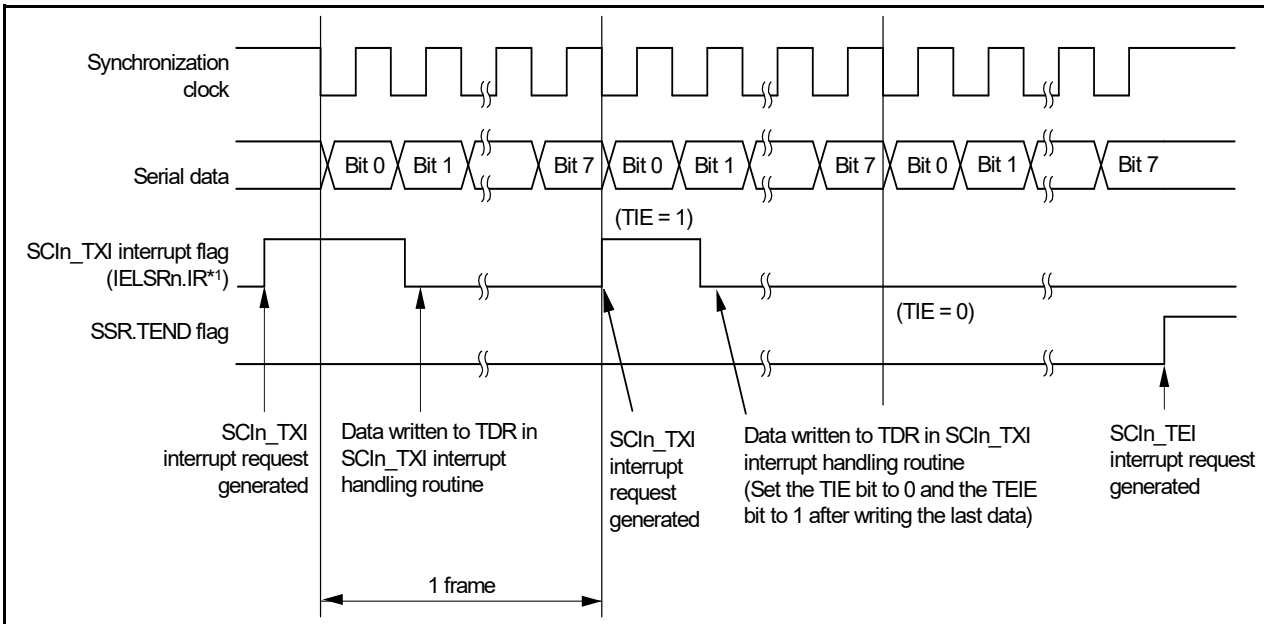
Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 27.34 Example of serial data transmission in Clock synchronous mode when the CTS function is not used at the beginning of transmission



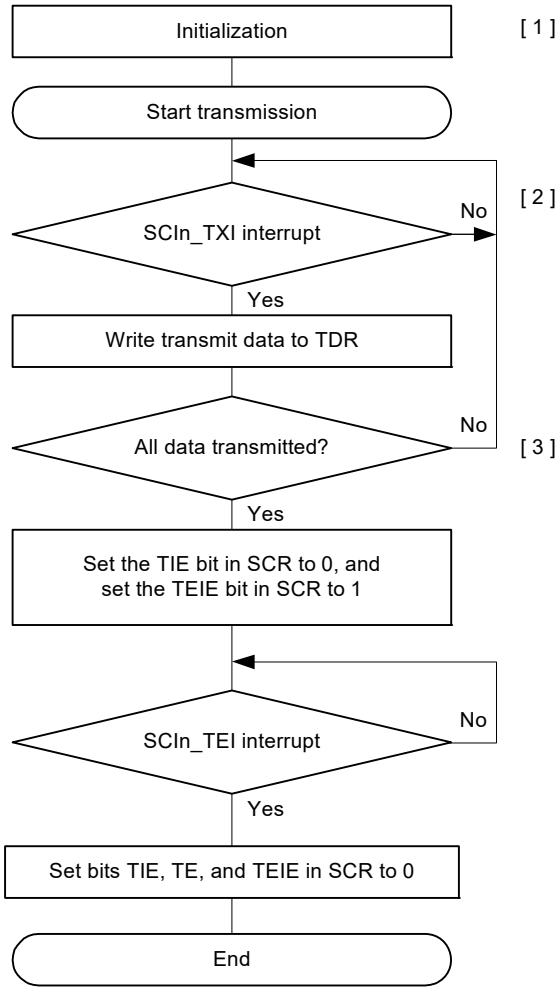
Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 27.35 Example of serial data transmission in clock synchronous mode when the CTS function is used at the beginning of transmission



Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 27.36 Example of serial data transmission in clock synchronous mode from the middle of transmission until transmission completion



[1] SCI initialization:
Set data transmission.

[2] Writing transmit data write to TDR by an SCIn_TXI interrupt request:
When transmit data is transferred from TDR to TSR, a transmit data empty interrupt (SCIn_TXI) request is generated.
Transmit data is written to TDR once from the handling routine for SCIn_TXI requests.

[3] Serial transmission continuation procedure:
To continue serial transmission, write transmit data to TDR upon accepting a transmit data empty interrupt (SCIn_TXI) request. Transmit data can also be written to TDR by activating the DTC by the SCIn_TXI interrupt request.
When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to the TDR.

Note: When the external clock is in use (the value of the SCR.CKE[1:0] bits is 10b or 11b), the rising edge on the SCK pin for the last bit sets the SSR.TEND flag to 1. Setting the SCR.TE bit to 0 immediately after this might lead to insufficient received-data hold time on the receiver side.

Figure 27.37 Example flow of serial transmission in clock synchronous mode with non-FIFO selected

(2) FIFO selected

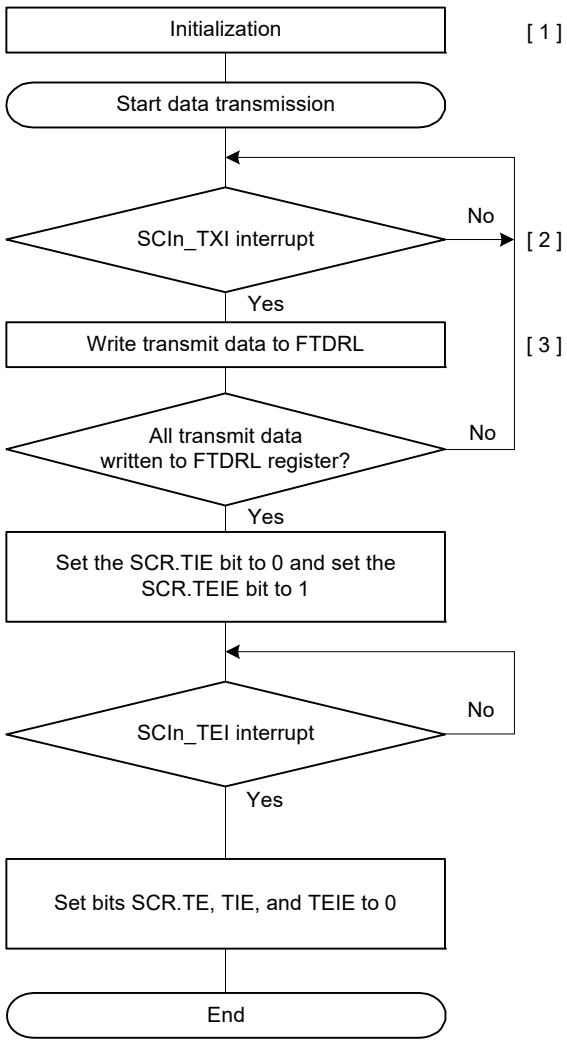
Figure 27.34 shows an example of serial transmission in clock synchronous mode with FIFO selected.

In serial data transmission, the SCI operates as follows:

1. The SCI transfers data from FTDRL*1 to TSR when data is written to FTDRL*1 in the SCIn_TXI interrupt handling routine. The amount of data that can be written to FTDRL is 16 minus FDR.T[4:0] bytes. The SCIn_TXI interrupt request at the beginning of transmission is generated when the TE bit in SCR is set to 1 but only after the TIE bit in SCR is also set to 1 or when these two bits are set to 1 simultaneously by a single instruction.
2. After transferring data from FTDRL to TSR, the SCI starts transmission. When the amount of transmit data written in FTDRL is equal to or less than the specified transmit triggering number, the SSR_FIFO.TDFE is set to 1. When the SCR.TIE bit is set to 1, an SCIn_TXI interrupt request is generated. Continuous transmission is enabled by writing the next transmit data to FTDRL in this SCIn_TXI interrupt handling routine before transmission of the current transmit data has finished. When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to the FTDRL from the handling routine for SCIn_TXI requests.
3. 8-bit data is sent from the TXDn pin in synchronization with the output clock when the clock output mode is specified and in synchronization with the input clock when the use of an external clock is specified. Output of the clock signal is suspended until the input CTS signal is low and while the CTSE bit in SPMR is 1.

4. The SCI checks whether non-transmitted data remains in FTDRL at the time of the output of the stop bit.
5. When FTDRL is updated, the next transmit data is transferred from FTDRL to TSR and serial transmission of the next frame starts.
6. If FTDRL is not updated, set the SSR_FIFO.TEND flag to 1. The TXDn pin retains the output state of the last bit. If the TEIE bit in SCR is 1, an SCIn_TEI interrupt request is generated and the SCKn pin is held high.

Note 1. In Clock synchronous mode, FTDRH is not used.



[1] SCI initialization:
Set data transmission.
After the TE bit in SCR is set to 1, 1 is output for a frame, and transmission is enabled.

[2] Transmit data write to FTDRL by an SCIn_TXI interrupt request:
When transmit data is transferred from FTDRL to TSR, and when the amount of transmit data written in FTDRL is equal to or less than the specified transmit triggering number, a transmit data FIFO empty interrupt (SCIn_TXI) request is generated. Write transmit data to FTDRL once in the SCIn_TXI interrupt handling routine.

[3] Serial transmission continuation procedure:
To continue serial transmission, write the next transmit data to FTDRL in this SCIn_TXI interrupt handling routine and clear the SSR_FIFO.TDFE flag to 0 before transmission of the current transmit data finished.
Transmit data can also be written to FTDRL by activating the DTC. The TDFE flag is cleared automatically in this case. Do not write to the TDFE flag.
When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to the FTDRL.

Note: When the external clock is in use (the value of the SCR.CKE[1:0] bits is 10b or 11b), the rising edge on the SCK pin for the last bit sets the SSR_FIFO.TEND flag to 1. Setting the SCR.TE bit to 0 immediately after this might lead to insufficient received-data hold time on the receiver side.

Figure 27.38 Example flow of serial transmission in clock synchronous mode with FIFO selected

27.5.5 Serial Data Reception in Clock Synchronous Mode

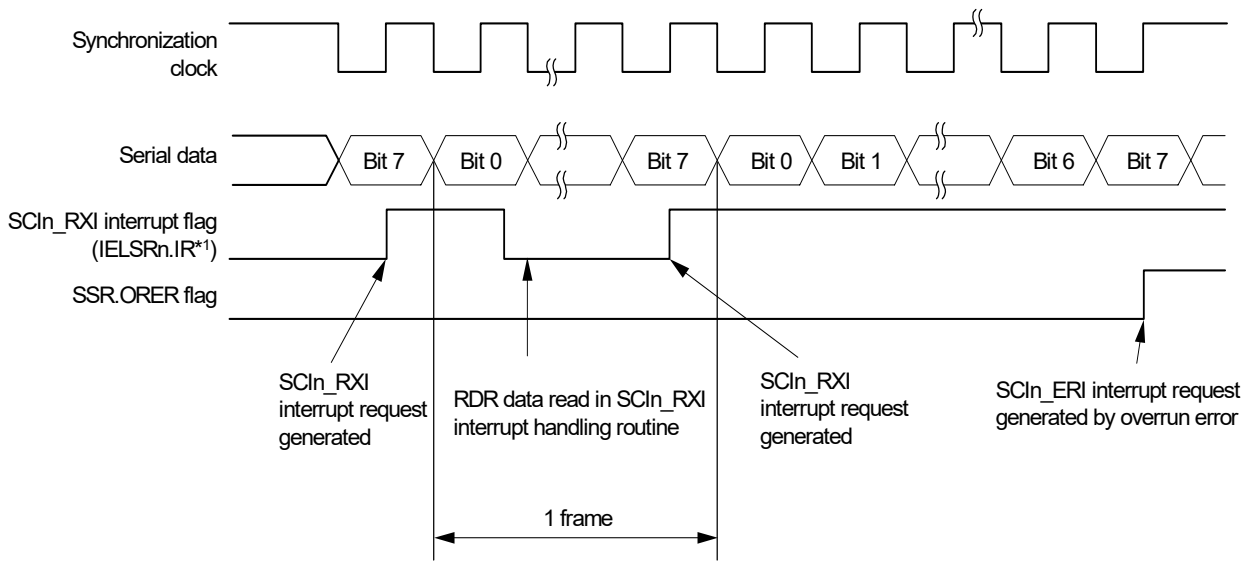
(1) Non-FIFO selected

Figure 27.39 and Figure 27.40 show examples of SCI operation for serial reception in clock synchronous mode.

In serial data reception, the SCI operates as follows:

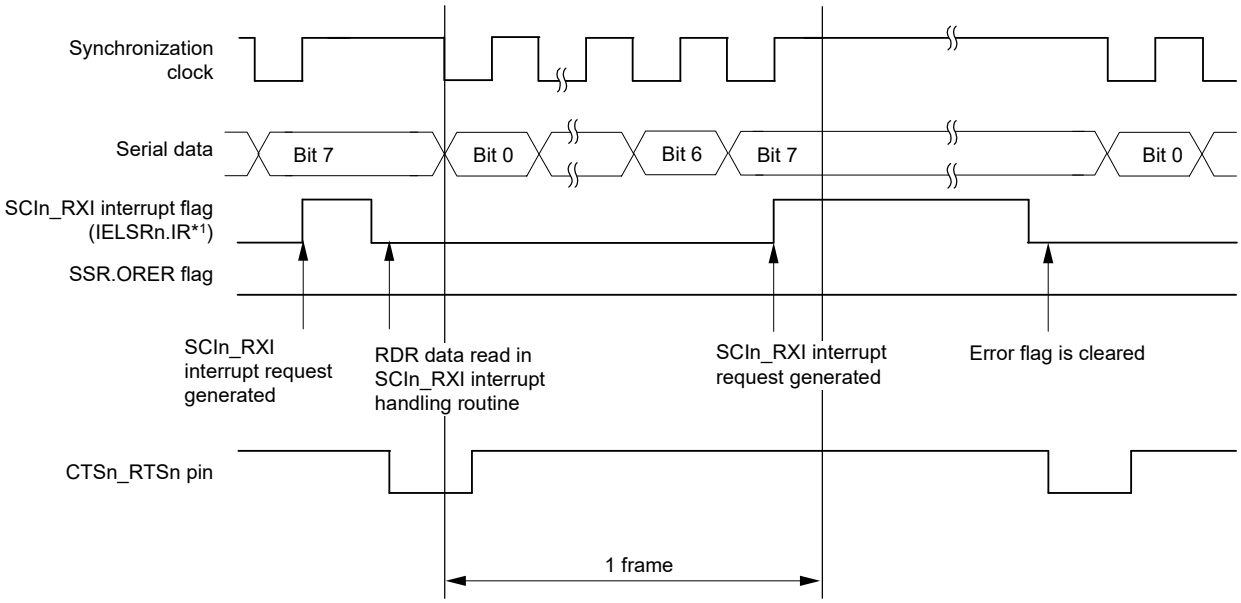
1. When the value of the RE bit in SCR becomes 1, the CTSn_RTSn pin goes low.
2. The SCI performs internal initialization and starts receiving data in synchronization with a synchronization clock input or output, and stores the receive data in RSR.

3. If an overrun error occurs, the ORER bit in SSR is set to 1. If the RIE bit in SCR is 1, an SCIn_ERI interrupt request is generated. Receive data is not transferred to RDR.
4. When reception completes successfully, receive data is transferred to RDR. If the RIE bit in SCR is 1, an SCIn_RXI interrupt request is generated. Continuous reception is enabled by reading the receive data transferred to RDR in the SCIn_RXI interrupt handling routine before reception of the next receive data completes. Reading the received data that is transferred to RDR causes the CTSn_RTSn pin to output low.



Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 27.39 Example operation for serial reception in clock synchronous mode (1) when RTS function is not used



Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 27.40 Example operation for serial reception in clock synchronous mode (2) when RTS function is used

Data transfer cannot resume while the receive error flag is 1. Therefore, clear the ORER, FER, and PER bits in SSR to 0 before resuming data reception. Additionally, be sure to read the RDR during overrun error processing. When a data reception is forced to terminate by setting the SCR.RE bit to 0 during operation, read the RDR because received data that has not yet been read might be left in the RDR.

Figure 27.41 shows an example flow for serial data reception.

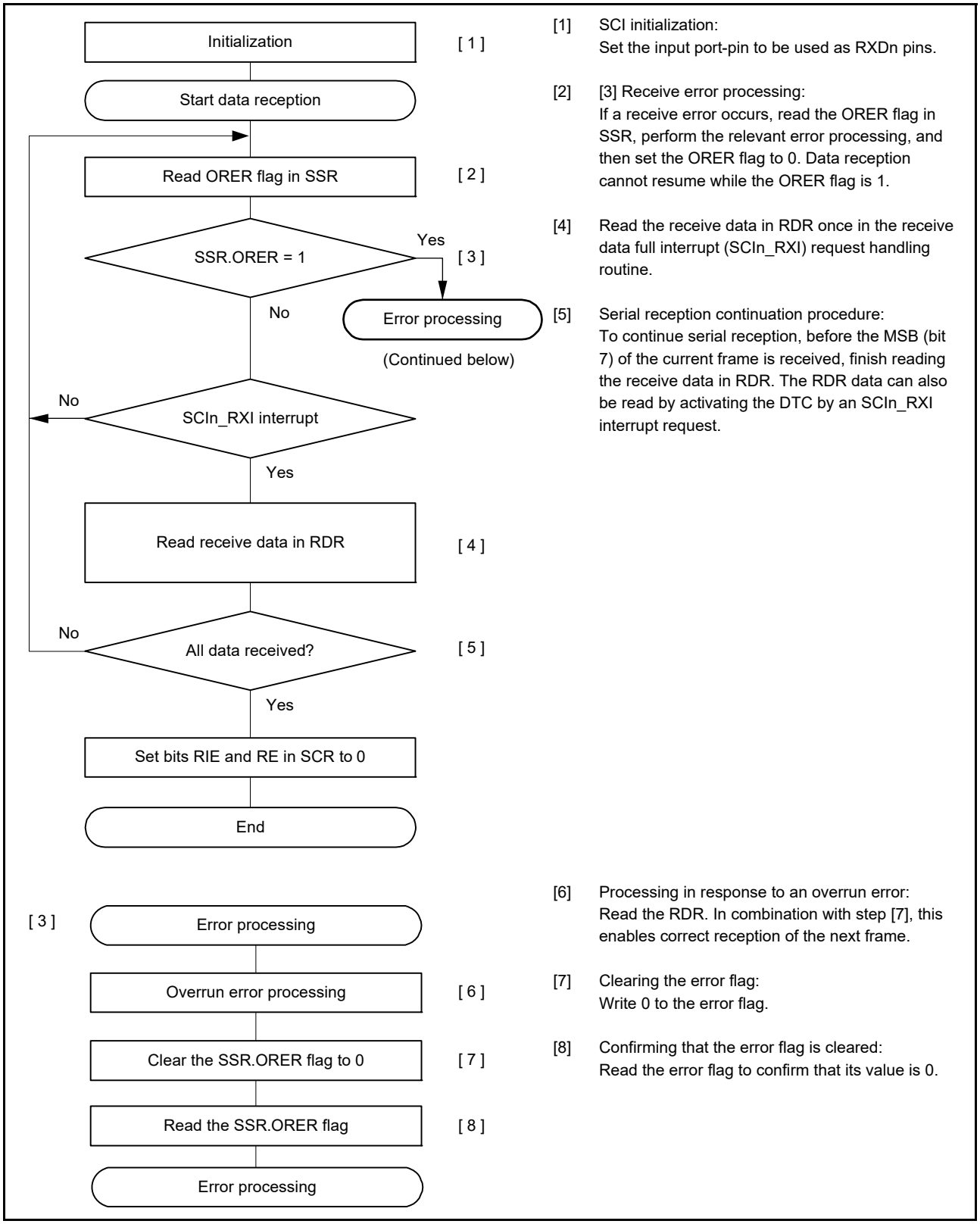


Figure 27.41 Example flow of serial reception in clock synchronous mode with non-FIFO selected

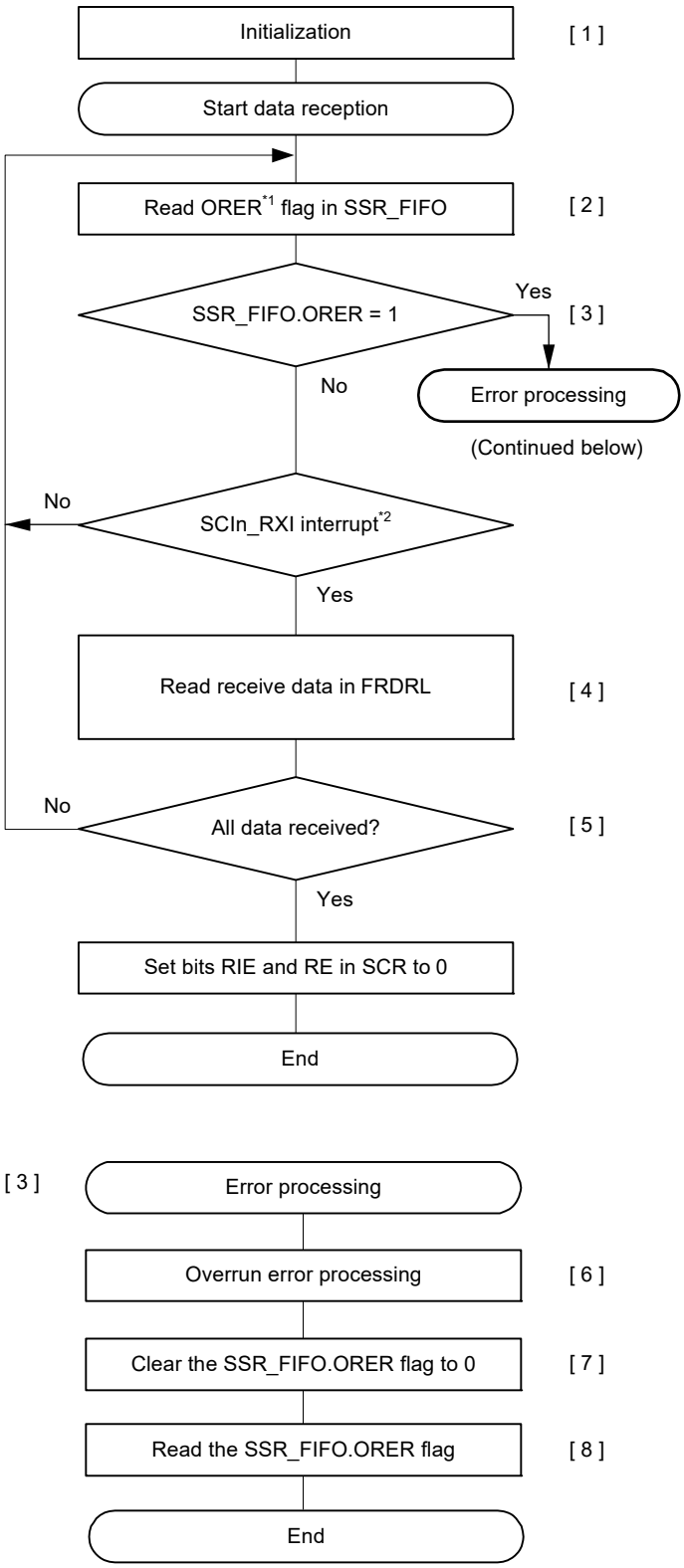
(2) FIFO selected

Figure 27.42 shows an example of serial reception in Clock synchronous mode with FIFO selected.

In serial data reception, the SCI operates as follows:

1. When the value of the RE bit in SCR becomes 1, the CTSn_RTSn pin goes low.
2. The SCI performs internal initialization and starts receiving data in synchronization with a synchronization clock input or output, and stores the receive data in RSR.
3. If an overrun error occurs, the ORER bit in SSR_FIFO is set to 1. If the RIE bit in SCR is 1, an SCIn_ERI interrupt request is generated. Received data is not transferred to FRDRL*1.
4. When data reception completes successfully, the receive data is transferred to FRDRL*1. RDF is set to 1 when the amount of the receive data is equal to or greater than the specified receive triggering number stored in FRDRHL. If the RIE bit in SCR is 1, an SCIn_RXI interrupt request is generated. Continuous data reception is enabled by reading the receive data transferred to FRDRL*2 in the SCIn_RXI interrupt handling routine before an overrun error occurs. If the amount of received data that is transferred to FRDRL is less than the RTS trigger number, the CTSn_RTSn pin goes low.

Note 1. In Clock synchronous mode, FTDRH is not used.
Note 2. Read the data in the order from FRDRH to FRDRL when RDF and ORER are read with receive data.



[1] SCI initialization:
Set the input port-pin to be used as RXDn pins.

[2] [3] Receive error processing:
If a receive error occurs, read the ORER flag in SSR_FIFO, perform the relevant error processing, then set the SSR_FIFO.ORER flag to 0. Data reception cannot resume while the ORER flag is 1.

[4] The reception data stored in FRDRL register is read until the number of stored data is less than the FCR.RTRG value. Software can check readable data in FDR.R[4:0].

[5] Serial reception continuation procedure:
To continue serial reception, before overrun error occurs, finish reading the receive data in FRDRL and clear the SSR_FIFO.RDF flag to 0.The FRDRL data can also be read by activating the DTC by an SCIn_RXI interrupt request. The RDF flag is cleared automatically in this case. Do not write to the RDF flag.

[6] Processing in response to an overrun error:
Read the FRDRL. In combination with step [7], this enables correct reception of the next frame.

[7] Clearing the error flag:
Write 0 to the error flag.

[8] Confirming that the error flag is cleared:
Read the error flag to confirm that its value is 0.

Note 1. It can also read from FRDRH.ORER. However, to clear the ORER flag, write 0 to the corresponding bit in the SSR_FIFO register.
Note 2. It should be all receive data and is an integer times FIFO triggering number.

Figure 27.42 Example flow of serial reception in clock synchronous mode with FIFO selected

27.5.6 Simultaneous Serial Data Transmission and Reception in Clock Synchronous Mode

(1) Non-FIFO selected

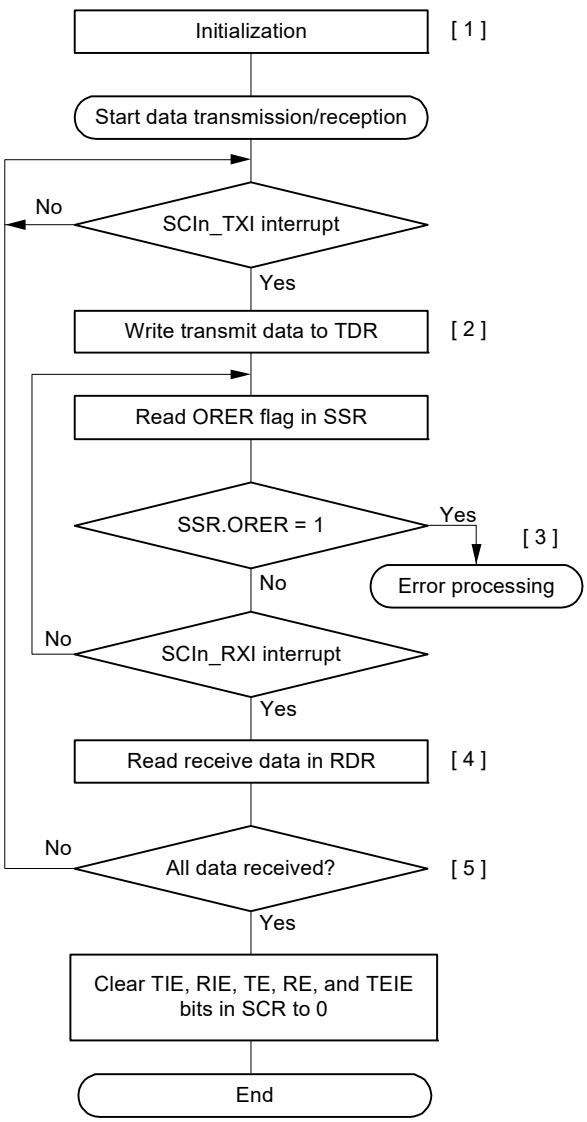
Figure 27.43 shows an example flow of simultaneous serial transmit and receive operations in clock synchronous mode with non-FIFO selected. After initializing the SCI, use the following procedure for simultaneous serial data transmit and receive operations.

To switch from transmit mode to simultaneous transmit and receive mode:

1. Check that the SCI completes the data transmission by verifying that the TEND flag in the SSR_FIFO register is set to 1.
2. Initialize the SCR register, then set the TIE, RIE, TE, and RE bits in the SCR register to 1 simultaneously with a single instruction.

To switch from receive mode to simultaneous transmit and receive mode:

1. Check that the SCI completes the data reception.
2. Set SCR.RIE and SCR.RE to 0, then check that the receive error flag ORER in the SSR register is 0.
3. Set the TIE, RIE, TE, and RE bits in the SCR register to 1 simultaneously with a single instruction.



[1] SCI initialization:
The TXDn pin can act as the output pin for transmitted data and the RXDn pin can act as the input pin for received data at the same time.

[2] Transmit data write:
Write transmit data to TDR once in the SCIn_TXI interrupt request handling routine.

[3] Receive error processing:
If a receive error occurs, read the ORER flag in SSR, perform the relevant error processing, then set the ORER flag to 0. Data reception cannot resume while the ORER flag is 1.

[4] Reading receive data:
Read the receive data in RDR once in the SCIn_RXI interrupt request handling routine.

[5] Serial transmission/reception continuation procedure:
To continue serial transmission and reception, before the MSB bit [7] of the current frame is received, finish reading the receive data in RDR by the SCIn_RXI interrupt. Also, before the MSB bit [7] of the current frame is transmitted, write data to TDR by the SCIn_TXI interrupt.
Transmit data can also be written to TDR by activating the DTC by a transmit data empty interrupt (SCIn_TXI) request. Similarly, the RDR data can also be read by activating the DTC by a receive data full interrupt (SCIn_RXI) request.

Note: When switching from transmit or receive operation to simultaneous transmit and receive operations, first set the TIE, RIE, TE, RE, and TEIE bits in SCR to 0, then set TIE, RIE, TE, and RE bits to 1, simultaneously.

Figure 27.43 Example flow of simultaneous serial transmission and reception in clock synchronous mode with non-FIFO selected

(2) FIFO selected

Figure 27.44 shows an example flow of simultaneous serial transmit and receive operations in clock synchronous mode with FIFO selected.

After initializing the SCI, use the following procedure for simultaneous serial data transmit and receive operations.

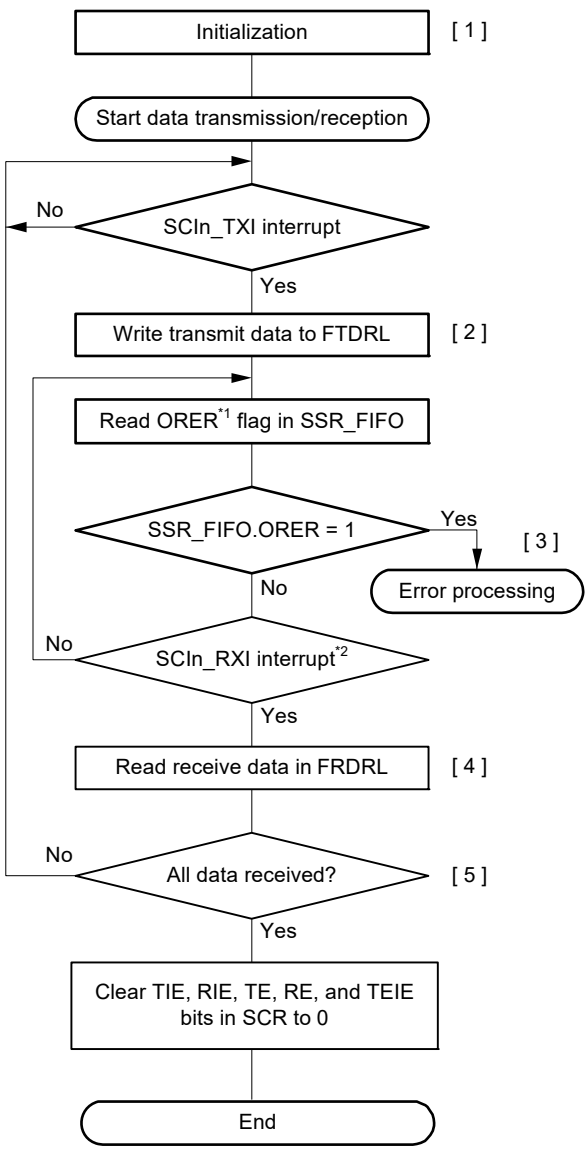
To switch from transmit mode to simultaneous transmit and receive mode:

1. Check that the SCI completes the transmission by verifying that the TEND flag in the SSR_FIFO register is set to 1.
2. Initialize the SCR register, then set the TIE, RIE, TE, and RE bits in the SCR register to 1 simultaneously with a single instruction.

To switch from receive mode to simultaneous transmit and receive mode:

1. Check that the SCI completes the reception.
2. Set SCR.RIE and SCR.RE bits to 0, then check that the receive error flag ORER in the SSR_FIFO register is 0.

3. Set the TIE, RIE, TE, and RE bits in the SCR register to 1 simultaneously with a single instruction.



[1] SCI initialization:
The TXDn pin can act as the output pin for transmitted data and the RXDn pin can act as the input pin for received data at the same time.

[2] Transmit data write:
Write transmit data to FTDRL in the SCIn_TXI Interrupt request handling routine. The number of transmission data that is possible to write in is 16 - the number of stored transmit FIFO data.

[3] Receive error processing:
If a receive error occurs, read the ORER flag in SSR_FIFO, perform the relevant error processing, and then set the ORER flag to 0. Data reception cannot resume while the ORER flag is 1.

[4] Reading receive data:
The reception data stored in FRDRL register is read until the number of stored data is less than the FCR.RTRG value. Software can check readable data in FDR.R[4:0].

[5] Serial transmission/reception continuation procedure:
To continue serial reception, before overrun error occurs, finish reading the receive data in FRDRL and clear the SSR_FIFO.RDF flag to 0. To continue serial transmission, before transmission of the current transmit data has finished, write the next transmit data to FTDRL In this SCIn_TXI interrupt handling routine and clear the SSR_FIFO.TDFE flag to 0.
Transmit data can also be written to FTDRL by activating the DTC by a transmit FIFO data empty interrupt (SCIn_TXI) request. Similarly, the FRDRL data can also be read by activating the DTC by a receive FIFO Data full interrupt (SCIn_RXI) request. The RDF and TDFE flags are cleared automatically in this case.
Do not write to the RDF And TDFE flags.

Note 1. It can also read from FRDRH.ORER. To clear the ORER flag, write 0 to the corresponding bit in the SSR_FIFO register.
Note 2. It should be all receive data with an integer times FIFO triggering number.

Figure 27.44 Example flow of simultaneous serial transmission and reception in clock synchronous mode with FIFO selected

27.6 Operation in Smart Card Interface Mode

The SCI supports smart card (IC card) interfaces conforming to ISO/IEC 7816-3 (standard for Identification Cards), as an extended function of the SCI.

Smart card interface mode can be selected using the appropriate register.

27.6.1 Example Connection

Figure 27.45 shows an example connection between a smart card (IC card) and the MCU.

As shown in Figure 27.45, because the MCU communicates with an IC card using a single transmission line, interconnect the TXDn and RXDn pins and pull up the data transmission line to VCC using a resistor.

Setting the TE and RE bits in SCR_SMCI to 1 with an IC card disconnected enables closed-loop transmission/reception allowing self-diagnosis. To supply an IC card with the clock pulses generated by the SCI, input the SCKn pin output to the CLK pin of an IC card.

The output port of the MCU can be used to output a reset signal.

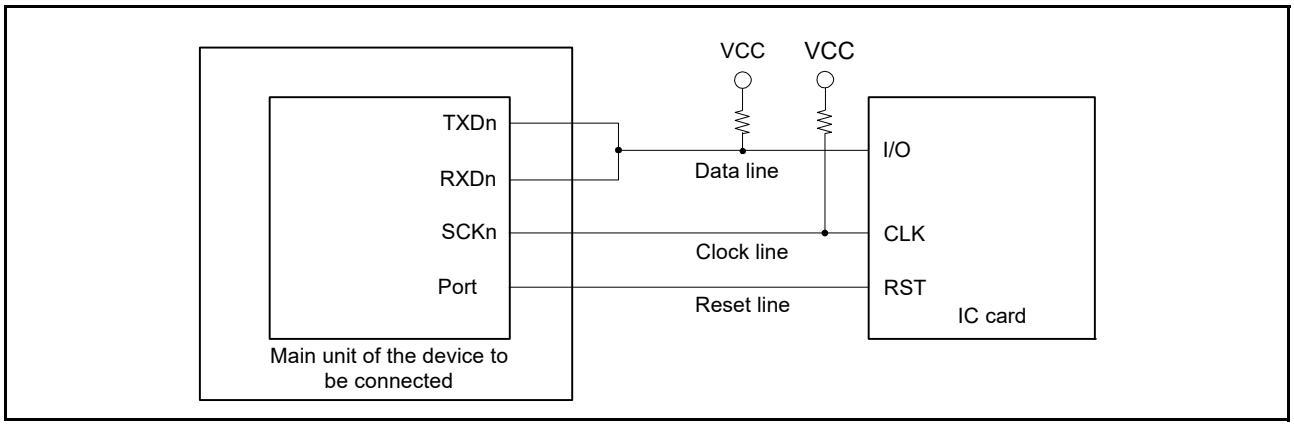


Figure 27.45 Example connection with a smart card (IC Card)

27.6.2 Data Format (Except in Block Transfer Mode)

Figure 27.46 shows the data transfer formats in smart card interface mode.

- One frame consists of 8-bit data and a parity bit in asynchronous mode
- During transmission, at least 2 ETUs (elementary time unit is the time required for transferring 1 bit) is set as a guard time from the end of the parity bit until the start of the next frame
- If a parity error is detected during reception, a low error signal is output for 1 ETU after 10.5 ETUs elapse from the start bit
- If an error signal is sampled during transmission, the same data is automatically retransmitted after at least 2 ETUs.

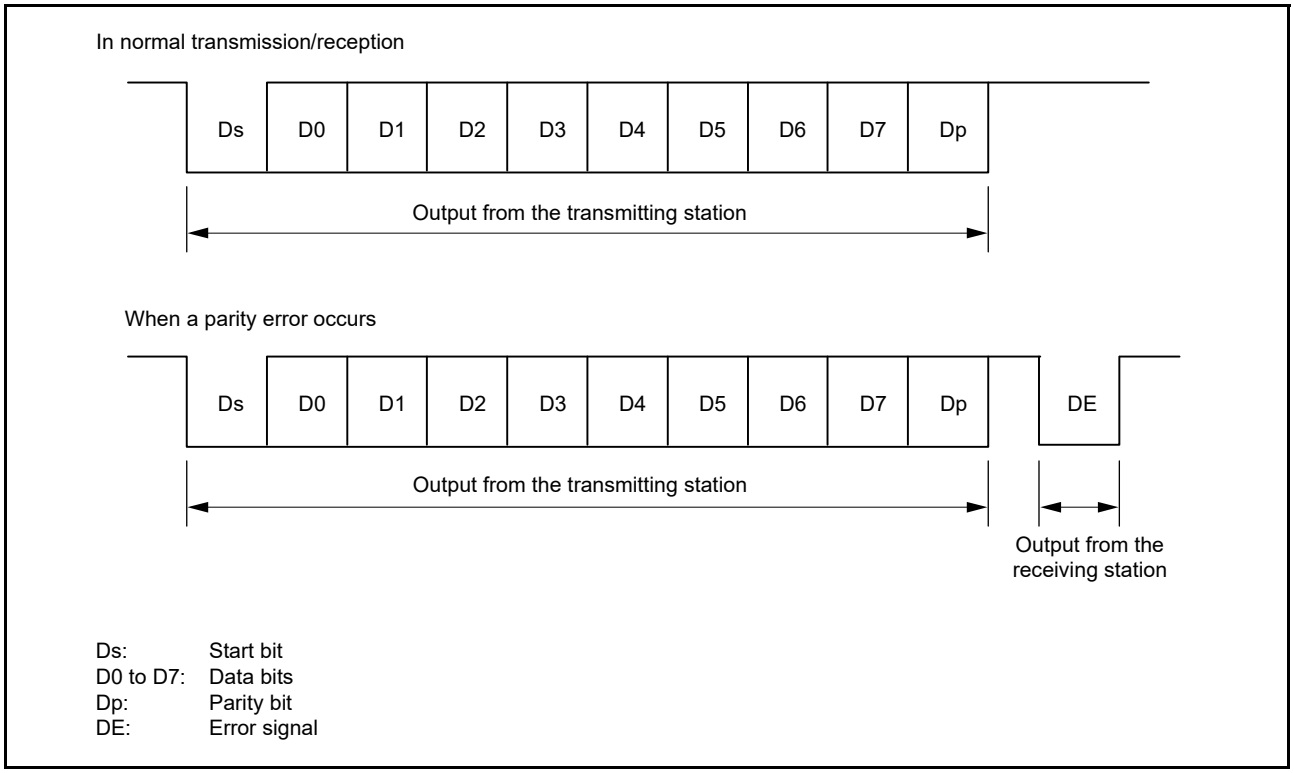


Figure 27.46 Data formats in smart card interface mode

For communications with IC cards of the direct convention type and inverse convention type, follow the procedures in this section.

(1) Direct convention type

For the direct convention type, logic levels 1 and 0 correspond to states Z and A, respectively, and data is transferred with LSB-first as the start character, as Figure 27.47 shows. Therefore, data in the start character in the figure is 3Bh.

When using the direct convention type, write 0 to both the SDIR and SINV bits in SCMR. Write 0 to the PM bit in SMR_SMCI to use even parity, which is described by the smart card standard.

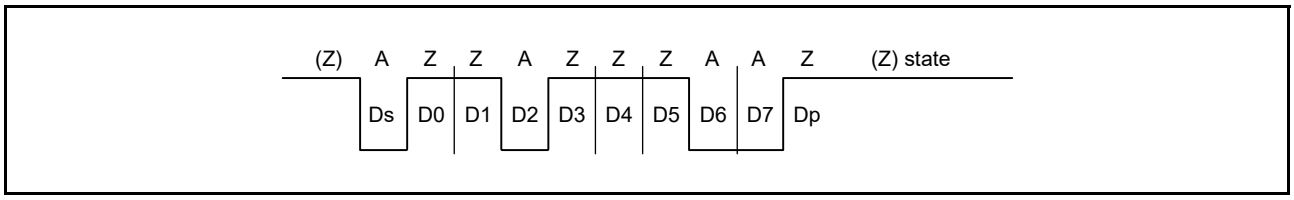


Figure 27.47 Direct convention with SDIR in SCMR = 0, SINV in SCMR = 0, and PM in SMR_SMCI = 0

(2) Inverse convention type

For the inverse convention type, logic levels 1 and 0 correspond to states A and Z, respectively and data is transferred with MSB-first as the start character, as Figure 27.48 shows. Therefore, data in the start character in the figure is 3Fh.

When using the inverse convention type, write 1 to both the SDIR and SINV bits in SCMR. The parity bit is logic level 0 to produce even parity, which is described by the smart card standard, and corresponds to state Z. Because the SINV bit of the MCU only inverts data bits D7 to D0, write 1 to the PM bit in SMR_SMCI to invert the parity bit for both transmission and reception.

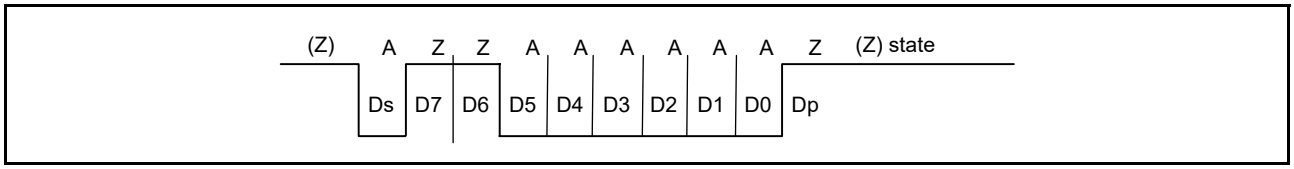


Figure 27.48 Inverse convention with SDIR in SCMR = 1, SINV in SCMR = 1, and PM in SMR_SMCI = 1

27.6.3 Block Transfer Mode

Block transfer mode differs from non-block transfer mode of smart card interface mode in the following respects:

- Even if a parity error is detected during reception, no error signal is output. Because the PER bit in SSR_SMCI is set by error detection, clear the PER bit before receiving the parity bit of the next frame
- During transmission, at least 1 ETU is set as a guard time from the end of the parity bit until the start of the next frame
- Because the same data is not retransmitted, the TEND flag in SSR_SMCI is set to 11.5 ETUs after transmission starts
- In block transfer mode, the ERS flag in SSR_SMCI indicates the error signal status as in non-block transfer mode of smart card interface mode, but the flag is read as 0 because no error signal is transferred.

27.6.4 Receive Data Sampling Timing and Reception Margin

Only the clock generated by the on-chip baud rate generator can be used as a transfer clock in smart card interface mode.

In this mode, the SCI can operate on a base clock with a frequency of 32, 64, 372, 256, 93, 128, 186, or 512 times the bit rate based on the BCP2 setting in SCMR and the BCP[1:0] bits in SMR_SMCI.

For data reception, the falling edge of the start bit is sampled with the base clock to perform synchronization.

Receive data is sampled on the 16th, 32nd, 186th, 128th, 46th, 64th, 93rd, and 256th rising edges of the base clock so that it can be latched at the middle of each bit as Figure 27.49 shows. The reception margin is determined by the following formula.

$$M = \left| (0.5 - \frac{1}{2N}) - (L - 0.5) F - \frac{\left| D - 0.5 \right|}{N} (1 + F) \right| \times 100 \ [\%]$$

M: Reception margin (%)
N: Ratio of bit rate to clock (N = 32, 64, 372, 256)
D: Duty cycle of clock (D = 0 to 1.0)
L: Frame length (L = 10)
F: Absolute value of clock frequency deviation

Assuming values of F = 0, D = 0.5, and N = 372 in the specified formula, the reception margin is determined by the following formula:

$M = \{0.5 - 1/(2 \times 372)\} \times 100 \ [\%] = 49.866\%$

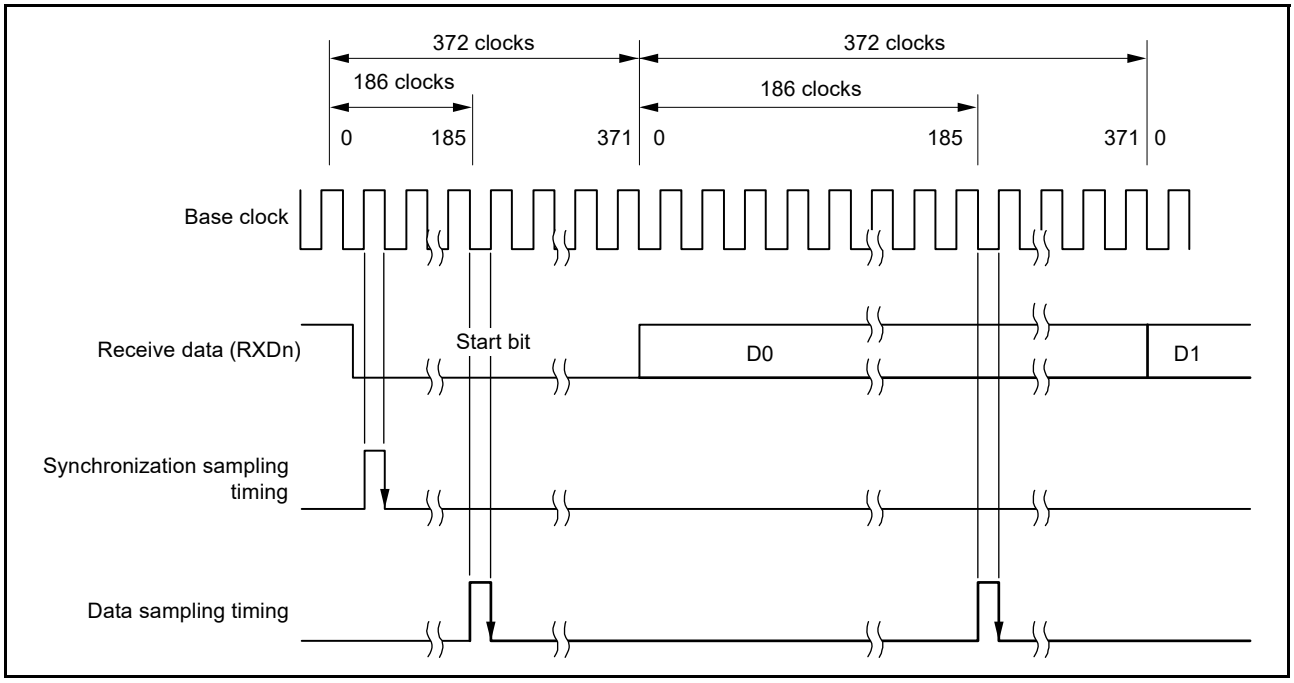


Figure 27.49 Receive data sampling timing in smart card interface mode when clock frequency is 372 times the bit rate

27.6.5 Initialization of the SCI

Before transmitting and receiving data, write the initial value 00h in the SCR_SMCI register and initialize the SCI following the example flow shown in Figure 27.50.

Be sure to set the initial value in the TIE, RIE, TE, RE, TEIE bits in the SCR_SMCI register before switching from transmission mode to reception mode and from reception mode to transmission mode. When the RE bit is set to 0, the RDR register is not initialized.

To change from reception mode to transmission mode, first check that reception is complete, then initialize the SCI. At the end of initialization, set TE = 1 and RE = 0. Reception completion can be verified by reading the SCIn_RXI request, ORER, or PER flag in SSR_SMCI.

To change from transmission mode to reception mode, first check that transmission is complete, then initialize the SCI. At the end of initialization, set TE = 0 and RE = 1. Transmission completion can be verified by reading the TEND flag in SSR_SMCI.

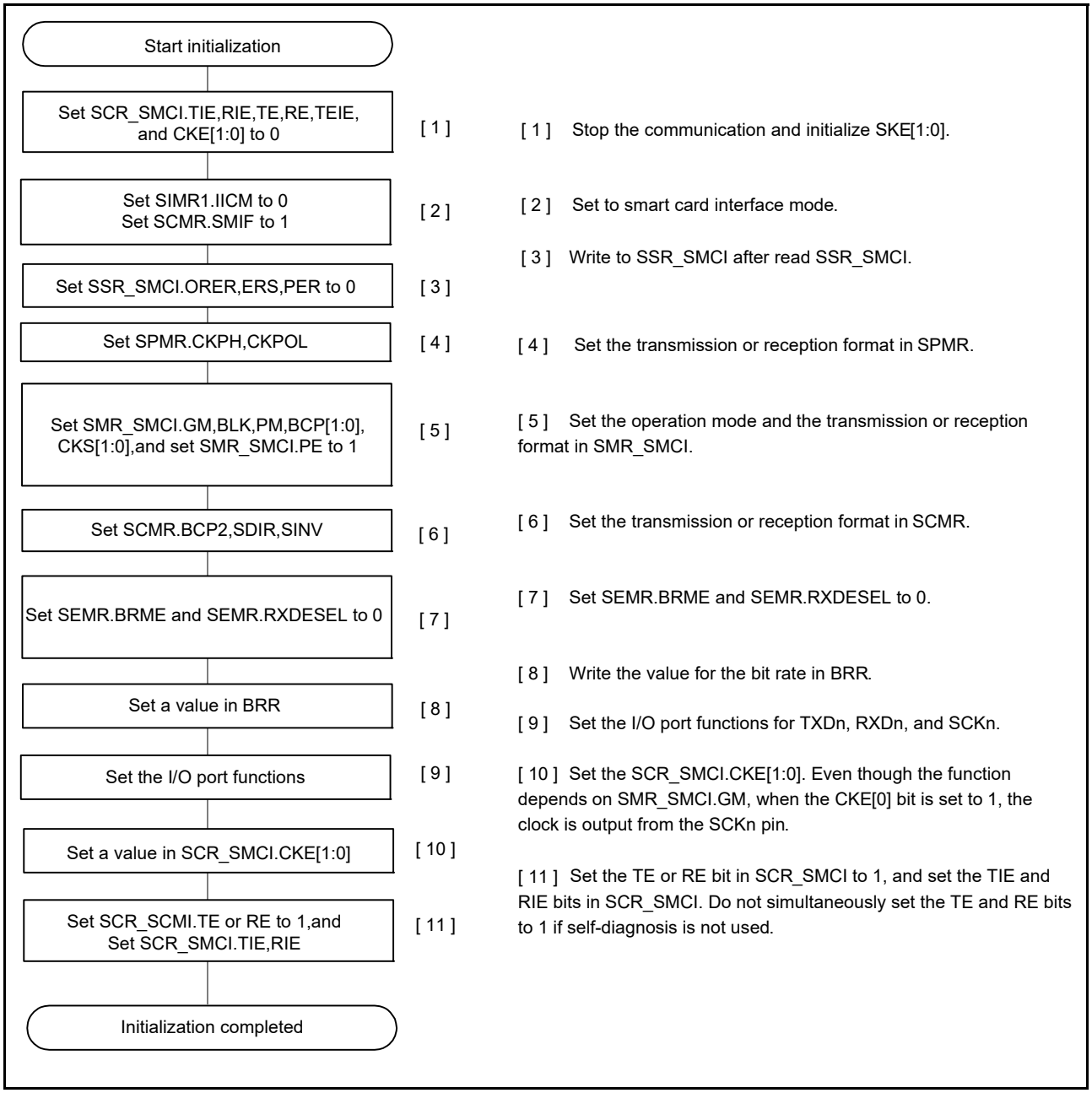


Figure 27.50 Example flow of SCI initialization in smart card interface mode

Figure 27.51 show a timing diagram when data transmission is performed by transitioning to smart card interface mode according to the flow in Figure 27.50. Figure 27.51 shows when the GM bit in SMR_SMCI is set to 0. The timing in this figure shows when the port is connected as SCKn and TXDn pin, the pins are Hi-Z because CKE[0] bit in SCR_SMCI is 0.

Start the clock output to the SCK pin by setting CKE[0] bit in SCR_SMCI to 1, then start data transmission by writing transmit data after setting TE bit in SCR_SMCI to 1. When the TE bit in SCR_SMCI changes from 0 to 1, there is a preamble period for one frame before data transmission starts. In smart card interface mode, the TXDn pin is Hi-Z during the preamble period. Pull-up or pull-down for the SCKn and TXDn pins is required outside the MCU

In smart card interface mode, even when the TE and RE bits in SCR_SMCI are 0, the clock is continuously output if the clock output setting is used.

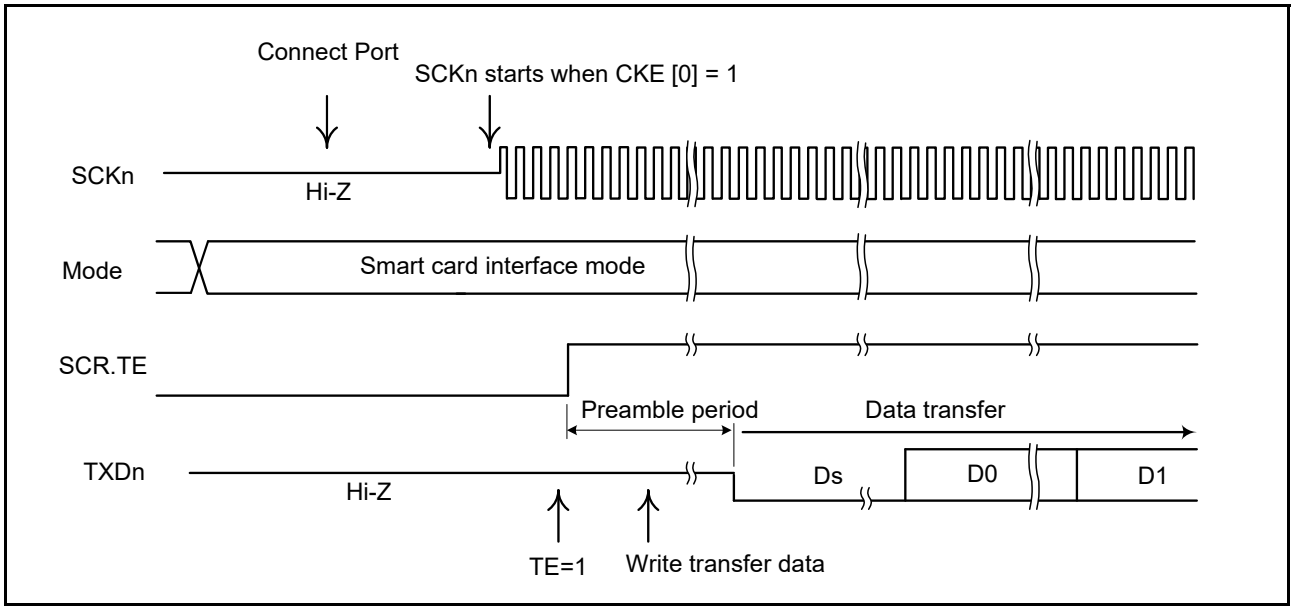


Figure 27.51 Example timing of data transmission in smart card interface mode

27.6.6 Serial Data Transmission (Except in Block Transfer Mode)

Serial data transmission in smart card interface mode (except in block transfer mode) is different from that in non-smart card interface mode, in that an error signal is sampled and data can be retransmitted in smart card interface mode. Figure 27.52 shows the data retransfer operation during transmission.

- [1] When an error signal from the receiver end is sampled after 1-frame data is transmitted, the ERS flag in SSR_SMCI is set to 1. If the RIE bit in SCR_SMCI is 1, an SCIn_ERI interrupt request is generated. Clear the ERS flag to 0 before the next parity bit is sampled.
- [2] For a frame in which an error signal is received, the TEND flag in SSR_SMCI is not set. Data is retransferred from TDR to TSR allowing automatic data retransmission.
- [3] If no error signal is returned from the receiver, the ERS flag is not set to 1.
- [4] In this case, the SCI determines that transmission of 1-frame data, including the retransfer, is complete, and the TEND flag is set. If the TIE bit in SCR_SMCI is 1, an SCIn_TXI interrupt request is generated. Write transmit data to the TDR to start transmission of the next data.

Figure 27.54 shows an example flow of serial transmission. All the processing steps are automatically performed using an SCIn_TXI interrupt request to activate the DTC.

When the TEND flag in SSR_SMCI is set to 1 in transmission and when the TIE bit in SCR_SMCI is 1, an SCIn_TXI interrupt request is generated.

The DTC is activated by an SCIn_TXI interrupt request if the SCIn_TXI interrupt request is specified as a source of DTC activation beforehand, allowing the transfer of transmit data. The TEND flag is automatically set to 0 when the DTC transfers the data.

If an error occurs, the SCI automatically retransmits the same data. During this retransmission, the TEND flag is kept to 0 and the DTC is not activated. Therefore, the SCI and DTC automatically transmit the specified number of bytes, including retransmission when an error occurs. Because the ERS flag is not automatically cleared, set the RIE bit to 1 before enabling an SCIn_ERI interrupt request to be generated if an error occurs, and clear the ERS flag to 0.

When transmitting/receiving data using the DTC, be sure to enable the DTC before setting the SCI.

For DTC settings, see section 15, Data Transfer Controller (DTC).

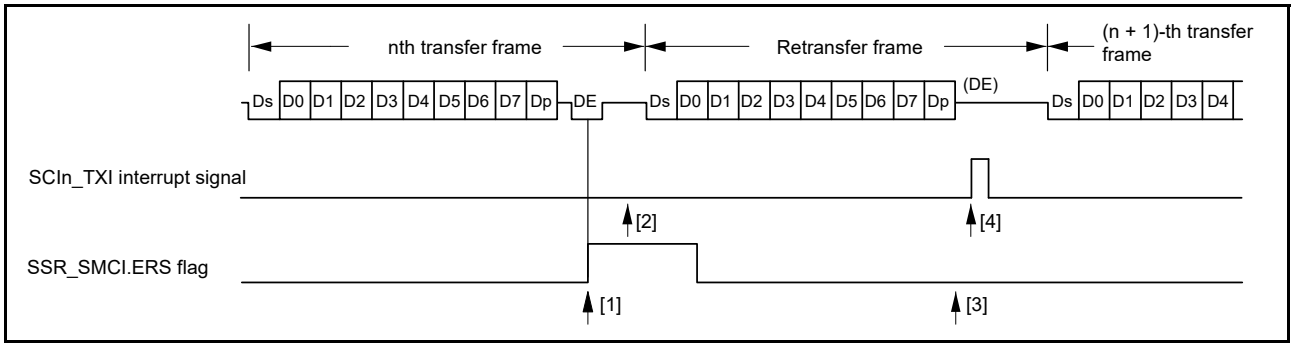


Figure 27.52 Data retransfered operation in SCI transmission mode

Note: The SSR_SMCI.TEND flag is set at different timings depending on the GM bit setting in SMR_SMCI.

Figure 27.53 shows the TEND flag generation timing.

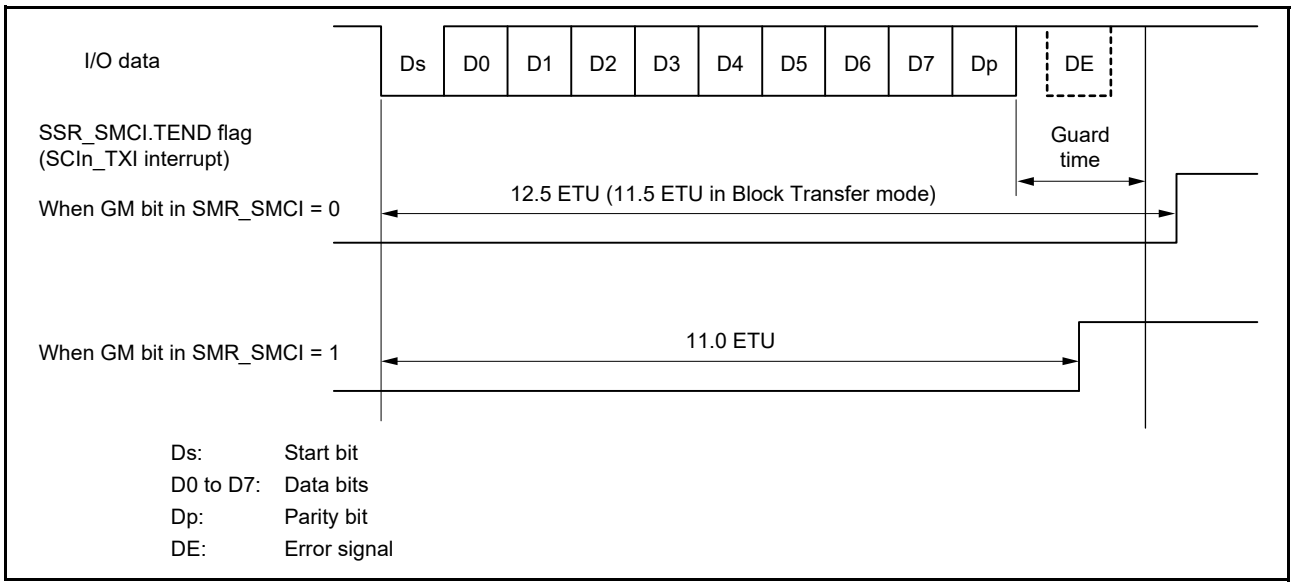


Figure 27.53 SSR.TEND flag generation timing during transmission

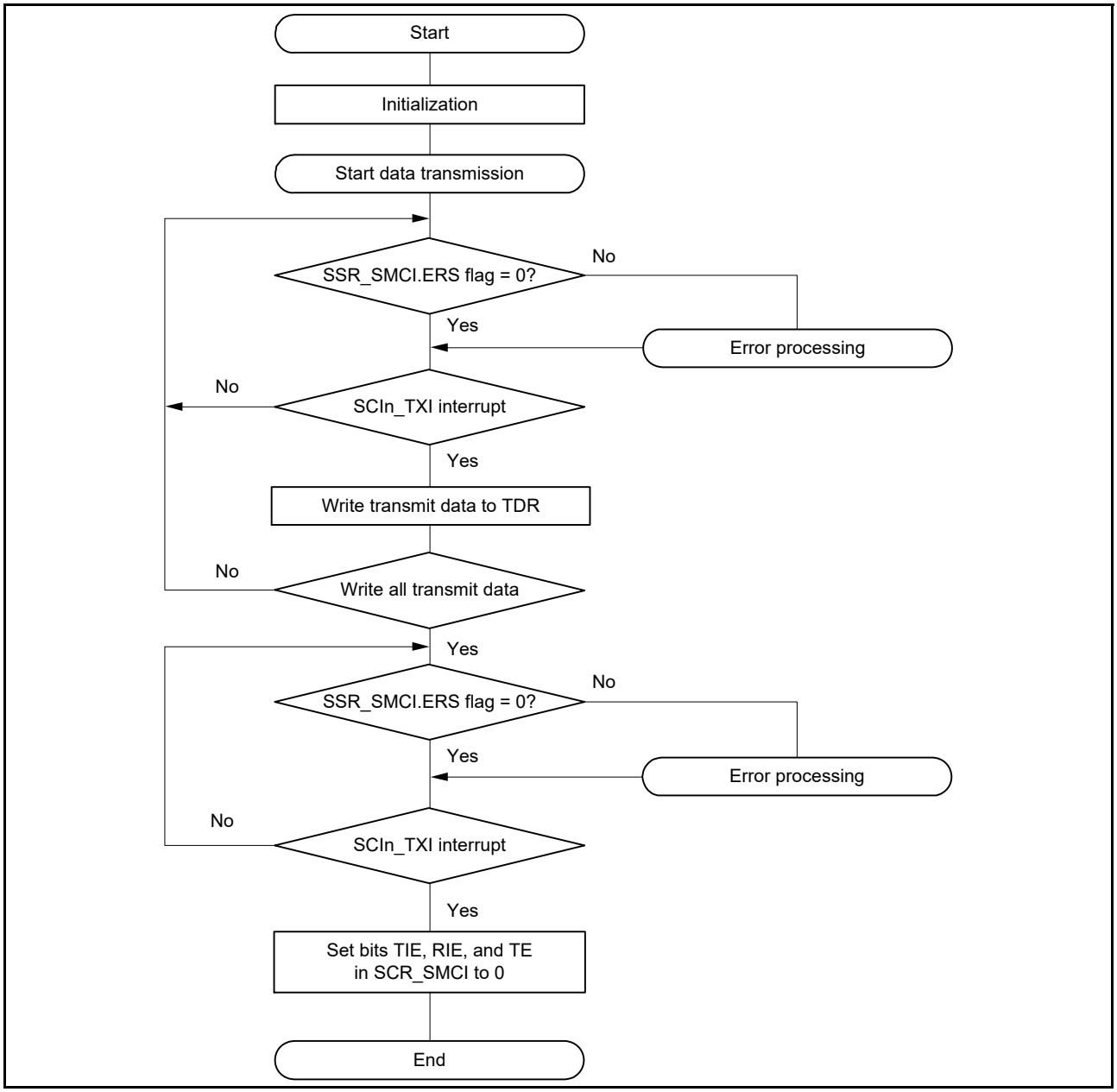


Figure 27.54 Example flow for smart card interface transmission

27.6.7 Serial Data Reception (Except in Block Transfer Mode)

Serial data reception in smart card interface mode is similar to that in non-smart card interface mode. Figure 27.55 shows the data retransfer operation in reception mode.

- [1] If a parity error is detected in the receive data, the PER flag in SSR_SMCI is set to 1. When the RIE bit in SCR_SMCI is 1, an SCIn_ERI interrupt request is generated. Clear the PER flag to 0 before the next parity bit is sampled.
- [2] For a frame in which a parity error is detected, no SCIn_RXI interrupt is generated.
- [3] When no parity error is detected, the PER flag in SSR_SMCI is not set to 1.
- [4] Data is determined to be received successfully. When the RIE bit in SCR_SMCI is 1, an SCIn_RXI interrupt request is generated.

Figure 27.56 shows an example flow for serial data reception. All the processing steps are automatically performed using an SCIn_RXI interrupt request to activate the DTC.

In reception, setting the RIE bit to 1 allows an SCIn_RXI interrupt request to be generated. The DTC is activated by an SCIn_RXI interrupt request if the SCIn_RXI interrupt request is specified as a source of DTC activation beforehand, allowing the transfer of receive data.

If an error occurs during reception and either the ORER or PER flag in SSR_SMCI is set to 1, a receive error interrupt (SCIn_ERI) request is generated. Clear the error flag after the error occurrence. If an error occurs, the DTC is not activated and receive data is skipped. Therefore, the number of bytes of receive data specified in the DTC is transferred.

If a parity error occurs and the PER flag is set to 1 during reception, the receive data is transferred to RDR, therefore allowing the data to be read.

When a reception is forced to terminate by setting the RE bit in SCR_SMCI to 0 during operation, read the RDR register because the received data that is not read might be left in the RDR.

Note: For operations in block transfer mode, see section 27.3.9, Serial Data Reception in Asynchronous Mode.

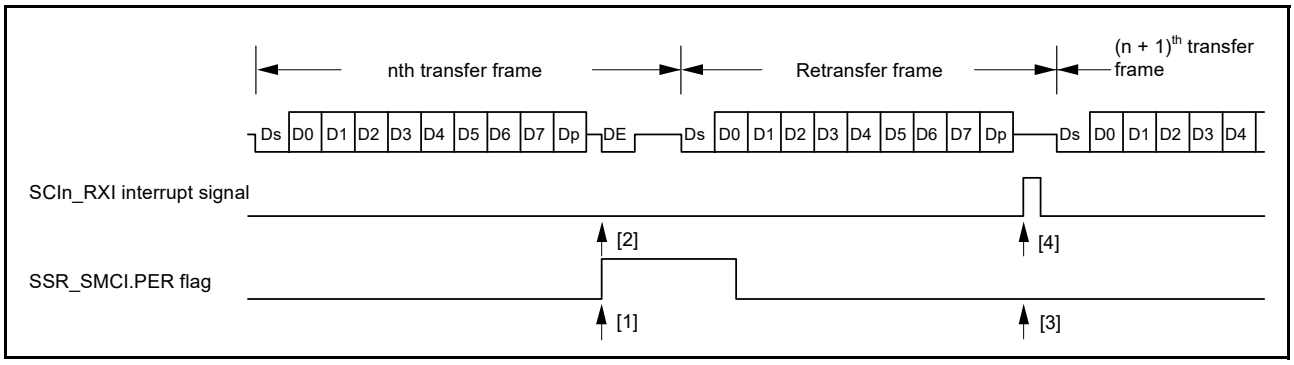


Figure 27.55 Data retransfer operation in SCI reception mode with data retransfer operation during reception

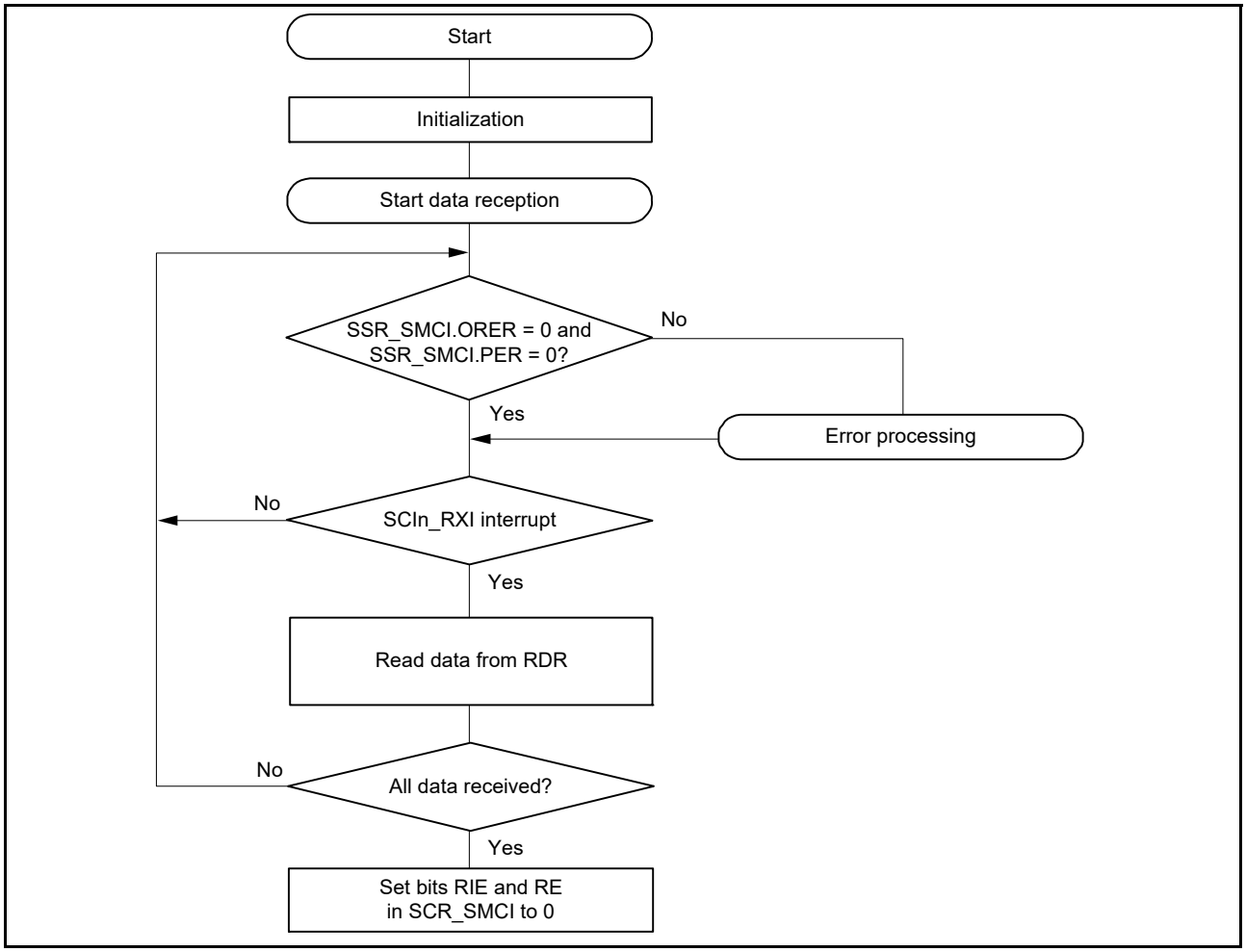


Figure 27.56 Example flow for smart card interface reception

27.6.8 Clock Output Control

When the GM bit in SMR_SMCI is set to 1, the clock output can be controlled by the CKE[1: 0] bits in SCR_SMCI. For details on the CKE[1:0] bits, see section 27.2.12, Serial Control Register for Smart Card Interface Mode (SCR_SMCI) (SCMR.SMIF = 1). When setting the clock output, the base clock described in section 27.6.4, Receive Data Sampling Timing and Reception Margin is output.

Figure 27.57 shows an example timing of the clock output control when the CKE[1] bit in SCR is set to 0, and the CKE[0] bit in SCR_SMCI is controlled.

When the GM bit in SMR_SMCI is 0, output control by the CKE[0] bit in SCR_SMCI is immediately reflected on the SCK pin, so there is a possibility that pulses with an unintended width might be output from the SCK pin.

When the GM bit in SMR_SMCI is 1, the clock with the same pulse width as the base clock is output even if the CKE[0] bit in SCR_SMCI is changed.

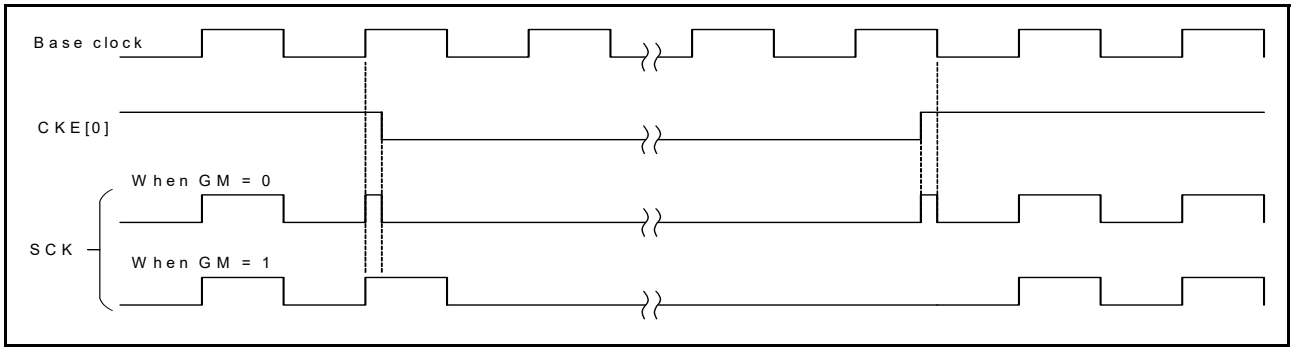


Figure 27.57 Clock output control

27.7 Operation in Simple IIC Mode

Simple I²C bus format is composed of 8 data bits and an acknowledge bit. By continuing into a slave-address frame after a start condition or restart condition, a master device can specify a slave device as the partner for communications. The currently specified slave device remains valid until a new slave device is specified or a stop condition is satisfied. The 8 data bits in all frames are transmitted in order from the MSB.

The I²C bus format and timing of the I²C bus are shown in Figure 27.58 and Figure 27.59.

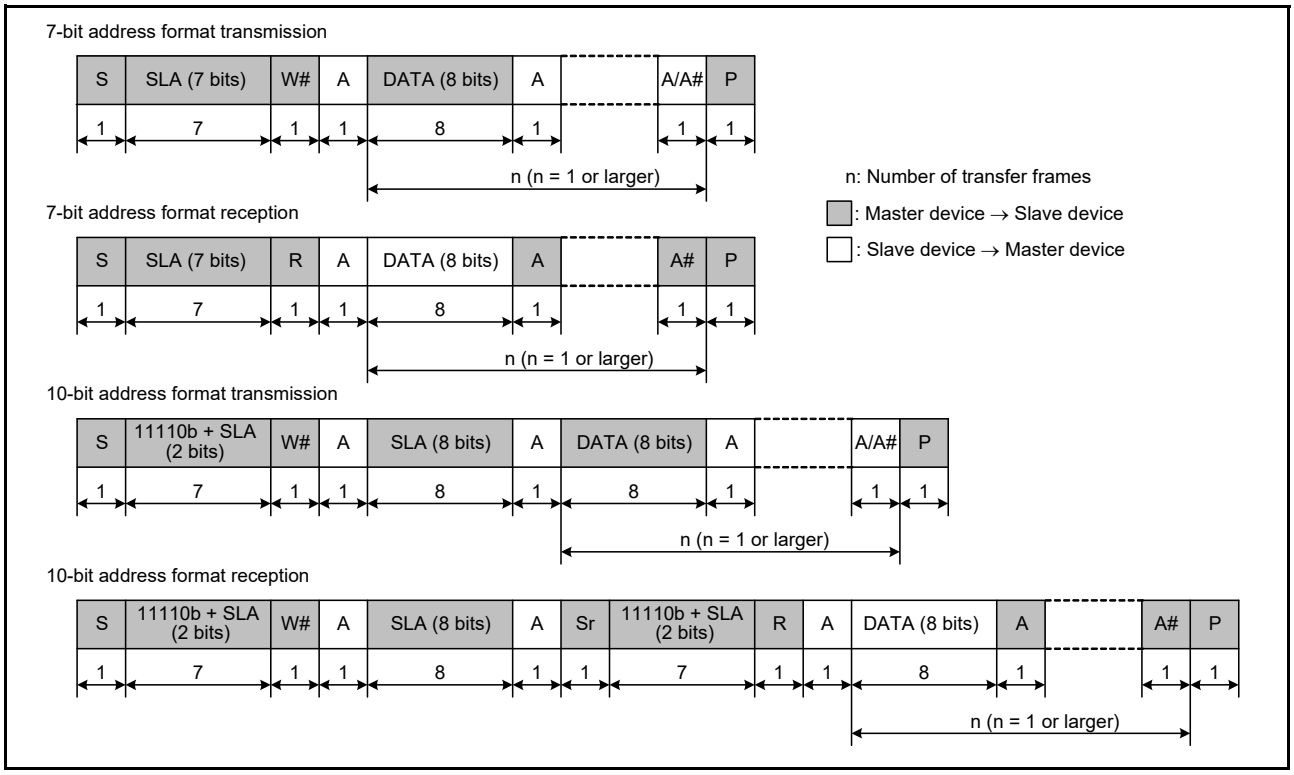


Figure 27.58 I²C bus format

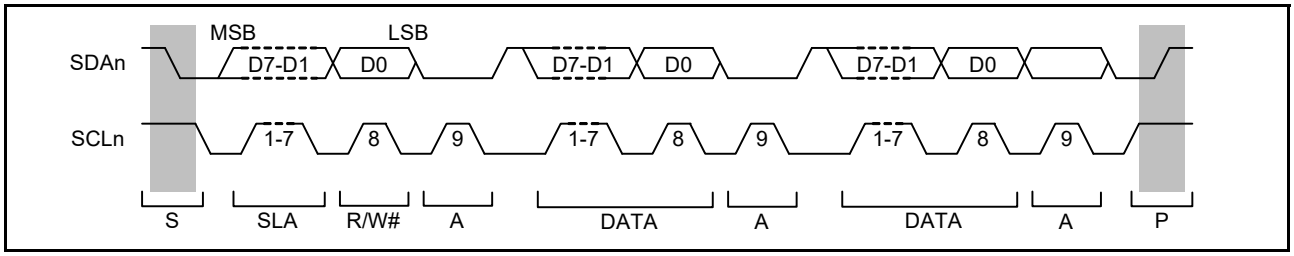


Figure 27.59 I²C bus timing when SLA is 7 bits

S: Indicates a start condition, for example, the master device changes the level on the SDAn line from high to low while the SCLn line is high.

SLA: Indicates a slave address, by which the master device selects a slave device.

R/W#: Indicates the direction of transfer (reception or transmission). The value 1 corresponds to transfer from the slave device to the master device and 0 corresponds to transfer from the master device to the slave device.

A/A#: Indicates an acknowledge bit. This is returned by the slave device for master transmission and by the master device for master reception. Return low indicates ACK and return high indicates NACK.

Sr: Indicates a restart condition, for example, the master device changes the level on the SDAn line from high to low while the SCLn line is high and after the setup time elapses.

DATA: Indicates the data is received or transmitted.

P: Indicates a stop condition, for example, the master device changes the level on the SDAn line from low to high while the SCLn line is high.

27.7.1 Generation of Start, Restart, and Stop Conditions

Writing 1 to the IICSTAREQ bit in SIMR3 causes the generation of a start condition. The generation of a start condition proceeds through the following operations.

- The level on the SDAn line falls (from a high level to a low level) and the SCLn line is kept in the released state
- The hold time for the start condition is set as half of a bit period at the bit rate determined by the BRR setting
- The level on the SCLn line falls (from the high level to the low level), the IICSTAREQ bit in SIMR3 is set to 0, and a start-condition generated interrupt is output.

Writing 1 to the IICRSTAREQ bit in SIMR3 causes the generation of a restart condition. The generation of a restart condition proceeds through the following operations.

- The SDAn line is released and the SCLn line is kept at a low level
- The period at the low level for the SCLn line is set as half of a bit period at the bit rate determined by the BRR setting
- The SCLn line is released (transition from a low to a high level)
- When the high level on the SCLn line is detected, the setup time for the restart condition is set as half of a bit period at the bit rate determined by the BRR setting
- The level on the SDAn line falls (from a high level to a low level)
- The hold time for the restart condition is set as half of a bit period at the bit rate determined by the BRR setting
- The level on the SCLn line falls (from a high level to a low level), the IICRSTAREQ bit in SIMR3 is set to 0, and a restart-condition generated interrupt is output.

Writing 1 to the IICSTPREQ bit in SIMR3 causes the generation of a stop condition. The generation of a stop condition proceeds through the following operations.

- The level on the SDAn line falls (from a high level to a low level) and the SCLn line is kept at the low level
- The period at a low level for the SCLn line is set as half of a bit period at the bit rate determined by the BRR setting

- The SCLn line is released (transition from the low to the high level)
- When the high level on the SCLn line is detected, the setup time for the stop condition is set as half of a bit period at the bit rate determined by the BRR setting
- The SDAn is released (transition from a low to a high level), the IICSTPREQ bit in SIMR3 is set to 0, and a stop-condition generated interrupt is output.

Figure 27.60 shows the timing of operations in the generation of start, restart, and stop conditions.

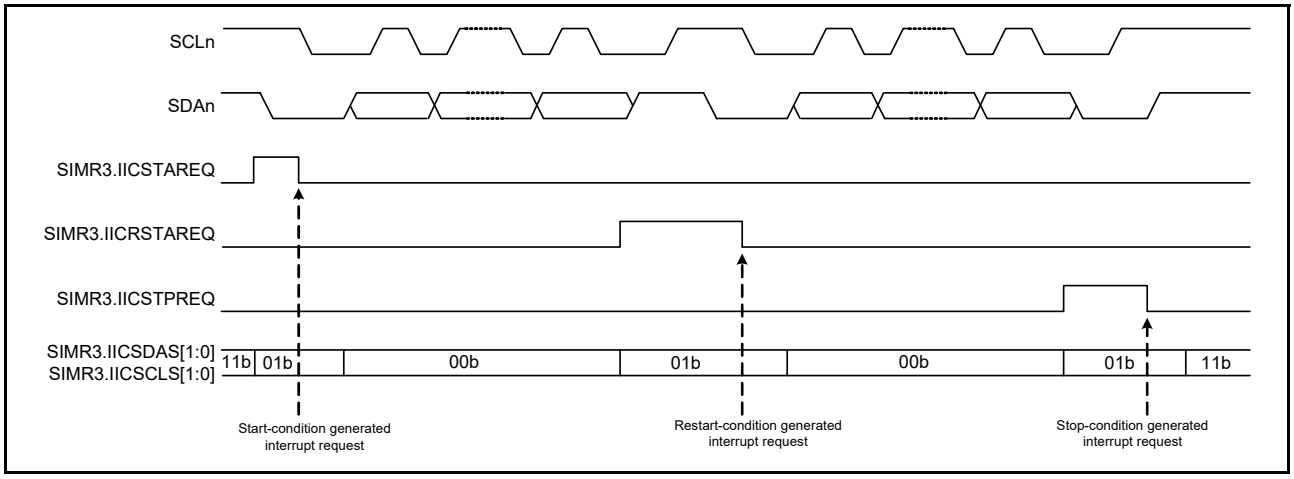


Figure 27.60 Timing operations in generation of start, restart, and stop conditions

27.7.2 Clock Synchronization

The SCLn line can be placed at the low level if a wait is inserted by a slave device at the other side of the transfer. Setting the IICCSC bit in SIMR2 to 1 applies control to obtain synchronization when a difference arises between the levels of the internal SCLn clock signal and the level being input on the SCLn pin.

When the IICCSC bit in SIMR2 is set to 1, the level of the internal SCLn clock signal changes from low to high. Counting to determine the period at a high level stops while the low level is input on the SCLn pin. Counting to determine the period at a high level starts after the transition of the input on the SCLn pin to the high level.

The interval from the time until counting to determine the period at high level starts on the transition of the SCLn pin to the high level is the total of the delay of SCLn output, delay for noise filtering of the input on the SCLn pin (2 or 3 cycles of sampling clock for the noise filter), and delay for internal processing (1 or 2 cycles of PCLKB). The period at high level of the internal SCLn clock is extended even when other devices do not place the low level on the SCLn line.

If the IICCSC bit in SIMR2 is 1, synchronization is obtained for the transmission and reception of data by taking the logical AND of the input on the SCLn pin and the internal SCLn clock. If the IICCSC bit in SIMR2 is 0, synchronization with the internal SCLn clock is obtained for the transmission and reception of data.

If a slave device inserts a wait period into the interval until the transition of the internal SCLn clock signal from the low to the high level after a request for the generation of a start, restart, or stop condition is issued, the time until generation is prolonged by that period.

If a slave device inserts a wait period after the transition of the internal SCLn clock signal from the low to the high level, although the generation-completed interrupt is issued without stopping the waiting period, generation of the condition itself is not guaranteed. Figure 27.61 shows an example of operations to synchronize the clocks.

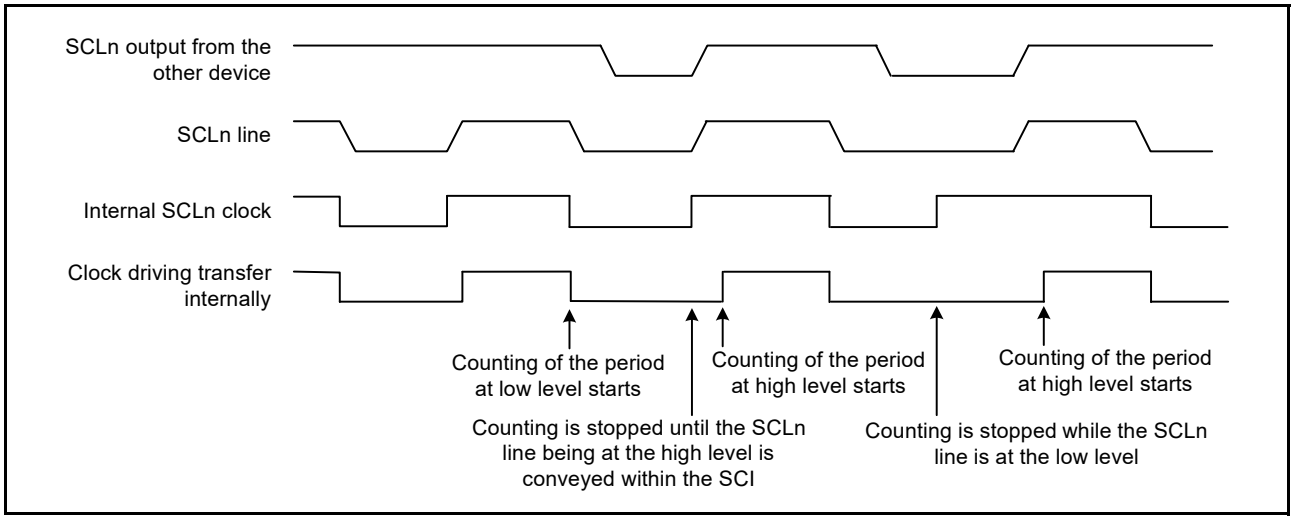


Figure 27.61 Example operations for clock synchronization

27.7.3 SDA Output Delay

The IICDL[4:0] bits in SIMR1 can be used to set a delay for output on the SDAn pin relative to the falling edges of output on the SCLn pin. Delay-time settings from 0 to 31 are selectable, representing periods of the corresponding numbers of cycles of the clock signal from the on-chip baud rate generator (derived by frequency-dividing the base clock, PCLKB, by the divisor selected in the CKS[1:0] bits in SMR). A delay for output on the SDAn pin applies to the start condition/restart condition/stop condition signal, 8-bit transmit data, and an acknowledge bit.

If the SDAn output delay is shorter than the time for the level on the SCLn pin to fall, the change of the output on the SDAn pin starts while the output level on the SCLn pin is falling, creating a possibility of erroneous operation for slave devices. Ensure that settings for the delay of output on the SDAn pin specify times greater than the time output on the SCLn pin takes to fall (300 ns for IIC in standard mode and fast mode).

Figure 27.62 shows the timing of delays in SDAn output.

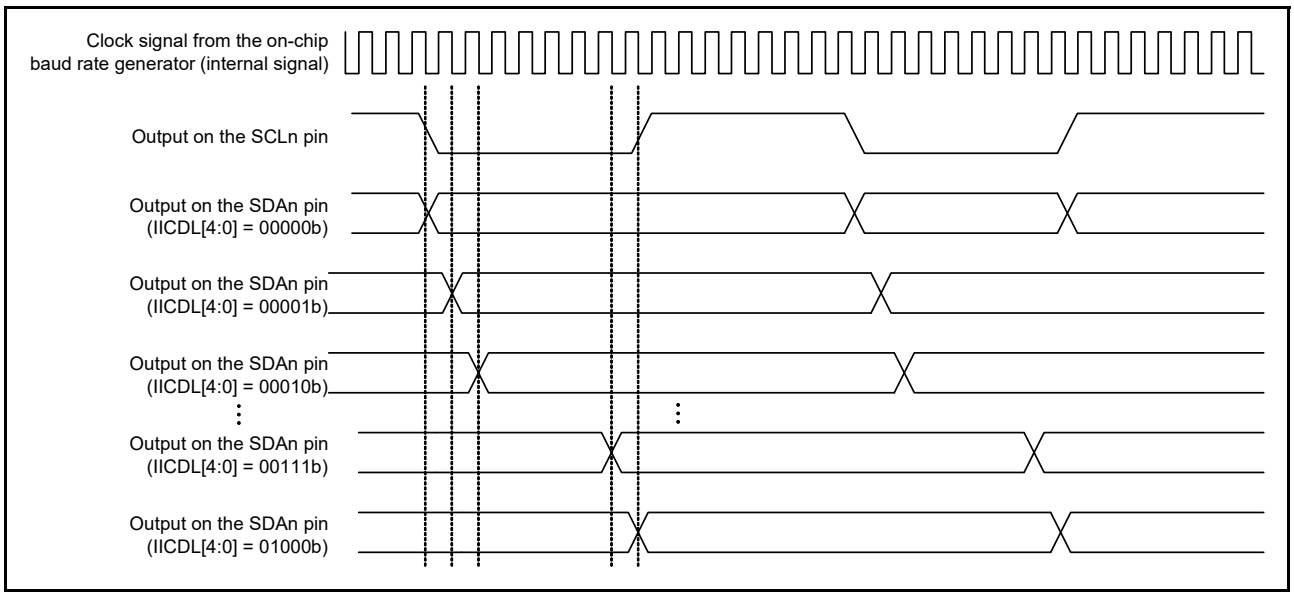


Figure 27.62 Timing of delays in SDAn output

27.7.4 SCI Initialization in Simple IIC Mode

Before transferring data, write the initial value 00h to SCR and initialize the interface following the example shown in Figure 27.63.

Before making any changes to the operating mode, or transfer format for example, be sure to set SCR to its initial value. In simple IIC mode, the open-drain setting for the communication ports should be made on the port side.

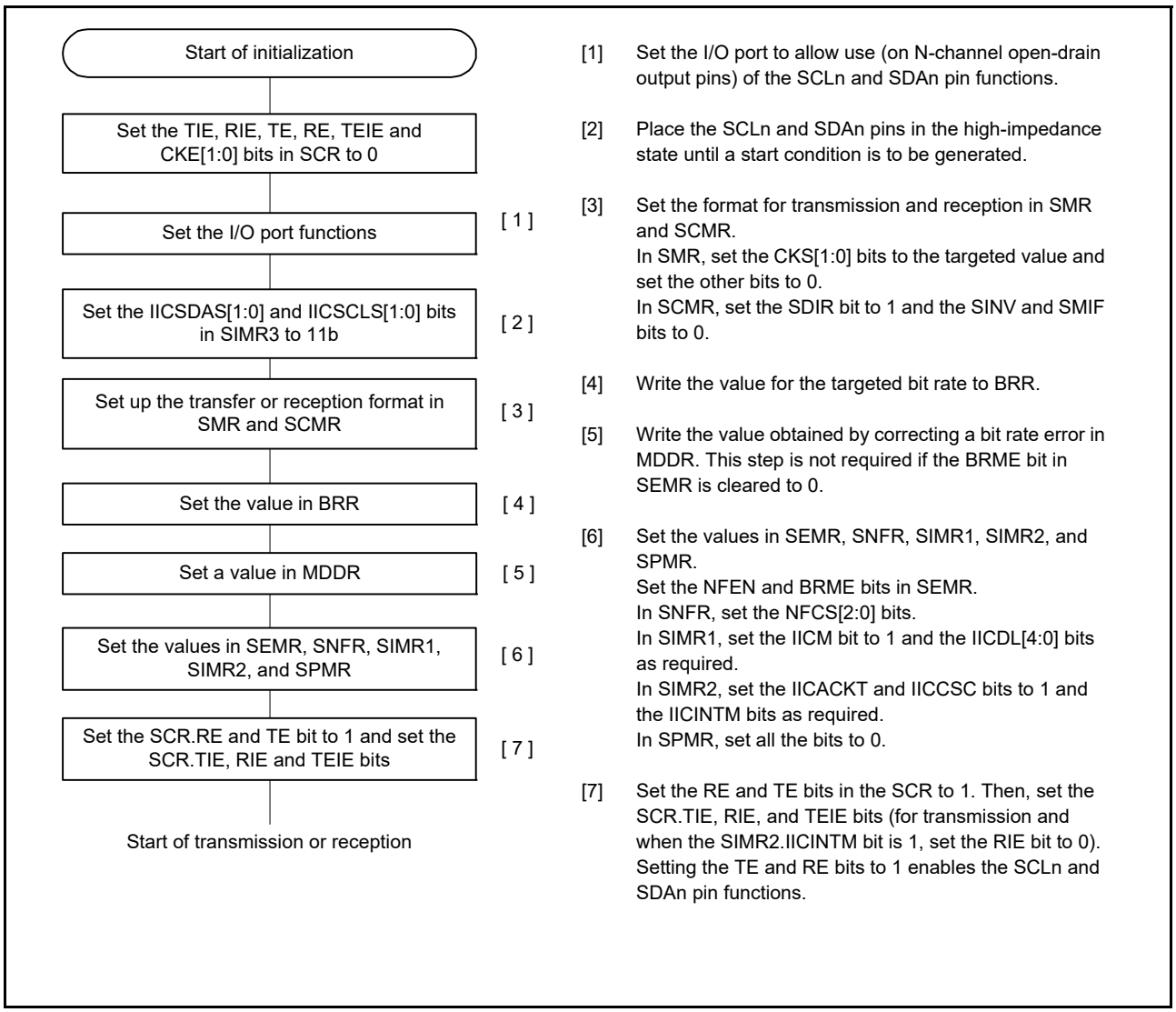


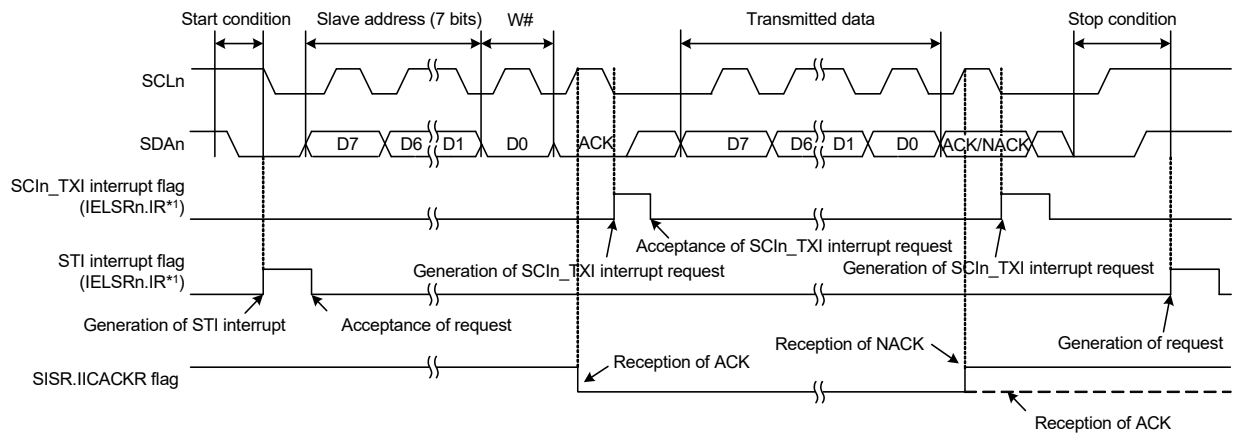
Figure 27.63 Example flow for SCI initialization in simple IIC mode

27.7.5 Operation in Master Transmission in Simple IIC Mode

Figure 27.64 and Figure 27.65 show examples of master transmission and Figure 27.66 is an example flow of data transmission. The value of the SIMR2.IICINTM bit is assumed to be 1 (use reception and transmission interrupts) and the value of the SCR.RIE bit is assumed to be 0 (SCIn_RXI and SCIn_ERI interrupt requests are disabled). See Table 27.29 for more information on the STI interrupt.

When 10-bit slave addresses are in use, steps [3] and [4] in Figure 27.66 are repeated twice.

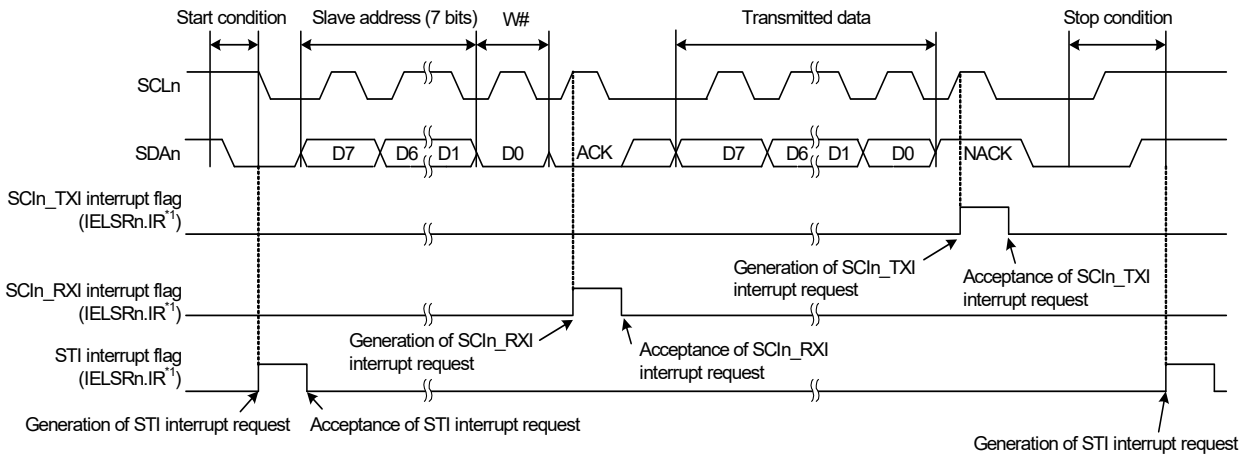
In simple IIC mode, the transmit data empty interrupt (SCIn_TXI) is generated when communication of one frame is complete, unlike the SCIn_TXI interrupt request generation timing during clock synchronous transmission.



Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 27.64 Example 1 of operations for master transmission in simple IIC mode with 7-bit slave addresses, transmission interrupts, and reception interrupts

When the SIMR2.IICINTM bit is set to 0 (use ACK/NACK interrupts) during master transmission, the DTC is activated by the ACK interrupt as the trigger and the required number of data bytes are transmitted. When a NACK is received, error processing, such as transmission stop and retransmission, is performed using the NACK interrupt as the trigger.



Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 27.65 Example 2 of operations for master transmission in simple IIC mode with 7-bit slave addresses, ACK interrupts, and NACK interrupts

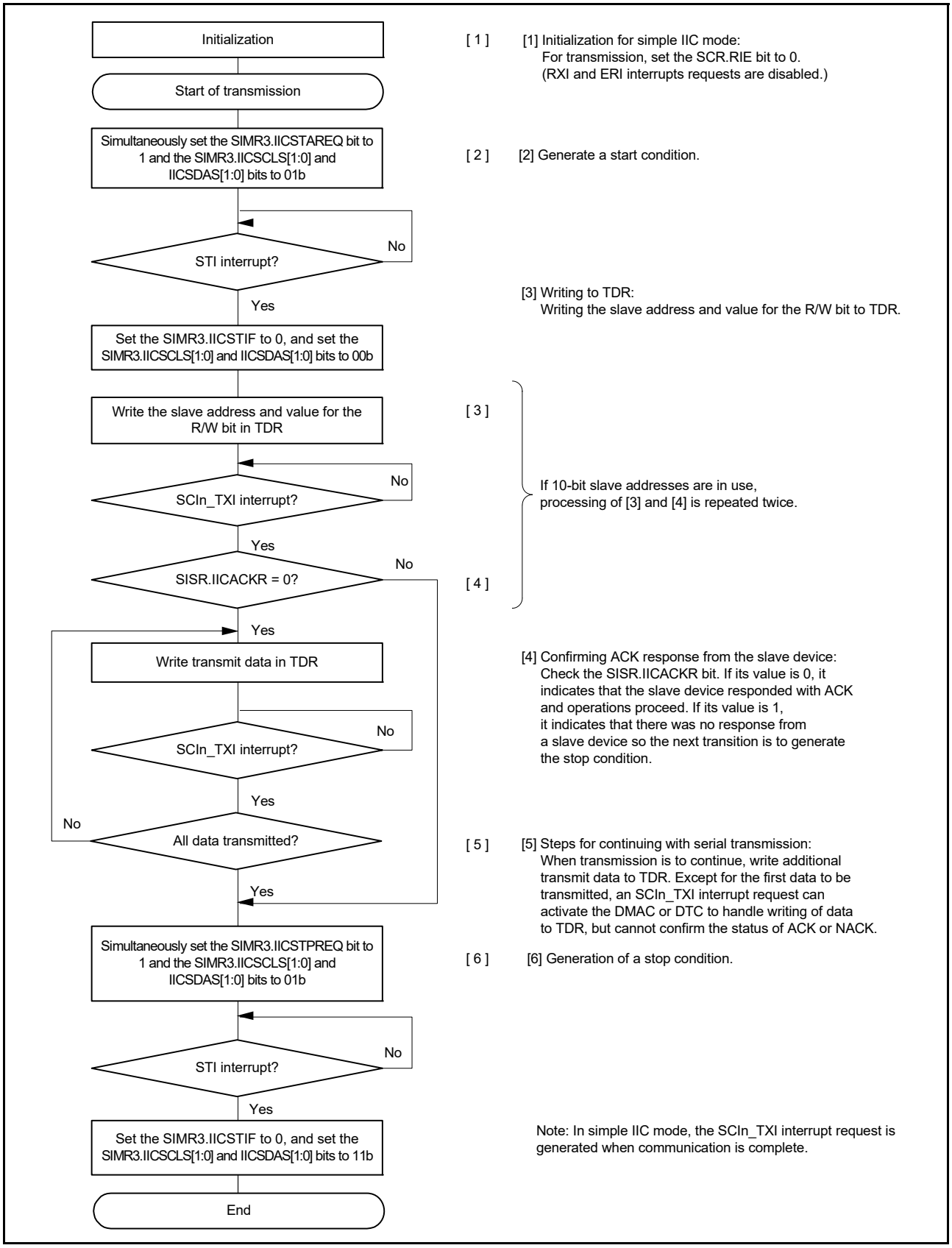


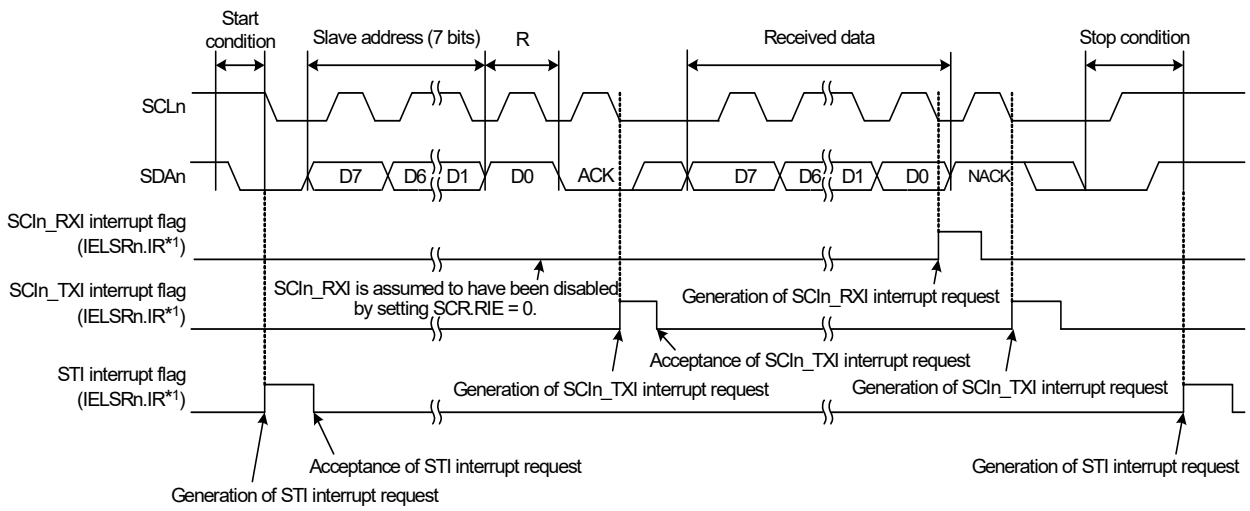
Figure 27.66 Example procedure for master transmission in simple IIC mode with transmission interrupts and reception interrupts

27.7.6 Master Reception in Simple IIC Mode

Figure 27.67 shows an example operation in simple IIC mode master reception and Figure 27.68 shows an example flow of master reception.

The value of the SIMR2.IICINTM bit is assumed to be 1 (use reception and transmission interrupts).

In simple IIC mode, the transmit data empty interrupt (SCIn_TXI) is generated when communication of one frame is complete, unlike the SCIn_TXI interrupt request generation timing during clock synchronous transmission.



Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 27.67 Example operations for master reception in simple IIC mode with 7-bit slave addresses, transmission interrupts, and reception interrupts

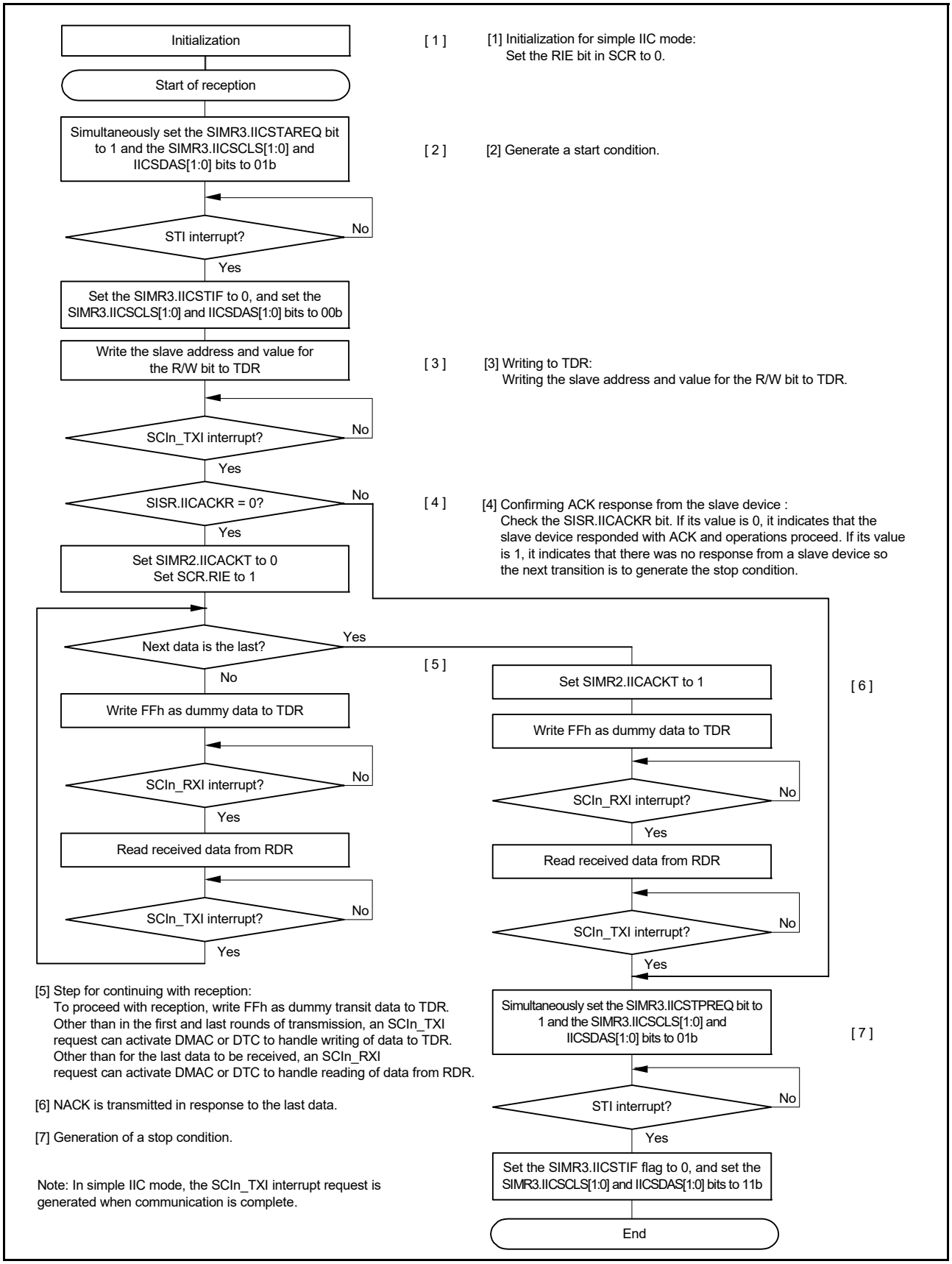


Figure 27.68 Example flow for master reception in simple IIC mode with transmission interrupts and reception interrupts

27.8 Operation in Simple SPI Mode

As an extended function, the SCI supports a simple SPI mode that handles transfer among one or multiple master devices and multiple slave devices.

Using the settings for clock synchronous mode (SCMR.SMIF = 0, SIMR1.IICM = 0, SMR.CM = 1) plus setting the SSE bit in the SPMR to 1 places the SCI in simple SPI mode. However, the SSn pin function on the master side is not required for connection of the device used as the master in simple SPI mode when the configuration only has a single master, therefore set the SSE bit in the SPMR to 0 in such cases.

Figure 27.69 shows an example of connections for simple SPI mode. Control a general port pin to produce the SSn output signal from the master.

In simple SPI mode, data is transferred in synchronization with clock pulses in the same way as in clock synchronous mode. One character of data for transfer consists of 8 bits of data, and parity bits cannot be appended to this. The data can be inverted by setting the SCMR.SINV bit to 1.

Because the receiver and transmitter are independent of each other within the SCI module, full-duplex communications are possible, with a common clock signal. Additionally, because both the transmitter and receiver have a buffered structure, writing the next transmit data while transmission is in progress and reading previously received data while reception is in progress are both possible. This enables continuous transfer.

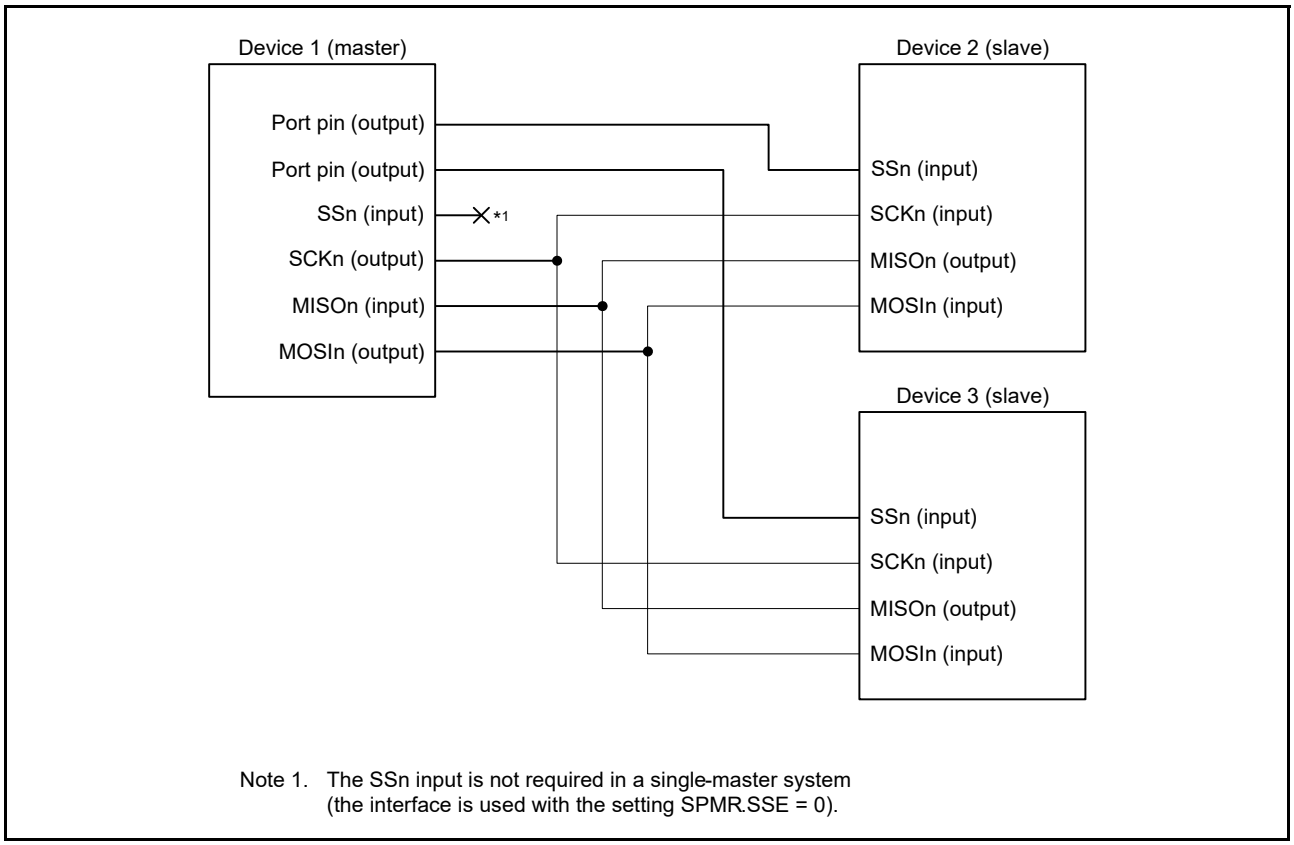


Figure 27.69 Example of connections using simple SPI mode in single master mode with SPMR.SSE bit = 0

27.8.1 States of Pins in Master and Slave Modes

The direction (input or output) of pins for the simple SPI mode interface differs according to whether the device is a master (SCR.CKE[1:0] = 00b or 01b and SPMR.MSS = 0) or slave (SCR.CKE[1:0] = 10b or 11b and SPMR.MSS = 1).

Table 27.25 lists the relationship between the pin states, mode, and the input level on the SSn pin.

Table 27.25 States of pins by mode and input level on SSn pin

Mode	Input on SSn pin	State of TXDn pin	State of RXDn pin	State of SCKn pin
Master mode*1	High level (transfer can proceed)	Output for data transmission*2	Input for received data	Clock output*3
	Low level (transfer cannot proceed)	High-impedance	Input for received data (but disabled)	High-impedance
Slave mode	High level (transfer cannot proceed)	Input for received data (but disabled)	High-impedance	Clock input (but disabled)
	Low level (transfer can proceed)	Input for received data	Output for data transmission	Clock input

Note 1. When there is only a single master (SPMR.SSE = 0), transfer is possible regardless of the input level on the SSn pin. This is equivalent to input of a high level on the SSn pin. Because the SSn pin function is not required, the pin is available for other purposes.
Note 2. The MOSIn pin output is in the high-impedance state when serial transmission is disabled (SCR.TE bit = 0).
Note 3. The SCKn pin output is in the high-impedance state when serial transmission is disabled (SCR.TE and RE bits = 00b) in a multi-master configuration (SPMR.SSE = 1).

27.8.2 SS Function in Master Mode

Setting the CKE[1:0] bits in the SCR to 00b and the MSS bit in the SPMR to 0 selects master operation. The SSn pin is not used in single-master configurations (SPMR.SSE = 0), so transmission or reception can proceed regardless of the value of the SSn pin.

When the level on the SSn pin is high in a multi-master configuration (SPMR.SSE = 1), a master device outputs clock signals from the SCKn pin before starting transmission or reception to indicate that there are no other masters or another master is performing reception or transmission. When the level on the SSn pin is low in a multi-master configuration (SPMR.SSE = 1), there are other masters, and this indicates that transmission or reception is in progress. At this time the MOSIn output and SCKn pins are placed in the high-impedance state and starting transmission or reception is not possible. Additionally, the value of the SPMR.MFF bit is 1, indicating a mode fault error. In a multi-master configuration, start error processing by reading SPMR.MFF flag. Even if a mode fault error occurs while transmission or reception is in progress, transmission or reception does not stop, but the MOSIn and SCKn pin output are placed in the high-impedance state after completion of the transfer. Control a general port pin to produce the SS output signal from the master.

27.8.3 SS Function in Slave Mode

Setting the CKE[1:0] bits in the SCR to 10b and the MSS bit in the SPMR to 1 selects slave operation. When the level on the SSn pin is high, the MISOn output pin is in the high-impedance state and clock input through the SCKn pin is ignored. When the level on the SSn pin is low, clock input through the SCKn pin is effective and transmission or reception can proceed.

If the input on the SSn pin changes from low to high level during transmission or reception, the MISOn output pin is placed in the high-impedance state. Meanwhile, the internal processing for transmission or reception continues at the rate of the clock input through the SCKn pin until processing for the current transmitted or received character is complete, after which it stops, and the appropriate interrupt (SCIn_TXI, SCIn_RXI, and SCIn_TEI) is then generated.

27.8.4 Relationship between Clock and Transmit/Receive Data

The CKPOL and CKPH bits in the SPMR can be used to set up the clock for use in transmission and reception in four different ways. The relation between the clock signal and the transmission and reception of data is shown in Figure 27.70. The relation is the same for both master and slave operation. This is the same as when the level on the SSn pin is high.

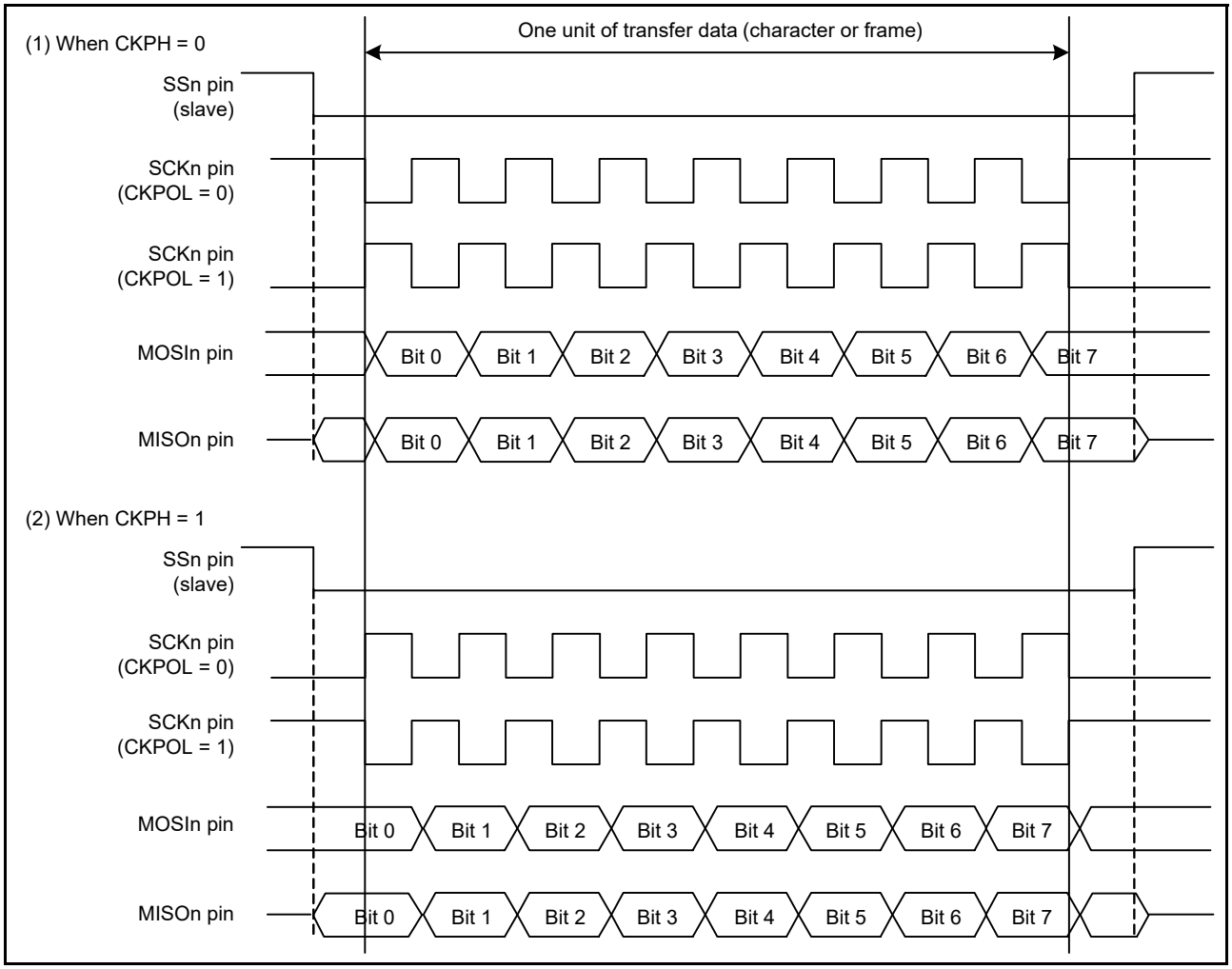


Figure 27.70 Relation between clock signal and transmit/receive data in simple SPI mode

27.8.5 SCI Initialization in Simple SPI Mode

SCI initialization in simple SPI mode is the same as in clock synchronous mode. See Figure 27.32. The CKPOL and CKPH bits in the SPMR must be set to ensure that the clock signal is suitable for both master and slave devices.

Always initialize the SCR register before making any changes to the operating mode or transfer format.

Note 1. Only the RE bit is set to 0. The SSR.ORER, FER, PER, and RDR flags are not initialized.
Note 2. Changing the value of the TE bit from 1 to 0 or from 0 to 1 leads to the generation of a transmit data empty interrupt (SCIn_TXI) if the value of the TIE bit in the SCR is 1 at the time.

27.8.6 Transmission and Reception of Serial Data in Simple SPI Mode

In master operation, ensure that the SSn pin of the slave device on the other side of the transfer is at a low level before starting the transfer and at a high level on completion of the transfer. Otherwise, the procedures are the same as in clock synchronous mode.

27.9 Bit Rate Modulation Function

Using the bit rate modulation function, the bit rate can be evenly corrected using the number specified in the MDDR register when the PCLKB is selected in the CKS[1:0] bits in SMR/SMR_SMCI.

Figure 27.71 shows an example where the PCLKB is selected in the CKS[1:0] bits in SMR/SMR_SMCI and the BRR bit is set to 0, and the MDDR is set to 160 in asynchronous mode. In this example, the cycle of the base clock is evenly corrected (256/160) and the bit rate is also corrected (160/256).

Note: Enabling an internal clock causes bias and expansion. Contraction is generated in the pulse width of the internal base clock.

Do not use this function in clock synchronous mode and in the highest speed settings in simple SPI mode (SMR.CKS[1:0] = 00b, SCR.CKE[1] = 0, and BRR = 0).

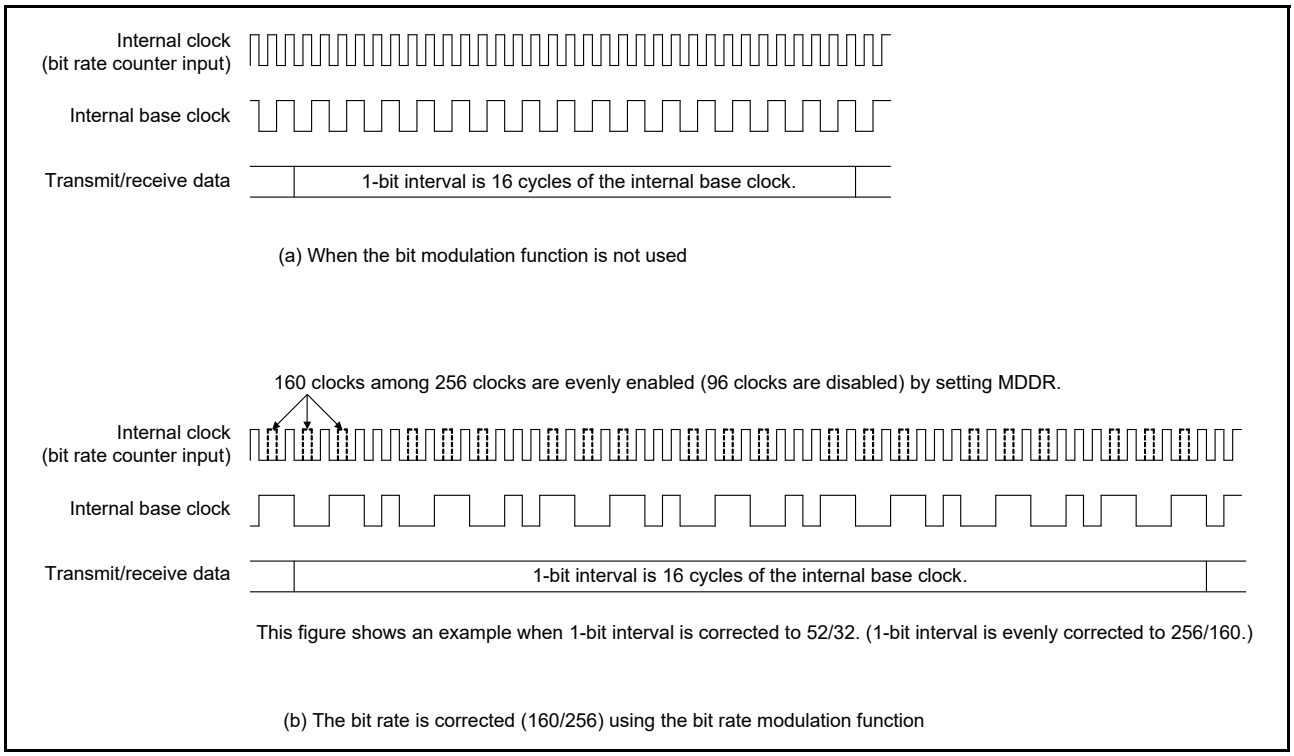


Figure 27.71 Example of internal base clock when bit rate modulation function is used

27.10 Interrupt Sources

27.10.1 Buffer Operations for SCIn_TXI and SCIn_RXI Interrupts (non-FIFO selected)

If the conditions for an SCIn_TXI and SCIn_RXI interrupt are satisfied while the interrupt status flag in the Interrupt Controller Unit (ICU) is 1, the ICU does not output the interrupt request but retains it internally (with a capacity for retention of one request per source).

When the value of the interrupt status flag in the ICU becomes 0, the interrupt request retained within the ICU is output. The internally retained interrupt request is automatically discarded when the actual interrupt is output. Clearing of the associated interrupt enable bit (the TIE or RIE bit in the SCR/SCR_SMCI) can also be used to discard an internally retained interrupt request.

27.10.2 Buffer Operations for SCIn_TXI and SCIn_RXI Interrupts (FIFO selected)

Even when an interrupt status flag in the ICU is set to 1, the SCIn_TXI and SCIn_RXI interrupts do not output interrupt requests to the ICU. When an interrupt status flag of the interrupt controller is set to 0, and if the conditions for an SCIn_TXI and SCIn_RXI interrupts are satisfied, an interrupt request is generated.

27.10.3 Interrupts in Asynchronous, Clock Synchronous, and Simple SPI Modes

(1) Non-FIFO selected

lists interrupt sources in asynchronous, clock synchronous, and simple SPI modes. A different interrupt vector can be assigned to each interrupt source. Individual interrupt sources can be enabled or disabled with the enable bits in SCR.

If the SCR.TIE bit is 1, an SCIn_TXI interrupt request is generated when transmit data is transferred from the TDR or TDRHL register*1 to the TSR. An SCIn_TXI interrupt request can also be generated using a single instruction to set the

SCR.TE and SCR.TIE bits to 1 simultaneously. An SCIn_TXI interrupt request can activate the DTC to handle data transfer.

An SCIn_TXI interrupt request is not generated by setting SCR.TE to 1 when SCR.TIE is 0 or by setting SCR.TIE to 1 when SCR.TE is 1.*2

When new data is not written by the time of transmission of the last bit of the current transmit data and SCR.TEIE is 1, the SSR.TEND flag becomes 1 and an SCIn_TEI interrupt request is generated. Additionally, when SCR.TE is 1, the SSR.TEND flag retains the value 1 until additional transmit data are written to the TDR or TDRHL register*1, and setting the SCR.TEIE bit to 1 leads to the generation of an SCIn_TEI interrupt request.

Writing data to the TDR or TDRHL register*1 leads to clearing of the SSR.TEND flag and, after a certain time, discarding of the SCIn_TEI interrupt request.

If the SCR.RIE bit is 1, an SCIn_RXI interrupt request is generated when received data is stored in the RDR. An SCIn_RXI interrupt request can activate the DTC to handle data transfer.

Setting any of the ORER, FER, and PER flags in the SSR to 1 when the SCR.RIE bit is 1 leads to the generation of an SCIn_ERI interrupt request. An SCIn_RXI interrupt request is not generated at this time. Clearing all three flags (ORER, FER, and PER) leads to discarding of the SCIn_ERI interrupt request.

(2) FIFO selected

Table 27.6 lists interrupt sources in FIFO selected mode.

If the SCR.TIE bit is 1, an SCIn_TXI interrupt request is generated when the stored number of data in FTDRL register becomes the threshold value indicated in FCR.TTRG or below. An SCIn_TXI interrupt request can also be generated using a single instruction to set the SCR.TIE and SCR.TE bits to 1 simultaneously or by setting SCR.TIE to 1 when SCR.TE is 1.

An SCIn_TXI interrupt request is not generated by setting SCR.TE to 1 while SCR.TIE is 0.

If SCR.TEIE bit is 1 and if the next data is not written to the FTDRL register by the time the last bit of the transmit data is sent, the SSR_FIFO.TEND flag is set to 1 and the SCIn_TEI interrupt request is generated.

If SCR.RIE bit is 1, the SCIn_RXI interrupt request is generated when the stored number of data in the FRDRL register is equal to or greater than the threshold value indicated in FCR.RTRG. When RTRG is set to 0, an SCIn_RXI interrupt does not occur even when the amount of data in the receive FIFO is equal to 0.

If the SCR.RIE bit is 1, when the SSR_FIFO.ORER flag is set to 1 or data with a framing error or a parity error is stored in the FRDRL register, the SCIn_ERI interrupt request is generated. When the number of data stored in the FRDRL register at this time is at the threshold value or above, the SCIn_RXI interrupt request is also generated. The SCIn_ERI interrupt request can be canceled in which case SSR_FIFO.ORER, FER, and PER flags are all cleared.

Note 1. When asynchronous mode and 9-bit data length are selected.
Note 2. To temporarily prohibit SCIn_TXI interrupts on transmission of the last of the data when a new round of transmission is to be started, after handling the transmission-completed interrupt, control activation of the interrupt by using the interrupt request enable bit in the ICU rather than using the SCR.TIE bit. This approach can prevent the suppression of SCIn_TXI interrupt requests in the transfer of new data.

Table 27.26 SCI interrupt sources with non-FIFO selected

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC activation
SCIn_ERI	Receive error*1	ORER, FER, PER, DFER, DPER	RIE	Not possible
SCIn_RXI	Receive data full	RDRF	RIE	Possible
	Address match	DCMF	RIE	Possible
SCIn_AM	Address match	DCMF	—	Possible
SCIn_TXI	Transmit data empty	TDRE	TIE	Possible
SCIn_TEI	Transmit end	TEND	TEIE	Not possible

Note 1. The interrupt flag is only ORER when in clock synchronous mode and simple SPI mode.

Table 27.27 SCI interrupt sources with FIFO selected

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC activation
SCIn_ERI	Receive error*1	ORER, FER, PER, DFER, DPER	RIE	Not possible
		DR (when FCR.DRES = 1)	RIE	Not possible
SCIn_RXI	Receive data full	RDF	RIE	Possible
	Receive data ready	DR (when FCR.DRES = 0)	RIE	Possible
	Address match	DCMF	RIE	Possible
SCIn_AM	Address match	DCMF	—	Possible
SCIn_TXI	Transmit data empty	TDFE	TIE	Possible
SCIn_TEI	Transmit end	TEND	TEIE	Not possible

Note 1. The interrupt flag is only ORER when in clock synchronous mode and simple SPI mode.

27.10.4 Interrupts in Smart Card Interface Mode

Table 27.28 lists interrupt sources in smart card interface mode. A transmit end interrupt (SCIn_TEI) request and an address match (SCIn_AM) request cannot be used in this mode.

Table 27.28 SCI interrupt sources in smart card interface mode

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC activation
SCIn_ERI	Receive error or error signal detection	ORER, FER, ERS	RIE	Not possible
SCIn_RXI	Receive data full	RDRF	RIE	Possible
SCIn_TXI	Transmit end	TEND	TIE	Possible

Data transmission/reception using the DTC is also possible in smart card interface mode. In transmission, when the TEND flag in SSR_SMCI is set to 1, an SCIn_TXI interrupt request is generated. This SCIn_TXI interrupt request activates the DTC allowing transfer of transmit data if the SCIn_TXI request is specified beforehand as a source of DTC activation. The TEND flag is automatically set to 0 when the DTC transfers the data.

If an error occurs, the SCI automatically retransmits the same data. During the retransmission, the TEND flag is kept at 0 and the DTC is not activated. Therefore, the SCI and DTC automatically transmit the specified number of bytes, including retransmission when errors occur. However, the ERS flag in SSR_SMCI is not automatically cleared to 0 at error occurrence. Therefore, the ERS flag must be cleared by previously setting the RIE bit in SCR_SMCI to 1 to enable an SCIn_ERI interrupt request to be generated at error occurrence.

When transmitting or receiving data using the DTC, always enable the DTC before making the SCI settings. For DTC settings, see section 15, Data Transfer Controller (DTC).

In reception, an SCIn_RXI interrupt request is generated when receive data is set to RDR. The SCIn_RXI interrupt request activates the DTC allowing the transfer of receive data if the SCIn_RXI request is previously specified as a source of DTC activation. If an error occurs, the error flag is set. Therefore, the DTC is not activated and an SCIn_ERI interrupt request is issued to the CPU instead. The error flag must be cleared.

27.10.5 Interrupts in Simple IIC Mode

Table 27.29 lists the interrupt sources in simple IIC mode. The STI interrupt is allocated to the transmit end interrupt (SCIn_TEI) request. The receive error interrupt (SCIn_ERI) and the address match (SCIn_AM) request cannot be used.

The DTC can also be used to handle transfer in simple IIC mode.

When the IICINTM bit in SIMR2 is 1:

- An SCIn_RXI request is generated on the falling edge of the SCLn signal for the 8th bit. If SCIn_RXI is previously set up as an activation source for the DTC, the SCIn_RXI request activates the DTC to handle transfer of the received data.
- An SCIn_TXI request is generated on the falling edge of the SCLn signal for the 9th bit (acknowledge bit). If SCIn_TXI is previously set up as an activation source for the DTC, the SCIn_TXI request activates the DTC to

handle transfer of the transmit data.

When the IICINTM bit in SIMR2 is 0:

- An SCIn_RXI request (ACK detection) is generated if the input on the SDAn pin is low on the rising edge of the SCLn signal for the 9th bit (acknowledge bit)
- An SCIn_TXI request (NACK detection) is generated if the input on the SDAn pin is high on the rising edge of the SCLn signal for the 9th bit (acknowledge bit)
- If the SCIn_RXI is previously set up as an activation source for the DTC, the SCIn_RXI request activates the DTC to handle transfer of the received data.

If the DTC is used for data transfer in reception or transmission, always set up and enable the DTC before setting up the SCI.

When the IICSTAREQ, IICRSTAREQ, and IICSTPREQ bits in SIMR3 are used to generate a start condition, restart condition, or stop condition, the STI request is issued when generation is complete.

Table 27.29 SCI interrupt sources in simple IIC mode

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC activation
SCIn_RXI	Reception, ACK detection	—	RIE	Possible
SCIn_TXI	Transmission, NACK detection	—	TIE	Possible
STIn	Completion of generation of a start, restart, or stop condition	IICSTIF	TEIE	Not possible

Note: Activation of the DTC is only possible when the SIMR2.IICINTM bit is 1 (use reception and transmission interrupts).

27.11 Event Linking

By using interrupt request signals as event signals, the SCI can provide linked operation through the Event Link Controller (ELC) for modules selected in advance.

Event signals can be output regardless of the values of the associated interrupt request enable bits.

(1) Error event output (receive error or error signal detected)

- Indicates abnormal termination because of a parity error during reception in asynchronous mode
- Indicates abnormal termination because of a framing error during reception in asynchronous mode
- Indicates abnormal termination because of an overrun error during reception
- Indicates detection of the error signal during transmission in smart card interface mode
- The SSR_FIFO.FER and PER flags are 0, and receive data less than the receive FIFO data trigger number is set in a reception FIFO buffer, and it indicates that time of 15 ETUs elapse when FIFO is selected and FCR.DRES is 1.

(2) Receive data full event output

- Indicates that ACK is detected if the SIMR2.IICINTM bit is 0 in simple IIC mode
- Indicates that the 8th bit SCLn falling edge is detected if the SIMR2.IICINTM bit is 1 in simple IIC mode
- When the SIMR2.IICINTM bit is 1 during master transmission in simple IIC mode, set the ELC so that receive data full events are not used.

(a) Non-FIFO selected

- Indicates that received data is set in the Receive Data Register (RDR or RDRHL).

(b) FIFO selected

- Using this event output is prohibited.

(3) Transmit data empty event output

- Indicates that the SCR/SCR_SMCI.TE bit is changed from 0 to 1
- Indicates that transmission is complete in smart card interface mode

- Indicates that NACK is detected if the SIMR2.IICINTM bit is 0 in simple IIC mode
- Indicates that the 9th bit SCLn falling edge is detected if the SIMR2.IICINTM bit is 1 in simple IIC mode.

(a) Non-FIFO selected

- Indicates that transmit data is transferred from the Transmit Data Register (TDR or TDRHL) to the Transmit Shift Register (TSR).

(b) FIFO selected

- Using this event output is prohibited.

(4) Transmit end event output

- Indicates the completion of transmission
- Indicates that the starting condition, resumption condition, or termination condition is generated in simple IIC mode.
- When FIFO is selected, using this event output is prohibited.

(5) Address match event output

- Indicates a match of the comparison data (CDR.CMPD) with one frame of receive data when DCCR.DCME is set to 1 in asynchronous mode, including multi-processor mode.

27.12 Address Mismatch Event Output (SCI0_DCUF)

The address mismatch event output, SCI0_DCUF, indicates a mismatch of the comparison data (CDR.CMPD) with one frame of receive data when DCCR.DCME is set to 1 in asynchronous mode, including multi-processor mode. This event can be used for snooze end request only.

27.13 Noise Cancellation Function

Figure 27.72 shows the configuration of the noise filter used for noise cancellation. The noise filter consists of a 2-stage flip-flop circuit and a match detection circuit. When the input signals of the noise filter and the output signals of the 2-stage flip-flop circuits completely match, the matched level is conveyed as an internal signal. Unless otherwise matched, the previous value is retained. When the same level is retained for 3 cycles or longer on the sampling clock of the noise filter, it is considered a valid receive signal. A change in pulse for 3 cycles or shorter is considered as noise, not as a receive signal.

When SEMR.ABCS = 0 and SEMR.ABCSE = 0, the cycle is 1/16 of a period 1 transfer bit.

When SEMR.ABCS = 1 and SEMR.ABCSE = 0, the cycle is 1/8 of a period 1 transfer bit.

When SEMR.ABCSE = 1, the cycle is 1/6 of a period 1 transfer bit.

In asynchronous mode, the noise cancellation function can be applied to the receive signal input to the RXDn pin. The receive level of the RXDn is taken from the flip-flop circuit of the noise filter on the base clock of asynchronous mode.

In simple IIC mode, the noise cancellation function can be used for the input terminals of SDAn and SCLn. The sampling clock for the noise cancellation function is selected in the SNFR.NFCS bit by dividing the baud rate generator source clock by 1, 2, 4, or 8.

If the base clock is stopped once with the noise filter enabled and then the base clock input is restarted again, the noise filter operation resumes from the state where the clock was stopped. When SCR.TE and SCR.RE are set to 0 during base clock input, all of the noise filter flip-flop values are initialized to 1. Accordingly, if the input data is 1 when reception operation resumes, the function determines that a level match is detected and the result is considered an internal signal. When the input level corresponds to 0, the initial output of the noise filter is retained until the level matches in 3 consecutive sampling cycles.

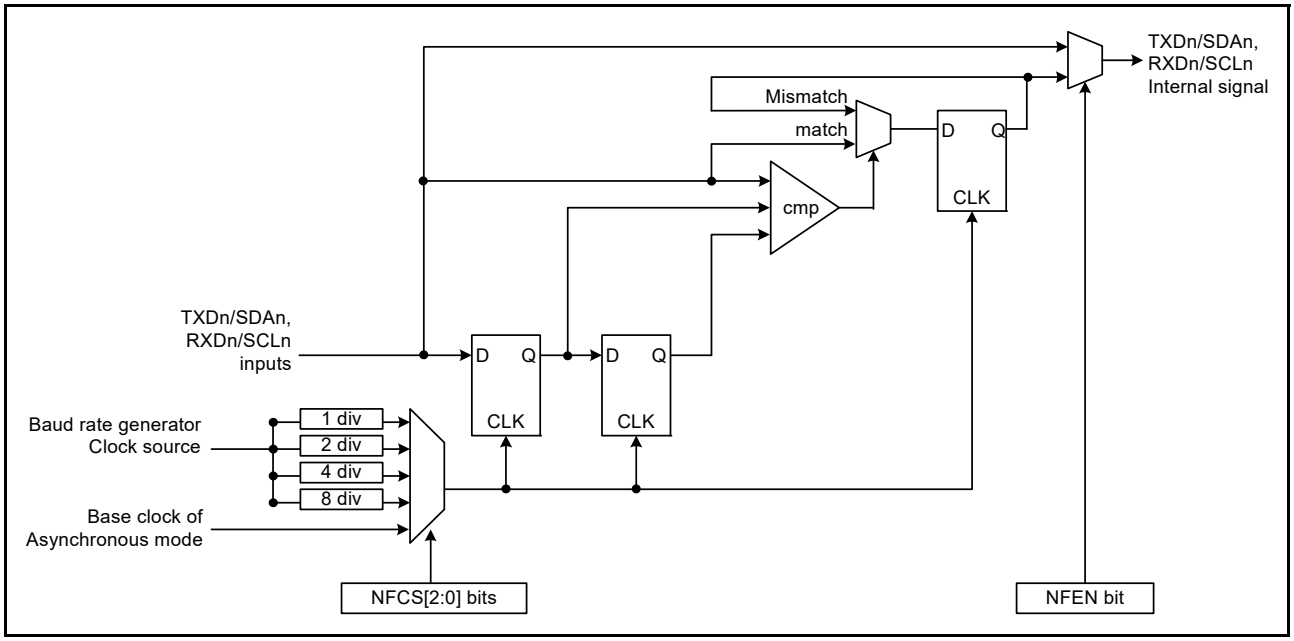


Figure 27.72 Digital noise filter circuit block diagram

27.14 Usage Notes

27.14.1 Settings for the Module-Stop State

The Module Stop Control Register B (MSTPCRB) can enable or disable SCI operation. The SCI is initially stopped after a reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

27.14.2 SCI Operations during Low Power State

(1) Transmission

When setting the module to the stopped state or in transitions to Software Standby mode, stop the operations (by setting the TIE, TE, and TEIE bits in the SCR/SCR_SMCI to 0) after switching the TXDn pin to the general I/O port pin function. When setting I/O port as an SCI function, the SPTR register can control the state of the TXDn pin. Setting the TE bit to 0 initializes the TSR register and the TEND bit in the SSR/SSR_SMCI is initialized to 1 with non-FIFO selected. The value is kept with the FIFO selected. Depending on the port settings and SPTR register settings, output pins might output the level before a transition to the low power state is made after release from the module-stop state or Software Standby mode. When transitions to these states are made during transmission, the transmitted data becomes indeterminate.

To transmit data in the same transmission mode after cancellation of the low power state:

1. Set the TE bit to 1.
2. Read SSR/SSR_FIFO/SSR_SMCI.
3. Write data to TDR sequentially to start data transmission.

To transmit data with a different transmission mode, initialize the SCI first.

Figure 27.73 shows an example flow for transition to Software Standby mode during transmission. Figure 27.74 and Figure 27.75 show the port pin states during transition to Software Standby mode.

Before specifying the module-stop state or making a transition to Software Standby mode from the transmission mode using DTC transfer, stop the transmit operations (TE = 0). To start transmission after cancellation using the DTC, set the TE bit to 1. The SCIn_TXI interrupt flag is set to 1 and transmission starts using the DTC.

(2) Reception

(a) When address match function is not used as wake-up condition

Before specifying the module-stop state or making a transition to Software Standby mode, stop the receive operations (RE = 0 in SCR/SCR_SMCI). If transition is made during data reception, the received data is invalid.

Figure 27.76 shows an example flow for transition to Software Standby mode during reception.

(b) When address match function is used as wake-up condition

Before specifying the module-stop state or making a transition to Software Standby mode:

1. Set the operations after cancellation of the low power state.
2. Set CDR.CMPD and DCCR.DCME to 1.
3. Set the receive operations (RE = 1 in SCR/SCR_SMCI).
4. Set the module-stop state or Software Standby mode.

When SCI transfers to the low power mode if the receive data pin (RXD) is at the low level, set SEMR.RXDESEL to 0. When setting it as SEMR.RXDESEL to 1, there is a possibility that a start bit (falling edge of RXDn pin) cannot be detected on release of the low power mode.

Figure 27.77 shows an example flow for transition to Software Standby mode during reception with address match.

(c) When using SCI0 in Snooze mode

When using SCI0 in Snooze mode, some restrictions, including the maximum bit rates, exist. For details, see section 10, Low Power Modes.

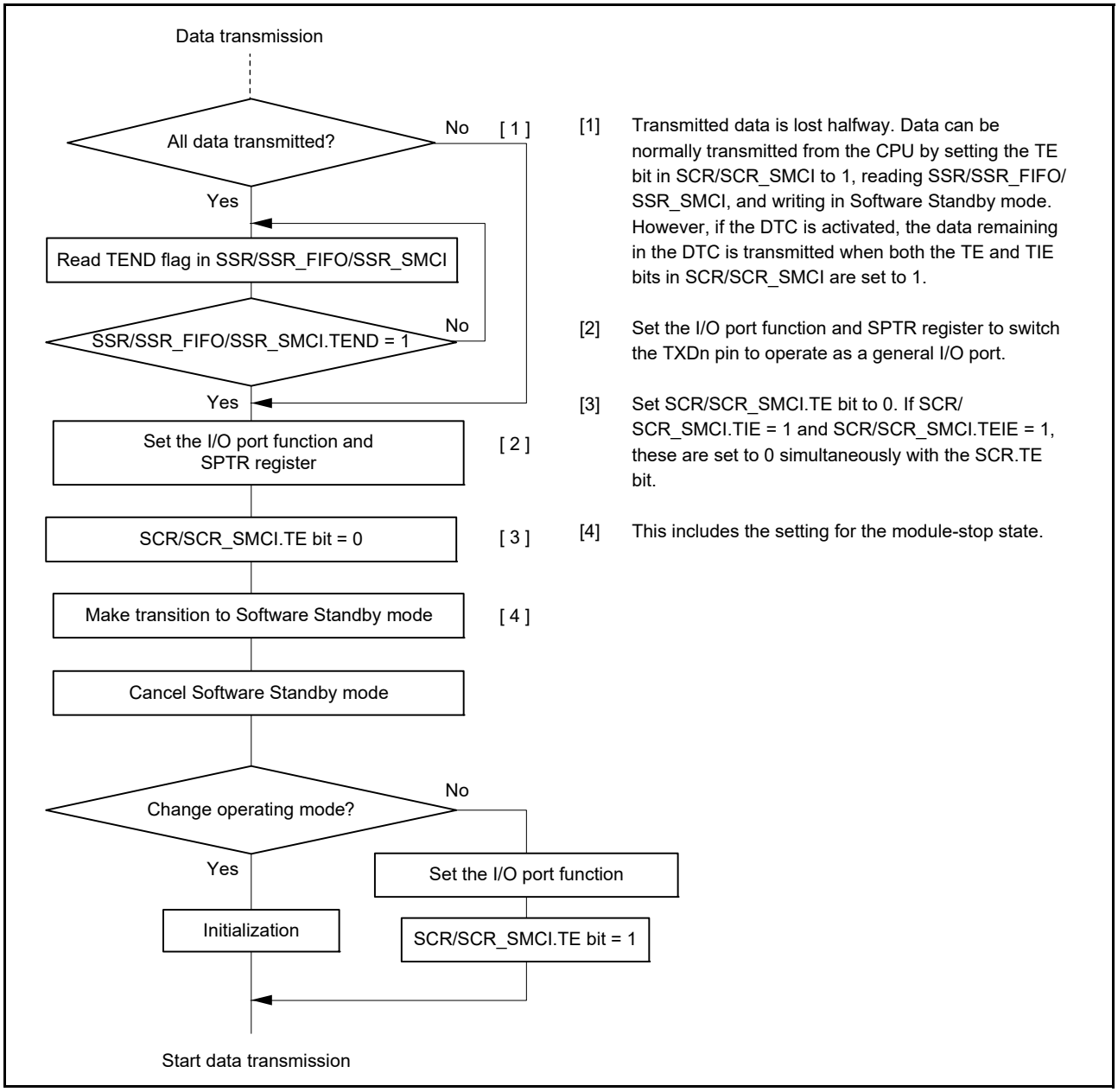


Figure 27.73 Example flow for transition to Software Standby mode during transmission

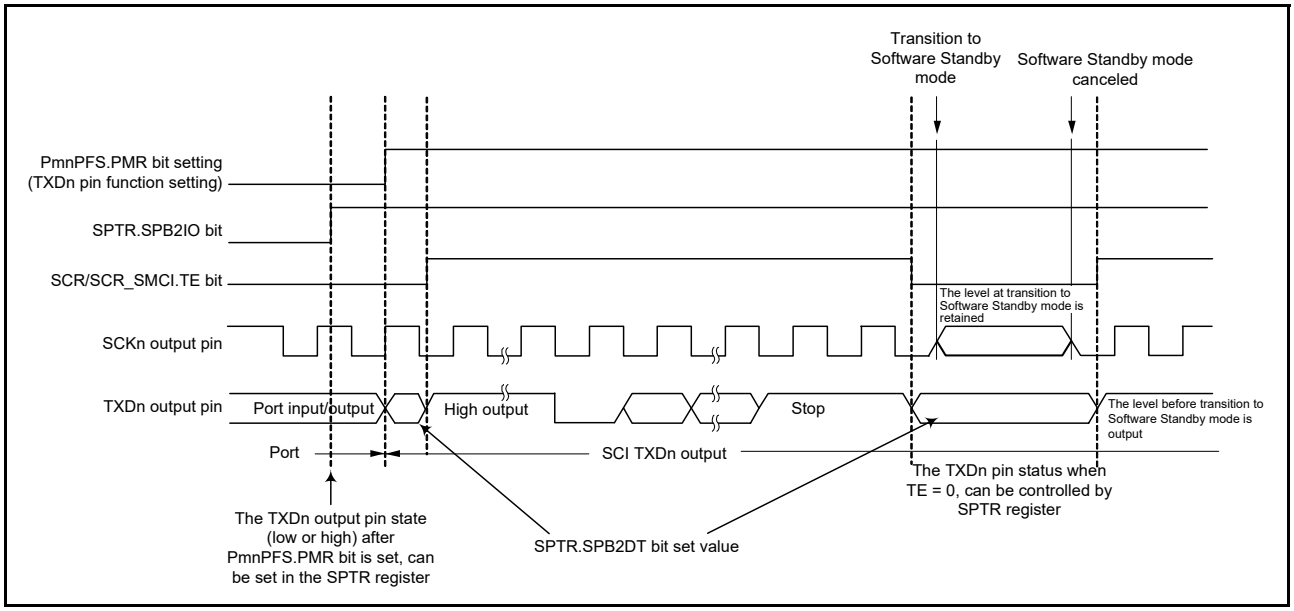


Figure 27.74 Port pin states during transition to Software Standby mode with internal clock and asynchronous transmission

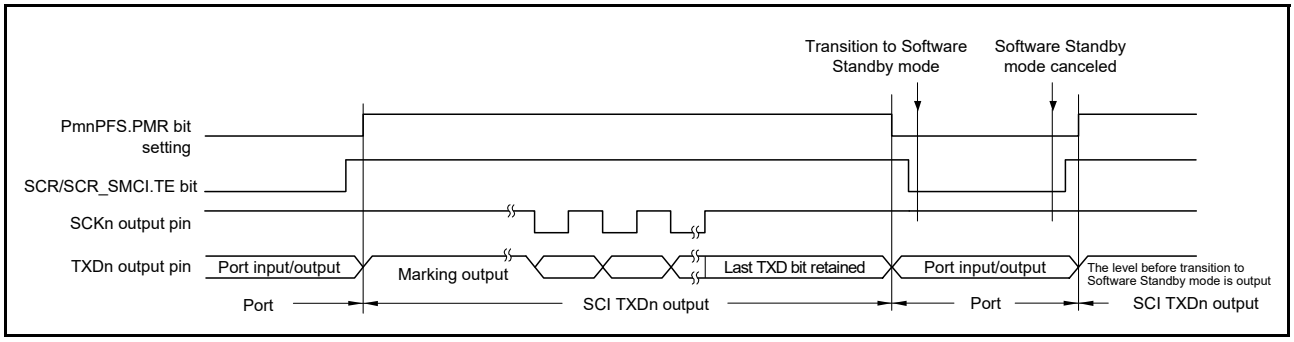


Figure 27.75 Port pin states during transition to Software Standby mode with internal clock and clock synchronous transmission

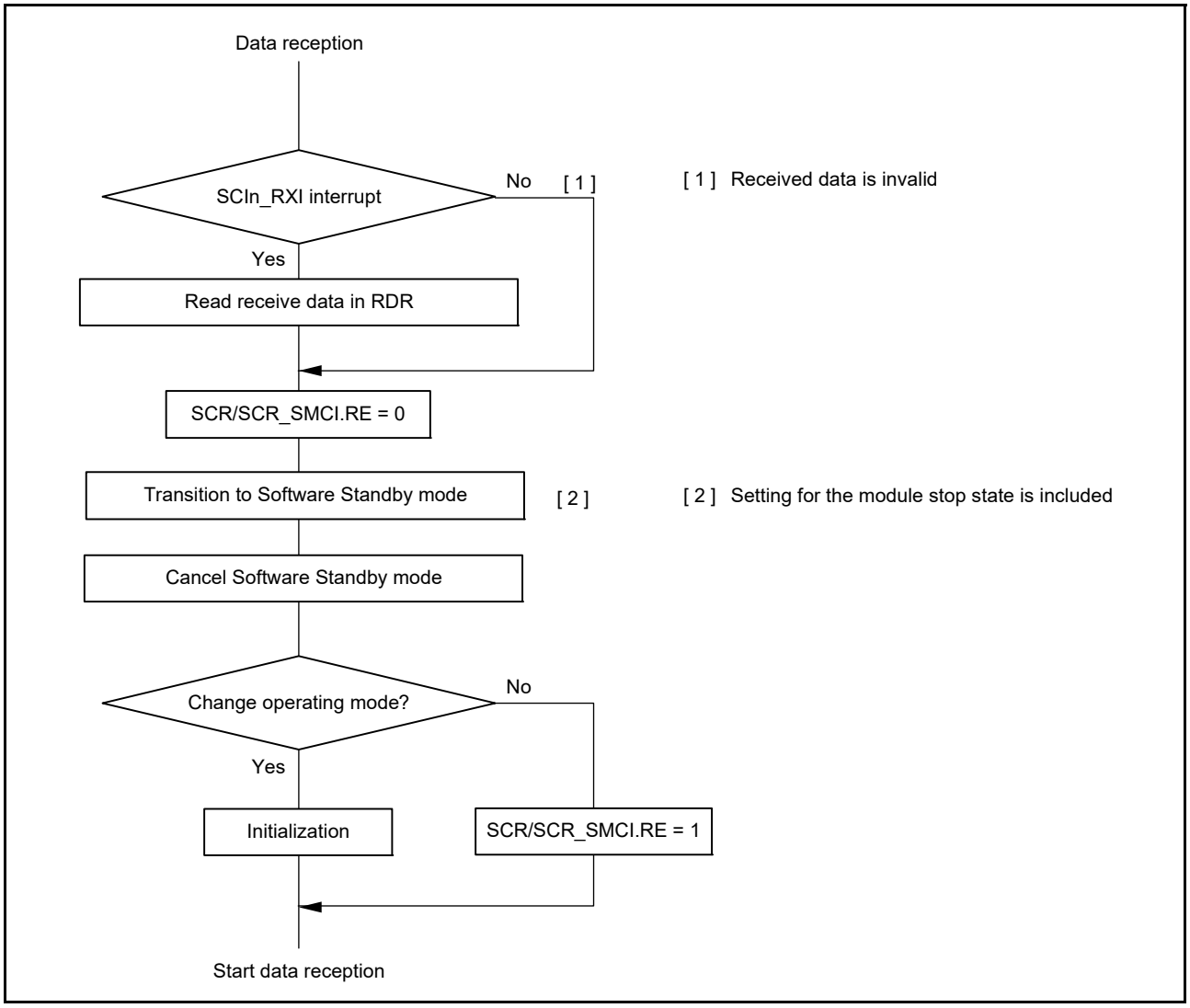


Figure 27.76 Example flow for transition to Software Standby mode during reception

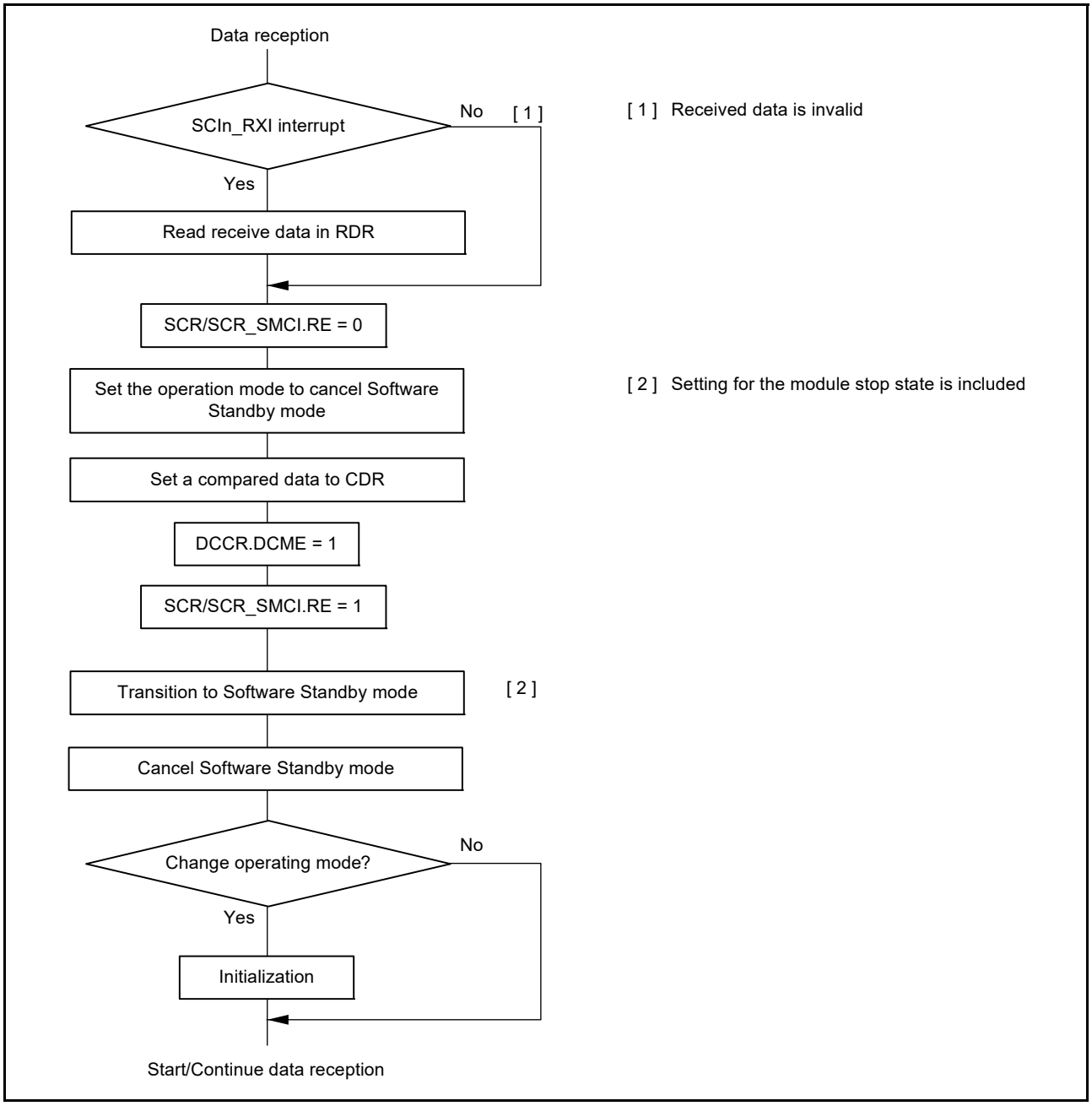


Figure 27.77 Example flow for transition to Software Standby mode during reception with address match

27.14.3 Break Detection and Processing

(1) Non-FIFO selected

When a framing error is detected, a break can be detected by reading the RXDn pin value directly. In a break, the input from the RXDn pin becomes all 0s, and so the FER flag in SSR is set to 1 to indicate a framing error, and the PER flag in SSR might also be set to 1 to indicate a parity error. The SCI continues the receive operation even after a break is received. Therefore, even when the FER flag is set to 0, indicating that no framing error occurred, it is set to 1 again. When the SEMR.RXDESEL bit is 1, the SCI sets the SSR.FER flag to 1 and stops receiving operations until a start bit of the next data frame is detected. If the SSR.FER flag is set to 0 at this time, the SSR.FER flag retains 0 during the break.

When the RXDn pin is set to 1 and the break ends, detecting the beginning of the start bit on the first falling edge of the RXDn pin allows the SCI to start the receiving operation.

(2) FIFO selected

When a framing error is detected and when the SCI detects that continuous receive data is 0 for one frame, reception stops. When a framing error is detected, a break can be detected by reading the SPTR.RXDMON bit value. After the RXD signal is in the mark state and the break ends, reception data to the FRDRHL register resumes.

27.14.4 Mark State and Production of Breaks

When the SCR/SCR_SMCI.TE bit is 0, disabling serial transmission, the state of the TXDn pin can be set using the SPTR.SPB2IO and SPTR.SPB2DT bits. With this approach, a TXDn pin can be placed in the mark state to transmit a break.

Before setting the SCR/SCR_SMCI.TE bit to 1, enabling serial transmission, set the SPB2IO and SPB2DT bits to put a communication line in the mark state (the state of 1), and change the TxDn pin using I/O port function. To output a break on data transmission, after setting the TXDn pin to output 0 by setting the SPB2IO and SPB2DT bits, change the TXDn pin using the I/O port function and set the SCR/SCR_SMCI.TE bit to 0. When the SCR/SCR_SMCI.TE bit is set to 0, the transmitter is initialized regardless of the current state of transmission.

27.14.5 Receive Error Flags and Transmit Operations in Clock Synchronous and Simple SPI Modes

Transmission cannot start when a receive error flag (ORER) in SSR/SSR_FIFO is set to 1, even when data is written to TDR or FTDRL*2. Always set the receive error flags to 0 before starting transmission.

Note 1. The receive error flags cannot be set to 0 even when the RE bit in SCR/SCR_SMCI is set to 0 (serial reception is disabled).
Note 2. Do not use the FTDRH register in simple SPI mode.

27.14.6 Restrictions on Clock Synchronous Transmission in Clock Synchronous and Simple SPI Modes

When the external clock source is used as a synchronization clock, the following restrictions apply.

(1) Start of transmission

Wait at least the following time from writing transmit data to TDR to the start of the external clock input:

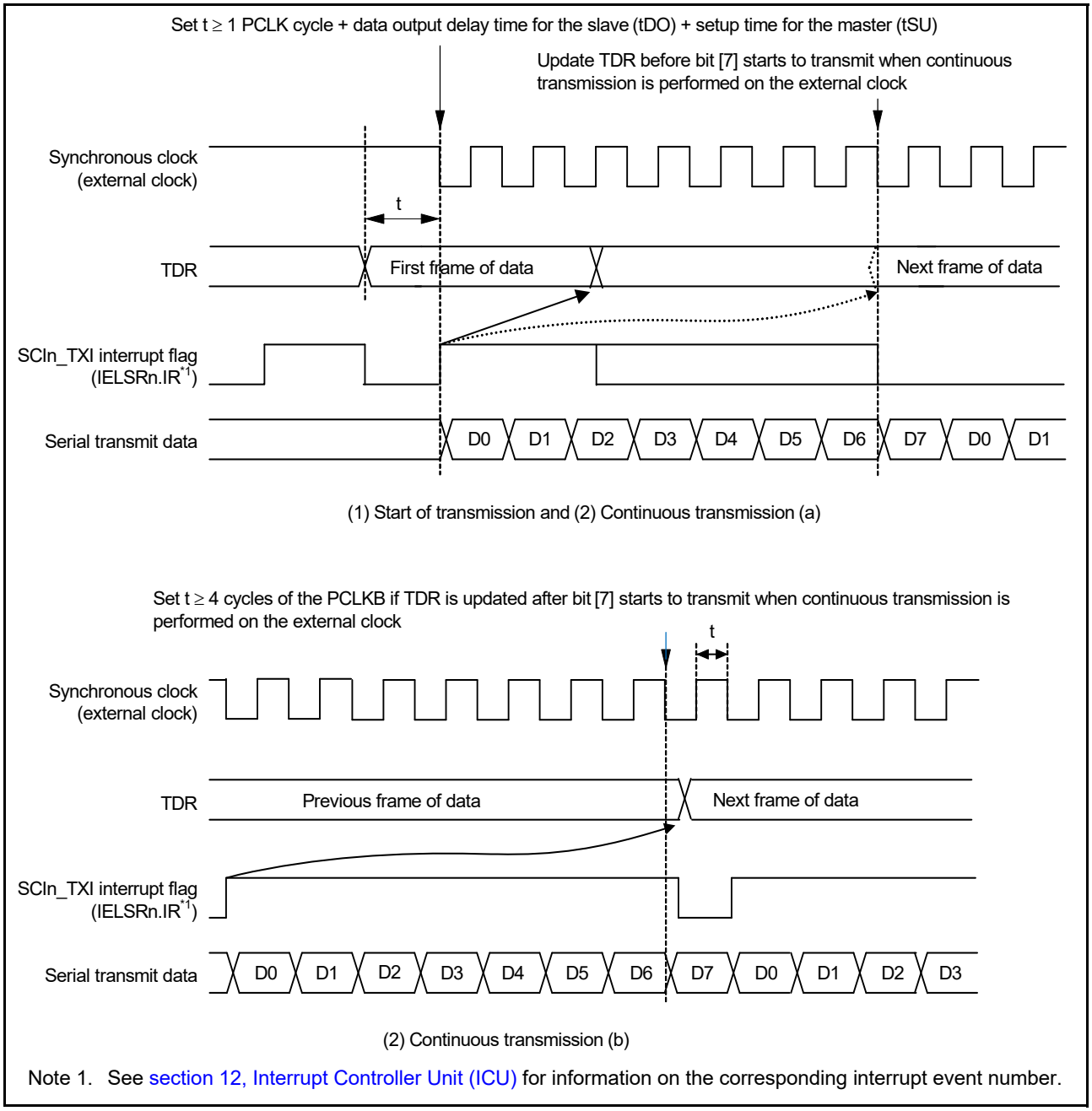
- 1 PCLKB cycle + data output delay time for the slave (tDO) + setup time for the master (tSU).

See Figure 27.78.

(2) Continuous transmission

Write the next transmit data to TDR or TDRHL before the falling edge of the transmit clock, bit [7], see Figure 27.78.

When updating TDR after bit [7] starts to transmit, update TDR while the synchronization clock is in the low-level period, and set the high-level width of the transmit clock, bit [7] to 4 PCLKB cycles or longer, see Figure 27.78.



Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 27.78 Restrictions on the use of external clock in clock synchronous transmission

27.14.7 Restrictions on using DTC

During transmission or reception operations using the DTC, do not set transfer data for the DTC.

(1) Writing data to TDR (FTDRHL)

(a) Non-FIFO selected

Data can be written to TDR and TDRHL. However, if new data is written to TDR or TDRHL when transmit data remains in TDR or TDRHL, the previous data in TDR and TDRHL is lost because it was not transferred to TSR yet. When using DTC, be sure to write transmit data to TDR or TDRHL in the SCIn_TXI interrupt request handling routine.

(b) FIFO selected

It is possible to write data to the FTDRH and FTDRL registers when SCR.TE is 1. Confirm the amount of writable data using the FDR.T[4:0] bits.

(2) Reading data from RDR (FRDRHL)

When using the DTC to read RDR and RDRHL, always set the receive data full interrupt (SCIn_RXI) as the activation source.

27.14.8 Notes on Starting Transfer

At the point where transfer starts when the interrupt status flag, IELSRn.IR, in the ICU is 1, follow the procedure in this section to clear interrupt requests before permitting operations (by setting the SCR/SCR_SMCI.TE or SCR/SCR_SMCI.RE bit to 1). For details on the interrupt status flag, see section 12, Interrupt Controller Unit (ICU).

- Confirm that transfer has stopped (the setting of the SCR/SCR_SMCI.TE or SCR/SCR_SMCI.RE bit is 0).
- Set the associated interrupt enable bit (SCR/SCR_SMCI.TIE or SCR/SCR_SMCI.RIE) to 0.
- Read the associated interrupt enable bit (SCR/SCR_SMCI.TIE or SCR/SCR_SMCI.RIE bit) to check that it is 0.
- Set the interrupt status flag, IELSRn.IR, in the ICU to 0.

27.14.9 External Clock Input in Clock Synchronous and Simple SPI Modes

In clock synchronous mode and simple SPI mode, the external clock (SCKn) must be input as follows:

High-pulse period, low-pulse period = 2 PCLKB cycles or more, period = 6 PCLKB cycles or more.

27.14.10 Limitations on Simple SPI Mode

(1) Master mode

- Use a resistor to pull up or pull down the clock line matching the initial settings for the transfer clock set by the SPMR.CKPH and CKPOL bits when the SPMR.SSE bit is 1.

  This prevents the clock line from being placed in the high-impedance state when the SCR.TE bit is set to 0 or unexpected edges from being generated on the clock line when the SCR.TE bit changes from 0 to 1. When the SPMR.SSE bit is 0 in single master mode, pulling up or pulling down the clock line is not required because the clock line is not placed in the high-impedance state even when the SCR.TE bit is set to 0.
- For the clock delay setting (SPMR.CKPH bit is 1), the receive data full interrupt (SCIn_RXI) is generated before the final clock edge on the SCKn pin as indicated in Figure 27.79. If the TE and RE bits in the SCR become 0 at this time before the final edge of the clock signal on the SCKn pin, the SCKn pin is placed in the high-impedance state, so the width of the last clock pulse of the transfer clock is shortened. Additionally, an SCIn_RXI interrupt might lead to the input signal on the SSn pin of a connected slave going to the high level before the final edge of the clock signal on the SCKn pin, leading to incorrect operation of the slave.
- In a multi-master configuration, take care because the SCKn pin output becomes high-impedance while the input on the SSn pin is at the low level if a mode fault error occurs as the current character is being transferred, stopping supply of the clock signal to the connected slave. Reset the connected slave to avoid misaligned bits when transfer is restarted.

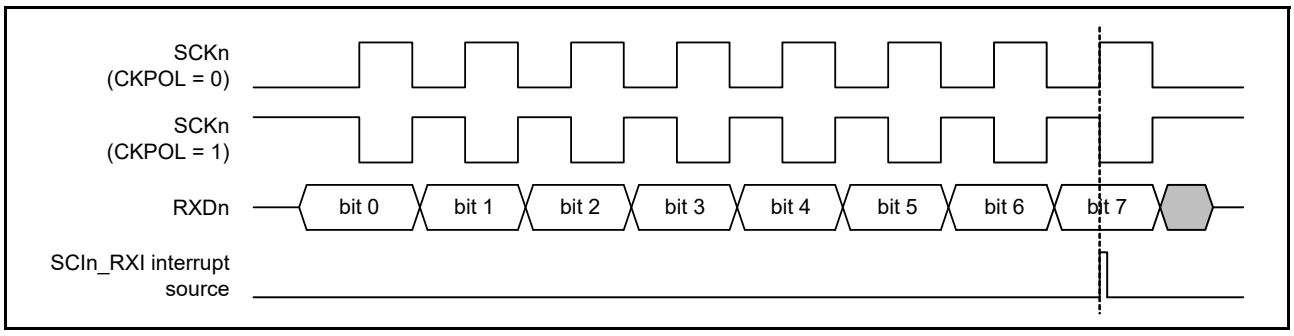


Figure 27.79 Timing of SCIn_RXI interrupt in simple SPI mode with clock delay

(2) Slave mode

- Wait at least the following time from writing transmit data in the TDR register to the start of the external clock input:
  1 PCLKB cycle + data output delay time for the slave (tDO) + setup time for the master (tSU)

  Also wait at least 5 PCLKB cycles from the input of the low level on the SSn pin to the start of the external clock input.
- Provide an external clock signal to the master the same as the data length for transfer
- Control the input on the SSn pin before the start and after the end of data transfer
- When the input level on the SSn pin changes from low to high while the current character is being transferred, set the TE and RE bits in the SCR to 0 and, after restoring the settings, restart transfer of the first byte.

28. Digital Addressable Lighting Interface (DALI)

28.1 Overview

The Digital Addressable Lighting Interface (DALI) module allows communication using the international open lighting control protocol that includes dimming control of electronic ballasts and LED lights from different manufacturers. The DALI interface module is designed to allow compliance with international standard IEC62386-101 Edition 1.0/2.0 (DALI 2), that includes software control.

In this section, PCLK refers to PCLKB.

Table 28.1 lists the DALI specifications and Figure 28.1 shows a block diagram.

Table 28.1 DALI specifications

Parameter	Description
Designed for compliance with	IEC 62386-101 Edition1.0/2.0 (DALI 2)
Communication mode	• Master/slave • Transmission, reception, transmission/reception.
Communication format	DALI data format
Serial data	• MSB-first • Receive data length undefined, minimum 1 bit, maximum 32 bits • Transmit data length, which is selectable from 8, 16, 17, 20, 24, and 32 bits.
Interrupt output	• Stop condition detection interrupt (DALI_SDI) • DALI error interrupt (DALI_DEI) • Collision detection interrupt (DALI_CLI) • Bus power down detection interrupt (DALI_BPI) • Falling-edge detection interrupt (DALI_FEI).
Error detection	• Manchester framing error • Overrun error • Frame size violation error • Bit timing violation error.
Communication function	• Adjusting the edge allowable area for the DRX input signal • DTX width modulation.
Module-stop function	• Module-stop state can be set

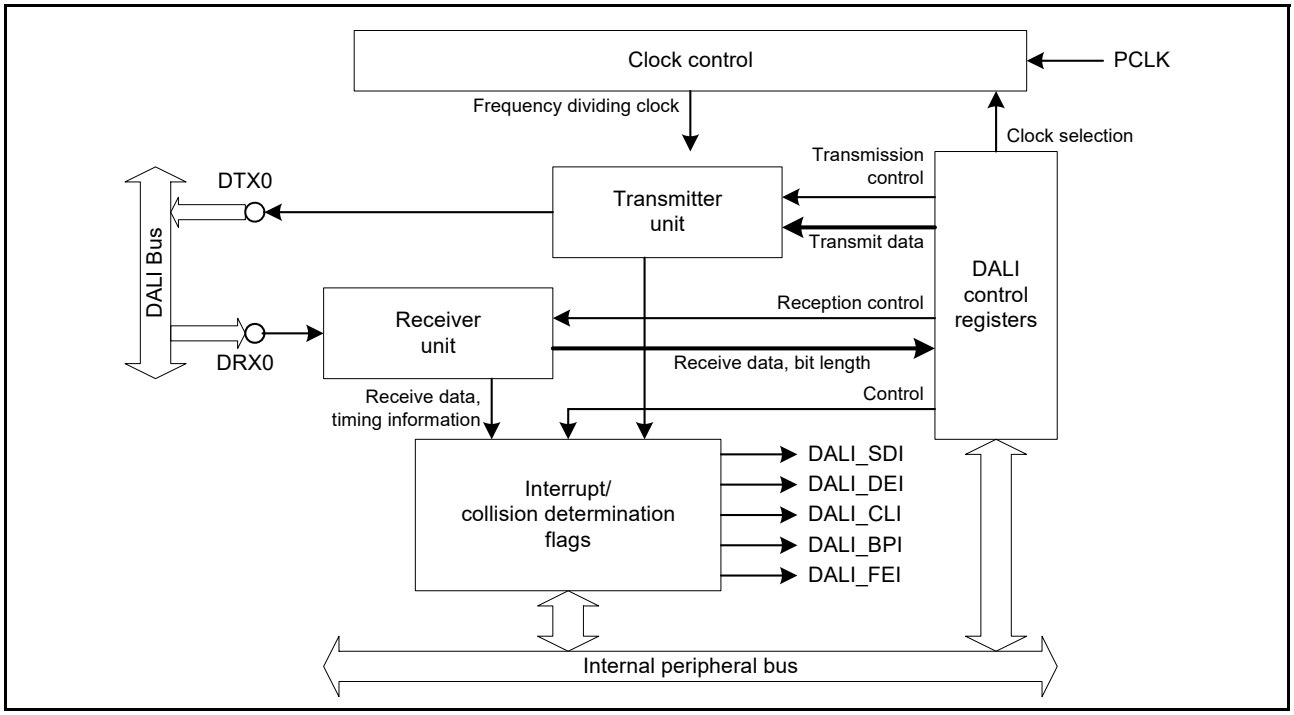


Figure 28.1 DALI block diagram

Table 28.2 lists the DALI I/O pins.

Table 28.2 DALI pin configuration

Pin name	I/O	Function
DRX0	Input	DALI reception pin
DTX0	Output	DALI transmission pin

28.2 Register Descriptions

28.2.1 DALI Configuration Register 1 (CNFR1)

Address(es): DALI0.CNFR1 4008 F012h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	CHL[2:0]			—	—	CKS[1:0]		BR[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b7 to b0	BR[7:0]	Bit Rate	Bit rate setting	R/W*1
b9, b8	CKS[1:0]	Clock Select	00: PCLK clock (x = 0) 01: PCLK/4 clock (x = 1) 10: PCLK/16 clock (x = 2) 11: PCLK/64 clock (x = 3).	R/W*1
b11, b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit name	Description	R/W
b14 to b12	CHL[2:0]	Character Length	000: 8 bits 001: 16 bits 010: 24 bits 011: 32 bits 100: 20 bits 101: 17 bits 11x: Setting prohibited.	R/W*1
b15	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. These bits must only be modified when the DALI0.STR1.BBF bit is 0.

BR[7:0] bits (Bit Rate)

The BR[7:0] bits are readable but they must be written only when the DALI0.CTR1.RE and DALI0.CTR1.TE bits are 00b.

The following formula shows the relation between these bits and bit rate B, where the set value of these bits is N.

$$N = \frac{PCLK \times 10^6}{512 \times 2^{2x-1} \times B} - 1$$

$$Error\ (\%) = \left\{ \frac{PCLK \times 10^6}{B \times 512 \times 2^{2x-1} \times (N+1)} - 1 \right\} \times 100$$

B: Bit rate in bps

N: Set value of baud rate generator: $0 \leq N \leq 255$

x: Value selected by CKS[1:0]

Specify x and N depending on a frequency with 1200 bps as the target. Table 28.3 shows a setting example.

Table 28.3 Example of baud rate setting

bps	Operating frequency of PCLK (MHz)								
	8			16			32		
	x	N	Error (%)	x	N	Error (%)	x	N	Error (%)
1200	0	25	0.16	1	12	0.16	1	25	0.16

CKS[1:0] bits (Clock Select)

The CKS[1:0] bits select the PCLK division ratio from 1/1, 1/4, 1/16, and 1/64 for the DALI operation clock.

CHL[2:0] bits (Character Length)

The CHL[2:0] bits set the transmit data length from 8, 16, 17, 20, 24, and 32 bits.

28.2.2 DALI Configuration Register 2 (CNFR2)

Address(es): DALI0.CNFR2 4008 F014h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	CDM0	CDE	TXWE	SGA	BTVM	BTVE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	BTVE	Bit Timing Violation Enable*1	0: Bit timing violation function is disabled 1: Bit timing violation function is enabled.	R/W*2

Bit	Symbol	Bit name	Description	R/W
b1	BTVM	Bit Timing Violation Mode	0: Edge in gray area between half bit and 2-half bit is not detected as bit timing violation 1: Edge in gray area between half bit and 2-half bit is detected as bit timing violation.	R/W*2
b2	SGA	Save an Edge of Gray Area Mode	0: The edge allowable area of the DRX0 input signal is the default 1: The edge allowable area of the DRX0 input signal is extended.	R/W*2
b3	TXWE	DTX Width Modulation Enable	0: The width of DTX0 waveform is not modulated 1: The width of DTX0 waveform is modulated.	R/W*2
b4	CDE	Collision Detect Enable*1	0: Collision detection is disabled 1: Collision detection is enabled.	R/W*2
b5	CDM0	Collision Detect Mode	0: Destroy area 1: Destroy area and avoidance area (edge).	R/W*2
b15 to b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Bit timing violation and collision are violations that are newly defined in DALI edition 2.0. If the specification which is compliant with the DALI edition 1.0 does not require detecting these violations, set bits BTVE and CDE to 0.

Note 2. The bit must be modified only when the DALI0.STR1.BBF bit is 0.

BTVE bit (Bit Timing Violation Enable)

The BTVE bit enables or disables the bit timing violation detection function. The bit is valid when the DALI0.CTR1.RE bit is 1.

BTVM bit (Bit Timing Violation Mode)

The BTVM bit sets the violation area when the bit timing violation function is enabled. The violation area set by this bit is the area between point G (half-bit) and point H (2-half bit) shown in Figure 28.11. This bit is valid when the BTVE bit is 1 and must be modified when the BTVE bit is 0.

SGA bit (Save an Edge of Gray Area Mode)

The SGA bit extends the edge allowable area of the DRX0 input signal. See section 28.3.5 for details.

TXWE bit (DTX Width Modulation Enable)

The TXWE bit enables or disables the DTX0 width modulation function. See section 28.3.6 for details.

CDE bit (Collision Detect Enable*1)

The CDE bit enables or disables the collision detection function. Set this bit to 0 for backward frame transmission*1.

Note 1. If the CDE bit is set to 1 during backward frame transmission, immediately after writing the DALI0.TRSTR1 register, a conflict of backward frames might be detected. Set the CDE bit to 1 after backward frame transmission completes.

CDM0 bit (Collision Detect Mode)

The CDM0 bit sets the condition for collision detection. For details on collision, see section 28.3.4.

28.2.3 DALI Control Register 1 (CTR1)

Address(es): DALI0.CTR1 4008 F026h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	FEIE	BPIE	CLIE	DEIE	SDIE	—	—	—	—	—	—	RE	TE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TE	Transmit Enabling	0: Transmit operation is disabled*2 1: Transmit operation is enabled.*1	R/W
b1	RE	Receive Enabling	0: Storing received data is disabled 1: Storing received data is enabled.*1	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	SDIE	DALI_SDI Output Enabling	0: DALI_SDI output is disabled 1: DALI_SDI output is enabled.	R/W
b9	DEIE	DALI_DEI Output Enabling	0: DALI_DEI output is disabled 1: DALI_DEI output is enabled.	R/W
b10	CLIE	DALI_CLI Output Enabling	0: DALI_CLI output is disabled 1: DALI_CLI output is enabled.	R/W
b11	BPIE	DALI_BPI Output Enabling	0: DALI_BPI output is disabled 1: DALI_BPI output is enabled.	R/W
b12	FEIE	DALI_FEI Output Enabling	0: DALI_FEI output is disabled 1: DALI_FEI output is enabled.	R/W
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. When the RE bit is changed from 0 to 1 while other masters are communicating, the DALI module attempts to receive data of that communication. To reduce this risk, check the DALI0.STR1.BBF bit to confirm the DALI bus is idle (DALI0.STR1.BBF bit is 0) before setting RE bit to 1.

Note 2. If the TE bit is changed from 1 to 0 during transmission, the DALI module stops the transmission immediately.

TE bit (Transmit Enabling)

The TE bit enables or disables transmit operation.

RE bit (Receive Enabling)

The RE bit enables or disables receive operation.

SDIE bit (DALI_SDI Output Enabling)

The SDIE bit enables or disables the stop bit detection interrupt (DALI_SDI). This bit is invalid when the TE bit is 0 and the RE bit is 0.

DEIE bit (DALI_DEI Output Enabling)

The DEIE bit enables or disables the DALI error interrupt (DALI_DEI).

CLIE bit (DALI_CLI Output Enabling)

The CLIE bit enables or disables the collision detection interrupt (DALI_CLI). This bit is valid only when the DALI0.CNFR2.CDE bit is 1.

BPIE bit (DALI_BPI Output Enabling)

The BPIE bit enables or disables the bus power down detection interrupt (DALI_BPI).

FEIE bit (DALI_FEI Output Enabling)

The FEIE bit enables or disables the falling edge detection interrupt (DALI_FEI).

28.2.4 DALI DTX Control Register 1 (TXDCTR1)

Address(es): DALI0.TXDCTR1 4008 F028h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TXASE	TXAS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TXAS	DTX Assert Level	0: The DTX0 pin is driven low 1: The DTX0 pin is driven high.	R/W*1
b1	TXASE	DTX Assert Enabling	0: An internal transmit data is output to the DTX0 pin 1: The level specified by TXAS bit is output to the DTX0 pin.	R/W*1
b15 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The bit can only be modified when the DALI0.CTR1.TE bit is 0.

TXAS bit (DTX Assert Level)

The TXAS bit selects the DTX0 pin level as low or high. This bit is valid when the TXASE bit is 1.

TXASE bit (DTX Assert Enabling)

The TXASE bit selects whether to use the specified level by the TXAS pin as the DTX0 pin level. Figure 28.2 shows the detailed operation.

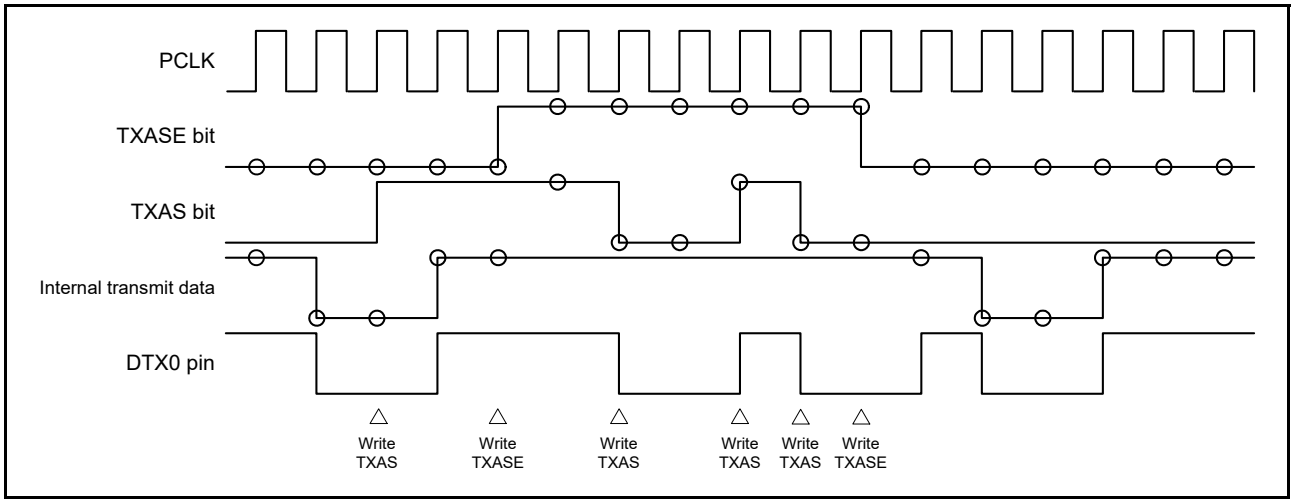


Figure 28.2 DTX0 pin level control

28.2.5 DALI Transmit Control Register 1 (TRSTR1)

Address(es): DALI0.TRSTR1 4008 F022h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TRST	Transmission Start Trigger	Writing 1 to this bit starts transmission	W
b15 to b1	—	Reserved	The write value should be 0	W

TRST bit (Transmission Start Trigger)

Writing 1 to this bit starts transmission. During transmission, the TRST bit cannot be set for new transmission*1. This bit is valid only when the DALI0.CTR1.TE bit is 1. The data length of a transmission is specified by the DALI0.CNFR1.CHL[2:0] bits. After writing 1 to this bit, data is transmitted with the MSB-first.

Note 1. The DALI module does not have a status flag to indicate the transmission status. Therefore, first confirm the DALI0.STR1.BBF bit is 0, and then set the TRST bit to 1. After that, the DALI0.STR1.BBF bit is set to 1, which indicates the frame transmission started. When the transmission completes, DALI_SDI is generated and the DALI0.STR1.BBF bit changes from 1 to 0.

28.2.6 DALI Bit Timing Violation Threshold Register 1 (BTVTHR1)

This register detects bit timing violation (BTV). See section 28.3.3.4 for details.

Address(es): DALI0.BTVTHR1 4008 F000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BTV2[7:0]								—	BTV1[6:0]						
Value after reset:	0	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b6 to b0	BTV1[6:0]	Bit Timing Violation Threshold 1	Specifies the bit timing violation threshold value 1	R/W*1
b7	—	Reserved	This bit is read as 0. The write value should be 0	R/W
b15 to b8	BTV2[7:0]	Bit Timing Violation Threshold 2	Specifies the bit timing violation threshold value 2	R/W*1

Note 1. These bits can be modified when the DALI0.CTR1.RE and DALI0.CTR1.TE bits are 0.

Note 2. The BTV area is specified using the bit timing violation threshold bits BTVy (y = 1 to 6) in the DALI0.BTVTHRx registers (x = 1 to 4). The following describes the definition of the BTV area with each BTVy bit.

Definition of the BTV area from an edge at the bit period boundary (boundary edge):
- Boundary edge < Bit timing violation area ≤ BTV1[6:0]
- BTV1[6:0] < Half bit area ≤ BTV2[7:0]
- BTV2[7:0] < Bit timing violation area ≤ BTV6[8:0]
- BTV6[8:0] < 'STOP condition' or 'Bus power down'

Definition of the BTV area from an edge in the middle of a bit period (middle edge):
- DALI0.CNFR2.BTVM = X: Middle edge < Bit timing violation ≤ BTV1[6:0]
- DALI0.CNFR2.BTVM = 0: BTV1[6:0] < Half bit area/2-half bit area ≤ BTV5[8:0]

- DALI0.CNFR2.BTVM = 1: BTV1[6:0] < Half bit area ≤ BTV3[7:0]
- DALI0.CNFR2.BTVM = 1: BTV3[7:0] < Bit timing violation ≤ BTV4[7:0]
- DALI0.CNFR2.BTVM = 1: BTV4[7:0] < 2-half bit area ≤ BTV5[8:0]
- DALI0.CNFR2.BTVM = X: BTV5[8:0] < Bit timing violation ≤ BTV6[8:0]
- DALI0.CNFR2.BTVM = X: BTV6[8:0] < 'STOP condition' or 'Bus power down'

BTV1[6:0] bits (Bit Timing Violation Threshold 1)

The BTV1[6:0] bits specify the bit timing violation (BTV) threshold value 1.

BTV threshold value 1 = BTV1[6:0] × 6.5[μs]

(1) Example

When a value set in the BTV1[6:0] bits is 33h, *BTV threshold value* 1 = 331.5[*μs*].

Values available to set these bits are from 0 to 825.5 μs (see section 28.3.3.4). The set value must satisfy the DALI specifications edition 2.0, taking into account a clock error. The gray area does not exist with the initial BTV threshold value.

BTV2[7:0] bits (Bit Timing Violation Threshold 2)

The BTV2[7:0] bits specify the bit timing violation (BTV) threshold value 2.

BTV threshold value 2 = (BTV2[7:0] + 1) × 6.5[μs]

(1) Example

When a value set in the BTV2[7:0] bits is 4Dh, BTV threshold value 2 = 507[μs].

Values available to set these bits are from 6.5 to 1664 μs (see section 28.3.3.4). The set value must satisfy the DALI specifications edition 2.0, taking into account a clock error. The gray area does not exist with the initial BTV threshold value.

28.2.7 DALI Bit Timing Violation Threshold Register 2 (BTVTHR2)

This register detects bit timing violation (BTV). See section 28.3.3.4 for details.

Address(es): DALI0.BTVTHR2 4008 F002h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BTV4[7:0]								BTV3[7:0]							
Value after reset:	0	1	1	0	0	1	0	1	0	1	0	0	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b7 to b0	BTV3[7:0]	Bit Timing Violation Threshold 3	Specifies the bit timing violation threshold value 3	R/W*1
b15 to b8	BTV4[7:0]	Bit Timing Violation Threshold 4	Specifies the bit timing violation threshold value 4	R/W*1

Note 1. These bits can only be modified when the DALI0.CTR1.RE and DALI0.CTR1.TE bits are 0.

BTV3[7:0] bits (Bit Timing Violation Threshold 3)

The BTV3[7:0] bits specify the bit timing violation (BTV) threshold value 3.

BTV threshold value 3 = (BTV3[7:0] + 1) × 6.5[μs]

(1) Example

When a value set in the BTV3[7:0] bits is 4Dh, BTV threshold value 3 = 507[μs].

Values available to set these bits are from 6.5 to 1664 μs (see section 28.3.3.4). The set value must satisfy the DALI specifications edition 2.0, taking into account a clock error.

BTV4[7:0] bits (Bit Timing Violation Threshold 4)

The BTV4[7:0] bits specify the bit timing violation (BTV) threshold value 4.

BTV threshold value 4 = BTV4[7:0] × 6.5[μs]

(1) Example

When a value set in the BTV4[7:0] bits is 66h, BTV threshold value 4 = 663[μs].

Values available to set these bits are from 0 to 1657.5 μs (see section 28.3.3.4). The set value set must satisfy the DALI specifications edition 2.0, taking into account a clock error.

28.2.8 DALI Bit Timing Violation Threshold Register 3 (BTVTHR3)

This register detects bit timing violation (BTV). See section 28.3.3.4 for details.

Address(es): DALI0.BTVTHR3 4008 F004h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	BTV5[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	1	0	0	1	1	1	0	1

Bit	Symbol	Bit name	Description	R/W
b7 to b0	BTV5[7:0]	Bit Timing Violation Threshold 5	Specifies the bit timing violation threshold value 5	R/W*1
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. These bits can only be modified when the DALI0.CTR1.RE and DALI0.CTR1.TE bits are 0.

BTV5[7:0] bits (Bit Timing Violation Threshold 5)

The BTV5[7:0] bits specify the bit timing violation (BTV) threshold value 5.

BTV threshold value 5 = (BTV5[7:0] + 1) × 6.5[μs]

(1) Example

When a value set in the BTV5[7:0] bits is 9Ah, BTV threshold value 5 = 1007.5[μs].

Values available to set these bits are from 6.5 to 1664 μs (see section 28.3.3.4). The set value must satisfy the DALI specifications edition 2.0, taking into account a clock error. The gray area does not exist with the initial BTV threshold value.

28.2.9 DALI Bit Timing Violation Threshold Register 4 (BTVTHR4)

This register detects bit timing violation (BTV) and defines the stop condition. Make sure to set this register for DALI communication regardless of whether BTV detection operation is enabled or disabled. See section 28.3.2 and section 28.3.3.4 for details.

Address(es): DALI0.BTVTHR4 4008 F006h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	BTV6[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	1	1	0	1	1	0	1	1

Bit	Symbol	Bit name	Description	R/W
b8 to b0	BTV6[8:0]	Bit Timing Violation Threshold 6	Specifies the bit timing violation threshold value 6	R/W*1
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. These bits can only be modified when the DALI0.CTR1.RE and DALI0.CTR1.TE bits are 0.

BTV6[8:0] bits (Bit Timing Violation Threshold 6)

The BTV6[8:0] bits specify the bit timing violation (BTV) threshold value 6.

BTV threshold value 6 = BTV6[8:0] × 6.5[μs]

BTV threshold value 6 is also used for the stop condition definition*3.

(1) Example

When a value set in the BTV6[8:0] bits is 0D8h, BTV threshold value 6 = 1404[μs].

Values available to set these bits are from 1248 to 3321.5 μs (values from 0 to less than 1248 μs. Values less than 1.5-bit width are not allowed. See section 28.3.3.4. The set value must satisfy the DALI specifications edition 2.0, taking into account a clock error. The gray area does not exist with the initial BTV threshold value.

28.2.10 DALI Collision Threshold Register 1 (COLTHR1)

This register detects collision (COL). See section 28.3.4 for details.

Address(es): DALI0.COLTHR1 4008 F008h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	COL2[5:0]						—	—	COL1[5:0]					
Value after reset:	0	0	1	1	1	0	0	0	0	0	0	0	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b5 to b0	COL1[5:0]	Collision Threshold 1	Specifies the collision threshold value 1	R/W*1
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13 to b8	COL2[5:0]	Collision Threshold 2	Specifies the collision threshold value 2	R/W*1
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. These bits can only be modified when the DALI0.CTR1.RE and DALI0.CTR1.TE bits are 0.

Note 2. The COL area is specified using the collision threshold bits (COLy, y = 1 to 9) in the DALI0.COLTHRx registers (x = 1 to 5). The following describes the definition of the COL area with each COLy bit.

Definition of the COL area from an edge at the bit period boundary (boundary edge):
- Boundary edge < Gray area ≤ COL1[5:0]
- COL1[5:0] < Destroy area ≤ COL2[5:0]
- COL2[5:0] < Gray area ≤ COL3[6:0]
- COL3[6:0] < Valid half bit ≤ COL4[6:0]
- COL4[6:0] < Gray area ≤ COL5[6:0]
- COL5[6:0] < Destroy area

Definition of the COL area from an edge in the middle of a bit period (middle edge):
- Middle edge < Gray area ≤ COL1[5:0]
- COL1[5:0] < Destroy area ≤ COL2[5:0]
- COL2[5:0] < Gray area ≤ COL3[6:0]
- COL3[6:0] < Valid half bit ≤ COL4[6:0]
- COL4[6:0] < Gray area ≤ COL5[6:0]
- COL5[6:0] < Destroy area ≤ COL6[6:0]
- COL6[6:0] < Gray area ≤ COL7[7:0]
- COL7[7:0] < 2 valid half bit ≤ COL8[7:0]
- COL8[7:0] < Gray area ≤ COL9[7:0]
- COL9[7:0] < Gray area

COL1[5:0] bits (Collision Threshold 1)

The COL1[5:0] bits specify the collision (COL) threshold value 1.

COL threshold value 1 = COL1[5:0] × 6.5[μs]

(1) Example

When a value set in the COL1[5:0] bits is 0Fh, COL threshold value 1 = 97.5[μs]

Values available to set these bits are from 0 to 409.5 μs (see section 28.3.4). The set value must satisfy the DALI specifications edition 2.0, taking into account a clock error.

COL2[5:0] bits (Collision Threshold 2)

The COL2[5:0] bits specify the collision (COL) threshold value 2.

COL threshold value 2 = (COL2[5:0] + 1) × 6.5[μs]

(1) Example

When a value set in the COL2[5:0] bits is 37h, COL threshold value 2 = 364[μs].

Values available to set these bits are from 6.5 to 416 μs (see section 28.3.4). The set value must satisfy the DALI specifications edition 2.0, taking into account a clock error.

28.2.11 DALI Collision Threshold Register 2 (COLTHR2)

This register detects collision (COL). See section 28.3.4 for details.

Address(es): DALI0.COLTHR2 4008 F00Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	COL4[6:0]							—	COL3[6:0]						
Value after reset:	0	1	0	0	0	1	0	0	0	0	1	1	1	1	0	0

Bit	Symbol	Bit name	Description	R/W
b6 to b0	COL3[6:0]	Collision Threshold 3	Specifies the collision threshold value 3	R/W*1
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b14 to b8	COL4[6:0]	Collision Threshold 4	Specifies the collision threshold value 4	R/W*1
b15	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. These bits can only be modified when the DALI0.CTR1.RE and DALI0.CTR1.TE bits are 0.

COL3[6:0] bits (Collision Threshold 3)

The COL3[6:0] bits specify the collision (COL) threshold value 3

COL threshold value 3 = COL3[6:0] × 6.5[μs]

(1) Example

When a value set in the COL3[6:0] bits is 3Dh, COL threshold value 3 = 396.5[μs].

Values available to set these bits are from 0 to 825.5 μs (see section 28.3.4). The set value must satisfy the DALI specifications edition 2.0, taking into account a clock error.

COL4[6:0] bits (Collision Threshold 4)

The COL4[6:0] bits specify the collision (COL) threshold value 4.

COL threshold value 4 = (COL4[6:0] + 1) × 6.5[μs]

(1) Example

When a value set in the COL4[6:0] bits is 43h, COL threshold value 4 = 442[μs]

Values available to set these bits are from 6.5 to 832 μs (see section 28.3.4). The set value must satisfy the DALI specifications edition 2.0, taking into account a clock error.

28.2.12 DALI Collision Threshold Register 3 (COLTHR3)

This register detects collision (COL). See section 28.3.4 for details.

Address(es): DALI0.COLTHR3 4008 F00Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	COL6[6:0]							—	COL5[6:0]						
Value after reset:	0	1	1	1	0	0	0	1	0	1	0	0	1	0	0	0

Bit	Symbol	Bit name	Description	R/W
b6 to b0	COL5[6:0]	Collision Threshold 5	Specifies the collision threshold value 5	R/W*1
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b14 to b8	COL6[6:0]	Collision Threshold 6	Specifies the collision threshold value 6	R/W*1
b15	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. These bits can only be modified when the DALI0.CTR1.RE and DALI0.CTR1.TE bits are 0.

COL5[6:0] bits (Collision Threshold 5)

The COL5[6:0] bits specify the collision (COL) threshold value 5.

COL threshold value 5 = COL5[6:0] × 6.5[μs]

(1) Example

When a value set in the COL5[6:0] bits is 49h, COL threshold value 5 = 474.5[μs].

Values available to set these bits are from 0 to 825.5 μs (see section 28.3.4). The set value must satisfy the DALI specifications edition 2.0, taking into account a clock error.

COL6[6:0] bits (Collision Threshold 6)

These bits specify the collision (COL) threshold value 6.

COL threshold value 6 = (COL6[6:0] + 1) × 6.5[μs]

(1) Example

When a value set in the COL6[6:0] bits is 70h, COL threshold value 6 = 734.5[μs].

Values available to set these bits are from 6.5 to 832 μs (see section 28.3.4). The set value must satisfy the DALI specifications edition 2.0, taking into account a clock error.

28.2.13 DALI Collision Threshold Register 4 (COLTHR4)

This register detects collision (COL). See section 28.3.4 for details.

Address(es): DALI0.COLTHR4 4008 F00Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	COL8[7:0]								COL7[7:0]							
Value after reset:	1	0	0	0	1	0	0	0	0	1	1	1	1	0	0	1

Bit	Symbol	Bit name	Description	R/W
b7 to b0	COL7[7:0]	Collision Threshold 7	Specifies the collision threshold value 7	R/W*1
b15 to b8	COL8[7:0]	Collision Threshold 8	Specifies the collision threshold value 8	R/W*1

Note 1. These bits must be modified when the DALI0.CTR1.RE and DALI0.CTR1.TE bits are 0.

COL7[7:0] bits (Collision Threshold 7)

The COL7[7:0] bits specify the collision (COL) threshold value 7.

COL threshold value 7 = COL7[7:0] × 6.5[μs]

(1) Example

When a value set in the COL7[7:0] bits is 7Dh, COL threshold value 7 = 812.5[μs].

Values available to set these bits are from 0 to 1657.5 µs (see section 28.3.4). The set value must satisfy the DALI specifications edition 2.0, taking into account a clock error.

COL8[7:0] bits (Collision Threshold 8)

The COL8[7:0] bits specify the collision (COL) threshold value 8.

COL threshold value 8 = (COL8[7:0] + 1) × 6.5[µs]

(1) Example

When a value set in the COL8[7:0] bits is 86h, COL threshold value 8 = 877.5[µs].

Values available to set these bits are from 6.5 to 1664 µs (see section 28.3.4). The set value must satisfy the DALI specifications edition 2.0, taking into account a clock error.

28.2.14 DALI Collision Threshold Register 5 (COLTHR5)

This register detects collision (COL). See section 28.3.4 for details on collision.

Address(es): DALI0.COLTHR5 4008 F010h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	COL9[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	COL9[7:0]	Collision Threshold 9	Specifies the collision threshold value 9	R/W*1
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. These bits can only be modified when the DALI0.CTR1.RE and DALI0.CTR1.TE bits are 0.

COL9[7:0] bits (Collision Threshold 9)

The COL9[7:0] bits specify the collision (COL) threshold value 9.

COL threshold value 9 = COL9[7:0] × 6.5[µs]

(1) Example

When a value set in the COL9[7:0] bits is 91h, COL threshold value 9 = 942.5[µs].

Values available to set these bits are from 0 to 1657.5 µs (see section section 28.3.4). The set value must satisfy the DALI specifications edition 2.0, taking into account a clock error.

28.2.15 DALI Transmit Data Register 1 (TDR1H, TDR1L)

Address(es): DALI0.TDR1H 4008 F01Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DTDR[31:16]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address(es): DALI0.TDR1L 4008 F020h

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
DTDR[15:0]															

Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0 (TDR1H register)	DTDR[31:16]	Transmit Data [31:16]	Upper 16-bit DALI transmit data	R/W
b15 to b0 (TDR1L register)	DTDR[15:0]	Transmit Data [15:0]	Lower 16-bit DALI transmit data	R/W

The maximum data length the DALI transmits is 32 bits (DTDR[31:0]). The TDR1H register stores the upper 16 bits (DTDR[31:16]) and the TDR1L register stores the lower 16 bits (DTDR[15:0]) of transmit data.

When a transmission is triggered, that is, writing 1 to the DALI0.TRSTR1.TRST bit, data for the length specified by the DALI0.CNFR1.CHL[2:0] bits is transmitted with the MSB-first. A value written to an unspecified bit is ignored.

Do not rewrite these register values until the transmission is stopped by a DALI_SDI output (transmission end) or a DALI_CLI output after the transmission trigger input.

(1) Example

When the DALI0.CNFR1.CHL[2:0] bits are 000b DTDR[7:0] are transmitted.

(2) Example

When the DALI0.CNFR1.CHL[2:0] bits are 010b DTDR[23:16] are transmitted, then DTDR[15:0] are transmitted.

28.2.16 DALI Reception Data Register 1 (RDR1H, RDR1L)

Address(es): DALI0.RDR1H 4008 F02Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DRDR[31:16]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address(es): DALI0.RDR1L 4008 F030h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DRDR[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0 (RDR1H register)	DRDR[31:16]	Receive Data [31:16]	Upper 16-bit of DALI receive data	R
b15 to b0 (RDR1L register)	DRDR[15:0]	Receive Data [15:0]	Lower 16-bit of DALI receive data	R

When the stop condition is detected and the DALI0.CTR1.RE is 1, the received data frame is stored in these registers as right-align. The registers store a sampling value at 3/4-bit timing as a logical value of the received data.

(1) Example

When 24-bit data is received, data is stored in the DALI0.RDR1H.DRDR[23:16] and DALI0.RDR1L.DRDR[15:0] bits.

(2) Example

When 8-bit data is received, data is stored in the DALI0.RDR1L.DRDR[7:0] bits.

When received data is stored from the internal shift register, the previous values are cleared. Bits that are not received in the internal shift register, are read as 0. Determine the valid bits by checking the receive data length in the DALI0.STR1.RDBL[5:0] bits.

28.2.17 DALI Status Register 1 (STR1)

Address(es): DALI0.STR1 4008 F032h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RDBL[5:0]						DAF	CDF	O32F	BPDF	BBF	TENDF	RDRF	BTVF	OVF	MFEF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	MFEF	Manchester Flaming Error Flag	0: No MFE occurred or 1 was written to the DALI0.FECR1.MFEFC bit*1 1: An MFE occurred.	R
b1	OVF	Overrun Error Flag	0: No overrun error occurred or 1 was written to the DALI0.FECR1.OVFC bit*1 1: An overrun error occurred.	R
b2	BTVF	Bit Timing Violation Flag	0: No bit timing violation occurred or 1 was written to the DALI0.FECR1.BTVFC bit*1 1: Bit timing violation occurred.	R
b3	RDRF	Receive Data Register Full Flag	0: The DALI0.RDR1L register was read*2 or 1 was written to the DALI0.FECR1.RDRFC*1 1: Receive data is stored in the DALI0.RDR1L or DALI0.RDR1H register.	R
b4	TENDF	Transmit End Flag	0: A value 1 was written to the DALI0.FECR1.TENDFC bit 1: Frame transmission completed.	R
b5	BBF	Bus BUSY Flag	0: DALI bus: IDLE 1: DALI bus: BUSY.	R
b6	BPDF	Bus Power Down Flag	0: This bit is set to 0 with any of the following conditions: - DALI bus power down was not detected - Writing 1 to the DALI0.FECR1.BPDFC bit*1 - Rising of DRX0 signal. 1: DRX0 was 0 for the period of BTV6[8:0], meaning bus power down detected.	R
b7	O32F	Over 32-Bit Data Reception Flag	0: Receive data is 32 bits or less, or 1 was written to the DALI0.FECR1.O32FC bit*1 1: Receive data is 33 bits or more. This bit is set to 1 when data bit [33] is confirmed.	R
b8	CDF	Collision Detect Flag	0: No collision occurred or 1 was written to the DALI0.FECR1.CDFC bit*1 1: A collision occurred.	R
b9	DAF	Destroy Area Flag	0: The collision did not occur in the destroy area or 1 was written to the DALI0.FECR1.DAFC bit 1: The collision occurred in the destroy area.	R
b15 to b10	RDBL[5:0]	Receive Data Bit Length	These bits store the bit length for data to be received successfully*1	R

Note 1. If conditions for setting and clearing the flag are conflicted, setting the flag has priority.

Note 2. When the DALI0.RDR1L register is read, the DALI determines that read operation for the received data completed. When the received data length is 17 to 32 bits, the upper 16 bits (DALI0.RDR1H register) must be read first. If lower bits (DALI0.RDR1L register) are read first, the RDRF bit becomes 0 even though the DALI0.RDR1H register was not read.

MFEF bit (Manchester Flaming Error Flag)

The MFEF bit indicates that a Manchester flaming error (MFE) was detected.

OVF bit (Overrun Error Flag)

The OVF bit indicates that an overrun error was detected.

BTVF bit (Bit Timing Violation Flag)

The BTVF bit indicates that bit timing violation was detected in received data.

RDRF bit (Receive Data Register Full Flag)

The RDRF bit indicates that the DALI0.RDR1L or DALI0.RDR1H register contains unread received data.

TENDF bit (Transmit End Flag)

The TENDF bit indicates that the DALI has transmitted a frame.

BBF bit (Bus BUSY Flag)

The BBF bit indicates the usage status of the DALI bus. When a collision occurs, the bit value is invalid.

This bit is invalid when the DALI0.CTR1.TE and DALI0.CTR1.RE bits are 0.

[Clear condition] (BBF bit = 0)

- Detecting the stop condition (DALI bus IDLE)
- Writing 1 to the DALI0.FECR1.BBFC bit. If conditions for setting and clearing the flag conflicted, setting the flag has priority.
- When the falling edge on the DALI bus is incorrectly detected as the start bit.

[Set condition] (BBF bit = 1)

- When the falling edge is detected on the DRX0 signal after the synchronization
- When the DALI0.CTR1.TE or DALI0.CTR1.RE bits are set to 1 from 0, the DRX0 signal level after the synchronization is low.

BPDF bit (Bus Power Down Flag)

The BPDF bit indicates that DALI bus power down was detected.

O32F bit (Over 32-Bit Data Reception Flag)

This bit indicates that receive data is more than 32 bits.

Note 1. The DALInO32F flag is set when data bit [33] is recognized. If data bit [33] is the MFE occurrence bit, but a high level is detected for the period of BTV threshold value 6, a stop condition is detected and the O32F flag is not set. If data bit [33] is an MFE occurrence bit, but a low level is detected for the period of BTV threshold value 6, the O32F flag is set on the falling edge detection. See Figure 28.3 for details.
In addition, when the DRX0 is driven low for the period of the BTV threshold value 6 and the DALI_BPI is generated, the DALI continues the receive operation, that is, the DALI continues to receive logical value 0. Therefore, if the DALI bus does not return after DALI_BPI output, the O32F flag is set.

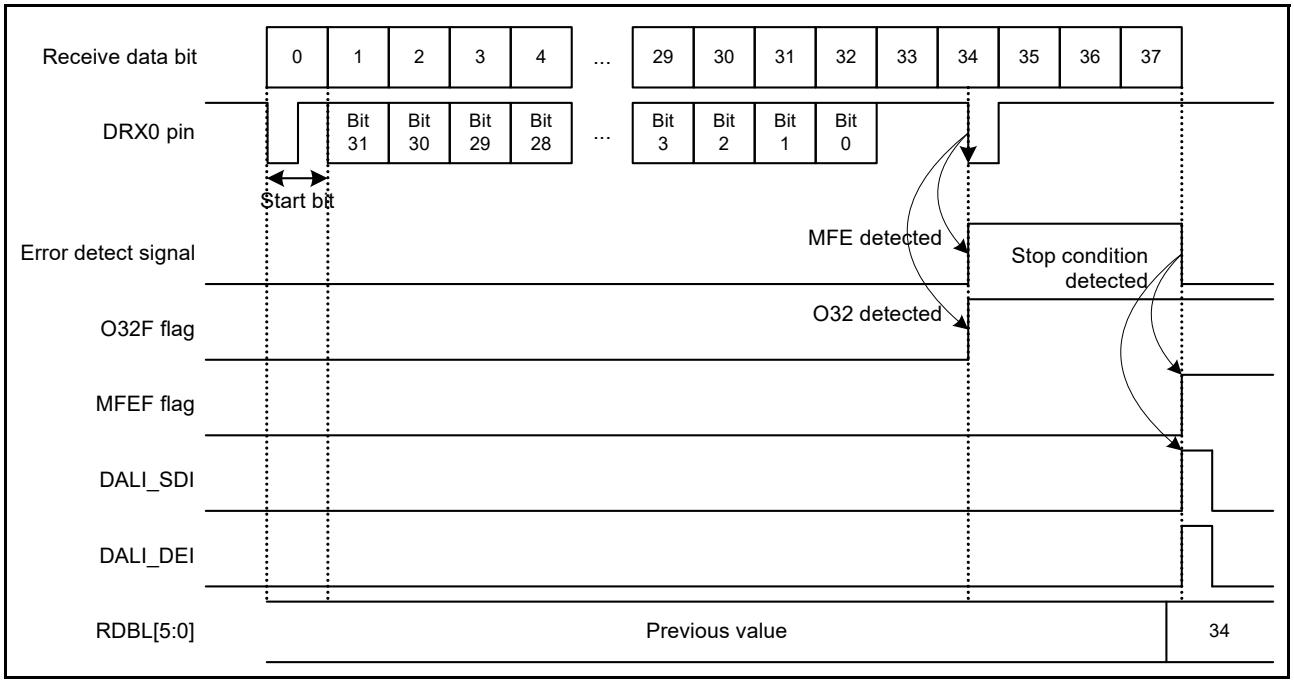


Figure 28.3 O32F set timing

CDF bit (Collision Detect Flag)

The CDF bit indicates whether a collision occurred.

DAF bit (Destroy Area Flag)

When a collision is detected, the DAF bit indicates whether the collision occurred in the destroy area.

RDBL[5:0] bits (Receive Data Bit Length)

The RDBL[5:0] bits store the bit length for data to be successfully received. If conditions for setting and clearing the flag conflict, setting the flag has higher priority.

(1) Example

When these bits are 001000b, 8-bit data is received. When the O32F bit is 0, the RDBL[5:0] bits indicate the receive data length without the start and stop bits.

If a receive operation is stopped because an error or a collision occurred, the RDBL[5:0] bits indicate the number of bits successfully received.

These bits are updated when a stop condition is detected. When reception completes, check these bits to determine frame size violation.

The DALI continues to receive data until a stop condition is detected. When the received data is more than 32 bits, the number of bits is counted until the internal counter reaches the maximum value. When this occurs, the counter overflows and restarts counting from 0. Therefore, when the O32F flag is 1, the value shown in these bits is invalid.

28.2.18 DALI Collision Register 1 (COLR1)

Address(es): DALI0.COLR1 4008 F036h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	TXDCV	RXDCEG	RXDMON	CLDAF	—	—	—	—	—	CDTF1	CDTF2[3:0]			
Value after reset:	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	CDTF2[3:0]	Collision Detect Timing Flag 2	0000: After reset is released 0001: Collision detection timing 1 0010: Collision detection timing 2 0011: Collision detection timing 3 0100: Collision detection timing 4 0101: Collision detection timing 5 0110: Collision detection timing 6 0111: Collision detection timing 7 *1 1000: Collision detection timing 8 *1 1001: Collision detection timing 9 *1 1010: Collision detection timing 10 *1 1011 or greater: Invalid.	R
b4	CDTF1	Collision Detect Timing Flag 1	0: Collision detection started on the edge of a bit period boundary (Figure 28.14) *2 1: Collision detection started on the edge in the middle of a bit period. (Figure 28.15) *2	R
b9 to b5	—	Reserved	These bits are read as 0.	R
b10	CLDAF	Collision Last Destroy Area Flag	0: Collision detection is caused by a DRX0 edge occurrence 1: Collision detection is not caused by a DRX0 edge occurrence (last destroy area).	R
b11	RXDMON	DRX Monitor	This bit monitors the DRX0 pin value after the DRX0 pin is synchronized.	R
b12	RXDCEG	DRX Collision Edge	0: Falling edge 1: Rising edge.	R
b13	TXDCV	DTX Collision Value	0: Low 1: High.	R
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R

Note 1. When the CDTF1 flag is 0, this condition does not occur.

Note 2. An edge in a bit period boundary is indicated with "*a" and an edge in the middle of a bit period is indicated with "*b" in Figure 28.4.

CDTF2[3:0] bits (Collision Detect Timing Flag 2)

When the CLDAF bit is 0, the CDTF2[3:0] bits store the collision detection timing.

When the CLDAF bit is 1, the bit holds the previous value.*1

These bits store the timing (1 to 10) as shown in Figure 28.14 and the timing when a collision is detected as shown in Figure 28.15.

Note 1. These bits are not cleared by clearing the DALI0.STR1.CDF bit but by a reset or software reset.

CDTF1 bit (Collision Detect Timing Flag 1)

The CDTF1 bit stores the collision detection timing.

CLDAF bit (Collision Last Destroy Area Flag)

The CLDAF bit stores the factor that causes the collision to be detected.

RXDMON bit (DRX Monitor)

The RXDMON bit monitors the DRX0 pin value after the DRX0 pin is synchronized.

This bit does not depend on the DALI0.CTR1.TE and DALI0.CTR1.RE bits. It shows the DRX0 pin value after synchronization. This bit holds the previous value during PCLK stop.

RXDCEG bit (DRX Collision Edge)

When the CLDAF bit is 0, the RXDCEG bit stores the edge (rising or falling) of the DRX0 pin that causes the collision to be detected. When the CLDAF bit is 1, this bit holds the previous value.*1

Note 1. These bits are not cleared by clearing the DALI0.STR1.CDF bit.

TXDCV bit (DTX Collision Value)

When the CLDAF bit is 0, the TXDCV bit stores the DTX0 pin value when collision of the DRX0 edge is detected. When the CLDAF bit is 1, this bit holds the previous value.*1

Note 1. These bits are not cleared by clearing the DALI0.STR1.CDF bit. They are cleared by a reset or software reset.

28.2.19 DALI Flag Error Clear Register 1 (FECR1)

Address(es): DALI0.FECR1 4008 F03Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	DAFC	CDFC	O32FC	BPDFC	BBFC	TENDFC	RDRFC	BTVFC	OVFC	MFEFC
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	MFEFC	Manchester Flaming Error Flag Clear	0: DALI0.STR1.MFEF bit is not cleared 1: DALI0.STR1.MFEF bit is cleared.	W*1
b1	OVFC	Overrun Error Flag Clear	0: DALI0.STR1.OVF bit is not cleared 1: DALI0.STR1.OVF bit is cleared.	W*1
b2	BTVFC	Bit Timing Violation Flag Clear	0: DALI0.STR1.BTVF bit is not cleared 1: DALI0.STR1.BTVF bit is cleared.	W*1
b3	RDRFC	Receive Data Register Full Flag Clear	0: DALI0.STR1.RDRF bit is not cleared 1: DALI0.STR1.RDRF bit is cleared.	W*1
b4	TENDFC	Transmit End Flag Clear	0: DALI0.STR1.TENDF bit is not cleared 1: DALI0.STR1.TENDF bit is cleared.	W*1
b5	BBFC	Bus BUSY Flag Clear	0: DALI0.STR1.BBF bit is not cleared 1: DALI0.STR1.BBF bit is cleared.*2	W*1
b6	BPDFC	Bus Power Down Flag Clear	0: DALI0.STR1.BPDF bit is not cleared 1: DALI0.STR1.BPDF bit is cleared.	W*1
b7	O32FC	Over 32-Bit Data Reception Flag Clear	0: DALI0.STR1.O32F bit is not cleared 1: DALI0.STR1.O32F bit is cleared.	W*1
b8	CDFC	Collision Detect Flag Clear	0: DALI0.STR1.CDF bit is not cleared 1: DALI0.STR1.CDF bit is cleared.	W*1
b9	DAFC	Destroy Area Flag Clear	0: DALI0.STR1.DAF bit is not cleared 1: DALI0.STR1.DAF bit is cleared.	W*1
b15 to b10	—	Reserved	The write value should be 0	W

Note 1. Writing 1 to each bit in this register clears the associated flag.

Note 2. Do not clear DALI0.STR1.BBF bit when DALI0.CTR1.TE or DALI0.CTR1.RE bits are 1.

28.2.20 DALI Software Reset Register 1 (SWRR1)

Address(es): DALI0.SWRR1 4008 F03Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SWR	Software Reset	Writing 1 to this bit causes a software reset	W
b15 to b1	—	Reserved	The write value should be 0	W

SWR bit (Software Reset)

Writing 1 to the SWR bit causes a software reset.

The DALI module is initialized by writing 1 to this bit. However, the control registers are not initialized. A software reset completes in 1 PCLK. The DALI module communicates from the next cycle after writing 1 to this bit.

With a software reset, the following registers and output pins of the DALI module are initialized.

Registers:

- DALI0.RDR1L, DALI0.RDR1H
- DALI0.STR1
- DALI0.COLR1, except bits RXDMON and CLDAF.

Output pins of the DALI module:

- DTX0
- Interrupt signals DALI_SD, DALI_FEI, DALI_BPI, DALI_CLI, and DALI_DEI.

28.2.21 DALI DTX Width Register 1 (TXWR1)

Address(es): DALI0.TXWR1 4008 F016h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	TXLW[6:0]						
Value after reset:	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b6 to b0	TXLW[6:0]	DTX Low Width	DTX0 pin low level width	R/W
b15 to b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TXLW[6:0] bits (DTX Low Width)

The TXLW[6:0] bits are valid when DALI0.CNFR2.TXWE bit is 1.

Values available for setting these bits are from 20h (214.5 µs) to 5Eh (617.5 µs).

The low level width and high level width of the DTX0 output waveform are modulated to the following values. See 28.3.6 for detail.

When the DALI0.CNFR2.TXWE bit is 1:

- Low level width: (*TXLW*[6:0] + 1) × 6.5[μs]
- High level width: 832[μs] - {(*TXLW*[6:0] + 1) × 6.5[μs]}.

When the DALI0.CNFR2.TXWE bit is 0:

- Low level width: 416 μs (Reset value = 3Fh)
- High level width: 416 μs (Reset value = 3Fh).

28.3 DALI Communication Function

28.3.1 Data Format

This section describes the data format used in DALI communication.

In DALI communication, bits are defined using Manchester code. Manchester code expresses logical 1 or 0, not by voltage level (high or low), but by level change (rising or falling edge).

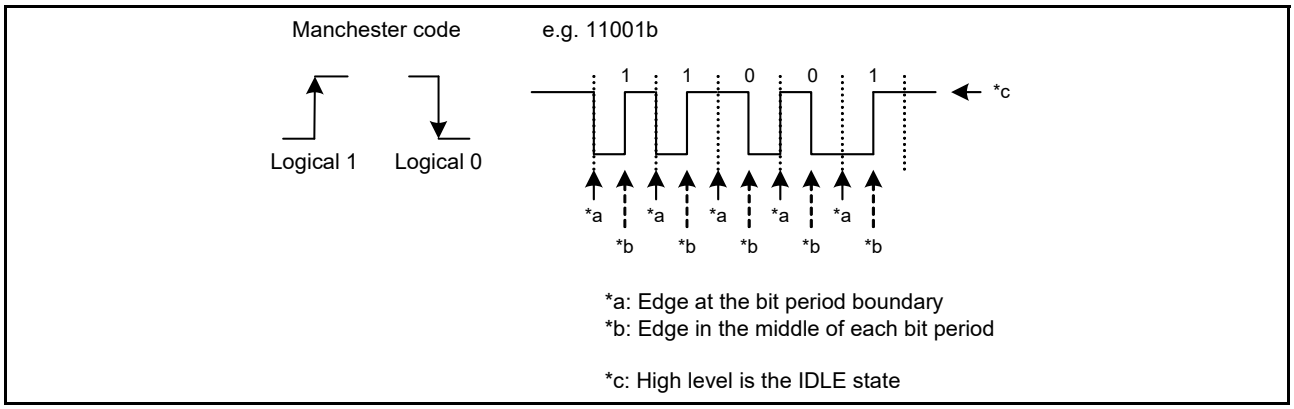


Figure 28.4 Manchester code

Frames in DALI communication are individually defined as forward frame and backward frame. Forward frame is transmitted from master to slave. Backward frame is transmitted from slave to master. A frame consists of a start bit, data bits, and a stop condition. The DRX0 pin is used for reception and the DTX0 pin is used for transmission. Communication is performed in units of data frames.

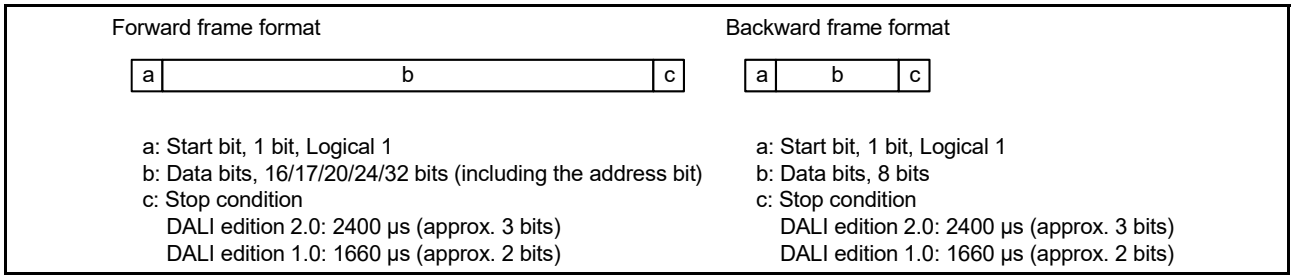


Figure 28.5 DALI data format

28.3.2 STOP Condition Detection and Settling Time

When the DRX0 bus is fixed to high for the period of BTV threshold value 6, the DALI determines that a stop condition was detected and outputs DALI_SDI.*1 Check the DALI0.STR1 register to determine if the stop condition is output from another master or in the frame transmitted from the DALI. When the DALI0.STR1.TENDF bit is 1, the stop condition is transmitted by the DALI.*2 Because the high level period of the DRX0 bus is measured from the last rising edge, the measurement start timing varies depending on the logical value of the last data bit (see Figure 28.6).

Note 1. Internal DRX0 signal (DALI0.COLR1.RXDMON bit) is delayed for 3 cycles of the internal operation clock from the point where the actual level of the bus changed.

Note 2. For the stop condition, consider the DRX0 to DTX0 delay in addition to the sync delay.*1 When other devices drive DRX0 low before the DALI detects a stop condition on DRX0, even if a transmission completes (DALI0.STR1.TENDF is 1), DALI_SDI cannot be output.

Note 3. The stop condition definition is specified in the DALI standard as follows:

Standard	DALI edition 1.0	DALI edition 2.0 Single-master	DALI edition 2.0 Multi-master
Stop condition definition	2 bits*4	2450 µs (min.)	2400 µs (min.)

Note 4. The stop condition is measured from the rising edge on DRX0.
If the logical value of the last data bit is 1, the stop condition starts from the rising edge within the last data bit period. The timing for the stop condition to occur is a half-bit length earlier as compared with when the last data bit is 0, see Figure 28.6.

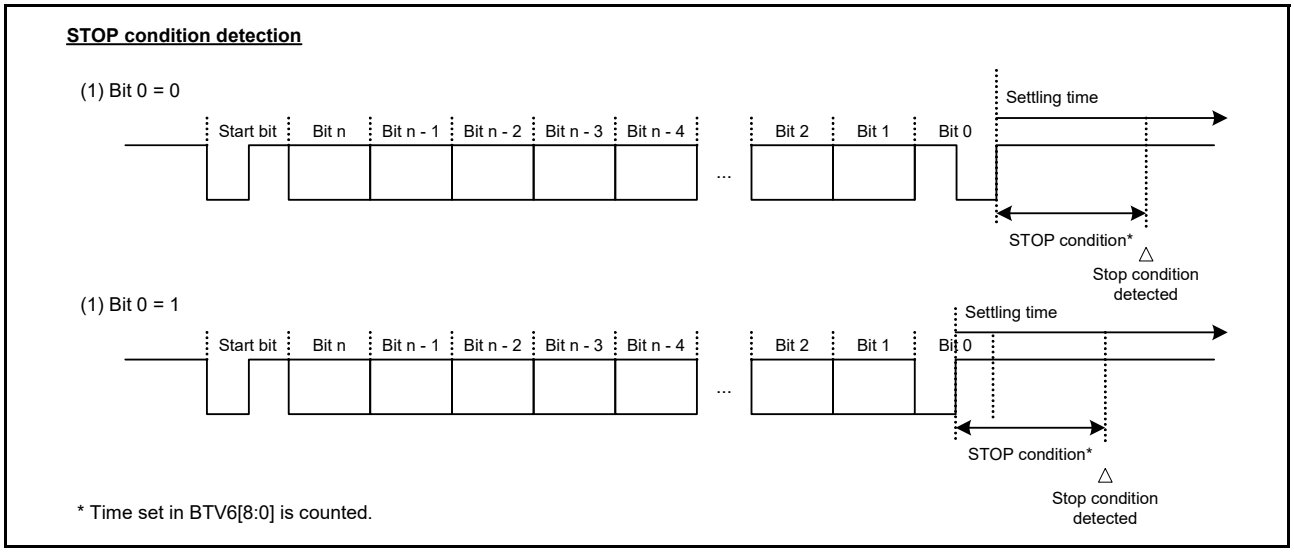


Figure 28.6 Stop condition detection

The reception settling time between frames is defined in the DALI specification edition 2.0. The reception settling time is defined in milliseconds and must be measured by software. Use the stop detection interrupt (DALI_SDI) and the falling edge detection interrupt (DALI_FEI) for the measurement. To use DALI_SDI as a trigger, add the time set in BTV6 [7:0] because the DALI_SDI output occurs when a stop condition detection completes, as shown in Figure 28.6.

The transmission settling time is also defined in the DALI specification edition 2.0 to avoid a bus collision. The transmission settling time is also defined in milliseconds and must be measured by software. To use DALI_SDI as a trigger to start the settling time measurement, add the time set in BTV6 [7:0]. Use DALI_FEI as a trigger to stop the settling time measurement.

Similar to DALI edition 2.0, the reception and transmission settling times between frames are also defined in the DALI specification edition 1.0. The settling time in the DALI specification edition 1.0 is defined in milliseconds and must be measured by software. To use DALI_SDI as a trigger to start the settling time measurement, add the time set in BTV6 [7:0]. Use DALI_FEI as a trigger to stop the settling time measurement.

28.3.3 DALI Error Detection

28.3.3.1 Manchester flaming error (MFE)

Manchester coding is used for bit definition of the DALI module. The values before and after the edge (1/4- and 3/4-bit length timing) in the middle of a bit period are sampled and compared to identify the Manchester code.

For a bit where an MFE is detected, the value sampled at the 3/4-bit timing is stored in the receive data registers (DALI0.RDR1L and DALI0.RDR1H).

When the sampled value at 1/4-bit timing and the sampled value at 3/4-bit timing are both 0s, logical value 0 is stored in

the data registers.

When the sampled value at 1/4-bit timing and the sampled value at 3/4-bit timing are both 1s, logical value 1 is stored in the data registers.

When an MFE is detected, the timing to output an interrupt (DALI_DEI) and set the flag (DALI0.STR1.MFEF) is when a stop condition is detected. This is the same as the DALI_SDI output timing.

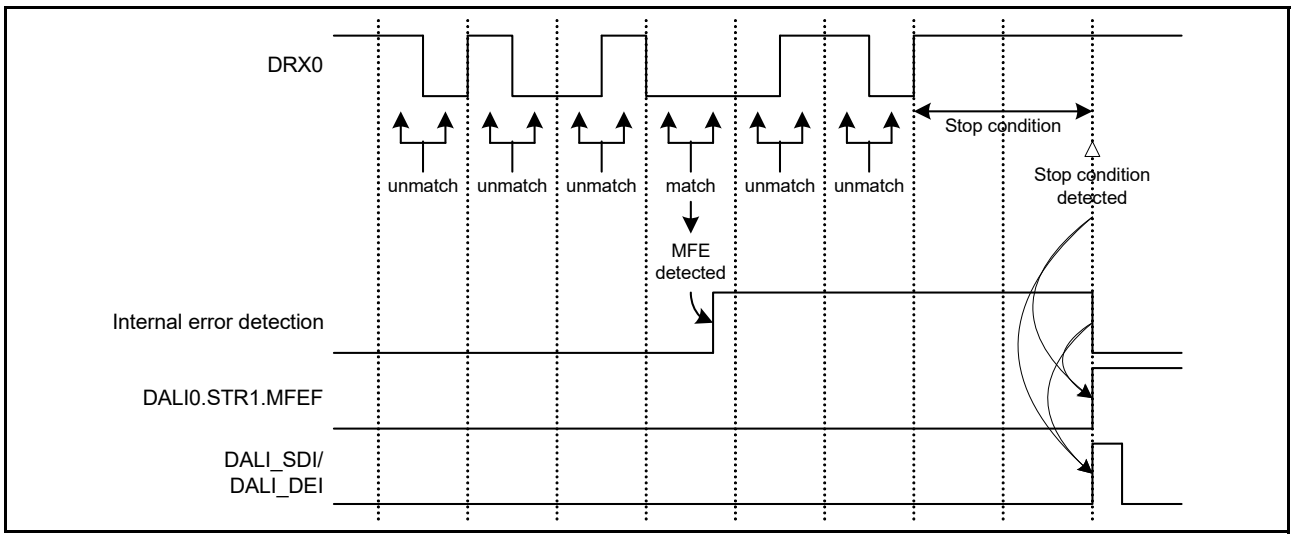


Figure 28.7 Manchester flaming error

28.3.3.2 Overrun error

After a receive operation for the current data completes, if the receive operation for the next data completes before reading the received current data, an overrun error occurs.

When an overrun error occurs, the DALI module outputs DALI_SDI and DALI_DEI at the completion of receiving the next data (when a stop condition is detected) and sets the DALI0.STR1.OVF bit.

The DALI module continues the receive operation while the DALI0.STR1.OVF bit is 1. The received data is overwritten in registers DALI0.RDR1L and DALI0.RDR1H and the received data width is overwritten in the DALI0.STR1.RDBL[5:0] bits. Flags in the DALI0.STR1 register are not overwritten. For example, if an MFE occurred in a received data 1 (DALI0.STR1.MFEF = 1) and no MFE occurred in next received data 2 (DALI0.STR1.MFEF = 0), then the previous value of the DALI0.STR1.MFEF bit remains (DALI0.STR1.MFEF = 1).

When DALI_DEI occurs, verify the error, clear the error flag, and read the received data where the error occurred. This prevents an overrun error when the next data reception completes.

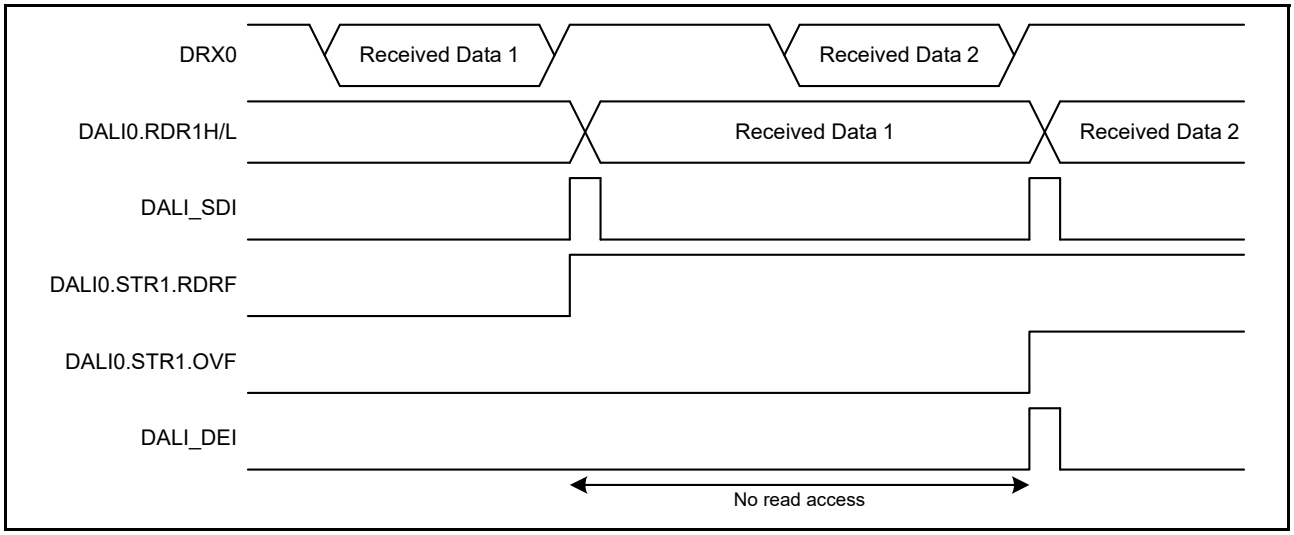


Figure 28.8 Overrun error

28.3.3.3 Frame size violation error

Frame size violation is newly defined in DALI specification edition 2.0. When the DALI module receives an unspecified data size of a frame, it results in a frame size violation.

The DALI module does not restrict the receive data length. The maximum receive data size is 32 bits. Therefore, frame size violation is not determined by hardware. When a data reception completes, check the DALI0.STR1.RDBL[5:0] bits value to ensure the received frame size is the specified data size and verify for a frame size violation with software.

The data size defined in the DALI specification edition 2.0 is as follows:

- Backward frame = 8 bits
- Forward frame = 16 bits, 20 bits *1, 24 bits, and 32 bit.*1

The DALI module continues to receive data until a stop condition is detected. When the received data is more than 32 bits, the number of bits is counted until the internal counter reaches 63, the maximum value of the counter. When the counter reaches the maximum value, it overflows and restarts counting from 0. Therefore when the O32F flag is 1, the value shown in these bits is invalid. When a stop condition is detected and the next data reception starts, the internal counter value is reset.

The DALI0.STR1.O32F flag*2 is set when the DALI module recognizes bit [33].

Note 1. Reserved forward frame is defined in DALI specification edition 2.0.

Note 2. The DALI0.STR1.RDBL[5:0] bits are updated when a stop condition is detected. This flag reports incorrect long data that is received before a stop condition is detected.

28.3.3.4 Bit timing violation error

Bit timing violation is newly defined in the DALI specification edition 2.0. It defines an edge interval of received data waveforms. To enable the bit timing violation detection function, set the DALI0.CNTR2.BTVE bit to 1.

(1) Bit timing violation

When a bit timing violation occurs, the DALI0.STR1.BTVF flag is set and DALI_DEI is output on a stop condition detection. Even if a bit timing violation occurs multiple times in a single frame, the DALI0.STR1.BTVF flag is set and DALI_DEI is only output once when a stop condition is detected.

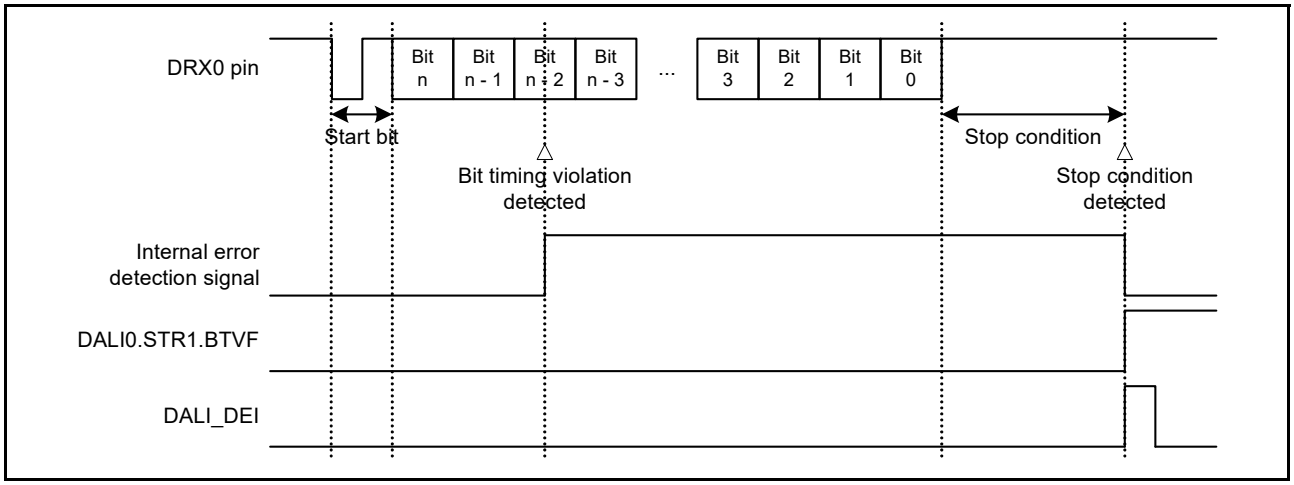


Figure 28.9 Bit timing violation error

(a) Conditions for bit timing violation occurrence

When condition 1, 2, or 3 is met as specified in the sections that follow, a bit timing violation occurs. The bit timing violation mode bit (DALI0.CNFR2.BTVM) specifies whether condition 3 is used for the violation occurrence.

To adjust the time slot for verifying the bit timing violation, set the bit timing violation threshold bits [6:1] (DALI0.BTVx; x = 1 to 6).

When the level of the DALI bus is driven high for the period of the BTV threshold value 6, it is determined as a top condition. When the level of the DALI bus is driven low for 45 ms or more, it is determined as a bus power down. The DALI module then counts up to the value specified with the BTV threshold value 6, sets the DALI0.STR1.BPDF flag, and outputs DALI_BPI. The bus power down must be verified by software.

[Condition 1]

Relative to the falling edge at the start of the start bit or the rising or falling edge at the start of the data bit, the next rising or falling edge is within the bit timing violation as shown in Figure 28.10.

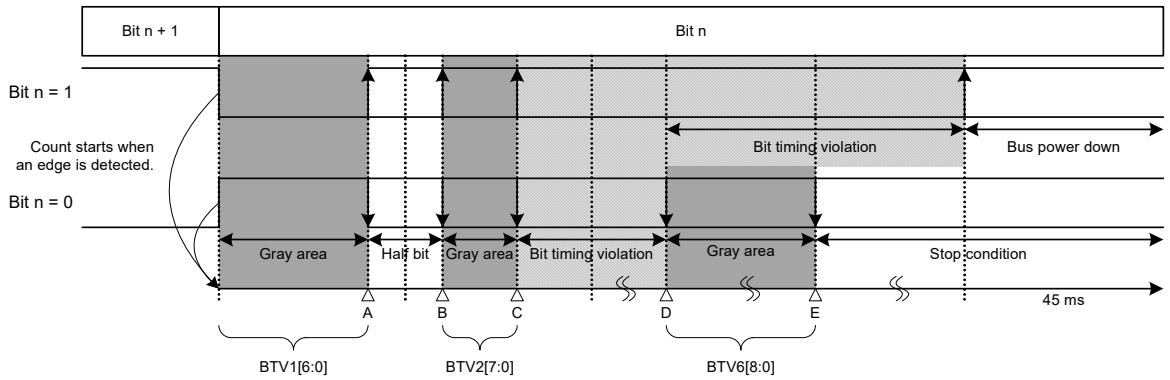
Note 1. The rising or falling edge at the start of a bit occurs when a bit, bit n, and the previous bit, bit n + 1, are of the same value. If they have different values, it is not the condition for a bit timing violation.

[Condition 2]

Relative to the rising or falling edge of the data bit, the next rising or falling edge is within the bit timing violation as shown in Figure 28.11.

[Condition 3]

Relative to the rising or falling edge of the data bit, the next rising or falling edge is within the gray area, between points G and H as shown in Figure 28.11.

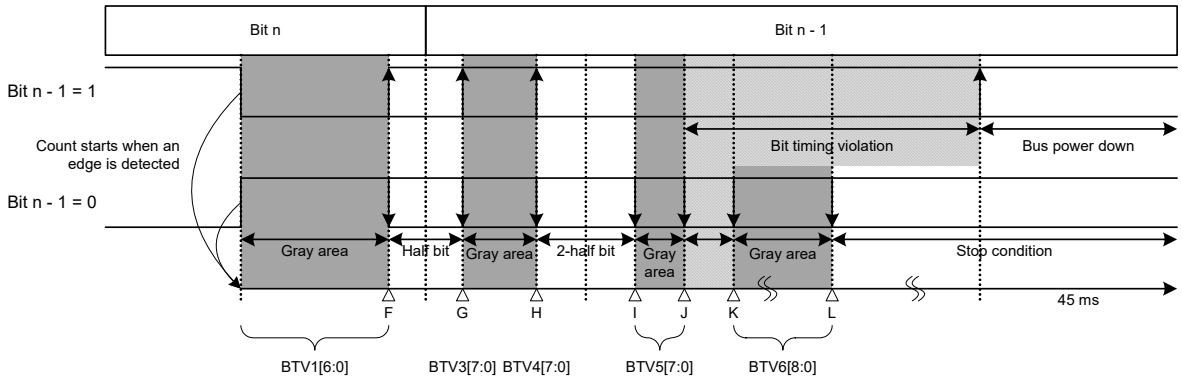


The gray area is divided into adjacent areas with the BTVx specified value as a threshold value.
The following table shows the DALI specification edition 2.0 standard values and the initial values of the DALI module.
The initial value of the BTVx (x = 1 to 6) bits includes clock error (1.5%) and sampling error in the DALI module as shown below.

Point	A	B	C	D	E
DALI standard value	333.3 µs	500.0 µs	750.0 µs	1400.0 µs	2400.0 µs
Initial value of the DALI module	BTV1 = 00h	BTV2 = 4Fh		BTV6 = DBh	
	BTV1 = 0 µs	BTV2 = 520 µs		BTV6 = 1423.5 µs	

Edge at the bit period boundary < Bit timing violation ≤ BTV threshold value 1
BTV threshold value 1 < Half bit area ≤ BTV threshold value 2
BTV threshold value 2 < Bit timing violation ≤ BTV threshold value 6
BTV threshold value 6 < Stop condition or bus power down

Figure 28.10 Bit timing violation 1



The gray area is divided into adjacent areas with the BTVx specified value as a threshold value.
The following table shows the DALI specification edition 2.0 standard values and the initial values of the DALI module.
The initial value of the BTVx (x = 1 to 6) bits includes clock error (1.5%) and sampling error in the DALI module as shown below.

Point	F	G	H	I	J	K	L
DALI standard value	333.3 µs	500.0 µs	666.7 µs	1000.0 µs	1200.0 µs	1400.0 µs	2400.0 µs
Initial value of the DALI module	BTV1 = 00h	BTV3 = 4Fh	BTV4 = 65h	BTV5 = 9Dh		BTV6 = DBh	
	BTV1 = 0 µs	BTV3 = 520 µs	BTV4 = 656.5 µs	BTV5 = 1027 µs		BTV6 = 1423.5 µs	

DALI0.CNFR2.BTVM = X: Edge at the bit period boundary < Bit timing violation ≤ BTV threshold value 1
DALI0.CNFR2.BTVM = 0: BTV threshold value 1 < Half bit area/2-half bit area ≤ BTV threshold value 5
DALI0.CNFR2.BTVM = 1: BTV threshold value 1 < Half bit area ≤ BTV threshold value 3
DALI0.CNFR2.BTVM = 1: BTV threshold value 3 < Bit timing violation ≤ BTV threshold value 4
DALI0.CNFR2.BTVM = 1: BTV threshold value 4 < 2-half bit area ≤ BTV threshold value 5
DALI0.CNFR2.BTVM = X: BTV threshold value 5 < Bit timing violation ≤ BTV threshold value 6
DALI0.CNFR2.BTVM = X: BTV threshold value 6 < Stop condition or bus power down

Figure 28.11 Bit timing violation 2

In the DALI module, the standard values shown in Figure 28.10 and Figure 28.11 are set with registers DALI0.BTVTHR1 to 4. The value set must satisfy the DALI specification edition 2.0, taking into account a clock error and sampling error of the DALI module.

Table 28.4 lists settings of bits BTV1 to 6.

Table 28.4 BTV threshold setting values

Bit name	Available value range [µs]	Initial value	Description
BTV1[6:0]	0 to 825.5	00h	Specify Point A in Figure 28.10 and Point F in Figure 28.11 within the available value range in 6.5 µs steps. The range from an edge to BTV threshold value 1 is determined as a bit timing violation. This range is described in the gray areas in Figure 28.10 and Figure 28.11. The range from BTV threshold value 1 to BTV threshold value 2 in Figure 28.10 and BTV threshold value 1 to BTV threshold value 3 in Figure 28.11 is the half bit area (pass area).
BTV2[7:0]	6.5 to 1664 (Condition: BTV1 + 1 < BTV2)	4Fh	Specify Point B in Figure 28.10 within the available value range in 6.5 µs steps. The range from BTV threshold value 1 to BTV threshold value 2 is the half bit area (pass area). The range from BTV threshold value 2 to BTV threshold value 6 is the bit timing violation.
BTV3[7:0]	6.5 to 1664 (Condition: BTV1 + 1 < BTV3)	4Fh	Specify Point G in Figure 28.11 within the available value range in 6.5 µs steps. The range from BTV threshold value 1 to BTV threshold value 3 is the half bit area (pass area). The range from BTV threshold value 3 to BTV threshold value 4 is determined as a bit timing violation when DALI0.CNFR2.BTVM is 1. This range is described in the gray areas in Figure 28.10 and Figure 28.11.
BTV4[7:0]	0 to 1657.5 (Condition: BTV3 + 1 < BTV4)	65h	Specify Point H in Figure 28.11 within the available value range in 6.5 µs steps. The range from BTV threshold value 3 to BTV threshold value 4 is determined as a bit timing violation when DALI0.CNFR2.BTVM is 1. This range is described in the gray areas in Figure 28.10 and Figure 28.11. The range from BTV threshold value 4 to BTV threshold value 5 is the 2-half bit area (pass area).
BTV5[7:0]	6.5 to 1664 (Condition: BTV4 + 1 < BTV5)	9Dh	Specify a threshold value between Point I and Point J in Figure 28.11 within the available value range in 6.5 µs steps. • When the DALI0.CNFR2.BTVM bit is 0, the range from BTV threshold value 1 to BTV threshold value 5 is the half-bit or 2-half bit area (pass area), and the range from BTV threshold value 5 to BTV threshold value 6 is the bit timing violation. • When the DALI0.CNFR2.BTVM bit is 1, the range from BTV threshold value 4 to BTV threshold value 5 is the 2-half bit area (pass area), and the range from BTV threshold value 5 to BTV threshold value 6 is the bit timing violation.
BTV6[8:0]	1254.5 to 3328 (Condition: BTV2 + 1 < BTV6 and BTV5 + 1 < BTV6)	DBh	Specify Point D in Figure 28.10 and a threshold value between Point K and Point L in Figure 28.11 within the available value range in 6.5 µs steps. It is prohibited to set a value smaller than 1254.5 µs. The minimum available value is C0h. The range from BTV threshold value 2 to BTV threshold value 6 in Figure 28.10 and BTV threshold value 5 to BTV threshold value 6 in Figure 28.11 is the bit timing violation. The range beginning with the BTV threshold value 6 is determined as the stop condition or the bus power down.

28.3.3.5 Bus power down

When the level of the DALI bus is driven low for 45 ms or more, it is a bus power down and appropriate actions must be taken.

A bus power down is determined when the DALI module counts the DALI bus low level period up to the period of BTV threshold value 6. Thereafter, the DALI0.STR1.BPDF flag is set and DALI_BPI is output. After DALI_BPI is output, measure the low level period of the DALI bus for least for 45 ms with software to determine whether it is a bus power down or not.

When the DALI module detects a rising edge of the DRX0 pin, it clears the DALI0.STR1.BPDF flag and returns to the receive operation process. When a stop condition is detected after the receive operation starts, DALI_SDI is output. When DALI_SDI is output, stop the 45 ms measurement. When a probable bus power down is detected again after the receive operation starts, the DALI0.STR1.BPDF flag is set to 1 again and DALI_BPI is output.

If the DALI0.STR1.BPDF flag is reset to 0 after the 45 ms measurement, it means that the DALI bus was not held low during the 45 ms measurement.

When the DALI bus is not held low during the 45 ms measurement, the DALI module returns to the receive operation process. In this case, the received data is not reliable, so discard the received data before a stop condition is detected after the DALI0.STR1.BPDF flag changed from 1 to 0.

When DALI_SDI or DALI_BPI is not output during the 45 ms measurement and the DALI0.STR1.BPDF flag is 1 after the 45 ms measurement, the DALI bus is determined as a bus power down.

The DALI module continues the receive operation until a stop condition is detected while the DALI0.STR1.BPDF flag is 1. Therefore, to stop the receive operation, set bits DALI0.CTR1.TE and DALI0.CTR1.RE to 0 and issue a software reset by setting the DALI0.SWRR1.SWR bit to 1. After the DALI bus is restored, set bits DALI0.CTR1.TE and DALI0.CTR1.RE to 1 to restart communication.

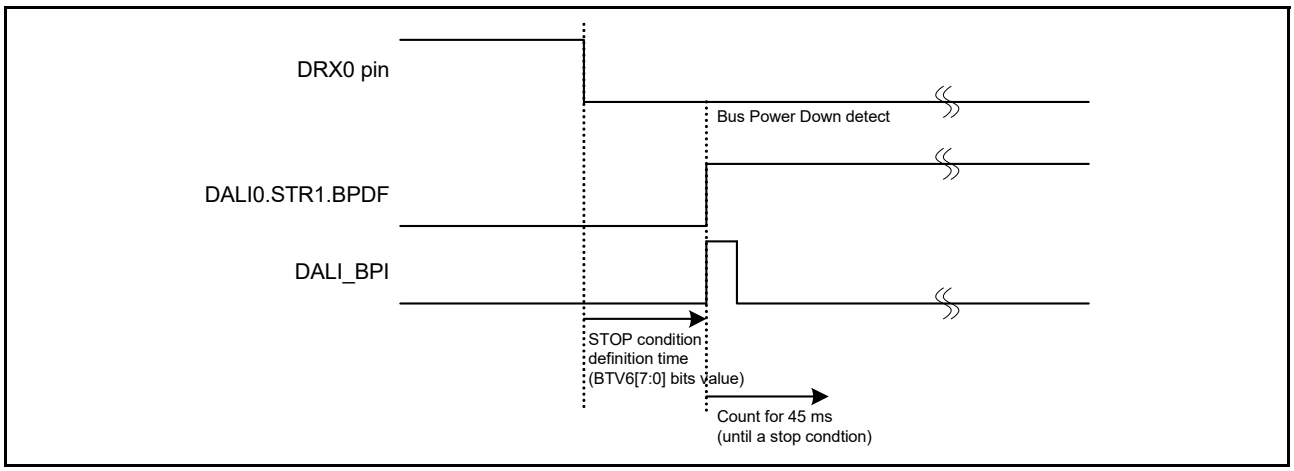


Figure 28.12 Bus power down

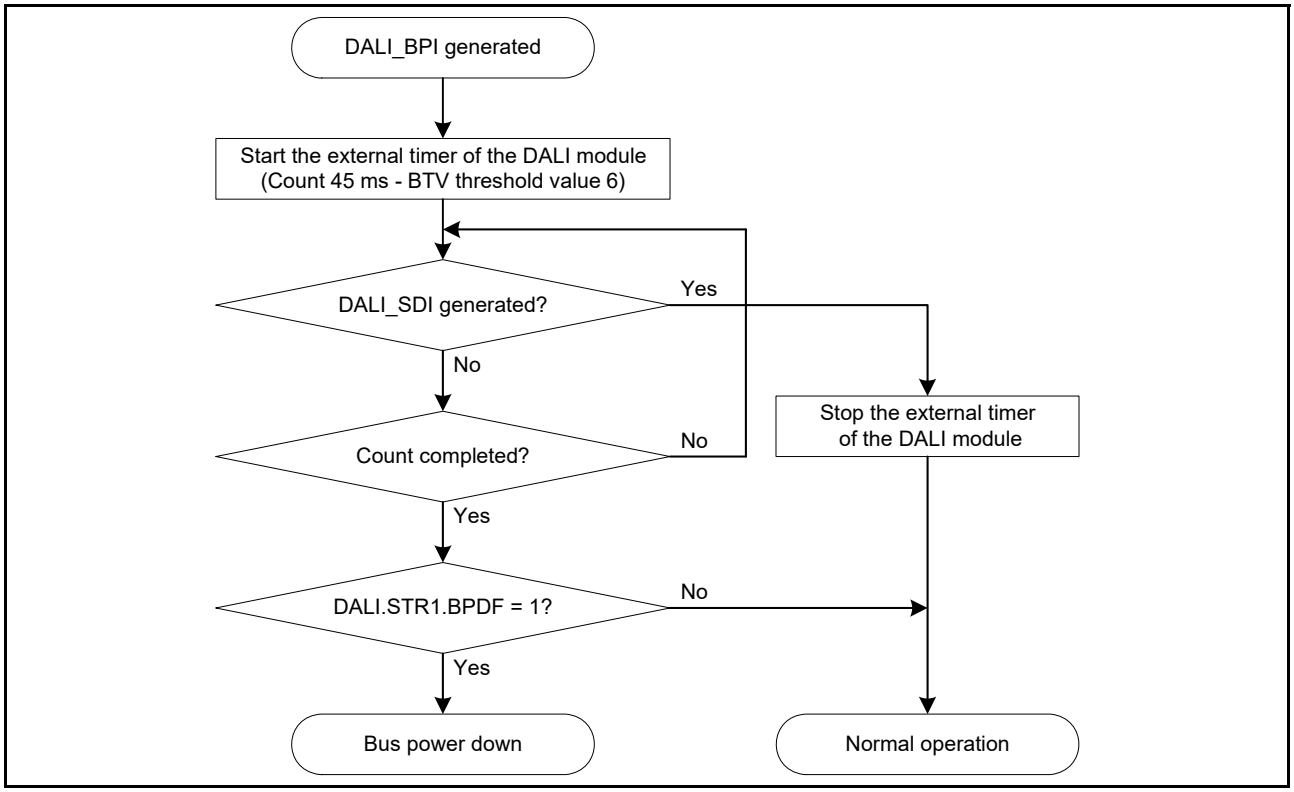


Figure 28.13 Flow of bus power down

28.3.4 DALI Collision

28.3.4.1 Overview of collision

The DALI module supports multi-master communication.

If two or more masters transmit data simultaneously during the multi-master communication, a collision occurs on the bus. When the DALI0.CNFR2.CDE bit is set to 1, the DALI module collision detection function is enabled and the collision detection interrupt (DALI_CLI) is generated. When a collision is detected during transmission, stop the transmission and perform the collision recovery or collision avoidance based on the collision occurrence condition.

For backward frame transmission, set the DALI0.CNFR2.CDE bit to 0 and disable the collision detection function.

The DALI module detects a collision during the receive operation, where DALI0.CTR1.RE bit = 1 and DALI0.CTR1.TE bit = 0. If you do not want to detect a collision between multiple masters, set the DALI0.CNFR2.CDE bit to 0.

28.3.4.2 Criteria for collision detection

Select the criteria for collision detection with the collision detection mode bit (DALI0.CDM0).

Table 28.5 shows the relation between collision detection mode and collision detection interrupt (DALI_CLI).

Table 28.5 Criteria based on CDM set values

Setting value in the CDM0	Collision detection area *1			Collision detection interrupt (DALI_CLI) condition *2
	Destroy	Avoidance	Valid	
0	Detected	Not detected	Not detected	Condition 1A or Condition 2A
1	Detected	Detected	Not detected	When one of the following conditions is met*3,*4 • Condition 1A or Condition 1B • Condition 2A or Condition 2B.

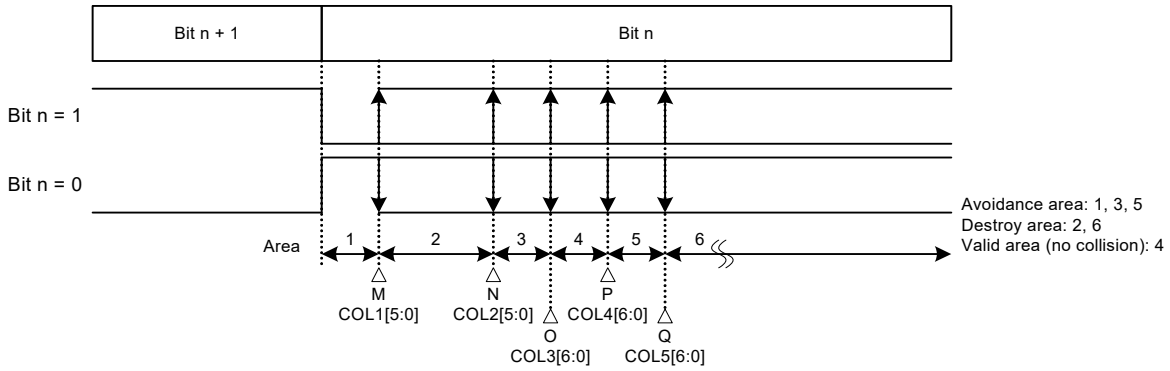
Note 1. The DALI specification edition 2.0 (IEC-62386-101) defines the following areas:
- Destroy: Destroy area
- Avoidance area: Gray area
- Valid area: Valid half bit/2 Valid half bit.

Note 2. For details on the conditions, see Figure 28.14 and Figure 28.15.

Note 3. Adjust the timing to determine a collision by setting COLx (x = 1 to 9) bits, see Figure 28.14 and Figure 28.15.

Note 4. When a collision detection interrupt (DALI_CLI) occurs, use the collision detection information to set any processing with software after the collision detection. For details, see section 28.3.4.4 Collision detection information.

The collision detection criteria are valid when any of the conditions shown in Figure 28.14 and Figure 28.15 are met.



The following table shows The DALI specification edition 2.0 standard values and initial values of the DALI module.
The initial value of COLx (x = 1 to 5) bits includes clock error (1.5%) and sampling error of the DALI module as shown below.

Point	M	N	O	P	Q
Setting bit	COL1[5:0]	COL2[5:0]	COL3[6:0]	COL4[6:0]	COL5[6:0]
DALI standard value	100.0 µs	356.7 µs	400.0 µs	433.3 µs	476.7 µs
Initial value of the DALI module	97.5 µs	370.5 µs	390.0 µs	448.5 µs	468.0 µs

Criteria for collision determination conditions:

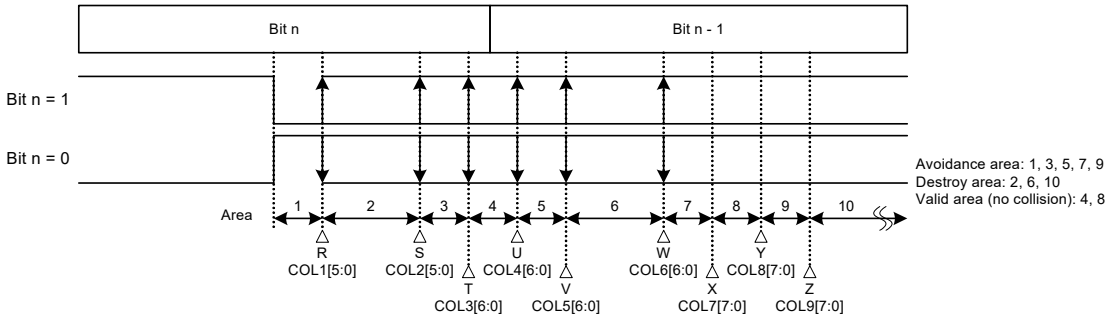
Condition 1A: Any of the following conditions is met.
- An edge is present in destroy area 2 and 6.
- DRX0 is held low until destroy area 6 comes.

Condition 1B: The following condition is met.
- An edge is present in avoidance area 1, 3, and 5.

Relation between the collision detection areas and the collision threshold values:

Edge at the bit period boundary < Area 1 ≤ COL threshold value 1
COL threshold value 1 < Area 2 ≤ COL threshold value 2
COL threshold value 2 < Area 3 ≤ COL threshold value 3
COL threshold value 3 < Area 4 ≤ COL threshold value 4
COL threshold value 4 < Area 5 ≤ COL threshold value 5
COL threshold value 5 < Area 6

Figure 28.14 Collision detection timing 1



The following table shows the DALI specification edition 2.0 standard values and initial values of the DALI module.
The initial value of COLx (x = 1 to 9) bits includes clock error (1.5%) and sampling error of the DALI module as shown below.

Point	R	S	T	U	V	W	X	Y	Z
Setting bit	COL1[5:0]	COL2[5:0]	COL3[6:0]	COL4[6:0]	COL5[6:0]	COL6[6:0]	COL7[7:0]	COL8[7:0]	COL9[7:0]
DALI standard value	100.0 µs	356.7 µs	400.0 µs	433.3 µs	476.7 µs	723.3 µs	800.0 µs	866.7 µs	943.3 µs
Initial value of the DALI module	97.5 µs	370.5 µs	390.0 µs	448.5 µs	468.0 µs	741.0 µs	786.5 µs	890.5 µs	923.0 µs

Criteria for collision determination conditions
Condition 2A: Any of the following conditions is met:
- An edge is present in destroy area 2, 6 and 10.
- DRX0 is held low until destroy area 10 comes.

Condition 2B: The following condition is met:
- An edge is present in avoidance area 1, 3, 5, 7 and 9.

Relation between collision detection areas and collision threshold values
Edge at the bit period boundary < Area 1 ≤ COL threshold value 1
COL threshold value 1 < Area 2 ≤ COL threshold value 2
COL threshold value 2 < Area 3 ≤ COL threshold value 3
COL threshold value 3 < Area 4 ≤ COL threshold value 4
COL threshold value 4 < Area 5 ≤ COL threshold value 5
COL threshold value 5 < Area 6 ≤ COL threshold value 6
COL threshold value 6 < Area 7 ≤ COL threshold value 7
COL threshold value 7 < Area 8 ≤ COL threshold value 8
COL threshold value 8 < Area 9 ≤ COL threshold value 9
COL threshold value 9 < Area 10

Figure 28.15 Collision detection timing 2

The DALI module sets the standard values shown in Figure 28.14 and Figure 28.15 in registers DALI0.COLTHR1 to DALI0.COLTHR5. The value set must satisfy the DALI specification edition 2.0 standard, taking into account a clock error and sampling error of the DALI module. Table 28.6 shows settings for bits COL1 to COL9.

Table 28.6 COL threshold setting values (1 of 2)

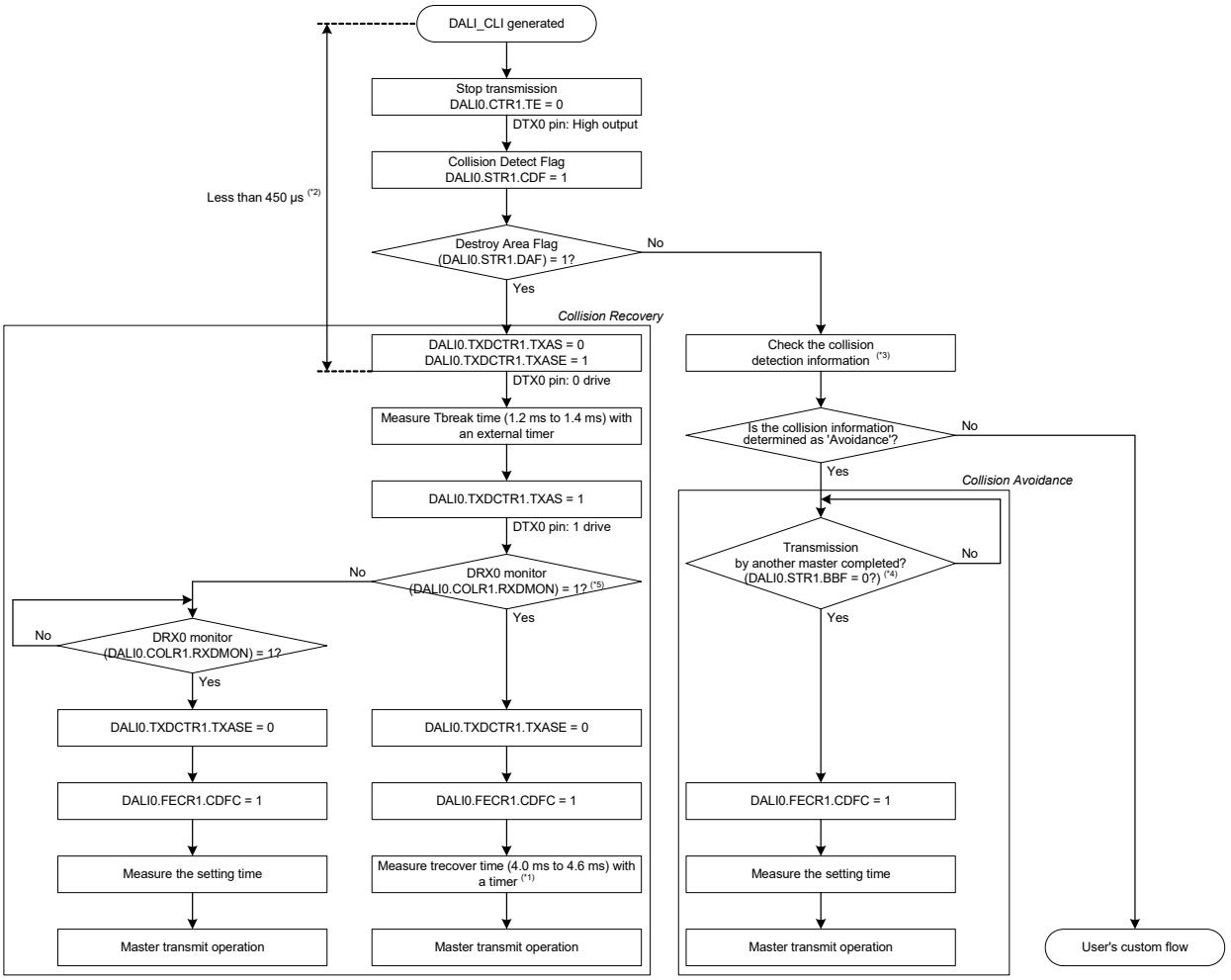
Bit name	Available value range [µs]	Initial Value	Description
COL1[5:0]	0 to 409.5	0Fh	Specify Point M in Figure 28.14 and Point R in Figure 28.15 within the available value range in 6.5 µs steps. The range from an edge to COL threshold value 1 is the avoidance area and the range from COL threshold value 1 to COL threshold value 2 is the destroy area.
COL2[5:0]	6.5 to 416 (Condition: COL1 + 1 < COL2)	38h	Specify Point N in Figure 28.14 and Point S in Figure 28.15 within the available value range in 6.5 µs steps. The range from COL threshold value 1 to COL threshold value 2 is the destroy area and the range from COL threshold value 2 to COL threshold value 3 is the avoidance area.
COL3[6:0]	0 to 825.5 (Condition: COL2 + 1 < COL3)	3Ch	Specify Point O in Figure 28.14 and Point T in Figure 28.15 within the available value range in 6.5 µs steps. The range from COL threshold value 2 to COL threshold value 3 is the avoidance area and the range from COL threshold value 3 to COL threshold value 4 is the valid area.
COL4[6:0]	6.5 to 832 (Condition: COL3 + 1 < COL4)	44h	Specify Point P in Figure 28.14 and Point U in Figure 28.15 within the available value range in 6.5 µs steps. The range from COL threshold value 3 to COL threshold value 4 is the valid area and the range from COL threshold value 4 to COL threshold value 5 is the avoidance area.

Table 28.6 COL threshold setting values (2 of 2)

Bit name	Available value range [µs]	Initial Value	Description
COL5[6:0]	0 to 825.5 (Condition: COL4 + 1 < COL5)	48h	Specify Point Q in Figure 28.14 and Point V in Figure 28.15 within the available value range in 6.5 µs steps. The range from COL threshold value 4 to COL threshold value 5 is the avoidance area and the range from COL threshold value 5 to COL threshold value 6 is the destroy area.
COL6[6:0]	6.5 to 832 (Condition: COL5 + 1 < COL6)	71h	Specify Point W in Figure 28.15 within the available value range in 6.5 µs steps. The range from COL threshold value 5 to COL threshold value 6 is the destroy area and the range from COL threshold value 6 to COL threshold value 7 is the avoidance area.
COL7[7:0]	0 to 1657.5 (Condition: COL6 + 1 < COL7)	79h	Specify Point X in Figure 28.15 within the available value range in 6.5 µs steps. The range from COL threshold value 6 to COL threshold value 7 is the avoidance area and the range from COL threshold value 7 to COL threshold value 8 is the valid area.
COL8[7:0]	6.5 to 1664 (Condition: COL7 + 1 < COL8)	88h	Specify Point Y in Figure 28.15 within the available value range in 6.5 µs steps. The range from COL threshold value 7 to COL threshold value 8 is the valid area and the range from COL threshold value 8 to COL threshold value 9 is the avoidance area.
COL9[7:0]	0 to 1657.5 (Condition: COL8 + 1 < COL9)	8Eh	Specify Point Z in Figure 28.15 within the available value range in 6.5 µs steps. The range from COL threshold value 8 to COL threshold value 9 is the avoidance area and the range beginning with COL threshold value 9 is the destroy area.

28.3.4.3 Collision processing flow

Figure 28.16 shows the flow of collision recovery and collision avoidance on a collision occurrence.



Note 1. To avoid collisions, it is strongly recommended that a multi-master transmitter starts its transmission at a random point between the minimum and maximum recovery time.

Note 2. When starting the collision recovery, the multi-master transmitter forces the bus to be in active state within 450 µs before measuring the break time (Tbreak).

Note 3. Check the collision information based on the values in Table 28.7 to determine whether it is 'Avoidance' or 'Not avoidance'. If it is 'Not avoidance', go to a custom flow.

Note 4. When the DALI0.CTR1.TE bit changes from 1 to 0, the DALI.STR1.BBF bit is active. The DALI0.STR1.BBF is active until a stop condition is detected.

Note 5. Read the DRX0 monitor after waiting for DTX0 to DRX0 delay.

Figure 28.16 Flow of collision process

When the DALI module detects a collision during transmission, check the DALI status register 1 (DALI0.STR1) and clear the flags that are set before starting the master transmission. See the collision recovery process or collision avoidance process in Figure 28.16. If you do not clear the collision flag (DALI0.STR1.CDF), the collision information is not updated to new information and if DALI0.STR1.RDRF bit is 1, the DALI reception data registers (DALI0.RDR1H and DALI0.RDR1L) also must be read.

When the DALI module detects a collision only during a reception, the processing shown in Figure 28.16 is not required. Check the DALI status register (DALI0.STR1), clear the flags, and read the DALI reception data registers (DALI0.RDR1H and DALI0.RDR1L) as needed.

28.3.4.4 Collision detection information

The DALI module saves the following information when a collision detection interrupt (DALI_CLI) occurs.

Table 28.7 Collision detection information

Collision detection information	Bit
DTX0 value on a collision occurrence	DALI0.COLR1.TXDCV
DRX0 state (rising or falling) on a collision occurrence	DALI0.COLR1.RXDCEG
Collision factor (edge or not edge)	DALI0.COLR1.CLDAF
Timing information on a collision occurrence	DALI0.COLR1.CDTF1 and DALI0.COLR1.CDTF2[3:0]

Note: The DALI module saves the collision detection information when a collision is detected.

The function to save the collision detection information is enabled when a collision occurs while the collision detect flag is not generated (DALI0.STR1.CDF = 0). After the collision detect flag (DALI0.STR1.CDF) is cleared, the next information is stored. Be sure to clear the collision detect flag (DALI0.STR1.CDF).

Figure 28.17 shows an example of how to use the collision detection information when a collision occurred on an edge in the middle of a bit period (middle edge).

Figure 28.18 shows an example of how to use the collision detection information when a collision occurred on an edge at the bit period boundary (boundary edge).

Figure 28.19 shows an example of how to use the collision detection information when a collision occurred on a middle edge without a boundary edge.

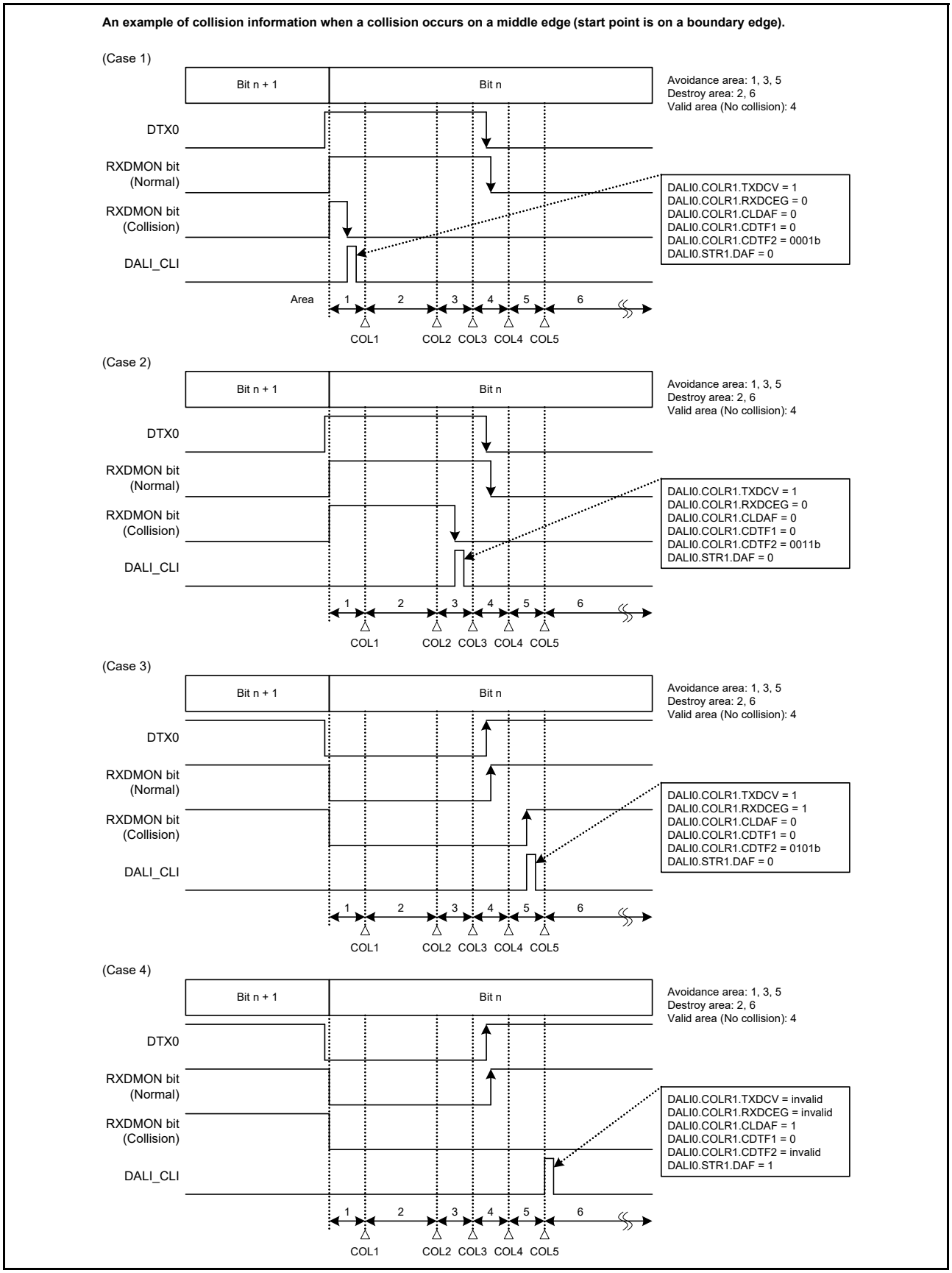


Figure 28.17 Usage example of collision detection information 1

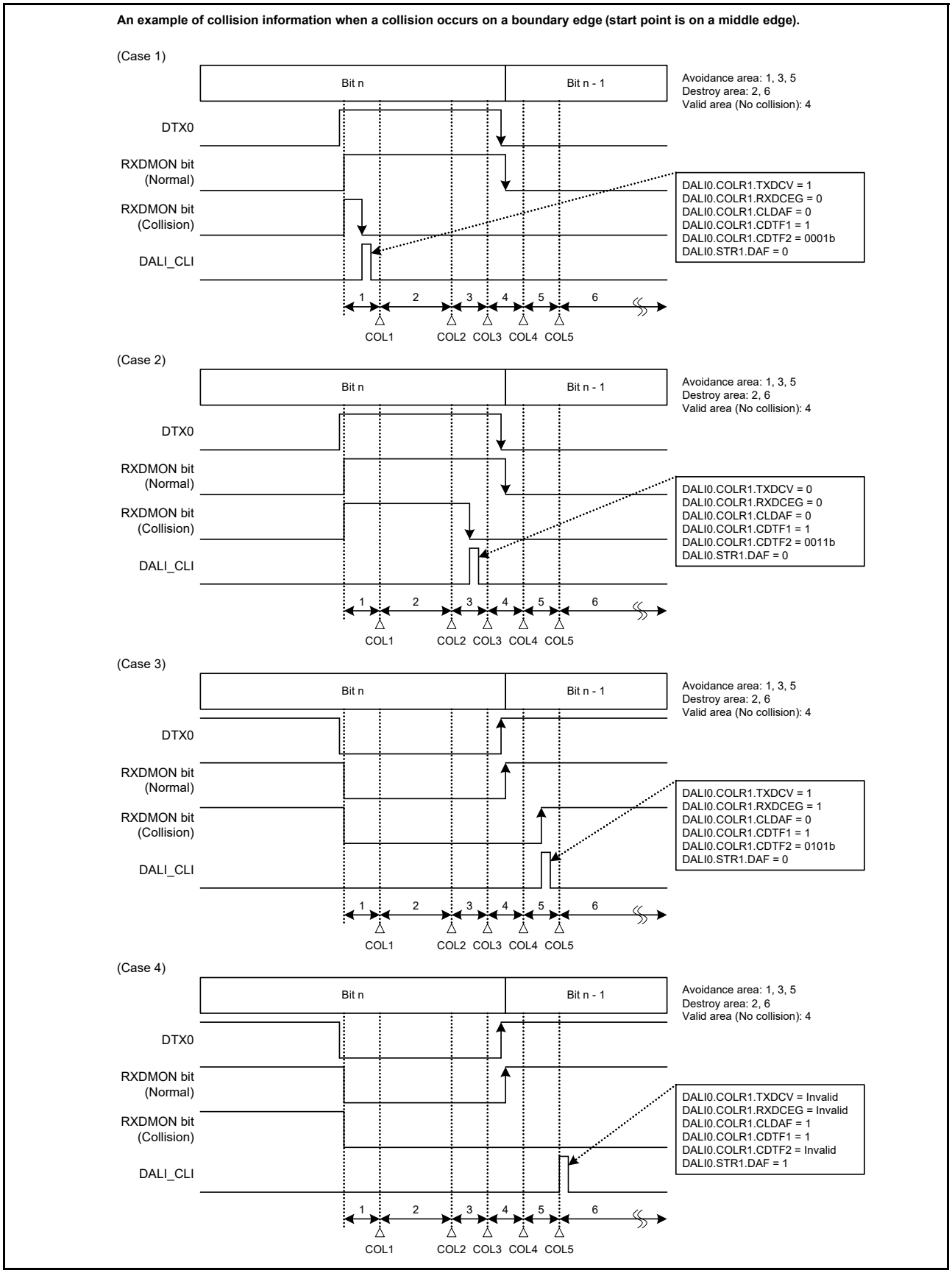


Figure 28.18 Usage example of collision detection information 2

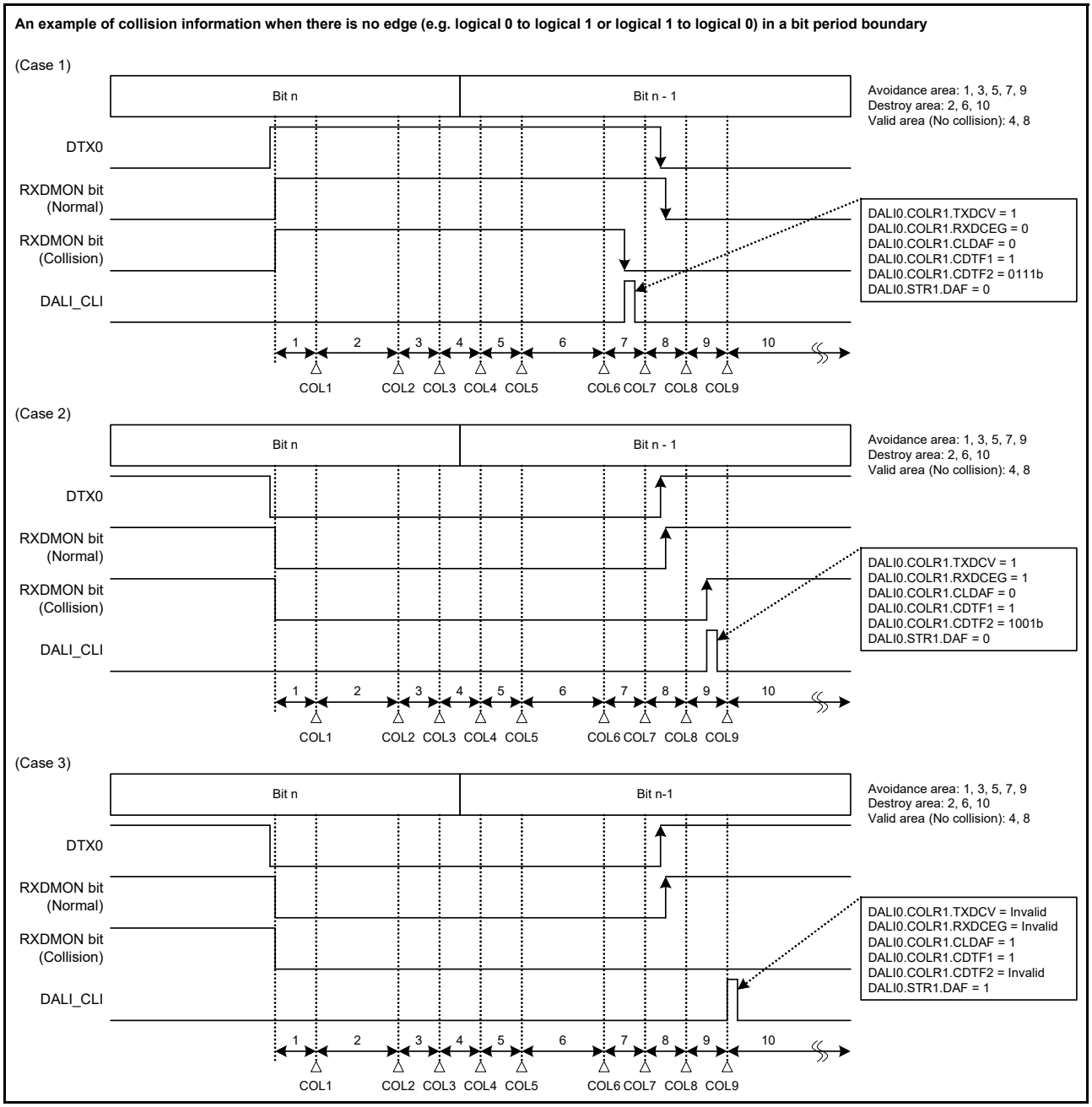


Figure 28.19 Usage example of collision detection information 3

28.3.5 Sampling Timing of the DRX Input Signal and Bit Length Adjustment

The DALI module uses Manchester code to define bits. An edge always occurs during a 1-bit period (middle edge). The DALI uses a middle edge to adjust the bit length and measure the sampling timing. 1/4-bit timing and 3/4-bit timing are defined before and after a middle edge and the DRX0 value after synchronization is sampled at these timings. The sampling value at 3/4-bit timing is used as the logical value.

If a middle edge occurs between 1/4- and 3/4-bit timing, the data bit is received. The waveform described in section 28.3.5.1 is used to detect an error of the bit length on a middle edge. An edge does not always occur on a boundary edge, so a boundary edge is not used as a reference.

In this manual, the sampling timings are referred to as 1/4-bit timing and 3/4-bit timing to make the descriptions clear. The sampling points in the DALI module are defined in Table 28.8 and are not exactly 3/4-bit timing. The sampling points also vary depending on the value in the DALI0.CNFR2.SGA bit.

Table 28.8 Sampling points

Definition	SGA bit = 0	SGA bit = 1
1/4 bit length 1/4 baud rate timing 1/4 bit sampling value 1/4 bit timing	Default value (1/4 bit length)	Default value - 16 cycles
3/4 bit length 3/4 bit sampling value 3/4 bit timing	Default value (3/4 bit length + 1 cycle)	Default value + 25 cycles

28.3.5.1 Adjusting the edge allowable area for the DRX input signal

The DALI module receives the high or low period. To extend the period, set the DALI0.CNFR2.SGA bit to 1.

When DALI0.CNFR2.SGA bit is 0 (default):

High/low period of Manchester code: 318.5[μs] to 510.25[μs]

When DALI0.CNFR2.SGA bit is 1:

High/low period of Manchester code: 295.75[μs] to 559[μs]

28.3.6 DTX Width Modulation

When a low or high level period of the DTX0 waveform becomes shorter due to degradation of an external device (photocoupler), use this function to adjust the low period of the DTX0 waveform. The function calculates the shortage of the period due to degradation and enables the receiver to accept a waveform that is nearly 50% of duty.

The DALI module adjusts the low width of the DTX0 waveform by setting the DALI0.CNFR2.TXWE bit to 1. If an external device is not degraded and the DTX0 waveform appears correct, disable this function (DALI0.CNFR2.TXWE bit = 0) and use the DALI0.TXWR1 register with the default value.

The DTX0 output waveform is modulated as follows:

When the DALI0.CNFR2.TXWE bit is 1:

- Low level width: (*Setting value of DALI0.TXWR1.TXLW*[6:0] + 1) × 6.5[μs]
- High level width: 832[μs] - {(*Setting value of DALI0.TXWR1.TXLW*[6:0] + 1) × 6.5[μs]}

When the DALI0.CNFR2.TXWE bit is 0:

- Low level width: 416[μs] (Reset value = 3Fh)
- High level width: 416[μs] (Reset value = 3Fh)

Values available for setting the DALI0.TXWR1.TXLW[6:0] bits are from 20h (= 214.5[μs]) to 5Eh (= 617.5[μs]).

28.4 Operation

28.4.1 Initial Setting

Before transmitting and receiving data, follow the flow in Figure 28.20 to set each control register.

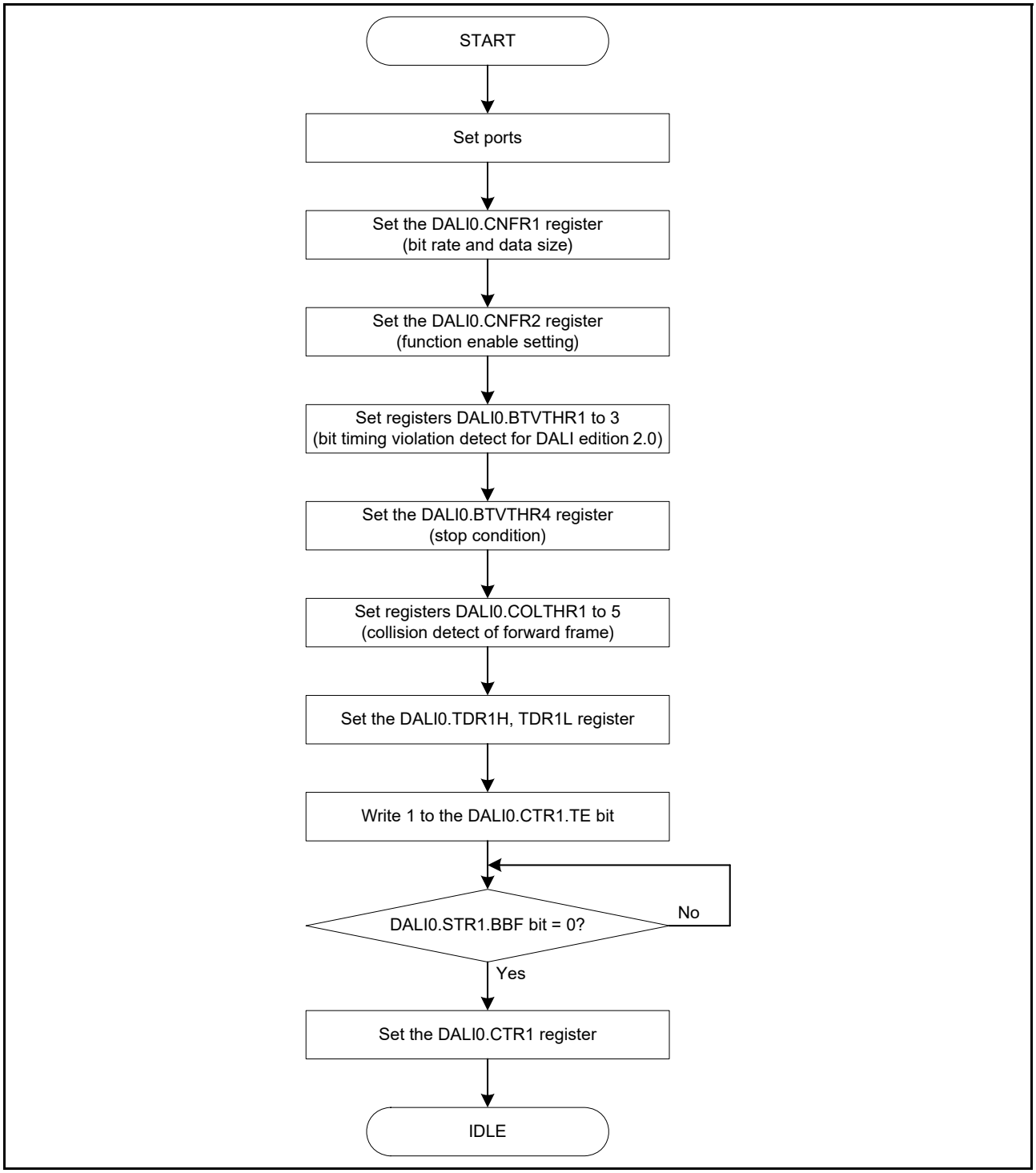


Figure 28.20 Initial setting flow

28.4.2 Software Reset

When a reset is required for data registers, flag bits, internal registers, and internal counters, follow the flow in Figure 28.21. Output pins of the DALI module are also reset. For target registers and output pins of the DALI module for software reset, see 28.2.20.

28.4.2.1 Use of software reset

(1) To halt a transmission and reception

Perform the flow in Figure 28.21 to halt a transmission and a reception.

(2) To stop a reception during bus power down

The DALI module continues to receive frames during a bus power down. To stop reception during a bus power down, perform the flow in Figure 28.21. That is, after a DALI bus returns from the bus power down state, set the DALI0.CTR1.TE and DALI0.CTR1.RE bits to 1, then resume communication.

(3) To stop a reception when receiving 32-bit data or longer

While the DALI module receives 32-bit or longer data, DALI_SDI is not output. To stop the reception, confirm the DALI0.STR1.O32F bit is 1 and perform the flow in Figure 28.21. That is, set the DALI0.CTR1.RE bit to 0, and after a DALI bus restores, set the DALI0.CTR1.RE bit to 1, then restart reception.

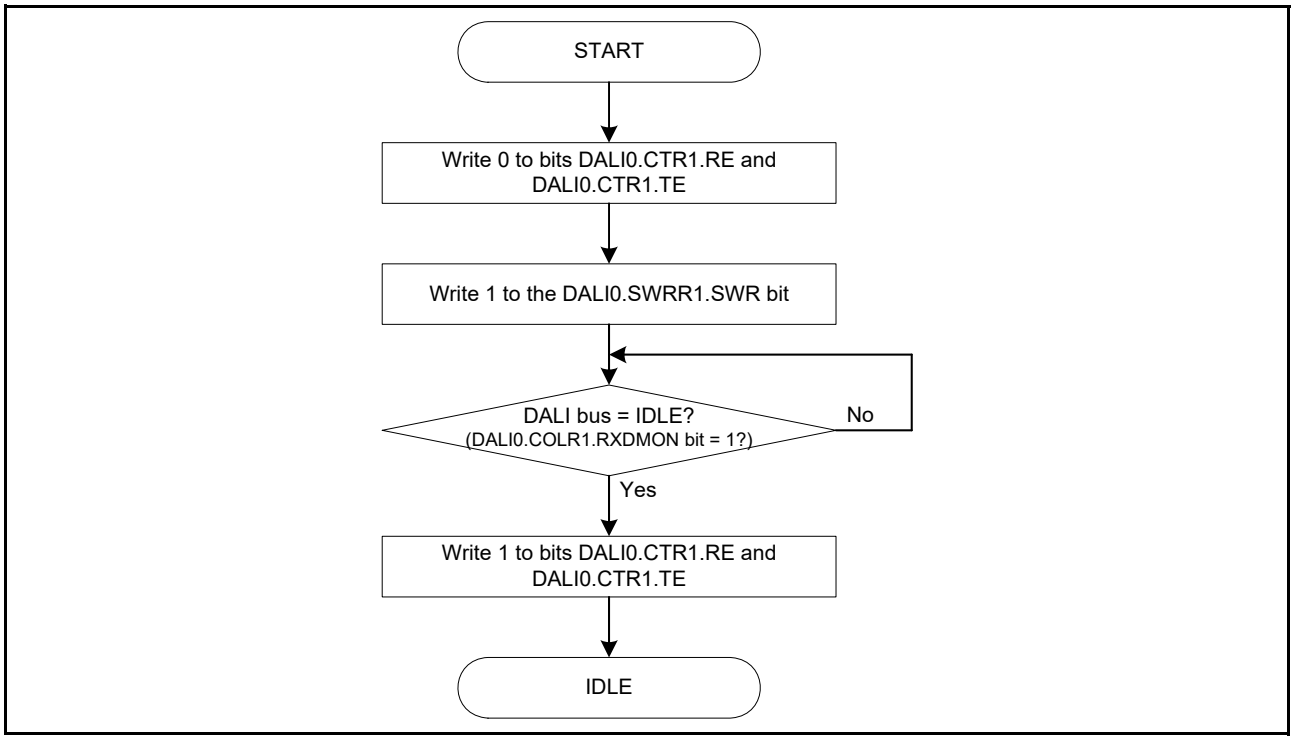
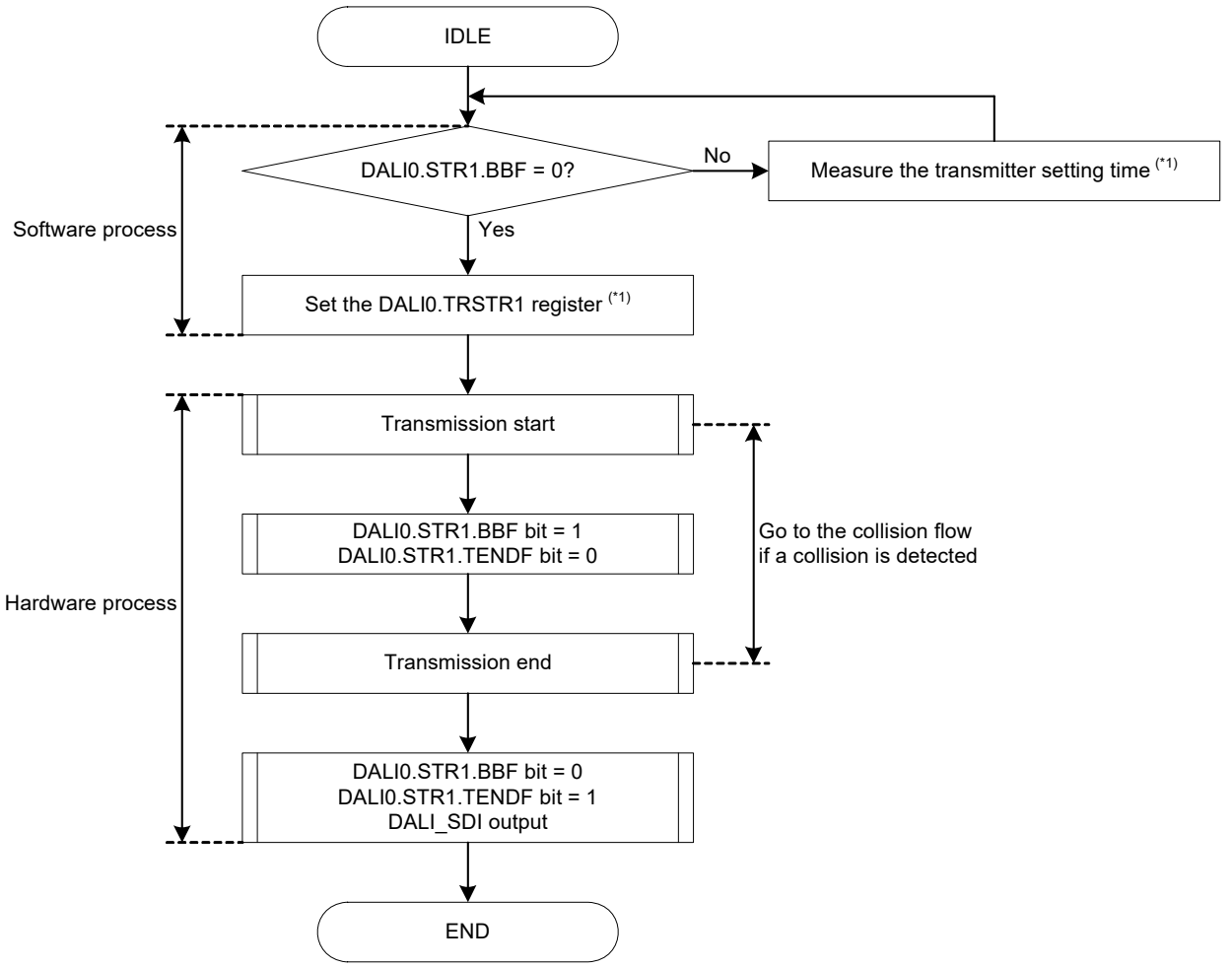


Figure 28.21 Software reset flow

28.4.3 Transmission

Figure 28.22 shows a flow for transmitting data in DALI communication.

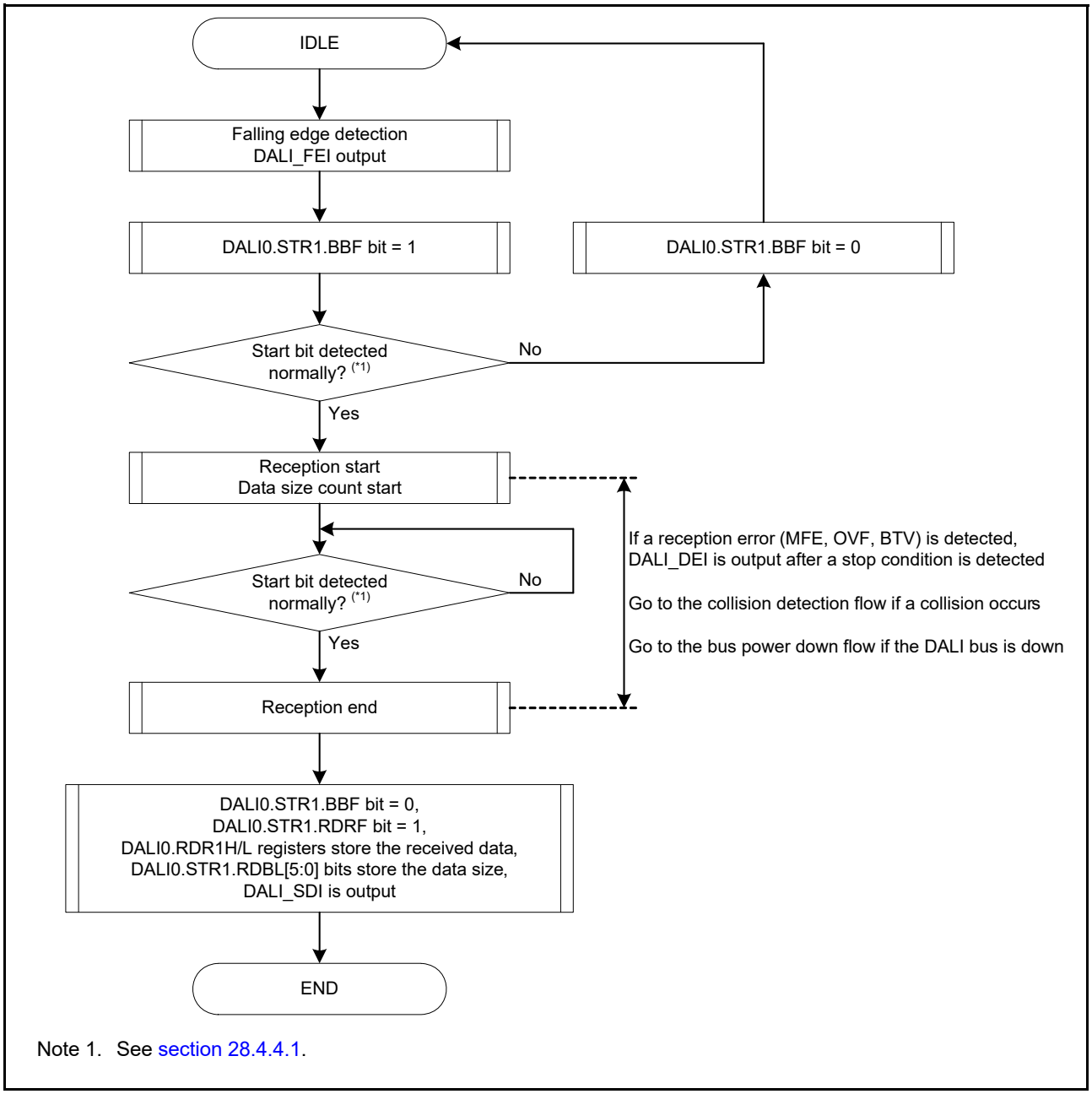


Note 1. The transmitter setting time is defined by the DALI specification edition 2.0, of which the DALI module does not measure. When writing in the DALI0.TRSTR1 register, follow the setting time defined.

Figure 28.22 Transmission flow

28.4.4 Reception

Figure 28.23 shows a flow for receiving data in DALI communication.



Note 1. See section 28.4.4.1.

Figure 28.23 Reception flow

28.4.4.1 Detecting a start bit

The DALI module has a function that can prevent from incorrectly detecting a start bit due to noise.

When a falling edge is input to the DRX0 pin, a receive operation starts. The DALI0.STR1.BBF flag is then set. When a high level on the DRX0 pin is detected at the 1/4-bit timing, the falling edge determines that it was caused by noise. The DALI0.STR1.BBF flag is then cleared and the internal state returns to IDLE.

This function removes noise generated during the period from falling edge detection through to 1/4-bit timing. However, if a start bit is generated during this period, the values of each bit are sampled at a maximum of 1/4-bit length earlier (see Figure 28.24). In that case, a Manchester flaming error, bit timing violation, or a frame size violation might be the cause.

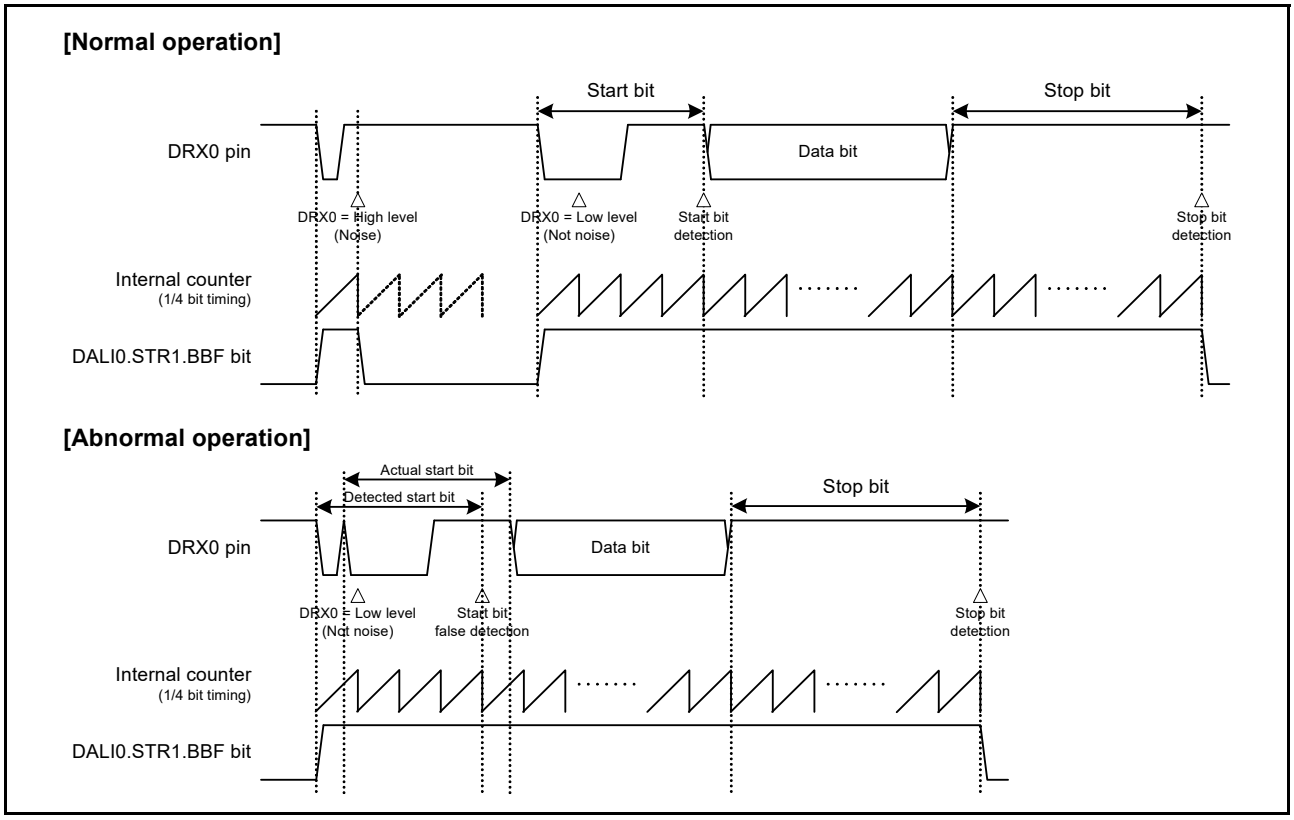


Figure 28.24 Detecting a start bit

28.4.5 Outputting an Interrupt

28.4.5.1 DALI_FEI, DALI_SDI, DALI_DEI

When DALI_SDI or DALI_DEI is received, verify the flag and the received data.

DALI_SDI and DALI_FEI are used for measurement with an external timer of the DALI module.

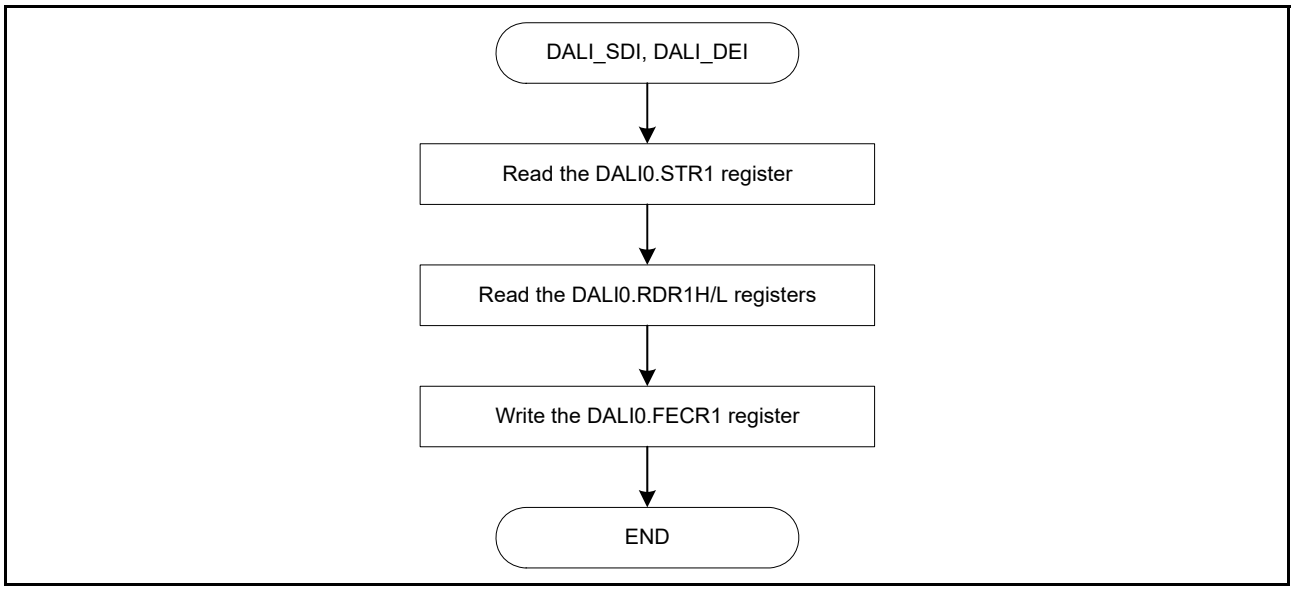


Figure 28.25 DALI_SDI and DALI_DEI operation flows (1 of 2)

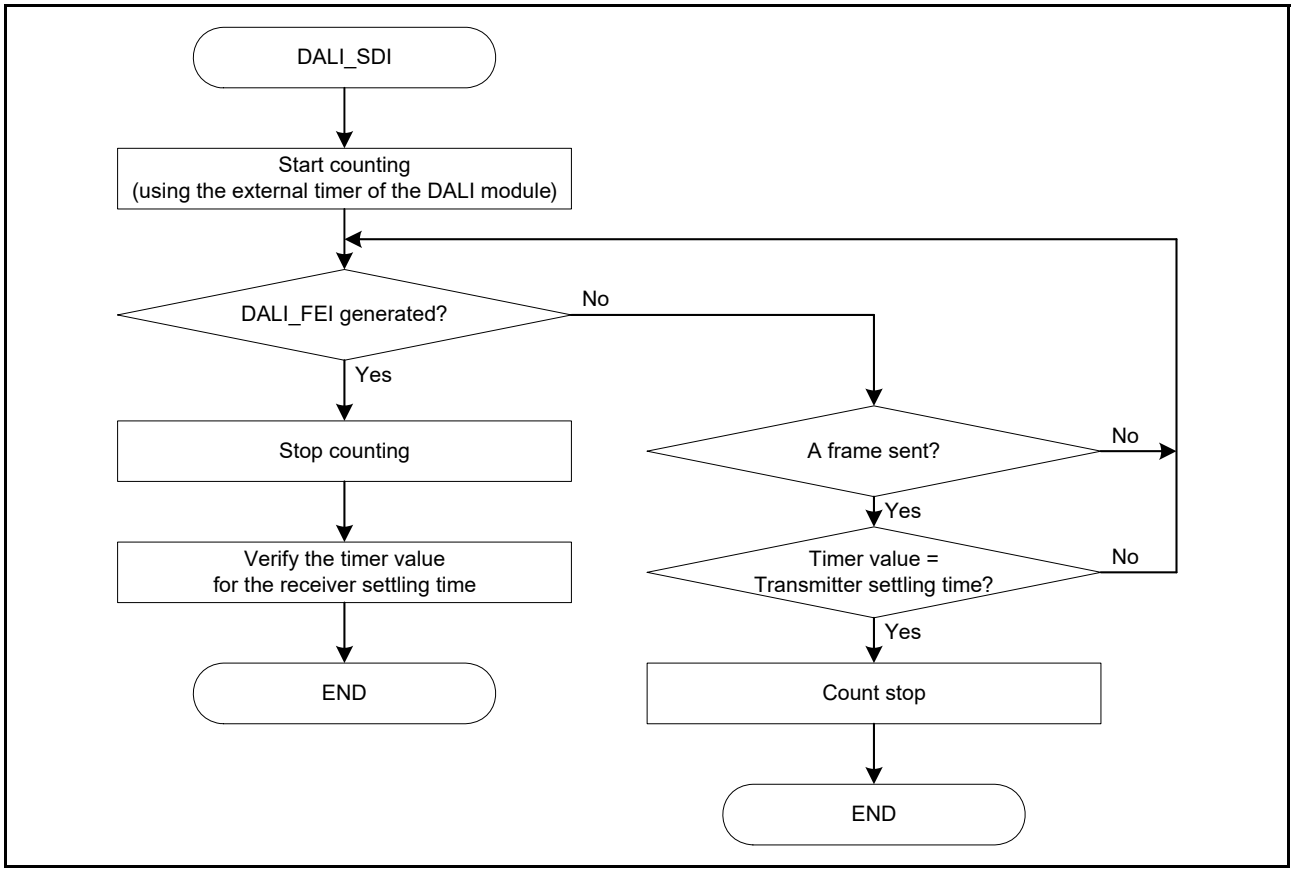


Figure 28.26 DALI_SDI and DALI_DEI operation flows (2 of 2)

28.4.5.2 DALI_CLI

See Figure 28.16 in 28.3.4.

28.4.5.3 DALI_BPI

See Figure 28.13 in 28.3.3.5.

28.5 Usage Notes

28.5.1 Module-Stop State

The Module Stop Control Register B (MSTPCRB) enables or disables DALI operation. The DALI module is stopped after a reset. The registers become accessible when the DALI module returns from the module-stop state. For details, see section 10, Low Power Modes.

28.5.2 False Recognition of Receive Data Length

When a high level of MFE continues for the period of the BTV threshold value 6 during data reception, the DALI module recognizes that a stop condition is detected but it does not detect MFE. That is, DALI_SDI is output but DALI_DEI is not output and DALI0.STR1.MFEF bit is not set. When the stop condition is defined as 3-bit length, for example, if bits [10:8] of 24-bit data is driven high, the DALI module recognizes bits [7:0] as 8-bit data, bits [10:8] as the stop condition, bit [11] as the start bit of the next frame, and bits [24:12] as data of the next frame. In this case, the bits are recognized as the second frame, and bits [24:11] are detected as invalid data by the frame size violation. However, the data that is recognized as the first frame (bits [7:0]) is determined as normal backward frame reception.

When 17-bit data (bits [16:0]) is received and the last received bit, bit [0], is MFE and fixed to high, the DALI module recognizes that the last received bit is a stop condition, so it does not detect MFE. Therefore, the data is recognized as normal reception of 16-bit data instead of error reception of 17-bit data with MFE.

If the DALI0.CTR1.RE bit is changed from 0 to 1 while another master is transmitting a frame, a data reception starts during the frame transmission. Set the DALI0.CTR1.RE bit while the DALI bus is idle. Verify the DALI0.STR1.BBF or DALI0.COLR1.RXDMON bit to determine if the DALI bus is idle.

28.5.3 Receiving more than 32 Bits Data

The maximum receive data size of the DALI module is 32 bits, but the DALI module continues the receive operation until it detects a stop condition.

When receiving a frame more than 32 bits, the DALI module sets the DALI0.STR1.O32F flag when it recognizes bit [33] of the receive data, and continues reception. Data length is counted up to the maximum value of the DALI0.STR1.RDBL[5:0] bits which is 63. However, if the stop condition cannot be detected before the counter reaches the maximum value, the counter overflows and restarts counting from 0. In this case, even if the DALI0.STR1.O32F flag is 1, the value of the DALI0.STR1.RDBL[5:0] bits is invalid. The value is not required for the receive data length.

When the stop condition cannot be detected for a long period, the DALI0.STR1.BBF flag remains 1 and no interrupt signal, such as DALI_SDI, is asserted. In this case, confirm the DALI0.STR1.O32F flag is 1, meaning it receives incorrect long data, and stop the receive operation of the DALI module by setting the DALI0.CTR1.RE bit to 0. After normal DALI bus state is restored, issue a software reset by setting the DALI0.SWRR1.SWR bit to 1 and restart the receive operation.

28.5.4 Oscillation Error and Sampling Error

In the DALI module, the operating clock is generated by dividing the frequency of PCLK. The data from the DALI bus is input synchronously with the operating clock of the DALI module. For this reason, set the bit timing violation detection threshold value and the collision detection threshold value, taking into account the PCLK oscillation error and the DALI module sampling error. The sampling error of the DALI module is 3.25 µs at a maximum.

The oscillation tolerance of the DALI module is ±1.5%.

28.5.5 Using an External Timer of the DALI Module

Some functions are achieved by using an external timer of the DALI module so that updates and changes to the DALI standard can be easily reflected. The following sections describe functions that use external timer control.

28.5.5.1 Bus power down determination

The DALI module measures a low level of the DALI bus for the period of the BTV threshold value 6 and outputs DALI_BPI. Bus power down is when a low period continues for 45 ms or more based on the DALI standard. Therefore, start the external timer of the DALI module by DALI_BPI and measure the period of {45 ms - (BTV threshold value 6)}. Check the DALI0.STR1.BPDF bit value after completion of the measurement to ensure the DALI bus is held low during the measurement. See section 28.3.3.5 for information about the bus power down operation of the DALI module.

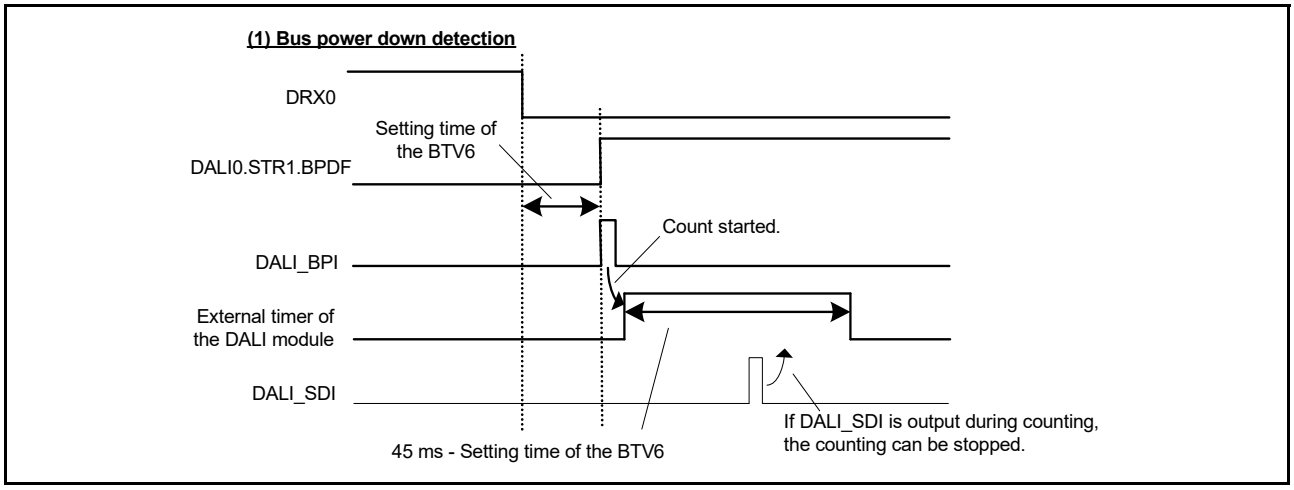


Figure 28.27 Example of bus power down detection

28.5.5.2 Measuring settling time

The settling time is defined in the DALI standard. Use DALI_SDI and DALI_FEI that the DALI module outputs to measure the settling time as specified in IEC62386-101. DALI_SDI is output when a stop condition, the time specified by DALI0.BTVTHR4.BTV6[8:0], is detected at the DRX0 pin of the DALI module. The DRX0 pin and the DALI bus are monitored even when receive operation is not performed (the DALI0.CTR1.RE bit set to 0).

DALI_FEI is output when the first falling edge is detected after the DALI bus IDLE (high level) state. The DALI module outputs DALI_FEI before it recognizes the start bit. Therefore, if the first falling edge from the DALI bus IDLE state is noise, then DALI_FEI is output, but the DALI module might not transition to the receive operation state. DALI_FEI is not used for internal operation, but is used for measuring the settling time.

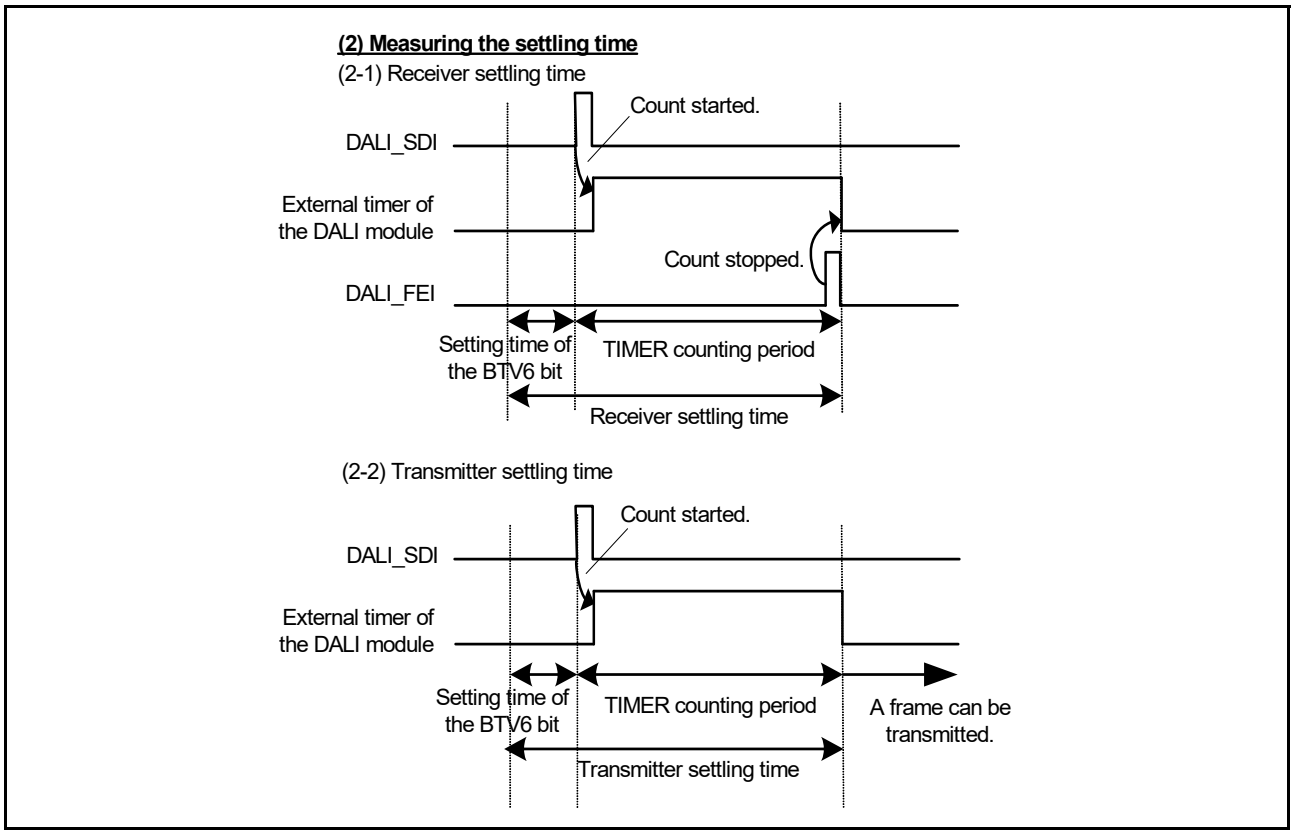


Figure 28.28 Example of measuring the settling time

28.5.5.3 Transmission control on a collision occurrence

When the DALI0.CNFR2.CDE bit is set to 1, collision detection starts. Even if a collision is detected, the DALI module continues to transmit. The DALI module must be controlled as described in section 28.3.4.

The break time, Tbreak, and recovery time, Trecover, for collision recovery, and the multi-master transmitter settling time must be measured.

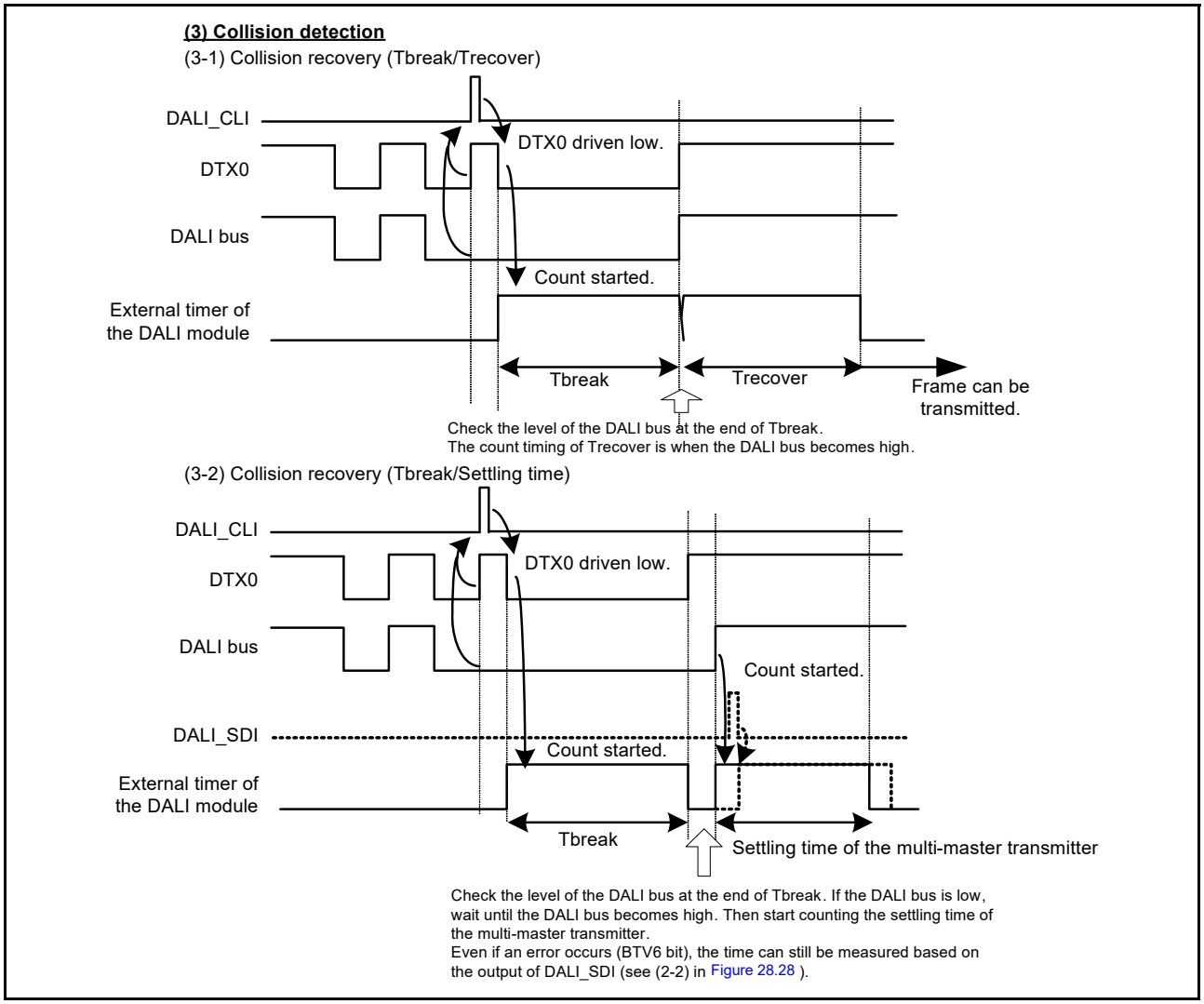


Figure 28.29 Example of collision detection

28.5.5.4 Startup operation control from Software Standby mode

In Software Standby mode, the DALI module waits for the receive operation , and PCLK is not supplied. After a falling edge is detected on the DRX0 pin, the DALI module starts the receive operation after PCLK is supplied, which is a transition to Snooze mode. However, if a falling edge on the DRX0 pin is noise, the DALI module cannot return to Software Standby mode. For this reason, if there is no interrupt (DALI_SDI or DALI_BPI) generated by the DALI module for a certain period, stop the clock supply. See section 28.5.6 for details.

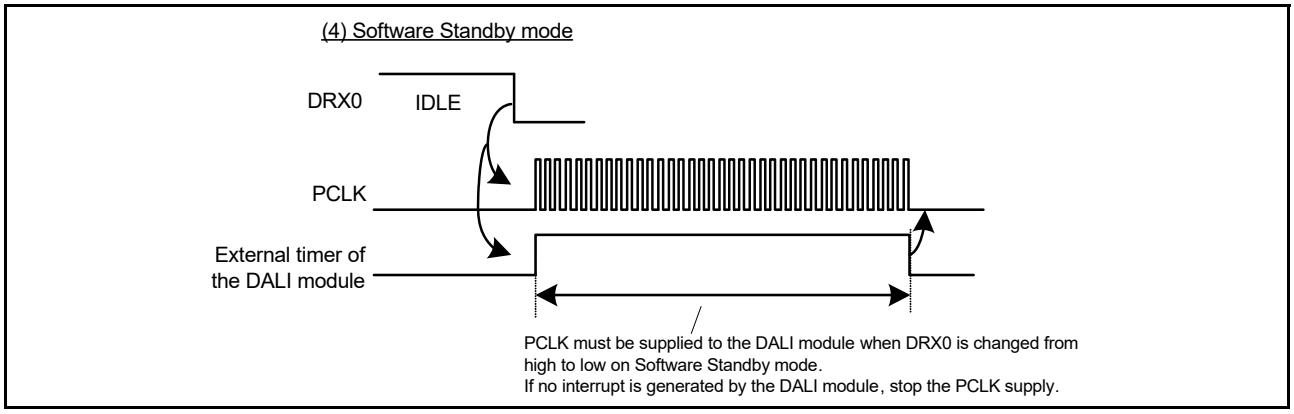


Figure 28.30 Software Standby mode

28.5.6 Startup Operation from Software Standby Mode

In Software Standby mode, PCLK is not supplied and the DALI module waits for the receive operation. The DALI module starts the receive operation after PCLK is supplied, which is a transition to Snooze mode from Software Standby mode. When a low level in the first half of the start bit period cannot be sampled at 1/4-bit timing after the reception is started, the DALI module cannot recognize the start bit and cannot receive the first frame successfully. A reception error such as MFE might occur or the DALI might remain in the reception standby state.

When the DALI module recognizes the start bit, a bit timing violation on the start bit or a collision might occur because the first half of the bit period becomes shorter as a result of the resume time to supply PCLK (transition to Snooze mode from Software Standby mode).

An external timer of the DALI module is started after the falling edge of DRX0 pin is detected. If there is no interrupt (DALI_SDI or DALI_BPI) generated by the DALI module for a certain period, stop the clock supply, which transitions to Software Standby mode. When using the DALI module in Snooze mode, some constraints, including the maximum bit rates, apply. For details on the constraints, see section 10, Low Power Modes.

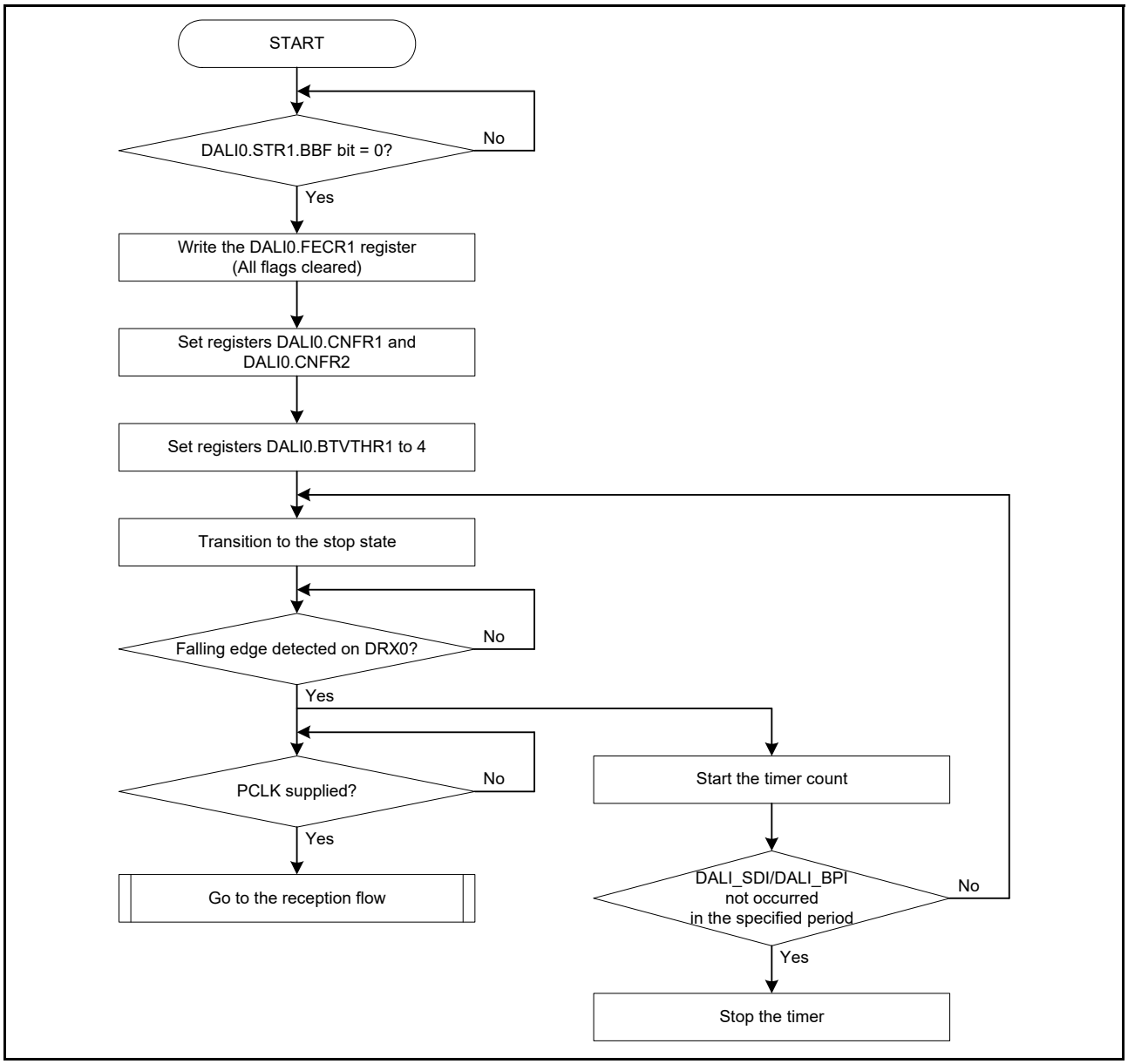


Figure 28.31 Startup flow from Software Standby mode

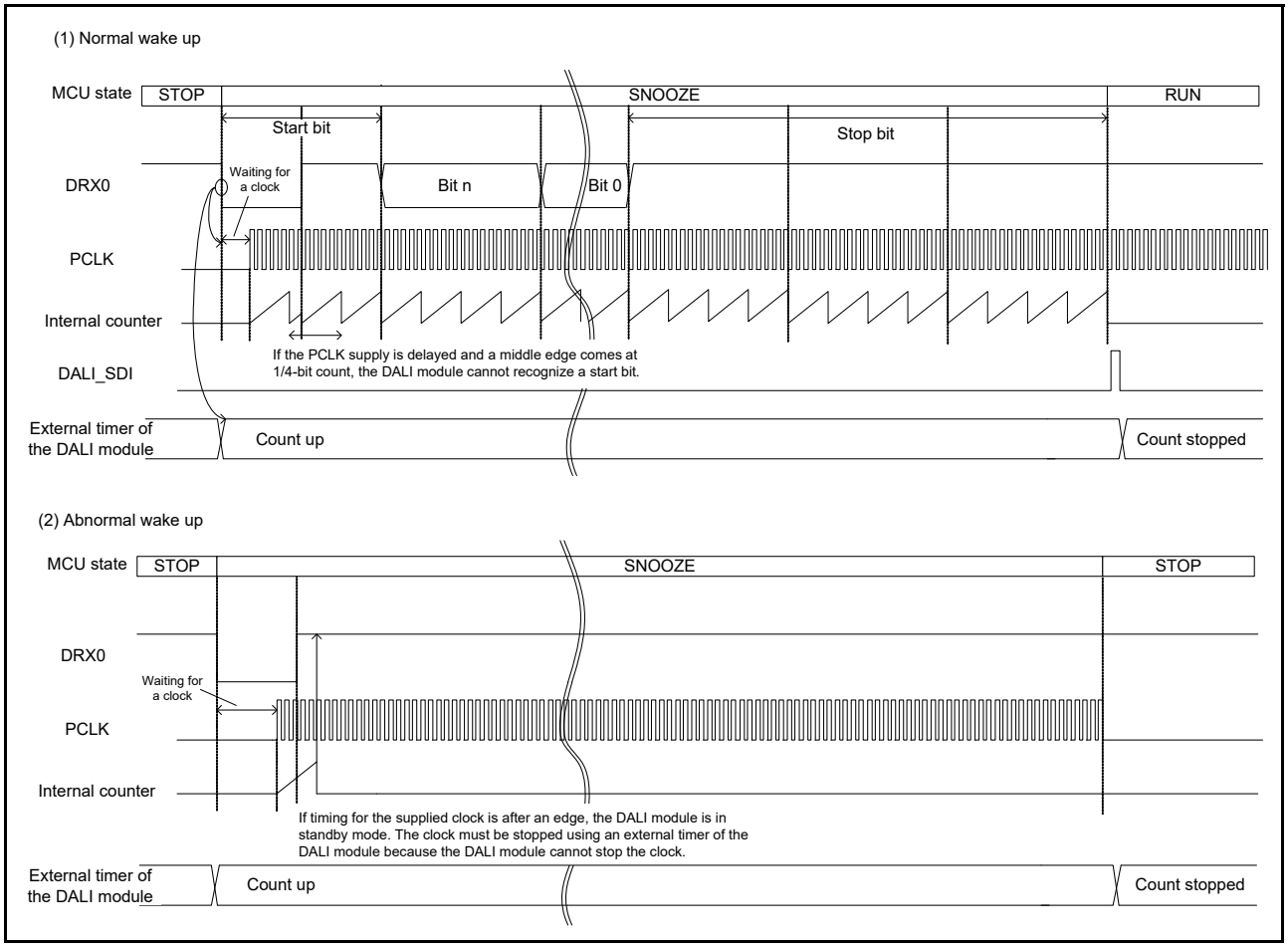


Figure 28.32 Startup from Snooze mode

28.5.7 Example of External Device Connection

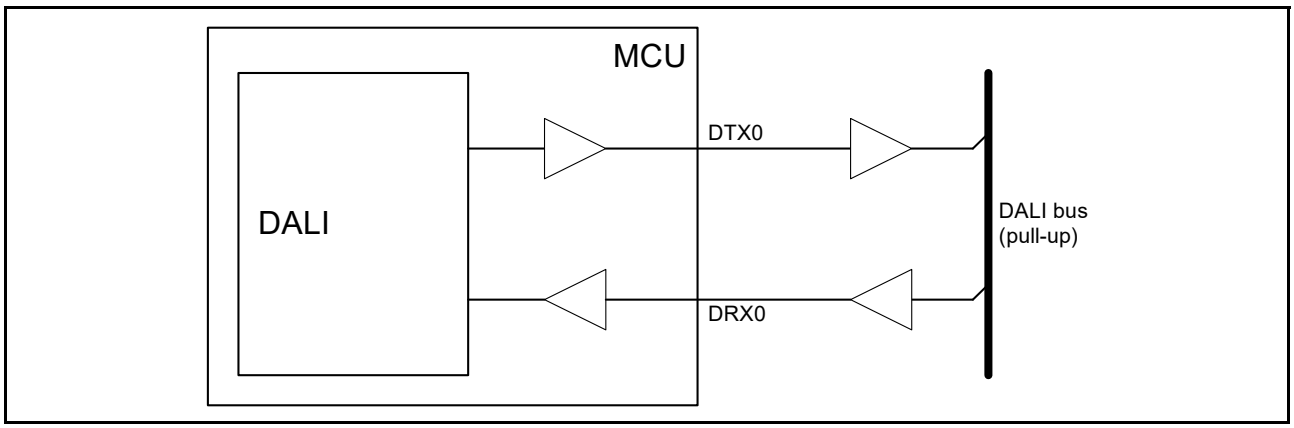


Figure 28.33 Example of external device connection

Connect pins DTX0 and DRX0 to the DALI bus as shown in Figure 28.33.

Design an external circuit to satisfy the international standard IEC 62386-101(Edition 2.0 2014-11).

29. I2C Bus Interface (IIC)

29.1 Overview

The MCU has a 2-channel I2C Bus Interface (IIC). The IIC module conforms with and provides a subset of the NXP I2C (Inter-Integrated Circuit) bus interface functions.

Table 29.1 lists the IIC specifications, Figure 29.1 shows a block diagram, and Figure 29.2 shows an example of I/O pin connections to external circuits. Table 29.2 lists the I/O pins.

Table 29.1 IIC specifications (1 of 2)

Parameter	Description
Communications format	• I2C bus or SMBus format • Master or slave mode selectable • Automatic securing of the setup times, hold times, and bus-free times for the transfer rate.
Transfer rate	Fast-mode supported up to 400 kbps
SCL clock	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%
Issuing and detecting conditions	• Start, restart, and stop conditions are automatically generated • Start conditions (including restart conditions) and stop conditions are detectable.
Slave address	• Configurable for up to three different slave addresses • 7-bit and 10-bit address formats supported, including simultaneous use • General call addresses, device ID addresses, and SMBus host addresses detectable.
Acknowledgment	• For transmission, automatic loading of the acknowledge bit Transfer of the next transmit data can be automatically suspended on detection of a not-acknowledge bit. • For reception, automatic transmission of the acknowledge bit. If a wait between the eighth and ninth clock cycles is selected, software can control the value in the acknowledge field in response to the received value.
Wait function	During reception, the following wait periods are available by holding the SCL clock low: • Waiting between the eighth and ninth clock cycles • Waiting between the ninth clock cycle and the first clock cycle of the next transfer.
SDA output delay function	Output timing of transmitted data, including the acknowledge bit, can be delayed
Arbitration	• For multi-master operation: - SCL clock synchronization is possible when conflict occurs with the SCL signal from another master - When issuing the start condition creates conflict on the bus, loss of arbitration is detected by testing for a mismatch between the internal signal for the SDA line and the level on the SDA line - In master operation, loss of arbitration is detected by testing for a mismatch between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration because the start condition occurs while the bus is busy is detectable, to prevent the issuing of double start conditions • Loss of arbitration is detectable on transfer of a not-acknowledge bit because the internal signal for the SDA line and the level on the SDA line do not match • Loss of arbitration because a mismatch of internal and line levels for data is detectable in slave transmission.
Timeout function	Internal detection of long-interval stops of the SCL clock
Noise cancellation	• Digital noise filters for both the SCL and SDA signals • Programmable window for noise cancellation by the filters.
Interrupt sources	• Transfer error or event occurrence (arbitration detection, NACK, timeout, start or restart condition, or stop condition) • Receive data full, including matching with a slave address • Transmit data empty, including matching with a slave address • Transmit end.
Module-stop function	Module-stop state can be set to reduce power consumption
IIC operating modes	• Master transmit • Master receive • Slave transmit • Slave receive.

Table 29.1 IIC specifications (2 of 2)

Parameter	Description
Event link function (output)	• Transfer error or event occurrences (arbitration detection, NACK, timeout, start or restart condition, or stop condition) • Receive data full, including matching with a slave address • Transmit data empty, including matching with a slave address • Transmit end.
Wakeup function*1	• CPU can return from Software Standby or Snooze mode using a wakeup event

Note 1. Only supported for IIC0. IIC1 is not supported.

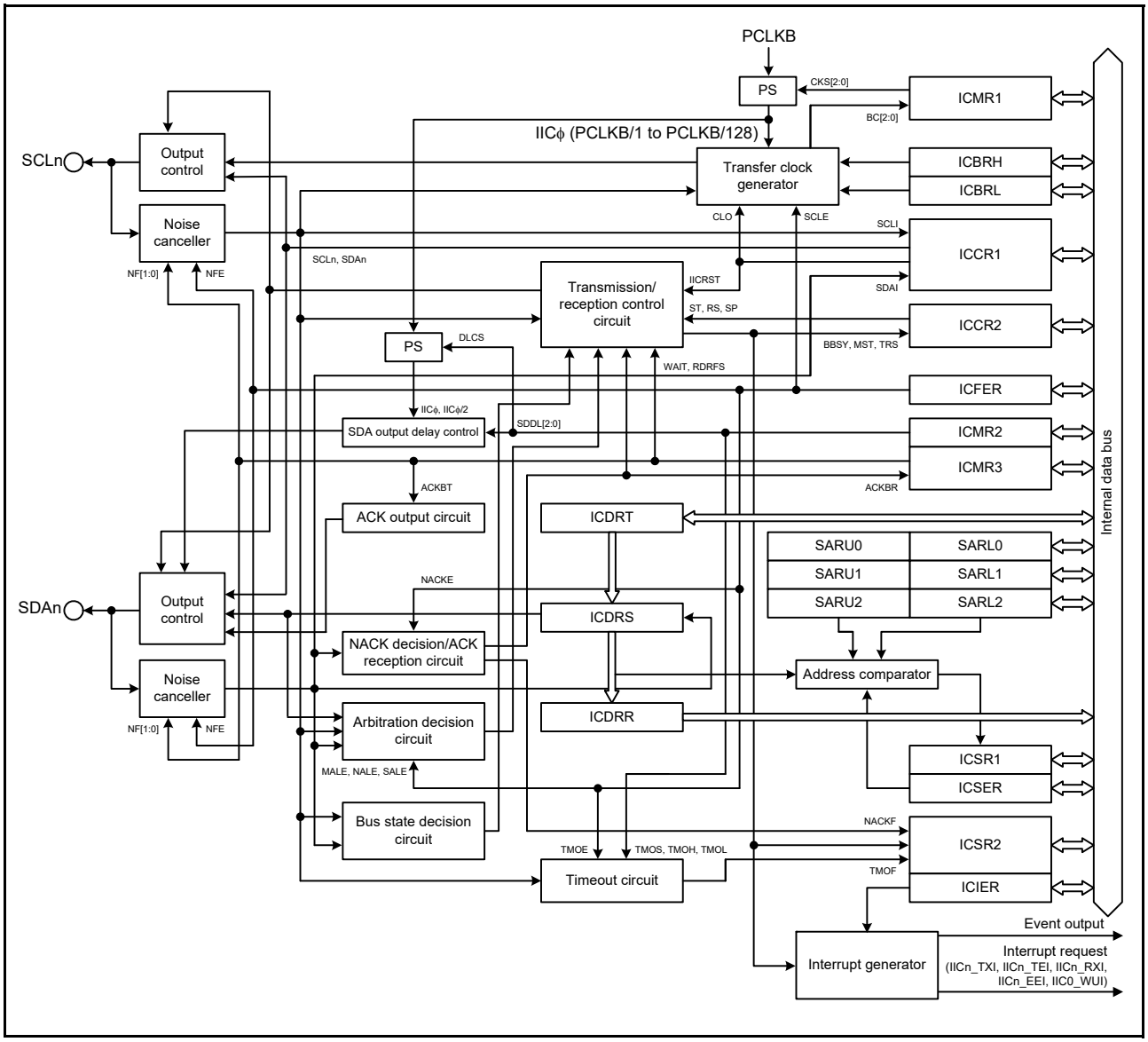


Figure 29.1 IIC block diagram

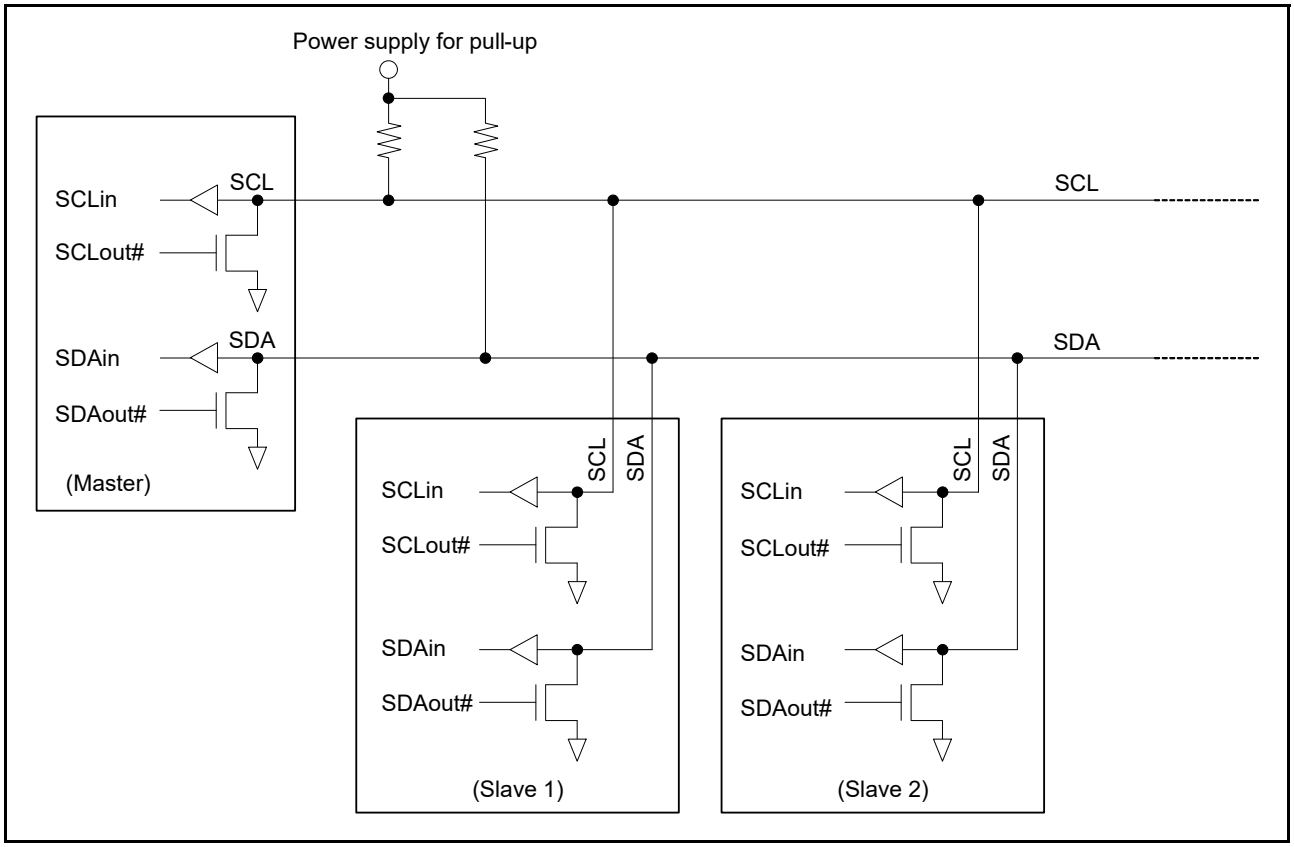


Figure 29.2 I/O pin connection to the external circuit (I2C bus configuration example)

The input level of the signals for IIC is CMOS when I2C bus is selected (ICMR3.SMBS = 0), or TTL when SMBus is selected (ICMR3.SMBS = 1).

Table 29.2 IIC pin configuration

Channel	Pin name	I/O	Function
IIC0	SCL0	I/O	IIC0 serial clock I/O pin
	SDA0	I/O	IIC0 serial data I/O pin
IIC1	SCL1	I/O	IIC1 serial clock I/O pin
	SDA1	I/O	IIC1 serial data I/O pin

29.2 Register Descriptions

29.2.1 I2C Bus Control Register 1 (ICCR1)

Address(es): IIC0.ICCR1 4005 3000h, IIC1.ICCR1 4005 3100h

	b7	b6	b5	b4	b3	b2	b1	b0
	ICE	IICRST	CLO	SOWP	SCLO	SDAO	SCLI	SDAI
Value after reset:	0	0	0	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b0	SDAI	SDA Line Monitor	0: SDAn line is low 1: SDAn line is high.	R

Bit	Symbol	Bit name	Description	R/W
b1	SCLI	SCL Line Monitor	0: SCLn line is low 1: SCLn line is high.	R
b2	SDAO	SDA Output Control/Monitor	• Read: 0: IIC drove SDAn pin low 1: IIC released SDAn pin. • Write: 0: Drive SDAn pin low through IIC 1: Release SDAn pin through IIC.	R/W
b3	SCLO	SCL Output Control/Monitor	• Read: 0: IIC drove SCLn pin low 1: IIC released SCLn pin. • Write: 0: Drive SCLn pin low through IIC 1: Release SCLn pin through IIC. Use an external pull-up resistor to drive the signal high.	R/W
b4	SOWP	SCLO/SDAO Write Protect	0: Write enable SCLO and SDAO bits 1: Write protect SCLO and SDAO bits. This bit is read as 1.	R/W
b5	CLO	Extra SCL Clock Cycle Output	0: Do not output extra SCL clock cycle (default) 1: Output extra SCL clock cycle. This bit clears automatically after one clock cycle is output.	R/W
b6	IICRST	IIC bus Interface Internal Reset	0: Release IIC reset or internal reset 1: Initiate IIC reset or internal reset. This setting clears the bit counter and the SCLn/SDAn output latch.	R/W
b7	ICE	IIC bus Interface Enable	0: Disable (SCLn and SDAn pins in inactive state) 1: Enable (SCLn and SDAn pins in active state). Combined with the IICRST bit to select either IIC or internal reset.	R/W

SDAO bit (SDA Output Control/Monitor) and SCLO bit (SCL Output Control/Monitor)

The SDAO and SCLO bits directly control the SDAn and SCLn signals output from the IIC.

When writing to these bits, also write 0 to the SOWP bit. Setting these bits results in input to the IIC by the input buffer. When slave mode is selected, a start condition might be detected and the bus might be released, depending on the bit settings.

Do not rewrite these bits during a start condition, stop condition, restart condition, or during transmission or reception. Operation after rewriting under these conditions is not guaranteed. When reading these bits, the state of signals output from the IIC can be read.

CLO bit (Extra SCL Clock Cycle Output)

The CLO bit allows output of an extra SCL clock cycle for debugging or error processing. Normally, set this bit to 0. Setting the bit to 1 in a normal communication state causes a communication error. For details on this function, see section 29.12.2, Extra SCL Clock Cycle Output Function.

IICRST bit (IIC bus Interface Internal Reset)

The IICRST bit initiates an internal state reset of the IIC. Setting this bit to 1 initiates an IIC reset or internal reset. Whether an IIC reset or internal reset is initiated is determined by the setting of this bit in combination with the ICE bit. Table 29.3 lists the IIC resets.

The IIC reset initializes all registers except ICCR1.ICE and ICCR1.IICRST bits, and internal states of the IIC. In addition to the internal states of the IIC, the internal reset initializes the following:

- Bit counter (ICMR1.BC[2:0] bits)
- I2C Bus Shift Register (ICDRS)
- I2C Bus Status Registers (ICSR1 and ICSR2)
- SDAO and SCLO Output Control/Monitor (ICCR1.SCLO and ICCR1.SDAO bits)
- I2C Bus Control Register 2 (except ICCR2.BBSY bit).

For the reset conditions for each register, see section 29.15, State of Registers When Issuing Each Condition.

An internal reset initiated with the IICRST bit set to 1 during operation (with the ICE bit set to 1) resets the internal states of the IIC without initializing the port settings and the control and setting registers of the IIC. If the IIC hangs up in a low level output state, resetting the internal states cancels the low level output state and releases the bus with the SCLn pin and SDAn pin at high impedance.

Note: If an internal reset is initiated using the IICRST bit for a bus hang-up that occurs during communication with the master device in slave mode, the slave and master devices might enter different states, because the bit counter information differs. For this reason, do not initiate an internal reset in slave mode. Initiate recovery processing from the master device. If an internal reset is necessary because the IIC hangs up with the SCLn line in a low level output state in slave mode, initiate an internal reset, then issue a restart condition from the master device, or issue a stop condition and resume communication from the start condition. If communication is restarted by initiating a reset solely in the slave device without issuing a start or restart condition from the master device, synchronization is lost because the master and slave devices operate asynchronously.

Table 29.3 IIC resets

IICRST	ICE	State	Specifications
1	0	IIC reset	Resets all registers except ICCR1.ICE and ICCR1.IICRST bits, and the internal states of the IIC
	1	Internal reset	Resets the following: • ICMR1.BC[2:0] bits • ICSR1, ICSR2, ICDRS registers • SDAO and SCLO Output Control/Monitor (ICCR1.SCLO and ICCR1.SDAO bits) • I2C Bus Control Register 2 (except ICCR2.BBSY bit) • Internal states of the IIC.

ICE bit (IIC bus Interface Enable)

The ICE bit selects the active or inactive state of the SCLn and SDAn pins. It can also be combined with the IICRST bit to initiate two types of resets. See Table 29.3 for the reset types.

Set the ICE bit to 1 when using the IIC. The SCLn and SDAn pins are placed in the active state when the ICE bit is set to 1. Set the ICE bit to 0 when the IIC is not used. The SCLn and SDAn pins are placed in the inactive state when the ICE bit is set to 0. Do not assign the SCLn or SDAn pin to the IIC when setting up the pin function control. Slave address comparison is performed if the pins are assigned to the IIC.

29.2.2 I2C Bus Control Register 2 (ICCR2)

Address(es): IIC0.ICCR2 4005 3001h, IIC1.ICCR2 4005 3101h

	b7	b6	b5	b4	b3	b2	b1	b0
	BBSY	MST	TRS	—	SP	RS	ST	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b1	ST	Start Condition Issuance Request	0: Do not issue a start condition request 1: Issue a start condition request.	R/W
b2	RS	Restart Condition Issuance Request	0: Do not issue a restart condition request 1: Issue a restart condition request.	R/W
b3	SP	Stop Condition Issuance Request	0: Do not issue a stop condition request 1: Issue a stop condition request.	R/W
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit name	Description	R/W
b5	TRS	Transmit/Receive Mode	0: Receive mode 1: Transmit mode.	R/W*1
b6	MST	Master/Slave Mode	0: Slave mode 1: Master mode.	R/W*1
b7	BBSY	Bus Busy Detection Flag	0: I2C bus released (bus free state) 1: I2C bus occupied (bus busy state).	R

Note 1. The MST and TRS bits can be written to when the ICMR1.MTWP bit is set to 1.

ST bit (Start Condition Issuance Request)

The ST bit requests transition to master mode and issues a start condition. When this bit is set to 1, a start condition is issued when the BBSY flag is set to 0 (bus free state). For details on issuing start conditions, see section 29.11, Start, Restart, and Stop Condition Issuing Function.

[Setting condition]

- When 1 is written to the ST bit.

[Clearing conditions]

- When 0 is written to the ST bit
- When a start condition is issued (a start condition is detected)
- When the AL (arbitration-lost) flag in the ICSR2 register is set to 1
- When 1 is written to the IICRST bit in the ICCR1 register to apply an IIC reset or an internal reset.

Note: Only set the ST bit to 1 (start condition request) when the BBSY flag is set to 0 (bus free state). Arbitration might be lost if the ST bit is set to 1 when the BBSY flag is 1 (bus busy state).

RS bit (Restart Condition Issuance Request)

The RS bit requests that a restart condition be issued in master mode.

When this bit is set to 1 to request a restart condition, a restart condition is issued when the BBSY flag is set to 1 (bus busy state) and the MST bit is set to 1 (master mode). For details on issuing restart conditions, see section 29.11, Start, Restart, and Stop Condition Issuing Function.

[Setting condition]

- When 1 is written to the RS bit with the BBSY flag in the ICCR2 register set to 1.

[Clearing conditions]

- When 0 is written to the RS bit
- When a restart condition is issued (a start condition is detected)
- When the AL (arbitration-lost) flag in the ICSR2 register is set to 1.
- When 1 is written to the IICRST bit in the ICCR1 register to apply an IIC reset or an internal reset.

Note: Do not set the RS bit to 1 while issuing a stop condition.
Note: If 1 (restart condition request) is written to the RS bit in slave mode, the restart condition is not issued, but the RS bit remains set to 1. If the operating mode changes to master mode without the bit being cleared, a restart condition might be issued.

SP bit (Stop Condition Issuance Request)

The SP bit requests that a stop condition be issued in master mode.

When this bit is set to 1, a stop condition is issued when the BBSY flag is set to 1 (bus busy state) and the MST bit is set to 1 (master mode). For details on issuing stop conditions, see section 29.11, Start, Restart, and Stop Condition Issuing Function.

[Setting condition]

- When 1 is written to the SP bit with both the BBSY flag and the MST bit in the ICCR2 register set to 1.

[Clearing conditions]

- When 0 is written to the SP bit
- When a stop condition is issued (a stop condition is detected)
- When the AL (arbitration-lost) flag in the ICSR2 is set to 1
- When a start condition and a restart condition are detected
- When 1 is written to the IICRST bit in the ICCR1 register to apply an IIC reset or an internal reset.

Note: Writing to the SP bit is not possible when the BBSY flag is 0 (bus free state).
Note: Do not set the SP bit to 1 when a restart condition is issued.

TRS bit (Transmit/Receive Mode)

The TRS bit indicates transmit or receive mode.

The IIC is in receive mode when the TRS bit is set to 0 and in transmit mode when the bit is set to 1. The combination of this bit and the MST bit indicates the IIC operating mode.

The value of the TRS bit automatically changes to 1 for transmit mode or 0 for receive mode when a start condition is issued or detected and the R/W# bit is set. Although writing to the TRS bit is possible when the MTWP bit in the ICMR1 register is set to 1, writing to this bit is not necessary during normal usage.

[Setting conditions]

- When a start condition is issued normally because of a start condition request (when a start condition is detected with the ST bit set to 1)
- When a restart condition is issued normally because of a restart condition request (when a restart condition is detected with the RS bit set to 1)
- When the R/W# bit appended to the slave address is set to 0 in master mode
- When the address received in slave mode matches the address enabled in the ICSER register, with the R/W# bit set to 1
- When 1 is written to the TRS bit with the MTWP bit in the ICMR1 register set to 1.

[Clearing conditions]

- When a stop condition is detected
- When the AL (arbitration-lost) flag in the ICSR2 register is set to 1
- When the R/W# bit appended to the slave address is set to 1 in master mode
- In slave mode, on a match between the received address and the address enabled in the ICSER register when the value of the received R/W# bit is 0, including when the received address is the general call address
- In slave mode, when a restart condition is detected (a restart condition is detected with ICCR2.BBSY = 1 and ICCR2.MST = 0)
- When 0 is written to the TRS bit with the MTWP bit in the ICMR1 register set to 1
- When 1 is written to the IICRST bit in the ICCR1 register to apply an IIC reset or an internal reset.

MST bit (Master/Slave Mode)

The MST bit indicates master or slave mode. The IIC is in slave mode when the MST bit is set to 0 and is in master mode when the bit is set to 1. The combination of this bit and the TRS bit indicates the operating mode of the IIC.

The value of the MST bit automatically changes to 1 for master mode or 0 for slave mode when a start condition is issued or a stop condition is issued or detected. Although writing to the MST bit is possible when the MTWP bit in the ICMR1 register is set to 1, writing to this bit is not necessary during normal usage.

[Setting conditions]

- When a start condition is issued normally because of a start condition request (when a start condition is detected with the ST bit set to 1)
- When 1 is written to the MST bit with the MTWP bit in ICMR1 set to 1.

[Clearing conditions]

- When a stop condition is detected
- When the AL (arbitration-lost) flag in the ICSR2 register is set to 1
- When 0 is written to the MST bit with the MTWP bit in the ICMR1 register set to 1
- When 1 is written to the IICRST bit in the ICCR1 register to apply an IIC reset or an internal reset.

BBSY flag (Bus Busy Detection Flag)

The BBSY flag indicates whether the I2C bus is occupied (bus busy state) or released (bus free state).

This flag is set to 1 when the SDAn line changes from high to low when the SCLn line is high, assuming that a start condition was issued. The flag is then set to 0 if the bus free time (ICBRL register setting) start condition is not detected, assuming that a stop condition was issued.

[Setting condition]

- When a start condition is detected.

[Clearing conditions]

- When the bus free time (ICBRL register setting) start condition is not detected after a stop condition detection
- When 1 is written to the IICRST bit in ICCR1 with the ICE bit in ICCR1 set to 0 (IIC reset).

29.2.3 I2C Bus Mode Register 1 (ICMR1)

Address(es): IIC0.ICMR1 4005 3002h, IIC1.ICMR1 4005 3102h

	b7	b6	b5	b4	b3	b2	b1	b0
	MTWP	CKS[2:0]			BCWP	BC[2:0]		
Value after reset:	0	0	0	0	1	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	BC[2:0]	Bit Counter	b2 b0 0 0 0: 9 bits 0 0 1: 2 bits 0 1 0: 3 bits 0 1 1: 4 bits 1 0 0: 5 bits 1 0 1: 6 bits 1 1 0: 7 bits 1 1 1: 8 bits.	R/W*1
b3	BCWP	BC Write Protect	0: Write enable BC[2:0] bits 1: Write protect BC[2:0] bits. This bit is read as 1.	R/W*1

Bit	Symbol	Bit name	Description	R/W
b6 to b4	CKS[2:0]	Internal Reference Clock Select	Select the internal reference clock source (IICϕ) for the IIC. b6 b4 0 0 0: PCLKB clock 0 0 1: PCLKB/2 clock 0 1 0: PCLKB/4 clock 0 1 1: PCLKB/8 clock 1 0 0: PCLKB/16 clock 1 0 1: PCLKB/32 clock 1 1 0: PCLKB/64 clock 1 1 1: PCLKB/128 clock.	R/W
b7	MTWP	MST/TRS Write Protect	0: Write protect MST and TRS bits in ICCR2 1: Write enable MST and TRS bits in ICCR2.	R/W

Note 1. Rewrite the BC[2:0] bits and set the BCWP bit to 0 at the same time.

BC[2:0] bits (Bit Counter)

The BC[2:0] bits function as a counter indicating the number of bits remaining to be transferred on detection of a rising edge on the SCLn line. Although the BC[2:0] bits are writable and readable, it is not normally necessary to access these bits.

To write to these bits, specify the number of bits to be transferred plus one, for an additional acknowledge bit, between transferred frames when the SCLn line is at a low level.

The value in the BC[2:0] bits returns to 000b at the end of a data transfer, including the acknowledge bit, or when a start or restart condition is detected.

29.2.4 I2C Bus Mode Register 2 (ICMR2)

Address(es): IIC0.ICMR2 4005 3003h, IIC1.ICMR2 4005 3103h

	b7	b6	b5	b4	b3	b2	b1	b0
	DLCS	SDDL[2:0]			—	TMOH	TMOL	TMOS
Value after reset:	0	0	0	0	0	1	1	0

Bit	Symbol	Bit name	Description	R/W
b0	TMOS	Timeout Detection Time Select	0: Select long mode 1: Select short mode.	R/W
b1	TMOL	Timeout L Count Control	0: Disable count when SCLn line is low 1: Enable count when SCLn line is low.	R/W
b2	TMOH	Timeout H Count Control	0: Disable count when SCLn line is high 1: Enable count when SCLn line is high.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit name	Description	R/W
b6 to b4	SDDL[2:0]	SDA Output Delay Counter	• When ICMR2.DLCS = 0 (IICϕ) b6 b4 0 0 0: No output delay 0 0 1: 1 IICϕ cycle 0 1 0: 2 IICϕ cycles 0 1 1: 3 IICϕ cycles 1 0 0: 4 IICϕ cycles 1 0 1: 5 IICϕ cycles 1 1 0: 6 IICϕ cycles 1 1 1: 7 IICϕ cycles • When ICMR2.DLCS = 1 (IICϕ/2) b6 b4 0 0 0: No output delay 0 0 1: 1 or 2 IICϕ cycles 0 1 0: 3 or 4 IICϕ cycles 0 1 1: 5 or 6 IICϕ cycles 1 0 0: 7 or 8 IICϕ cycles 1 0 1: 9 or 10 IICϕ cycles 1 1 0: 11 or 12 IICϕ cycles 1 1 1: 13 or 14 IICϕ cycles.	R/W
b7	DLCS	SDA Output Delay Clock Source Select	0: Select internal reference clock (IICϕ) as clock source for SDA output delay counter 1: Select internal reference clock divided by 2 (IICϕ/2) as clock source for SDA output delay counter.*1	R/W

Note 1. The setting DLCS = 1 (IICϕ/2) is only valid when SCL is low. When SCL is high, the DLCS = 1 setting is invalid and the clock source becomes the internal reference clock (IICϕ).

TMOS bit (Timeout Detection Time Select)

The TMOS bit selects long mode or short mode for the timeout detection time when the timeout function is enabled (ICFER.TMOE bit = 1). When this bit is set to 0, long mode is selected. When it is set to 1, short mode is selected. In long mode, the timeout detection internal counter functions as a 16 bit-counter. In short mode, the counter functions as a 14 bit-counter. While the SCLn line is in the state that enables this counter as specified in the TMOH and TMOL bits, the counter counts up in sync with the internal reference clock (IICϕ) as a count source.

For details on the timeout function, see section 29.12.1, Timeout Function.

TMOL bit (Timeout L Count Control)

The TMOL bit enables or disables up-counting on the internal counter of the timeout function when the SCLn line is held low and the timeout function is enabled (ICFER.TMOE bit = 1).

TMOH bit (Timeout H Count Control)

The TMOH bit enables or disables up-counting on the internal counter of the timeout function while the SCLn line is held high and the timeout function is enabled (ICFER.TMOE bit = 1).

SDDL[2:0] bits (SDA Output Delay Counter)

The SDDL[2:0] bits can be used to delay the SDA output. This counter works with the clock source selected in the DLCS bit. The SDDL[2:0] setting can be used for all types of SDA output, including transmission of the acknowledge bit.

Set the SDA output delay to meet the I2C bus standard for the data enable time/acknowledge enable time*1, or the SMBus standard, within [data hold time (300 ns or more + the SCL clock low-level period) - the data setup time (250 ns)]. If a value outside the standard is set, communication between devices might malfunction or falsely indicate a start or stop condition, depending on the bus state.

For details on this function, see section 29.5, SDA Output Delay Function.

Note 1. Data enable time/acknowledge enable time
3,450 ns for up to 100 kbps: Standard-mode (Sm)
900 ns for up to 400 kbps: Fast-mode (Fm)

29.2.5 I2C Bus Mode Register 3 (ICMR3)

Address(es): IIC0.ICMR3 4005 3004h, IIC1.ICMR3 4005 3104h

	b7	b6	b5	b4	b3	b2	b1	b0
	SMBS	WAIT	RDRFS	ACKWP	ACKBT	ACKBR	NF[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	NF[1:0]	Noise Filter Stage Select	b1 b0 0 0: Filter out noise of up to 1 IICϕ cycle (single-stage filter) 0 1: Filter out noise of up to 2 IICϕ cycles (2-stage filter) 1 0: Filter out noise of up to 3 IICϕ cycles (3-stage filter) 1 1: Filter out noise of up to 4 IICϕ cycles (4-stage filter).	R/W
b2	ACKBR	Receive Acknowledge	0: 0 received as the acknowledge bit (ACK reception) 1: 1 received as the acknowledge bit (NACK reception).	R
b3	ACKBT	Transmit Acknowledge	0: Send 0 as the acknowledge bit (ACK transmission) 1: Send 1 as the acknowledge bit (NACK transmission).	R/W*1
b4	ACKWP	ACKBT Write Protect	0: Write-protect ACKBT bit 1: Write-enable ACKBT bit.	R/W*1
b5	RDRFS	RDRF Flag Set Timing Select	0: Set the RDRF flag on the rising edge of the ninth SCL clock cycle The SCLn line is not held low on the falling edge of the eighth clock cycle. 1: Set the RDRF flag on the rising edge of the eighth SCL clock cycle. The SCLn line is held low on the falling edge of the eighth clock cycle. Low-hold is released by writing to ACKBT.	R/W*2
b6	WAIT	WAIT	0: No wait The period between ninth clock cycle and first clock cycle is not held low. 1: Wait The period between ninth clock cycle and first clock cycle is held low. Low-hold is released by reading ICDRR.	R/W*2
b7	SMBS	SMBus/IIC bus Select	0: I2C bus selected 1: SMBus selected.	R/W

Note 1. Write to the ACKBT bit only when the ACKWP bit is 1. If the application writes 1 to the ACKWP and ACKBT bits at the same time, the ACKBT bit is not set to 1.

Note 2. The WAIT and RDRFS bits are valid only in receive mode (invalid in transmit mode).

NF[1:0] bits (Noise Filter Stage Select)

The NF[1:0] bits select the number of stages in the digital noise filter.

For details on the digital noise filter function, see section 29.6, Digital Noise Filter Circuits.

Note: Set the noise range to be filtered within a range less than the SCLn line high-level period or low-level period. If the noise range is set to a value of [SCL clock width: high-level period or low-level period, whichever is shorter] - [1.5 internal reference clock (IICϕ) cycles + analog noise filter: 120 ns (reference values)] or more, the SCL clock is regarded as noise, which might prevent the IIC from operating normally.

ACKBR bit (Receive Acknowledge)

The ACKBR bit stores the acknowledge bit information received from the receive device in transmit mode.

[Setting condition]

- When 1 is received as the acknowledge bit with the TRS bit in the ICCR2 register set to 1.

[Clearing conditions]

- When 0 is received as the acknowledge bit with the TRS bit in the ICCR2 register set to 1
- When 1 is written to the IICRST bit in the ICCR1 register while the ICE bit in the ICCR1 register is 0 (IIC reset).

ACKBT bit (Transmit Acknowledge)

The ACKBT bit sets the acknowledge bit to be sent in receive mode.

[Setting condition]

- When 1 is written to this bit with the ACKWP bit set to 1.

[Clearing conditions]

- When 0 is written to this bit with the ACKWP bit set to 1
- When a stop condition issuance is detected (when a stop condition is detected with the SP bit in the ICCR2 register set to 1)
- When 1 is written to the IICRST bit in the ICCR1 register when the ICE bit in ICCR1 is 0 (IIC reset).

ACKWP bit (ACKBT Write Protect)

The ACKWP bit controls write enabling of the ACKBT bit.

RDRFS bit (RDRF Flag Set Timing Select)

The RDRFS bit selects the RDRF flag set timing in receive mode and also selects whether to hold the SCLn line low on the falling edge of the eighth SCL clock cycle.

When the RDRFS bit is 0, the SCLn line is not held low on the falling edge of the eighth SCL clock cycle, and the RDRF flag is set to 1 on the rising edge of the ninth SCL clock cycle.

When the RDRFS bit is 1, the RDRF flag is set to 1 on the rising edge of the eighth SCL clock cycle, and the SCLn line is held low on the falling edge of the eighth SCL clock cycle. The low-hold of the SCLn line is released by a write to the ACKBT bit.

After data is received with this setting, the SCLn line is automatically held low before the acknowledge bit is sent. This enables processing to send ACK (ACKBT = 0) or NACK (ACKBT = 1), based on the receive data.

WAIT bit (WAIT)

The WAIT bit controls whether to hold the period between the ninth SCL clock cycle and the first SCL clock cycle low until the receive data buffer (ICDRR) is completely read each time single-byte data is received in receive mode.

When the WAIT bit is 0, the receive operation is continued without holding the period between the ninth and the first SCL clock cycle low. When both the RDRFS and WAIT bits are 0, continuous receive operation is enabled with the double buffer.

When the WAIT bit is 1, the SCLn line is held low from the falling edge of the ninth clock cycle until the ICDRR value is read each time single-byte data is received. This enables receive operation in byte units.

Note: When the value of the WAIT bit is to be read, be sure to read the ICDRR register first.

SMBS bit (SMBus/IIC bus Select)

Setting this bit to 1 selects the SMBus and enables the HOAE bit in ICSER.

29.2.6 I2C Bus Function Enable Register (ICFER)

Address(es): IIC0.ICFER 4005 3005h, IIC1.ICFER 4005 3105h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	SCLE	NFE	NACKE	SALE	NALE	MALE	TMOE
Value after reset:	0	1	1	1	0	0	1	0

Bit	Symbol	Bit name	Description	R/W
b0	TMOE	Timeout Function Enable	0: Disable 1: Enable.	R/W
b1	MALE	Master Arbitration-Lost Detection Enable	0: Disable Disables the arbitration-lost detection function and disables automatic clearing of the MST and TRS bits in the ICCR2 register when arbitration is lost. 1: Enable Enables the arbitration-lost detection function and enables automatic clearing of the MST and TRS bits in the ICCR2 register when arbitration is lost.	R/W
b2	NALE	NACK Transmission Arbitration-Lost Detection Enable	0: Disable 1: Enable.	R/W
b3	SALE	Slave Arbitration-Lost Detection Enable	0: Disable 1: Enable.	R/W
b4	NACKE	NACK Reception Transfer Suspension Enable	0: Do not suspend transfer operation during NACK reception (transfer suspension disabled) 1: Suspend transfer operation during NACK reception (transfer suspension enabled).	R/W
b5	NFE	Digital Noise Filter Circuit Enable	0: Do not use digital noise filter circuit 1: Use digital noise filter circuit.	R/W
b6	SCLE	SCL Synchronous Circuit Enable	0: Do not use SCL synchronous circuit 1: Use SCL synchronous circuit.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

TMOE bit (Timeout Function Enable)

The TMOE bit enables or disables the timeout function.

For details on the timeout function, see section 29.12.1, Timeout Function.

MALE bit (Master Arbitration-Lost Detection Enable)

The MALE bit specifies whether to use the arbitration-lost detection function in master mode. Normally, set this bit to 1.

NALE bit (NACK Transmission Arbitration-Lost Detection Enable)

The NALE bit specifies whether to cause arbitration to be lost when ACK is detected during transmission of NACK in receive mode, for example when slaves with the same address exist on the bus or when two or more masters select the same slave device simultaneously with a different number of receive bytes.

SALE bit (Slave Arbitration-Lost Detection Enable)

The SALE bit specifies whether to cause arbitration to be lost when a value different from the value being transmitted is detected on the bus in slave transmit mode, for example when slaves with the same address exist on the bus or when a mismatch with the transmit data occurs because of noise.

NACKE bit (NACK Reception Transfer Suspension Enable)

The NACKE bit specifies whether to continue or discontinue the transfer operation when NACK is received in transmit mode. Normally, set this bit to 1.

When NACK is received with the NACKE bit set to 1, the next transfer operation is suspended. When the NACKE bit is

0, the next transfer operation is continued regardless of the received acknowledge content.

For details on the NACK reception transfer suspension function, see section 29.9.2, NACK Reception Transfer Suspension Function.

SCLE bit (SCL Synchronous Circuit Enable)

The SCLE bit specifies whether to synchronize the SCL clock with the SCL input clock. Normally, set this bit to 1.

When the SCLE bit is set to 0 (no SCL synchronous circuit used), the IIC does not synchronize the SCL clock with the SCL input clock. In this setting, the IIC outputs the SCL clock with the transfer rate set in ICBRH and ICBRL, regardless of the SCLn line state. For this reason, if the bus load of the I2C bus line is much larger than the specification value, or if the SCL clock output overlaps in multiple masters, a short-cycle SCL clock that does not meet the specification might be output. When no SCL synchronous circuit is used, the issuance of the start, restart, and stop conditions, and the continuous output of extra SCL clock cycles are also affected.

This bit must not be set to 0 except when checking the output of the set transfer rate.

29.2.7 I2C Bus Status Enable Register (ICSER)

Address(es): IIC0.ICSER 4005 3006h, IIC1.ICSER 4005 3106h

	b7	b6	b5	b4	b3	b2	b1	b0
	HOAE	—	DIDE	—	GCAE	SAR2E	SAR1E	SAR0E
Value after reset:	0	0	0	0	1	0	0	1

Bit	Symbol	Bit name	Description	R/W
b0	SAR0E	Slave Address Register 0 Enable	0: Disable slave address in SARL0 and SARU0 1: Enable slave address in SARL0 and SARU0.	R/W
b1	SAR1E	Slave Address Register 1 Enable	0: Disable slave address in SARL1 and SARU1 1: Enable slave address in SARL1 and SARU1.	R/W
b2	SAR2E	Slave Address Register 2 Enable	0: Disable slave address in SARL2 and SARU2 1: Enable slave address in SARL2 and SARU2.	R/W
b3	GCAE	General Call Address Enable	0: Disable general call address detection 1: Enable general call address detection.	R/W
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5	DIDE	Device-ID Address Detection Enable	0: Disable device-ID address detection 1: Enable device-ID address detection.	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	HOAE	Host Address Enable	0: Disable host address detection 1: Enable host address detection.	R/W

SARyE bit (Slave Address Register y Enable) (y = 0 to 2)

The SARyE bit enables or disables the received slave address and the slave address set in the SARLy and SARUy registers.

When this bit is set to 1, the slave address set in the SARLy and SARUy registers is enabled and is compared with the received slave address. When this bit is set to 0, the slave address set in SARLy and SARUy is disabled and is ignored even if it matches the received slave address.

GCAE bit (General Call Address Enable)

The GCAE bit specifies whether to ignore the general call address (0000 000b + 0 [W]: All 0s) when it is received.

When this bit is set to 1, if the received slave address matches the general call address, the IIC recognizes the received slave address as the general call address independently of the slave addresses set in the SARLy and SARUy registers (y = 0 to 2), and it performs the data receive operation. When this bit is set to 0, the received slave address is ignored even if it matches the general call address.

DIDE bit (Device-ID Address Detection Enable)

The DIDE bit specifies whether to recognize and execute the device-ID address when a device ID (1111 100b) is received in the first frame after a start or restart condition is detected.

When this bit is set to 1, if the received first frame matches the device ID, the IIC recognizes that the device-ID address was received. When the subsequent R/W# bit is 0 [W], the IIC recognizes the second and subsequent frames as slave addresses and continues the receive operation. When this bit is set to 0, the IIC ignores the received first frame even if it matches the device ID address and recognizes the first frame as a normal slave address.

For details on the device-ID address detection, see section 29.7.3, Device-ID Address Detection.

HOAE bit (Host Address Enable)

The HOAE bit specifies whether to ignore the received host address (0001 000b) when the SMBS bit in the ICMR3 register is 1.

When this bit is set to 1 while the SMBS bit in the ICMR3 register is 1, if the received slave address matches the host address, the IIC recognizes the received slave address as the host address independently of the slave addresses set in the SARLy and SARUy registers (y = 0 to 2) and performs the receive operation.

When the SMBS bit in ICMR3 or the HOAE bit is set to 0, the received slave address is ignored even if it matches the host address.

29.2.8 I2C Bus Interrupt Enable Register (ICIER)

Address(es): IIC0.ICIER 4005 3007h, IIC1.ICIER 4005 3107h

	b7	b6	b5	b4	b3	b2	b1	b0
	TIE	TEIE	RIE	NAKIE	SPIE	STIE	ALIE	TMOIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TMOIE	Timeout Interrupt Request Enable	0: Disable timeout interrupt (TMOIn) request 1: Enable timeout interrupt (TMOIn) request.	R/W
b1	ALIE	Arbitration-Lost Interrupt Request Enable	0: Disable arbitration-lost interrupt (ALIn) request 1: Enable arbitration-lost interrupt (ALIn) request.	R/W
b2	STIE	Start Condition Detection Interrupt Request Enable	0: Disable start condition detection interrupt (STIn) request 1: Enable start condition detection interrupt (STIn) request.	R/W
b3	SPIE	Stop Condition Detection Interrupt Request Enable	0: Disable stop condition detection interrupt (SPIn) request 1: Enable stop condition detection interrupt (SPIn) request.	R/W
b4	NAKIE	NACK Reception Interrupt Request Enable	0: Disable NACK reception interrupt (NAKIn) request 1: Enable NACK reception interrupt (NAKIn) request.	R/W
b5	RIE	Receive Data Full Interrupt Request Enable	0: Disable receive data full interrupt (IICn_RXI) request 1: Enable receive data full interrupt (IICn_RXI) request.	R/W
b6	TEIE	Transmit End Interrupt Request Enable	0: Disable transmit end interrupt (IICn_TEI) request 1: Enable transmit end interrupt (IICn_TEI) request.	R/W
b7	TIE	Transmit Data Empty Interrupt Request Enable	0: Disable transmit data empty interrupt (IICn_TXI) request 1: Enable transmit data empty interrupt (IICn_TXI) request.	R/W

TMOIE bit (Timeout Interrupt Request Enable)

The TMOIE bit enables or disables timeout interrupt (TMOIn) requests when the TMOF flag in the ICSR2 register is set to 1. To cancel a TMOI interrupt request, set the TMOF flag or the TMOIE bit to 0.

ALIE bit (Arbitration-Lost Interrupt Request Enable)

The ALIE bit enables or disables arbitration-lost interrupt (ALIn) requests when the AL flag in the ICSR2 register is 1. To cancel an ALI interrupt request, set the AL flag or the ALIE bit to 0.

STIE bit (Start Condition Detection Interrupt Request Enable)

The STIE bit enables or disables start condition detection interrupt (STIn) requests when the START flag in the ICSR2 register is 1. To cancel an STI interrupt request, set the START flag or the STIE bit to 0.

SPIE bit (Stop Condition Detection Interrupt Request Enable)

The SPIE bit enables or disables stop condition detection interrupt (SPIn) requests when the STOP flag in the ICSR2 register is 1. To cancel an SPI interrupt request, set the STOP flag or the SPIE bit to 0.

NAKIE bit (NACK Reception Interrupt Request Enable)

The NAKIE bit enables or disables NACK reception interrupt (NAKIn) requests when the NACKF flag in the ICSR2 register is 1. To cancel an NAKI interrupt request, set the NACKF flag or the NAKIE bit to 0.

RIE bit (Receive Data Full Interrupt Request Enable)

The RIE bit enables or disables receive data full interrupt (IICn_RXI) requests when the RDRF flag in the ICSR2 register is 1.

TEIE bit (Transmit End Interrupt Request Enable)

The TEIE bit enables or disables transmit end interrupt (IICn_TEI) requests when the TEND flag in the ICSR2 register is 1. To cancel an IICn_TEI interrupt request, set the TEND flag or the TEIE bit to 0.

TIE bit (Transmit Data Empty Interrupt Request Enable)

The TIE bit enables or disables transmit data empty interrupt (IICn_TXI) requests when the TDRE flag in the ICSR2 register is 1.

29.2.9 I2C Bus Status Register 1 (ICSR1)

Address(es): IIC0.ICSR1 4005 3008h, IIC1.ICSR1 4005 3108h

	b7	b6	b5	b4	b3	b2	b1	b0
	HOA	—	DID	—	GCA	AAS2	AAS1	AAS0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	AAS0	Slave Address 0 Detection Flag	0: Slave address 0 not detected 1: Slave address 0 detected.	R/(W) *1
b1	AAS1	Slave Address 1 Detection Flag	0: Slave address 1 not detected 1: Slave address 1 detected.	R/(W) *1
b2	AAS2	Slave Address 2 Detection Flag	0: Slave address 2 not detected 1: Slave address 2 detected.	R/(W) *1
b3	GCA	General Call Address Detection Flag	0: General call address not detected 1: General call address detected.	R/(W) *1
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5	DID	Device-ID Address Detection Flag	0: Device-ID command not detected 1: Device-ID command detected. This bit is set to 1 when the first frame received immediately after a start condition is detected matches a value of (device ID (1111 100b) + 0[W]).	R/(W) *1
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	HOA	Host Address Detection Flag	0: Host address not detected 1: Host address detected. This bit is set to 1 when the received slave address matches the host address (0001 000b).	R/(W) *1

Note 1. Only 0 can be written to clear the flag.

AASy flag (Slave Address y Detection Flag) (y = 0 to 2)

[Setting conditions]

For 7-bit address format (SARUy.FS = 0):

- When the received slave address matches the SVA[6:0] value in the SARLy register, with the SARyE bit in the ICSER register set to 1 (slave address y detection enabled). This flag is set to 1 on the rising edge of the ninth SCL clock cycle in the frame.

For 10-bit address format (SARUy.FS = 1):

- When the received slave address matches a value of (11110b + SVA[1:0] in SARUy), and the subsequent address matches the SARLy value with the SARyE bit in the ICSER register set to 1 (slave address y detection enabled). This flag is set to 1 on the rising edge of the ninth SCL clock cycle in the frame.

[Clearing conditions]

- When 0 is written to the AASy bit after reading AASy = 1
- When a stop condition is detected
- When 1 is written to the IICRST bit in the ICCR1 register to apply an IIC reset or an internal reset.

For 7-bit address format (SARUy.FS = 0):

- When the received slave address does not match the SVA[6:0] value in SARLy, with the SARyE bit in the ICSER register set to 1 (slave address y detection enabled). This flag is set to 0 on the rising edge of the ninth SCL clock cycle in the frame.

For 10-bit address format (SARUy.FS = 1):

- When the received slave address does not match a value of (11110b + SVA[1:0] in SARUy), with the SARyE bit in the ICSER register set to 1 (slave address y detection enabled). This flag is set to 0 on the rising edge of the ninth SCL clock cycle in the frame.
- When the received slave address matches a value of (11110b + SVA[1:0] in SARUy), and the subsequent address does not match the SARLy value with the SARyE bit in ICSER set to 1 (slave address y detection enabled). This flag is set to 0 on the rising edge of the ninth SCL clock cycle in the frame.

GCA flag (General Call Address Detection Flag)

[Setting condition]

- When the received slave address matches the general call address (0000 000b + 0 [W]), with the GCAE bit in the ICSER register set to 1 (general call address detection enabled). This flag is set to 1 on the rising edge of the ninth SCL clock cycle in the frame.

[Clearing conditions]

- When 0 is written to the GCA bit after reading GCA = 1
- When a stop condition is detected
- When the received slave address does not match the general call address (0000 000b + 0 [W]), with the GCAE bit in ICSER set to 1 (general call address detection enabled). This flag is set to 0 on the rising edge of the ninth SCL clock cycle in the frame.
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

DID flag (Device-ID Address Detection Flag)

[Setting condition]

- When the first frame received immediately after a start or restart condition is detected matches a value of (device ID (1111 100b) + 0 [W]), with the DIDE bit in ICSER set to 1 (device-ID address detection enabled). This flag is set to 1 on the rising edge of the ninth SCL clock cycle in the frame.

[Clearing conditions]

- When 0 is written to the DID bit after reading DID = 1

- When a stop condition is detected
- When the first frame received immediately after a start or restart condition is detected does not match a value of (device ID (1111 100b)), with the DIDE bit in ICSER set to 1 (device-ID address detection enabled). This flag is set to 0 on the rising edge of the ninth SCL clock cycle in the frame.
- When the first frame received immediately after a start or restart condition is detected matches a value of (device ID (1111 100b) + 0 [W]), and the second frame does not match any slave address from 0 to 2, with the DIDE bit in ICSER set to 1 (device-ID address detection enabled). This flag is set to 0 on the rising edge of the ninth SCL clock cycle in the frame.
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

HOA flag (Host Address Detection Flag)

[Setting condition]

- When the received slave address matches the host address (0001 000b), with the HOAE bit in ICSER set to 1 (host address detection enabled). This flag is set to 1 on the rising edge of the ninth SCL clock cycle in the frame.

[Clearing conditions]

- When 0 is written to the HOA bit after reading HOA = 1
- When a stop condition is detected
- When the received slave address does not match the host address (0001 000b), with the HOAE bit in ICSER set to 1 (host address detection enabled). This flag is set to 0 on the rising edge of the ninth SCL clock cycle in the frame.
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

29.2.10 I2C Bus Status Register 2 (ICSR2)

Address(es): IIC0.ICSR2 4005 3009h, IIC1.ICSR2 4005 3109h

	b7	b6	b5	b4	b3	b2	b1	b0
	TDRE	TEND	RDRF	NACKF	STOP	START	AL	TMOF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TMOF	Timeout Detection Flag	0: Timeout not detected 1: Timeout detected.	R/(W) *1
b1	AL	Arbitration-Lost Flag	0: Arbitration not lost 1: Arbitration lost.	R/(W) *1
b2	START	Start Condition Detection Flag	0: Start condition not detected 1: Start condition detected.	R/(W) *1
b3	STOP	Stop Condition Detection Flag	0: Stop condition not detected 1: Stop condition detected.	R/(W) *1
b4	NACKF	NACK Detection Flag	0: NACK not detected 1: NACK detected.	R/(W) *1
b5	RDRF	Receive Data Full Flag	0: ICDRR contains no receive data 1: ICDRR contains receive data.	R/(W) *1
b6	TEND	Transmit End Flag	0: Data being transmitted 1: Data transmit complete.	R/(W) *1
b7	TDRE	Transmit Data Empty Flag	0: ICDRT contains transmit data 1: ICDRT contains no transmit data.	R

Note 1. Only 0 can be written to clear the flag.

TMOF flag (Timeout Detection Flag)

The TMOF flag is set to 1 when the IIC detects a timeout because the SCLn line state remained unchanged for the set period.

[Setting condition]

- When the SCLn line state remains unchanged for the period specified in the ICMR2.TMOH, TMOL, and TMOS bits while the ICFER.TMOE bit is 1 (timeout function enabled) in master or in slave mode, and the received slave address matches.

[Clearing conditions]

- When 0 is written to the TMOF bit after reading TMOF = 1
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

AL flag (Arbitration-Lost Flag)

The AL flag indicates that bus mastership was lost in arbitration because of a bus conflict or some other reason when a start condition was issued or an address and data was transmitted. The IIC monitors the level on the SDAn line during transmission and, if the level on the line does not match the value of the bit being output, sets the value of the AL flag to 1 to indicate that the bus is occupied by another device.

The IIC can also set the AL flag to indicate the detection of arbitration loss during NACK transmission or during data transmission.

[Setting conditions]

When master arbitration-lost detection is enabled (ICFER.MALE = 1):

- When the internal SDA output state does not match the SDAn line level on the rising edge of the SCL clock, except for the ACK period during data transmission in master transmit mode
- When a start condition is detected while the ST bit in ICCR2 is 1 (start condition requested) or the internal SDA output state does not match the SDAn line level
- When the ST bit in ICCR2 is 1 (start condition requested), with the BBSY flag in ICCR2 set to 1.

When NACK arbitration-lost detection is enabled (ICFER.NALE = 1):

- When the internal SDA output state does not match the SDAn line level on the rising edge of the SCL clock in the ACK period during NACK transmission in receive mode.

When slave arbitration-lost detection is enabled (ICFER.SALE = 1):

- When the internal SDA output state does not match the SDAn line level on the rising edge of the SCL clock, except for the ACK period during data transmission in slave transmit mode.

[Clearing conditions]

- When 0 is written to the AL flag after reading AL = 1
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

Table 29.4 Relationship between arbitration-lost generation sources and arbitration-lost enable functions

ICFER			ICSR2		
MALE	NALE	SALE	AL	Error	Arbitration-lost generation source
1	×	×	1	Start condition issuance error	When internal SDA output state does not match SDAn line level when a start condition is detected, when the ST bit in ICCR2 is 1
					When ST in ICCR2 is set to 1 and BBSY in ICCR2 is 1
			1	Transmit data mismatch	When transmit data (including slave address) does not match the bus state in master transmit mode
×	1	×	1	NACK transmission mismatch	When ACK is detected during transmission of NACK in master or slave receive mode

Table 29.4 Relationship between arbitration-lost generation sources and arbitration-lost enable functions

ICFER			ICSR2		
MALE	NALE	SALE	AL	Error	Arbitration-lost generation source
×	×	1	1	Transmit data mismatch	When transmit data does not match the bus state in slave transmit mode

×: Don't care

START flag (Start Condition Detection Flag)

[Setting condition]

- When a start (or restart) condition is detected.

[Clearing conditions]

- When 0 is written to the START bit after reading START = 1
- When a stop condition is detected
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

STOP flag (Stop Condition Detection Flag)

[Setting condition]

- When a stop condition is detected.

[Clearing conditions]

- When 0 is written to the STOP bit after reading STOP = 1
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

NACKF flag (NACK Detection Flag)

[Setting condition]

- When acknowledge is not received (NACK received) from the receive device in transmit mode, with the NACKE bit in ICFER set to 1 (transfer suspension enabled).

[Clearing conditions]

- When 0 is written to the NACKF bit after reading NACKF = 1
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

Note: When the NACKF flag is set to 1, the IIC suspends data transmission and reception. Writing to ICDRT in transmit mode or reading from ICDRR in receive mode with the NACKF flag set to 1 does not enable data transmit or receive operation. To restart data transmission or reception, set the NACKF flag to 0.

RDRF flag (Receive Data Full Flag)

[Setting conditions]

- When receive data is transferred from ICDRS to ICDRR. This flag is set to 1 on the rising edge of the eighth or ninth SCL clock cycle (selected in the RDRFS bit in ICMR3).
- When the received slave address matches, after a start (or restart) condition is detected, with the TRS bit in ICCR2 set to 0.

[Clearing conditions]

- When 0 is written to the RDRF bit after reading RDRF = 1
- When data is read from ICDRR
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

TEND flag (Transmit End Flag)

[Setting condition]

- On the rising edge of the ninth SCL clock cycle while the TDRE flag is 1.

[Clearing conditions]

- When 0 is written to the TEND bit after reading TEND = 1
- When data is written to ICDRT
- When a stop condition is detected
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

TDRE flag (Transmit Data Empty Flag)

[Setting conditions]

- When data is transferred from ICDRT to ICDRS and ICDRT becomes empty
- When the TRS bit in ICCR2 is set to 1
- When the received slave address matches while the TRS bit is 1.

[Clearing conditions]

- When data is written to ICDRT
- When the TRS bit in ICCR2 is set to 0
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

Note: When the NACKF flag is set to 1 while the NACKE bit in ICFER is 1, the IIC suspends data transmission and reception. In this case, if the TDRE flag is 0 (next transmit data written), data is transferred to the ICDRS register and the ICDRT register becomes empty on the rising edge of the ninth clock cycle, but the TDRE flag is not set to 1.

29.2.11 I2C-Bus Wakeup Unit Register (ICWUR)

Address(es): IIC0.ICWUR 4005 3016h

	b7	b6	b5	b4	b3	b2	b1	b0
	WUE	WUIE	WUF	WUACK	—	—	—	WUAFA
Value after reset:	0	0	0	1	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	WUAFA	Wakeup Analog Filter Additional Selection	0: Do not add the wakeup analog filter 1: Add the wakeup analog filter.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	WUACK	ACK bit for Wakeup Mode	Choice of four response modes in combination with ICCR1.IICRST and WUACK. See Table 29.5.	R/W
b5	WUF	Wakeup Event Occurrence Flag	0: Slave address not matching during wakeup 1: Slave address matching during wakeup.	R/W
b6	WUIE	Wakeup Interrupt Request Enable	0: Disable wakeup interrupt request (IIC0_WUI) 1: Enable wakeup interrupt request (IIC0_WUI).	R/W
b7	WUE	Wakeup Function Enable	0: Disable wakeup function 1: Enable wakeup function.	R/W

Table 29.5 Wakeup mode

IICRST	WUACK	Operation mode	Description
0	0	Normal wakeup mode 1	ACK response on ninth SCL and SCL low hold, and after on ninth SCL
0	1	Normal wakeup mode 2	No ACK response immediately and SCL low hold between eight and ninth SCL. SCL low hold release and ACK response on ninth SCL.
1	0	Command recovery mode	ACK response on ninth SCL and no SCL low hold
1	1	EEP response mode	NACK response on ninth SCL and no SCL low hold

WUF flag (Wakeup Event Occurrence Flag)

[Setting condition]

- When PCLKB is supplied after detecting the same address (Device ID address is excluded) that is enabled by ICSER while the PCLKB asynchronous operation with the wakeup function is enabled.

[Clearing conditions]

- When 0 is written to the WUF bit after reading WUF = 1
- ICCR1.ICE = 0 and IICRST = 1.

29.2.12 I2C Bus Wakeup Unit Register 2 (ICWUR2)

Address(es): IIC0.ICWUR2 4005 3017h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	WUSYF	WUASYF	WUSEN
Value after reset:	1	1	1	1	1	1	0	1

Bit	Symbol	Bit name	Description	R/W
b0	WUSEN	Wakeup Function Synchronous Enable	0: Enable IIC asynchronous circuit 1: Enable IIC synchronous circuit.	R/W
b1	WUASYF	Wakeup Function Asynchronous Operation Status Flag	0: IIC synchronous circuit enable condition 1: IIC asynchronous circuit enable condition.	R
b2	WUSYF	Wakeup Function Synchronous Operation Status Flag	0: IIC asynchronous circuit enable condition 1: IIC synchronous circuit enable condition.	R
b7 to b3	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

WUSEN flag (Wakeup Function Synchronous Enable)

The WUSEN flag works in combination with the WUASYF flag (or WUSYF flag) when the wakeup function is enabled (ICWUR.WUE bit =1). PCLKB synchronous operation and PCLKB asynchronous operation are switched according to the combination setting.

When switching from PCLKB synchronous operation to PCLKB asynchronous operation:

- The operation is switched to PCLKB asynchronous operation when the ICCR2.BBSY flag is 0 (bus free state) if 0 is written to the WUSEN bit while the WUASYF flag is 0
- The reception (wakeup event detection) can be performed regardless of the PCLKB operation status (operating/stopped) even after the operation is switched to PCLKB asynchronous operation.

When switching from the PCLKB asynchronous operation to the PCLKB synchronous operation:

- Even if 1 is written to the WUSEN bit while the WUASYF flag is 1 (IIC asynchronous circuit enable condition), the operation is switched to PCLKB synchronous operation only when 1 is written to the WUSEN bit on a wakeup event detection. After switching to PCLKB synchronous operation, the WUASYF flag becomes 0.
- The operation is also switched to PCLKB synchronous operation when a stop condition is detected while a wakeup

event is not detected.

WUASYF flag (Wakeup Function Asynchronous Operation Status Flag)

The WUASYF flag indicates that the IIC is in PCLKB asynchronous operation when the wakeup function is enabled (ICWUR.WUE bit =1).

[Setting condition]

- When the ICCR2.BBSY flag is 0 (bus free state) while the ICWUR.WUE bit is set to 1 (wakeup function enabled) after writing 0 to the WUSEN bit (IIC asynchronous circuit enabled).

[Clearing conditions]

- When 1 is written to the WUSEN flag (IIC synchronous circuit enabled) after detecting a wakeup event while the ICWUR.WUE bit is set to 1 (wakeup function enabled)
- When a stop condition is detected while the WUSEN flag is set to 1 before detecting the wakeup event with the ICWUR.WUE bit set to 1 and the WUASY flag set to1 (IIC synchronous circuit enable condition)
- When 1 is written to the WUSEN flag while the WUASYF flag is 1 and the ICWUR.WUE bit is 1 with a wakeup event detected
- When ICCR1.ICE is 0 and IICRST is 1 (IIC reset)
- When CWUR.WUE is 0.

WUSYF flag (Wakeup Function Synchronous Operation Status Flag)

The WUSYF flag indicates that the IIC is in PCLKB synchronous operation when the wakeup function is enabled (ICWUR.WUE bit =1). This flag always has a reversed value of the WUASYF flag.

[Setting condition]

- When 1 is written to the WUSEN flag after detecting the wakeup event while the WUSYF flag is cleared to 0 and the ICWUR.WUE bit is set to 1
- When a stop condition is detected with the WUSEN flag set to 1 before detecting a wakeup event while the WUSYF flag is cleared to 0 and the ICWUR.WUE bit is set to 1
- When ICCR1.ICE is 0 and IICRST is 1 (IIC reset)
- When ICWUR.WUE is 0.

[Clearing conditions]

- When the ICCR2.BBSY flag is 0 while the ICWUR.WUE bit is set to 1 after writing 0 to the WUSEN flag.

29.2.13 Slave Address Register Ly (SARLy) (y = 0 to 2)

Address(es): IIC0.SARL0 4005 300Ah, IIC1.SARL0 4005 310Ah,
IIC0.SARL1 4005 300Ch, IIC1.SARL1 4005 310Ch,
IIC0.SARL2 4005 300Eh, IIC1.SARL2 4005 310Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	SVA[6:0]							SVA0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SVA0	10-Bit Address LSB	Slave address setting	R/W
b7 to b1	SVA[6:0]	7-Bit Address/10-Bit Address Lower Bits	Slave address setting	R/W

SVA0 bit (10-Bit Address LSB)

When the 10-bit address format is selected (SARUy.FS = 1), the SVA0 bit functions as the LSB of a 10-bit address and combines with the SVA[6:0] bits to form the lower 8 bits of a 10-bit address.

When the SARyE bit in ICSER is set to 1 (SARLy and SARUy enabled) and the SARUy.FS bit is 1, this bit is valid. When the SARUy.FS bit or SARyE bit is 0, the setting of this bit is ignored.

SVA[6:0] bits (7-Bit Address/10-Bit Address Lower Bits)

When the 7-bit address format is selected (SARUy.FS = 0), the SVA[6:0] bits function as a 7-bit address. When the 10-bit address format is selected (SARUy.FS = 1), these bits combine with the SVA0 bit to form the lower 8 bits of a 10-bit address.

When the SARyE bit in ICSER is 0, the setting in these bits is ignored.

29.2.14 Slave Address Register Uy (SARUy) (y = 0 to 2)

Address(es): IIC0.SARU0 4005 300Bh, IIC1.SARU0 4005 310Bh, IIC0.SARU1 4005 300Dh, IIC1.SARU1 4005 310Dh, IIC0.SARU2 4005 300Fh, IIC1.SARU2 4005 310Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SVA[1:0]		FS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	FS	7-Bit/10-Bit Address Format Select	0: Select 7-bit address format 1: Select 10-bit address format.	R/W
b2, b1	SVA[1:0]	10-Bit Address Upper Bits	Slave address setting	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

FS bit (7-Bit/10-Bit Address Format Select)

The FS bit selects the 7-bit or 10-bit format for slave address y in SARLy and SARUy.

When the SARyE bit in ICSER is set to 1 (SARLy and SARUy enabled) and the SARUy.FS bit is 0, the 7-bit address format is selected for slave address y, the SVA[6:0] setting in SARLy is valid, and the SVA[1:0] bits and the SVA0 bit in the SARLy register are ignored.

When the SARyE bit in ICSER is set to 1 (SARLy and SARUy enabled) and the SARUy.FS bit is 1, the 10-bit address format is selected for slave address y, and the SVA[1:0] bits and the SARLy register are valid.

When the SARyE bit in ICSER is 0 (SARLy and SARUy disabled), the SARUy.FS bit is invalid.

SVA[1:0] bits (10-Bit Address Upper Bits)

When the 10-bit address format is selected (FS = 1), the SVA[1:0] bits function as the upper 2 bits of a 10-bit address. When the SARyE bit in ICSER is set to 1 (SARLy and SARUy enabled) and the SARUy.FS bit is 1, these bits are valid. While the SARUy.FS or SARyE bit is 0, the setting in these bits is ignored.

29.2.15 I2C Bus Bit Rate Low-Level Register (ICBRL)

Address(es): IIC0.ICBRL 4005 3010h, IIC1.ICBRL 4005 3110h

	b7	b6	b5	b4	b3	b2	b1	b0
	—		—	BRL[4:0]				
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b4 to b0	BRL[4:0]	Bit Rate Low-Level Period	Low-level period of SCL clock	R/W
b7 to b5	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

BRL[4:0] bits (Bit Rate Low-Level Period)

The BRL[4:0] bits set the low-level period of SCL clock. The IIC counts the low-level period with the internal reference clock source (IICφ) specified by the CKS[2:0] bits in ICMR1. The IIC also generates the data setup time for automatic SCL low-hold operation, see section 29.9, Automatic Low-Hold Function for SCL. When the IIC is used in slave mode, the BRL[4:0] bits must be set to a value longer than the data setup time*1. If the digital noise filter is enabled (NFE bit in ICFER is 1), set these bits to a value at least 1 greater than the number of stages in the noise filter. See the description of the ICMR3.NF[1:0] bits for details on the number of stages.

Note 1. Data setup time (tSU: DAT)
250 ns for up to 100 kbps: Standard-mode (Sm)
100 ns for up to 400 kbps: Fast-mode (Fm)

29.2.16 I2C Bus Bit Rate High-Level Register (ICBRH)

Address(es): IIC0.ICBRH 4005 3011h, IIC1.ICBRH 4005 3111h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	BRH[4:0]				
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b4 to b0	BRH[4:0]	Bit Rate High-Level Period	High-level period of SCL clock	R/W
b7 to b5	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

BRH[4:0] bits (Bit Rate High-Level Period)

The BRH[4:0] bits set the high-level period of SCL clock. BRH[4:0] bits are valid in master mode. If the IIC is used only in slave mode, do not set the BRH[4:0] bits.

The IIC counts the high-level period with the internal reference clock source (IICϕ) specified in the CKS[2:0] bits in ICMR1. If the digital noise filter is enabled (the NFE bit in ICFER is 1), set these bits to a value at least 1 greater than the number of stages in the noise filter. See the description of the ICMR3.NF[1:0] bits for more details on the number of stages.

The IIC transfer rate and the SCL clock duty are calculated using the following expression:

1) ICFER.SCLE = 0
Transfer rate = 1/{[(BRH + 1) + (BRL + 1)]/IICφ*1 + tr*2 + tf*2}
Duty cycle = {tr + [(BRH + 1)/IICφ]}/{tr + tf + [(BRH + 1) + (BRL + 1)]/IICφ}

2) ICFER.SCLE = 1 and ICFER.NFE = 0 and CKS[2:0] = 000b (IICφ = PCLKB)
Transfer rate = 1/{[(BRH + 3) + (BRL+ 3)]/IICφ + tr + tf}
Duty cycle = {tr + [(BRH + 3)/IICφ]}/{tr + tf + [(BRH + 3) + (BRL + 3)]/IICφ}

3) ICFER.SCLE = 1 and ICFER.NFE = 1 and CKS[2:0] = 000b (IICφ = PCLKB)
Transfer rate = 1/{[(BRH + 3 + nf*3) + (BRL + 3 + nf)]/IICφ + tr + tf}
Duty cycle = {tr + [(BRH + 3 + nf)/IICφ]}/{tr + tf + [(BRH + 3 + nf) + (BRL + 3 + nf)]/IICφ}

4) ICFER.SCLE = 1 and ICFER.NFE = 0 and CKS[2:0] ≠ 000b
Transfer rate = 1/{[(BRH + 2) + (BRL + 2)]/IICφ + tr + tf}
Duty cycle = {tr + [(BRH + 2)/IICφ]}/{tr + tf + [(BRH + 2) + (BRL + 2)]/IICφ}

5) ICFER.SCLE = 1 and ICFER.NFE = 1 and CKS[2:0] ≠ 000b
Transfer rate = 1/{[(BRH + 2 + nf) + (BRL + 2 + nf)]/IICφ + tr + tf}
Duty cycle = {tr + [(BRH + 2 + nf)/IICφ]}/{tr + tf + [(BRH + 2 + nf) + (BRL + 2 + nf)]/IICφ}

Note 1. IICφ = PCLKB × Division ratio
Note 2. The SCLn line rise time [tr] and SCLn line fall time [tf] depend on the total bus line capacitance [Cb] and the pull-

up resistor [Rp]. For details, see the I2C bus standard from NXP Semiconductors.

Note 3. nf = Number of digital noise filters selected in the ICMR3.NF bit.

Table 29.6 Example of ICBRH/ICBRL settings for transfer rate when SCLE = 0

Transfer rate (kbps)	CKS[2:0]	BRH[4:0]	BRL[4:0]	PCLKB[MHz]	NF[1:0]	Computation expression
100	011	15 (EFh)	18 (F2h)	32	—	1)
400	001	9 (E9h)	20 (F4h)	32	—	1)

Note: SCLn line rising time (tr): 100 kbps or less, [Sm]: 1000 ns, 400 kbps or less, [Fm]: 300 ns.
SCLn line falling time (tf): 400 kbps or less, [Sm/Fm]: 300 ns.

Table 29.7 Example of ICBRH/ICBRL settings for transfer rate when SCLE = 1 and NFE = 0

Transfer rate (kbps)	CKS[2:0]	BRH	BRL	PCLKB[MHz]	NF[1:0]	Computation expression
100	011	14 (EEh)	17 (F1h)	32	—	4)
400	001	8 (E8h)	19 (F3h)	32	—	4)

Note: SCLn line rising time (tr): ≤100 kbps; Sm: 1000 ns, ≤ 400 kbps; Fm: 300 ns, ≤ 1 Mbps; Fm+: 120 ns
SCLn line falling time (tf): ≤ 400 kbps; Sm/Fm: 300 ns, ≤ 1 Mbps; Fm+: 120 ns

Table 29.8 Example of ICBRH/ICBRL settings for transfer rate when SCLE = 1 and NFE = 1

Transfer rate (kbps)	CKS[2:0]	BRH	BRL	PCLKB[MHz]	NF[1:0]	Computation expression
100	011	12 (ECh)	15 (EFh)	32	01b	5)
400	001	6 (E6h)	17 (F1h)	32	01b	5)

Note: SCLn line rising time (tr): ≤100 kbps; Sm: 1000 ns, ≤ 400 kbps; Fm: 300 ns.
SCLn line falling time (tf): ≤ 400 kbps; Sm/Fm: 300 ns, ≤ 1 Mbps.

29.2.17 I2C Bus Transmit Data Register (ICDRT)

Address(es): IIC0.ICDRT 4005 3012h, IIC1.ICDRT 4005 3112h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

When ICDRT detects a space in the I2C-Bus Shift Register (ICDRS), it transfers the transmit data that was written to ICDRT to ICDRS and starts transmitting data in transmit mode. The double-buffer structure of ICDRT and ICDRS allows continuous transmit operation if the next transmit data is written to ICDRT while the ICDRS data is being transmitted.

ICDRT can always be read and written to. Write transmit data to ICDRT once when a transmit data empty interrupt (IICn_TXI) request is generated.

29.2.18 I2C Bus Receive Data Register (ICDRR)

Address(es): IIC0.ICDRR 4005 3013h, IIC1.ICDRR 4005 3113h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0

When 1 byte of data is received, the received data is transferred from the I2C-Bus Shift Register (ICDRS) to ICDRR to enable the next data to be received. The double-buffer structure of ICDRS and ICDRR allows continuous receive operation if the received data is read from ICDRR while ICDRS is receiving data. ICDRR cannot be written to. Read data from ICDRR once when a receive data full interrupt (IICn_RXI) request is generated.

If ICDRR receives the next receive data before the current data is read from ICDRR (while the RDRF flag in ICSR2 is 1), the IIC automatically holds the SCL low for 1 clock cycle before the RDRF flag is set to 1 next.

29.2.19 I2C-Bus Shift Register (ICDRS)

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	—	—	—	—	—	—	—	—

ICDRS is an 8-bit shift register for data transmit and receive. During transmission, transmit data is transferred from ICDRT to ICDRS and is sent from the SDAn pin. During reception, data is transferred from ICDRS to ICDRR after 1 byte of data is received. ICDRS cannot be accessed directly.

29.3 Operation

29.3.1 Communication Data Format

The I2C bus format consists of 8-bit data and 1-bit acknowledge. The frame following a start or restart condition is an address frame that specifies a slave device with which the master device communicates. The specified slave is valid until a new slave is specified or a stop condition is issued.

Figure 29.3 shows the I2C bus format, and Figure 29.4 shows the I2C bus timing.

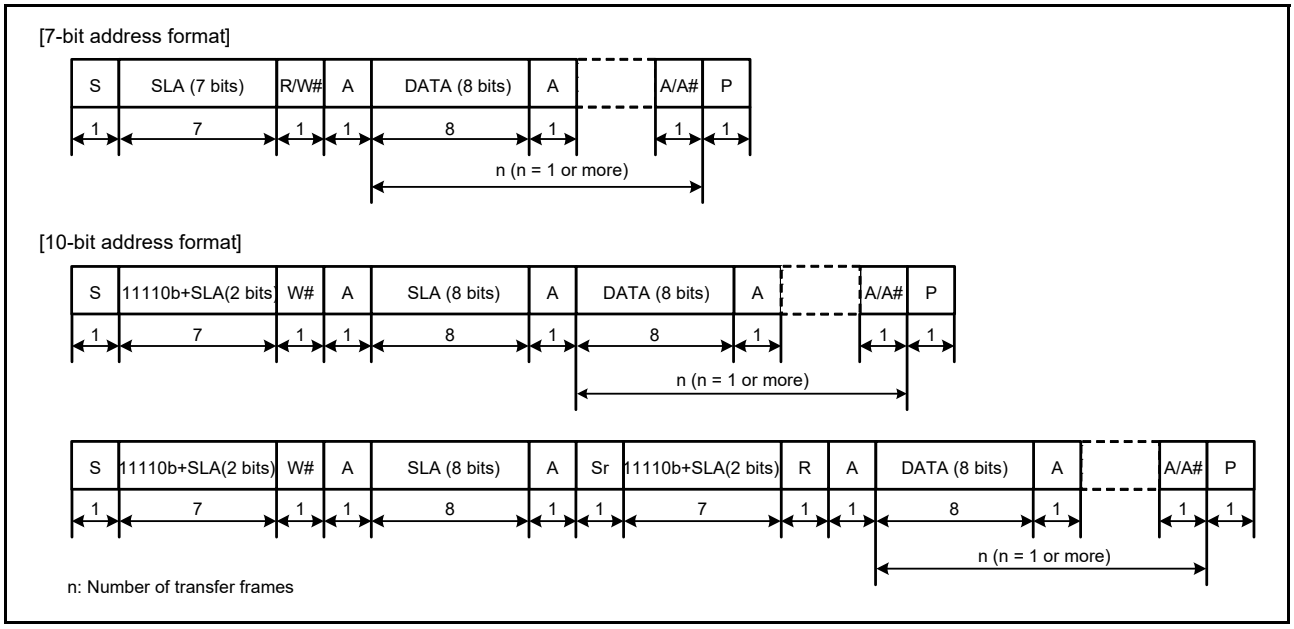


Figure 29.3 I2C bus format

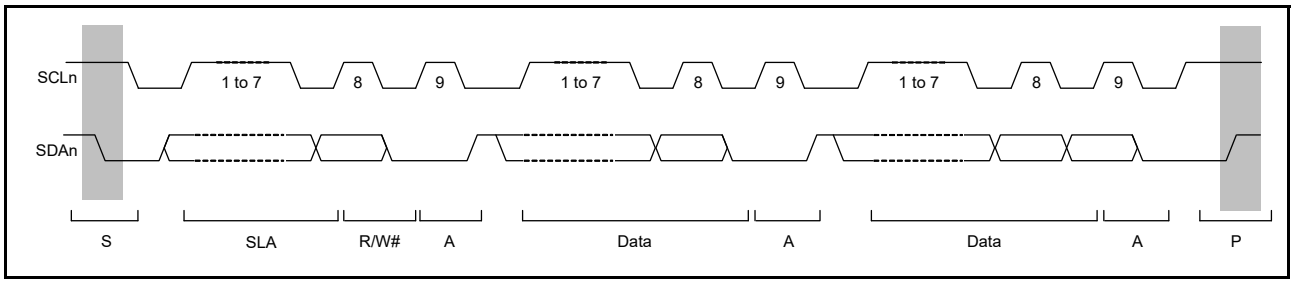


Figure 29.4 I2C bus timing (SLA = 7 bits)

S: Start condition. The master device drives the SDAn line low from high while the SCLn line is high.

SLA: Slave address, by which the master device selects a slave device.

R/W#: Indicates the direction of data transfer: from the slave device to the master device when R/W# is 1, or from the master device to the slave device when R/W# is 0.

A: Acknowledge. The receive device drives the SDAn line low. (In master transmit mode, the slave device returns acknowledge. In master receive mode, the master device returns acknowledge.)

A#: Not Acknowledge. The receive device drives the SDAn line high.

Sr: Restart condition. The master device drives the SDAn line low from the high level after the setup time has elapsed with the SCLn line high.

DATA: Transmitted or received data.

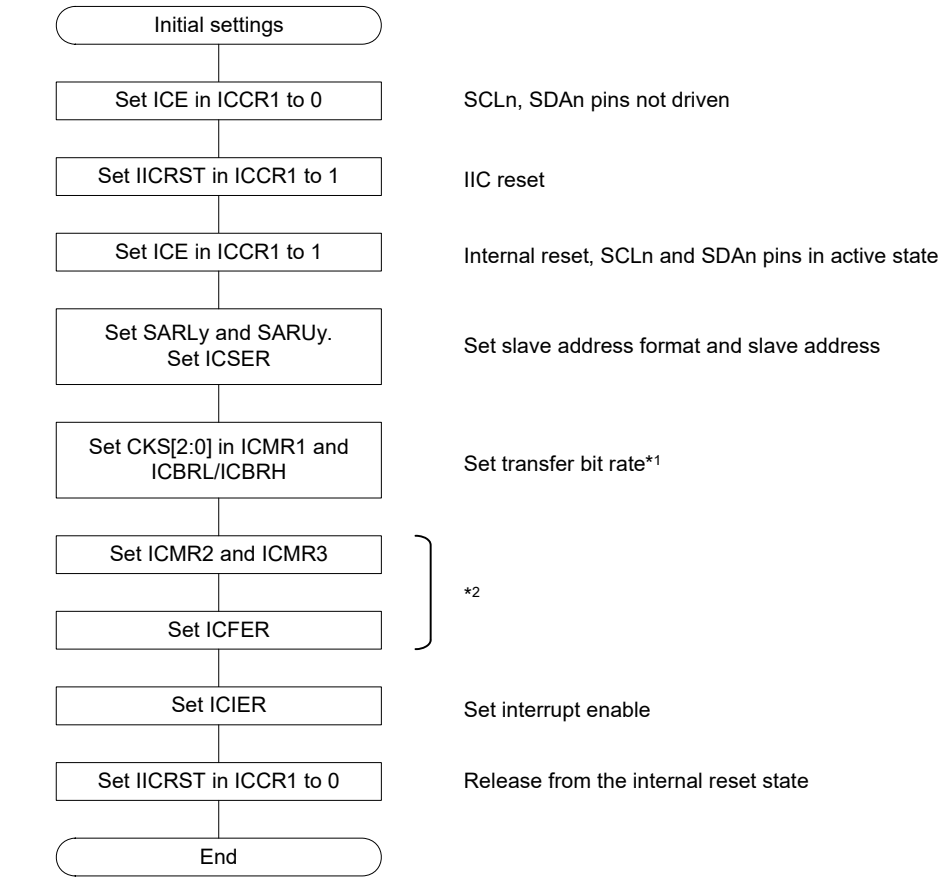
P: Stop condition. The master device drives the SDAn line high from low when the SCLn line is high.

29.3.2 Initial Settings

Before starting data transmission or reception, initialize the IIC according to the procedure shown in Figure 29.5.

1. Set the ICCR1.ICE bit to 0 to set the SCLn and SDAn pins to the inactive state.
2. Set the ICCR1.IICRST bit to 1 to initiate IIC reset.
3. Set the ICCR1.ICE bit to 1 to initiate internal reset.
4. Set the SARLy, SARUy, ICSER, ICMR1, ICBRH, and ICBRL registers (y = 0 to 2), and set the other registers as necessary. For initial settings of the IIC, see Figure 29.5.
5. When the necessary register settings are complete, set the ICCR1.IICRST bit to 0 to release the IIC reset.

Note: This procedure is not necessary if initialization of the IIC is already complete.



y = 0 to 2

Note 1. When the IIC is used only in slave mode, set the ICBRL register to a value longer than the data setup time.

Note 2. Set these registers as required.

Figure 29.5 Example IIC initialization flow

29.3.3 Master Transmit Operation

In a master transmit operation, the IIC outputs the SCL clock and transmitted data signals as the master device, and the slave device returns acknowledgments. Figure 29.6 shows an example of master transmission, and Figure 29.7 to Figure 29.9 show the operation timing in master transmission.

To set up and perform master transmission:

1. Initial settings. For details, see section 29.3.2, Initial Settings.
2. Read the BBSY flag in ICCR2 to check that the bus is open, then set the ST bit in ICCR2 to 1 (start condition request). On receiving the request, the IIC issues a start condition. At the same time, the BBSY flag and the START flag in ICSR2 automatically set to 1, and the ST bit is automatically set to 0. At this time, if the start condition is detected and the internal levels for the SDA output state and the levels on the SDAn line match while the ST bit is 1, the IIC recognizes that the start condition requested by the ST bit has successfully complete, and the MST and TRS bits in ICCR2 automatically set to 1, placing the IIC in master transmit mode. The TDRE flag in ICSR2 is also automatically set to 1 in response to the TRS bit = 1.
3. Check that the TDRE flag in ICSR2 is 1, then write the value for transmission (the slave address and the R/W# bit) to ICDRT. When the transmit data is written to ICDRT, the TDRE flag is automatically set to 0, the data is transferred from ICDRT to ICDRS, and the TDRE flag is again set to 1. After the byte containing the slave address and R/W# bit is transmitted, the value of the TRS bit automatically updates to select master transmit or master

receive mode according to the value of the transmitted R/W# bit. If the value of the R/W# bit is 0, the IIC continues in master transmit mode. If the ICSR2.NACKF flag is 1, indicating that no slave device recognizes the address or there was an error in communications, write 1 to the ICCR2.SP bit to issue a stop condition.
For data transmission with an address in the 10-bit format, start by writing 1111 0b, the 2 upper-order bits of the slave address, and W to ICDRT as the first address transmission. For the second address transmission, write the 8 lower-order bits of the slave address to ICDRT.

4. Check that the TDRE flag in ICSR2 is 1, then write the transmit data to the ICDRT register. The IIC automatically holds the SCLn line low until the transmit data is ready or a stop condition is issued.
5. After all bytes of transmit data are written to the ICDRT register, wait until the value in the TEND flag in ICSR2 returns to 1, then set the SP bit in ICCR2 to 1 (stop condition requested). On receiving a stop condition request, the IIC issues the stop condition. For information on issuing a stop condition, see section 29.11.3, Issuing a Stop Condition.
6. On detecting the stop condition, the IIC automatically sets the MST and TRS bits in ICCR2 to 00b and enters slave receive mode. Additionally, it automatically sets the TDRE and TEND flags to 0, and sets the STOP flag in ICSR2 to 1.
7. Check that the ICSR2.STOP flag is 1, then set the ICSR2.NACKF and STOP flags to 0 for the next transfer operation.

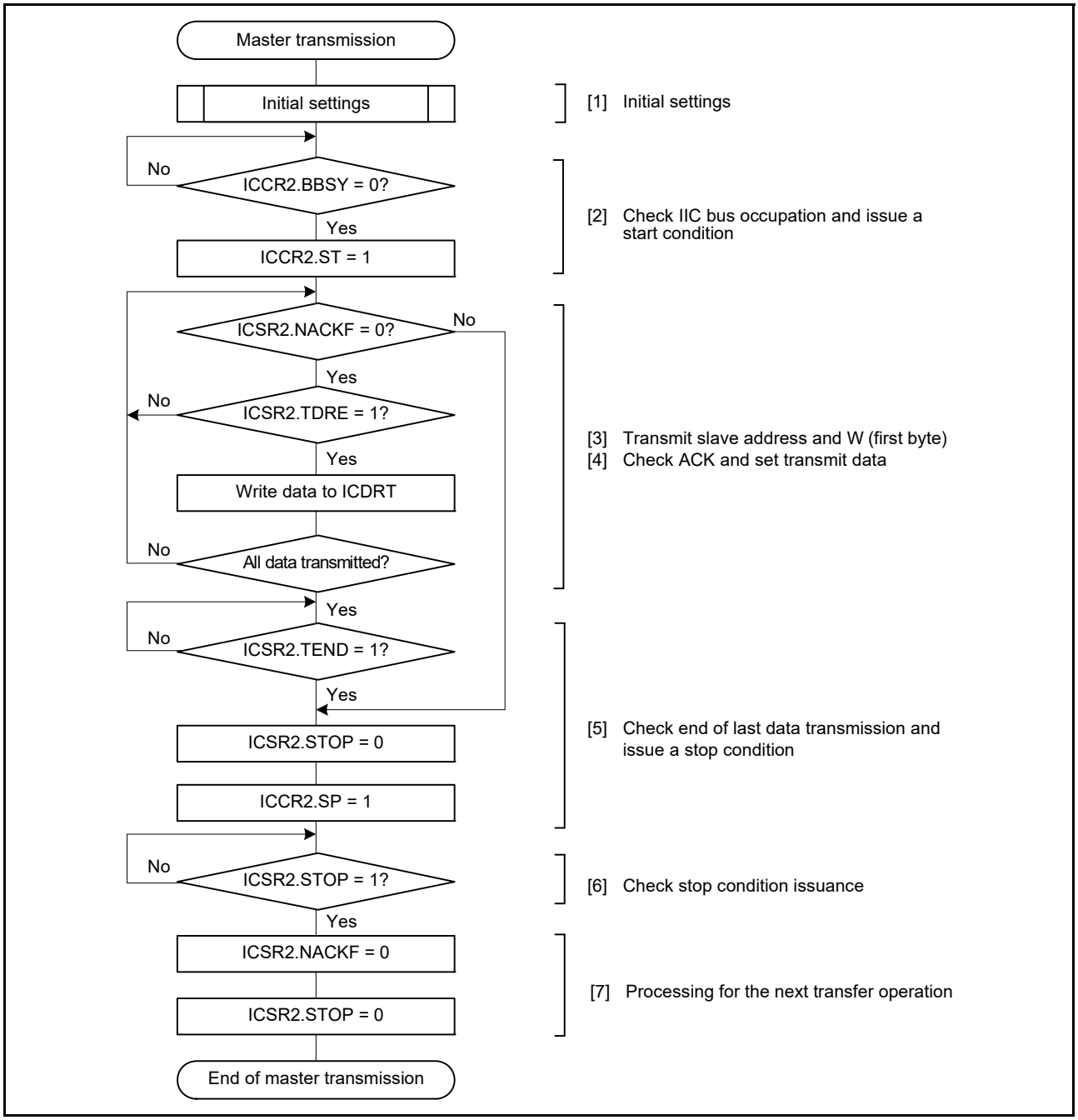


Figure 29.6 Example master transmission flow

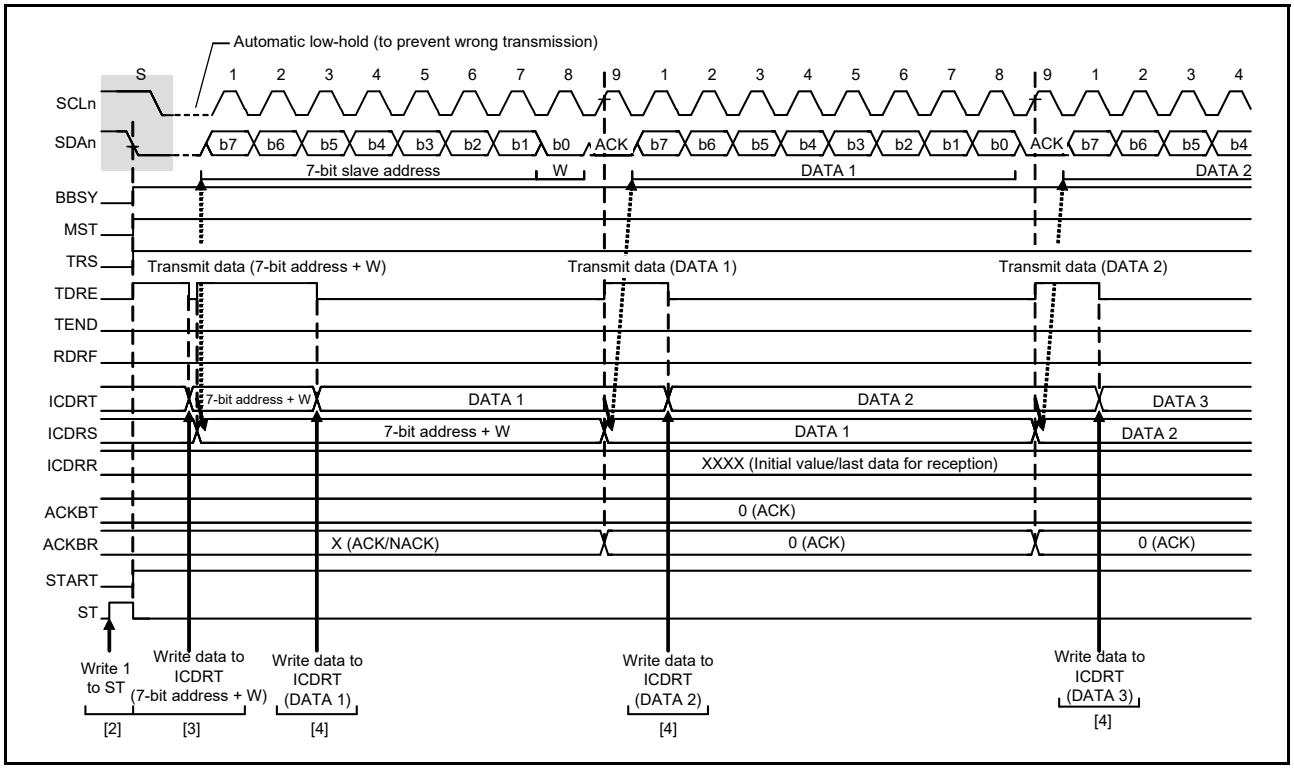


Figure 29.7 Master transmit operation timing (1) (7-bit address format)

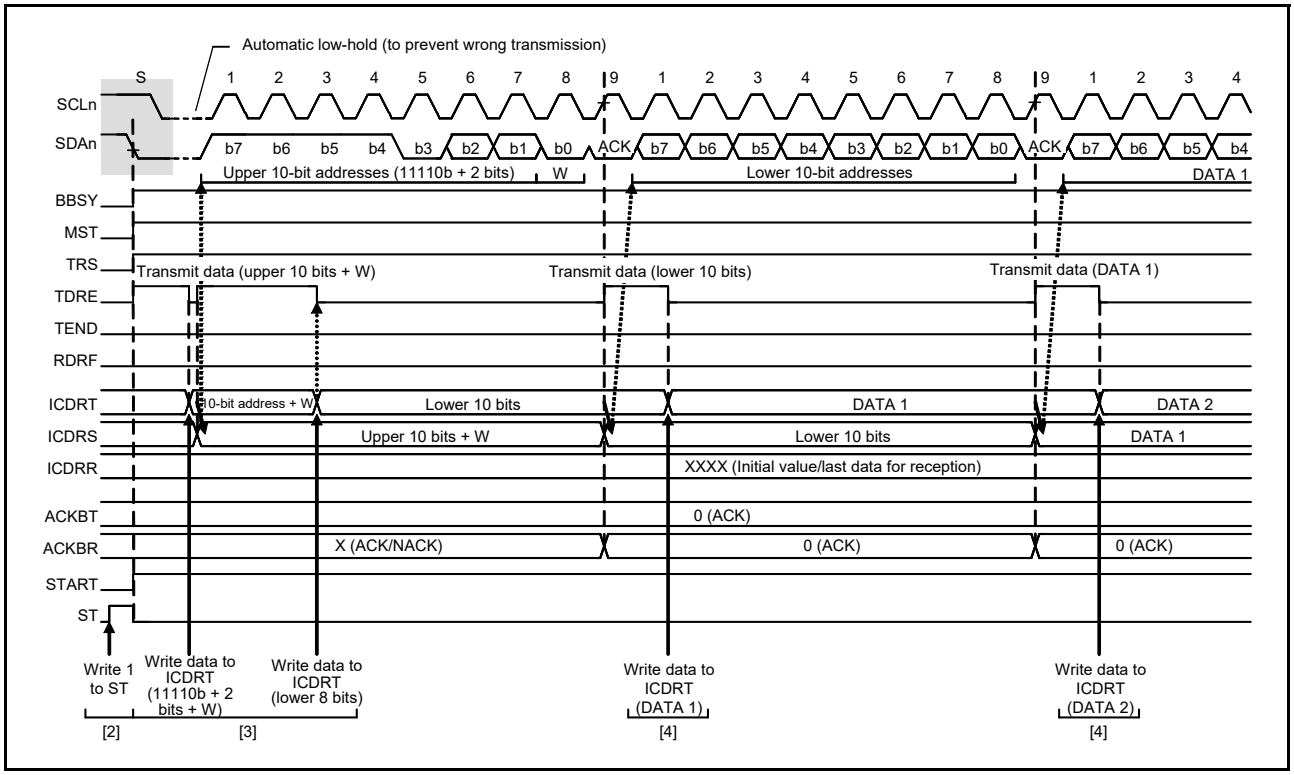


Figure 29.8 Master transmit operation timing (2) (10-bit address format)

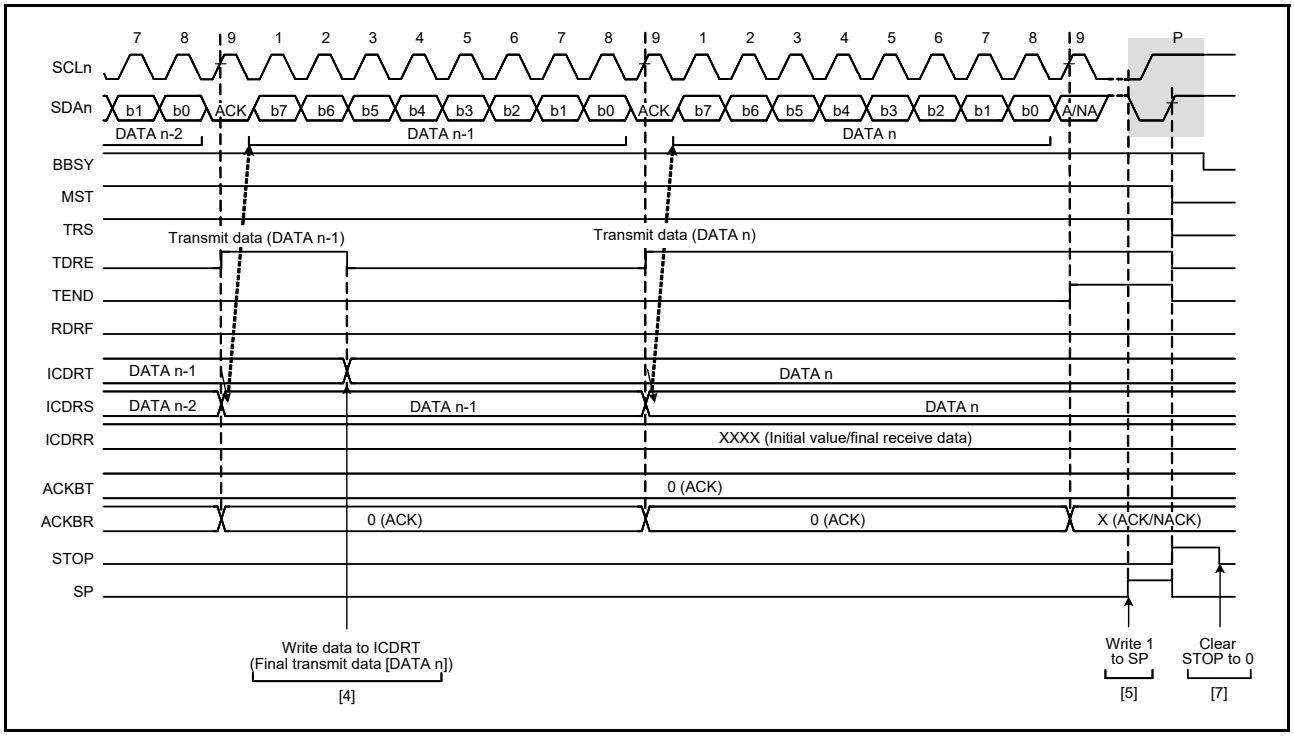


Figure 29.9 Master transmit operation timing (3)

29.3.4 Master Receive Operation

In a master receive operation, the IIC as a master device outputs the SCL clock, receives data from the slave device, and returns acknowledgments. Because the IIC must start by sending a slave address to the associated slave device, the slave address phase of the procedure is performed in master transmit mode, but the subsequent steps are performed in master receive mode.

Figure 29.10 and Figure 29.11 show examples of master reception (7-bit address format), and Figure 29.12 to Figure 29.14 show the operation timing in master reception.

To set up and perform master reception:

1. IIC initial settings. For details, see section 29.3.2, Initial Settings.
2. Read the BBSY flag in ICCR2 to check that the bus is open, then set the ST bit in ICCR2 to 1 (start condition request). On receiving the request, the IIC issues a start condition. When the IIC detects the start condition, the BBSY and START flags in ICSR2 automatically set to 1, and the ST bit is automatically set to 0. If the start condition is detected and the levels for the SDA output and the levels on the SDAn line match while the ST bit is 1, the IIC recognizes that start condition requested by the ST bit has successfully complete, and the MST and TRS bits in ICCR2 automatically set to 1, placing the IIC in master transmit mode. The TDRE flag in ICSR2 is also automatically set to 1 in response to the setting of the TRS bit to 1.
3. Check that the TDRE flag in ICSR2 is 1, then write the value for transmission (the first byte indicates the slave address and value of the R/W# bit) to ICDRT. When the transmit data is written to ICDRT, the TDRE flag is automatically set to 0, the data is transferred from ICDRT to ICDRS, and the TDRE flag is again set to 1. When the byte containing the slave address and R/W# bit is transmitted, the value of the ICCR2.TRS bit automatically updates to select transmit or receive mode according to the value of the transmitted R/W# bit. If the value of the R/W# bit is 1, the TRS bit is set to 0 on the rising edge of the ninth cycle of the SCL clock, placing the IIC in master receive mode. At this time, the TDRE flag is set to 0 and the ICSR2.RDRF flag is automatically set to 1.
   If the ICSR2.NACKF flag is 1, indicating that no slave device recognized the address or there was an error in communications, write 1 to the ICCR2.SP bit to issue a stop condition.
   For master reception from a device with a 10-bit address, start by using master transmission to issue the 10-bit address, and then issue a restart condition. After that, transmit 1111 0b, the 2 upper-order bits of the slave address, and the R bit to place the IIC in master receive mode.

4. Dummy read the ICDRR after confirming that the RDRF flag in ICSR2 is 1. Doing so causes the IIC to start output of the SCL clock and start data reception.
5. After 1 byte of data is received, the RDRF flag in ICSR2 is set to 1 on the rising edge of the eighth or ninth cycle of the SCL clock, as selected in the RDRFS bit in ICMR3. Reading ICDRR produces the received data, and the RDRF flag is automatically set to 0. The value of the acknowledgment field received during the ninth cycle of the SCL clock is returned as the value set in the ICMR3.ACKBT bit. If the next byte to be received is the next-to-last byte, set the ICMR3.WAIT bit to 1 for wait insertion before reading ICDRR, containing the second-to-last byte. In addition to enabling NACK output, even when interrupts or other operations result in delays in setting the ICMR3.ACKBT bit to 1 (NACK) in step (6), this fixes the SCLn line to the low level on the rising edge of the ninth clock cycle in reception of the last byte, which enables the issuing of a stop condition.
6. When the ICMR3.RDRFS bit is 0, and the slave device must be notified that it is to end transfer for data reception after transfer of the next and final byte, set the ICMR3.ACKBT bit to 1 (NACK).
7. After reading the second-to-last byte from the ICDRR register, if the value of the ICSR2.RDRF flag is 1, write 1 to the SP bit in ICCR2 (stop condition requested), then read the last byte from ICDRR. When ICDRR is read, the IIC is released from the wait state and issues the stop condition after low-level output in the ninth clock cycle is complete or the SCLn line is released from the low-hold state.
8. On detecting the stop condition, the IIC automatically sets the MST and TRS bits in ICCR2 to 00b and enters slave receive mode. Additionally, detection of the stop condition sets the ICSR2.STOP flag to 1.
9. Check that the ICSR2.STOP flag is 1, then set the ICSR2.NACKF and STOP flags to 0 for the next transfer operation.

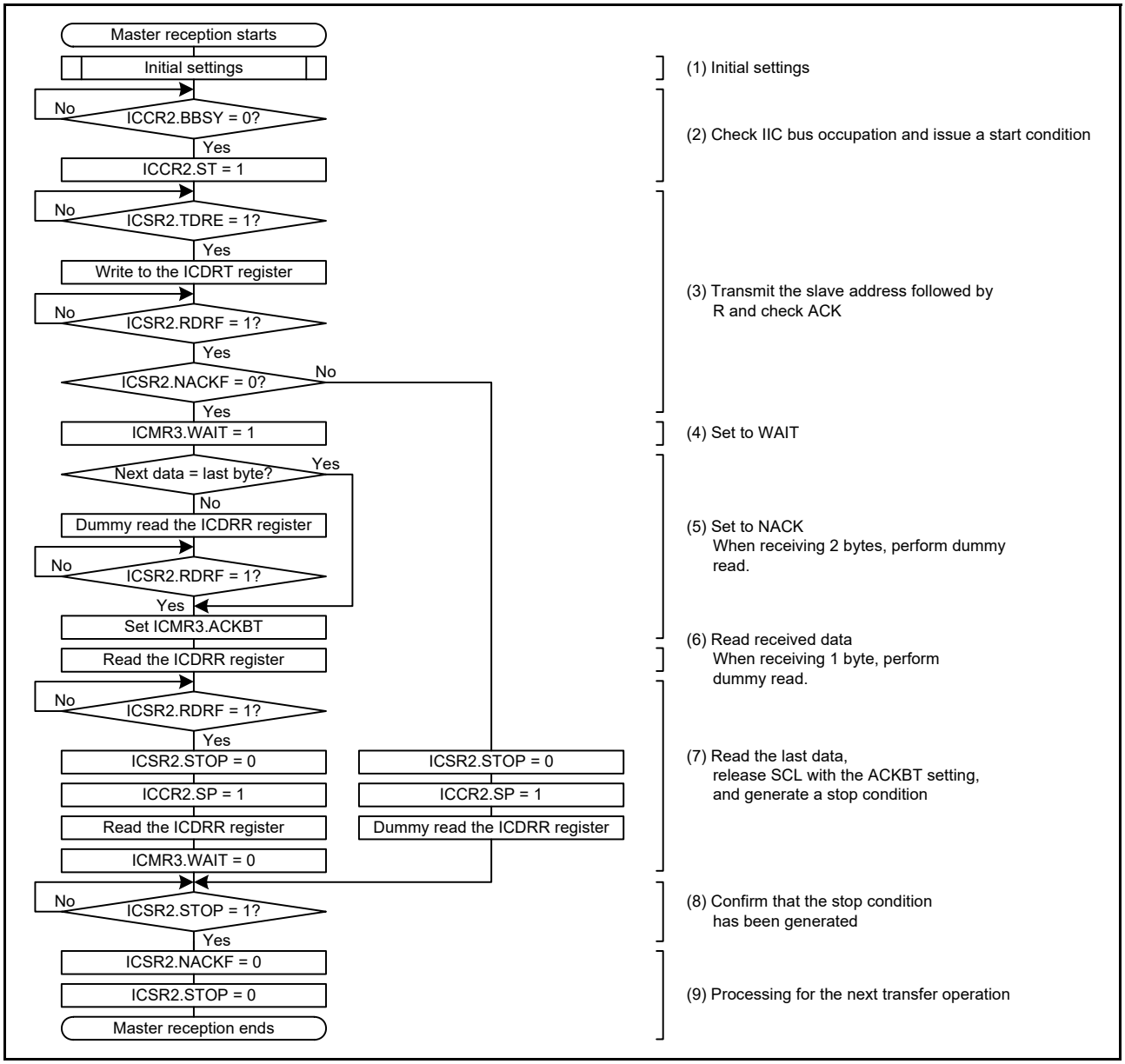


Figure 29.10 Example of master reception flow with 7-bit address format of 1 or 2 bytes

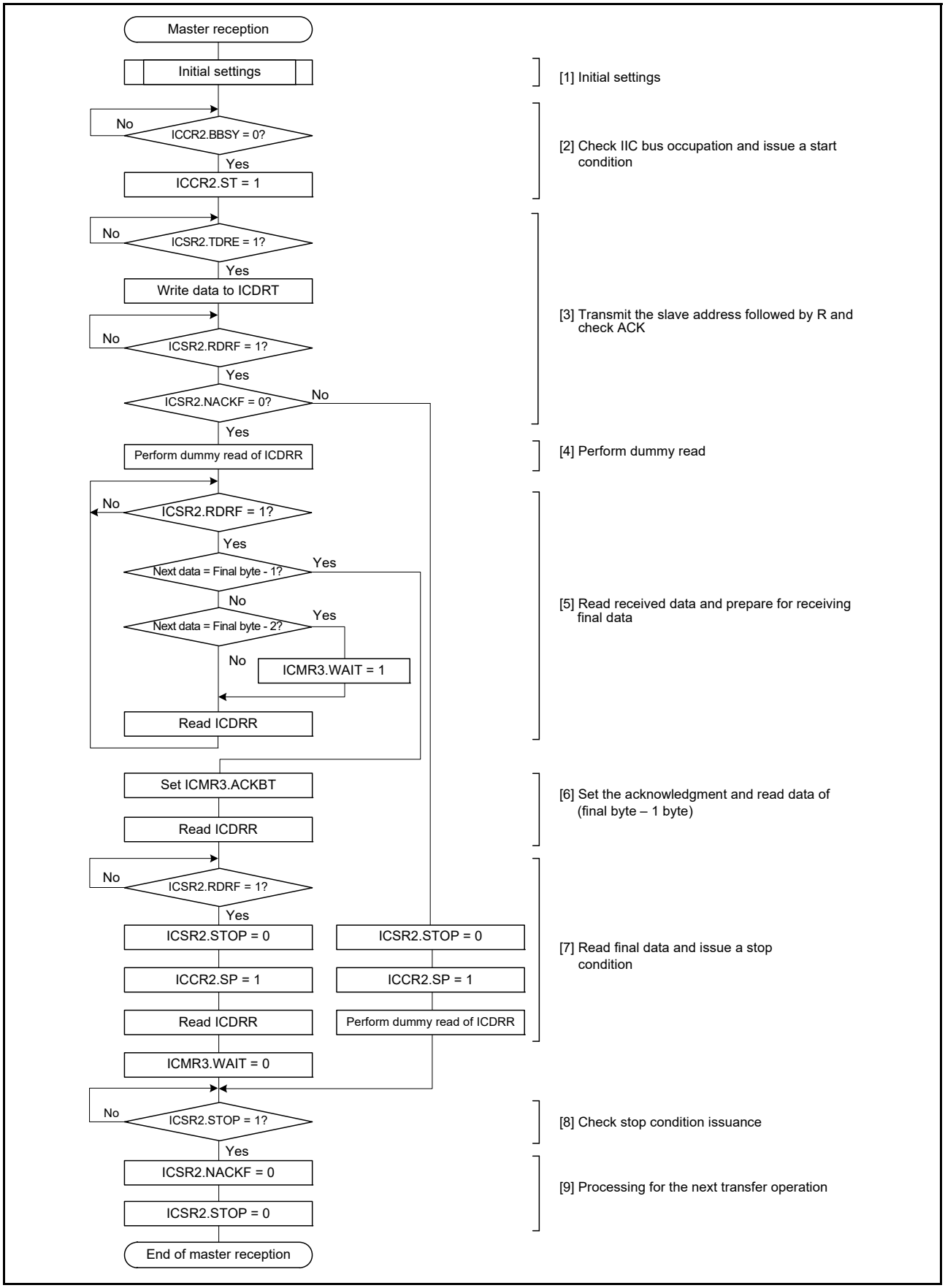


Figure 29.11 Example master reception flow with 7-bit address format of 3 or more bytes

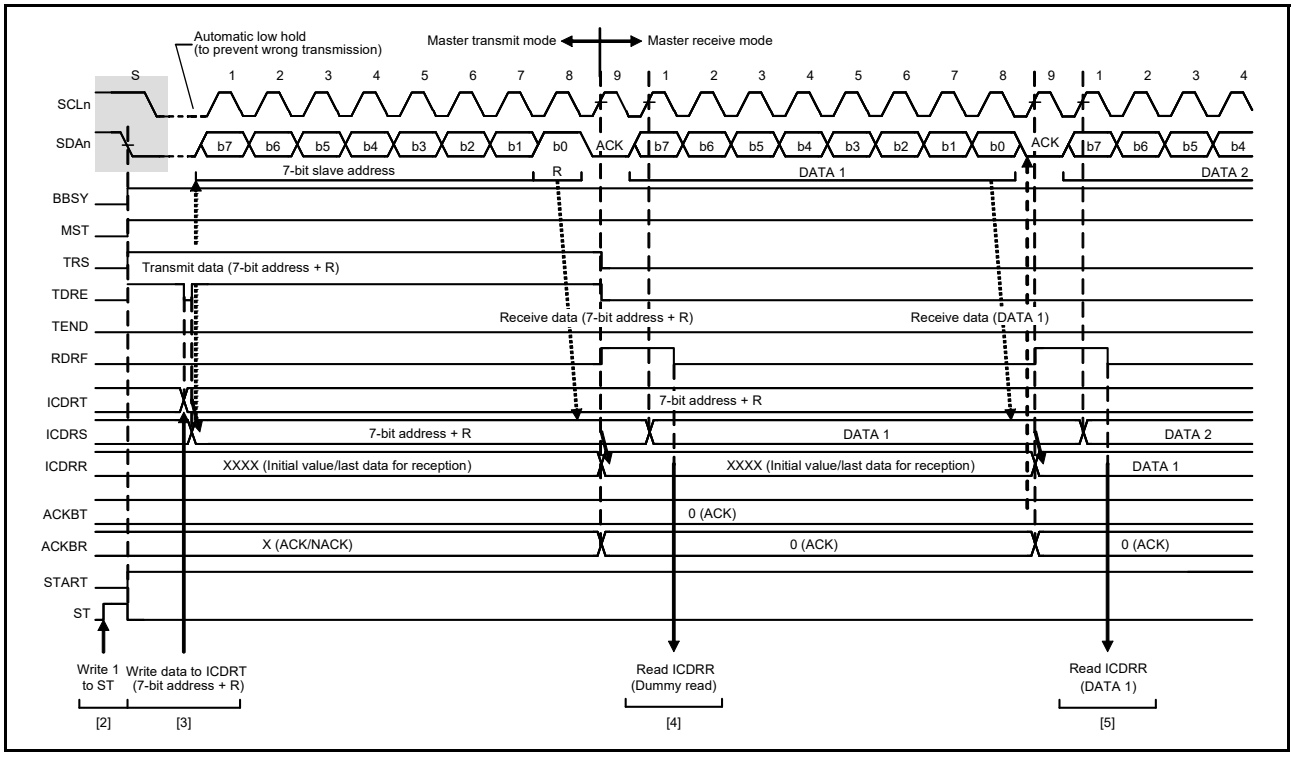


Figure 29.12 Master receive operation timing (1) with 7-bit address format when RDRFS = 0

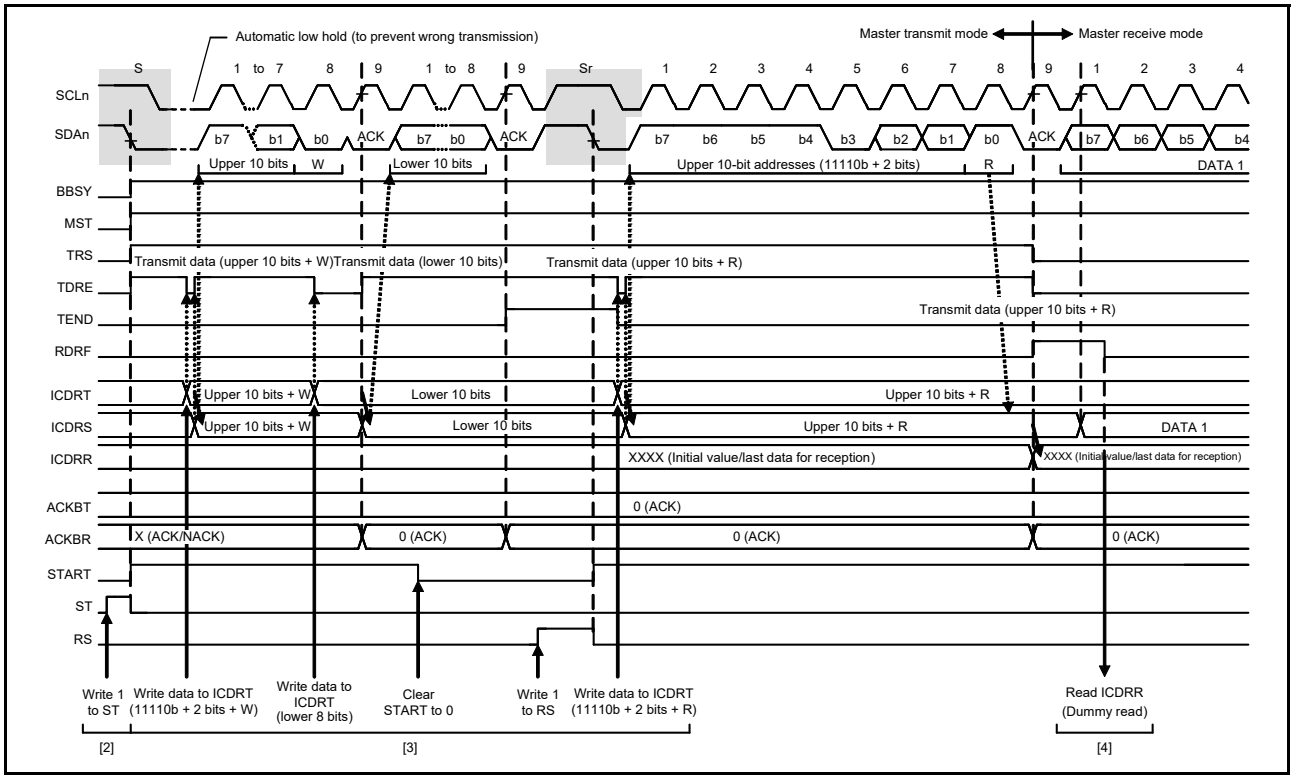


Figure 29.13 Master receive operation timing (2) with 10-bit address format when RDRFS = 0

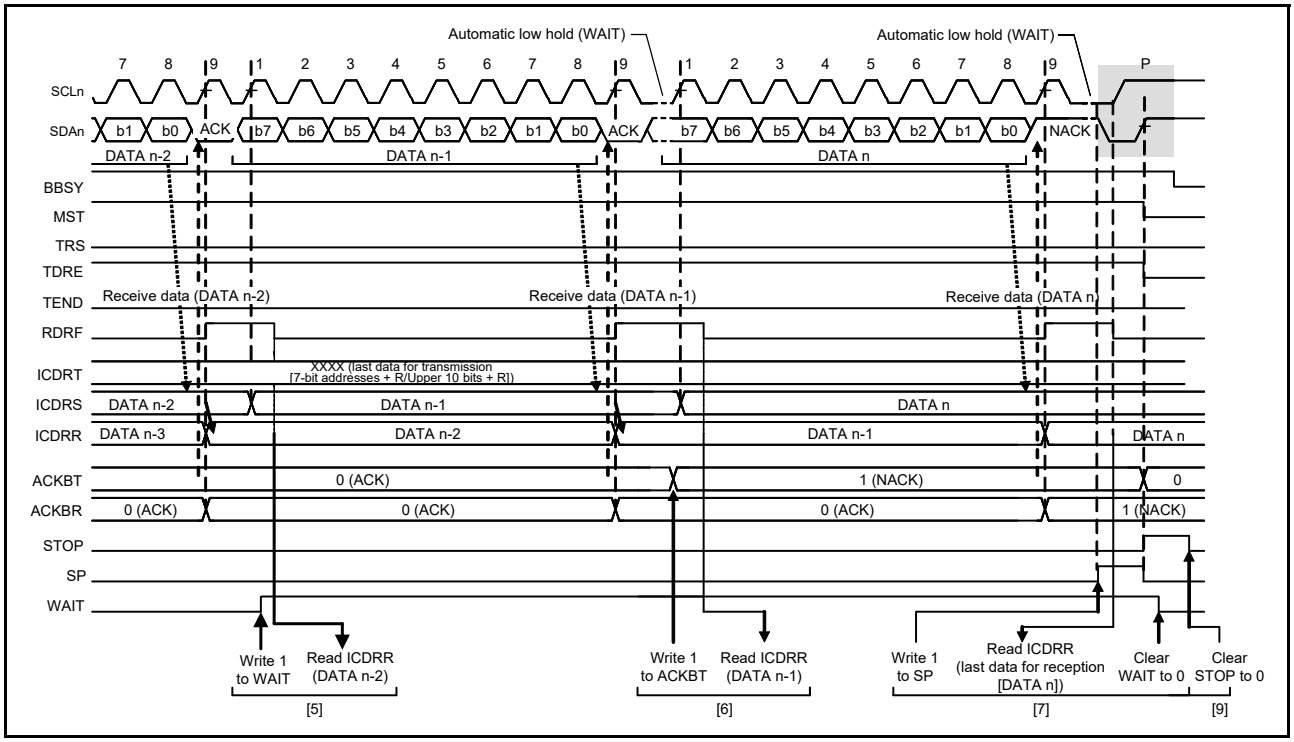


Figure 29.14 Master receive operation timing (3) when RDRFS = 0

29.3.5 Slave Transmit Operation

In a slave transmit operation, the master device outputs the SCL clock, the IIC transmits data as a slave device, and the master device returns acknowledgments.

Figure 29.15 shows an example of slave transmission, and Figure 29.16 and Figure 29.17 show the operation timing in slave transmission.

To set up and perform slave transmission:

1. IIC initial settings. For details, see section 29.3.2, Initial Settings.
   After the initial settings, the IIC stays in the standby state until it receives a slave address that it matches.
2. After receiving a matching slave address, the IIC sets one of the associated ICSR1.HOA, GCA, and AASy bits (y = 0 to 2) to 1 on the rising edge of the ninth cycle of the SCL clock and outputs the value set in the ICMR3.ACKBT bit to the acknowledge bit on the ninth cycle of the SCL clock. If the value of the received R/W# bit is 1, the IIC automatically places itself in slave transmit mode by setting both the ICCR2.TRS bit and the ICSR2.TDRE flag to 1.
3. Check that the ICSR2.TEND flag is 1, then write the transmit data to the ICDRT register. If the IIC receives no acknowledge from the master device (receives an NACK signal) when the ICFER.NACKE bit is 1, the IIC suspends transfer of the next data.
4. Wait unit the ICSR2.TEND flag is set to 1 while the ICSR2.TDRE flag is 1, after the ICSR2.NACKF flag is set to 1 or the last byte for transmission is written to the ICDRT register. When the ICSR2.NACKF flag or the TEND flag is 1, the IIC drives the SCLn line low on the ninth falling edge of the SCL clock.
5. When the ICSR2.NACKF flag or the ICSR2.TEND flag is 1, dummy read ICDRR to complete the processing. This releases the SCLn line.
6. On detecting the stop condition, the IIC automatically sets the ICSR1.HOA, GCA, and AASy bits (y = 0 to 2), the ICSR2.TDRE and TEND flags, and the ICCR2.TRS bit to 0, and enters slave receive mode.
7. Check that the ICSR2.STOP flag is 1, and then set the ICSR2.NACKF and STOP flags to 0 for the next transfer operation.

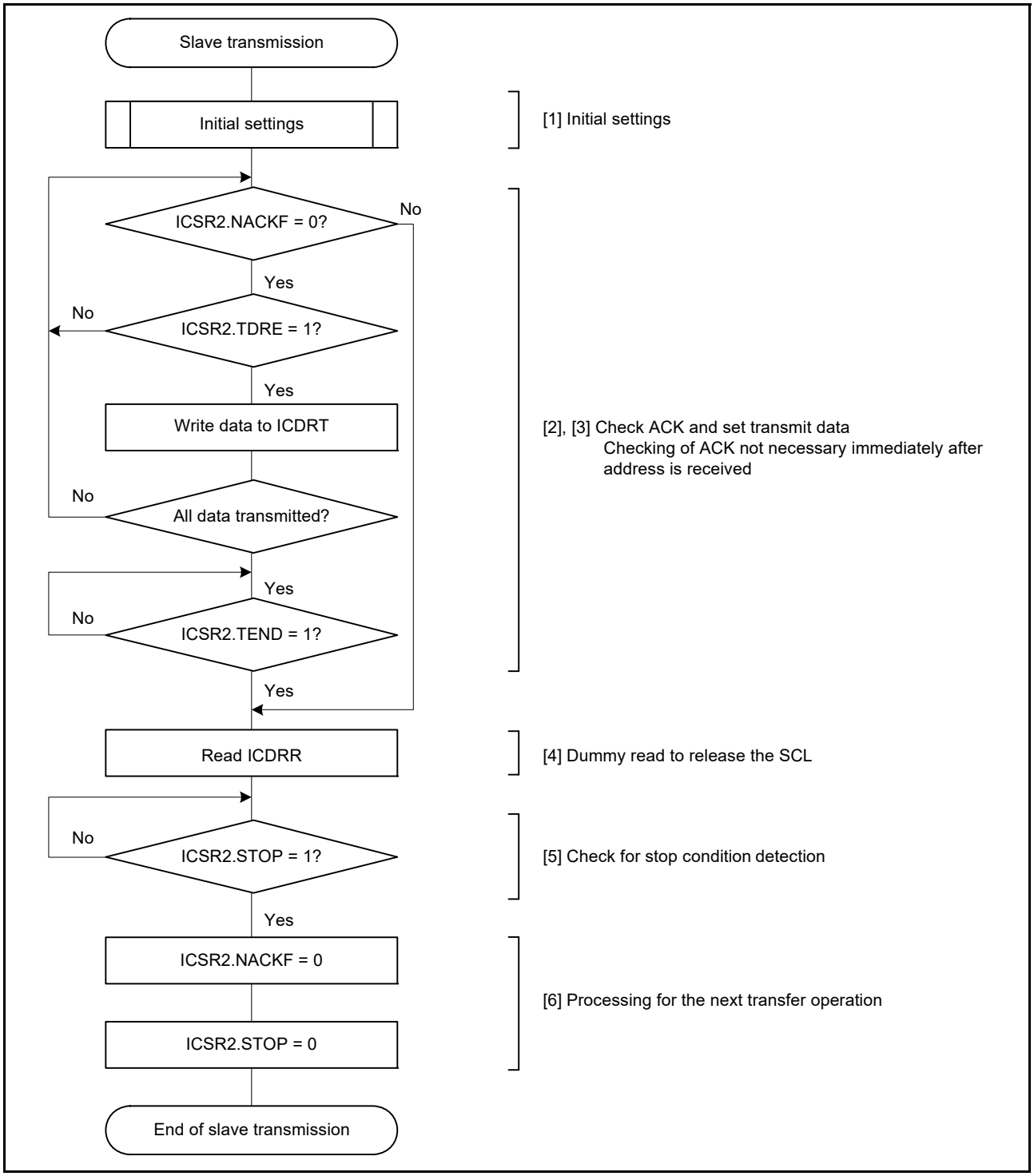


Figure 29.15 Example slave transmission flow

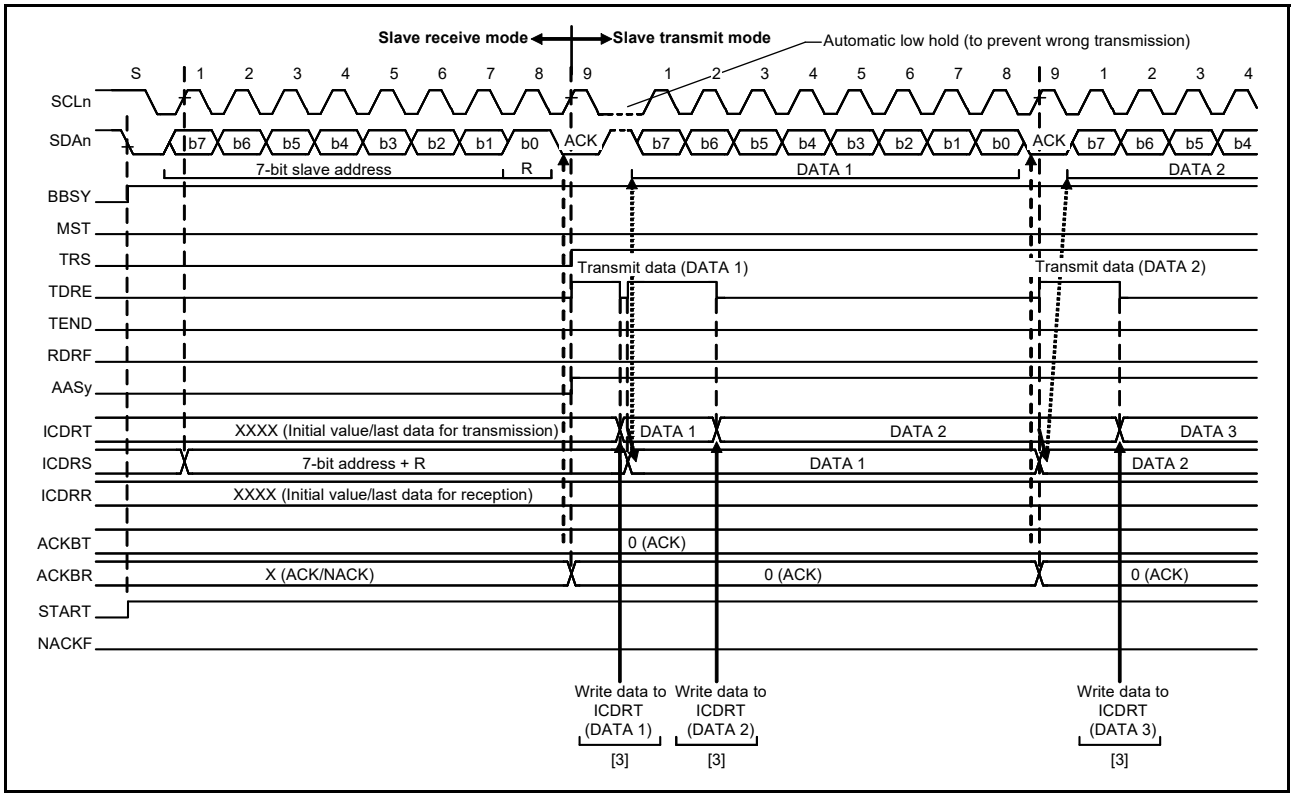


Figure 29.16 Slave transmit operation timing (1) with 7-bit address format

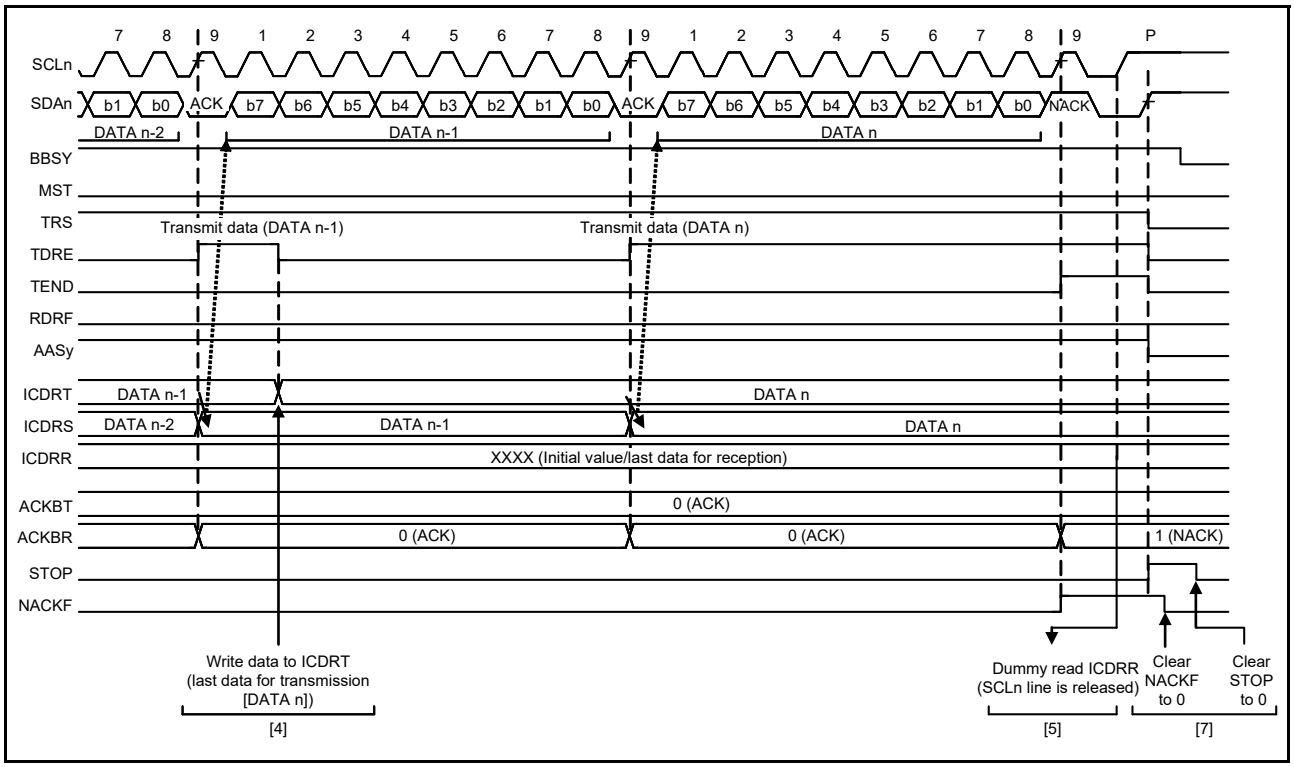


Figure 29.17 Slave transmit operation timing (2)

29.3.6 Slave Receive Operation

In a slave receive operation, the master device outputs the SCL clock and transmit data, and the IIC returns acknowledgments as a slave device.

Figure 29.18 shows an example of slave reception, and Figure 29.19 and Figure 29.20 show the operation timing in slave reception.

To set up and perform slave reception:

1. IIC initial settings. For details, see section 29.3.2, Initial Settings.
   After initialization, the IIC stays in the standby state until it receives a slave address that it matches.
2. After receiving a matching slave address, the IIC sets one of the associated ICSR1.HOA, GCA, and AASy bits (y = 0 to 2) to 1 on the rising edge of the ninth cycle of the SCL clock and outputs the value set in the ICMR3.ACKBT bit to the acknowledge bit on the ninth cycle of the SCL clock. If the value of the received R/W# bit is 0, the IIC continues to place itself in slave receive mode and sets the RDRF flag in ICSR2 to 1.
3. Check that the ICSR2.STOP flag is 0 and the ICSR2.RDRF flag is 1, then dummy read ICDRR. The dummy value consists of the slave address and R/W# bit when the 7-bit address format is selected, or the lower 8 bits when the 10-bit address format is selected.
4. When ICDRR is read, the IIC automatically sets the ICSR2.RDRF flag to 0. If reading of ICDRR is delayed and a next byte is received while the RDRF flag is still set to 1, the IIC holds the SCLn line low from one SCL cycle before the point where RDRF must be set. In this case, reading ICDRR releases the SCLn line from being held at the low level.
   When the ICSR2.STOP flag is 1 and the ICSR2.RDRF flag is also 1, read ICDRR until all the data is completely received.
5. On detecting the stop condition, the IIC automatically sets the ICSR1.HOA, GCA, and AASy bits (y = 0 to 2) to 0.
6. Check that the ICSR2.STOP flag is 1, then set the ICSR2.STOP flag to 0 for the next transfer operation.

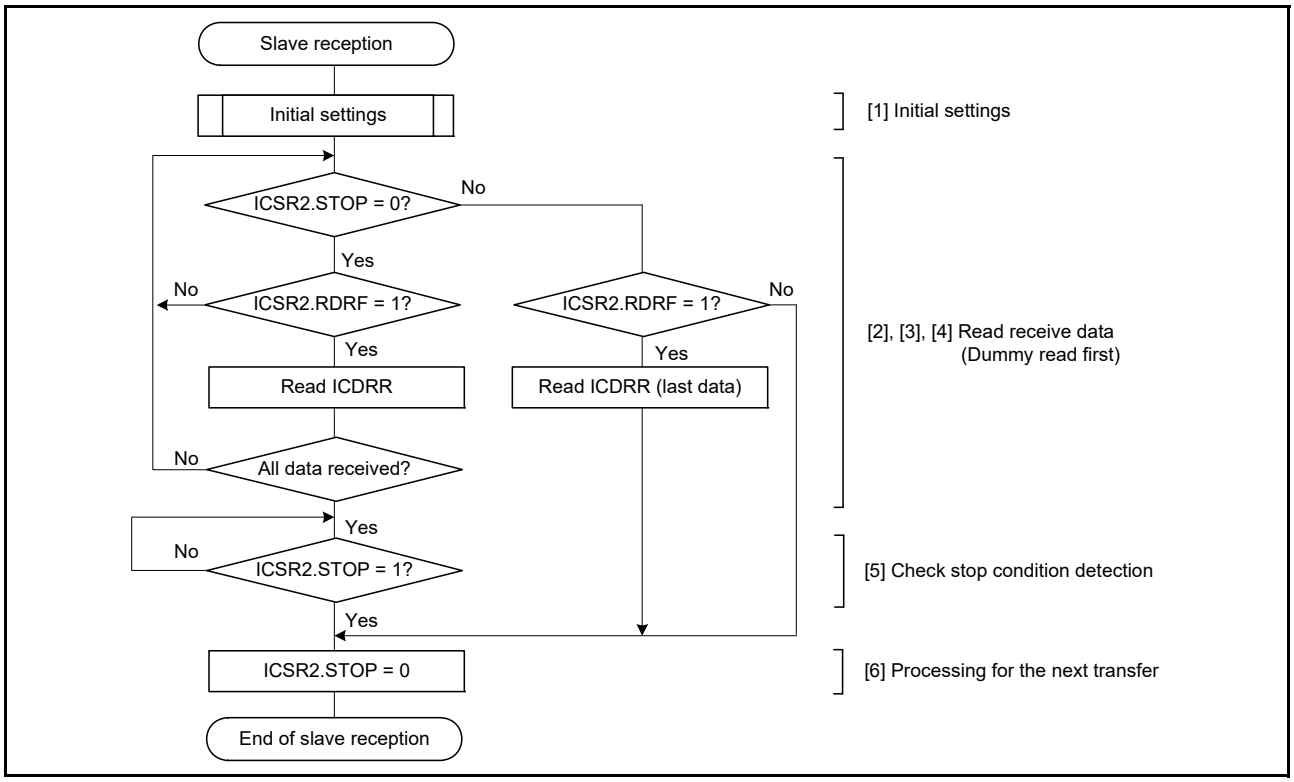


Figure 29.18 Example slave reception flow

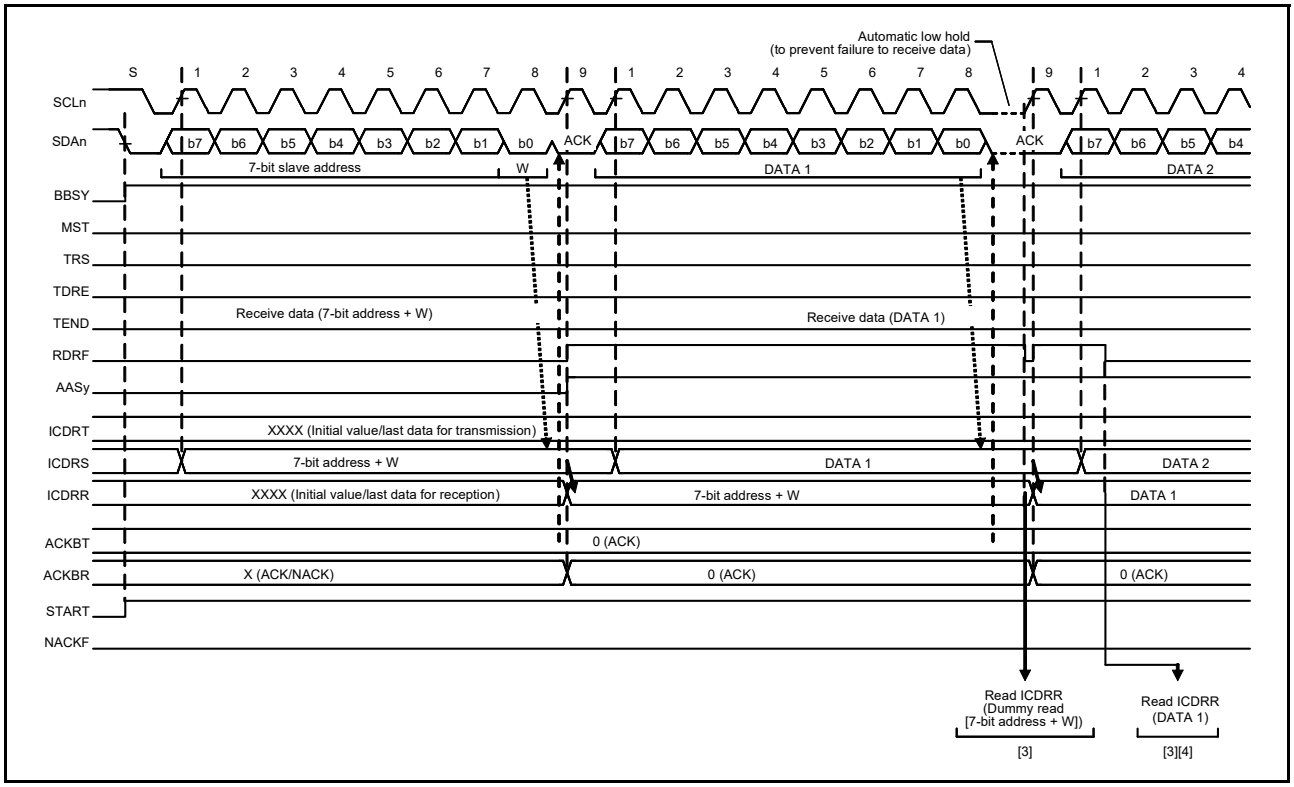


Figure 29.19 Slave receive operation timing (1) with 7-bit address format, when RDRFS = 0

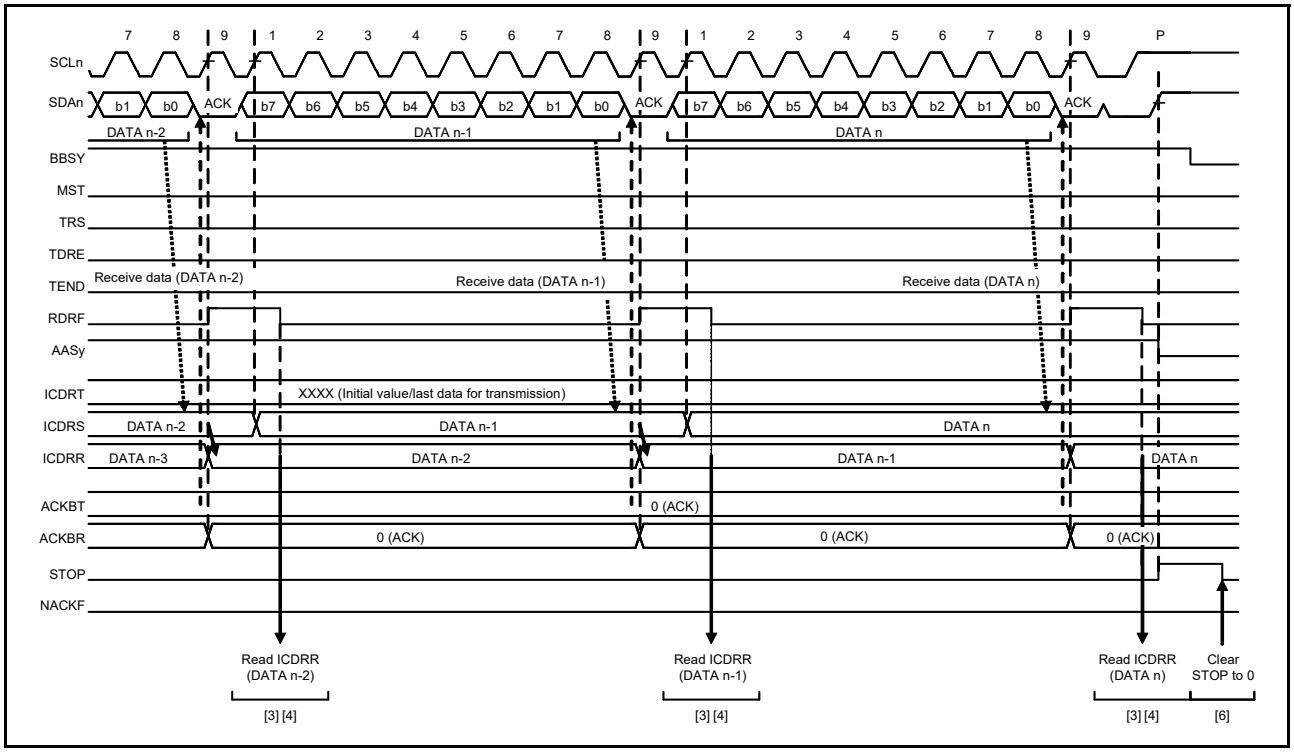


Figure 29.20 Slave receive operation timing (2) when RDRFS = 0

29.4 SCL Synchronization Circuit

To generate the SCL clock, the IIC starts counting the value for the high-level period specified in ICBRH.BRH[4:0] when it detects a rising edge on the SCLn line, then drives the SCLn line low when it completes counting. When the IIC detects the falling edge of the SCLn line, it starts counting the value for the low-level period specified in

ICBRL.BRL[4:0], and then it stops driving the SCLn line (releases the line) when it completes counting. The IIC repeats this process to generate the SCL clock.

If multiple master devices are connected to the I2C bus, a collision of SCL signals might arise because of contention with another master device. In such cases, the master devices must synchronize their SCL signals. Because this synchronization of SCL signals must be bit-by-bit, the IIC includes an SCL synchronization circuit to obtain bit-by-bit synchronization by monitoring the SCLn line while in master mode.

When the IIC detects a rising edge on the SCLn line and so starts counting out the high-level period specified in ICBRH.BRH[4:0], and the level on the SCLn line falls because an SCL signal is being generated by another master device, the IIC stops counting when it detects the falling edge, drives the level on the SCLn line low, and starts counting the low-level period specified in ICBRL.BRL[4:0]. When the IIC finishes counting the low-level period, it stops driving the SCLn line low to release the line. If the low-level period of the SCL clock signal from the other master device is longer than the low-level period set in the IIC, the low-level period of the SCL signal is extended. When the low-level period for the other master device has ended, the SCL signal rises because the SCLn line was released. When the IIC finishes outputting the low-level period of the SCL clock, the SCLn line is released and the SCL clock rises. That is, when SCL signals from more than one master are contending, the high-level period of the SCL signal is synchronized with that of the clock with the narrower period, and the low-level period of the SCL signal is synchronized with that of the clock with the broader period. However, such synchronization of the SCL signal is only enabled when the SCLE bit in ICFER is set to 1.

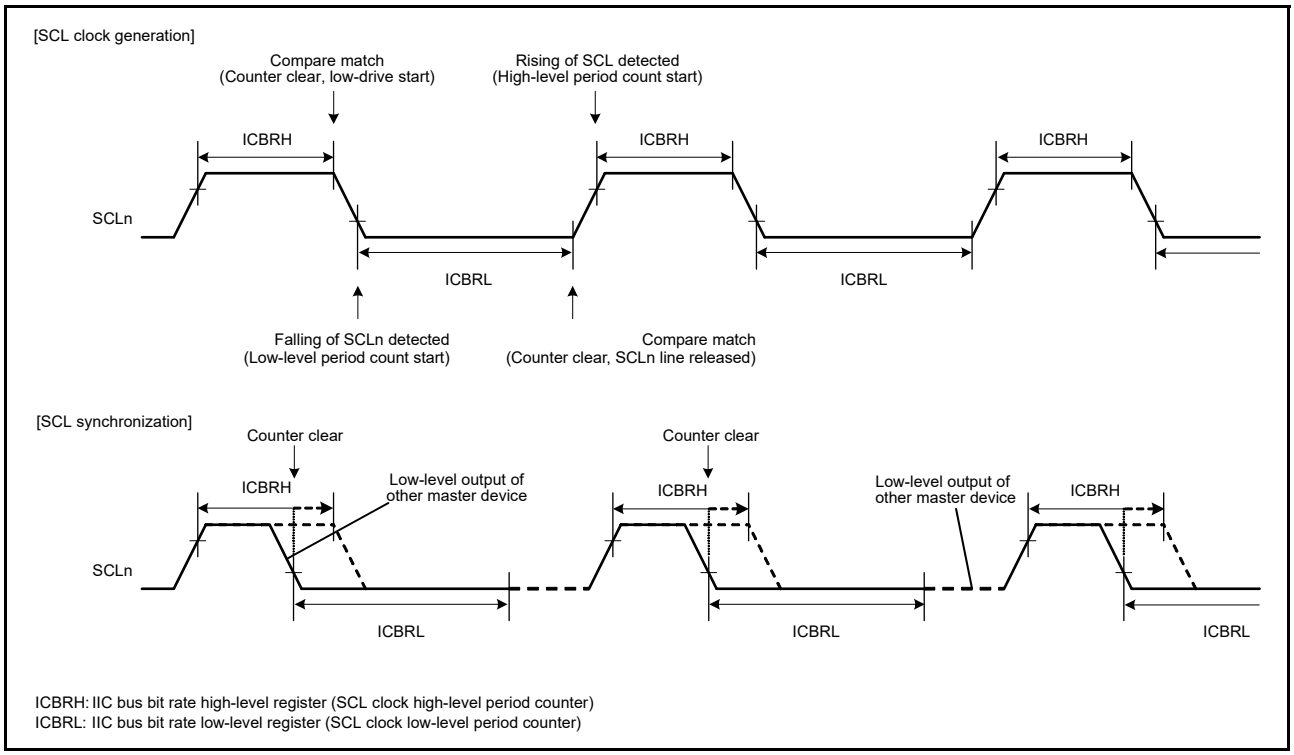


Figure 29.21 Generation and synchronization of SCL signal from IIC

29.5 SDA Output Delay Function

The IIC module incorporates a function for delaying output on the SDA line. The delay can be applied to all output on the SDA line, including issuing of the start, restart, and stop conditions, data, and the ACK and NACK signals.

With this function, SDA output is delayed from the detection of a falling edge of the SCL signal to ensure that the SDA signal is output within the interval during which the SCL clock is low. This approach helps prevent erroneous operation of communications devices, with the aim of satisfying the 300-ns minimum data-hold time requirement of the SMBus specification. The output delay function is enabled by setting the SDDL[2:0] bits in ICMR2 to any value other than 000b, and disabled by setting the same bits to 000b.

While the SDA output delay function is enabled, for example, while the SDDL[2:0] bits in ICMR2 are set to any value other than 000b, the DLCS bit in ICMR2 selects the clock source for counting by the SDA output delay counter either as

the internal base clock (IICϕ) for the IIC module or as the internal base clock divided by two (IICϕ/2). The counter counts the number of cycles set in the SDDL[2:0] bits in ICMR2. After delay cycles count is complete, the IIC module places the required output (start, restart, or stop condition, data, or an ACK or NACK signal) on the SDA line.

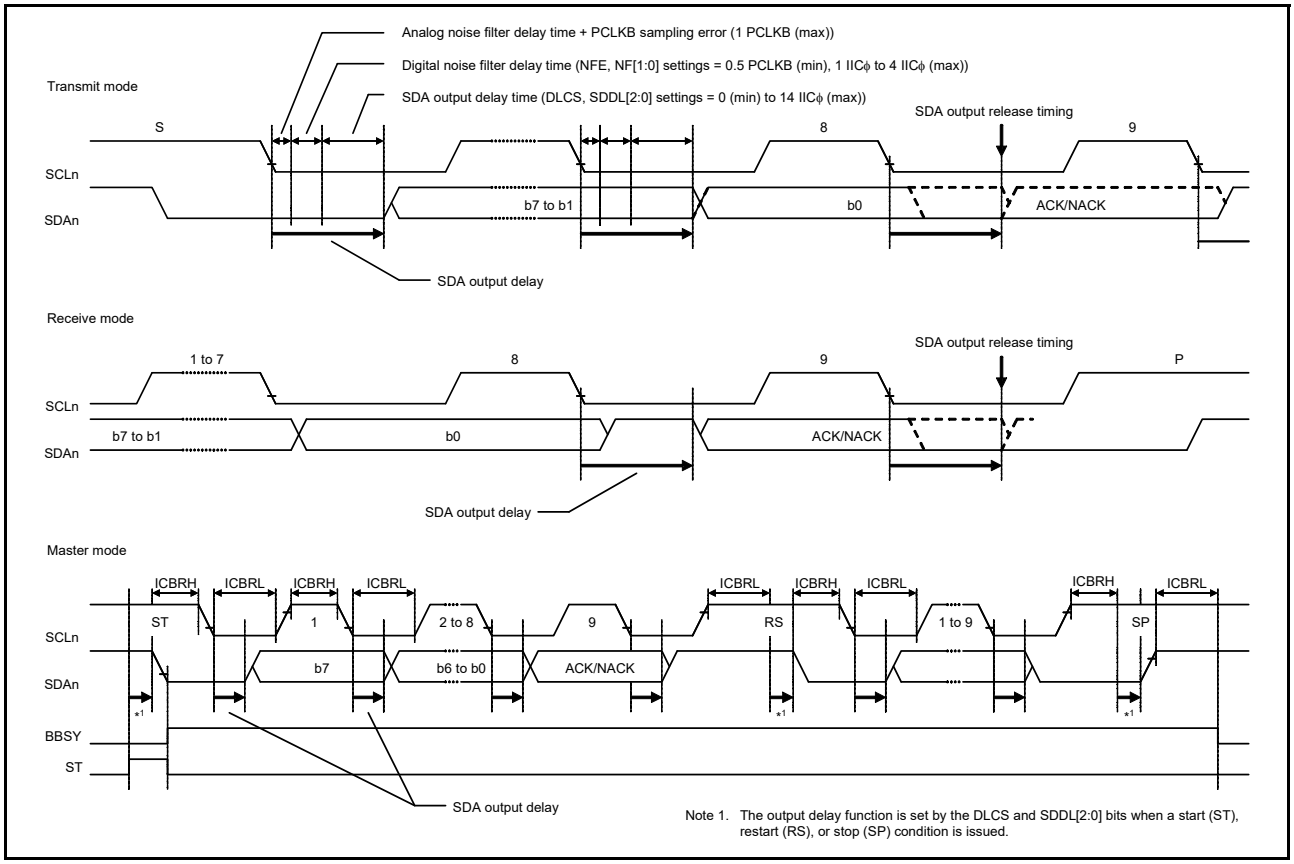


Figure 29.22 SDA output delay function

29.6 Digital Noise Filter Circuits

The states of the SCLn and SDAn pins are conveyed to the internal circuitry through analog noise-filter and digital noise-filter circuits. Figure 29.23 is a block diagram of the digital noise-filter circuit.

The on-chip digital noise-filter circuit of the IIC consists of four flip-flop circuit stages connected in series and a match-detection circuit.

The number of effective stages in the digital noise filter is selected in the NF[1:0] bits in ICMR3. The selected number of effective stages determines the noise-filtering capability as a period from one to four IICϕ cycles.

The input signal to the SCLn pin (or SDAn pin) is sampled on falling edges of the IICϕ signal. When the input signal level matches the output level of the number of effective flip-flop circuit stages as selected in the NF[1:0] bits in ICMR3, the signal level is conveyed to the subsequent stage. If the signal levels do not match, the previous value is saved.

If the ratio between the frequency of the internal operating clock (PCLKB) and the transfer rate is small, for instance, if data transfer at 400 kbps with PCLKB at 4 MHz, the characteristics of the digital noise filter might lead to the elimination of required signals as noise. In such cases, it is possible to disable the digital noise-filter circuit, by setting the ICFER.NFE bit to 0, and use only the analog noise-filter circuit.

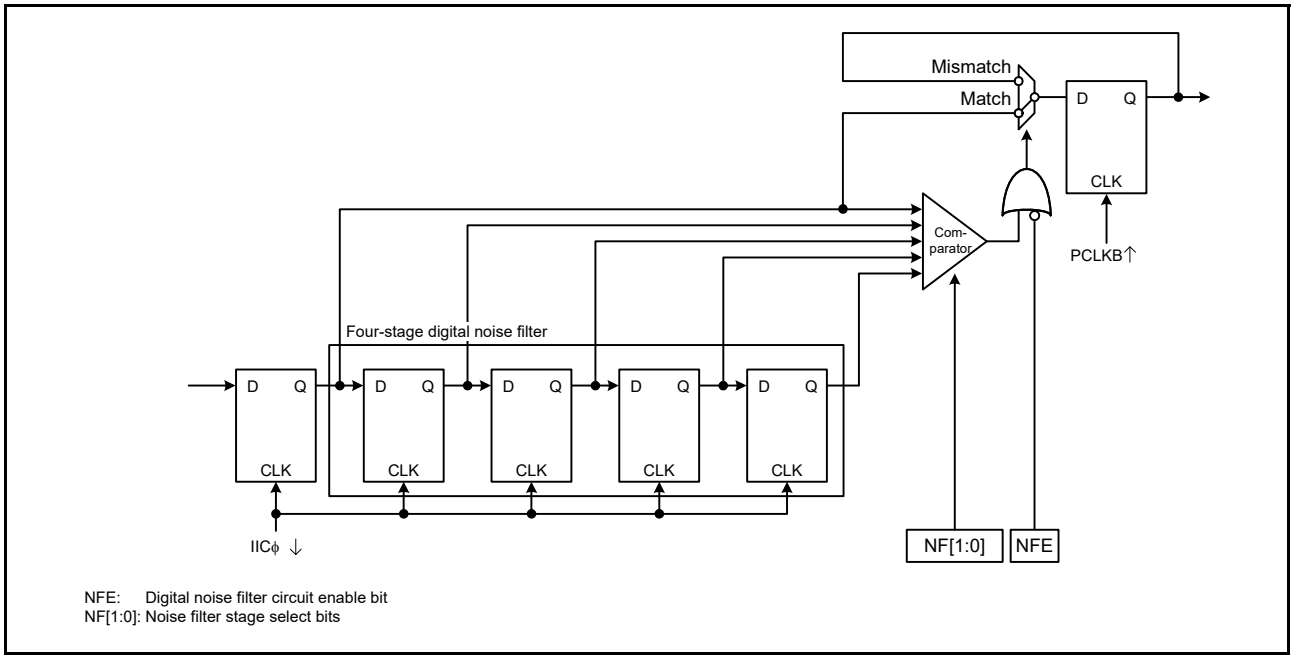


Figure 29.23 Digital noise filter circuit block diagram

29.7 Address Match Detection

The IIC can set three unique slave addresses in addition to the general call address and host address, and also can set 7-bit or 10-bit slave addresses.

29.7.1 Slave-Address Match Detection

The IIC can set three unique slave addresses and has a slave address detection function for each unique slave address. When the SARyE bit (y = 0 to 2) in ICSER is set to 1, the slave addresses set in SARUy and SARLy (y = 0 to 2) can be detected.

When the IIC detects a match of the set slave address, the associated AASy flag (y = 0 to 2) in ICSR1 is set to 1 on the rising edge of the ninth SCL clock cycle, and the RDRF flag in ICSR2 or the TDRE flag in ICSR2 is set to 1 by the subsequent R/W# bit. This causes a receive data full interrupt (IICn_RXI) or transmit data empty interrupt (IICn_TXI) to be generated. The AASy flag identifies which slave address is specified.

Figure 29.24 to Figure 29.26 show the AASy flag set timing in three cases.

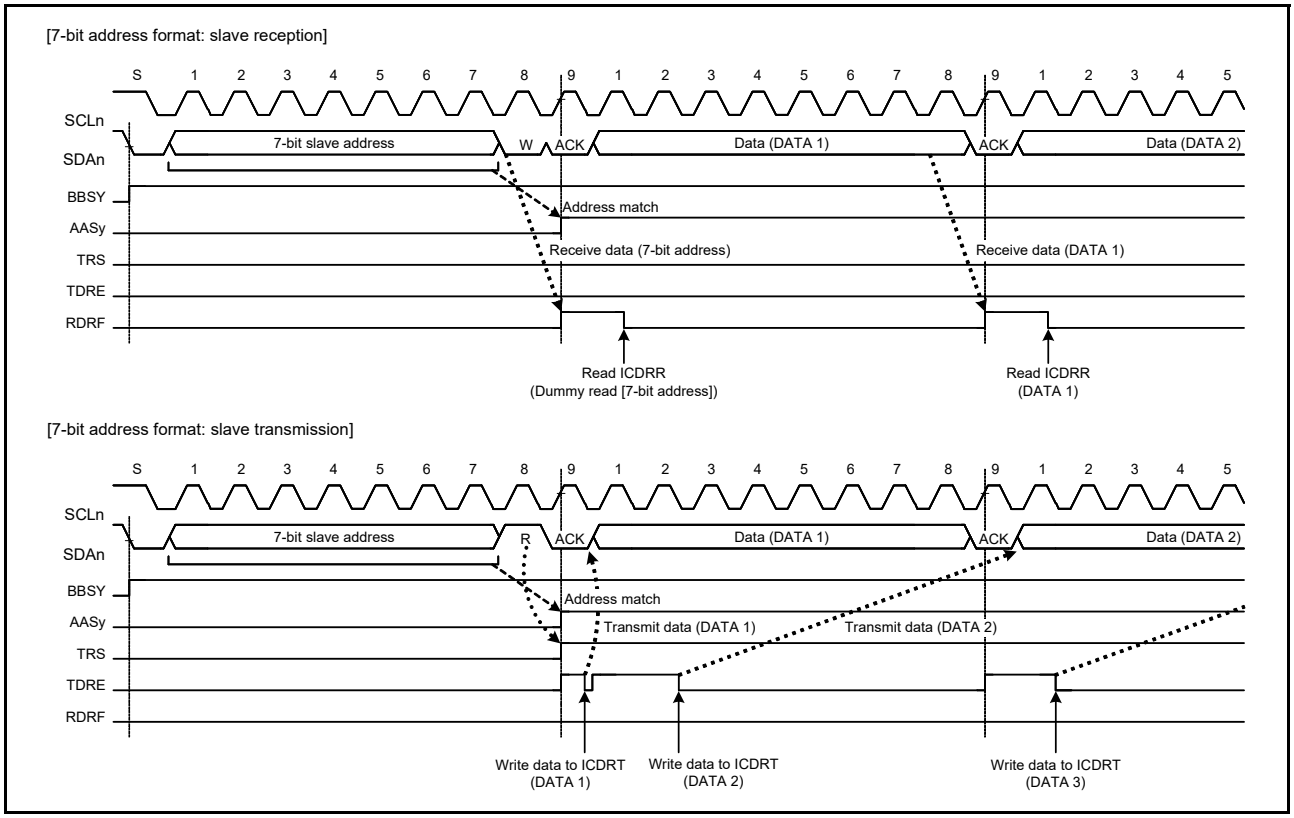


Figure 29.24 AASy flag set timing with 7-bit address format

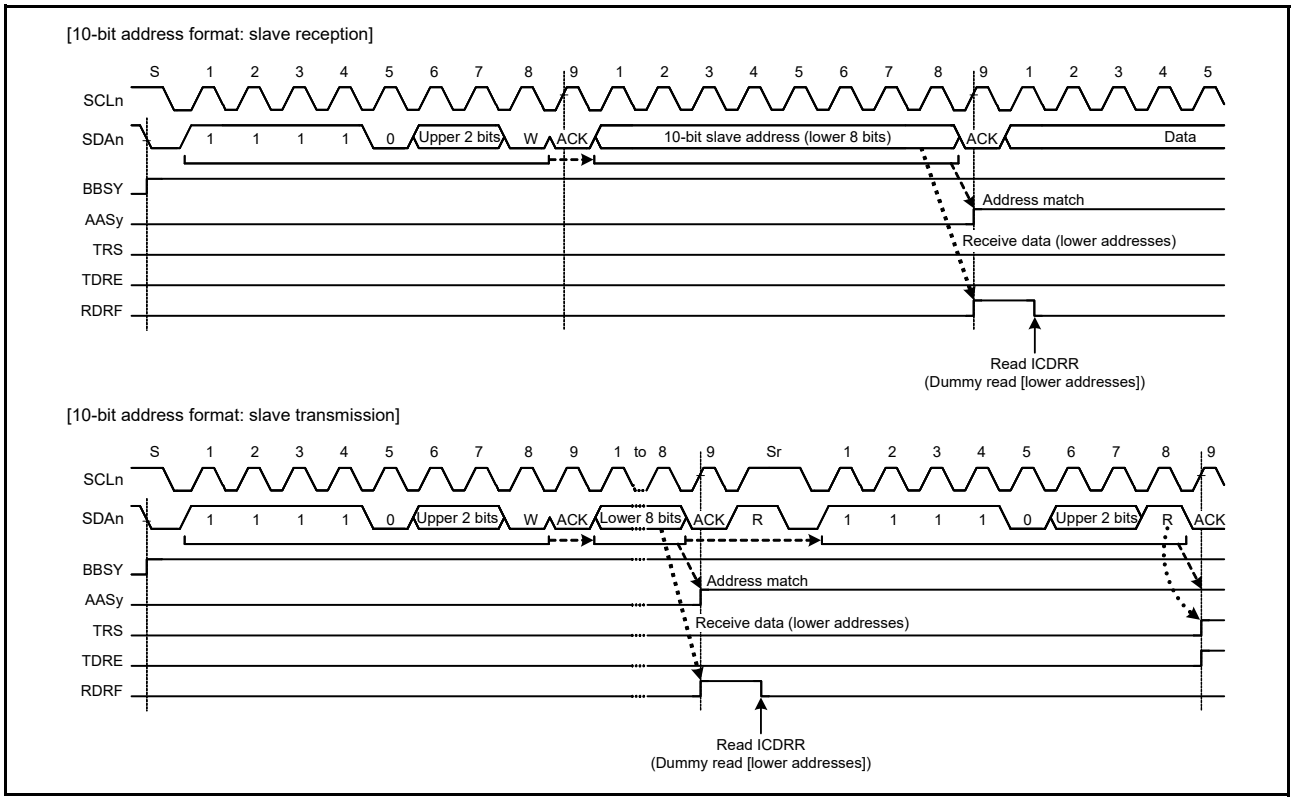


Figure 29.25 AASy flag set timing with 10-bit address format

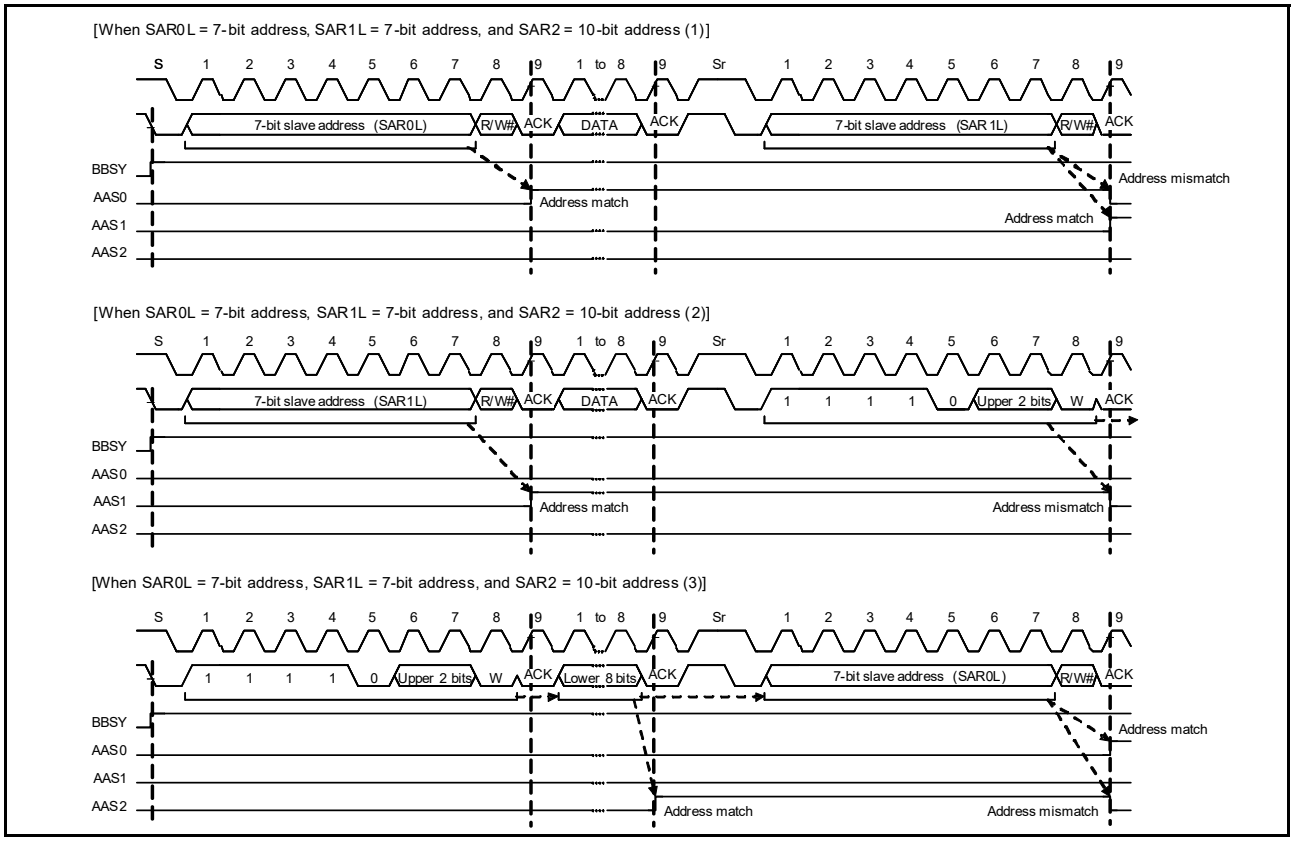


Figure 29.26 AASy flag set and clear timing with 7-bit and 10-bit address formats mixed

29.7.2 Detection of General Call Address

The IIC provides detection of the general call address (0000 000b + 0 [W]). This is enabled by setting the GCAE bit in ICSER to 1.

If the address received after a start or restart condition is issued is 0000 000b + 1[R] (start byte), the IIC recognizes this as the address of a slave device with an all-zero address, but not as the general call address.

When the IIC detects the general call address, both the GCA flag in ICSR1 and the RDRF flag in ICSR2 are set to 1 on the rising edge of the ninth cycle of the SCL clock. This leads to the generation of a receive data full interrupt (IICn_RXI). The value of the GCA flag can be checked to confirm that the general call address was transmitted.

Operation after detection of the general call address is the same as normal slave receive operation.

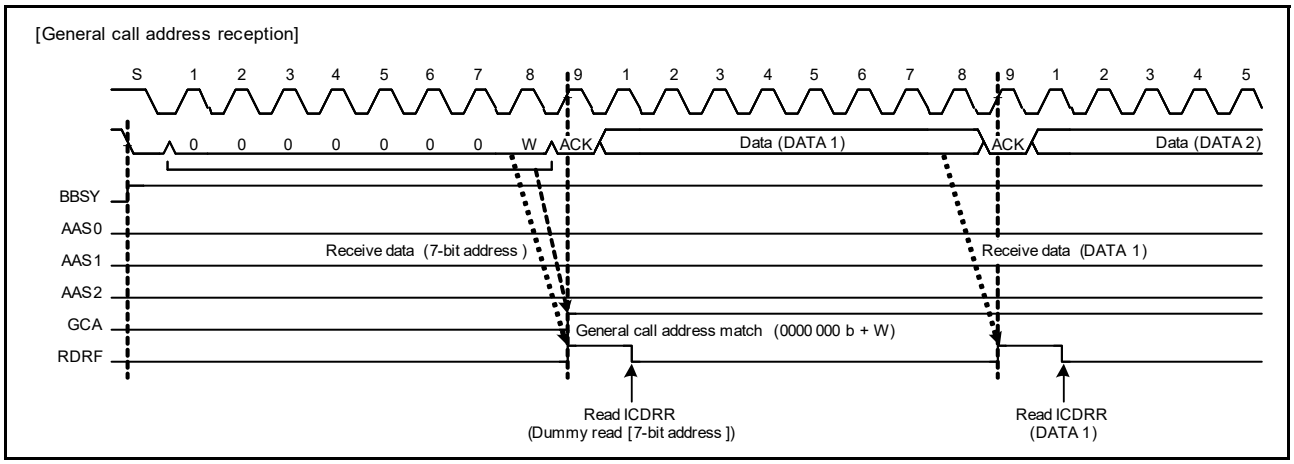


Figure 29.27 Timing of GCA flag setting during reception of general call address

29.7.3 Device-ID Address Detection

The IIC module provides detection of device-ID address in compliance with the I2C bus specification (Rev. 03). When the IIC receives 1111 100b as the first byte after a start or restart condition was issued with the DIDE bit in ICSER set to 1, it recognizes the address as a device ID, sets the DID flag in ICSR1 to 1 on the rising edge of the 9th SCL clock cycle when the subsequent R/W# bit is 0, then compares the second and subsequent bytes with its own slave address. If the address matches the value in the slave address register, the IIC sets the associated AASy flag (y = 0 to 2) in ICSR1 to 1.

After that, when the first byte received after issuance of a start or restart condition matches the device ID address (1111 100b) again and the subsequent R/W# bit is 1, the IIC does not compare the second and subsequent bytes and sets the ICSR2.TDRE flag to 1.

In the device-ID address detection function, the IIC sets the DID flag to 0 if a match with the IIC slave address is not obtained or a match with the device ID address is not obtained after a match with the IIC slave address and the detection of a restart condition. If the first byte after detection of a start or restart condition matches the device ID address (1111 100b) and the R/W# bit is 0, the IIC sets the DID flag to 1 and compares the second and subsequent bytes with the slave address of the IIC. If the R/W# bit is 1, the DID flag holds the previous value and the IIC does not compare the second and subsequent bytes. Therefore, the reception of a device-ID address can be checked by reading the DID flag after confirming that TDRE = 1.

Additionally, prepare the device-ID fields (3 bytes: 12 bits indicating the manufacturer + 9 bits identifying the part + 3 bits indicating the revision) that must be sent to the host after reception of a continuous device-ID field as normal transmit data. For details on the information that must be included in device-ID fields, contact NXP Semiconductors.

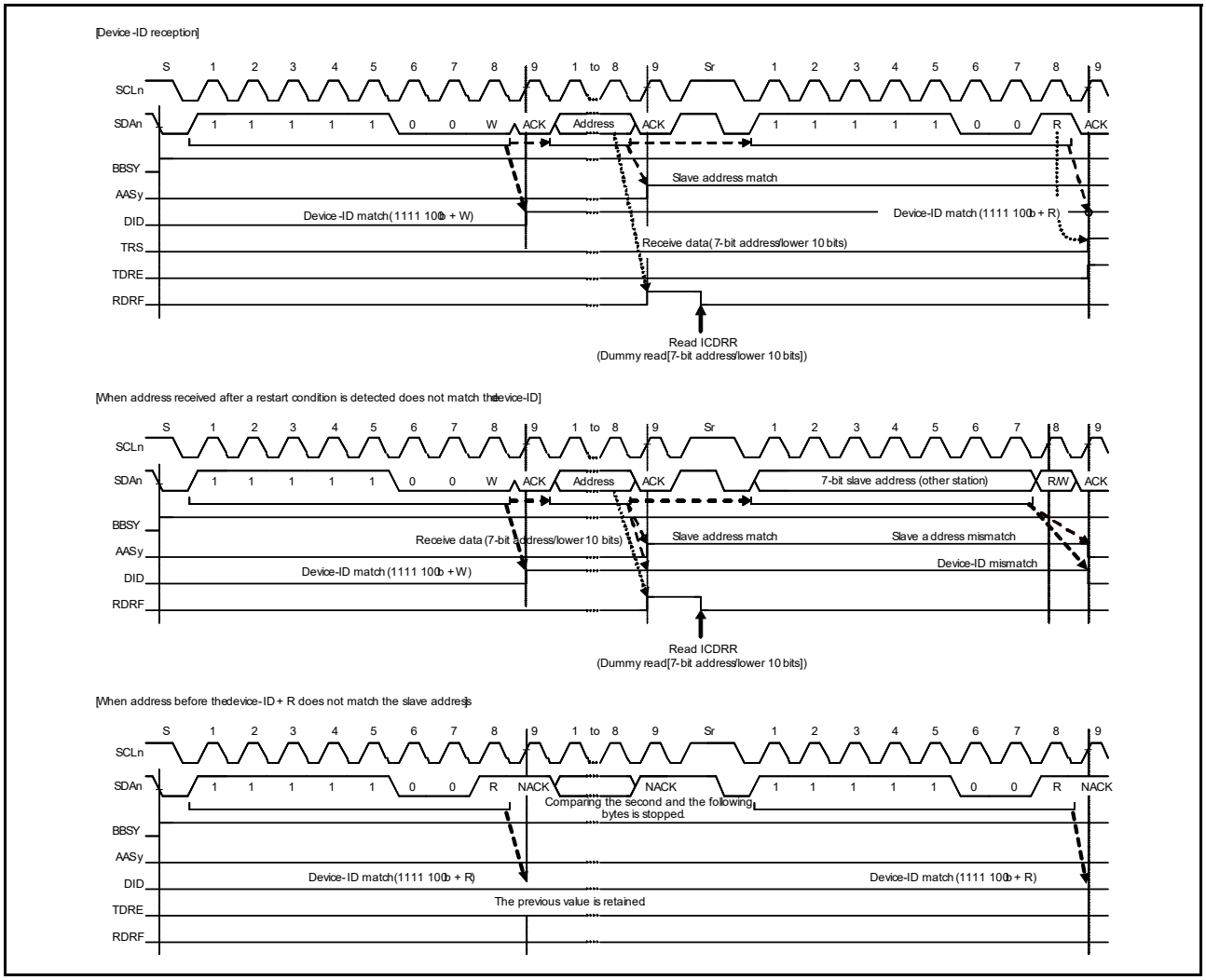


Figure 29.28 AASy/DID flag set and clear timing during reception of device ID

29.7.4 Host Address Detection

The IIC provides host address detection while the SMBus is operating. When the HOAE bit in ICSER is set to 1 while the SMBS bit in ICMR3 is 1, the IIC can detect the host address (0001 000b) in slave receive mode (MST and TRS bits = 00b in ICCR2).

When the IIC detects the host address, the HOA flag in ICSR1 is set to 1 on the rising edge of the ninth SCL clock cycle, and at the same time, the RDRF flag in ICSR2 is set to 1 when the R/W# bit is 0 (Wr bit). This causes a receive data full interrupt (IICn_RXI) to be generated. The HOA flag indicates that the host address was sent from other devices.

If the bit following the host address (0001 000b) is an Rd bit (R/W# bit = 1), the IIC can also detect the host address. After the host address is detected, the IIC operates in the same manner as in normal slave operation.

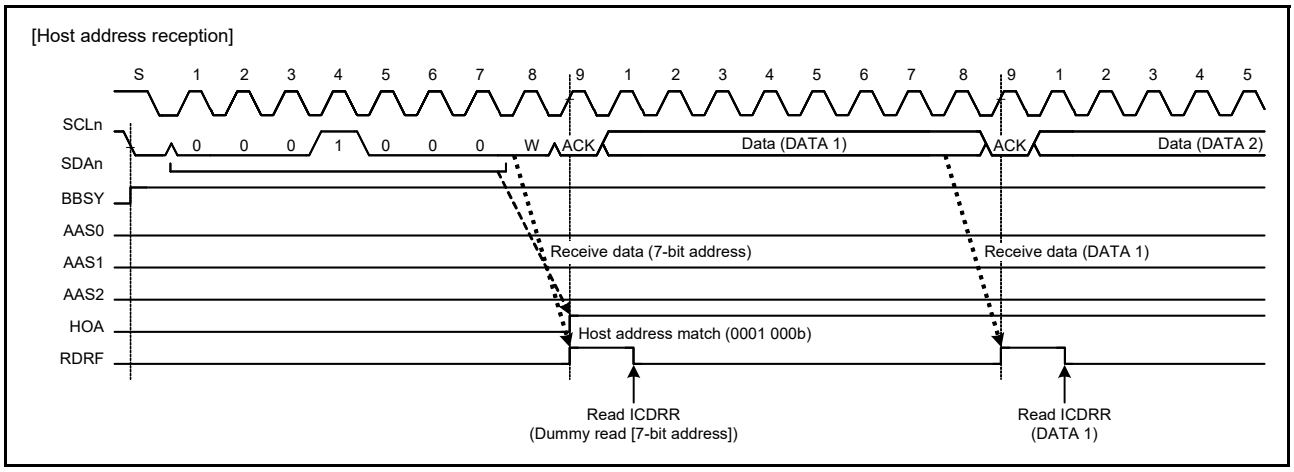


Figure 29.29 HOA flag set timing during reception of host address

29.8 Wakeup Function

The IIC provides a wakeup function that causes the MCU to transition from Software Standby mode or Snooze mode to normal operation. The wakeup function is used to generate a wakeup interrupt signal when the received data matches the address set as the wakeup interrupt source, and while PCLKB is stopped (PCLKB asynchronous operation). This wakeup interrupt signal becomes a trigger for the MCU to transition to normal operation. After the wakeup interrupt occurs, switch the IIC to PCLKB synchronous operation so that the communication can continue.

The wakeup function has four operation modes:

- Normal wakeup mode 1
- Normal wakeup mode 2
- Command recovery mode
- EEP response mode.

Table 29.9 describes the behavior in these modes.

Table 29.9 Wakeup operation modes (1 of 2)

Operation mode	ACK response timing	ACK response before wakeup to PCLKB synchronous operation	SCL state during wakeup to PCLKB synchronous operation
Normal wakeup mode 1	Before wakeup to PCLKB synchronous operation*1	ACK	Fixed low
Normal wakeup mode 2	After wakeup to PCLKB synchronous operation*2	Before wakeup: no response (NACK level retained) After wakeup: ACK response	Fixed low
Command recovery mode	Before wakeup to PCLKB synchronous operation*1	ACK	Open

Table 29.9 Wakeup operation modes (2 of 2)

Operation mode	ACK response timing	ACK response before wakeup to PCLKB synchronous operation	SCL state during wakeup to PCLKB synchronous operation
EEP response mode	Before recovery to PCLKB synchronous operation*1	NACK	Open

Note 1. Switching timing from PCLKB asynchronous operation to PCLKB synchronous operation is the falling edge of the ninth clock of the SCL.
Note 2. Switching timing from PCLKB asynchronous operation to PCLKB synchronous operation is the falling edge of the eighth clock of the SCL.

The following can be selected as wakeup interrupt sources:

- Host address detection (valid when ICSER.HOAE = 1)
- General call address detection (valid when ICSER.GCAE = 1)
- Slave address 0 *1 detection (valid when ICSER.SAR0E = 1)
- Slave address 1 *1 detection (valid when ICSER.SAR1E = 1)
- Slave address 2 *1 detection (valid when ICSER.SAR2E = 1).

Note 1. Only 7-bit address can be set. Set the FS bit in SARUy (y = 0 to 2) to 0.

Precautions on the use of the wakeup function

- Do not change the registers in the IIC except the WUSEN bit in ICWUR2 while the WUASYF flag in ICWUR2 is 1 (during PCLKB asynchronous operation)
- Set ICWUR.WUE and ICWUR.WUIE to 1, and ICCR2.MST and ICCR2.TRS to 0 (slave reception mode) before switching to PCLKB asynchronous mode
- The device ID and the 10-bit slave address cannot be selected for the wakeup interrupt source. Set the DIDE bit in ICSER and FS bit in SARUy (y = 0 to 2) to 0.
- Set bits TIE, TEIE, RIE, NAKIE, SPIE, STIE, ALIE, and TMOIE in the ICIER register to 0 (interrupt disabled) before switching to the asynchronous operation
- Do not use the timeout function when the wakeup function is enabled (ICWUR.WUE = 1)
- Even when a wakeup interrupt is generated during PCLKB asynchronous operation (when ICWUR2.WUASYF = 1), if the slave addresses match in PCLKB synchronous mode (ICWUR2.WUASYF = 0), the wakeup interrupt does not occur and the WUF flag is not set.
- If the timing of writing 0 to the ICWUR2.WUSEN bit and the timing of detecting a start condition conflict, the IIC might start the next reception in PCLKB synchronous operation mode. In this case, ICWUR2.WUASYF flag becomes 1 (switch to PCLKB asynchronous mode) when the data communication is complete, a stop condition is detected, and detection of a wakeup event starts.
- After writing 0 to the WUSEN bit in ICWUR2, do not change registers relate to the IIC operation mode setting (ICMR3, ICSER, and SARLy) until the mode is switched to PCLKB asynchronous operation from PCLKB synchronous operation (while the ICWUR2.WUASYF flag is 1). If the register value changes during this period by an interrupt handling or another factor, the IIC might malfunction before switching to the asynchronous operation.

29.8.1 Normal Wakeup Mode 1

This section describes the behavior, the timing, and a use case of normal wakeup mode 1.

1. A wakeup interrupt triggered by the match of the slave address initiates the transition to normal operation as follows:

   Before wakeup: ACK is sent in response to the data received with its own slave address of the IIC.
   During wakeup: ACK response is made on the ninth clock cycle of SCL, and SCL is held low afterwards.*1
   After wakeup: Normal operation continues.

   If the slave address does not match, the SCL line is not held low after the fall of the ninth clock cycle of SCL, and the slave operation continues. Figure 29.32 provides detailed timing. For a use case, see Figure 29.30.

Note 1. Between the ninth clock cycle and first clock cycle during wakeup, WAIT = 1 does not work.

2. If the transition from Software Standby mode or Snooze mode is triggered by an interrupt other than a wakeup interrupt, for example IRQn, the WUF flag is not set to 1. Follow the processing shown in Figure 29.31.

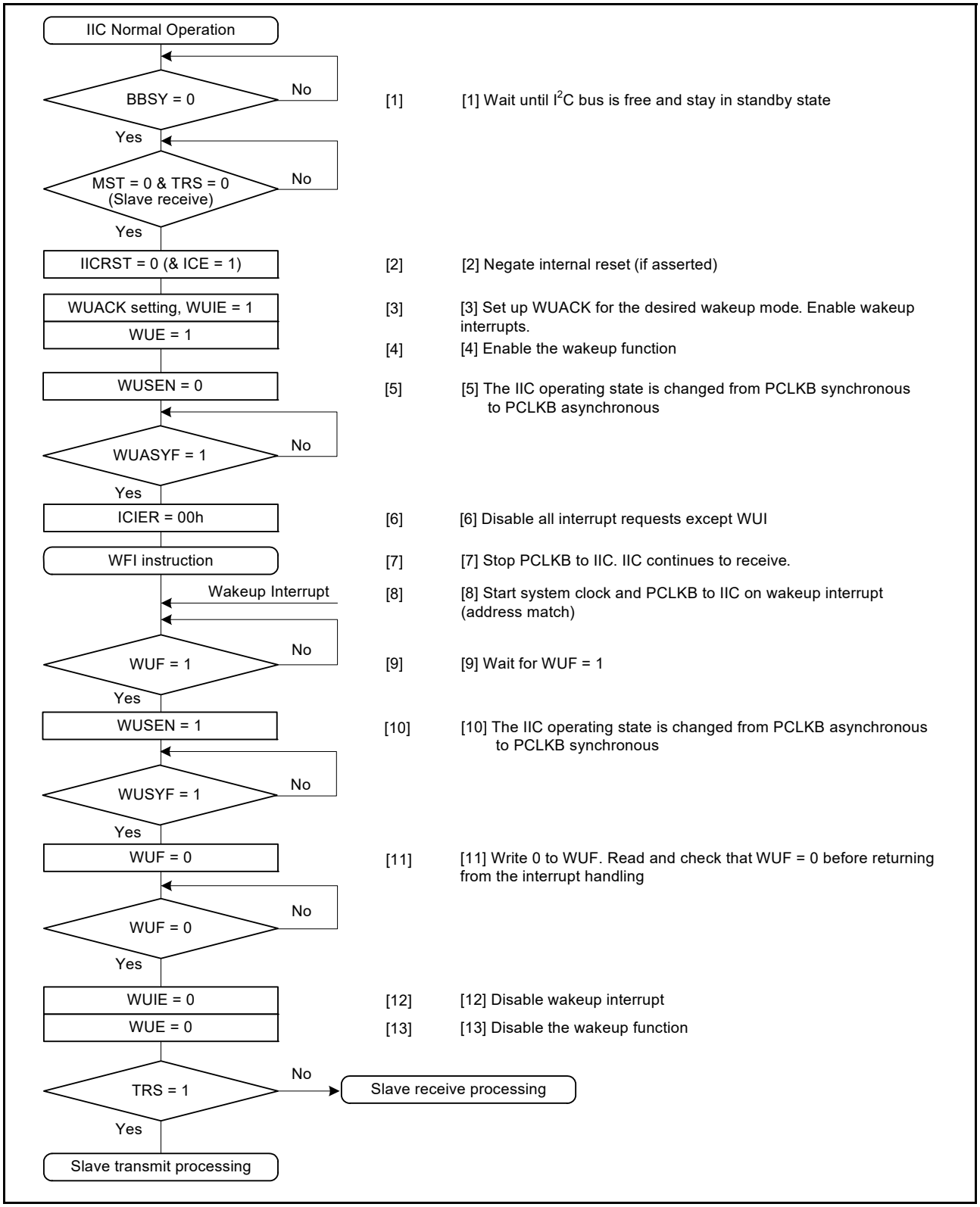
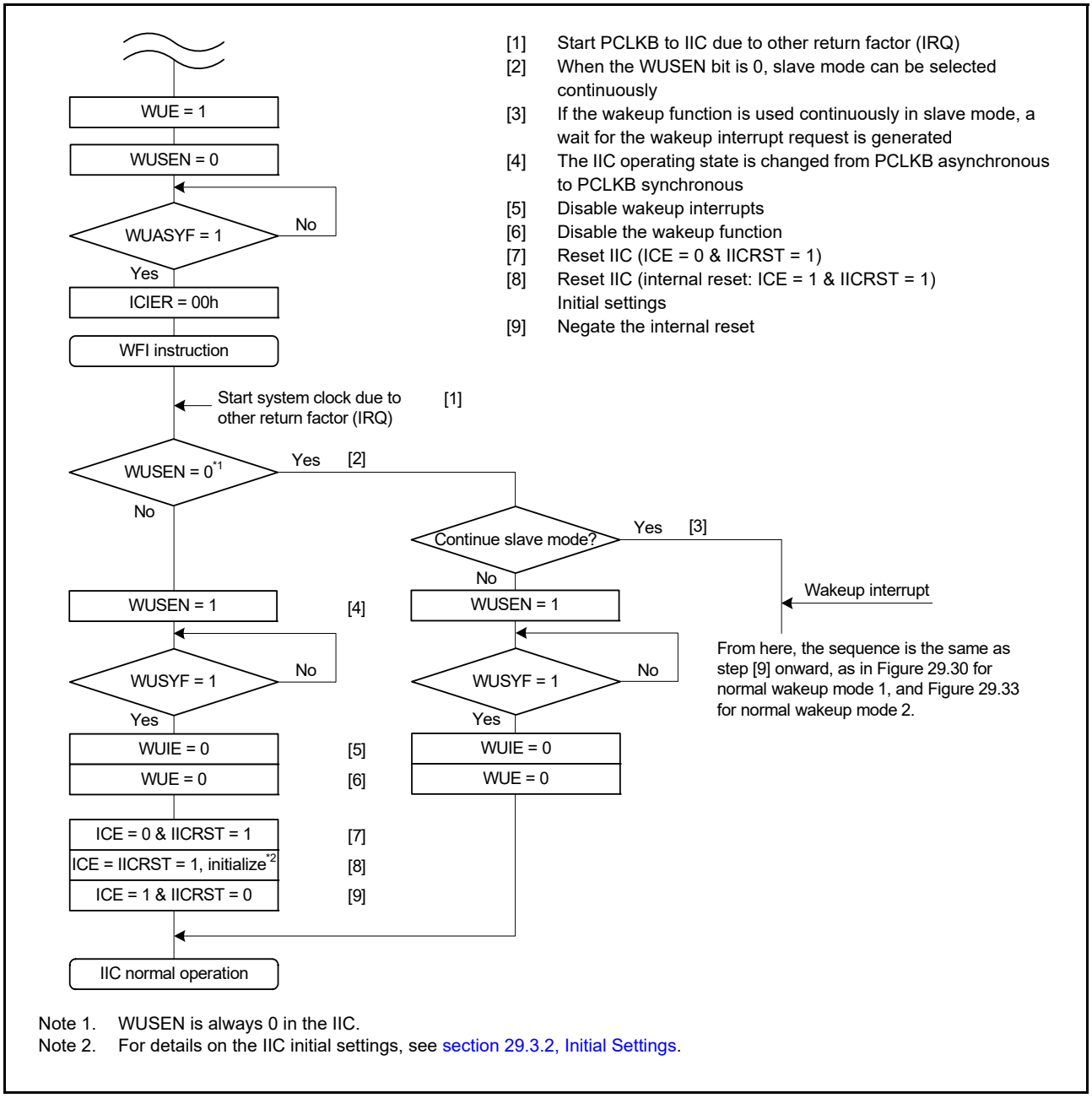


Figure 29.30 Example operation of normal wakeup mode 1 when wakeup is triggered by a wakeup interrupt on match of the slave address



Note 1. WUSEN is always 0 in the IIC.
Note 2. For details on the IIC initial settings, see section 29.3.2, Initial Settings.

Figure 29.31 Example operation of normal wakeup modes 1 and 2 when wakeup by an interrupt other than IIC wakeup interrupt, for example IRQn

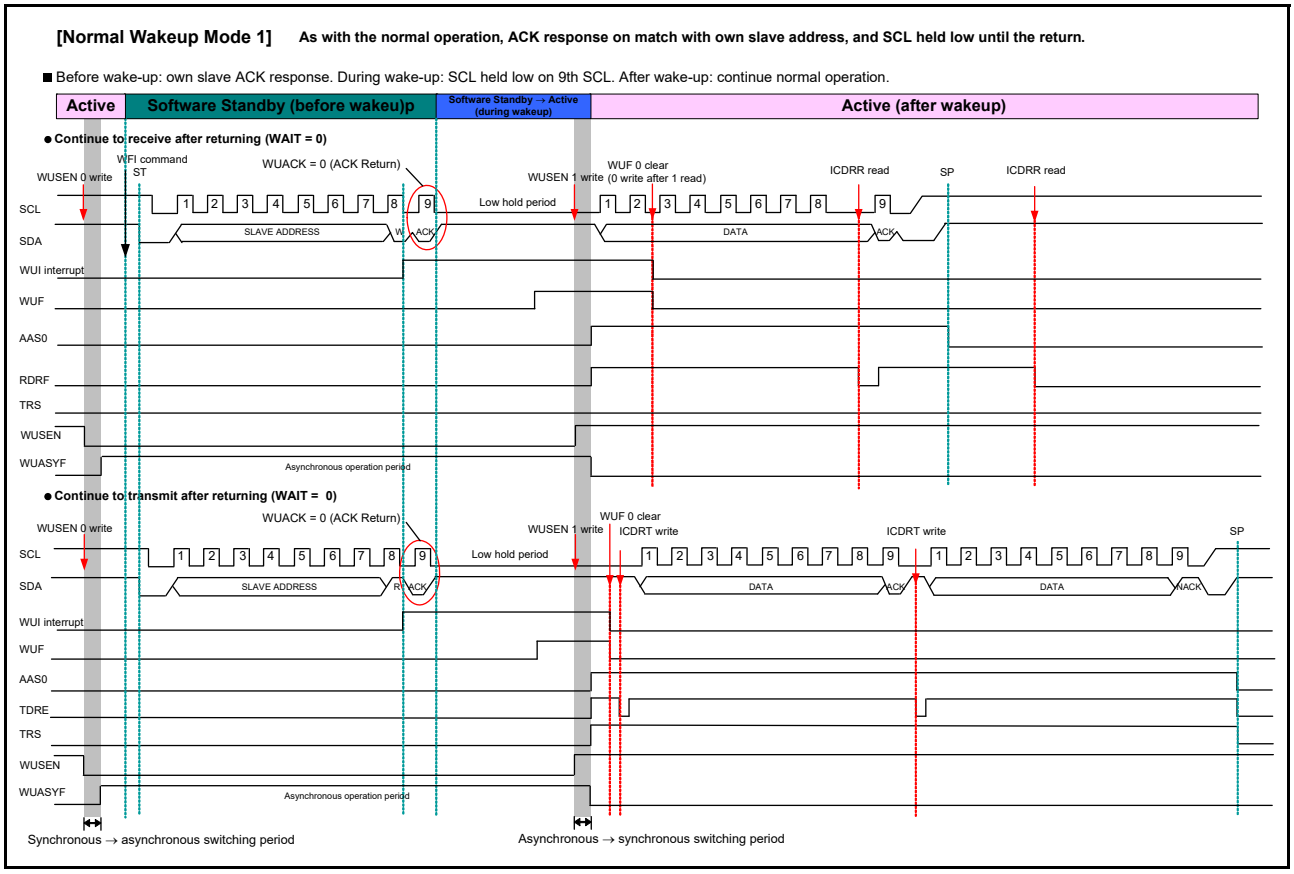


Figure 29.32 Timing of normal wakeup mode 1

29.8.2 Normal Wakeup Mode 2

This section describes the behavior, the timing, and a use case of normal wakeup mode 2.

1. A wakeup interrupt triggered by the match of the slave address initiates the transition to normal operation as follows:

   Before wakeup: No response to the data received with its own slave address of the IIC until the end of the eighth SCL cycle

   During wakeup: SCL line held low during the eighth and ninth clock cycles.

   After wakeup: ACK returns on the ninth clock cycle of SCL, and normal operation continues.

   If the slave address does not match, the SCL line is not held low after the fall of the eighth SCL clock cycle, and the slave operation continues. Figure 29.34 provides detailed timing. For a use case, see Figure 29.33.

2. If the transaction from Software Standby mode or Snooze mode is triggered by an interrupt other than a wakeup interrupt, for example IRQ. WUF is not set to 1. Follow the processing shown in Figure 29.31.

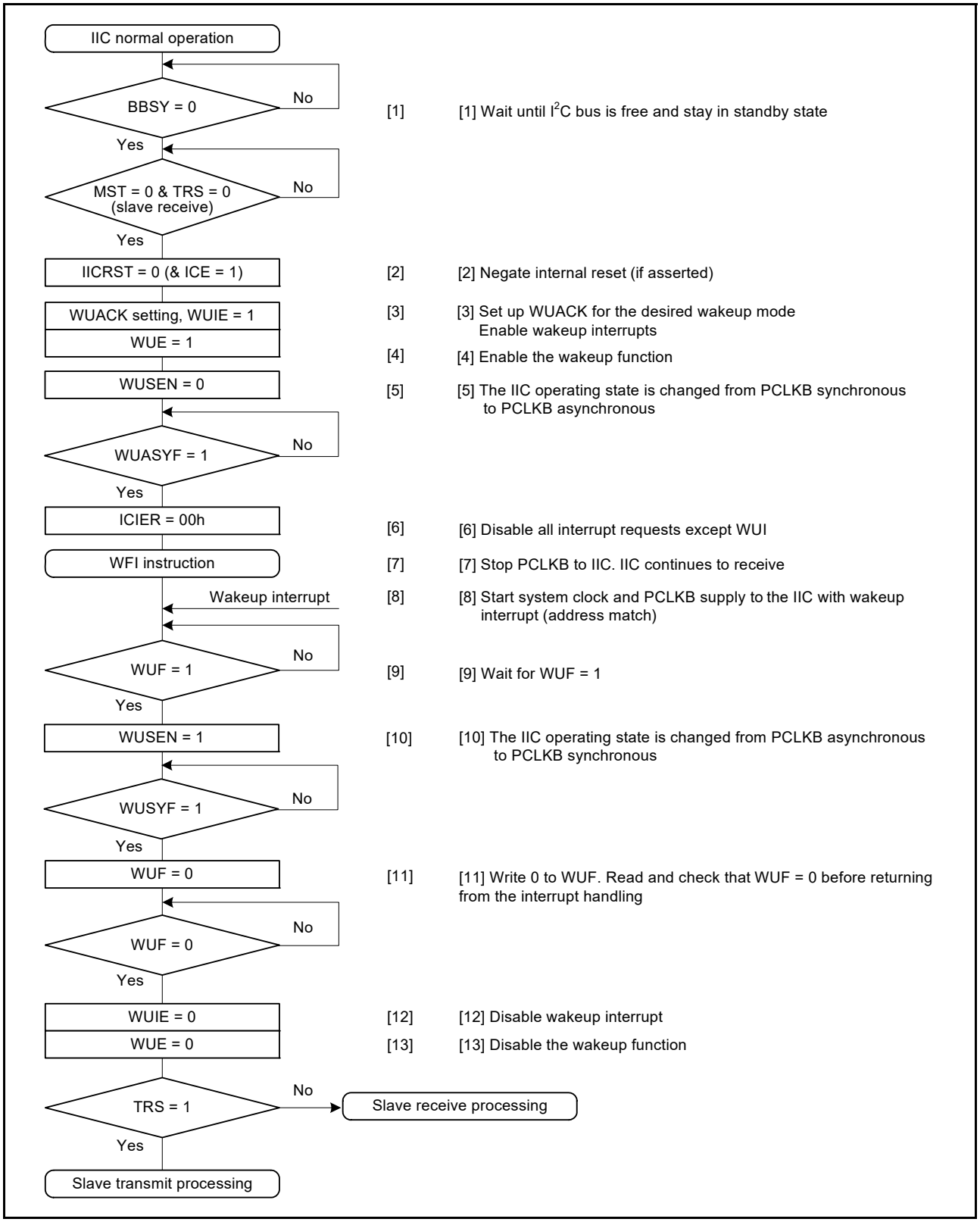


Figure 29.33 Example operation of normal wakeup mode 2 when wakeup is triggered by a wakeup interrupt on match of the slave address

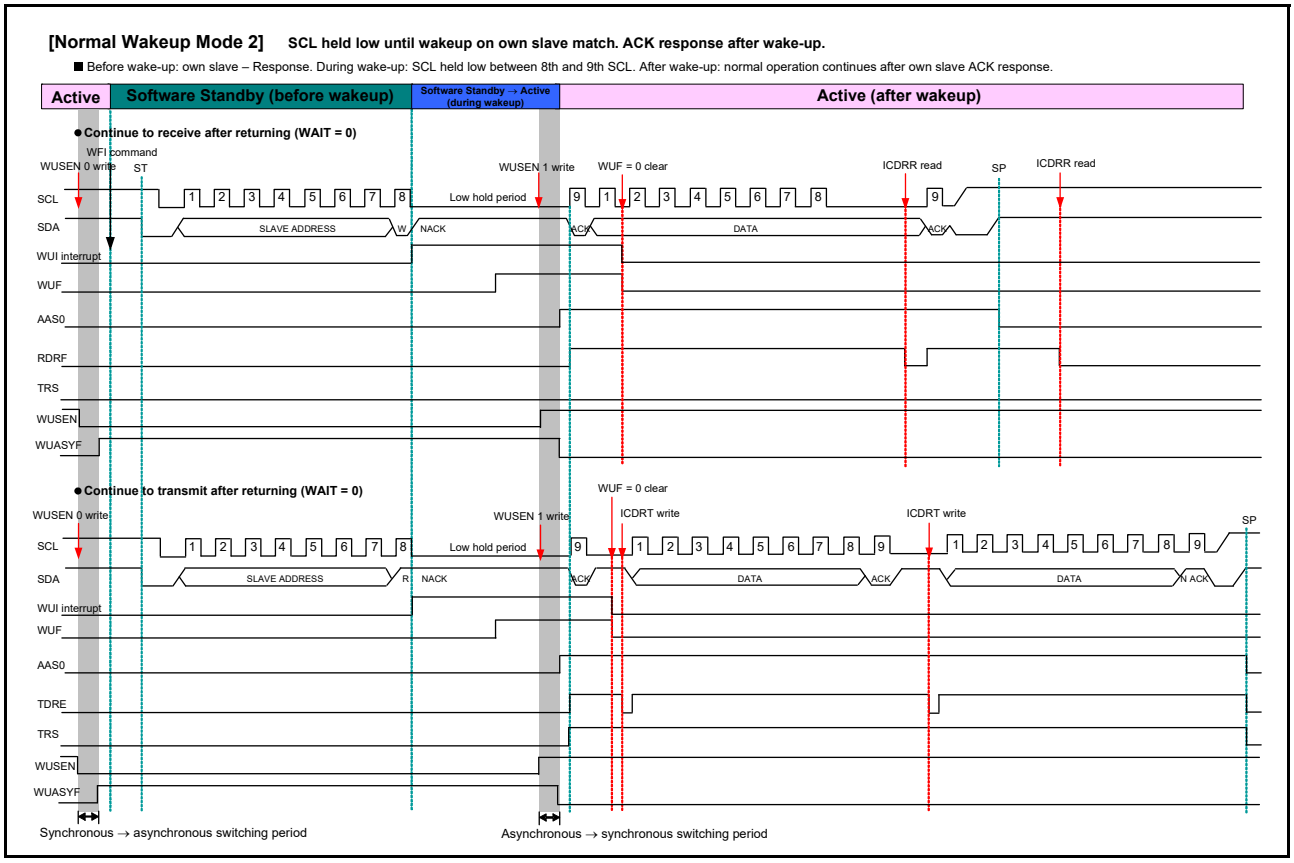


Figure 29.34 Timing of normal wakeup mode 2

29.8.3 Command Recovery Mode and EEP Response Mode (Special Wakeup Modes)

In the command recovery and EEP response modes, the SCL line is not held low during the wakeup period (after the rise of the ninth clock cycle of SCL), so other IIC devices can use the I2C bus during this period.

This section describes the behavior, the timing, and use cases of the command recovery and EEP response modes.

1. A wakeup interrupt triggered by the match of the slave address initiates the transition to normal operation as follows:

   Before wakeup: In response to the data received with its own slave address of the IIC, ACK (command recovery mode) or NACK (EEP response mode) is returned.

   During wakeup: The SCL line is not held low.

   After wakeup: Normal operation continues after the IIC initial settings.

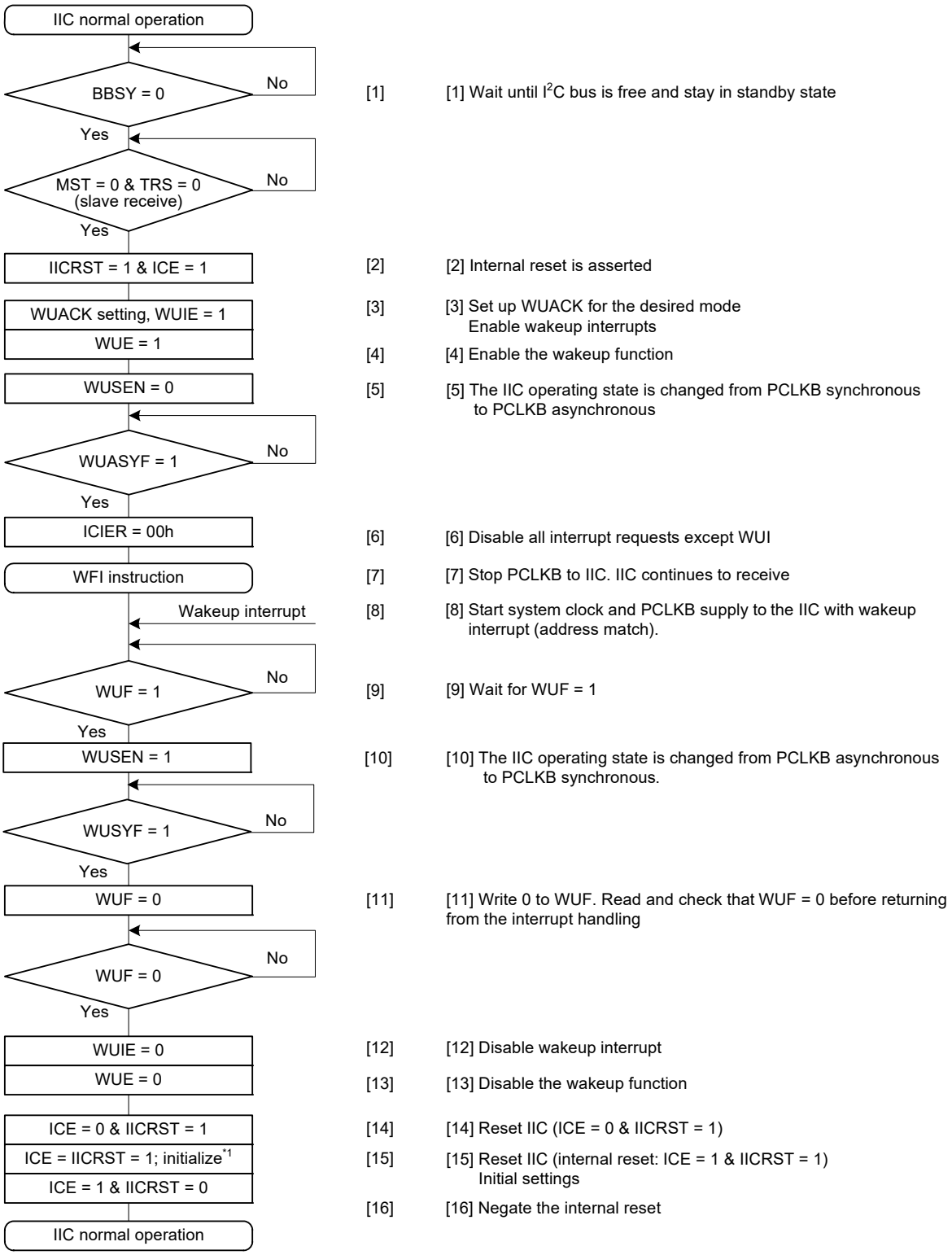
   If the slave address does not match, the slave operation continues.

Note 1. Because the SCL line is not held low during wakeup, transmission or reception of the data that follows the slave address is not possible.

Note 2. The command recovery and EEP response modes are internal reset states (ICE = IICRST = 1). Therefore, the match of the slave address does not set the ICSR1 register flags HOA, GCA, AAS0, AAS1, and AAS2.

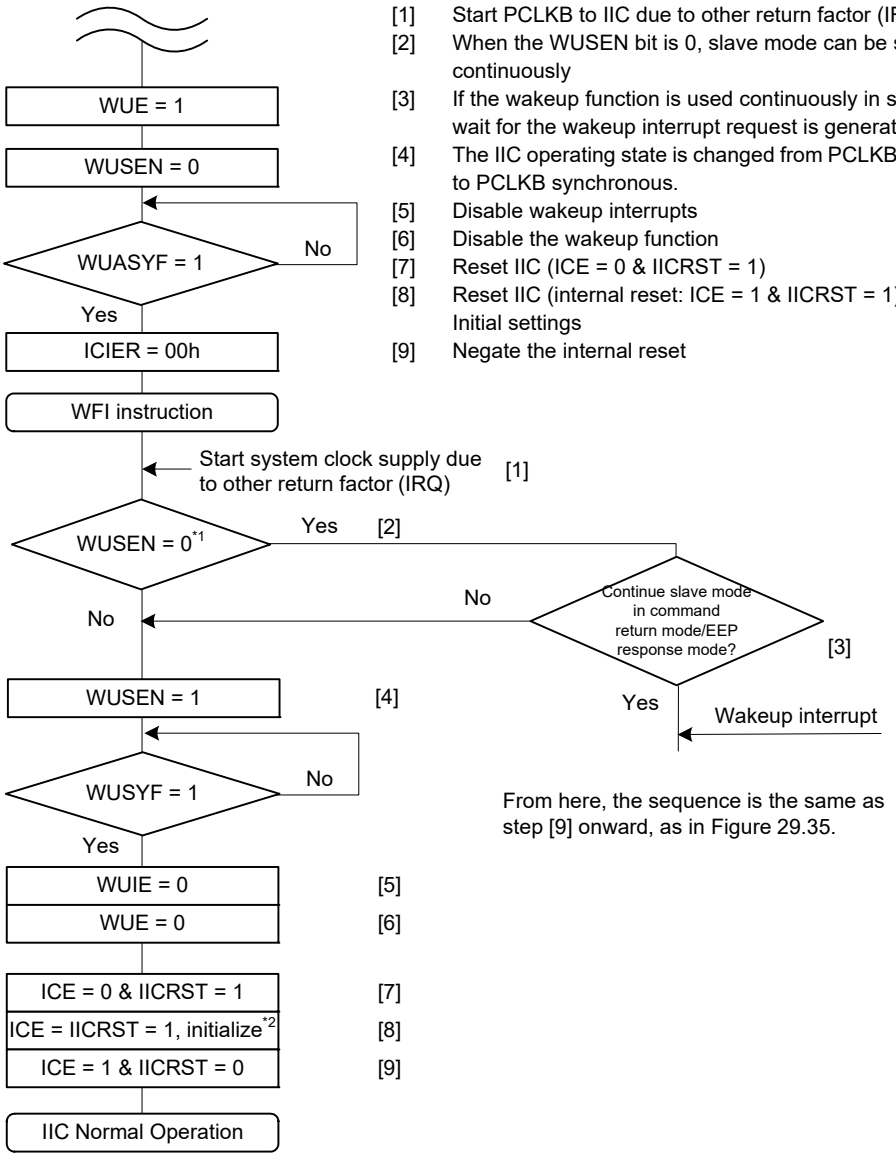
Figure 29.37 provides detailed timing. For a use case, see Figure 29.35.

2. If the transaction from Software Standby mode or Snooze mode is triggered by the interrupt, for example IRQn, other than a wakeup interrupt. WUF is not set in this case. Follow the processing shown in Figure 29.36.



Note 1. For details on the IIC initial settings, see section 29.3.2, Initial Settings.

Figure 29.35 Example operation of command recover mode and EEP response mode when wakeup is triggered by a wakeup interrupt on match of the slave address



[1] Start PCLKB to IIC due to other return factor (IRQ)
[2] When the WUSEN bit is 0, slave mode can be selected continuously
[3] If the wakeup function is used continuously in slave mode, a wait for the wakeup interrupt request is generated.
[4] The IIC operating state is changed from PCLKB asynchronous to PCLKB synchronous.
[5] Disable wakeup interrupts
[6] Disable the wakeup function
[7] Reset IIC (ICE = 0 & IICRST = 1)
[8] Reset IIC (internal reset: ICE = 1 & IICRST = 1)
Initial settings
[9] Negate the internal reset

Note 1. WUSEN is always 0 in the IIC.
Note 2. For details on the IIC initial settings, see section 29.3.2, Initial Settings.

Figure 29.36 Example operation of command recover mode and EEP response mode when wakeup is triggered by an interrupt other than IIC wakeup interrupt, for example IRQn

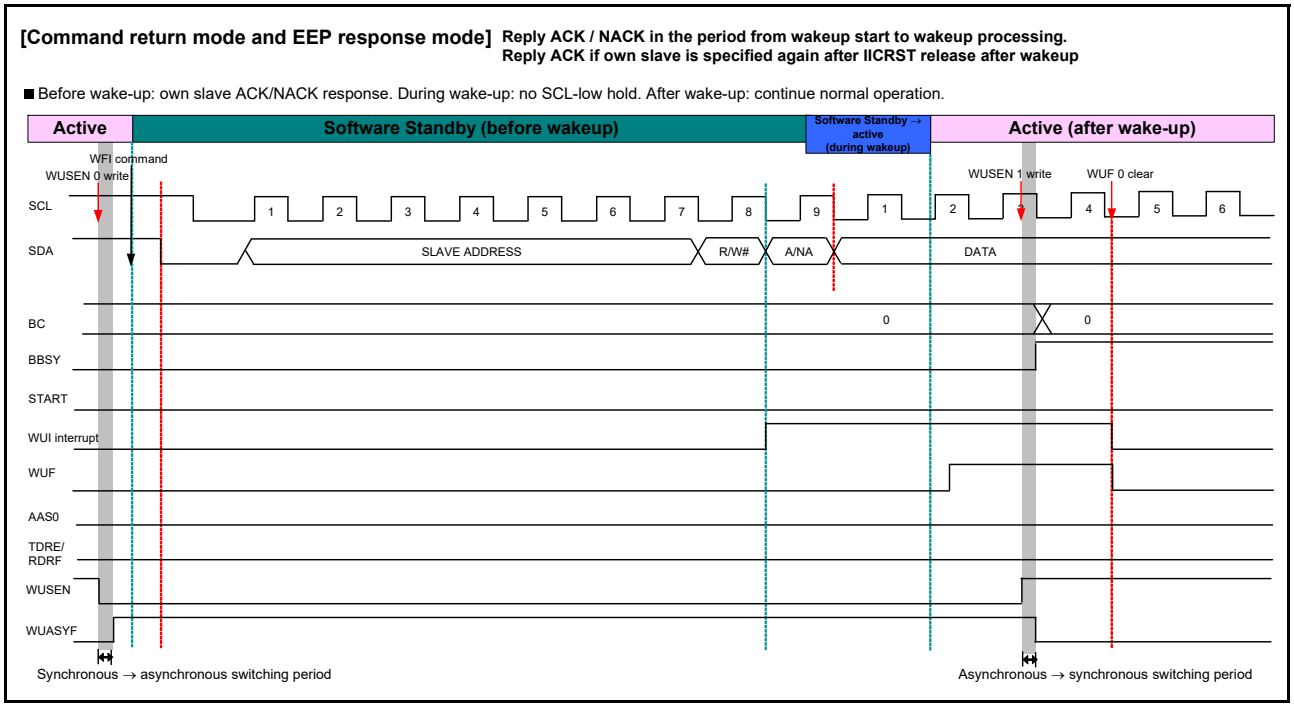


Figure 29.37 Timing of command recovery and EEP response modes

29.9 Automatic Low-Hold Function for SCL

29.9.1 Function to Prevent Wrong Transmission of Transmit Data

If the I2C Bus Shift Register (ICDRS) is empty when data has not been written to the IIC Bus Transmit Data Register (ICDRT) with the IIC in transmission mode (TRS bit = 1 in ICCR2), the SCLn line is automatically held low over the subsequent intervals. This low-hold period is extended until the transmit data is written, which prevents the unintended transmission of erroneous data.

Master transmit mode:

- Low-level interval after a start or restart condition is issued
- Low-level interval between the ninth clock cycle of one transfer and the first clock cycle of the next.

Slave transmit mode:

- Low-level interval between the ninth clock cycle of one transfer and the first clock cycle of the next.

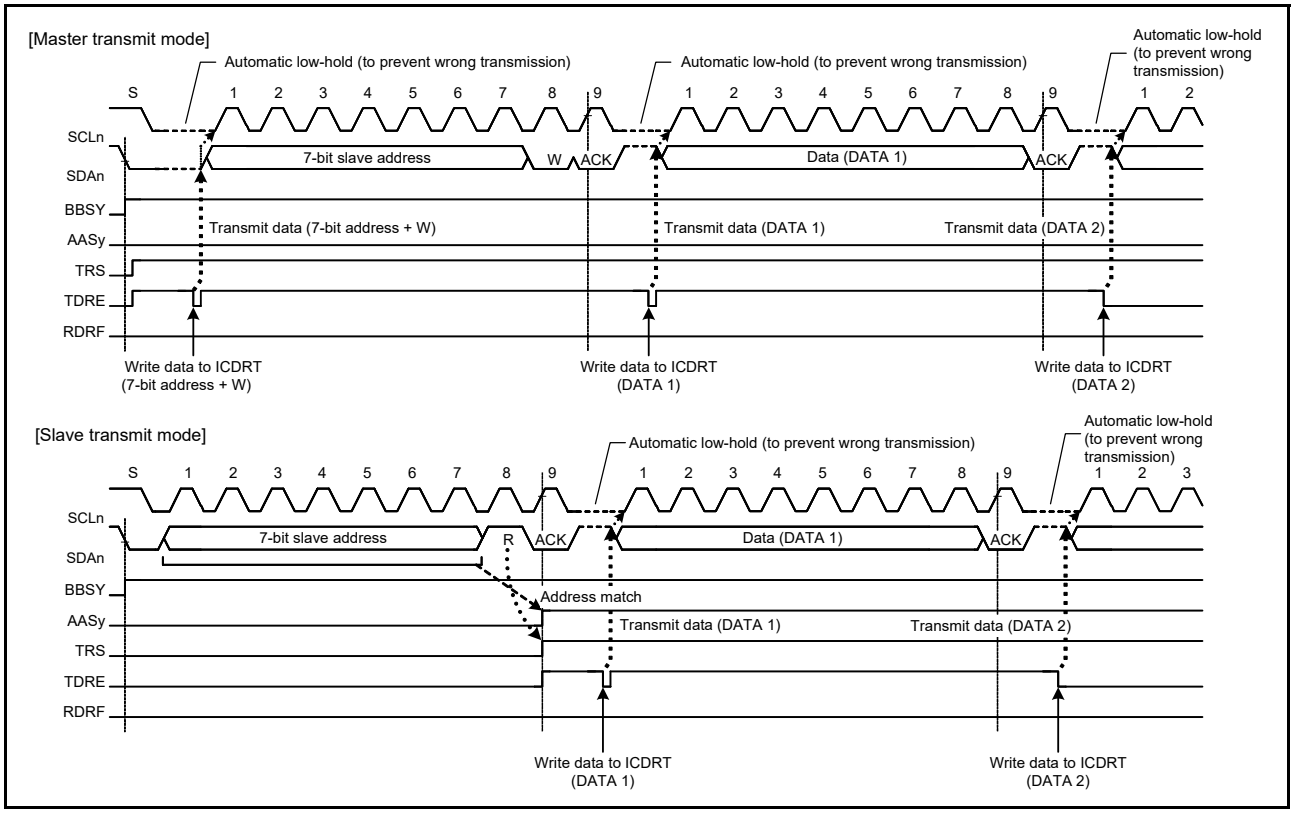


Figure 29.38 Automatic low-hold operation in transmit mode

29.9.2 NACK Reception Transfer Suspension Function

This function suspends transfer operation when NACK is received in transmit mode (TRS bit = 1 in ICCR2). This function is enabled when the NACKE bit in ICFER is set to 1. If the next transmit data is already written (TDRE flag = 0 in ICSR2) when NACK is received, the next data transmission on the falling edge of the ninth SCL clock cycle is automatically suspended. This prevents the SDAn line output level from being held low when the MSB of the next transmit data is 0.

If the transfer operation is suspended by this function (NACKF flag = 1 in ICSR2), transmit and receive operations are discontinued. To restore transmit and receive operation, set the NACKF flag to 0. In master transmit mode, after issuing a restart or stop condition, set the NACKF flag to 0, and then issue a start condition again.

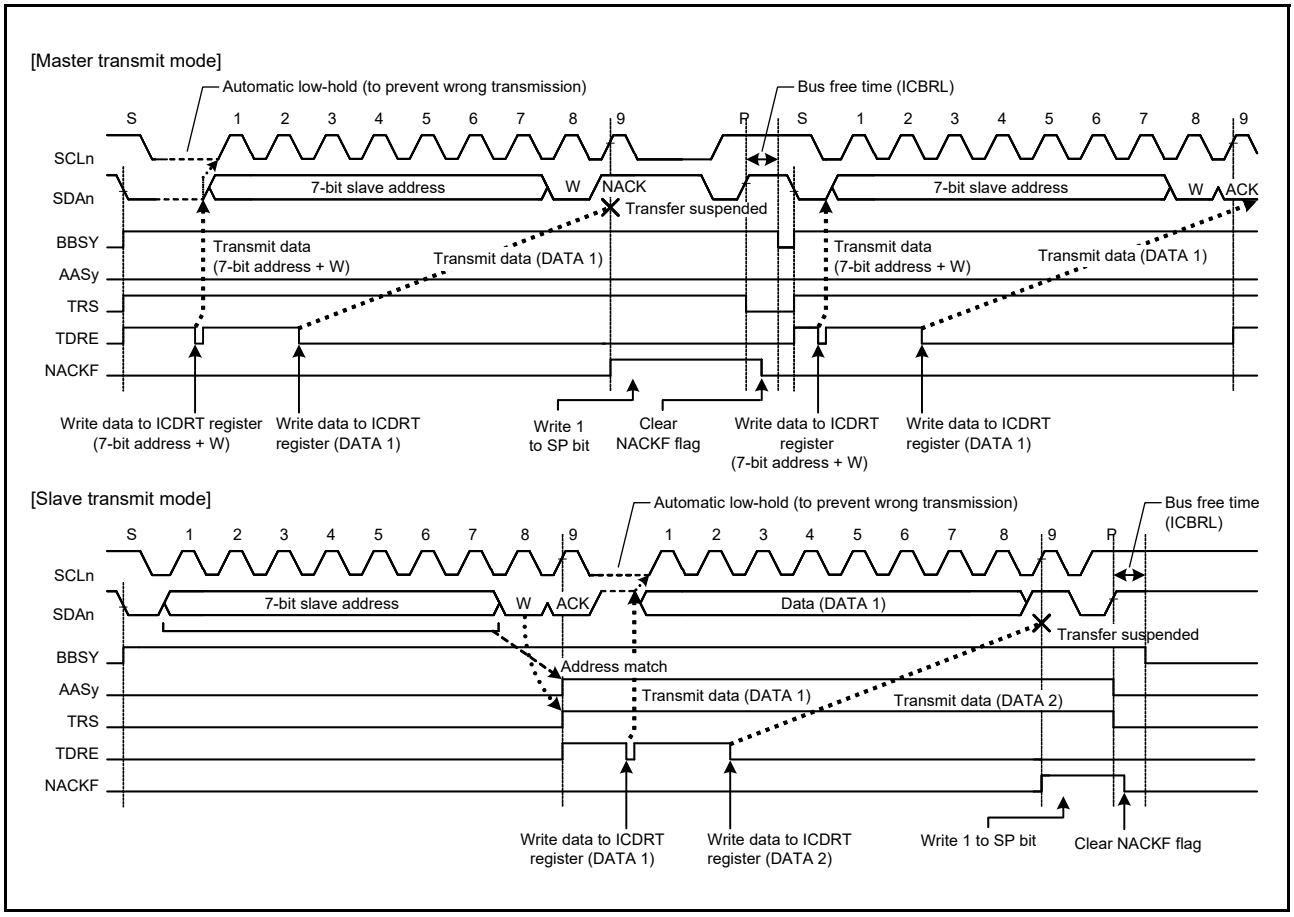


Figure 29.39 Suspension of data transfer when NACK is received (NACKE = 1)

29.9.3 Function to Prevent Failure to Receive Data

If response processing when receive data (ICDRR) read is delayed for a period of one transfer frame or more with receive data full (RDRF flag = 1 in ICSR2) in receive mode (TRS = 0 in ICCR2), the IIC holds the SCLn line low automatically immediately before the next data is received to prevent failure to receive data.

This function is enabled even if the read processing of the final receive data is delayed and, in the meantime, the IIC slave address is designated after a stop condition is issued. This function does not interfere with other communication because the IIC does not hold the SCLn line low when a mismatch with its own slave address occurs after a stop condition is issued.

Periods in which the SCLn line is held low can be selected with a combination of the WAIT and RDRFS bits in ICMR3.

(1) 1-byte receive operation and automatic low-hold function using the WAIT bit

When the WAIT bit in ICMR3 is set to 1, the IIC performs a 1-byte receive operation using the WAIT bit function. Additionally, when the ICMR3.RDRFS bit is 0, the IIC automatically sends the ACKBT bit value in ICMR3 for the acknowledge bit in the period from the falling edge of the eighth SCL clock cycle to the falling edge of the ninth SCL clock cycle, and automatically holds the SCLn line low on the falling edge of the ninth SCL clock cycle using the WAIT bit function. This low-hold is released by reading data from ICDRR, which enables byte-wise receive operation.

The WAIT bit function is enabled for receive frames after a match with the IIC slave address, including the general call address and host address, is obtained in master receive mode or slave receive mode.

(2) 1-byte receive operation (ACK/NACK transmission control) and automatic low-hold function using the RDRFS bit

When the RDRFS bit in ICMR3 is set to 1, the IIC performs a 1-byte receive operation using the RDRFS bit function. When the RDRFS bit is set to 1, the RDRF flag in ICSR2 is set to 1 (receive data full) on the rising edge of the eighth

SCL clock cycle, and the SCLn line is automatically held low on the falling edge of the eighth SCL clock cycle. This low-hold is released by writing a value to the ACKBT bit in ICMR3, but cannot be released by reading data from ICDRR, which enables receive operation through the ACK or NACK transmission control based on the data received in byte units.

The RDRFS bit function is enabled for receive frames after a match with the IIC slave address, including the general call address and host address, is obtained in master receive mode or slave receive mode.

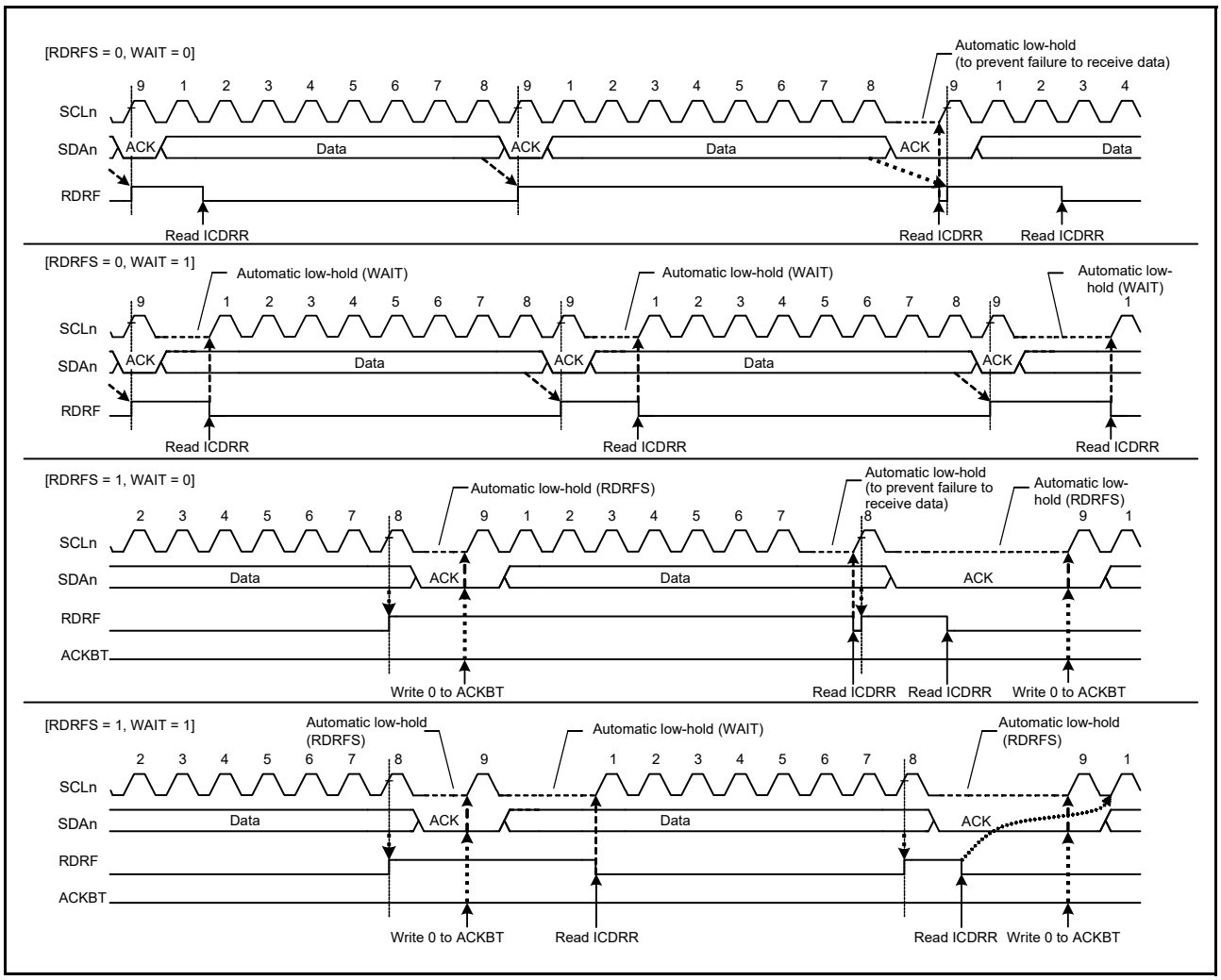


Figure 29.40 Automatic low-hold operation in receive mode using RDRFS and WAIT bits

29.10 Arbitration-Lost Detection Functions

In addition to the normal arbitration-lost detection function defined by the I2C bus standard, the IIC has functions to prevent double-issue of a start condition, detect arbitration-lost during transmission of NACK, and detect arbitration-lost in slave transmit mode.

29.10.1 Master Arbitration-Lost Detection (MALE Bit)

The IIC drives the SDAn line low to issue a start condition. However, if the SDAn line was already driven low by another master device issuing a start condition, the IIC regards its own start condition as an error and considers this a loss in arbitration. Priority is given to transfer by the other master device. Similarly, if a request to issue a start condition is made by setting the ST bit in ICCR2 to 1 while the bus is busy (BBSY flag = 1 in ICCR2), the IIC regards this as a double-issuing-of-start-condition error and considers itself to have lost the arbitration. This prevents a failure of transfer resulting from a start condition being issued while transfer is in progress.

When a start condition is issued successfully, if the transmit data including the address bits (internal SDA output level) and the level on the SDAn line do not match (high output as the internal SDA output, meaning the SDAn pin is in the

high-impedance state) and a low level is detected on the SDAn line, the IIC loses in arbitration.

After a loss in arbitration of mastership, the IIC immediately enters slave receive mode. If a slave address, including the general call address, matches its own address at this time, the IIC continues in slave operation.

A loss in arbitration of mastership is detected when the following conditions are met while the MALE bit in ICFER is 1 (master arbitration-lost detection enabled).

[Master arbitration-lost conditions]

- Mismatching of the internal level for output on SDA and the level on the SDAn line after a start condition was issued by setting the ICCR2.ST bit to 1 while the BBSY flag in ICCR2 was set to 0 (erroneous issuing of a start condition)
- Setting the ICCR2.ST bit to 1 (start condition double-issue error) while the BBSY flag is 1.
- When the transmit data excluding acknowledge (internal SDA output level) does not match the level on the SDAn line in master transmit mode (MST and TRS bits = 11b in ICCR2).

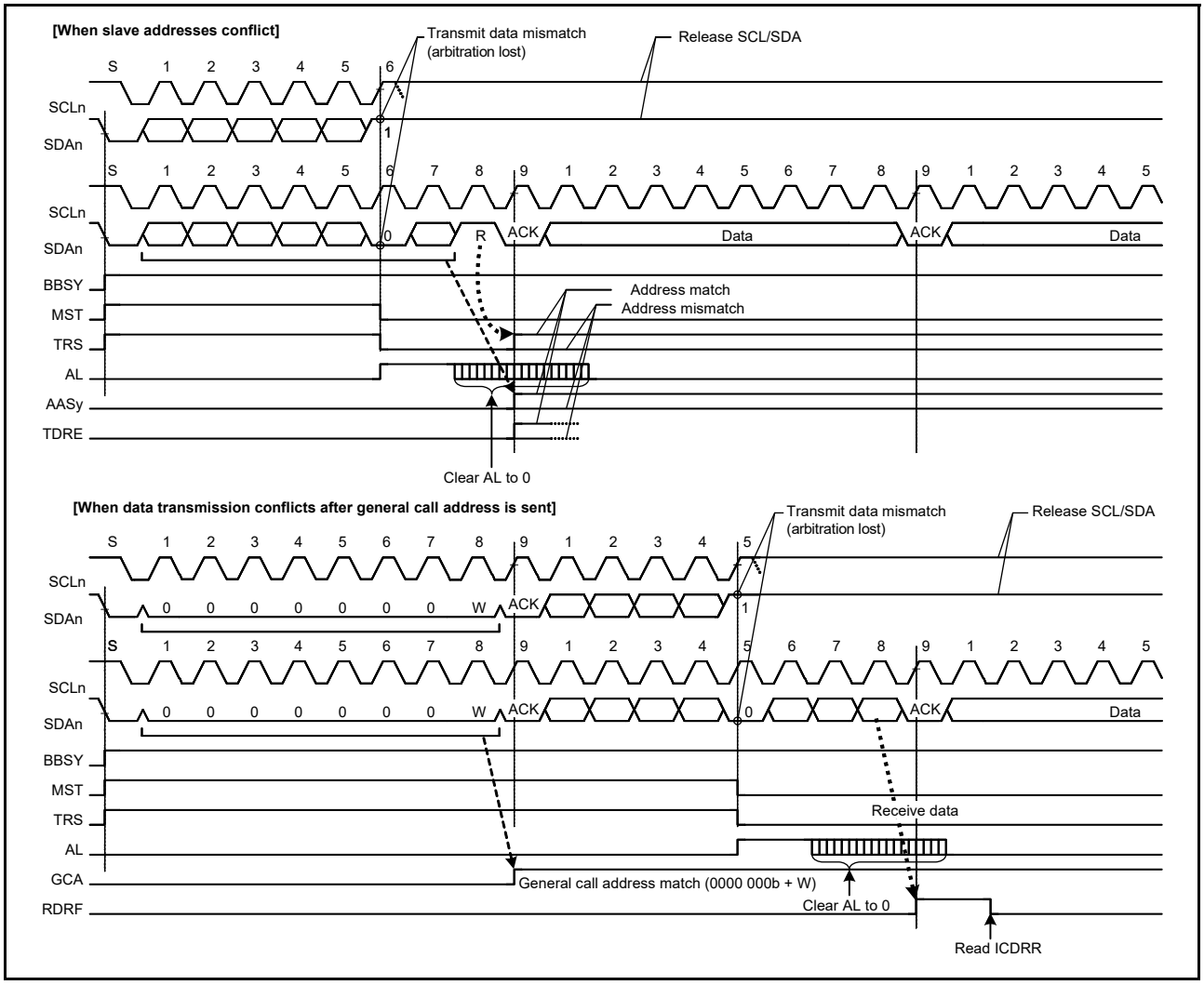


Figure 29.41 Examples of master arbitration-lost detection (MALE = 1)

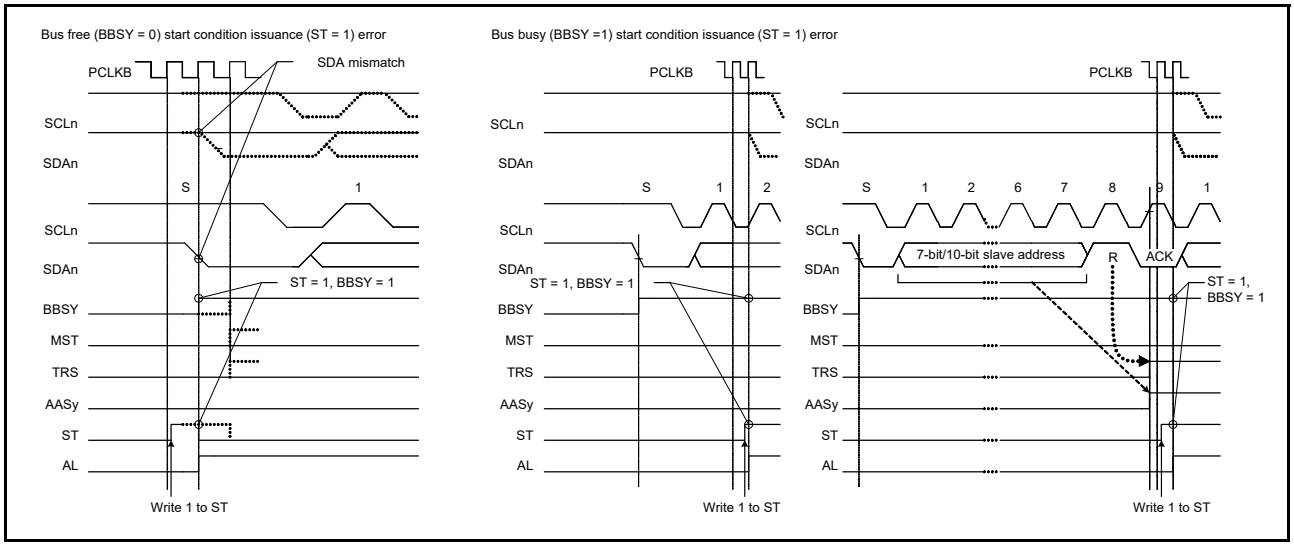


Figure 29.42 Arbitration-lost when start condition is issued (MALE = 1)

29.10.2 Function to Detect Loss of Arbitration during NACK Transmission (NALE Bit)

This function causes arbitration to be lost if the internal SDA output level does not match the level on the SDAn line (high output as the internal SDA output, meaning the SDAn pin is in the high-impedance state) and a low level is detected on the SDAn line during transmission of NACK in receive mode. Arbitration is lost because of a conflict of NACK transmission and ACK transmission when two or more master devices receive data from the same slave device simultaneously in a multi-master system. Such conflict occurs when multiple master devices send or receive the same information through a single slave device. Figure 29.43 shows an example of arbitration-lost detection during transmission of NACK.

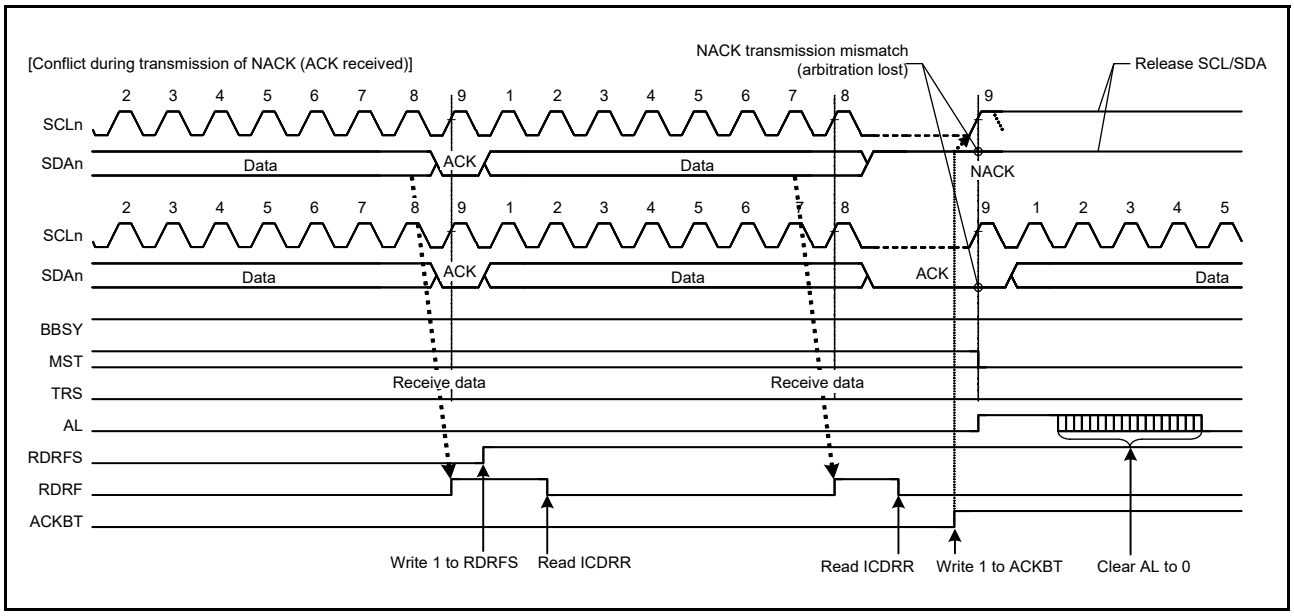


Figure 29.43 Example of arbitration-lost detection during transmission of NACK (NALE = 1)

The following example explains arbitration-lost detection where two master devices (masters A and B) and a single slave device are connected through the bus. In this example, master A receives 2 bytes of data from the slave device, and master B receives 4 bytes of data from the slave device.

If masters A and B access the slave device simultaneously, because the slave address is identical, arbitration is not lost in either master A or B during access to the slave device. Both masters A and B recognize that they obtained the bus mastership and operate as such. Master A sends NACK when it has received 2 final bytes of data from the slave device.

Meanwhile, master B sends ACK because it has not received the necessary 4 bytes of data. At this time, the NACK transmission from master A and the ACK transmission from master B conflict. In general, if a conflict like this occurs, master A cannot detect the ACK transmitted by master B and issues a stop condition. The issuance of the stop condition conflicts with the SCL clock output of master B, which disrupts communication.

When the IIC receives ACK during transmission of NACK, it detects a defeat in conflict with other master devices and causes arbitration to be lost. If arbitration is lost during transmission of NACK, the IIC immediately cancels the slave match condition and enters slave receive mode. This prevents a stop condition from being issued, preventing a communication failure on the bus.

Similarly, in the ARP command processing of SMBus, the function to detect loss of arbitration during transmission of NACK is also available to eliminate the extra clock cycle processing, such as FFh transmission processing, necessary if the UDID (Unique Device Identifier) of the assigned address does not match in the Get UDID general processing after the Assign Address command.

The IIC detects arbitration-lost during transmission of NACK when the following condition is met with the NALE bit in ICFER set to 1 (arbitration-lost detection during NACK transmission enabled).

[Condition for arbitration-lost during NACK transmission]

- When the internal SDA output level does not match the SDAn line (ACK is received) during transmission of NACK (ACKBT bit = 1 in ICMR3).

29.10.3 Slave Arbitration-Lost Detection (SALE Bit)

This function causes arbitration to be lost if the transmit data (internal SDA output level) and the level on the SDAn line do not match (high output as the internal SDA output, meaning the SDAn pin is in the high-impedance state), and a low level is detected on the SDAn line in slave transmit mode. This arbitration-lost detection function is mainly used when transmitting a UDID (Unique Device Identifier) over an SMBus.

When the IIC loses slave arbitration, the IIC is immediately released from the slave-matched state and enters slave receive mode. This function can detect conflicts of data during transmission of UDIDs over an SMBus and eliminates subsequent redundant processing for the transmission of FFh.

The IIC detects slave arbitration-lost when the following condition is met with the SALE bit in ICFER set to 1 (slave arbitration-lost detection enabled).

[Condition for slave arbitration-lost]

- When transmit data excluding acknowledge (internal SDA output level) does not match the SDAn line in slave transmit mode (MST and TRS bits = 01b in ICCR2).

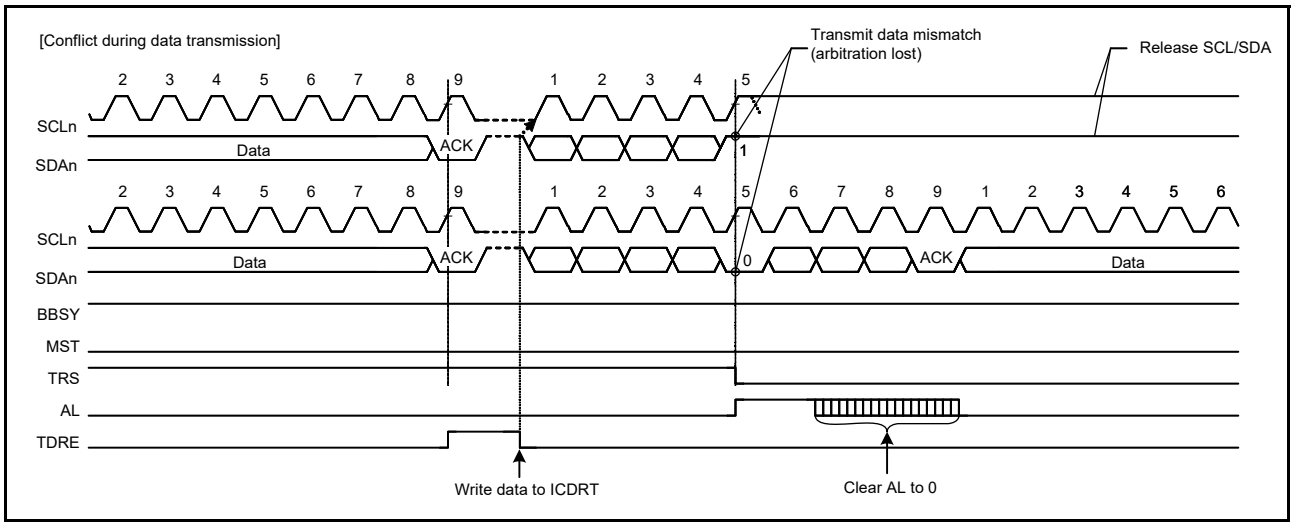


Figure 29.44 Example of slave arbitration-lost detection (SALE = 1)

29.11 Start, Restart, and Stop Condition Issuing Function

29.11.1 Issuing a Start Condition

The IIC issues a start condition when the ST bit in the ICCR2 register is set to 1. When the ST bit is set to 1, a start condition request is made, and the IIC issues a start condition when the BBSY flag in ICCR2 is 0 (bus free state). When a start condition is issued normally, the IIC automatically shifts to the master transmit mode.

To issue a start condition:

1. Drive the SDAn line low (high level to low level).
2. Ensure that the time set in ICBRH.BRH[4:0] and the start condition hold time elapse.
3. Drive the SCLn line low (high level to low level).
4. Detect low level of the SCLn line and ensure the low-level period of the SCLn line set in ICBRL.BRL[4:0] elapses.

29.11.2 Issuing a Restart Condition

The IIC issues a restart condition when the RS bit in ICCR2 is set to 1. When the RS bit is set to 1, a restart condition request is made, and the IIC issues a restart condition when the BBSY flag in ICCR2 is 1 (bus busy state) and the MST bit in ICCR2 is 1 (master mode).

To issue a restart condition:

1. Release the SDAn line.
2. Ensure the low-level period of SCLn line set in ICBRL.BRL[4:0] elapses.
3. Release the SCLn line (low level to high level).
4. Detect a high level on the SCLn line and ensure the time set in ICBRL.BRL[4:0] and the restart condition setup time elapse.
5. Drive the SDAn line low (high level to low level).
6. Ensure the time set in ICBRH.BRH[4:0] and the restart condition hold time elapse.
7. Drive the SCLn line low (high level to low level).
8. Detect a low level on the SCLn line and ensure the low-level period of SCLn line set in ICBRL.BRL[4:0] elapses.

Note: When issuing restart condition requests, write the slave address to ICDRT after confirming that ICCR2.RS = 0. Data written while ICCR2.RS = 1 is not forwarded because of the retransmission condition before the occurrence.

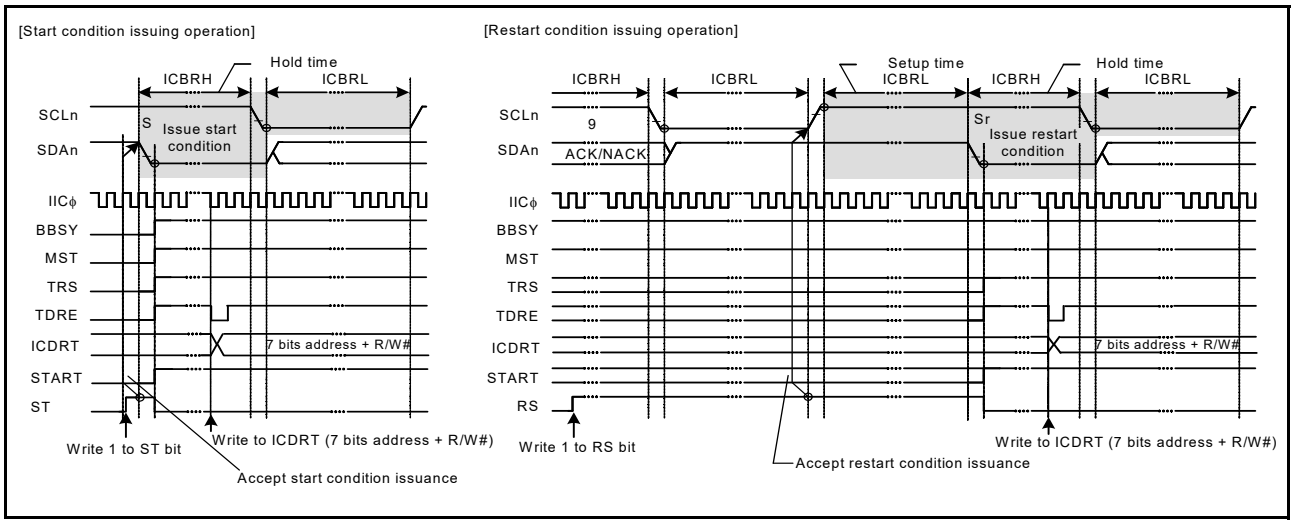


Figure 29.45 Start and restart condition issue timing using the ST and RS bits

Figure 29.46 shows the operation timing when a restart condition is issued after the master transmission.

[Restart condition issuance after the master transmission]

1. Initial setting. For details, see section 29.3.2, Initial Settings.
2. Read the IICR2.BBSY flag to check that the bus is free, then set the ICCR2.ST bit to 1 (start condition issuance request). On receiving the request, the IIC issues a start condition. At the same time, the ICSR2.BBSY flag and ICSR2.START flag are automatically set to 1 and the ST bit is automatically set to 0. If the start condition is detected and the internal levels for the SDA output state and the levels on the SDAn line have matched while the ST bit is 1, the IIC recognizes that issuing of the start condition as requested by the ST bit has successfully completed. The MST and TRS bits in ICCR2 are automatically set to 1, placing the IIC in master transmit mode. The TDRE flag in ICSR2 is also automatically set to 1 in response to setting of the ICCR2.TRS bit to 1.
3. Check that the ICSR2.TDRE flag is 1, then write the value for transmission (the slave address and the R/W# bit) to the ICDRT register. After the transmit data are written to the ICDRT register, the TDRE flag is automatically set to 0, the data is transferred from the ICDRT register to the ICDRS register, and the TDRE flag is again set to 1. After the byte containing the slave address and R/W# bit has been transmitted, the value of the TRS bit is automatically updated to select master transmit or master receive mode according to the value of the transmitted R/W# bit. If the value of the R/W# bit was 0, the IIC continues in master transmit mode. If the NACKF.ICSR2 flag is 1 at this time, indicating that no slave device recognized the address or there was an error in communications, write 1 to ICCR2.SP bit to issue a stop condition.

   To transmit data with an address in the 10-bit format, start by writing 1111 0b, the 2 upper-order bits of the slave address, and W to the ICDRT register as the first address transmission. Then, as the second address transmission, write the 8 lower-order bits of the slave address to the ICDRT register.
4. After confirming that the ICSR2.TDRE flag is 1, write the data for transmission to the ICDRT register. The IIC automatically holds the SCLn line low until the transmit data is ready, a restart condition or a stop condition is issued.
5. After all bytes of data for transmission are written to the ICDRT register, wait until the value of the ICSR2.TEND flag returns to 1. Then, after checking that the ICSR2.START flag is 1, set the ICSR2.START flag to 0.
6. Set the ICCR2.RS bit to 1 (restart condition issuance request). On receiving the request, the IIC issues a restart condition.
7. After checking that the ICSR2.START flag is 1, write the value for transmission (the slave address and the R/W# bit) to the ICDRT register.

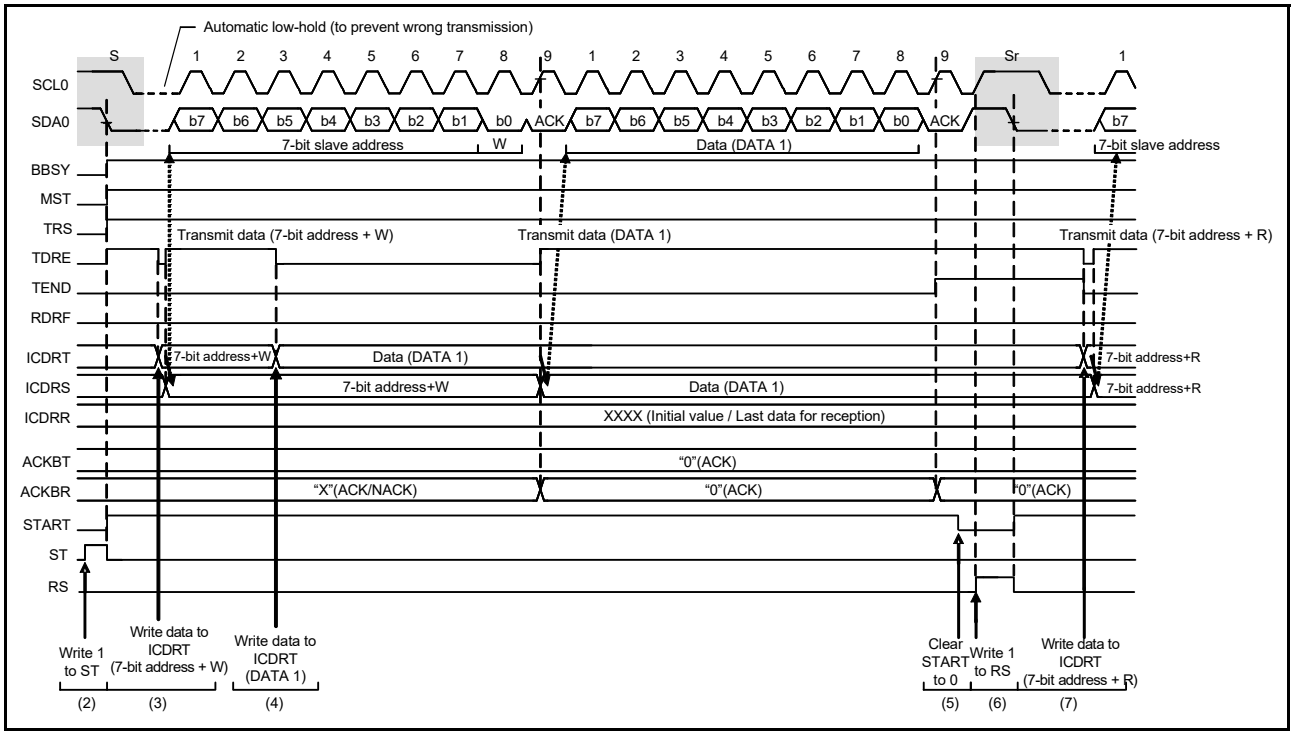


Figure 29.46 Restart condition issue timing after master transmission

29.11.3 Issuing a Stop Condition

The IIC issues a stop condition when the SP bit in ICCR2 is set to 1.

When the SP bit is set to 1, a stop condition request is made, and the IIC issues a stop condition when the BBSY flag in ICCR2 is 1 (bus busy state) and the MST bit in ICCR2 is 1 (master mode).

To issue a stop condition:

1. Drive the SDAn line low (high level to low level).
2. Ensure the low-level period of SCLn line set in ICBRL.BRL[4:0] elapses.
3. Release the SCLn line (low level to high level).
4. Detect a high level of the SCLn line and ensure the time set in ICBRH.BRH[4:0] and the stop condition setup time elapse.
5. Release the SDAn line (low level to high level).
6. Ensure the time set in ICBRL.BRL[4:0] and the bus free time elapse.
7. Clear the BBSY flag to 0 to release the bus mastership.

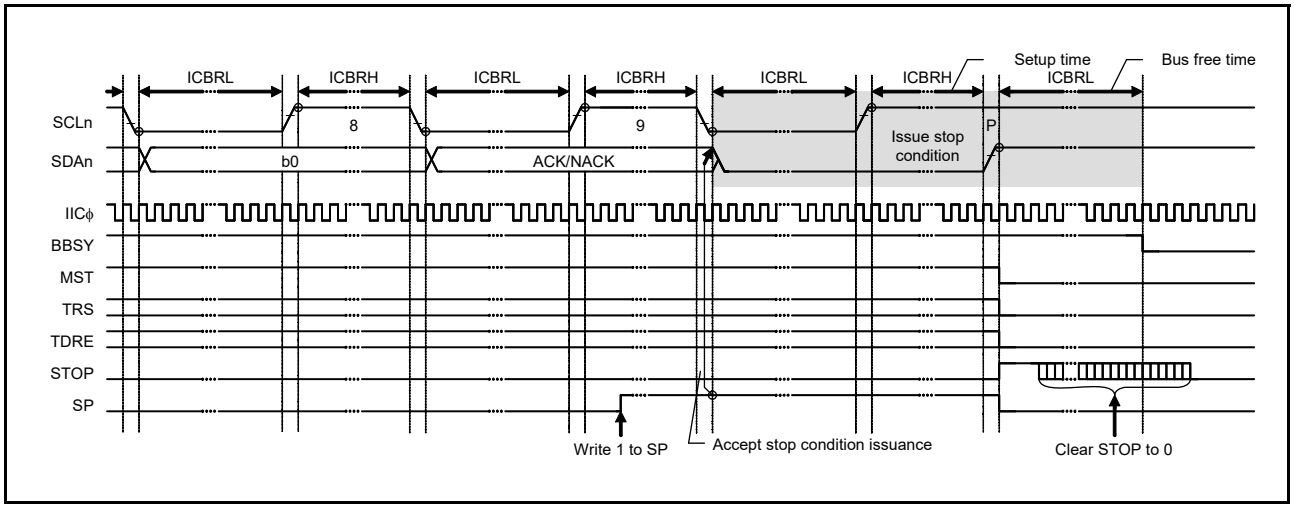


Figure 29.47 Stop condition issue timing using the SP bit

29.12 Bus Hanging

If the clock signals from the master and slave devices are out of synchronization because of noise or other factors, the I2C bus might hang with a fixed level on the SCLn line or SDAn line. To manage bus hanging, the IIC has:

- A timeout function to detect hanging by monitoring the SCLn line
- A function for outputting an extra SCL clock cycle to release the bus from a hung state because of clock signals being out of sync
- The IIC reset function
- An internal reset function.

By checking the SCLO, SDAO, SCLI, and SDAI bits in ICCR1, it is possible to determine whether the IIC or its communicating partner is placing the low level on the SCLn or SDAn lines.

29.12.1 Timeout Function

The timeout function can detect when the SCLn line is stuck longer than the predetermined time. The IIC can detect an abnormal bus state by monitoring that the SCLn line is stuck low or high for a predetermined time.

The timeout function monitors the SCLn line state and counts the low-level period or high-level period using the internal counter. The timeout function resets the internal counter each time the SCLn line changes (rising or falling), but continues to count unless the SCLn line changes. If the internal counter overflows because no SCLn line changes, the IIC can detect the timeout and report the bus hung state.

This timeout function is enabled when the ICFER.TMOE bit is 1. It detects a hung state when the SCLn line is stuck low or high during the following conditions:

- The bus is busy (ICCR2.BBSY flag is 1) in master mode (ICCR2.MST bit is 1)
- The IIC slave address is detected (ICSR1 register is not 00h) and the bus is busy (ICCR2.BBSY flag is 1) in slave mode (ICCR2.MST bit is 0)
- The bus is free (ICCR2.BBSY flag is 0) while a start condition is requested (ICCR2.ST bit is 1).

The internal counter of the timeout function uses the internal reference clock (IICϕ) set in the CKS[2:0] bits in ICMR1 as a count source. It functions as a 16-bit counter when long mode is selected (TMOS bit = 0 in ICMR2) or a 14-bit counter when short mode is selected (TMOS bit = 1).

The SCLn line level (low, high, or both levels) during which this counter is activated can be selected in the TMOH and TMOL bits in ICMR2. If both TMOL and TMOH bits are set to 0, the internal counter is disabled.

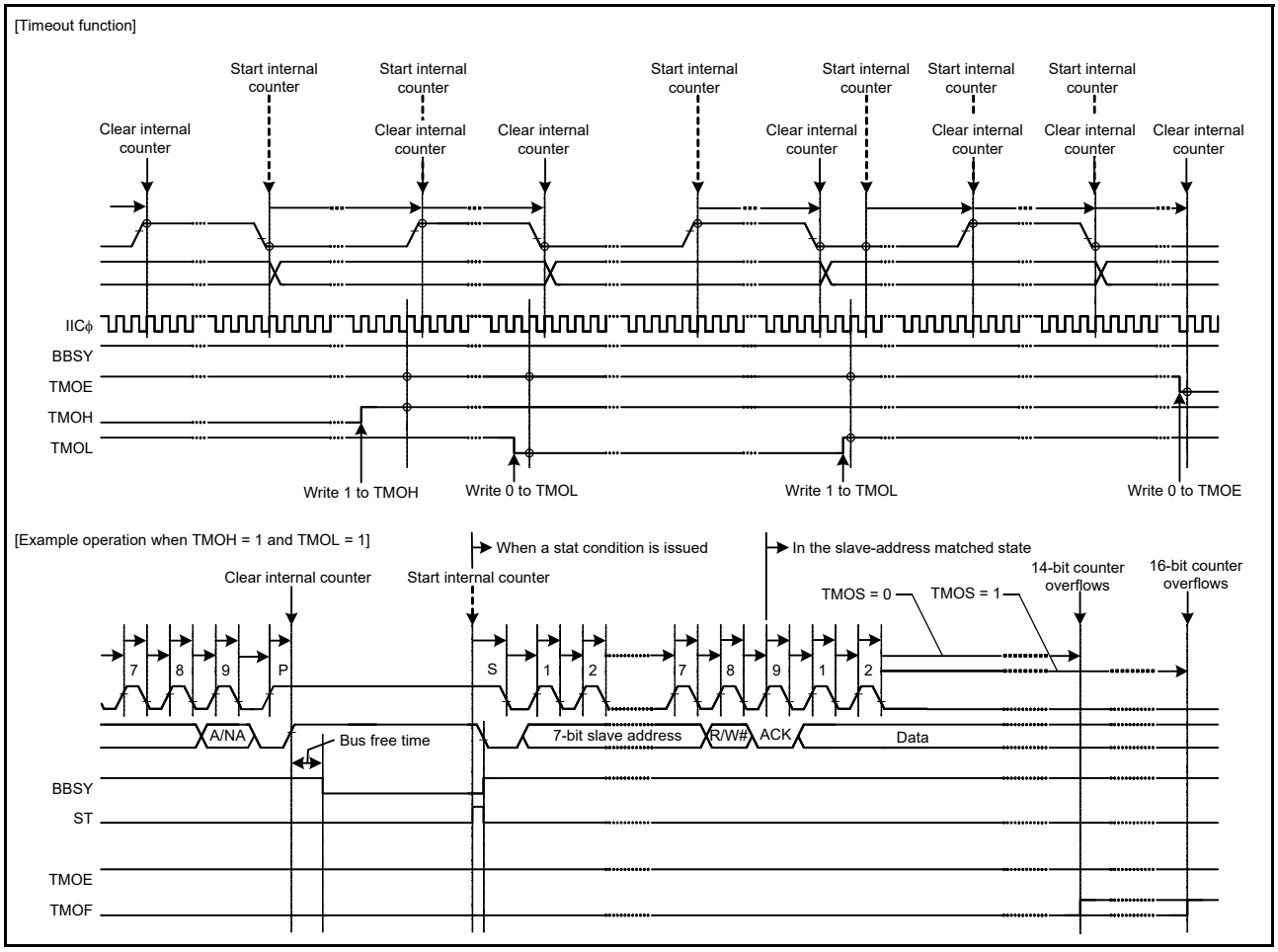


Figure 29.48 Timeout function using the TMOE, TMOS, TMOH, and TMOL bits

29.12.2 Extra SCL Clock Cycle Output Function

In master mode, the extra SCL clock cycle function outputs extra SCL clock cycles to release the SDAn line of the slave device from being held at the low level because the master is out of sync with the slave device. This function is mainly used in master mode to release the SDAn line of the slave device from being fixed low by including extra cycles of SCL output from the IIC. It uses single cycles of the SCL clock for a bus error where the IIC cannot issue a stop condition because the slave device is holding the SDAn line at the low level. Do not use this function in normal situations. Using it when communications are proceeding correctly leads to malfunctions.

When the CLO bit in ICCR1 is set to 1 in master mode, a single cycle of the SCL clock at the transfer rate, which is specified in the CKS[2:0] bits in ICMR1, the BRH[4:0] bits in ICBRH, and the BRL[4:0] bits in ICBRL, is output as an extra clock cycle. After output of this single cycle of the SCL clock, the CLO bit automatically is set to 0. If the BBSY flag is 1, SCL terminal keeps low output, if BBSY flag is 0, SCL terminal keeps high output. Additional clock cycles can be output consecutively by writing 1 to the CLO bit with software after reading the bit as 0.

When the IIC module is in master mode and the slave device is holding the SDAn line at the low level because synchronization with the slave device was lost because of noise or other effects, the output of a stop condition is not possible. This function can be used to output extra cycles of SCL one by one to make the slave device release the SDAn line from being held low, and so recovering the bus from an unusable state. Release of the SDAn line by the slave device can be monitored by reading the SDAI bit in ICCR1. After confirming release of the SDAn line by the slave device, complete communications by reissuing the stop condition.

[Output conditions for using the CLO bit in ICCR1]:

- When the bus is free (BBSY flag in ICCR2 = 0) or in master mode (MST bit = 1 and BBSY flag = 1 in ICCR2)
- When the communication device does not hold the SCLn line low.

Figure 29.49 shows the operation timing of the extra SCL clock cycle output function (CLO bit).

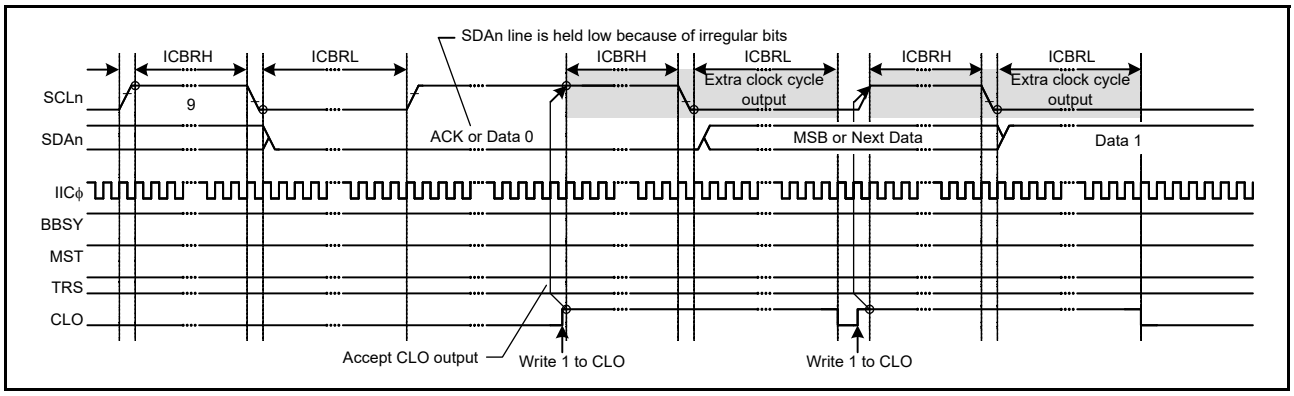


Figure 29.49 Extra SCL clock cycle output function using the CLO bit

29.12.3 IIC Reset and Internal Reset

The IIC module incorporates a function for resetting itself. There are two types of reset:

- An IIC reset, which initializes all registers, including the BBSY flag in ICCR2
- An internal reset, which releases the IIC from the slave-address matched state and initializes the internal counter while saving other settings.

After issuing a reset, be sure to set the IICRST bit in ICCR1 to 0. Both types of reset are effective for release from bus-hung states, because both restore the output state of the SCLn and SDAn pins to the high-impedance state.

Issuing a reset during slave operation might lead to a loss of synchronization between the master device clock and the slave device clock, so avoid this when possible. In addition, monitoring of the bus state, such as for the presence of a start condition, is not possible during an IIC reset (ICE and IICRST bits = 01b in ICCR1).

For a detailed description of the IIC and internal resets, see section 29.15, State of Registers When Issuing Each Condition.

29.13 SMBus Operation

The IIC supports data communication conforming to the SMBus Specification (version 2.0). To perform SMBus communication, set the SMBS bit in ICMR3 to 1. To use the transfer rate within a range of 10 kbps to 100 kbps of the SMBus standard, set the CKS[2:0] bits in ICMR1, BRH[4:0] bits in ICBRH, and BRL[4:0] bits in ICBRL. In addition, determine the values of the DLCS bit in ICMR2 and the SDDL[2:0] bits in ICMR2 to meet the data hold time specification of 300 ns or more. When the IIC is used only as a slave device, the transfer rate setting is not required, but ICBRL.BRL[4:0] must be set to a value longer than the data setup time (250 ns).

For the SMBus device default address (1100 001b), use one of the slave address registers L0 to L2 (SARL0, SARL1, and SARL2), and set the associated FS bit (7- or 10-bit address format select) in SARUy (y = 0 to 2) to 0 (7-bit address format).

When transmitting the UDID (Unique Device Identifier), set the SALE bit in ICFER to 1 to enable the slave arbitration-lost detection function.

29.13.1 SMBus Timeout Measurement

(1) Measuring slave device timeout

The following period (timeout interval: $T_{LOW:\ SEXT}$) must be measured for slave devices in SMBus communication:

- From start condition to stop condition.

To measure timeout for slave devices, measure the period from start condition detection to stop condition detection with the GPT using the IIC start condition detection interrupt (STIn) and stop condition detection interrupt (SPIn). The measured timeout period must be within the total clock low-level period [slave device] $T_{LOW:\ SEXT}$: 25 ms (max.) of the SMBus standard.

If the time measured with the GPT exceeds the clock low-level detection timeout $T_{TIMEOUT}$: 25 ms (minimum) of the SMBus standard, the slave device must release the bus by writing 1 to the IICRST bit in ICCR1 to issue an internal reset of the IIC. When an internal reset is issued, the IIC stops driving the bus for the SCLn pin and SDAn pin and makes the SCLn and SDAn pin output high-impedance, which releases the bus.

(2) Measuring master device timeout

The following periods (timeout interval: $T_{LOW:\ MEXT}$) must be measured for master devices in SMBus communication:

- From start condition to acknowledge bit
- Between acknowledge bits
- From acknowledge bit to stop condition.

To measure timeout for master devices, measure these periods with the GPT using the IIC start condition detection interrupt (STIn), stop condition detection interrupt (SPIn), transmit end interrupt (IICn_TEI), or receive data full interrupt (IICn_RXI). The measured timeout period must be within the total clock low-level extended period (master device) $T_{LOW:\ MEXT}$: 10 ms (maximum) of the SMBus standard, and the total of all $T_{LOW:\ MEXT}$ from start condition to stop condition must be within $T_{LOW:\ SEXT}$: 25 ms (maximum).

For the ACK receive timing (rising edge of the ninth SCL clock cycle), monitor the TEND flag in ICSR2 in master transmit mode (master transmitter) and the RDRF flag in ICSR2 in master receive mode (master receiver). Perform byte-wise transmit operations in master transmit mode, and hold the RDRFS bit in ICMR3 0 until the byte immediately before reception of the final byte in master receive mode. While the RDRFS bit is 0, the RDRF flag is set to 1 on the rising edge of the ninth SCL clock cycle.

If the period measured with the GPT exceeds the total clock low-level extended period (master device) $T_{LOW:\ MEXT}$: 10 ms (maximum) of the SMBus standard or the total of measured periods exceeds the clock low-level detection timeout $T_{TIMEOUT}$: 25 ms (minimum) of the SMBus standard, the master device must stop the transaction by issuing a stop condition. In master transmit mode, immediately stop the transmit operation (writing data to ICDRT).

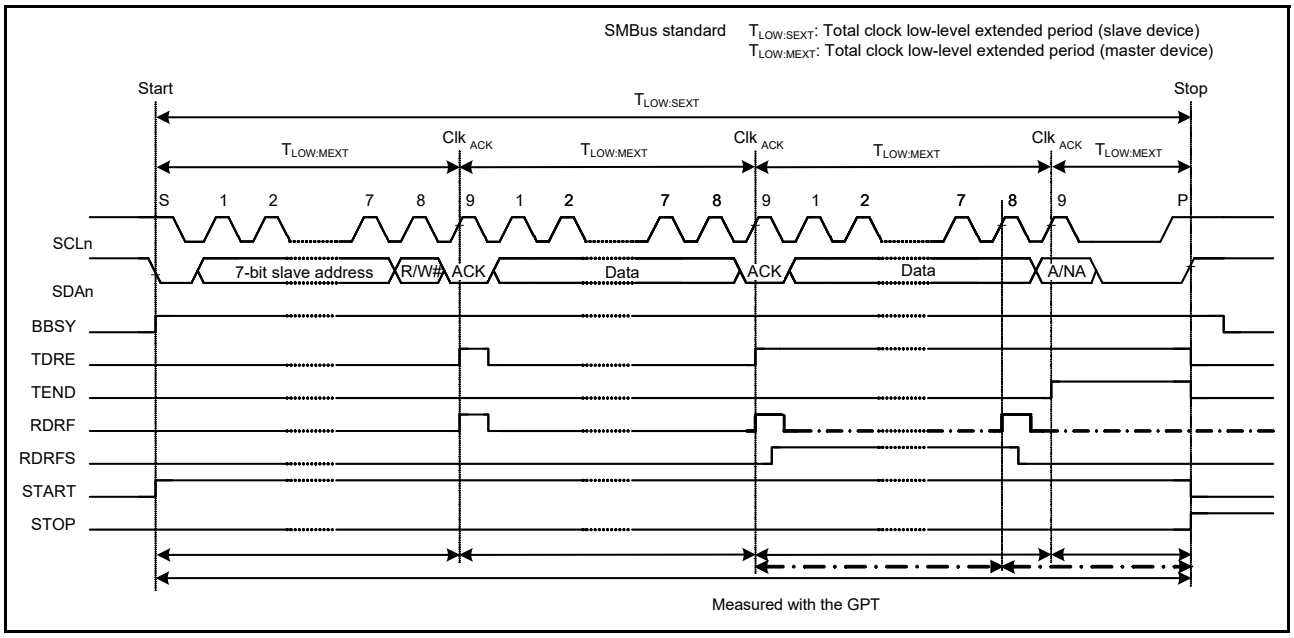


Figure 29.50 SMBus timeout measurement

29.13.2 Packet Error Code (PEC)

The MCU incorporates a CRC calculator that enables transmission of a packet error code (PEC) or allows checking the received data in SMBus data communication of the IIC. For the CRC generating polynomials of the CRC calculator, see section 32, Cyclic Redundancy Check (CRC) Calculator.

The PEC data in master transmit mode can be generated by writing all transmit data to the CRC data input register (CRCDIR) in the CRC calculator.

The PEC data in master receive mode can be checked by writing all receive data to CRCDIR in the CRC calculator and comparing the obtained value in the CRC data output register (CRCDOR) with the received PEC data.

To send ACK or NACK according to the match or mismatch result when the final byte is received as a result of the PEC code check, set the RDRFS bit in ICMR3 to 1 before the rising edge of the eighth SCL clock cycle during reception of the final byte, and hold the SCLn line low on the falling edge of the eighth clock cycle.

29.13.3 SMBus Host Notification Protocol (Notify ARP Master Command)

In communications over an SMBus, a slave device can temporarily act as a master device to notify the SMBus host or ARP master of its own slave address, or to request its own slave address from the SMBus host.

To operate as an SMBus host or ARP master, the host address (0001 000b) sent from the slave device must be detected as a slave address, so the IIC has a function for detecting the host address. To detect the host address as a slave address, set the SMBS bit in ICMR3 and the HOAE bit in ICSER to 1. Operation after the host address is detected is the same as normal slave operation.

29.14 Interrupt Sources

The IIC issues five types of interrupt request:

- Transfer error or event generation (arbitration-lost, NACK detection, timeout detection, start condition detection, and stop condition detection)
- Receive data full
- Transmit data empty
- Transmit end
- Address match during wakeup function.

Table 29.10 lists details about the interrupt requests. The receive data full and transmit data empty are both capable of activating data transfer by the DTC.

Table 29.10 Interrupt sources

Symbol	Interrupt source	Interrupt flag	DTC activation	Interrupt condition
IICn_EEI*5	Transfer error/event generation	AL	Not possible	AL = 1, ALIE = 1
		NACKF		NACKF = 1, NAKIE = 1
		TMOF		TMOF = 1, TMOIE = 1
		START		START = 1, STIE = 1
		STOP		STOP = 1, SPIE = 1
IICn_RXI*2, *5	Receive data full	RDRF	Possible	RDRF = 1, RIE = 1
IICn_TXI*1, *5	Transmit data empty	TDRE	Possible	TDRE = 1, TIE = 1
IICn_TEI*3, *5	Transmit end	TEND	Not possible	TEND = 1, TEIE = 1
IIC0_WUI*4	Address match during wakeup function	WUF, WUSYF or WUASYF	Not possible	• Address match • WUASYF = 1 • WUIE = 1 or • WUF = 1 • WUSYF = 1 • WUIE = 1

Note: There is a delay between the execution of a write instruction for a peripheral module by the CPU and the actual writing to the module. When an interrupt flag is cleared or masked, read the relevant flag again to check whether clearing or masking is complete, and then return from interrupt handling. Not doing so creates the possibility of repeated processing of the same interrupt.

Note 1. Because IICn_TXI is an edge-detected interrupt, it does not require clearing. Additionally, the TDRE flag in ICSR2 (a condition for IICn_TXI) is automatically set to 0 when transmit data is written to ICDRT or a stop condition is detected (STOP flag = 1 in ICSR2).

Note 2. Because IICn_RXI is an edge-detected interrupt, it does not require clearing. Additionally, the RDRF flag in

ICSR2 (a condition for IICn_RXI) is automatically set to 0 when data is read from ICDRR.

Note 3. When using the IICn_TEI interrupt, clear the TEND flag in ICSR2 in the IICn_TEI interrupt handling. The TEND flag in ICSR2 is automatically set to 0 when transmit data is written to ICDRT or a stop condition is detected (STOP flag = 1 in ICSR2).

Note 4. Only channel 0 has a wakeup function, so IIC0_WUI is for channel 0 only.

Note 5. Channel number (n = 0, 1)

Clear or mask each flag during interrupt handling.

29.14.1 Buffer Operation for IICn_TXI and IICn_RXI Interrupts

If the conditions for generating an IICn_TXI and IICn_RXI interrupt are satisfied while the associated IR flag is 1, the interrupt request is not output for the ICU but saved internally. One request per source can be saved internally.

An interrupt request that is saved within the ICU is output when the value of the ICU.IELSRn.IR flag becomes 0. Internally saved interrupt requests are automatically cleared under normal usage conditions. Internally saved interrupt requests can also be cleared by writing 0 to the interrupt enable bit within the given peripheral module.

29.15 State of Registers When Issuing Each Condition

The IIC has two dedicated resets, IIC reset and internal reset. Table 29.11 lists the registers states when issuing each condition.

Table 29.11 Register states when issuing each condition (1 of 2)

Registers		Reset	IIC reset (ICE = 0, IICRST = 1)	Internal reset (ICE = 1, IICRST = 1)	Start or restart condition detection	Stop condition detection
ICCR1	ICE, IICRST	Reset	Saved	Saved	Saved	Saved
	SCLO, SDAO		Reset	Reset		
	Others			Saved		
ICCR2	BBSY	Reset	Reset	Saved	Set	Reset
	ST, RS			Reset	Reset	Saved
	SP					Reset
	TRS				Set or saved	
	MST					
ICMR1	BC[2:0]	Reset	Reset	Reset	Reset	Saved
	Others			Saved	Saved	
ICMR2		Reset	Reset	Saved	Saved	Saved
ICMR3	ACKBIT	Reset	Reset	Saved	Saved	Reset
	Others					Saved
ICFER		Reset	Reset	Saved	Saved	Saved
ICSER		Reset	Reset	Saved	Saved	Saved
ICIER		Reset	Reset	Saved	Saved	Saved
ICSR1		Reset	Reset	Reset	Saved	Reset
ICSR2	TEND	Reset	Reset	Reset	Saved	Reset
	TDRE				Set or saved	
	START				Set	
	STOP				Saved	Set
	Others				Saved	Saved
ICWUR		Reset	Reset	Saved	Saved	Saved
SARL0, SARL1, SARL2 SARU0, SARU1, SARU2		Reset	Reset	Saved	Saved	Saved
ICBRH, ICBRL		Reset	Reset	Saved	Saved	Saved
ICDRT		Reset	Reset	Saved	Saved	Saved

Table 29.11 Register states when issuing each condition (2 of 2)

Registers		Reset	IIC reset (ICE = 0, IICRST = 1)	Internal reset (ICE = 1, IICRST = 1)	Start or restart condition detection	Stop condition detection
ICDRR		Reset	Reset	Saved	Saved	Saved
ICDRS		Reset	Reset	Reset	Saved	Saved
ICWUR2	WUSEN	Reset	Reset	Saved	Saved	Saved
	Others					Set, reset, or saved
Timeout function		Reset	Reset	Reset	Operation	Operation
Bus free time measurement		Reset	Reset	Operation	Operation	Operation

29.16 Event Link Output

The IIC0 and IIC1 modules handle event output for the Event Link Controller for the following sources:

(1) Transfer Error Event

When a transfer error event occurs, the associated event signal can be output to another module by the ELC.

(2) Receive Data Full

When a receive data register becomes full, the associated event signal can be output to another module by the ELC.

(3) Transmit Data Empty

When a transmit data register becomes empty, the associated event signal can be output to another module by the ELC.

(4) Transmit End

On completion of transfer, the associated event signal can be output to another module by the ELC.

29.16.1 Interrupt Handling and Event Linking

Each of the IIC interrupt types (see Table 29.10) has an enable bit to control enabling and disabling of the associated interrupt signal. An interrupt request signal is output to the CPU when an interrupt source condition is satisfied while the associated enable bit is set.

The associated event link output signals are sent to other modules as event signals by the ELC when the interrupt source conditions are satisfied, regardless of the interrupt enable bit settings. For details on interrupt sources, see Table 29.10.

29.17 Usage Notes

29.17.1 Settings for the Module-Stop State

The Module Stop Control Register B (MSTPCRB) can enable or disable IIC operation. The module is initially stopped after a reset. The registers become accessible on release from the module-stop state. For details on Module Stop Control Register B, see section 10, Low Power Modes.

29.17.2 Notes on Starting Transfer

If the IR flag associated with the IIC interrupt is 1 when transfer is started (ICCR1.ICE bit = 1), use the following procedure to clear interrupts before enabling operations. Starting transfer with the IR flag set to 1 while the ICCR1.ICE bit is 1 leads to an interrupt request being internally saved after transfer starts, and this can lead to unexpected behavior of the IR flag.

1. Confirm that the ICCR1.ICE bit is 0.
2. Set the relevant interrupt enable bits, such as ICIER.TIE, to 0.
3. Read the relevant interrupt enable bits, such as ICIER.TIE, and confirm that the value is 0.
4. Set the IR flag to 0.

30. Controller Area Network (CAN) Module

30.1 Overview

The CAN module uses a message-based protocol to receive and transmit data between multiple slaves and masters in electromagnetically noisy applications. The module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported. The CAN module requires an additional external CAN transceiver.

Table 30.1 lists the CAN specifications, and Figure 30.1 shows a block diagram.

Table 30.1 CAN specifications (1 of 2)

Parameter	Description
Data transfer rate	ISO11898-1-compliant for standard and extended frames
Bit rate	Data transfer rate programmable up to 1 Mbps (fCAN ≥ 8 MHz) fCAN: CAN clock source
Message box	32 mailboxes, with two selectable mailbox modes • Normal mode: 32 mailboxes independently configurable for either transmission or reception • FIFO mode: 24 mailboxes independently configurable for either transmission or reception, with remaining mailboxes used for receive (RX) and transmit (TX) 4-stage FIFOs.
Reception	• Support for data frame and remote frame reception • Reception ID format selectable to only standard ID, only extended ID, or mixed IDs • Programmable one-shot reception function • Selectable between overwrite mode (unread message overwritten) and overrun mode (unread message saved) • Reception complete interrupt independently enabled or disabled for each mailbox.
Acceptance filter	• Eight acceptance masks (one for every four mailboxes) • Masks independently enabled or disabled for each mailbox.
Transmission	• Support for data frame and remote frame transmission • Transmission ID format selectable to only standard ID, only extended ID, or mixed IDs) • Programmable one-shot transmission function • Broadcast messaging function • Priority mode selectable based on message ID or mailbox number • Support for transmission request abort, with abort completion confirmable in status flag • Transmission complete interrupt independently enabled or disabled for each mailbox.
Mode transition for bus-off recovery	Mode transition for the recovery from the bus-off state selectable to: • ISO11898-1 specification-compliant • Automatic entry into CAN halt mode on bus-off entry • Automatic entry into CAN halt mode on bus-off end • Transition to CAN halt mode through software • Transition to error-active state through software.
Error status monitoring	• Monitoring of CAN bus errors, including stuff error, form error, ACK error, 15-bit CRC error, bit error, and ACK delimiter error • Detection of transition to error states, including error-warning, error-passive, bus-off entry, and bus-off recovery • Supports reading of error counters.
Time stamping	• Time stamp function using a 16-bit counter • Reference clock selectable to 1-, 2-, 4-, and 8-bit time periods.
Interrupt function	Supports five interrupt sources: reception complete, transmission complete, receive FIFO, transmit FIFO, and error interrupts
CAN sleep mode	CAN clock stopped to reduce power consumption
Software support unit	Three software support units: • Acceptance filter support • Mailbox search support, including receive mailbox search, transmit mailbox search, and message lost search • Channel search support.
CAN clock source	CANMCLK

Table 30.1 CAN specifications (2 of 2)

Parameter	Description
Test mode	Three test modes available for evaluation purposes: • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback).
Module-stop function	Module-stop state can be set to reduce power consumption

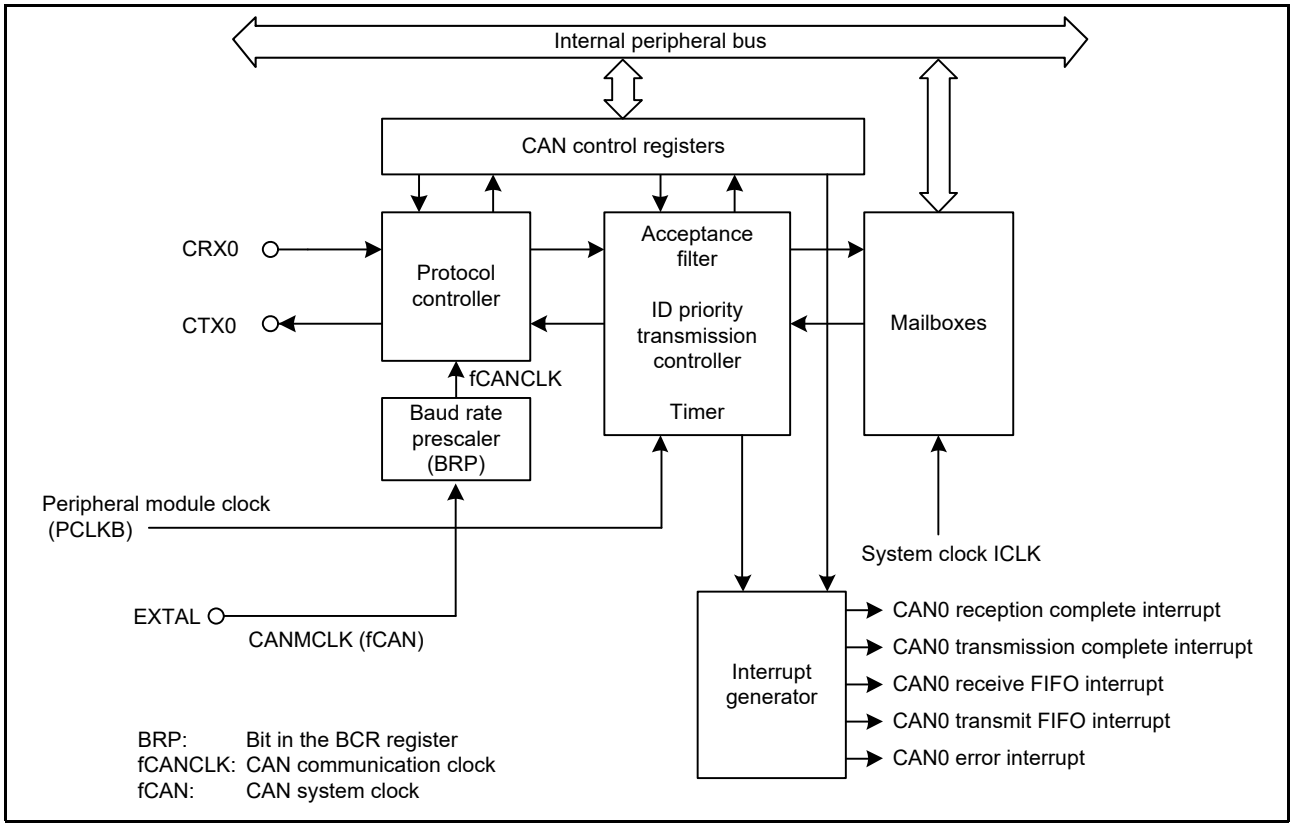


Figure 30.1 CAN module block diagram

The CAN module includes the following blocks:

- CAN input and output pins
  CRX0 and CTX0
- Protocol controller
  Handles CAN protocol processing such as bus arbitration, bit timing during transmission and reception, stuffing, and error handling.
- Mailboxes
  Consists of 32 mailboxes, which can be configured as either transmit or receive. Each mailbox has an individual ID, data length code (DLC), data field (8 bytes), and time stamp.
- Acceptance filter
  Performs filtering of received messages using MKRk register settings.
- Timer
  Used for the time stamp function. The timer value when a message is stored in the mailbox is written as the time stamp value.
- Interrupt generator for five types of interrupts:
  - CAN0 reception complete interrupt
  - CAN0 transmission complete interrupt

- CAN0 receive FIFO interrupt
- CAN0 transmit FIFO interrupt
- CAN0 error interrupt.

The CAN module communicates on the pins listed in Table 30.2. These pins are multiplexed with other signals on the MCU. For details, see section 17, I/O Ports.

Table 30.2 Pin configuration

Pin name	I/O	Function
CRX0	Input	Data receive pin
CTX0	Output	Data transmit pin

30.2 Register Descriptions

30.2.1 Control Register (CTLR)

Address(es): CAN0.CTLR 4005 0840h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	RBOC	BOM[1:0]		SLPM	CANM[1:0]		TSPS[1:0]		TSRC	TPM	MLM	IDFM[1:0]		MBM
Value after reset:	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	MBM	CAN Mailbox Mode Select*1	0: Normal mailbox mode 1: FIFO mailbox mode.	R/W
b2, b1	IDFM[1:0]	ID Format Mode Select *1	b2 b1 0 0: Standard ID mode: All mailboxes, including FIFO mailboxes, handle only standard IDs 0 1: Extended ID mode: All mailboxes, including FIFO mailboxes, handle only extended IDs 1 0: Mixed ID mode: All mailboxes, including FIFO mailboxes, handle both standard and extended IDs. In normal mailbox mode, use the associated IDE bit to differentiate standard and extended IDs. In FIFO mailbox mode, the associated IDE bits are used for mailboxes 0 to 23, the IDE bits in FIDCR0 and FIDCR1 are used for the receive FIFO, and the IDE bit associated with mailbox 24 is used for the transmit FIFO. 1 1: Setting prohibited.	R/W
b3	MLM	Message Lost Mode Select*1	0: Overwrite mode 1: Overrun mode.	R/W
b4	TPM	Transmission Priority Mode Select*1	0: ID priority transmit mode 1: Mailbox number priority transmit mode.	R/W
b5	TSRC	Time Stamp Counter Reset Command*4	0: Do not reset time stamp counter 1: Reset time stamp counter.*3	R/W
b7, b6	TSPS[1:0]	Time Stamp Prescaler Select*1	b7 b6 0 0: Every 1-bit time 0 1: Every 2-bit time 1 0: Every 4-bit time 1 1: Every 8-bit time.	R/W
b9, b8	CANM[1:0]	CAN Mode Operation Select*5	b9 b8 0 0: CAN operation mode 0 1: CAN reset mode 1 0: CAN halt mode 1 1: CAN reset mode (forced transition).	R/W
b10	SLPM	CAN Sleep Mode*5,*6	0: Exit sleep mode 1: Enter CAN sleep mode.	R/W

Bit	Symbol	Bit name	Description	R/W
b12, b11	BOM[1:0]	Bus-Off Recovery Mode*1	b12 b11 0 0: Normal mode (ISO11898-1-compliant) 0 1: Enter CAN halt mode automatically on entering bus-off state 1 0: Enter CAN halt mode automatically on end of bus-off state 1 1: Enter CAN halt mode during bus-off recovery period through a software request.	R/W
b13	RBOC	Forced Return from Bus-Off*2	0: No return occurred 1: Forced return from bus-off state.*3	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Write to the BOM[1:0], TSPS[1:0], TPM, MLM, IDFM[1:0], and MBM bits in CAN reset mode.
Note 2. Set the RBOC bit to 1 in the bus-off state.
Note 3. This bit automatically clears to 0 after being set to 1. It should be read as 0.
Note 4. Set the TSRC bit to 1 in CAN operation mode.
Note 5. When the CANM[1:0] and SLPM bits are changed, check STR to ensure that the mode is switched. Do not change the CANM[1:0] bits or SLPM bit until the mode is switched.
Note 6. Write to the SLPM bit in CAN reset mode or CAN halt mode. When changing the SLPM bit, write 0 or 1 to only the SLPM bit.

MBM bit (CAN Mailbox Mode Select)

When the MBM bit is 0 (normal mailbox mode), mailboxes 0 to 31 are configured as transmit or receive mailboxes.

When the MBM bit is 1 (for FIFO mailbox mode):

- Mailboxes 0 to 23 are configured as transmit or receive mailboxes
- Mailboxes 24 to 27 are configured as a transmit FIFO
- Mailboxes 28 to 31 are configured as a receive FIFO
- Transmit data is written into mailbox 24, the window mailbox for the transmit FIFO
- Receive data is read from mailbox 28, the window mailbox for the receive FIFO.

Table 30.3 lists the mailbox configurations.

IDFM[1:0] bits (ID Format Mode Select)

The IDFM[1:0] bits specify the ID format.

MLM bit (Message Lost Mode Select)

The MLM bit specifies the operation when a new message is captured in the unread mailbox. Overwrite mode or overrun mode can be selected. In both cases, the mode applies to all mailboxes, including the receive FIFO.

When MLM is 0, all mailboxes are set to overwrite mode. Any new message received overwrites the pre-existing one.

When MLM is 1, all mailboxes are set to overrun mode. Any new message received does not overwrite the pre-existing one and is discarded.

TPM bit (Transmission Priority Mode Select)

The TPM bit specifies the priority when transmitting messages. ID priority transmit mode or mailbox number transmit mode can be selected. All mailboxes are set for either ID priority transmission or mailbox number priority transmission.

When TPM is 0, ID priority transmit mode is selected and transmission priority is arbitrated as defined in the ISO11898-1 CAN specification. In ID priority transmit mode, mailboxes 0 to 31 (in normal mailbox mode), and mailboxes 0 to 23 (in FIFO mailbox mode), and the transmit FIFO are compared for the IDs of mailboxes configured for transmission. If two or more mailbox IDs are the same, the mailbox with the smaller number has higher priority.

Only the next message to be transmitted from the transmit FIFO is included in the transmission arbitration. If a FIFO message is currently being transmitted, the next pending message within the transmit FIFO is included in the arbitration.

When TPM is 1, mailbox number transmit mode is selected and the transmit mailbox with the smallest number has the highest priority. In FIFO mailbox mode, the transmit FIFO has lower priority than normal mailboxes (0 to 23).

TSRC bit (Time Stamp Counter Reset Command)

The TSRC bit resets the time stamp counter. When it is set to 1, TSR is set to 0000h. TSRC is set to 0 automatically.

TSPS[1:0] bits (Time Stamp Prescaler Select)

The TSPS[1:0] bits select the prescaler for the time stamp. The reference clock for the time stamp can be selected to 1-, 2-, 4-, or 8-bit time periods.

CANM[1:0] bits (CAN Mode Operation Select)

The CANM[1:0] bits select one of the following modes:

- CAN operation mode
- CAN reset mode
- CAN halt mode.

CAN sleep mode is set in the SLPM bit. For details, see section 30.3, Operation Modes. When the CAN module enters CAN halt mode based on the setting in the BOM[1:0] bits, the CANM[1:0] bits automatically set to 10b.

SLPM bit (CAN Sleep Mode)

When the SLPM bit is set to 1, the CAN module enters CAN sleep mode. When the SLPM bit is set to 0, the CAN module exits CAN sleep mode. For details, see section 30.3, Operation Modes.

BOM[1:0] bits (Bus-Off Recovery Mode)

The BOM[1:0] bits select bus-off recovery mode for the CAN module.

When the BOM[1:0] bits are 00b, the recovery from bus-off is compliant with the ISO11898-1 specification. The CAN module recovers CAN communication (error-active state) after detecting 11 consecutive recessive bits 128 times. A bus-off recovery interrupt request occurs when recovering from bus-off.

When the BOM[1:0] bits are 01b and the CAN module reaches the bus-off state, the CANM[1:0] bits in CTLR set 10b to enter CAN halt mode. No bus-off recovery interrupt request occurs when recovering from bus-off, and TECR and RECR are set to 00h.

When the BOM[1:0] bits are 10b, the CANM[1:0] bits are set to 10b as soon as the CAN module reaches the bus-off state. The CAN module enters CAN halt mode after the recovery from the bus-off state, after detecting 11 consecutive recessive bits 128 times. A bus-off recovery interrupt request occurs when recovering from bus-off, and TECR and RECR are set to 00h.

When the BOM[1:0] bits are 11b, the CAN module enters CAN halt mode by setting the CANM[1:0] bits to 10b while the CAN module is still in the bus-off state. No bus-off recovery interrupt request is generated when recovering from bus-off and TECR and RECR are set to 00h. However, the interrupt is generated if the CAN module recovers from bus-off after detecting 11 consecutive recessive bits 128 times before the CANM[1:0] bits are set to 10b.

If the CPU requests an entry to the CAN reset mode at the same time as the CAN module attempts to enter CAN halt mode (at bus-off entry when the BOM[1:0] bits are 01b, or at bus-off end when the BOM[1:0] bits are 10b), then the CPU request has higher priority.

RBOC bit (Forced Return from Bus-Off)

When the RBOC bit is set to 1 in the bus-off state, the CAN module forcibly exits bus-off. The RBOC bit is automatically set to 0, and the error state changes from bus-off to error-active. When the RBOC bit is set to 1, RECR and TECR are set to 00h and the BOST bit in STR is set to 0, indicating no bus-off state. The other registers remain unchanged when RBOC is set to 1. No bus-off recovery interrupt request is generated. Use the RBOC bit only when the BOM[1:0] bits are 00b (normal mode).

Table 30.3 Mailbox configuration

Mailbox	MBM bit = 0 (normal mailbox mode)	MBM bit = 1 (FIFO mailbox mode)*1 to *5
Mailboxes 0 to 23	Normal mailbox	Normal mailbox
Mailboxes 24 to 27		Transmit FIFO
Mailboxes 28 to 31		Receive FIFO

Note 1. This disables transmit FIFO control by TFCR, and the MCTL_TXj registers associated with mailboxes 24 to 27 are disabled. MCTL_TX24 to MCTL_TX27 cannot be used by the transmit FIFO.
Note 2. This disables receive FIFO control by RFCR, and the MCTL_RXj registers associated with mailboxes 28 to 31 are disabled. MCTL_RX28 to MCTL_RX31 cannot be used by the receive FIFO.
Note 3. See the MIER_FIFO description for information on FIFO interrupts.
Note 4. The bits in MKIVLR associated with mailboxes 24 to 31 are disabled. Set 0 to these bits.
Note 5. The transmit and receive FIFOs can be used for both data and remote frames.

30.2.2 Bit Configuration Register (BCR)

Address(es): CAN0.BCR 4005 0844h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	TSEG1[3:0]				—	—	BRP[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	SJW[1:0]		—	TSEG2[2:0]			—	—	—	—	—	—	—	CCLKS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CCLKS	CAN Clock Source Selection	0: Setting prohibited 1: CANMCLK (generated by the main clock) This bit must be set to 1 when using the CAN module.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b10 to b8	TSEG2[2:0]	Time Segment 2 Control	b10 b8 0 0 0: Setting prohibited 0 0 1: 2 Tq 0 1 0: 3 Tq 0 1 1: 4 Tq 1 0 0: 5 Tq 1 0 1: 6 Tq 1 1 0: 7 Tq 1 1 1: 8 Tq.	R/W
b11	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b13, b12	SJW[1:0]	Synchronization Jump Width Control	b13 b12 0 0: 1 Tq 0 1: 2 Tq 1 0: 3 Tq 1 1: 4 Tq.	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b25 to b16	BRP[9:0]	Baud Rate Prescaler Select*1	These bits set the frequency of the CAN communication clock (fCANCLK).	R/W
b27, b26	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit name	Description	R/W
b31 to b28	TSEG1[3:0]	Time Segment 1 Control	b31 b28 0 0 0 0: Setting prohibited 0 0 0 1: Setting prohibited 0 0 1 0: Setting prohibited 0 0 1 1: 4 Tq 0 1 0 0: 5 Tq 0 1 0 1: 6 Tq 0 1 1 0: 7 Tq 0 1 1 1: 8 Tq 1 0 0 0: 9 Tq 1 0 0 1: 10 Tq 1 0 1 0: 11 Tq 1 0 1 1: 12 Tq 1 1 0 0: 13 Tq 1 1 0 1: 14 Tq 1 1 1 0: 15 Tq 1 1 1 1: 16 Tq.	R/W

Tq: Time Quantum

Note 1. Do not select a value less than 1 while the SCKSCR.CKSEL[2:0] bits are 011b (selecting the main clock oscillator).

For setting the bit timing, see section 30.4, Data Transfer Rate Configuration. Set BCR before entering CAN halt mode or CAN operation mode from CAN reset mode. After the setting is made once, this register can be written to in CAN reset mode or CAN halt mode. A 32-bit read/write access must be performed carefully so as not to change bits 0 to 7.

TSEG2[2:0] bits (Time Segment 2 Control)

The TSEG2[2:0] bits specify the length of the phase buffer segment 2 (PHASE_SEG2) with a Tq value. A value from 2 to 8 Tq can be set. Set a value smaller than that of the TSEG1[3:0] bits.

SJW[1:0] bits (Synchronization Jump Width Control)

The SJW[1:0] bits specify the synchronization jump width with a Tq value. A value from 1 to 4 Tq can be set. Set a value smaller than or equal to that of the TSEG2[2:0] bits.

BRP[9:0] bits (Baud Rate Prescaler Select)

The BRP[9:0] bits set the frequency of the CAN communication clock (fCANCLK). The fCANCLK cycle is 1 Tq. If the setting is P (0 to 1023), the baud rate prescaler divides fCAN by P + 1.

TSEG1[3:0] bits (Time Segment 1 Control)

The TSEG1[3:0] bits specify the total length of the propagation time segment (PROP_SEG) and phase buffer segment 1 (PHASE_SEG1) with a time quantum (Tq) value. A value from 4 to 16 Tq can be set.

30.2.3 Mask Register k (MKRk) (k = 0 to 7)

Address(es): CAN0.MKR[0] 4005 0400h to CAN0.MKR[7] 4005 041Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	SID[10:0]											EID[17:0]	
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	EID[17:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b17 to b0	EID[17:0]	Extended ID	0: Do not compare associated EID[17:0] bit 1: Compare associated EID[17:0] bit.	R/W
b28 to b18	SID[10:0]	Standard ID	0: Do not compare associated SID[10:0] bit 1: Compare associated SID[10:0] bit.	R/W
b31 to b29	—	Reserved	These bits are read as undefined. The write value should be 0.	R/W

For the mask function in FIFO mailbox mode, see section 30.6, Acceptance Filtering and Masking Functions.

Write to MKRk in CAN reset mode or CAN halt mode.

EID[17:0] bits (Extended ID)

The EID[17:0] bits are the filter mask bits associated with the CAN extended ID bits. They are used to receive extended ID messages. When an EID[17:0] bit is set to 0, the received ID is not compared with the associated mailbox ID. When an EID[17:0] bit is set to 1, the received ID is compared with the associated mailbox ID.

SID[10:0] bits (Standard ID)

The SID[10:0] bits are the filter mask bits associated with the CAN standard ID bits. They are used to receive both standard ID and extended ID messages. When the SID[10:0] bits are set to 0, the received ID is not compared with the associated mailbox ID. When the SID[10:0] bits are set to 1, the received ID is compared with the associated mailbox ID.

30.2.4 FIFO Received ID Compare Registers 0 and 1 (FIDCR0 and FIDCR1)

Address(es): CAN0.FIDCR0 4005 0420h, CAN0.FIDCR1 4005 0424h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IDE	RTR	—	SID[10:0]											EID[17:0]	
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	EID[17:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b17 to b0	EID[17:0]	Extended ID	Extended ID of the data and remote frames	R/W
b28 to b18	SID[10:0]	Standard ID	Standard ID of the data and remote frames	R/W
b29	—	Reserved	This bit is read as undefined. The write value should be 0.	R/W

Bit	Symbol	Bit name	Description	R/W
b30	RTR	Remote Transmission Request	0: Data frame 1: Remote frame.	R/W
b31	IDE	ID Extension*1	0: Standard ID 1: Extended ID.	R/W

Note 1. When the CTLR.IDFM[1:0] bits are not 10b, the IDE bit should be written with 0 and read as 0.

FIDCR0 and FIDCR1 are enabled when the MBM bit in CTLR is set to 1 (FIFO mailbox mode). In this mode, the EID[17:0], SID[10:0], RTR, and IDE bits in mailbox 28 to mailbox 31 are disabled. Write to these registers in CAN reset or CAN halt mode. For information on using FIDCR0 and FIDCR1, see section 30.6, Acceptance Filtering and Masking Functions.

EID[17:0] bits (Extended ID)

The EID[17:0] bits set the extended ID of data and remote frames. They are used to receive extended ID messages.

SID[10:0] bits (Standard ID)

The SID[10:0] bits set the standard ID of data and remote frames. They are used to receive both standard ID and extended ID messages.

RTR bit (Remote Transmission Request)

The RTR bit sets the frame format to data frames or remote frames.

- When both RTR bits in FIDCR0 and FIDCR1 are set to 0, only data frames are received
- When both RTR bits in FIDCR0 and FIDCR1 are set to 1, only remote frames are received
- When the RTR bits in FIDCR0 and FIDCR1 are set to different values, both data and remote frames are received.

IDE bit (ID Extension)

The IDE bit sets the ID format to standard ID or extended ID. The IDE bit is enabled when the IDFM[1:0] bits in CTLR are 10b (mixed ID mode).

- When both IDE bits in FIDCR0 and FIDCR1 are set to 0, only standard ID frames are received
- When both IDE bits in FIDCR0 and FIDCR1 are set to 1, only extended ID frames are received
- When the IDE bits in FIDCR0 and FIDCR1 are set to different values, both standard ID and extended ID frames are received.

30.2.5 Mask Invalid Register (MKIVLR)

Address(es): CAN0.MKIVLR 4005 0428h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MB31	MB30	MB29	MB28	MB27	MB26	MB25	MB24	MB23	MB22	MB21	MB20	MB19	MB18	MB17	MB16
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MB15	MB14	MB13	MB12	MB11	MB10	MB9	MB8	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b31 to b0	MB31 to MB0	Mask Invalid	0: Mask valid 1: Mask invalid.	R/W

Each bit in MKIVLR is associated with a mailbox of the same number. Bit [0] in MKIVLR corresponds to mailbox 0 (MB0), and bit [31] corresponds to mailbox 31 (MB31).

Note: Set bits [31:24] to 0 in FIFO mailbox mode.

When a bit is set to 1, the associated acceptance mask register becomes invalid for the associated mailbox. When a mask invalid bit is set to 1, a message is received by the associated mailbox only if the receive message ID matches the mailbox ID exactly.

Write to MKIVLR in CAN halt mode.

30.2.6 Mailbox Register j (MBj_ID, MBj_DL, MBj_Dm, MBj_TS) (j = 0 to 31, m = 0 to 7)

Table 30.4 lists the CAN0 mailbox memory mapping, and Table 30.5 lists the CAN data frame configuration.

The value after reset of the CAN0 mailbox is undefined.

Write to MBj_ID, MBj_DL, MBj_Dm, and MBj_TS only when the associated MCTL_TXj or MCTL_RXj (j = 0 to 31) is 00h and the associated mailbox is not processing an abort request.

See Table 30.4 for specific register addresses.

Table 30.4 CAN0 mailbox memory mapping

Address for CAN0	Mapped message content
4005 0200h + 16 × j + 0	IDE, RTR, SID10 to SID6
4005 0200h + 16 × j + 1	SID5 to SID0, EID17, EID16
4005 0200h + 16 × j + 2	EID15 to EID8
4005 0200h + 16 × j + 3	EID7 to EID0
4005 0200h + 16 × j + 4	—
4005 0200h + 16 × j + 5	Data length code (DLC[3:0])
4005 0200h + 16 × j + 6	Data byte 0
4005 0200h + 16 × j + 7	Data byte 1
4005 0200h + 16 × j + 8	Data byte 2
4005 0200h + 16 × j + 9	Data byte 3
4005 0200h + 16 × j + 10	Data byte 4
4005 0200h + 16 × j + 11	Data byte 5
4005 0200h + 16 × j + 12	Data byte 6
4005 0200h + 16 × j + 13	Data byte 7
4005 0200h + 16 × j + 14	Upper byte time stamp
4005 0200h + 16 × j + 15	Lower byte time stamp

Table 30.5 CAN data frame configuration

SID10 to SID6	SID5 to SID0	EID17 to EID16	EID15 to EID8	EID7 to EID0	DLC3 to DLC1	DATA0	DATA1	…	DATA7

The previous value of each mailbox is saved unless a new message is received.

Address(es): CAN0.MB0_ID 4005 0200h to CAN0.MB31_ID 4005 03F0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IDE	RTR	—	SID[10:0]											EID[17:0]	
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	EID[17:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b17 to b0	EID[17:0]	Extended ID*1	Extended ID of the data and remote frames	R/W
b28 to b18	SID[10:0]	Standard ID	Standard ID of the data and remote frames	R/W
b29	—	Reserved	This bit is read as undefined. The write value should be 0.	R/W
b30	RTR	Remote Transmission Request	0: Data frame 1: Remote frame.	R/W
b31	IDE	ID Extension*2	0: Standard ID 1: Extended ID.	R/W

Note 1. If the mailbox receives a standard ID message, the EID bits in the mailbox are undefined.
Note 2. The IDE bit is enabled when the IDFM[1:0] bits in CTLR are 10b (mixed ID mode). When the IDFM[1:0] bits are not 10b, only write 0. It reads as 0.

Address(es): CAN0.MB0_DL 4005 0204h to CAN0.MB31_DL 4005 03F4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	DLC[3:0]			
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	DLC[3:0]	Data Length Code*1	b3 b0 0 0 0 0: Data length = 0 byte 0 0 0 1: Data length = 1 byte 0 0 1 0: Data length = 2 bytes 0 0 1 1: Data length = 3 bytes 0 1 0 0: Data length = 4 bytes 0 1 0 1: Data length = 5 bytes 0 1 1 0: Data length = 6 bytes 0 1 1 1: Data length = 7 bytes 1 x x x: Data length = 8 bytes.	R/W
b15 to b4	—	Reserved	These bits are read as undefined. The write value should be 0.	R/W

x: Don't care
Note 1. If the mailbox receives a message with data length (set in DLC[3:0]) of n bytes, where n is less than 8, the data in the DATAn to DATA7 registers in the mailbox is undefined. DATA0 to DATA7 are data registers for this mailbox. For example, if data length is 6 bytes (DLC[3:0] = 6h), the data in DATA6 and DATA7 registers is undefined.

Address(es): CAN0.MB0_D0 4005 0206h to CAN0.MB31_D0 4005 03F6h

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA0							
Value after reset:	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D1 4005 0207h to CAN0.MB31_D1 4005 03F7h

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA1							
Value after reset:	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D2 4005 0208h to CAN0.MB31_D2 4005 03F8h

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA2							
Value after reset:	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D3 4005 0209h to CAN0.MB31_D3 4005 03F9h

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA3							
Value after reset:	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D4 4005 020Ah to CAN0.MB31_D4 4005 03FAh

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA4							
Value after reset:	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D5 4005 020Bh to CAN0.MB31_D5 4005 03FBh

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA5							
Value after reset:	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D6 4005 020Ch to CAN0.MB31_D6 4005 03FCh

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA6							
Value after reset:	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D7 4005 020Dh to CAN0.MB31_D7 4005 03FDh

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA7							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b7 to b0	DATA0 to DATA7	Data Bytes 0 to 7*1,*2	DATA0 to DATA7 store the transmitted or received CAN message data. Transmission or reception starts from DATA0. The bit order on the CAN bus is MSB-first, and transmission or reception starts from bit 7.	R/W

Note 1. If the mailbox receives a message with n bytes where n is less than 8 bytes, the values of DATAn to DATA7 in the mailbox are undefined.

Note 2. If the mailbox receives a remote frame, the previous values of DATA0 to DATA7 in the mailbox are saved.

Address(es): CAN0.MB0_TS 4005 020Eh to CAN0.MB31_TS 4005 03FEh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TSH[7:0]								TSL[7:0]							
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b7 to b0	TSL[7:0]	Time Stamp Lower Byte	Bits TSH[7:0] and TSL[7:0] store the counter value of the time stamp when received messages are stored in the mailbox.	R/W
b15 to b8	TSH[7:0]	Time Stamp Higher Byte		R/W

EID[17:0] bits (Extended ID)

The EID[17:0] bits set the extended ID of data frames and remote frames. They are used to transmit or receive extended ID messages.

SID[10:0] bits (Standard ID)

The SID[10:0] bits set the standard ID of data frames and remote frames. They are used to transmit or receive both standard ID and extended ID messages.

RTR bit (Remote Transmission Request)

The RTR bit sets the frame format to data frames or remote frames.

- The receive mailbox only receives frames with the format specified in the RTR bit
- The transmit mailbox transmits with the frame format specified in the RTR bit
- The receive FIFO mailbox receives the data frame, remote frame, or both frames, as specified in the RTR bit in FIDCR0 and FIDCR1
- The transmit FIFO mailbox transmits the data or remote frame, as specified in the RTR bit in the transmit message.

IDE bit (ID Extension)

The IDE bit sets the ID format to standard ID or extended ID. The IDE bit is enabled when the IDFM[1:0] bits in CTLR are 10b (mixed ID mode).

- The receive mailbox only receives the ID format specified in the IDE bit
- The transmit mailbox transmits with the ID format specified in the IDE bit
- The receive FIFO mailbox receives messages with the standard ID and extended ID settings specified in the IDE bits in FIDCR0 and FIDCR1
- The transmit FIFO mailbox transmits messages with the standard ID or extended ID specified in the IDE bit in the associated transmit message.

DLC[3:0] bits (Data Length Code)

The DLC[3:0] bits specify the data length to be transmitted in data frames. When a remote frame is used to request data,

this field specifies the requested data length.

When a data frame is received, the received data length is stored in this field. When a remote frame is received, this field stores the requested data length.

30.2.7 Mailbox Interrupt Enable Register (MIER)

Address(es): CAN0.MIER 4005 042Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MB31	MB30	MB29	MB28	MB27	MB26	MB25	MB24	MB23	MB22	MB21	MB20	MB19	MB18	MB17	MB16
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MB15	MB14	MB13	MB12	MB11	MB10	MB9	MB8	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b31 to b0	MB31 to MB0	Interrupt Enable	0: Disable interrupt 1: Enable interrupt. Bit [31] is associated with mailbox 31 (MB31), and bit [0] with mailbox 0 (MB0).	R/W

The MIER register can enable interrupts for each mailbox, independently. This register is available in normal mailbox mode. Do not access this register in FIFO mailbox mode.

Each bit is associated with the mailbox having the same number. These bits enable or disable transmission and reception complete interrupts for the associated mailboxes.

- Bit [0] in MIER corresponds to mailbox 0 (MB0)
- Bit [31] in MIER corresponds to mailbox 31 (MB31).

Write to MIER only when the associated MCTL_TXj or MCTL_RXj (j = 0 to 31) register is 00h and the associated mailbox is not processing a transmission or reception abort request.

30.2.8 Mailbox Interrupt Enable Register for FIFO Mailbox Mode (MIER_FIFO)

Address(es): CAN0.MIER_FIFO 4005 042Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	MB29	MB28	—	—	MB25	MB24	MB23	MB22	MB21	MB20	MB19	MB18	MB17	MB16
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MB15	MB14	MB13	MB12	MB11	MB10	MB9	MB8	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b23 to b0	MB23 to MB0	Interrupt Enable	0: Disable interrupt 1: Enable interrupt. Bit [23] is associated with mailbox 23 (MB23), and bit [0] with mailbox 0 (MB0).	R/W

Bit	Symbol	Bit name	Description	R/W
b24	MB24	Transmit FIFO Interrupt Enable	0: Disable interrupt 1: Enable interrupt.	R/W
b25	MB25	Transmit FIFO Interrupt Generation Timing Control	0: Generate every time transmission completes 1: Generate when the transmit FIFO empties on transmission completion.	R/W
b27, b26	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b28	MB28	Receive FIFO Interrupt Enable	0: Disable interrupt 1: Enable interrupt.	R/W
b29	MB29	Receive FIFO Interrupt Generation Timing Control*1	0: Generate every time reception completes 1: Generate when the receive FIFO becomes a buffer warning*2 on reception completion.	R/W
b31, b30	—	Reserved	The read value is undefined. The write value should be 0.	R/W

Note 1. No interrupt request occurs when the receive FIFO becomes a buffer warning because it is full.
Note 2. "Buffer warning" indicates a state in which the third message is stored in the receive FIFO.

The MIER_FIFO register can individually enable interrupts for each mailbox and FIFO. This register is available in FIFO mailbox mode. Do not access it in normal mailbox mode.

The MB0 to MB23 bits are associated with the mailbox having the same number. These bits enable or disable transmission and reception complete interrupts for the associated mailboxes.

- Bit [0] in MIER_FIFO corresponds to mailbox 0 (MB0)
- Bit [23] in MIER_FIFO corresponds to mailbox 23 (MB23).

MB24, MB25, MB28 and MB29 specify whether transmit and receive FIFO interrupts are enabled and the timing of interrupt requests.

Write to the MIER_FIFO register only when the associated MCTL_TXj or MCTL_RXj (j = 0 to 31) register is 00h and the associated mailbox is not processing a transmission or reception abort request. In addition, change the bits in MIER_FIFO for the selected FIFO only when the following conditions are met:

- The TFE bit in TFCR is 0 and the TFEST bit is 1
- The RFE bit in RFCR is 0 and the RFEST bit in RFCR is 1.

30.2.9 Message Control Register for Transmit (MCTL_TXj) (j = 0 to 31)

- Transmit mode (when the TRMREQ bit is 1 and the RECREQ bit is 0)

Address(es): CAN0.MCTL_TX[0] 4005 0820h to CAN0.MCTL_TX[31] 4005 083Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	TRMREQ	RECREQ	—	ONESHOT	—	TRMABT	TRMACTIVE	SENTDATA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SENTDATA	Transmission Complete Flag *1,*2	0: Transmission not complete 1: Transmission complete.	R/W
b1	TRMACTIVE	Transmission-in-Progress Status Flag	0: Transmission pending or not requested 1: Transmission in progress.	R
b2	TRMABT	Transmission Abort Complete Flag*1,*2	0: Transmission started, transmission abort failed because transmission completed, or transmission abort not requested 1: Transmission abort complete.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit name	Description	R/W
b4	ONESHOT	One-Shot Enable*2,*3	0: Disable one-shot transmission 1: Enable one-shot transmission.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	RECREQ	Receive Mailbox Request *2,*3,*4,*5	0: Do not configure for reception 1: Configure for reception.	R/W
b7	TRMREQ	Transmit Mailbox Request *2,*4	0: Do not configure for transmission 1: Configure for transmission.	R/W

Note 1. Write 0 only. Writing 1 has no effect.
Note 2. When writing to bits of this register, write 1 to the SENTDATA and TRMABT flags if these bits are not the write target.
Note 3. To enter one-shot transmit mode, write 1 to the ONESHOT bit at the same time as setting the TRMREQ bit to 1. To exit one-shot transmit mode, write 0 to the ONESHOT bit after the message is transmitted or aborted.
Note 4. Do not set both the RECREQ and TRMREQ bits to 1.
Note 5. When setting the RECREQ bit to 0, set the SENDDATA, TRMACTIVE, and TRMABT flags to 0 simultaneously.

The MCTL_TXj register sets mailbox j to transmit or receive mode. In transmit mode, MCTL_TXj also controls and indicates the status of transmission. Do not access MCTL_TXj if mailbox j is in receive mode. Only write to MCTL_TXj in CAN operation mode or CAN halt mode. Do not use the MCTL_TX24 to MCTL_TX31 registers in FIFO mailbox mode.

SENTDATA flag (Transmission Complete Flag)

The SENTDATA flag is set to 1 when data transmission from the associated mailbox is complete. The SENTDATA flag is set to 0 through a software write. To set the SENTDATA flag to 0, first set the TRMREQ bit to 0. The SENTDATA and TRMREQ bits cannot be set to 0 simultaneously. To transmit a new message from the associated mailbox, set the SENTDATA flag to 0.

TRMACTIVE flag (Transmission-in-Progress Status Flag)

The TRMACTIVE flag is set to 1 when the associated mailbox of the CAN module begins transmitting a message. The TRMACTIVE flag is set to 0 when the CAN module loses CAN bus arbitration, a CAN bus error occurs, or data transmission is complete.

TRMABT flag (Transmission Abort Complete Flag)

The TRMABT flag is set to 1 in the following cases:

- Following a transmission abort request, when the transmission abort is complete before starting transmission
- Following a transmission abort request, when the CAN module detects CAN bus arbitration-lost or CAN bus error
- In one-shot transmission mode (RECREQ bit = 0, TRMREQ bit = 1, and ONESHOT bit = 1), when the CAN module detects CAN bus arbitration-lost or a CAN bus error.

The TRMABT flag is not set to 1 when data transmission is complete. The SENTDATA flag is set to 1 and the TRMABT flag is set to 0 through a software write.

ONESHOT bit (One-Shot Enable)

When the ONESHOT bit is set to 1 in transmit mode (RECREQ bit = 0 and TRMREQ bit = 1), the CAN module transmits a message only one time. The CAN module does not transmit the message again if a CAN bus error or CAN bus arbitration-lost error occurs. When transmission is complete, the SENTDATA flag is set to 1. If transmission does not complete because of a CAN bus error or CAN bus arbitration-lost error, the TRMABT flag is set to 1. Set the ONESHOT bit to 0 after the SENTDATA or TRMABT flag is set to 1.

RECREQ bit (Receive Mailbox Request)

The RECREQ bit selects the receive modes listed in Table 30.10.

When the RECREQ bit is set to 1, the associated mailbox is configured for reception of a data or remote frame.

When the RECREQ bit is set to 0, the associated mailbox is not configured for reception of a data or remote frame.

Due to hardware protection, the RECREQ bit cannot be set to 0 through a software write during the following period:

- Hardware protection is started from acceptance filter processing (the beginning of the CRC field)
- Hardware protection is released:
  - For the mailbox that is specified to receive the incoming message, after the received data is stored in the mailbox or a CAN bus error occurs. This means that the maximum period of hardware protection is from the beginning of the CRC field to the end of the 7th bit of EOF.
  - For the other mailboxes, after acceptance filter processing
  - If no mailbox is specified to receive the message, after acceptance filter processing.

When setting the RECREQ bit to 1, do not set the TRMREQ bit to 1. To change the configuration of a mailbox from transmission to reception, first abort the transmission, then set the SENTDATA and TRMABT flags to 0 before changing to reception.

Note: MCTL_TXj.RECREQ is the mirror bit of MCTL_RXj.REQREQ.

TRMREQ bit (Transmit Mailbox Request)

The TRMREQ bit selects the transmit modes listed in Table 30.10.

When the TRMREQ bit is set to 1, the associated mailbox is configured for transmission of a data or remote frame.

When the TRMREQ bit is set to 0, the associated mailbox is not configured for transmission of a data or remote frame.

If the TRMREQ bit is changed from 1 to 0 to cancel the associated transmission request, either the TRMABT or SENTDATA flag is set to 1. When setting the TRMREQ bit to 1, do not set the RECREQ bit to 1. To change the configuration of a mailbox from reception to transmission, first abort the reception, then set the NEWDATA and MSGLOST flags to 0 before changing to transmission.

Note: MCTL_TXj.TRMREQ is the mirror bit of MCTL_RXj.TRMREQ.

30.2.10 Message Control Register for Receive (MCTL_RXj) (j = 0 to 31)

- Receive mode (when the TRMREQ bit is 0 and the RECREQ bit is 1)

Address(es): CAN0.MCTL_RX[0] 4005 0820h to CAN0.MCTL_RX[31] 4005 083Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	TRMREQ	RECREQ	—	ONESHOT	—	MSGLOST	INVALDATA	NEWDATA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	NEWDATA	Reception Complete Flag*1,*2	0: No data received, or 0 was written to the bit 1: New message being stored or was stored to the mailbox.	R/W
b1	INVALDATA	Reception-in-Progress Status Flag	0: Message valid 1: Message being updated.	R
b2	MSGLOST	Message Lost Flag*1,*2	0: Message not overwritten or overrun 1: Message overwritten or overrun.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	ONESHOT	One-Shot Enable*2,*3	0: Disable one-shot reception 1: Enable one-shot reception.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	RECREQ	Receive Mailbox Request *2,*3,*4,*5	0: Do not configure for reception 1: Configure for reception.	R/W
b7	TRMREQ	Transmit Mailbox Request *2,*4	0: Do not configure for transmission 1: Configure for transmission.	R/W

Note 1. Write 0 only. Writing 1 has no effect.
Note 2. When writing to bits of this register, write 1 to NEWDATA and MSGLOST if these bits are not the write target.
Note 3. To enter one-shot receive mode, write 1 to the ONESHOT bit at the same time as setting the RECREQ bit to 1. To exit one-shot receive mode, write 0 to the ONESHOT bit after writing 0 to the RECREQ bit and confirming that it is 0.
Note 4. Do not set both the RECREQ and TRMREQ bits to 1.
Note 5. When setting the RECREQ bit to 0, set the MSGLOST, NEWDATA flags, and RECREQ bit to 0 simultaneously.

The MCTL_RXj register sets mailbox j to transmit or receive mode. In receive mode, MCTL_RXj also controls and indicates the status of reception. Do not access MCTL_RXj if mailbox j is in transmit mode. Only write to MCTL_RXj in CAN operation mode or CAN halt mode. Do not use MCTL_RX24 to MCTL_RX31 in FIFO mailbox mode.

NEWDATA flag (Reception Complete Flag)

The NEWDATA flag is set to 1 when a new message is being stored or was stored in the mailbox. Always set this bit to 1 simultaneously with the INVALDATA flag. The NEWDATA flag is set to 0 through a software write. The NEWDATA flag cannot be set to 0 through a software write when the associated INVALDATA flag is 1.

INVALDATA flag (Reception-in-Progress Status Flag)

After the completion of a message reception, the INVALDATA flag is set to 1 while the received message is being updated in the associated mailbox. The INVALDATA flag is set to 0 immediately after the message is stored. If the mailbox is read when the INVALDATA flag is 1, the data is undefined.

MSGLOST flag (Message Lost Flag)

The MSGLOST flag is set to 1 when the mailbox is overwritten or overrun by a new received message while the NEWDATA flag is 1. The MSGLOST flag is set to 1 at the end of bit [6] of EOF. The MSGLOST flag is set to 0 through a software write.

In both overwrite and overrun modes, the MSGLOST flag cannot be set to 0 through a software write during the 5 PCLKB cycles following the 6th bit of EOF.

ONESHOT bit (One-Shot Enable)

When the ONESHOT bit is set to 1 in receive mode (RECREQ = 1 and TRMREQ = 0), the mailbox receives a message only one time. The mailbox does not behave as a receive mailbox after having received a message one time. The behavior of the NEWDATA and INVALDATA flags is the same as in normal receive mode. In one-shot receive mode, the MSGLOST flag is not set to 1. To set the ONESHOT bit to 0, first write 0 to the RECREQ bit and ensure that it is 0.

RECREQ bit (Receive Mailbox Request)

The RECREQ bit selects the receive modes listed in Table 30.10.

When the RECREQ bit is set to 1, the associated mailbox is configured for reception of a data frame or remote frame.

When the RECREQ bit is set to 0, the associated mailbox is not configured for reception of a data frame or remote frame.

Due to hardware protection, the RECREQ bit cannot be set to 0 through a software write during the following:

- Hardware protection is started from acceptance filter processing (the beginning of CRC field)
- Hardware protection is released:
  - For the mailbox that is specified to receive the incoming message, after the received data is stored in the mailbox or a CAN bus error occurs. The maximum period of hardware protection is from the beginning of the CRC field to the end of 7th bit of EOF.
  - For the other mailboxes, after acceptance filter processing
  - If no mailbox is specified to receive the message, after acceptance filter processing.

When setting the RECREQ bit to 1, do not set the TRMREQ bit to 1. To change the configuration of a mailbox from transmission to reception, first abort the transmission, then set the SENTDATA and TRMABT flags to 0 before changing to reception.

Note: MCTL_RXj.RECREQ is the mirror bit of MCTL_TXj.REQREQ.

TRMREQ bit (Transmit Mailbox Request)

The TRMREQ bit selects the transmit modes listed in Table 30.10.

When the TRMREQ bit is set to 1, the associated mailbox is configured for transmission of a data frame or remote frame.

When the TRMREQ bit is set to 0, the associated mailbox is not configured for transmission of a data frame or remote frame.

If the TRMREQ bit is changed from 1 to 0 to cancel the associated transmission request, either the TRMABT or SENTDATA flag is set to 1. When setting the TRMREQ bit to 1, do not set the RECREQ bit to 1. To change the configuration of a mailbox from reception to transmission, first abort the reception, then set the NEWDATA and MSGLOST flags to 0 before changing to transmission.

Note: MCTL_RXj.TRMREQ is the mirror bit of MCTL_TXj.TRMREQ.

30.2.11 Receive FIFO Control Register (RFCR)

Address(es): CAN0.RFCR 4005 0848h

	b7	b6	b5	b4	b3	b2	b1	b0
	RFEST	RFWST	RFFST	RFMLF	RFUST[2:0]			RFE
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RFE	Receive FIFO Enable	0: Disable receive FIFO 1: Enable receive FIFO.	R/W
b3 to b1	RFUST[2:0]	Receive FIFO Unread Message Number Status	b3 b1 0 0 0: No unread message 0 0 1: 1 unread message 0 1 0: 2 unread messages 0 1 1: 3 unread messages 1 0 0: 4 unread messages 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved.	R
b4	RFMLF	Receive FIFO Message Lost Flag	0: Receive FIFO message not lost 1: Receive FIFO message lost.	R/W
b5	RFFST	Receive FIFO Full Status Flag	0: Receive FIFO not full 1: Receive FIFO full (4 unread messages)	R
b6	RFWST	Receive FIFO Buffer Warning Status Flag	0: Receive FIFO is not buffer warning 1: Receive FIFO is buffer warning (3 unread messages).	R
b7	RFEST	Receive FIFO Empty Status Flag	0: Unread message in receive FIFO 1: No unread message in receive FIFO.	R

Write to the RFCR register in CAN operation mode or CAN halt mode.

RFE bit (Receive FIFO Enable)

When the RFE bit is set to 1, the receive FIFO is enabled. When the RFE bit is set to 0, the receive FIFO is disabled for reception and becomes empty (RFEST = 1). Write 0 to the RFE bit simultaneously with the RFMLF flag setting.

Do not set the RFE bit to 1 in normal mailbox mode (MBM bit in CTLR = 0).

Due to hardware protection, the RFE bit cannot be set to 0 through a software write during the following period:

- Hardware protection is started from acceptance filter processing (the beginning of the CRC field)
- Hardware protection is released:
  - If the receive FIFO is specified to receive the incoming message, after the received data is stored in the receive FIFO or a CAN bus error occurs. This means that the maximum period of hardware protection is from the beginning of CRC field to the end of the 7th bit of EOF.

- If the receive FIFO is not specified to receive the message, after acceptance filter processing.

RFUST[2:0] bits (Receive FIFO Unread Message Number Status)

The RFUST[2:0] bits indicate the number of unread messages in the receive FIFO. The value of the RFUST[2:0] bits initializes to 000b when the RFE bit is set to 0.

RFMLF flag (Receive FIFO Message Lost Flag)

The RFMLF flag is set to 1 (receive FIFO message was lost) when the receive FIFO receives a new message and is full. It is set to 1 at the end of the 6th bit of EOF.

The RFMLF flag is set to 0 through a software write (writing 1 has no effect). In both overwrite and overrun modes, if the receive FIFO is full and determined to have received a message, the RFMLF flag cannot be set to 0 (receive FIFO message was not lost) through a software write because of hardware protection during the 5 PCLKB cycles following the 6th bit of EOF.

RFFST flag (Receive FIFO Full Status Flag)

The RFFST flag is set to 1 (receive FIFO is full) when the number of unread messages in the receive FIFO is 4. It is 0 (receive FIFO is not full) when the number of unread messages in the receive FIFO is less than 4. The flag is set to 0 when the RFE bit is 0.

RFWST flag (Receive FIFO Buffer Warning Status Flag)

The RFWST flag is set to 1 (receive FIFO is a buffer warning) when the number of unread messages in the receive FIFO is 3. It is 0 (receive FIFO is not a buffer warning) when the number of unread messages in the receive FIFO is less than 3 or equal to 4. The flag is set to 0 when the RFE bit is 0.

RFEST flag (Receive FIFO Empty Status Flag)

The RFEST flag is set to 1 (no unread message in receive FIFO) when the number of unread messages in the receive FIFO is 0. It is set to 1 when the RFE bit is set to 0. The flag is set to 0 (unread message in receive FIFO) when the number of unread messages in the receive FIFO is one or more. Figure 30.2 shows the receive FIFO mailbox operation.

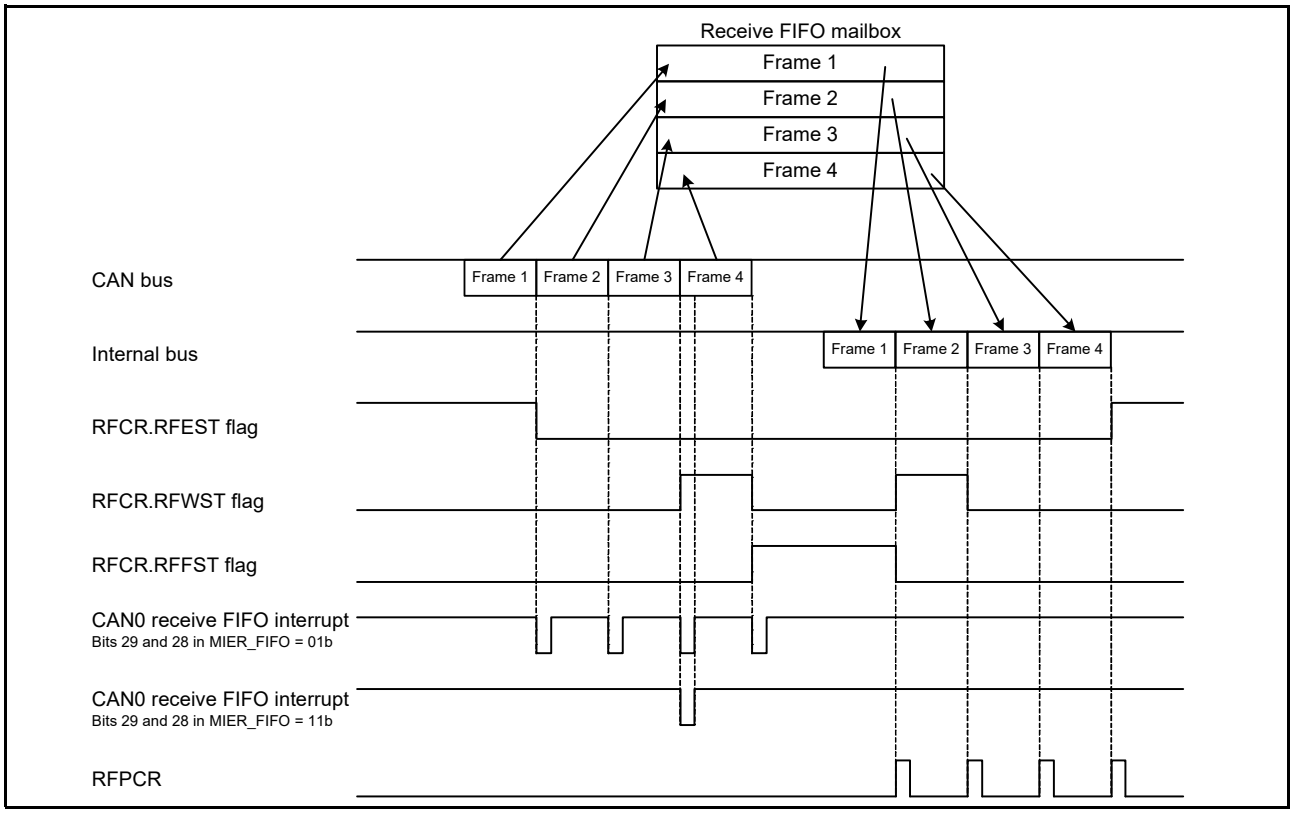


Figure 30.2 Receive FIFO mailbox operation, when bits [29] and [28] in MIER_FIFO = 01b or 11b

30.2.12 Receive FIFO Pointer Control Register (RFPCR)

Address(es): CAN0.RFPCR 4005 0849h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Description	R/W
b7 to b0	The CPU pointer for the receive FIFO is incremented by writing FFh to RFPCR	W

When the receive FIFO is not empty, write FFh to the RFPCR register through software to increment the CPU pointer to the next mailbox location. Do not write to RFPCR when the RFE bit in RFCR is 0 (receive FIFO disabled).

Both the CAN and CPU pointers increment when a new message is received and the RFFST bit is 1 (receive FIFO is full) in overwrite mode. When RFMLF is 1 in this state, the CPU pointer does not increment on a software write to RFPCR.

30.2.13 Transmit FIFO Control Register (TFCR)

Address(es): CAN0.TFCR 4005 084Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	TFEST	TFFST	—	—	TFUST[2:0]			TFE
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TFE	Transmit FIFO Enable	0: Disable transmit FIFO 1: Enable transmit FIFO.	R/W
b3 to b1	TFUST[2:0]	Transmit FIFO Unsent Message Number Status	b3 b1 0 0 0: 0 unsent messages 0 0 1: 1 unsent message 0 1 0: 2 unsent messages 0 1 1: 3 unsent messages 1 0 0: 4 unsent messages 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved.	R
b5, b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	TFFST	Transmit FIFO Full Status	0: Transmit FIFO not full 1: Transmit FIFO full (4 unsent messages).	R
b7	TFEST	Transmit FIFO Empty Status	0: Unsent message in transmit FIFO 1: No unsent message in transmit FIFO.	R

Write to the TFCR register in CAN operation mode or CAN halt mode.

TFE bit (Transmit FIFO Enable)

Setting the TFE bit to 1 enables the transmit FIFO. Setting the TFE bit to 0 empties the transmit FIFO (TFEST bit = 1), and unsent messages in the transmit FIFO are lost in the following ways:

- Immediately if a message from the transmit FIFO is not scheduled for the next transmission or already in transmission
- On completion of transmission, a CAN bus error, CAN bus arbitration-lost, or entry to CAN halt mode, if a message from the transmit FIFO is scheduled for the next transmission or already in transmission.

Before setting the TFE bit to 1 again, ensure that the TFEST bit is set to 1. After setting the TFE bit to 1, write transmit data to mailbox 24.

Do not set the TFE bit to 1 in normal mailbox mode (MBM bit in CTLR = 0).

TFUST[2:0] bits (Transmit FIFO Unsent Message Number Status)

The TFUST[2:0] bits indicate the number of unsent messages in the transmit FIFO. They are set to 000b after the TFE bit is set to 0 and transmission aborts or completes.

TFFST bit (Transmit FIFO Full Status)

The TFFST bit is set to 1 (transmit FIFO is full) when the number of unsent messages in the transmit FIFO is 4. The TFFST bit is set to 0 (transmit FIFO is not full) when the number of unsent messages in the transmit FIFO is less than 4. The TFFST bit is set to 0 when transmission from the transmit FIFO is aborted.

TFEST bit (Transmit FIFO Empty Status)

The TFEST bit is set to 1 (no message in transmit FIFO) when the number of unsent messages in the transmit FIFO is 0. The TFEST bit is set to 1 when transmission from the transmit FIFO is aborted. The TFEST bit is set to 0 (message in transmit FIFO) when the number of unsent messages in the transmit FIFO is not 0.

Figure 30.3 shows the transmit FIFO mailbox operation.

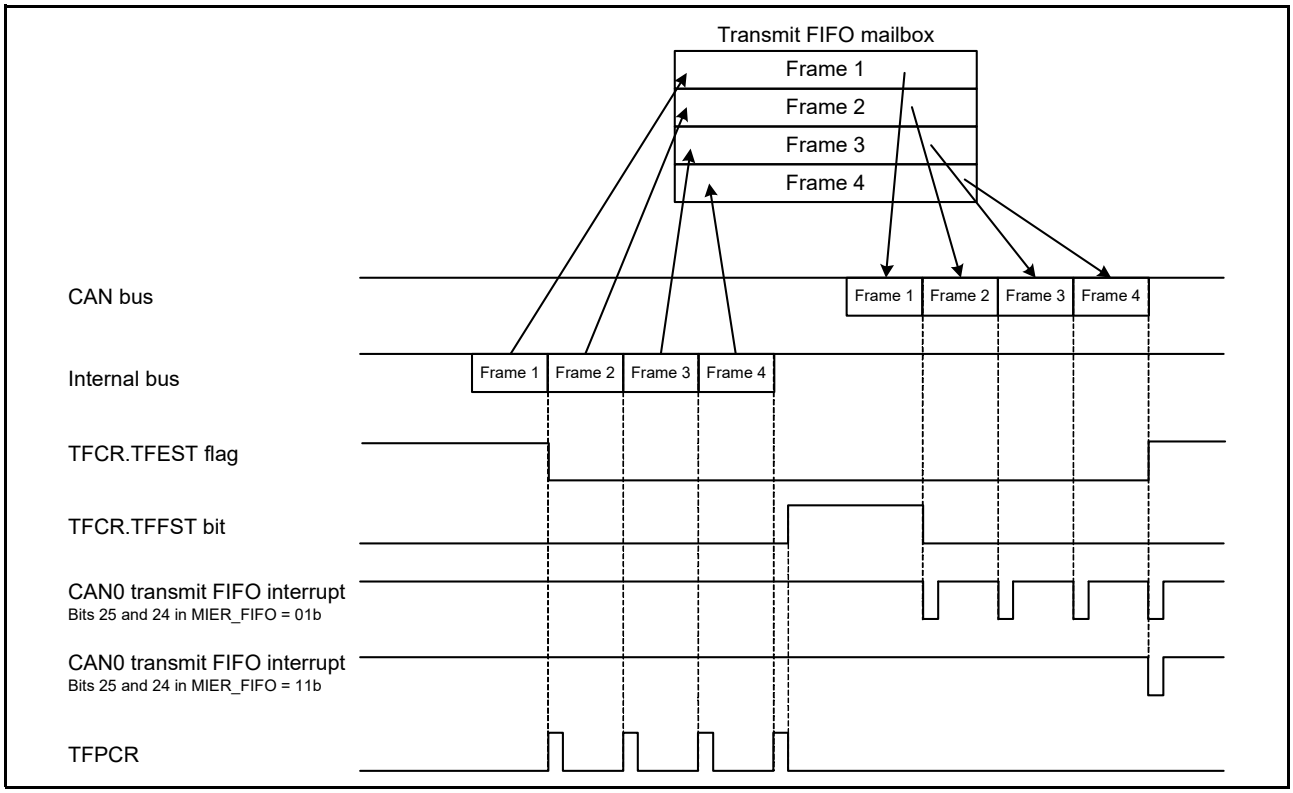


Figure 30.3 Transmit FIFO mailbox operation when bits [25] and [24] in MIER_FIFO = 01b or 11b

30.2.14 Transmit FIFO Pointer Control Register (TFPCR)

Address(es): CAN0.TFPCR 4005 084Bh

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Description	R/W
b7 to b0	The CPU pointer for the transmit FIFO is incremented by writing FFh to TFPCR	W

When the transmit FIFO is not full, write FFh to the TFPCR register through software to increment the CPU pointer for the transmit FIFO to the next mailbox location.

Do not write to TFPCR when the TFE bit in TFCR is 0 (transmit FIFO disabled).

30.2.15 Status Register (STR)

Address(es): CAN0.STR 4005 0842h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	RECST	TRMST	BOST	EPST	SLPST	HLTST	RSTST	EST	TABST	FMLST	NMLST	TFST	RFST	SDST	NDST
Value after reset:	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	NDST	NEWDATA Status Flag	0: No mailbox with NEWDATA flag = 1 1: 1 or more mailboxes with NEWDATA flag = 1.	R
b1	SDST	SENTDATA Status Flag	0: No mailbox with SENTDATA flag = 1 1: 1 or more mailboxes with SENTDATA flag = 1.	R
b2	RFST	Receive FIFO Status Flag	0: Receive FIFO empty 1: Message in receive FIFO.	R
b3	TFST	Transmit FIFO Status Flag	0: Transmit FIFO full 1: Transmit FIFO not full.	R
b4	NMLST	Normal Mailbox Message Lost Status Flag	0: No mailbox with MSGLOST flag = 1 1: 1 or more mailboxes with MSGLOST flag = 1.	R
b5	FMLST	FIFO Mailbox Message Lost Status Flag	0: RFMLF flag = 0 1: RFMLF flag = 1	R
b6	TABST	Transmission Abort Status Flag	0: No mailbox with TRMABT flag = 1 1: 1 or more mailboxes with TRMABT flag = 1.	R
b7	EST	Error Status Flag	0: No error occurred 1: Error occurred.	R
b8	RSTST	CAN Reset Status Flag	0: Not in CAN reset mode 1: In CAN reset mode.	R
b9	HLTST	CAN Halt Status Flag	0: Not in CAN halt mode 1: In CAN halt mode.	R
b10	SLPST	CAN Sleep Status Flag	0: Not in CAN sleep mode 1: In CAN sleep mode.	R
b11	EPST	Error-Passive Status Flag	0: Not in error-passive state 1: In error-passive state.	R
b12	BOST	Bus-Off Status Flag	0: Not in bus-off state 1: In bus-off state.	R

Bit	Symbol	Bit name	Description	R/W
b13	TRMST	Transmit Status Flag	0: Bus idle or reception in progress 1: Transmission in progress or module in bus-off state.	R
b14	RECST	Receive Status Flag	0: Bus idle or transmission in progress 1: Reception in progress.	R
b15	—	Reserved	This bit is read as 0.	R

NDST flag (NEWDATA Status Flag)

The NDST flag is set to 1 when at least one NEWDATA flag in MCTL_RXj (j = 0 to 31) is 1, regardless of the value of MIER or MIER_FIFO. It is set to 0 when all NEWDATA flags are 0.

SDST flag (SENTDATA Status Flag)

The SDST flag is set to 1 when at least one SENTDATA flag in MCTL_TXj (j = 0 to 31) is 1, regardless of the value of MIER or MIER_FIFO. It is set to 0 when all SENTDATA flags are 0.

RFST flag (Receive FIFO Status Flag)

The RFST flag is set to 1 when the receive FIFO is not empty. It is set to 0 when the receive FIFO is empty or normal mailbox mode is selected.

TFST flag (Transmit FIFO Status Flag)

The TFST flag is set to 1 when the transmit FIFO is not full. It is set to 0 when the transmit FIFO is full or normal mailbox mode is selected.

NMLST flag (Normal Mailbox Message Lost Status Flag)

The NMLST flag is set to 1 when at least one MSGLOST flag in MCTL_RXj (j = 0 to 31) is 1, regardless of the value of MIER or MIER_FIFO. It is set to 0 when all MSGLOST flags are 0.

FMLST flag (FIFO Mailbox Message Lost Status Flag)

The FMLST flag is set to 1 when the RFMLF flag in RFCR is 1, regardless of the value of MIER_FIFO. The FMLST flag is set to 0 when the RFMLF flag is 0.

TABST flag (Transmission Abort Status Flag)

The TABST flag is set to 1 when at least one TRMABT flag in MCTL_TXj (j = 0 to 31) is 1, regardless of the value of MIER or MIER_FIFO. It is set to 0 when all TRMABT flags are 0.

EST flag (Error Status Flag)

The EST flag is set to 1 when at least one error is detected by EIFR, regardless of the value of EIER. It is set to 0 when no error is detected by EIFR.

RSTST flag (CAN Reset Status Flag)

The RSTST flag is set to 1 when the CAN module is in CAN reset mode. It is 0 when the CAN module is not in CAN reset mode. It remains 1, even when the state changes from CAN reset mode to CAN sleep mode.

HLTST flag (CAN Halt Status Flag)

The HLTST flag is set to 1 when the CAN module is in CAN halt mode. It is set to 0 when the CAN module is not in CAN halt mode. It remains 1, even when the state changes from CAN halt mode to CAN sleep mode.

SLPST flag (CAN Sleep Status Flag)

The SLPST flag is set to 1 when the CAN module is in CAN sleep mode. It is set to 0 when the CAN module is not in CAN sleep mode.

EPST flag (Error-Passive Status Flag)

The EPST flag is set to 1 when the value of TECR or RECR exceeds 127 and the CAN module is in the error-passive state (128 ≤ TEC < 256 or 128 ≤ REC < 256). It is set to 0 when the CAN module is not in the error-passive state.

BOST flag (Bus-Off Status Flag)

The BOST flag is set to 1 when the value of TECR exceeds 255 and the CAN module is in the bus-off state (TEC ≥ 256). It is set to 0 when the CAN module is not in the bus-off state.

TRMST flag (Transmit Status Flag)

The TRMST flag is set to 1 when the CAN module performs as a transmitter node or is in the bus-off state. It is set to 0 when the CAN module performs as a receiver node or is in the bus-idle state.

RECST flag (Receive Status Flag)

The RECST flag is set to 1 when the CAN module performs as a receiver node. It is set to 0 when the CAN module performs as a transmitter node or is in the bus-idle state.

30.2.16 Mailbox Search Mode Register (MSMR)

Address(es): CAN0.MSMR 4005 0853h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	MBSM[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	MBSM[1:0]	Mailbox Search Mode Select	b1 b0 0 0: Receive mailbox search mode 0 1: Transmit mailbox search mode 1 0: Message lost search mode 1 1: Channel search mode.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Write to the MSMR register in CAN operation mode or CAN halt mode.

MBSM[1:0] bits (Mailbox Search Mode Select)

The MBSM[1:0] bits select the search mode for the mailbox search function.

When the MBSM[1:0] bits are 00b, receive mailbox search mode is selected. In this mode, the search targets are the NEWDATA flag in MCTL_RXj (j = 0 to 31) for the normal mailbox and the RFEST flag in RFCR.

When the MBSM[1:0] bits are 01b, transmit mailbox search mode is selected. In this mode, the search target is the SENTDATA flag in MCTL_TXj.

When the MBSM[1:0] bits are 10b, message lost search mode is selected. In this mode, the search targets are the MSGLOST flag in MCTL_RXj for the normal mailbox and the RFMLF flag in RFCR.

When the MBSM[1:0] bits are 11b, channel search mode is selected. In this mode, the search target is CSSR. See section 30.2.18, Channel Search Support Register (CSSR).

30.2.17 Mailbox Search Status Register (MSSR)

Address(es): CAN0.MSSR 4005 0852h

	b7	b6	b5	b4	b3	b2	b1	b0
	SEST	—	—	MBNST[4:0]				
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	MBNST[4:0]	Search Result Mailbox Number Status	These bits output the smallest mailbox number that is found in each mode of MSMR	R
b6, b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	SEST	Search Result Status	0: Search result found 1: No search result.	R

MBNST[4:0] bits (Search Result Mailbox Number Status)

In all MSMR modes, the MBNST[4:0] bits output the smallest found mailbox number. In receive mailbox search mode, transmit mailbox search mode, and message lost search mode, the value of the mailbox (search result to be output) is updated under the following conditions:

- When the NEWDATA, SENTDATA, or MSGLOST flag is set to 0 for a mailbox output by MBNST
- When the NEWDATA, SENTDATA, or MSGLOST flag is set to 1 for a mailbox with a smaller number than that in MBNST.

If the MBSM[1:0] bits are set to 00b (receive mailbox search mode) or 10b (message lost search mode), the receive FIFO (mailbox 28) is output when it is not empty and there are no unread received messages and no lost messages in any of the normal mailboxes (0 to 23). If the MBSM[1:0] bits are set to 01b (transmit mailbox search mode), the transmit FIFO (mailbox 24) is not output. Table 30.6 lists the behavior of the MBNST[4:0] bits in FIFO mailbox mode.

In channel search mode, the MBNST[4:0] bits output the associated channel number. After the MSSR register is read by software, the next target channel number is output.

SEST bit (Search Result Status)

The SEST bit is set to 1 (no search result) when no associated mailbox is found after searching all mailboxes. For example, in transmit mailbox search mode, the SEST bit is set to 1 when no SENTDATA flag for the mailboxes is 1. The SEST bit is set to 0 when at least one SENTDATA flag is 1. When the SEST bit is 1, the value of the MBNST[4:0] bits is undefined.

Table 30.6 Behavior of MBNST[4:0] bits in FIFO mailbox mode

MBSM[1:0] bits	Mailbox 24 (transmit FIFO)	Mailbox 28 (receive FIFO)
00b	Mailbox 24 is not output.	Mailbox 28 is output when no MCTL_RXj.NEWDATA flag for the normal mailboxes is set to 1 (new message is being stored or was stored to the mailbox) and the receive FIFO is not empty
01b		Mailbox 28 is not output
10b		Mailbox 28 is output when no MCTL_RXj.MSGLOST flag for the normal mailboxes is set to 1 (message is overwritten or overrun) and the RFCR.RFMLF bit is set to 1 (receive FIFO message was lost) in the receive FIFO
11b		Mailbox 28 is not output

30.2.18 Channel Search Support Register (CSSR)

Address(es): CAN0.CSSR 4005 0851h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Description	R/W
b7 to b0	When the value for the channel search is input, the channel number is output to MSSR	R/W

The bits in CSSR, which are set to 1, are encoded by an 8/3 encoder (the LSB position has the higher priority) and output to the MBNST[4:0] bits in MSSR. MSSR outputs the updated value whenever MSSR is read by the software.

Write to CSSR only when the MSMR.MBSM[1:0] bits are 11b (channel search mode). Write to CSSR in CAN operation mode or CAN halt mode.

Figure 30.4 shows writes to and reads from CSSR and MSSR.

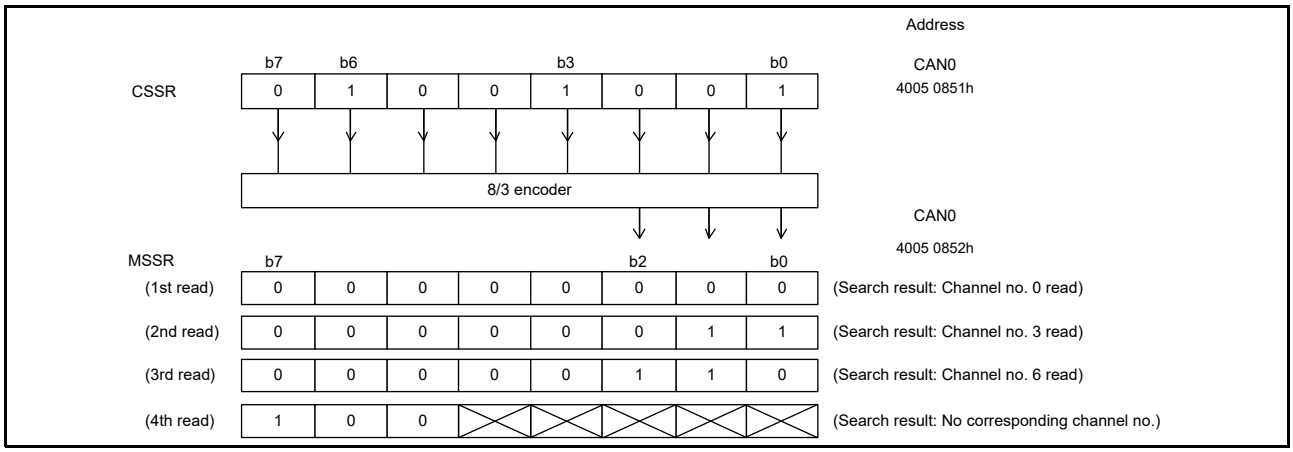


Figure 30.4 Writes to and reads from CSSR and MSSR

The value of CSSR is also updated whenever MSSR is read. On this read, the value prior to conversion by the 8/3 encoder can be read.

30.2.19 Acceptance Filter Support Register (AFSR)

Address(es): CAN0.AFSR 4005 0856h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Description	R/W
b15 to b0	After the standard ID of a received message is written, the value converted for data table search can be read	R/W

Note: Write to AFSR in CAN operation mode or CAN halt mode.

The acceptance filter support unit (ASU) can be used for data table (8 bits × 256) searches. In the data table, all standard IDs that are created are set to be valid or invalid in bit units. When AFSR is written with data in 16-bit units including the

SID[10:0] bits in MBj_ID (j = 0 to 31), in which a received standard ID is stored, a decoded row (byte offset) position and column (bit) position for data table search can be read. The ASU can be used for standard (11-bit) IDs only.

The ASU is enabled in the following cases:

- When the IDs to be received cannot be masked by the acceptance filter, for example if the IDs to be received are 078h, 087h, and 111h
- When there are too many IDs to receive, and the software filtering time is expected to be shortened.

Note: The AFSR register cannot be set in CAN reset mode.

Figure 30.5 shows writes to and reads from the AFSR register.

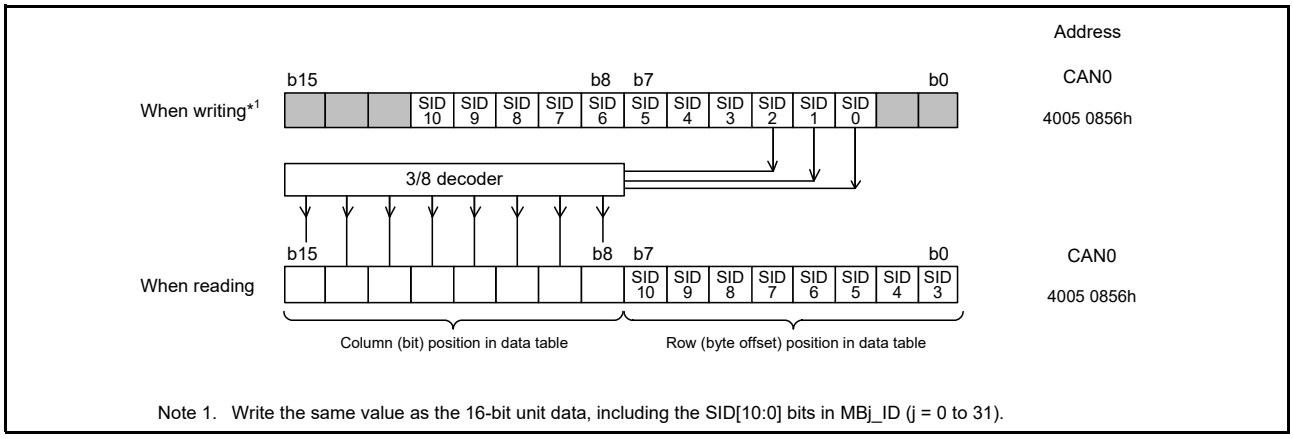


Figure 30.5 Writes to and reads from AFSR

30.2.20 Error Interrupt Enable Register (EIER)

Address(es): CAN0.EIER 4005 084Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	BLIE	OLIE	ORIE	BORIE	BOEIE	EPIE	EWIE	BEIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	BEIE	Bus Error Interrupt Enable	0: Disable interrupt 1: Enable interrupt.	R/W
b1	EWIE	Error-Warning Interrupt Enable	0: Disable interrupt 1: Enable interrupt.	R/W
b2	EPIE	Error-Passive Interrupt Enable	0: Disable interrupt 1: Enable interrupt.	R/W
b3	BOEIE	Bus-Off Entry Interrupt Enable	0: Disable interrupt 1: Enable interrupt.	R/W
b4	BORIE	Bus-Off Recovery Interrupt Enable	0: Disable interrupt 1: Enable interrupt.	R/W
b5	ORIE	Overrun Interrupt Enable	0: Disable interrupt 1: Enable interrupt.	R/W
b6	OLIE	Overload Frame Transmit Interrupt Enable	0: Disable interrupt 1: Enable interrupt.	R/W
b7	BLIE	Bus Lock Interrupt Enable	0: Disable interrupt 1: Enable interrupt.	R/W

The EIER register enables or disables each error interrupt source independently in EIFR. Write to EIER in CAN reset mode.

BEIE bit (Bus Error Interrupt Enable)

When the BEIE bit is 0, no error interrupt request occurs even if the BEIF bit in EIFR is 1. When the BEIE bit is 1, an error interrupt request occurs if the BEIF bit is set to 1.

EWIE bit (Error-Warning Interrupt Enable)

When the EWIE bit is 0, no error interrupt request occurs even if the EWIF bit in EIFR is 1. When the EWIE bit is 1, an error interrupt request occurs if the EWIF bit is set to 1.

EPIE bit (Error-Passive Interrupt Enable)

When the EPIE bit is 0, no error interrupt request occurs even if the EPIF bit in EIFR is 1. When the EPIE bit is 1, an error interrupt request occurs if the EPIF bit is set to 1.

BOEIE bit (Bus-Off Entry Interrupt Enable)

When the BOEIE bit is 0, no error interrupt request occurs even if the BOEIF bit in EIFR is 1. When the BOEIE bit is 1, an error interrupt request occurs if the BOEIF bit is set to 1.

BORIE bit (Bus-Off Recovery Interrupt Enable)

When the BORIE bit is 0, an error interrupt request does not occur even if the BORIF bit in EIFR is 1. When the BORIE bit is set to 1, an error interrupt request occurs if the BORIF bit is set to 1.

ORIE bit (Overrun Interrupt Enable)

When the ORIE bit is 0, an error interrupt request does not occur even if the ORIF bit in EIFR is 1. When the ORIE bit is 1, an error interrupt request occurs if the ORIF bit is set to 1.

OLIE bit (Overload Frame Transmit Interrupt Enable)

When the OLIE bit is 0, no error interrupt request occurs even if the OLIF bit in EIFR is 1. When the OLIE bit is 1, an error interrupt request occurs if the OLIF bit is set to 1.

BLIE bit (Bus Lock Interrupt Enable)

When the BLIE bit is 0, no error interrupt request occurs even if the BLIF bit in EIFR is 1. When the BLIE bit is 1, an error interrupt request occurs if the BLIF bit is set to 1.

30.2.21 Error Interrupt Factor Judge Register (EIFR)

Address(es): CAN0.EIFR 4005 084Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	BLIF	OLIF	ORIF	BORIF	BOEIF	EPIF	EWIF	BEIF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	BEIF	Bus Error Detect Flag	0: No bus error detected 1: Bus error detected.	R/W
b1	EWIF	Error-Warning Detect Flag	0: No error-warning detected 1: Error-warning detected.	R/W
b2	EPIF	Error-Passive Detect Flag	0: No error-passive detected 1: Error-passive detected.	R/W
b3	BOEIF	Bus-Off Entry Detect Flag	0: No bus-off entry detected 1: Bus-off entry detected.	R/W
b4	BORIF	Bus-Off Recovery Detect Flag	0: No bus-off recovery detected 1: Bus-off recovery detected.	R/W
b5	ORIF	Receive Overrun Detect Flag	0: No receive overrun detected 1: Receive overrun detected.	R/W

Bit	Symbol	Bit name	Description	R/W
b6	OLIF	Overload Frame Transmission Detect Flag	0: No overload frame transmission detected 1: Overload frame transmission detected.	R/W
b7	BLIF	Bus Lock Detect Flag	0: No bus lock detected 1: Bus lock detected.	R/W

If an event associated with one of these bit occurs, the associated bit in EIFR is set to 1, regardless of the EIER setting.

Clear the bits to 0 through a software write. If a bit is set to 1 at the same time that the software clears it, it becomes 1. When setting a single bit to 0 in software, use the transfer instruction (MOV) to ensure that only the specified bit is set to 0 and the other bits are set to 1. Writing 1 has no effect on these bit values.

BEIF flag (Bus Error Detect Flag)

The BEIF flag is set to 1 when a bus error is detected.

EWIF flag (Error-Warning Detect Flag)

The EWIF flag is set to 1 when the value of the receive error counter (REC) or transmit error counter (TEC) exceeds 95. It is set to 1 only when REC or TEC initially exceeds 95. If 0 is written to the EWIF flag by software while REC or TEC remains greater than 95, the EWIF flag is not set to 1 until REC or TEC goes below 95 then exceeds 95 again.

EPIF flag (Error-Passive Detect Flag)

The EPIF flag is set to 1 when the CAN error state becomes error-passive, when the receive error counter (REC) or transmit error counter (TEC) exceeds 127. It is set to 1 only when REC or TEC initially exceeds 127. If 0 is written to the EPIF flag by software while REC or TEC remains greater than 127, the EPIF flag is not set to 1 until REC or TEC goes below 127 then exceeds 127 again.

BOEIF flag (Bus-Off Entry Detect Flag)

The BOEIF flag is set to 1 when the CAN error state becomes bus-off, when the transmit error counter (TEC) value exceeds 255. The BOEIF flag is also set to 1 when the BOM[1:0] bits in CTLR are 01b (automatic entry to CAN halt mode on bus-off entry) and the CAN module enters the bus-off state.

BORIF flag (Bus-Off Recovery Detect Flag)

The BORIF flag is set to 1 when the CAN module recovers from the bus-off state normally by detecting 11 consecutive recessive bits 128 times in the following conditions:

- When the BOM[1:0] bits in CTLR are 00b
- When the BOM[1:0] bits in CTLR are 10b
- When the BOM[1:0] bits in CTLR are 11b.

However, the BORIF flag is not set to 1 if the CAN module recovers from the bus-off state in the following conditions:

- When the CANM[1:0] bits in CTLR are set to 01b or 11b (CAN reset mode)
- When the RBOC bit in CTLR is set to 1 (forced return from bus-off)
- When the BOM[1:0] bits in CTLR are set to 01b
- When the BOM[1:0] bits in CTLR are set to 11b and the CANM[1:0] bits in CTLR are set to 10b (CAN halt mode) before normal recovery occurs.

Table 30.7 lists the behavior of the BOEIF and BORIF bits for each CTLR.BOM[1:0] setting.

Table 30.7 Behavior of BOEIF and BORIF flags for each CTLR.BOM[1:0] setting

BOM[1:0] bits	BOEIF flag	BORIF flag
00b	Sets to 1 on entry to bus-off state.	Sets to 1 on exit from bus-off state
01b		Is not set to 1
10b		Sets to 1 on exit from the bus-off state
11b		Sets to 1 if normal bus-off recovery occurs before the CANM[1:0] bits are set to 10b (CAN halt mode)

ORIF flag (Receive Overrun Detect Flag)

The ORIF flag is set to 1 when a receive overrun occurs. It is not set to 1 in overwrite mode.

In overwrite mode, a reception complete interrupt request occurs if an overwrite condition occurs and the ORIF bit is not set to 1.

In overrun mode with normal mailbox mode, if an overrun occurs in any of mailboxes 0 to 31, this flag is set to 1. In overrun mode with FIFO mailbox mode, if an overrun occurs in any of mailboxes 0 to 23 or the receive FIFO, this flag is set to 1.

OLIF flag (Overload Frame Transmission Detect Flag)

The OLIF flag is set to 1 if the transmitting condition of an overload frame is detected when the CAN module is transmitting or receiving.

BLIF flag (Bus Lock Detect Flag)

The BLIF flag is set to 1 if 32 consecutive dominant bits are detected on the CAN bus while the CAN module is in CAN operation mode.

After the flag is set to 1, 32 consecutive dominant bits are detected again in either of the following conditions:

- Recessive bits are detected after this flag changes to 0 from 1
- The CAN module enters CAN reset or halt mode and then enters CAN operation mode again after this flag changes to 0 from 1.

30.2.22 Receive Error Count Register (RECR)

Address(es): CAN0.RECR 4005 084Eh

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Description	R/W
b7 to b0	Receive error count function RECR increments or decrements the counter value based on the error status of the CAN module during reception.	R

The RECR register indicates the value of the receive error counter. See the CAN specification (ISO11898-1) for information about the increment and decrement conditions of the receive error counter.

The value of RECR in the bus-off state is undefined.

30.2.23 Transmit Error Count Register (TECR)

Address(es): CAN0.TECR 4005 084Fh

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Description	R/W
b7 to b0	Transmit error count function TECR increments or decrements the counter value based on the error status of the CAN module during transmission.	R

The TECR register indicates the value of the transmit error counter. See the CAN specification (ISO11898-1) for information about the increment and decrement conditions of the transmit error counter.

The value of TECR in the bus-off state is undefined.

30.2.24 Error Code Store Register (ECSR)

Address(es): CAN0.ECSR 4005 0850h

	b7	b6	b5	b4	b3	b2	b1	b0
	EDPM	ADEF	BE0F	BE1F	CEF	AEF	FEF	SEF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SEF	Stuff Error Flag*1,*2	0: No stuff error detected 1: Stuff error detected.	R/W
b1	FEF	Form Error Flag*1,*2	0: No form error detected 1: Form error detected.	R/W
b2	AEF	ACK Error Flag*1,*2	0: No ACK error detected 1: ACK error detected.	R/W
b3	CEF	CRC Error Flag*1,*2	0: No CRC error detected 1: CRC error detected.	R/W
b4	BE1F	Bit Error (recessive) Flag*1,*2	0: No bit error (recessive) detected 1: Bit error (recessive) detected.	R/W
b5	BE0F	Bit Error (dominant) Flag*1,*2	0: No bit error (dominant) detected 1: Bit error (dominant) detected.	R/W
b6	ADEF	ACK Delimiter Error Flag*1,*2	0: No ACK delimiter error detected 1: ACK delimiter error detected.	R/W
b7	EDPM	Error Display Mode Select*3,*4	0: Output first detected error code 1: Output accumulated error code.	R/W

Note 1. Writing 1 has no effect on these bit values.
Note 2. To write 0 to the SEF, FEF, AEF, CEF, BE1F, BE0F, and ADEF bits, use the transfer (MOV) instruction to ensure that only the specified bit is set to 0 and the other bits are set to 1.
Note 3. Write to the EDPM bit in CAN reset or halt mode.
Note 4. If more than one error condition is detected simultaneously, all related bits are set to 1.

The ECSR register indicates whether an error occurs on the CAN bus. See the CAN specification (ISO11898-1) for the conditions when each error occurs.

Clear all of the bits, except for EDPM, to 0 through a software write. If a bit is set to 1 at the same time that software

clears it, it becomes 1.

SEF flag (Stuff Error Flag)

The SEF flag is set to 1 when a stuff error is detected.

FEF flag (Form Error Flag)

The FEF flag is set to 1 when a form error is detected.

AEF flag (ACK Error Flag)

The AEF flag is set to 1 when an ACK error is detected.

CEF flag (CRC Error Flag)

The CEF flag is set to 1 when a CRC error is detected.

BE1F flag (Bit Error (recessive) Flag)

The BE1F flag is set to 1 when a recessive bit error is detected.

BE0F flag (Bit Error (dominant) Flag)

The BE0F flag is set to 1 when a dominant bit error is detected.

ADEF flag (ACK Delimiter Error Flag)

The ADEF flag is set to 1 when a form error is detected with the ACK delimiter during transmission.

EDPM bit (Error Display Mode Select)

The EDPM bit selects the output mode of ECSR. When the EDPM bit is set to 0, ECSR outputs the first error code. When the EDPM bit is set to 1, ECSR outputs the accumulated error code.

30.2.25 Time Stamp Register (TSR)

Address(es): CAN0.TSR 4005 0854h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	R/W
b15 to b0	Free-running counter value for the time stamp function	R

Note: Read TSR in 16-bit units.

When TSR is read, the value of the time stamp counter (16-bit free-running counter) at that moment is read. The time stamp counter reference clock is configured in the TSPS[1:0] bits in CTLR. The counter stops in CAN sleep and halt mode, and is initialized in CAN reset mode. Its value is stored to bits TSL[7:0] and TSH[7:0] in MBj_TS when a received message is stored in a receive mailbox.

30.2.26 Test Control Register (TCR)

Address(es): CAN0.TCR 4005 0858h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	TSTM[1:0]		TSTE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TSTE	CAN Test Mode Enable	0: Disable CAN test mode 1: Enable CAN test mode.	R/W
b2, b1	TSTM[1:0]	CAN Test Mode Select	b2 b1 0 0: Not CAN test mode 0 1: Listen-only mode 1 0: Self-test mode 0 (external loopback) 1 1: Self-test mode 1 (internal loopback).	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The TCR register controls the CAN test mode. Write to TCR in CAN halt mode only.

(1) Listen-only mode

The CAN specification (ISO11898-1) recommends an optional bus monitoring mode. In listen-only mode, valid data frames and valid remote frames can be received. However, only recessive bits can be sent on the CAN bus. The ACK bit, overload flag, and active error flag cannot be sent.

Listen-only mode can be used for baud rate detection. Do not request transmission from any mailboxes in listen-only mode.

Figure 30.6 shows the connection when listen-only mode is selected.

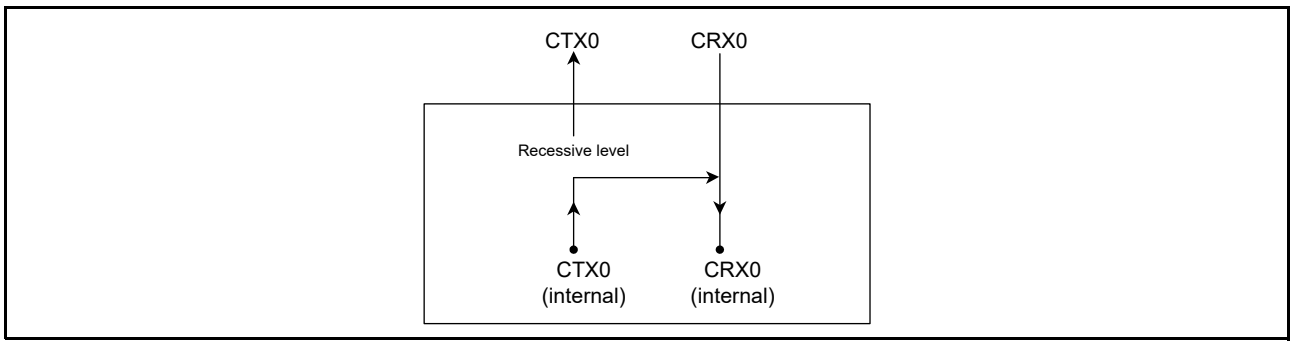


Figure 30.6 Connection when listen-only mode is selected

(2) Self-test mode 0 (external loopback)

Self-test mode 0 is provided for CAN transceiver tests. In this mode, the protocol module treats its own transmitted messages as those received by the CAN transceiver and stores them into the receive mailbox. To be independent from external stimulation, the protocol module generates the ACK bit.

Connect the CTX0 and CRX0 pins to the transceiver.

Figure 30.7 shows the connection when self-test mode 0 is selected.

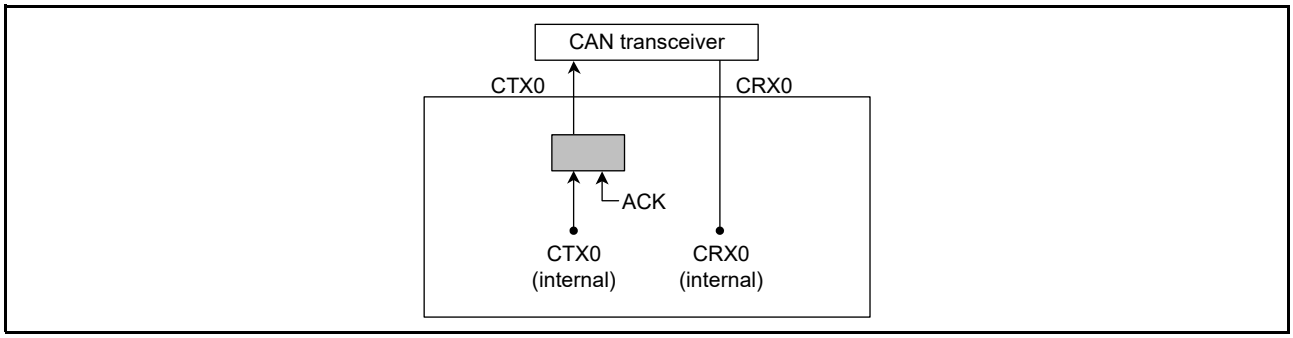


Figure 30.7 Connection when self-test mode 0 is selected

(3) Self-test mode 1 (internal loopback)

Self-test mode 1 is provided for self-test functions.

In self-test mode 1, the protocol controller treats its transmitted messages as received messages and stores them into the receive mailbox. To be independent from external stimulation, the protocol controller generates the ACK bit.

In self-test mode 1, the protocol controller performs internal loopback from the internal CTX0 pin to the internal CRX0 pin. The input value of the external CRX0 pin is ignored. The external CTX0 pin outputs only recessive bits. The CTX0 and CRX0 pins are not required to connect to the CAN bus or any external device.

Figure 30.8 shows the connection when self-test mode 1 is selected.

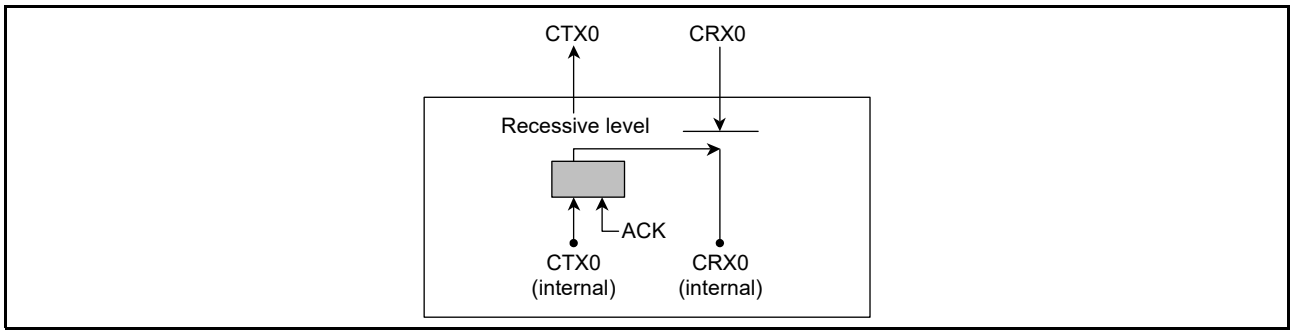


Figure 30.8 Connection when self-test mode 1 is selected

30.3 Operation Modes

The CAN module operation modes include:

- CAN reset mode
- CAN halt mode
- CAN operation mode
- CAN sleep mode.

Figure 30.9 shows the transitions between the operation modes.

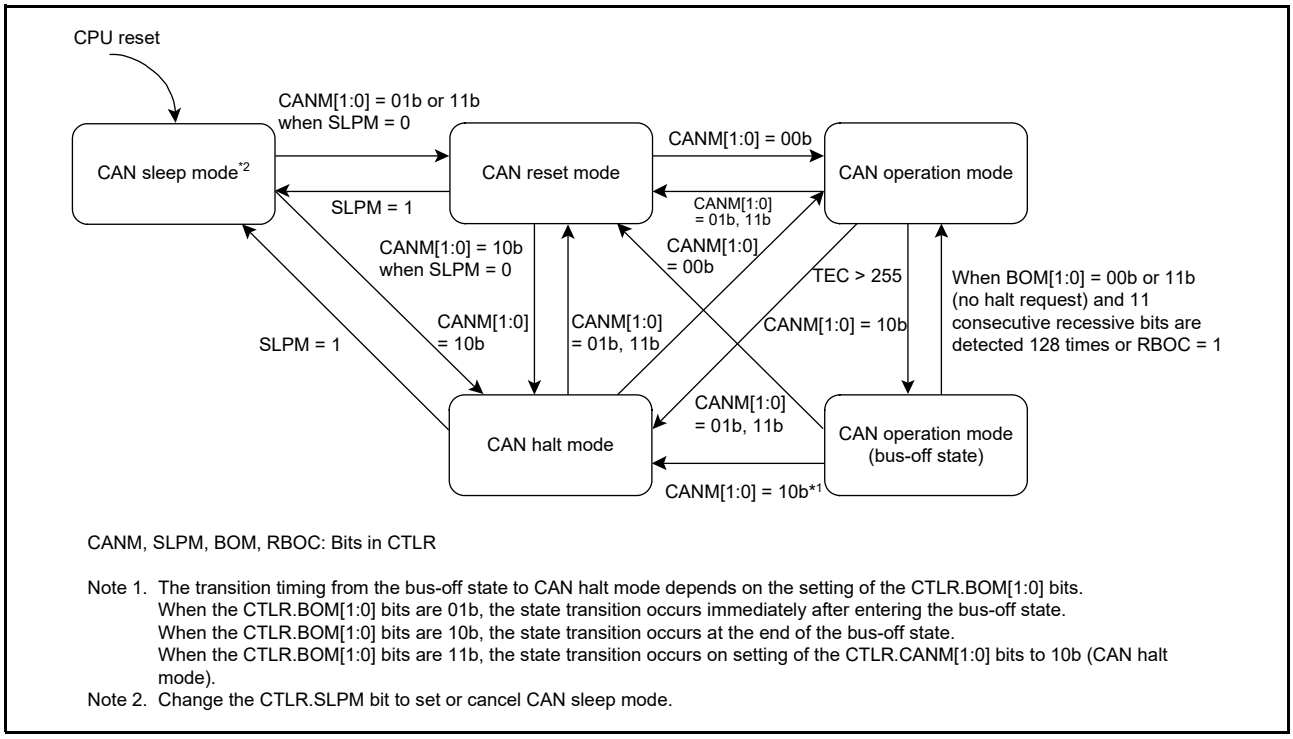


Figure 30.9 Transition between different modes of operation

30.3.1 CAN Reset Mode

CAN reset mode is provided for CAN communication configuration. When the CTLR.CANM[1:0] bits are set to 01b or 11b, the CAN module enters CAN reset mode. The STR.RSTST flag then is set to 1. Do not change the CTLR.CANM[1:0] bits until the RSTST flag is 1. Set BCR before exiting CAN reset mode to any other modes.

The following registers are initialized to their reset values after entering CAN reset mode, and their initial values are saved during CAN reset mode:

- MCTL_TXj and MCTL_RXj
- STR (except for the SLPST and TFST flags)
- EIFR
- RECR
- TECR
- TSR
- MSSR
- MSMR
- RFCR
- TFCR
- TCR
- ECSR (except for the EDPM bit).

The following registers retain their previous values even after entering CAN reset mode:

- CTLR
- STR (only the SLPST and TFST flags)
- MIER and MIER_FIFO

- EIER
- BCR
- CSSR
- ECSR (only the EDPM bit)
- MBj_ID, MBj_DL, MBj_Dm and MBj_TS
- MKRk
- FIDCR0 and FIDCR1
- MKIVLR
- AFSR
- RFPCR
- TFPCR.

30.3.2 CAN Halt Mode

CAN halt mode is used for mailbox configuration and test mode setting.

When the CTLR.CANM[1:0] bits are set to 10b, CAN halt mode is selected. The STR.HLTST bit is then set to 1. Do not change the CTLR.CANM[1:0] bits until the HLTST bit is 1.

See Table 30.8 for the state transition conditions when transmitting or receiving.

All registers except for the RSTST, HLTST, and SLPST flags in STR remain unchanged when the CAN enters CAN halt mode.

Do not change the CTLR register (except for the CANM[1:0] and SLPM bits) and EIER in CAN halt mode. The BCR register can be changed in CAN halt mode only when listen-only mode is selected for automatic baud rate detection.

Table 30.8 Operation in CAN reset mode and CAN halt mode

Operation mode	Receiver	Transmitter	Bus-off
CAN reset mode (forced transition) CA79	CAN module enters CAN reset mode without waiting for the end of message reception	CAN module enters CAN reset mode without waiting for the end of message transmission	CAN module enters CAN reset mode without waiting for the end of bus-off recovery
CAN reset mode CANM[1:0] = 01b	CAN module enters CAN reset mode without waiting for the end of message reception	CAN module enters CAN reset mode after waiting for the end of message transmission*1,*4	CAN module enters CAN reset mode without waiting for the end of bus-off recovery
CAN halt mode	CAN module enters CAN halt mode after waiting for the end of message reception*2,*3	CAN module enters CAN halt mode after waiting for the end of message transmission*1,*4	When the BOM[1:0] bits are 00b: A halt request from the software is accepted only after bus-off recovery. When the BOM[1:0] bits are 01b: CAN module automatically enters CAN halt mode without waiting for the end of bus-off recovery, regardless of a halt request from software. When the BOM[1:0] bits are 10b: CAN module automatically enters CAN halt mode after waiting for the end of bus-off recovery, regardless of a halt request from software. When the BOM[1:0] bits are 11b: CAN module enters CAN halt mode, without waiting for the end of bus-off recovery, if a halt is requested by software during bus-off.

BOM[1:0] bits: Bits in CTLR.

Note 1. If transmission of multiple messages is requested, a mode transition occurs after completion of the first transmission. If the CAN reset mode is being requested during suspend transmission, the mode transition occurs when the bus is idle, the next transmission ends, or the CAN module becomes a receiver.
Note 2. If the CAN bus is locked at the dominant level, the program can detect this state by monitoring the BLIF bit in EIFR.
Note 3. If a CAN bus error occurs during reception after CAN halt mode is requested, the CAN module transitions to CAN halt mode.
Note 4. If a CAN bus error or arbitration-lost occurs during transmission after CAN reset mode or CAN halt mode is requested, the CAN module transitions to the requested CAN mode.

30.3.3 CAN Sleep Mode

CAN sleep mode reduces power consumption by stopping the clock supply to the CAN module. After a reset from an MCU pin or a software reset, the CAN module starts from CAN sleep mode.

When the SLPM bit in CTLR is set to 1, the CAN module enters CAN sleep mode. The SLPST bit in STR is then set to 1. Do not change the value of the SLPM bit until the SLPST bit is 1. The other registers remain unchanged when the CAN module enters CAN sleep mode.

Write to the SLPM flag in CAN reset mode and CAN halt mode. Do not change any registers (except for the SLPM bit) during CAN sleep mode. Read operation is still allowed.

When the SLPM bit is set to 0, the CAN module is released from CAN sleep mode. When the CAN module exits CAN sleep mode, the other registers remain unchanged.

30.3.4 CAN Operation Mode (Excluding Bus-Off State)

CAN operation mode is used for CAN communication.

When the CANM[1:0] bits in CTLR are set to 00b, the CAN module enters CAN operation mode. The RSTST and HLTST flags in STR are then set to 0. Do not change the value of the CANM[1:0] bits until the RSTST and HLTST flags are 0.

If 11 consecutive recessive bits are detected after entering CAN operation mode, the following occur:

- The CAN module becomes an active node on the network, which enables transmission and reception of CAN messages
- Error monitoring of the CAN bus, such as receive and transmit error counters, is performed.

During CAN operation mode, the CAN module is in one of the following three sub-modes, depending on the status of the CAN bus:

- Idle mode: No transmission or reception occurs
- Receive mode: A CAN message sent by another node is being received
- Transmit mode: A CAN message is being transmitted. The CAN module receives a message transmitted by the local node simultaneously when self-test mode 0 (TSTM[1:0] bits in TCR = 10b) or self-test mode 1 (TSTM[1:0] bits = 11b) is selected.

Figure 30.10 shows the sub-modes in CAN operation mode.

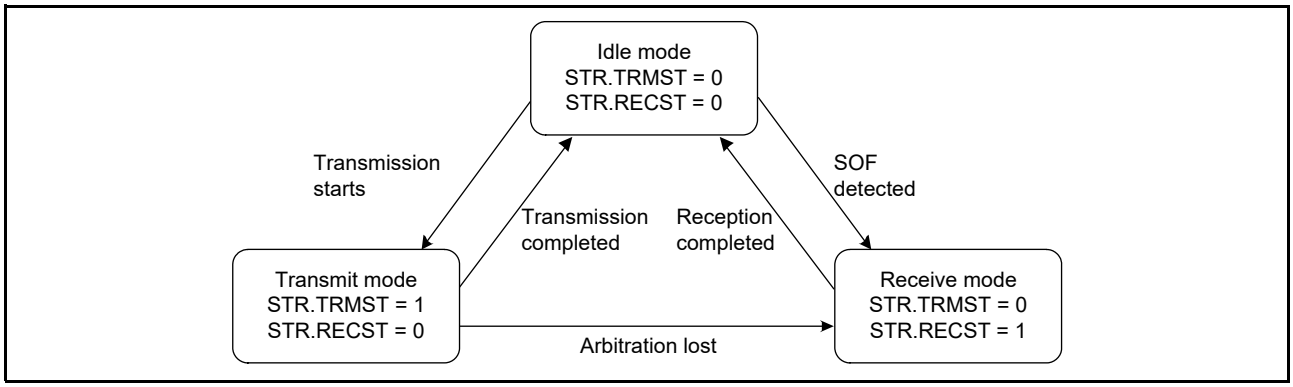


Figure 30.10 Sub-modes of CAN operation mode

30.3.5 CAN Operation Mode (Bus-Off State)

The CAN module enters the bus-off state based on the incrementing and decrementing rules for transmit and error counters defined in the CAN specification. The following cases apply when the CAN module is recovering from the bus-off state. When the CAN module is in the bus-off state, the values in the CAN-related registers remain unchanged, except for those in STR, EIFR, RECR, TECR, and TSR.

(1) When the CTLR.BOM[1:0] = 00b (normal mode)

The CAN module enters the error-active state after it completes recovery from the bus-off state and CAN communication is enabled. The BORIF flag in EIFR is set to 1 (bus-off recovery detected).

(2) When the CTLR.RBOC = 1 (forced return from bus-off)

The CAN module enters the error-active state when it is in the bus-off state and the RBOC bit is 1. CAN communication is enabled again after 11b consecutive recessive bits are detected. The BORIF flag is not set to 1.

(3) When the CTLR.BOM[1:0] = 01b (automatic transition to CAN halt mode on bus-off entry)

The CAN module enters CAN halt mode when it reaches the bus-off state. The BORIF flag is not set to 1.

(4) When CTLR.BOM[1:0] = 10b (automatic transition to CAN halt mode on bus-off end)

The CAN module enters CAN halt mode when it completes the recovery from bus-off. The BORIF flag is set to 1.

(5) When CTLR.BOM[1:0] = 11b (automatic transition to CAN halt mode through software) and the CTLR.CANM[1:0] = 10b (CAN halt mode) during bus-off state

The CAN module enters CAN halt mode when it is in the bus-off state and the CANM[1:0] bits are set to 10b (CAN halt mode). The BORIF flag is not set to 1.

If the CANM[1:0] bits are not set to 10b during bus-off, the same behavior as (1) applies.

30.4 Data Transfer Rate Configuration

This section describes how to configure the data transfer rate.

30.4.1 Clock Setting

The CAN module provides a CAN clock generator, as shown in Figure 30.11. Select the clock in the CCLKS and BRP[9:0] bits in BCR.

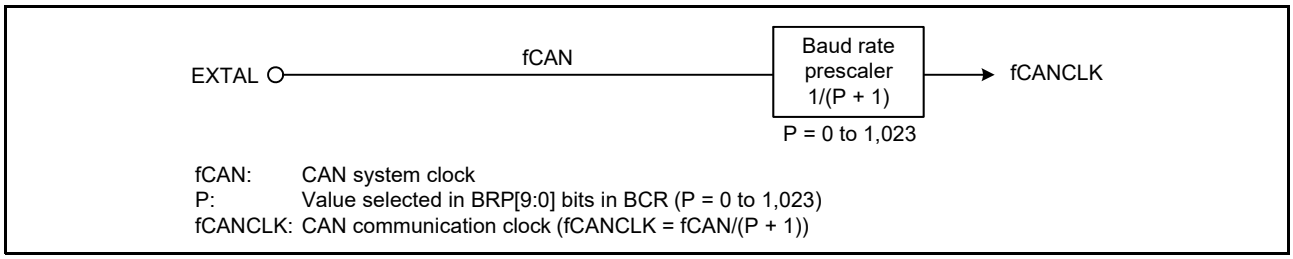


Figure 30.11 CAN clock generator block diagram

30.4.2 Bit Time Setting

The bit time consists of the three segments shown in Figure 30.12.

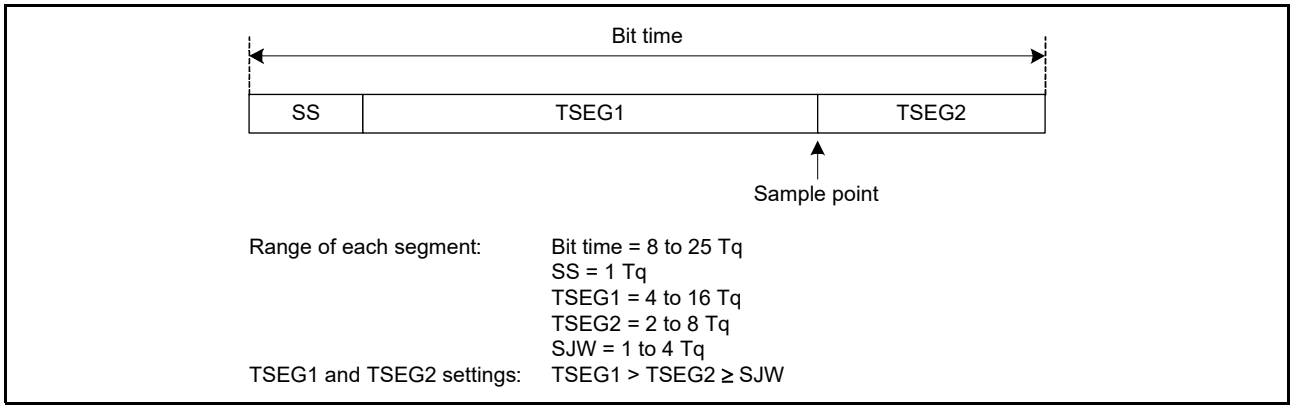


Figure 30.12 Bit timing

30.4.3 Data Transfer Rate

The data transfer rate depends on the division value of fCAN (CAN system clock), the division value of the baud rate prescaler, and the Tq count for 1 bit time.

$$\textbf{Data transfer rate [bps]} = \frac{\textbf{fCAN}}{\textbf{Baud rate prescaler division value}^{*1}\textbf{ x number of Tq of 1 bit time}} = \frac{\textbf{fCANCLK}}{\textbf{Number of Tq of 1 bit time}}$$

Note 1. Division value of baud rate prescaler = P + 1 (P: 0 to 1,023), where P is the BRP[9:0] setting in BCR.

Table 30.9 lists data transfer rate examples.

Table 30.9 Data transfer rate examples when fCAN = 20 MHz (1 of 2)

Data transfer rate	Tq Count	P + 1
1 Mbps	5 Tq 10 Tq	4 2
500 kbps	5 Tq 10 Tq	8 4
250 kbps	5 Tq 10 Tq	16 8
125 kbps	5 Tq 10 Tq	32 16
83.3 kbps	5 Tq 10 Tq	48 24

Table 30.9 Data transfer rate examples when fCAN = 20 MHz (2 of 2)

Data transfer rate	Tq Count	P + 1
33.3 kbps	5 Tq	120
	8 Tq	75
	10 Tq	60

30.5 Mailbox and Mask Register Structure

Figure 30.13 shows the structure of the 32 mailbox registers MBj_ID, MBj_DL, MBj_Dm, and MBj_TS.

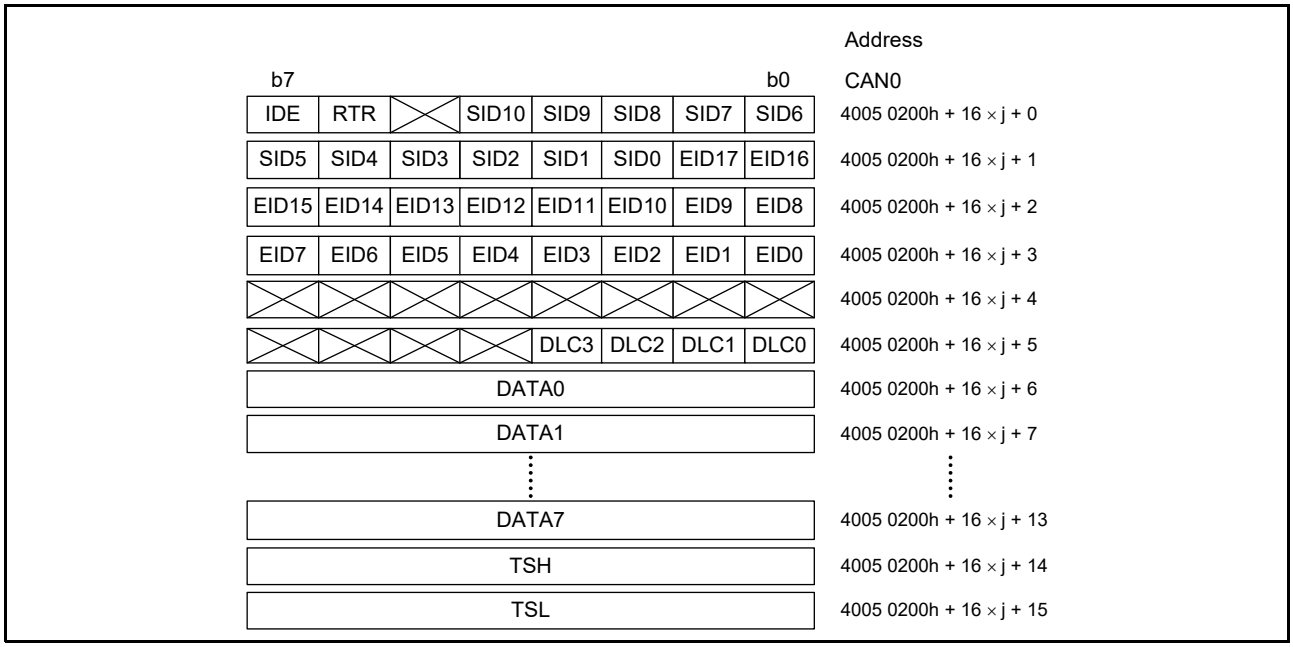


Figure 30.13 Structure of the mailbox registers (j = 0 to 31)

Figure 30.14 shows the structure of the eight mask registers MKRk.

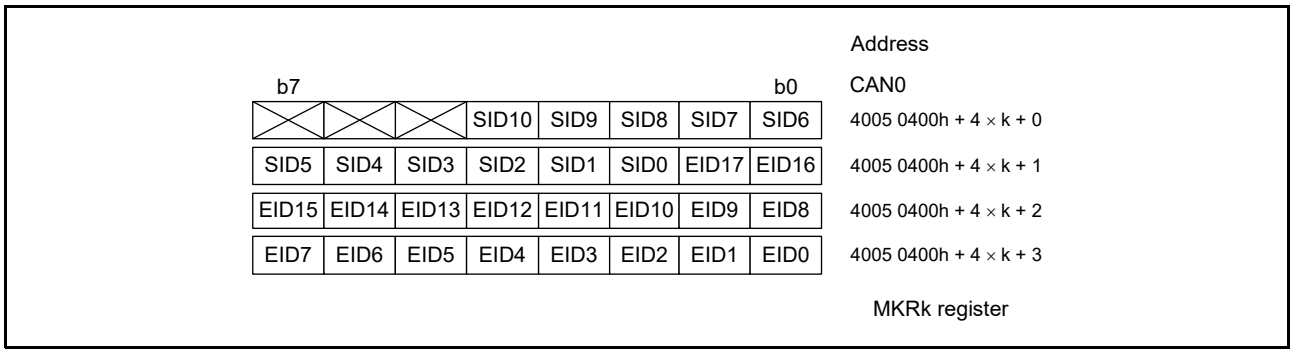


Figure 30.14 Structure of the MKRk registers (k = 0 to 7)

Figure 30.15 shows the structure of the two FIFO received ID compare registers, FIDCR0 and FIDCR1.

b7							b0	Address CAN0
IDE	RTR		SID10	SID9	SID8	SID7	SID6	4005 0420h + 4 × n + 0
SID5	SID4	SID3	SID2	SID1	SID0	EID17	EID16	4005 0420h + 4 × n + 1
EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8	4005 0420h + 4 × n + 2
EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0	4005 0420h + 4 × n + 3

FIDCRn register

Figure 30.15 Structure of the FIDCRn registers (n = 0, 1)

30.6 Acceptance Filtering and Masking Functions

The acceptance filtering and masking functions allow you to select and receive messages with multiple IDs for mailboxes within a specified range.

The MKRk registers can mask the standard ID and the extended ID for 29 bits, as follows:

- MKR0 controls mailboxes 0 to 3
- MKR1 controls mailboxes 4 to 7
- MKR2 controls mailboxes 8 to 11
- MKR3 controls mailboxes 12 to 15
- MKR4 controls mailboxes 16 to 19
- MKR5 controls mailboxes 20 to 23
- MKR6 controls mailboxes 24 to 27 in normal mailbox mode and the receive FIFO mailboxes 28 to 31 in FIFO mailbox mode
- MKR7 controls mailboxes 28 to 31 in normal mailbox mode and the receive FIFO mailboxes 28 to 31 in FIFO mailbox mode.

The MKIVLR register disables acceptance filtering independently for each mailbox.

The IDE bit in MBj_ID is valid when the IDFM[1:0] bits in CTLR are 10b (mixed ID mode).

The RTR bit in MBj_ID selects a data frame or a remote frame.

In FIFO mailbox mode, the normal mailboxes (0 to 23) use one associated register from MKR0 to MKR5 for acceptance filtering. The receive FIFO mailboxes (28 to 31) use two registers, MKR6 and MKR7, for acceptance filtering.

The receive FIFO also uses two registers, FIDCR0 and FIDCR1, for ID comparison. The EID[17:0], SID[10:0], RTR, and IDE bits in mailbox 28 to mailbox 31 for the receive FIFO are disabled. As acceptance filtering depends on the result of two logic OR operations, two ranges of IDs can be received into the receive FIFO.

MKIVLR is disabled for the receive FIFO.

If different standard ID and extended ID values are set in the IDE bits in FIDCR0 and FIDCR1, both ID formats are received.

If different data and remote frame values are set in the RTR bits in FIDCR0 and FIDCR1, both data and remote frames are received.

When a combination of two ranges of IDs is not necessary, set the same mask value and the same ID in both the FIFO ID and mask registers.

Figure 30.16 shows the associations between mask registers and mailboxes. Figure 30.17 shows the acceptance filtering.

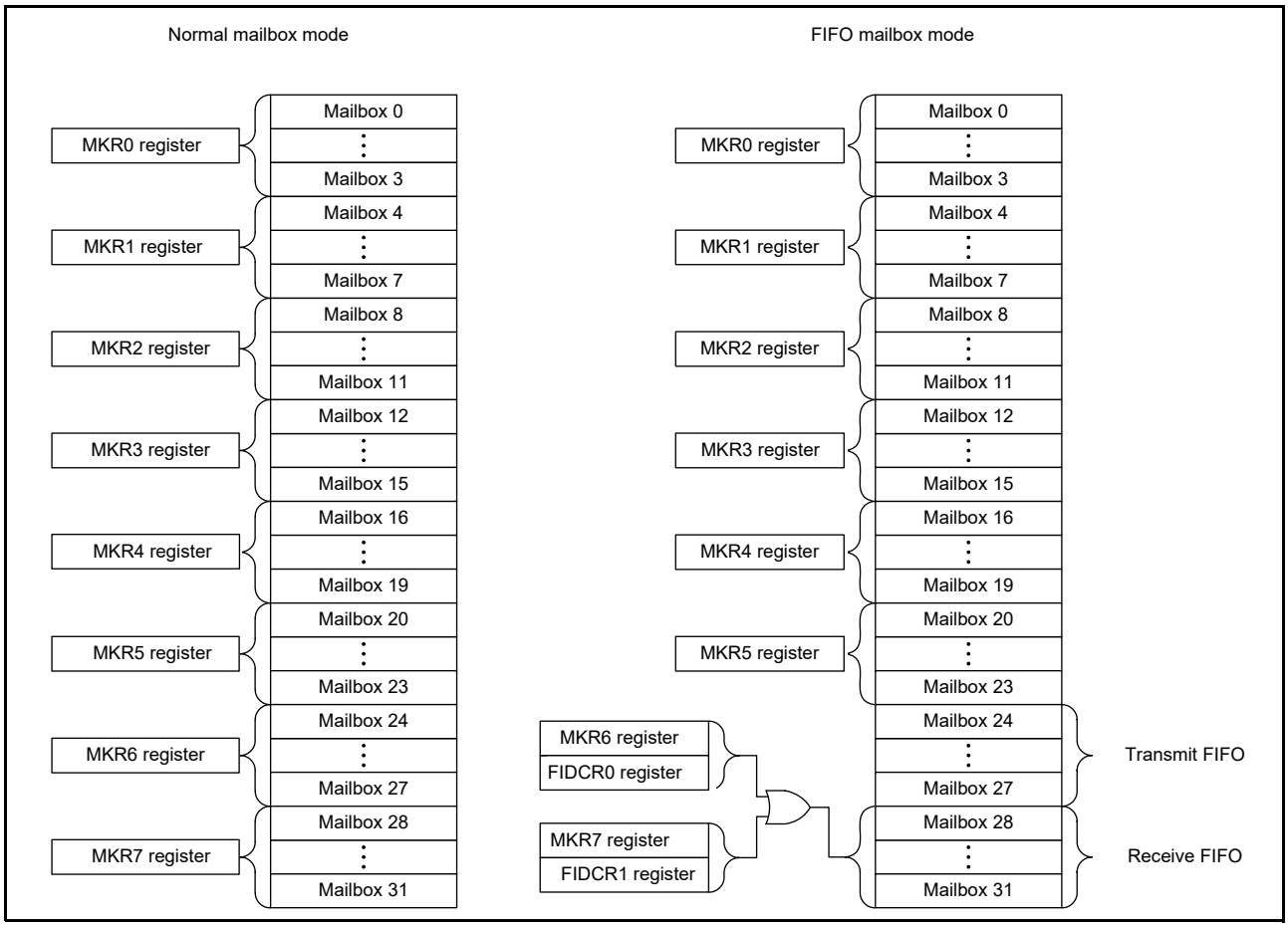
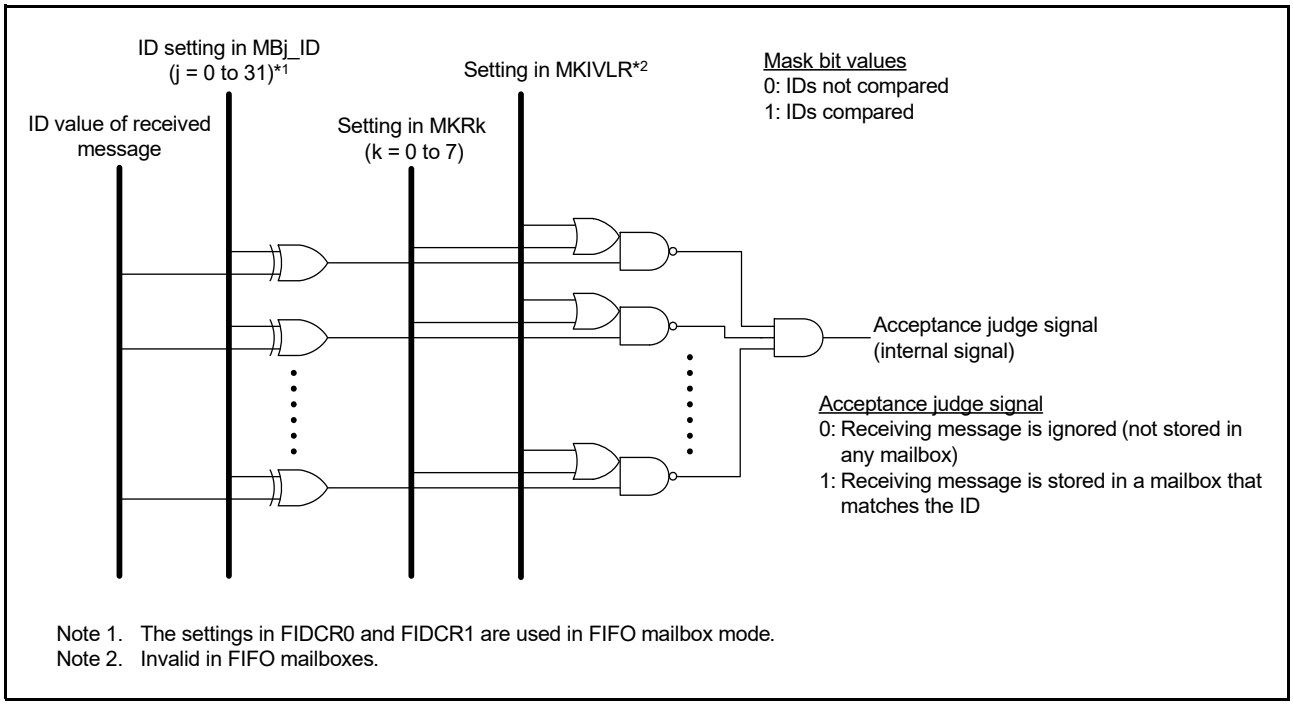


Figure 30.16 Associations between mask registers and mailboxes



Note 1. The settings in FIDCR0 and FIDCR1 are used in FIFO mailbox mode.
Note 2. Invalid in FIFO mailboxes.

Figure 30.17 Acceptance filtering

30.7 Reception and Transmission

Table 30.10 lists the CAN communication mode settings.

Table 30.10 Settings for CAN receive and transmit modes

MCTL_TXj and MCTL_RXj.TRMREQ	MCTL_TXj and MCTL_RXj.RECREQ	MCTL_TXj and MCTL_RXj.ONESHOT	Mailbox communication mode
0	0	0	Mailbox disabled or transmission aborted
0	0	1	Can be configured only when transmission or reception from a mailbox programmed in one-shot mode is aborted
0	1	0	Configured as a receive mailbox for a data frame or a remote frame
0	1	1	Configured as a one-shot receive mailbox for a data frame or a remote frame
1	0	0	Configured as a transmit mailbox for a data frame or a remote frame
1	0	1	Configured as a one-shot transmit mailbox for a data frame or a remote frame
1	1	0	Do not set
1	1	1	Do not set

j = 0 to 31

When a mailbox is configured as a receive mailbox or a one-shot receive mailbox:

- Before configuring the mailbox, set MCTL_RXj to 00h
- A received message is stored into the first mailbox that matches the conditions resulting from the receive mode settings and acceptance filtering. The matching mailbox with the smallest number takes priority for storing the received message.
- In CAN operation mode, the CAN module does not receive its own transmitted data even if the ID is a match. In self-test mode, however, the CAN module receives its own transmitted data and returns ACK.

When configuring a mailbox as a transmit mailbox or a one-shot transmit mailbox:

- Before configuring the mailbox, ensure that MCTL_TXj is 00h and that there is no pending abort process.

30.7.1 Reception

Figure 30.18 shows an operation example of data frame reception in overwrite mode. The example shows the overwriting of the first message when the CAN module receives two consecutive CAN messages that match the receiving conditions in MCTL_RXj (j = 0 to 31).

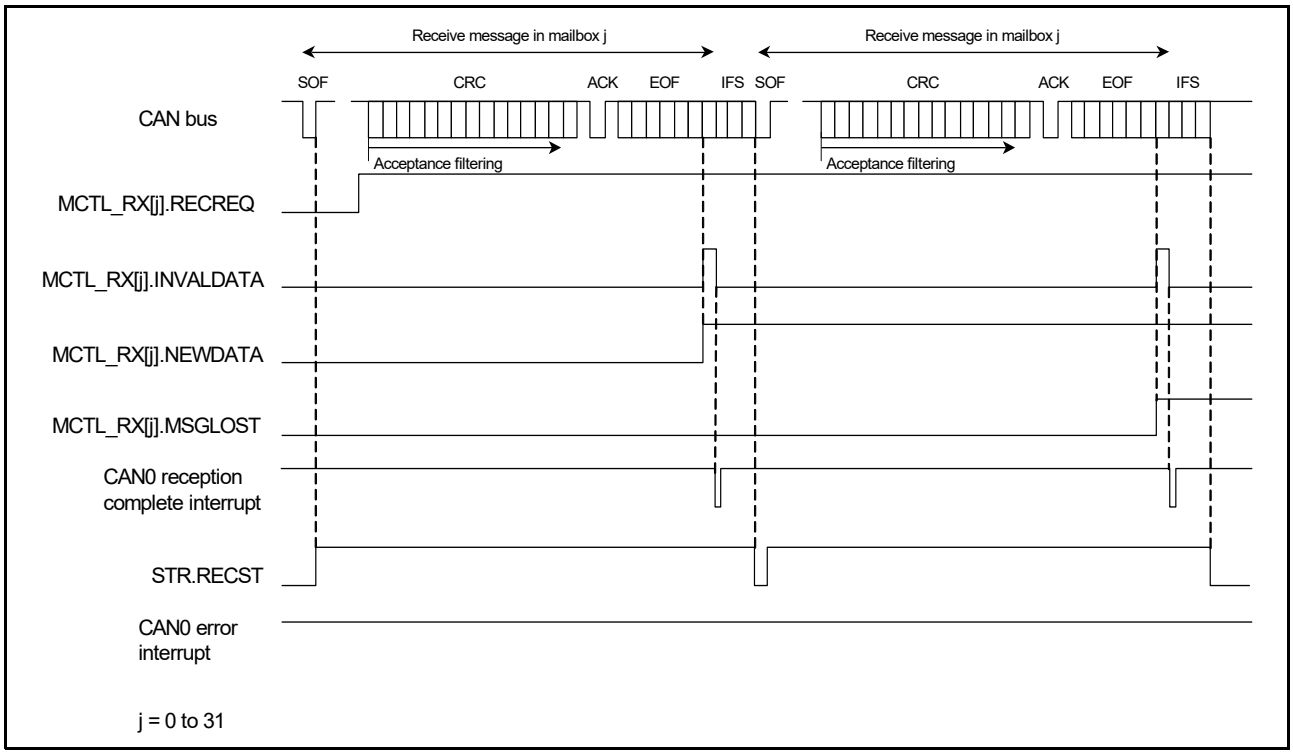


Figure 30.18 Operation example of data frame reception in overwrite mode

1. When an SOF is detected on the CAN bus, the RECST bit in STR is set to 1 (reception in progress) if the CAN module has no message ready to start transmission.
2. Acceptance filtering starts at the beginning of the CRC field to select the receive mailbox.
3. After a message is received, the NEWDATA flag in MCTL_RXj for the receive mailbox is set to 1 (new message is being stored or was stored to the mailbox). The INVALDATA flag in MCTL_RXj is set to 1 (message is updated) at the same time, and the INVALDATA flag is set to 0 (message valid) again after the complete message is transferred to the mailbox.
4. When the interrupt enable bit in MIER for the receive mailbox is 1 (interrupt enabled), the INVALDATA flag is set to 0, which triggers a CAN0 reception complete interrupt request.
5. After reading the message from the mailbox, the NEWDATA flag must be set to 0 by software.
6. In overwrite mode, if the next CAN message is received while the NEWDATA flag in MCTL_RXj is set to 1, the MSGLOST flag in MCTL_RXj is set to 1 (message was overwritten). The new received message is transferred to the mailbox. The CAN0 reception complete interrupt request occurs the same as in step 4.

Figure 30.19 shows an operation example of data frame reception in overrun mode. The example shows the overrunning of the second message when the CAN module receives two consecutive CAN messages that match the receiving conditions in MCTL_RXj (j = 0 to 31).

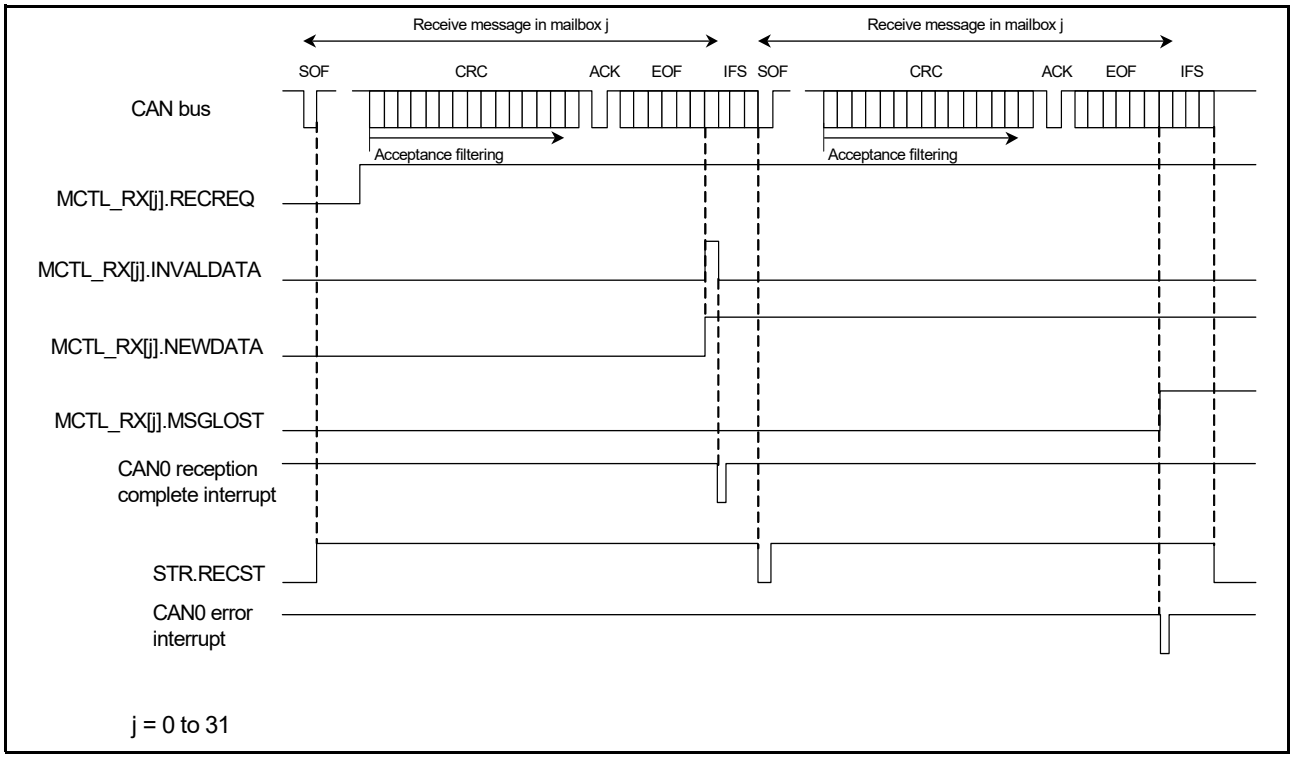


Figure 30.19 Operation example of data frame reception in overrun mode

Steps 1 to 5 are the same as in overwrite mode.

6. In overrun mode, if the next CAN message is received before the NEWDATA flag in MCTL_RXj is set to 0, the MSGLOST flag in MCTL_RXj is set to 1 (message overrun). The new received message is discarded and a CAN0 error interrupt request occurs if the associated interrupt enable bit in EIER is 1 (interrupt enabled).

30.7.2 Transmission

Figure 30.20 shows an operation example of data frame transmission.

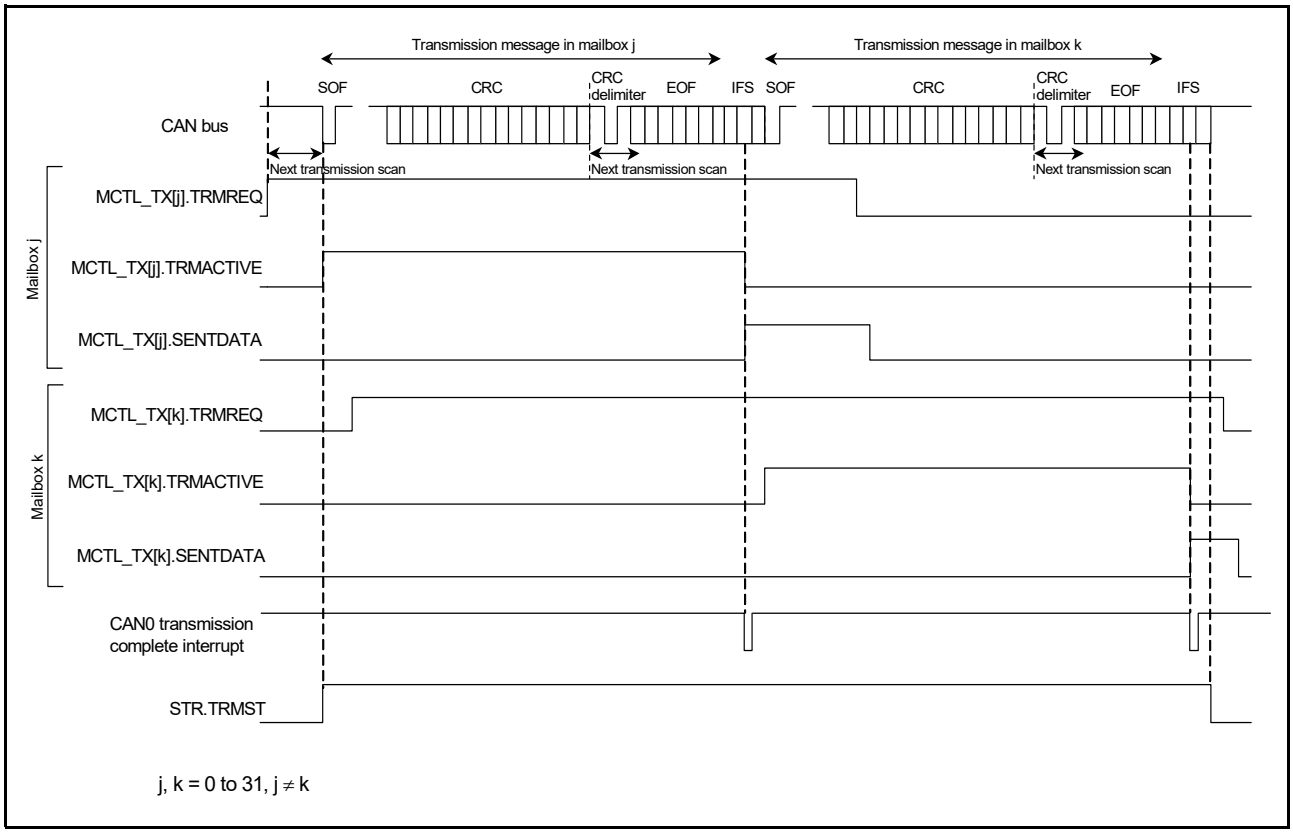


Figure 30.20 Operation example of data frame transmission

1. When a TRMREQ bit in MCTL_TXj (j = 0 to 31) is set to 1 (transmit mailbox) in the bus-idle state, mailbox scanning determines the highest-priority mailbox for transmission. When the transmit mailbox is determined, the TRMACTIVE flag in MCTL_TXj is set to 1 (from acceptance of transmission request to completion of transmission, or until error or arbitration-lost), the TRMST flag in STR is set to 1 (transmission in progress), and the CAN module starts transmission.*1
2. If other TRMREQ bits are set, the transmission scanning starts with the CRC delimiter for the next transmission.
3. If transmission is complete without losing arbitration, the SENTDATA flag in MCTL_TXj is set to 1 (transmission completes) and the TRMACTIVE flag is set to 0 (transmission is pending or transmission is not requested). If the interrupt enable bit in MIER is 1 (interrupt enabled), the CAN0 transmission complete interrupt request is generated.
4. When requesting the next transmission from the same mailbox, set the SENTDATA flag and the TRMREQ bit to 0, then set the TRMREQ bit to 1 after checking that the SENTDATA flag and the TRMREQ bit are set to 0.

Note 1. If arbitration is lost after the CAN module starts transmission, the TRMACTIVE flag is set to 0. Transmission scanning is performed again to search for the highest-priority transmit mailbox from the beginning of the CRC delimiter. If an error occurs either during transmission or following arbitration-lost, transmission scanning is performed again to search for the highest-priority transmit mailbox from the start of the error delimiter.

30.8 Interrupt

The CAN module provides the following interrupts for each channel. Table 30.11 lists CAN interrupts.

- CAN0 reception complete interrupt for mailboxes 0 to 31 (CAN0_RXM)
- CAN0 transmission complete interrupt for mailboxes 0 to 31 (CAN0_TXM)
- CAN0 receive FIFO interrupt (CAN0_RXF)
- CAN0 transmit FIFO interrupt (CAN0_TXF)
- CAN0 error interrupt (CAN0_ERS).

Eight interrupt sources are available for CAN0 error interrupts. Check the EIFR register to determine whether these sources are triggered:

- Bus error
- Error-warning
- Error-passive
- Bus-off entry
- Bus-off recovery
- Receive overrun
- Overload frame transmission
- Bus lock.

Table 30.11 CAN interrupts

Module	Interrupt name	Interrupt source	Source flag
CAN0	CAN0_ERS	Bus lock detected	EIFR.BLIF
		Overload frame transmission detected	EIFR.OLIF
		Overrun detected	EIFR.ORIF
		Bus-off recovery detected	EIFR.BORIF
		Bus-off entry detected	EIFR.BOEIF
		Error-passive detected	EIFR.EPIF
		Error-warning detected	EIFR.EWIF
		Bus error detected	EIFR.BEIF
	CAN0_RXF	Receive FIFO message received (MIER_FIFO.MB29 = 0)	RFCR.RFUST[2:0]
		Receive FIFO warning (MIER_FIFO.MB29 = 1)	
	CAN0_TXF	Transmit FIFO message transmission complete (MIER_FIFO.MB25 = 0)	TFCR.TFUST[2:0]
		FIFO last message transmission complete (MIER_FIFO.MB25 = 1)	
	CAN0_RXM	Mailbox 0 to 31 message received	MCTL_RX[0].NEWDATA to MCTL_RX[31].NEWDATA
	CAN0_TXM	Mailbox 0 to 31 message transmission complete	MCTL_TX[0].SENTDATA to MCTL_TX[31].SENTDATA

30.9 Usage Notes

30.9.1 Settings for the Module-Stop State

The Module Stop Control Register B (MSTPCRB) can enable or disable CAN operation. The CAN module is stopped after a reset. The registers become accessible on release from the module-stop state. For details, see section 10, Low Power Modes.

30.9.2 Settings for the Operating Clock

The following clock constraints must be satisfied for the CAN module:

- fPCLKB ≥ fCANMCLK
- The clock frequency ratio of ICLK and PCLKB must be 2:1 when using the CAN module. Operation is not guaranteed for other settings.

31. Serial Peripheral Interface (SPI)

31.1 Overview

The MCU includes two independent channels of the Serial Peripheral Interface (SPI). The SPI channels are capable of high-speed, full-duplex synchronous serial communications with multiple processors and peripheral devices.

Table 31.1 lists the SPI specifications, Figure 31.1 shows a block diagram, and Table 31.2 lists the I/O pins.

In this section, *n* indicates A or B, and *i* indicates 0 or 1. A lower-case letter *i* in pin and signal names indicates a value from 0 to 3.

Table 31.1 SPI specifications (1 of 2)

Parameter	Description
Number of channels	Two channels
SPI transfer functions	• MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (SPI clock) signals enable serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method) • Transmit-only operation available • Communication mode selectable to full-duplex or transmit-only • Switching of RSPCK polarity • Switching of RSPCK phase.
Data format	• MSB-first or LSB-first selectable • Transfer bit length selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits • 32-bit transmit and receive buffers.
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLKB, programmable from divide-by-2 to divide-by-4,096 • In slave mode, the minimum PCLKB clock divided by 6 can be input as RSPCK (maximum RSPCK frequency is PCLKB divided by 6). Width at high level: 3 PCLKB cycles; width at low level: 3 PCLKB cycles
Buffer configuration	• Double buffer configuration for the transmit/receive buffers • 32 bits for the transmit and receive buffers.
Error detection	• Mode fault error detection • Underrun error detection • Overrun error detection*1 • Parity error detection.
SSL control function	• Four SSL pins (SSLn0 to SSLn3) for each channel • In single-master mode, SSLn0 to SSLn3 pins for output • In multi-master mode, SSLn0 pin for output, and SSLn1 to SSLn3 pins either for output or unused • In slave mode: SSLn0 pin for input, and SSLn1 to SSLn3 pins unused • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity.
Control in master transfer	• Support for the following commands: SSL signal value, bit rate, RSPCK polarity and phase, transfer data length, MSB- or LSB-first, RSPCK delay, SSL negation delay, and next-access delay • Transfers initiated by writing to the transmit buffer • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function.
Interrupt sources	• Receive buffer full interrupt • Transmit buffer empty interrupt • SPI error interrupt (mode fault, overrun, parity error) • SPI idle interrupt (SPI idle) • Transmission-complete interrupt.

Table 31.1 SPI specifications (2 of 2)

Parameter	Description
Event link function (output)	The following events can be output to the event link controller: • Receive buffer full signal • Transmit buffer empty signal • Mode fault, underrun, overrun, or parity error signal • SPI idle signal • Transmission-complete signal.
Other	• Function for initializing the SPI • Loopback mode.
Module-stop function	Module-stop state can be set.

Note 1. In master reception and when the RSPCK auto-stop function is enabled, an overrun error does not occur, because the transfer clock is stopped on overrun error detection.

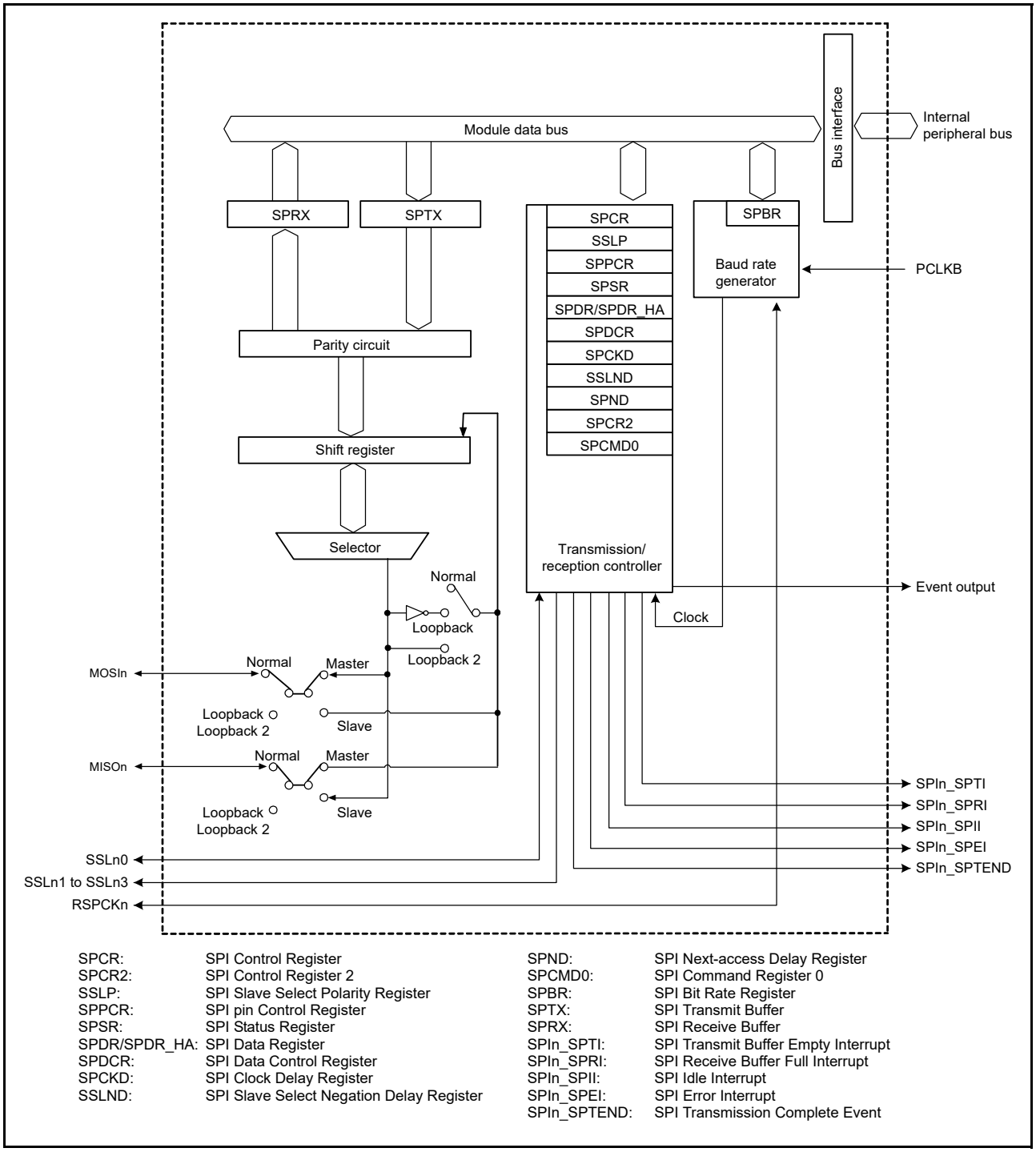


Figure 31.1 SPI block diagram

The SPI automatically switches the I/O direction of the SSLn0 pin. SSLn0 is an output when the SPI is a single master and an input when the SPI is a multi-master or a slave. The RSPCKn, MOSIn, and MISOn pins are automatically set as inputs or outputs based on the master or slave setting and the level input on the SSLn0 pin.

See section 31.3.2, Controlling the SPI Pins for details.

Table 31.2 SPI pin configuration

Channel	Pin name	I/O	Function
SPI0	RSPCKA	I/O	Clock I/O
	MOSIA	I/O	Master transmit data I/O
	MISOA	I/O	Slave transmit data I/O
	SSLA0	I/O	Slave selection I/O
	SSLA1	Output	Slave selection output
	SSLA2	Output	Slave selection output
	SSLA3	Output	Slave selection output
SPI1	RSPCKB	I/O	Clock I/O
	MOSIB	I/O	Master transmit data I/O
	MISOB	I/O	Slave transmit data I/O
	SSLB0	I/O	Slave selection I/O
	SSLB1	Output	Slave selection output
	SSLB2	Output	Slave selection output
	SSLB3	Output	Slave selection output

31.2 Register Descriptions

31.2.1 SPI Control Register (SPCR)

Address(es): SPI0.SPCR 4007 2000h, SPI1.SPCR 4007 2100h

	b7	b6	b5	b4	b3	b2	b1	b0
	SPRIE	SPE	SPTIE	SPEIE	MSTR	MODFEN	TXMD	SPMS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SPMS	SPI Mode Select	0: Select SPI operation (4-wire method) 1: Select clock synchronous operation (3-wire method).	R/W
b1	TXMD	Communications Operating Mode Select	0: Select full-duplex synchronous serial communications 1: Select serial communications with transmit only.	R/W
b2	MODFEN	Mode Fault Error Detection Enable	0: Disable detection of mode fault errors 1: Enable detection of mode fault errors.	R/W
b3	MSTR	SPI Master/Slave Mode Select	0: Select slave mode 1: Select master mode.	R/W
b4	SPEIE	SPI Error Interrupt Enable	0: Disable SPI error interrupt requests 1: Enable SPI error interrupt requests.	R/W
b5	SPTIE	Transmit Buffer Empty Interrupt Enable	0: Disable transmit buffer empty interrupt requests 1: Enable transmit buffer empty interrupt requests.	R/W
b6	SPE	SPI Function Enable	0: Disable SPI function 1: Enable SPI function.	R/W
b7	SPRIE	SPI Receive Buffer Full Interrupt Enable	0: Disable SPI receive buffer full interrupt requests 1: Enable SPI receive buffer full interrupt requests.	R/W

If the SPCR.MSTR, SPCR.MODFEN, or SPCR.TXMD bit is changed while the SPCR.SPE bit is 1, do not perform subsequent operations.

SPMS bit (SPI Mode Select)

The SPMS bit selects SPI operation (4-wire method) or clock synchronous operation (3-wire method).

The SSLn0 to SSLn3 pins are not used in clock synchronous operation. The RSPCKn, MOSIn, and MISOn pins handle communications. For clock synchronous operation in master mode (SPCR.MSTR = 1), the SPCMD0.CPHA bit can be set to either 0 or 1. For clock synchronous operation in slave mode (SPCR.MSTR = 0), set the CPHA bit to 1. Do not perform operations if the CPHA bit is set to 0 for clock synchronous operation in slave mode (SPCR.MSTR = 0).

TXMD bit (Communications Operating Mode Select)

The TXMD bit selects full-duplex synchronous serial communications or transmit-only operations.

When this bit is set to 1, the SPI only performs transmit operations and not receive operations (see section 31.3.6, Data Transfer Modes), and receive buffer full interrupt requests cannot be used.

MODFEN bit (Mode Fault Error Detection Enable)

The MODFEN bit enables or disables the detection of mode fault errors (see section 31.3.8, Error Detection). In addition, the SPI determines the I/O direction of the SSLn0 to SSLn3 pins based on combinations of the MODFEN and MSTR bit settings (see section 31.3.2, Controlling the SPI Pins).

MSTR bit (SPI Master/Slave Mode Select)

The MSTR bit selects master or slave mode for the SPI. Based on the MSTR bit settings, the SPI determines the direction of the RSPCKn, MOSIn, MISOn, and SSLn0 to SSLn3 pins.

SPEIE bit (SPI Error Interrupt Enable)

The SPEIE bit enables or disables the generation of SPI error interrupt requests when:

- The SPI detects a mode fault error or underrun error and sets the SPSR.MODF flag to 1
- The SPI detects an overrun error and sets the SPSR.OVRF flag to 1
- The SPI detects a parity error and sets the SPSR.PERF flag to 1.

See section 31.3.8, Error Detection.

SPTIE bit (Transmit Buffer Empty Interrupt Enable)

The SPTIE bit enables or disables the generation of transmit buffer empty interrupt requests when the SPI detects that the transmit buffer is empty.

A transmit buffer empty interrupt request on transmission start is generated by setting the SPE and SPTIE bits to 1 at the same time or by setting the SPE bit to 1 after setting the SPTIE bit to 1. The interrupt occurs when the SPTIE bit is 1, even if the SPI function is disabled (the SPE bit is changed to 0).

SPE bit (SPI Function Enable)

The SPE bit enables or disables the SPI function.

The SPE bit cannot be set to 1 when the SPSR.MODF flag is 1. For details, see section 31.3.8, Error Detection.

Setting the SPE bit to 0 disables the SPI function and initializes a part of the module function. For details, see section 31.3.9, Initializing SPI. In addition, a state change on the SPE bit, from 0 to 1 or 1 to 0, triggers a transmit buffer empty interrupt request.

SPRIE bit (SPI Receive Buffer Full Interrupt Enable)

The SPRIE bit enables or disables the generation of an interrupt request if the SPI detects a receive buffer full write after completing a serial transfer.

31.2.2 SPI Slave Select Polarity Register (SSLP)

Address(es): SPI0.SSLP 4007 2001h, SPI1.SSLP 4007 2101h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	SSL3P	SSL2P	SSL1P	SSL0P
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SSL0P	SSL0 Signal Polarity Setting	0: Set SSL0 signal to active-low 1: Set SSL0 signal to active-high.	R/W
b1	SSL1P	SSL1 Signal Polarity Setting	0: Set SSL1 signal to active-low 1: Set SSL1 signal to active-high.	R/W
b2	SSL2P	SSL2 Signal Polarity Setting	0: Set SSL2 signal to active-low 1: Set SSL2 signal to active-high.	R/W
b3	SSL3P	SSL3 Signal Polarity Setting	0: Set SSL3 signal to active-low 1: Set SSL3 signal to active-high.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

If the contents of SSLP are changed while the SPCR.SPE bit is 1, do not perform subsequent operations.

31.2.3 SPI Pin Control Register (SPPCR)

Address(es): SPI0.SPPCR 4007 2002h, SPI1.SPPCR 4007 2102h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	MOIFE	MOIFV	—	—	SPLP2	SPLP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SPLP	SPI Loopback	0: Normal mode 1: Loopback mode, with data inverted for transmission.	R/W
b1	SPLP2	SPI Loopback 2	0: Normal mode 1: Loopback mode, with data not inverted for transmission.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	MOIFV	MOSI Idle Fixed Value	0: The level output on the MOSIn pin during MOSI idling is defined as low 1: The level output on the MOSIn pin during MOSI idling is defined as high	R/W
b5	MOIFE	MOSI Idle Value Fixing Enable	0: MOSI output value equals final data from previous transfer 1: MOSI output value equals the value set in the MOIFV bit	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

If the contents of SPPCR are changed while the SPCR.SPE bit is 1, do not perform subsequent operations.

SPLP bit (SPI Loopback)

The SPLP bit selects the mode of the SPI pins. When the SPLP bit is set to 1, the SPI shuts off the path between the MISOn pin and the shift register if the SPCR.MSTR bit is 1, and between the MOSIn pin and the shift register if the SPCR.MSTR bit is 0. The SPI then connects and inverts the input path and output path for the shift register, establishing loopback mode.

SPLP2 bit (SPI Loopback 2)

The SPLP2 bit selects the mode of the SPI pins. When the SPLP2 bit is set to 1, the SPI shuts off the path between the

MISOn pin and the shift register if the SPCR.MSTR bit is 1, and between the MOSIn pin and the shift register if the SPCR.MSTR bit is 0. The SPI then connects the input path and output path for the shift register, establishing loopback mode 2.

MOIFV bit (MOSI Idle Fixed Value)

If the MOIFE bit is 1 in master mode, the MOIFV bit determines the MOSIn pin output value during the SSL negation period.

MOIFE bit (MOSI Idle Value Fixing Enable)

The MOIFE bit fixes the MOSIn output value when the SPI is in master mode and in an SSL negation period. When the MOIFE bit is 0, the SPI outputs to the MOSIn pin the last data from the previous serial transfer during the SSL negation period. When the MOIFE bit is 1, the SPI outputs the fixed value set in the MOIFV bit to the MOSIn pin.

31.2.4 SPI Status Register (SPSR)

Address(es): SPI0.SPSR 4007 2003h, SPI1.SPSR 4007 2103h

	b7	b6	b5	b4	b3	b2	b1	b0
	SPRF	—	SPTEF	UDRF	PERF	MODF	IDLNF	OVRF
Value after reset:	0	0	1	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	OVRF	Overrun Error Flag	0: No overrun error occurred 1: Overrun error occurred.	R/(W)*1
b1	IDLNF	SPI Idle Flag	0: SPI is in the idle state 1: SPI is in the transfer state	R
b2	MODF	Mode Fault Error Flag	0: No mode fault error or underrun error occurred 1: A mode fault error or underrun error occurred.	R/(W)*1
b3	PERF	Parity Error Flag	0: No parity error occurred 1: A parity error occurred.	R/(W)*1
b4	UDRF	Underrun Error Flag	0: A mode fault error occurred (MODF = 1) 1: An underrun error occurred (MODF = 1). This bit is invalid when MODF is 0.	R/W*1,*2
b5	SPTEF	SPI Transmit Buffer Empty Flag	0: Data found in the transmit buffer 1: No data in the transmit buffer.	R/(W)*3
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	SPRF	SPI Receive Buffer Full Flag	0: No valid data in SPDR/SPDR_HA 1: Valid data found in SPDR/SPDR_HA.	R/(W)*3

Note 1. Only 0 can be written to clear the flag after reading 1.
Note 2. Clear the UDRF flag at the same time that you clear the MODF flag.
Note 3. The write value should be 1.

OVRF flag (Overrun Error Flag)

The OVRF flag indicates the occurrence of an overrun error. In master mode (SPCR.MSTR = 1) and when the RSPCK clock auto-stop function is enabled (SPCR2.SCKASE = 1), overrun errors do not occur, and this flag does not set to 1. For details, see section 31.3.8.1, Overrun errors.

[Setting condition]

- When the next serial transfer ends while the SPCR.TXMD bit is 0 and the receive buffer is full.

[Clearing condition]

- When SPSR is read while this flag is 1, and then 0 is written to this flag.

IDLNF flag (SPI Idle Flag)

The IDLNF flag indicates the transfer status of the SPI.

[Setting condition]

Master mode:

- When conditions 1. and 2. in the master mode [Clearing condition] are not satisfied.

Slave mode:

- When the SPCR.SPE bit is 1, enabling the SPI function.

[Clearing condition]

Master mode:

- When condition 1. or conditions 2. and 3. are satisfied.

1. The SPCR.SPE bit is 0 for SPI initialization.
2. The transmit buffer (SPTX) is empty, meaning data for the next transfer is not set.
3. The SPI internal sequencer is in the idle state, indicating that operations up to the next-access delay are complete.

Slave mode:

- When condition 1. is satisfied.

MODF flag (Mode Fault Error Flag)

The MODF flag indicates the occurrence of a mode fault error or an underrun error. Use the UDRF to identify which errors occurred.

[Setting condition]

Multi-master mode:

- When the input level of the SSLni pin changes to the active level while the SPCR.MSTR bit is 1 (master mode) and the SPCR.MODFEN bit is 1 (mode fault error detection enabled), the SPI detects a mode fault error.

Slave mode:

- When condition 1. or 2. is satisfied.

1. The SSLni pin is negated before the RSPCK cycle necessary for data transfer ends while the SPCR.MSTR bit is 0 (slave mode) and the SPCR.MODFEN bit is 1 (mode fault error detection enabled), triggering a mode fault error.
2. The serial transfer begins with the SPCR.MSTR bit set to 0 (slave mode), the SPCR.SPE bit set to 1, and the transmission data is not prepared, triggering an underrun error.

The active level of the SSLni signal is determined by the SSLP.SSLiP bit (SSLi signal polarity setting).

[Clearing condition]

- When SPSR is read while this flag is 1, and then 0 is written to this flag.

PERF flag (Parity Error Flag)

The PERF flag indicates the occurrence of a parity error.

[Setting condition]

- When a serial transfer ends while the SPCR.TXMD bit is 0 and the SPCR2.SPPE bit is 1, triggering a parity error.

[Clearing condition]

- When SPSR is read while this flag is 1, and then 0 is written to this flag.

UDRF flag (Underrun Error Flag)

The UDRF flag indicates the occurrence of an underrun error.

[Setting condition]

- When the serial transfer begins with the SPCR.MSTR bit set to 0 (slave mode), SPCR.SPE bit set to 1, and the transmission data is not prepared, triggering an underrun error.

[Clearing condition]

- When SPSR is read while this flag is 1, and then 0 is written to this flag.

SPTEF flag (SPI Transmit Buffer Empty Flag)

The SPTEF flag indicates the status of the transmit buffer for the SPI Data Register (SPDR/SPDR_HA).

[Setting condition]

- When condition 1. or 2. is satisfied.

1. The SPCR.SPE bit is 0 for SPI initialization.
2. Transmit data is transferred from the transmit buffer to the shift register.

[Clearing condition]

- When data is written to SPDR/SPDR_HA.

Data can only be written to SPDR/SPDR_HA when the SPTEF bit is 1. If data is written to the transmit buffer of SPDR/SPDR_HA when the SPTEF bit is 0, the data in the transmit buffer is not updated.

SPRF flag (SPI Receive Buffer Full Flag)

The SPRF flag indicates the status of the receive buffer for the SPI Data Register (SPDR/SPDR_HA).

[Setting condition]

- When a serial transfer ends while the communication operating mode select bit (TXMD) in the SPI Control Register (SPCR) is 0 and the SPRF bit is 0, and the SPI transfers the receive data from the shift register to SPDR/SPDR_HA. However, when the OVRF flag is 1, SPRF does not change from 0 into 1.

[Clearing condition]

- When received data is read from SPDR/SPDR_HA.

31.2.5 SPI Data Register (SPDR/SPDR_HA)

Address(es): SPI0.SPDR 4007 2004h, SPI1.SPDR 4007 2104h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address(es): SPI0.SPDR_HA 4007 2004h, SPI1.SPDR_HA 4007 2104h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SPDR/SPDR_HA is the interface with the buffers that hold data for transmission and reception by the SPI. When accessing this register in words (SPLW = 1), access SPDR. When accessing it in halfwords (SPLW = 0), access SPDR_HA.

The transmit buffer (SPTX) and receive buffer (SPRX) are independent but are both mapped to SPDR/SPDR_HA.

Figure 31.2 shows the configuration of SPDR/SPDR_HA.

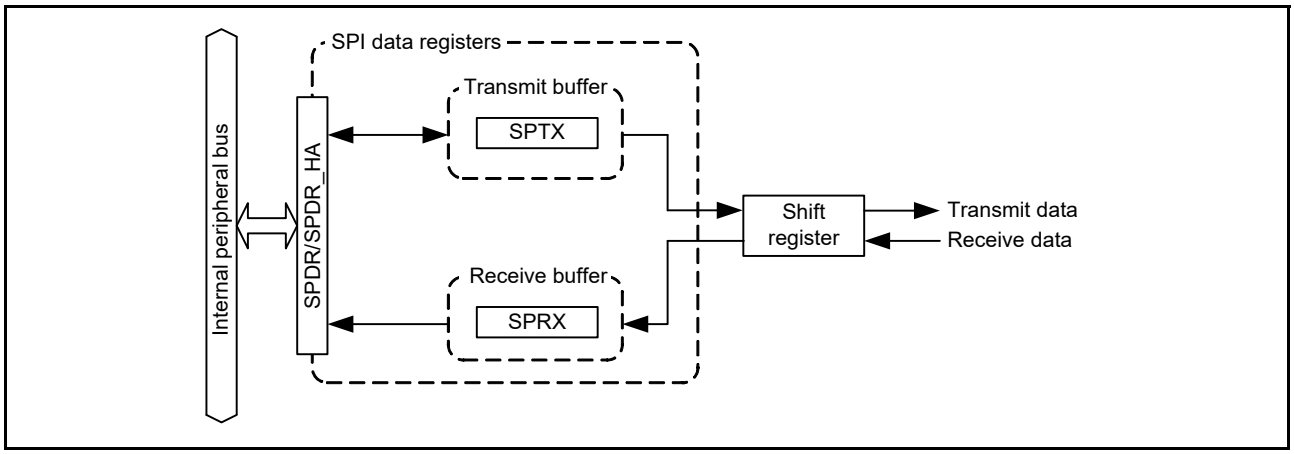


Figure 31.2 Configuration of SPDR/SPDR_HA

The transmit and receive buffers each have one stage. The two stages of the buffer are all mapped to the single address of SPDR/SPDR_HA. Data written to SPDR/SPDR_HA is written to a transmit-buffer stage (SPTX) and then transmitted from the buffer. The receive buffer holds received data on completion of reception. The receive buffer is not updated if an overrun occurs.

If the data length is not 32 bits, bits not referred to in SPTX are stored in the associated bits in SPRX. For example, if the data length is 9 bits, the received data is stored in the SPRX[8:0] bits, and the SPTX[31:9] bits are stored in the SPRX[31:9] bits.

(1) Bus Interface

SPDR/SPDR_HA is an interface with 32-bit wide transmit and receive buffers, each of which has one stage, for a total of 8 bytes. The 8 bytes are mapped to the 4-byte address space for SPDR/SPDR_HA. The unit of access for SPDR/SPDR_HA is selected in the SPI halfword access specification bit in the SPI Data Control Register (SPDCR.SPLW).

Flush transmission data at the LSB end of the register and store received data at the LSB end.

This section describes operations involved in writing to and reading from SPDR/SPDR_HA.

(a) Writing

Data written to SPDR/SPDR_HA is written to a transmit buffer (SPTX). This is not affected by the value of the SPDCR.SPRDTD bit, unlike when reading from SPDR/SPDR_HA.

Figure 31.3 shows the configuration of the bus interface with the transmit buffer when writing to SPDR/SPDR_HA.

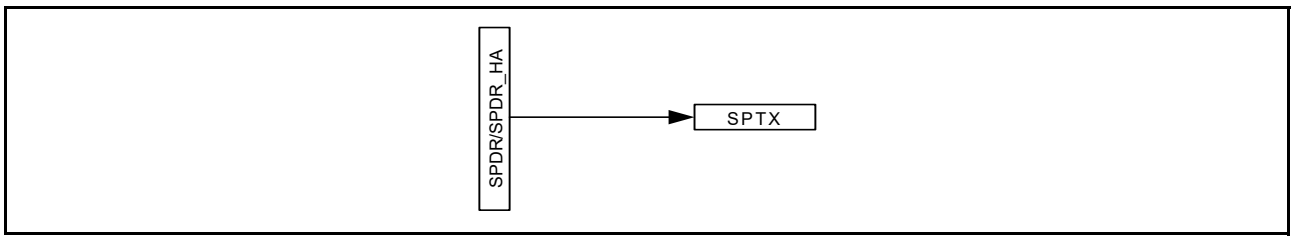


Figure 31.3 Configuration of SPDR/SPDR_HA for write access

Write the transfer data to SPTX after generating the transmit buffer empty interrupt (when SPSR.SPTEF is 1). Even when the data is written to the transmit buffer (SPTX), the value of the buffer is not updated after completion of the writing and before the next transmit buffer empty interrupt is generated (when SPTEF is 0).

(b) Reading

SPDR/SPDR_HA can be accessed to read the value of a receive buffer (SPRX) or a transmit buffer (SPTX). The setting in the SPI receive/transmit data select bit in the SPI Data Control Register (SPDCR.SPRDTD) selects whether reading is of the receive or transmit buffer.

Figure 31.4 shows the configuration of the bus interface with the receive and transmit buffers, for reads from SPDR/SPDR_HA.

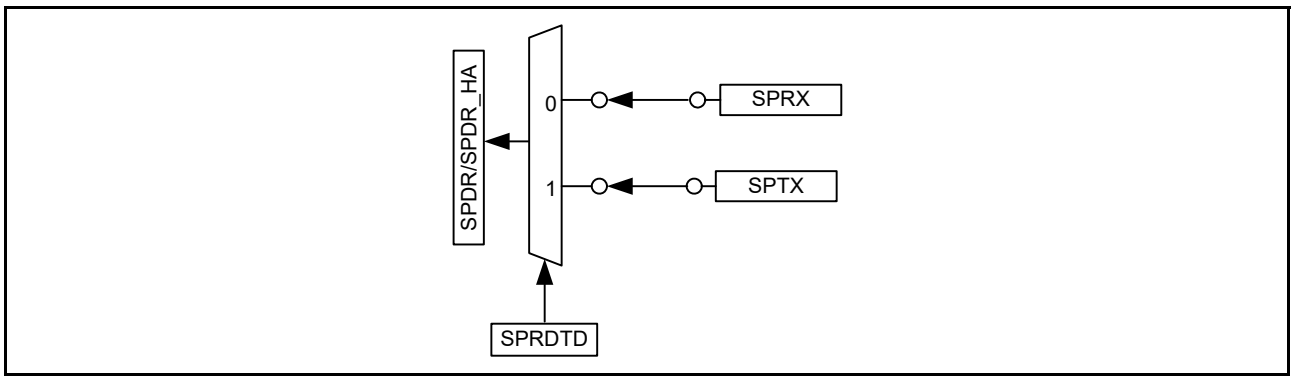


Figure 31.4 Configuration of SPDR/SPDR_HA for read access

After generation of the transmit buffer empty interrupt, the values read from the buffer are all 0s in the interval after completion of writing the data frame and before generation of the next buffer empty interrupt (when SPSR.SPTEF is 0).

31.2.6 SPI Bit Rate Register (SPBR)

Address(es): SPI0.SPBR 4007 200Ah, SPI1.SPBR 4007 210Ah

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

SPBR sets the bit rate in master mode. If the contents of SPBR are changed while both the SPCR.MSTR and SPCR.SPE bits are 1, do not perform subsequent operations.

When the SPI is used in slave mode, the bit rate depends on the bit rate of the input clock, regardless of the settings in the SPBR and the SPCMD0.BRDV[1:0] bits (bit rate division setting). For the input clock, use bit rates that satisfy the electrical characteristics of the device.

The bit rate is determined by the combination of the SPBR and SPCMD0.BRDV[1:0] settings. The equation to calculate the bit rate is as follows:

$$\text{Bit rate} = \frac{f\,(\text{PCLKB})}{2 \times (n + 1) \times 2^{N}}$$

In the equation, n denotes an SPBR setting (0, 1, 2, …, 255), and N denotes a BRDV[1:0] bit setting (0, 1, 2, or 3).

Table 31.3 lists examples of the relationship between the SPBR settings, BRDV[1:0] settings, and bit rates.

Table 31.3 Relationship between SPBR settings, BRDV[1:0] settings, and bit rates (1 of 2)

SPBR (n)	BRDV[1:0] bits (N)	Division ratio	Bit rate when PCLKB = 32 MHz
0	0	2	16.0 Mbps
1	0	4	8.00 Mbps
2	0	6	5.33 Mbps
3	0	8	4.00 Mbps
4	0	10	3.20 Mbps
5	0	12	2.67 Mbps
5	1	24	1.33 Mbps
5	2	48	667 kbps

Table 31.3 Relationship between SPBR settings, BRDV[1:0] settings, and bit rates (2 of 2)

SPBR (n)	BRDV[1:0] bits (N)	Division ratio	Bit rate when PCLKB = 32 MHz
5	3	96	333 kbps
255	3	4096	7.81 kbps

31.2.7 SPI Data Control Register (SPDCR)

Address(es): SPI0.SPDCR 4007 200Bh, SPI1.SPDCR 4007 210Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	SPBYT	SPLW	SPRDTD	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	SPRDTD	SPI Receive/Transmit Data Select	0: Read SPDR/SPDR_HA values from receive buffer 1: Read SPDR/SPDR_HA values from transmit buffer, but only if the transmit buffer is empty.	R/W
b5	SPLW	SPI Word Access/Halfword Access Specification	0: Set SPDR_HA to valid for halfword access 1: Set SPDR to valid for word access.	R/W
b6	SPBYT	SPI Byte Access Specification	0: SPDR is accessed in halfword or word (SPLW is valid) 1: SPDR is accessed in byte (SPLW is invalid).	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

SPRDTD bit (SPI Receive/Transmit Data Select)

The SPRDTD bit selects whether the SPDR/SPDR_HA reads values from the receive buffer or from the transmit buffer. If reading is from the transmit buffer, the last value written to SPDR/SPDR_HA register is read. Read the transmit buffer after generation of the transmit buffer empty interrupt (when SPSR.SPTEF is 1).

For details, see section 31.2.5, SPI Data Register (SPDR/SPDR_HA).

SPLW bit (SPI Word Access/Halfword Access Specification)

The SPLW bit specifies the access width for the SPDR register. Access to SPDR_HA in halfwords is valid when the SPLW bit is 0 and access to the SPDR register in words is valid when the SPLW bit is 1. In addition, when the SPLW bit is 0, set the SPCMD0.SPB[3:0] bits (SPI data length setting bits) from 8 to 16 bits. When 20, 24, or 32 bits is specified, do not perform any operations.

SPBYT bit (SPI Byte Access Specification)

This bit is used to set the data width of access to the SPI Data Register (SPDR). When SPBYT = 0, use word or half word access to SPDR. When SPBYT = 1 (in that case, SPLW is invalid), use byte access to SPDR. When SPBYT = 1, set the SPI data length bits (SPB[3:0]) in the SPI Command Register n (SPCMDn) to 8 bits. If SPB[3:0] are set to 9 to 16, 20, 24, or 32 bit, subsequent operation is not guaranteed.

31.2.8 SPI Clock Delay Register (SPCKD)

Address(es): SPI0.SPCKD 4007 200Ch, SPI1.SPCKD 4007 210Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SCKDL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	SCKDL[2:0]	RSPCK Delay Setting	b2 b0 0 0 0: 1 RSPCK 0 0 1: 2 RSPCK 0 1 0: 3 RSPCK 0 1 1: 4 RSPCK 1 0 0: 5 RSPCK 1 0 1: 6 RSPCK 1 1 0: 7 RSPCK 1 1 1: 8 RSPCK.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SPCKD sets the RSPCK delay, the period from the beginning of SSLni signal assertion to RSPCK oscillation, when the SPCMD0.SCKDEN bit is 1. If the contents of SPCKD are changed while both the SPCR.MSTR and SPCR.SPE bits are 1, do not perform subsequent operations.

SCKDL[2:0] bits (RSPCK Delay Setting)

The SCKDL[2:0] bits set an RSPCK delay value when the SPCMD0.SCKDEN bit is 1. When using the SPI in slave mode, set the SCKDL[2:0] bits to 000b.

31.2.9 SPI Slave Select Negation Delay Register (SSLND)

Address(es): SPI0.SSLND 4007 200Dh, SPI1.SSLND 4007 210Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SLNDL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	SLNDL[2:0]	SSL Negation Delay Setting	b2 b0 0 0 0: 1 RSPCK 0 0 1: 2 RSPCK 0 1 0: 3 RSPCK 0 1 1: 4 RSPCK 1 0 0: 5 RSPCK 1 0 1: 6 RSPCK 1 1 0: 7 RSPCK 1 1 1: 8 RSPCK.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SSLND sets the SSL negation delay, the period from the transmission of a final RSPCK edge to the negation of the SSLni signal during a serial transfer by the SPI in master mode. If the contents of SSLND are changed while both the SPCR.MSTR and SPCR.SPE bits are 1, do not perform subsequent operations.

SLNDL[2:0] bits (SSL Negation Delay Setting)

The SLNDL[2:0] bits set an SSL negation delay value when the SPI is in master mode. When using the SPI in slave mode, set the SLNDL[2:0] bits to 000b.

31.2.10 SPI Next-Access Delay Register (SPND)

Address(es): SPI0.SPND 4007 200Eh, SPI1.SPND 4007 210Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SPNDL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	SPNDL[2:0]	SPI Next-Access Delay Setting	b2 b0 0 0 0: 1 RSPCK + 2 PCLKB 0 0 1: 2 RSPCK + 2 PCLKB 0 1 0: 3 RSPCK + 2 PCLKB 0 1 1: 4 RSPCK + 2 PCLKB 1 0 0: 5 RSPCK + 2 PCLKB 1 0 1: 6 RSPCK + 2 PCLKB 1 1 0: 7 RSPCK + 2 PCLKB 1 1 1: 8 RSPCK + 2 PCLKB.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SPND sets the next-access delay, the non-active period of the SSLni signal after termination of a serial transfer when the SPCMD0.SPNDEN bit is 1. If the contents of SPND are changed while both the SPCR.MSTR and SPCR.SPE bits are 1, do not perform subsequent operations.

SPNDL[2:0] bits (SPI Next-Access Delay Setting)

The SPNDL[2:0] bits set a next-access delay when the SPCMD0.SPNDEN bit is 1. When using the SPI in slave mode, set the SPNDL[2:0] bits to 000b.

31.2.11 SPI Control Register 2 (SPCR2)

Address(es): SPI0.SPCR2 4007 200Fh, SPI1.SPCR2 4007 210Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SCKASE	PTE	SPIIE	SPOE	SPPE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SPPE	Parity Enable	0: No parity bit added to transmit data and parity bit in receive data not checked 1: When SPCR.TXMD = 0: Parity bit added to transmit data and parity bit of receive data checked When SPCR.TXMD = 1: Parity bit added to transmit data but parity bit of receive data not checked.	R/W
b1	SPOE	Parity Mode	0: Even parity selected for transmission and reception 1: Odd parity selected for transmission and reception.	R/W
b2	SPIIE	SPI Idle Interrupt Enable	0: Idle interrupt requests disabled 1: Idle interrupt requests enabled.	R/W
b3	PTE	Parity Self-Testing	0: Self-diagnosis function of the parity circuit disabled 1: Self-diagnosis function of the parity circuit enabled.	R/W
b4	SCKASE	RSPCK Auto-Stop Function Enable	0: RSPCK auto-stop function disabled 1: RSPCK auto-stop function enabled.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

If the SPPE, SPOE, or SCKASE bit in SPCR2 is changed while the SPCR.SPE bit is 1, do not perform subsequent operations.

SPPE bit (Parity Enable)

The SPPE bit enables or disables the parity function.

When the SPCR.TXMD bit is 0 and this bit is 1, the parity bit is added to transmit data and parity checking is performed for receive data. When the SPCR.TXMD bit is 1 and this bit is 1, the parity bit is added to transmit data but parity checking is not performed for receive data.

SPOE bit (Parity Mode)

The SPOE bit specifies odd or even parity.

When even parity is set, parity bit addition is performed so that the total number of 1-bits in the transmit or receive character plus the parity bit is even. Similarly, when odd parity is set, parity bit addition is performed so that the total number of 1-bits in the transmit or receive character plus the parity bit is odd.

The SPOE bit is valid only when the SPPE bit is 1.

SPIIE bit (SPI Idle Interrupt Enable)

The SPIIE bit enables or disables the generation of SPI idle interrupt requests when an SPI idle state is detected and the SPSR.IDLNF flag is set to 0.

PTE bit (Parity Self-Testing)

The PTE bit enables self-diagnosis of the parity circuit to check whether the parity function is operating correctly.

SCKASE bit (RSPCK Auto-Stop Function Enable)

The SCKASE bit enables or disables the RSPCK auto-stop function. When this function is enabled, the RSPCK clock is stopped before an overrun error occurs when data is received in master mode. For details, see section 31.3.8.1, Overrun errors.

31.2.12 SPI Command Registers 0 (SPCMD0)

Address(es): SPI0.SPCMD0 4007 2010h, SPI1.SPCMD0 4007 2110h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SCKDEN	SLNDEN	SPNDEN	LSBF	SPB[3:0]				—	SSLA[2:0]			BRDV[1:0]		CPOL	CPHA
Value after reset:	0	0	0	0	0	1	1	1	0	0	0	0	1	1	0	1

Bit	Symbol	Bit name	Description	R/W
b0	CPHA	RSPCK Phase Setting	0: Select data sampling on leading edge, data change on trailing edge 1: Select data change on leading edge, data sampling on trailing edge.	R/W
b1	CPOL	RSPCK Polarity Setting	0: Set RSPCK low when idle 1: Set RSPCK high when idle.	R/W
b3, b2	BRDV[1:0]	Bit Rate Division Setting	b3 b2 0 0: Base bit rate 0 1: Base bit rate divided by 2 1 0: Base bit rate divided by 4 1 1: Base bit rate divided by 8.	R/W
b6 to b4	SSLA[2:0]	SSL Signal Assertion Setting	b6 b4 0 0 0: SSL0 0 0 1: SSL1 0 1 0: SSL2 0 1 1: SSL3 1 x x: Setting prohibited. x: Don't care.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit name	Description	R/W
b11 to b8	SPB[3:0]	SPI Data Length Setting	b11 b8 0100 to 0111: 8 bits 1 0 0 0: 9 bits 1 0 0 1: 10 bits 1 0 1 0: 11 bits 1 0 1 1: 12 bits 1 1 0 0: 13 bits 1 1 0 1: 14 bits 1 1 1 0: 15 bits 1 1 1 1: 16 bits 0 0 0 0: 20 bits 0 0 0 1: 24 bits 0010, 0011: 32 bits.	R/W
b12	LSBF	SPI LSB First	0: MSB-first 1: LSB-first.	R/W
b13	SPNDEN	SPI Next-Access Delay Enable	0: Next-access delay is 1 RSPCK + 2 PCLKB 1: Next-access delay equals to the setting in the SPI Next-access Delay register (SPND).	R/W
b14	SLNDEN	SSL Negation Delay Setting Enable	0: An SSL negation delay of 1 RSPCK 1: An SSL negation delay equals to the setting in the SPI Slave Select Negation Delay register (SSLND).	R/W
b15	SCKDEN	RSPCK Delay Setting Enable	0: An RSPCK delay of 1 RSPCK 1: An RSPCK delay equals to the setting in the SPI Clock Delay register (SPCKD).	R/W

SPCMD0 sets a transfer format for the SPI in master mode.

Set this register while the transmit buffer is empty (SPSR.SPTEF is 1 and data for the next transfer is not set), and before the setting of data to be transmitted when this register is referenced.

If the contents of SPCMD0 are changed while the SPCR.SPE bit is 1, do not perform subsequent operations.

CPHA bit (RSPCK Phase Setting)

The CPHA bit sets the RSPCK phase for the SPI in master mode or slave mode. Data communications between SPI modules require the same RSPCK phase setting between the modules.

CPOL bit (RSPCK Polarity Setting)

The CPOL bit sets the RSPCK polarity for the SPI in master mode or slave mode. Data communications between SPI modules require the same RSPCK polarity setting between the modules.

BRDV[1:0] bits (Bit Rate Division Setting)

The BRDV[1:0] bits determine the bit rate combination of the settings in SPBR (see section 31.2.6, SPI Bit Rate Register (SPBR)). The SPBR settings determine the base bit rate. The BRDV[1:0] settings select a bit rate obtained by dividing the base bit rate by 1, 2, 4, or 8. Different BRDV[1:0] bit settings can be specified, enabling execution of serial transfers at a different bit rate for each command.

SSLA[2:0] bits (SSL Signal Assertion Setting)

The SSLA[2:0] bits control the SSLni signal assertion when the SPI performs serial transfers in master mode.

When an SSLni signal is asserted, its polarity is determined by the value set in the associated SSLP. When the SSLA[2:0] bits are set to 000b in multi-master mode, serial transfers are performed with all the SSL signals in the negated state, as the SSLn0 pin acts as input.

When using the SPI in slave mode, set the SSLA[2:0] bits to 000b.

SPB[3:0] bits (SPI Data Length Setting)

The SPB[3:0] bits set a transfer data length for the SPI in master or slave mode.

When the SPLW bit is 0, set these bits from 8 to 16 bits.

LSBF bit (SPI LSB First)

The LSBF bit sets the data format of the SPI in master or slave mode to MSB-first or LSB-first.

SPNDEN bit (SPI Next-Access Delay Enable)

The SPNDEN bit sets the next-access delay, the period from when the SPI in master mode terminates a serial transfer and sets the SSLni signal inactive until the SPI enables the SSLni signal assertion for the next access. If the SPNDEN bit is 0, the SPI sets the next-access delay to 1 RSPCK + 2 PCLKB. If the SPNDEN bit is 1, the SPI inserts a next-access delay according to the SPND setting.

When using the SPI in slave mode, set the SPNDEN bit to 0.

SLNDEN bit (SSL Negation Delay Setting Enable)

The SLNDEN bit sets the SSL negation delay, the period from when the SPI in master mode stops RSPCK oscillation until the SPI sets the SSLni signal inactive. If the SLNDEN bit is 0, the SPI sets the SSL negation delay to 1 RSPCK. If the SLNDEN bit is 1, the SPI negates the SSL signal to an SSL negation delay according to the SSLND setting.

When using the SPI in slave mode, set the SLNDEN bit to 0.

SCKDEN bit (RSPCK Delay Setting Enable)

The SCKDEN bit sets the SPI clock delay, the period from when the SPI in master mode activates the SSLni signal until the RSPCK starts oscillation. If the SCKDEN bit is 0, the SPI sets the RSPCK delay to 1 RSPCK. If the SCKDEN bit is 1, the SPI starts the oscillation of RSPCK at an RSPCK delay according to the SPCKD setting.

When using the SPI in slave mode, set the SCKDEN bit to 0.

31.3 Operation

In this section, the *serial transfer period* means the period from the beginning of driving valid data to the fetching of the final valid data.

31.3.1 Overview of SPI Operations

The SPI is capable of synchronous serial transfers in the following modes:

- Slave mode (SPI operation)
- Single-master mode (SPI operation)
- Multi-master mode (SPI operation)
- Slave mode (clock synchronous operation)
- Master mode (clock synchronous operation).

The SPI mode can be selected with the MSTR, MODFEN, and SPMS bits in SPCR. Table 31.4 lists the relationship between SPI modes and SPCR settings, and a description of each mode.

Table 31.4 Relationship between SPI modes and SPCR settings and description of each mode (1 of 2)

Mode	Slave (SPI operation)	Single-master (SPI operation)	Multi-master (SPI operation)	Slave (clock synchronous operation)	Master (clock synchronous operation)
MSTR bit setting	0	1	1	0	1
MODFEN bit setting	0 or 1	0	1	0	0
SPMS bit setting	0	0	0	1	1
RSPCKn signal	Input	Output	Output/Hi-Z	Input	Output
MOSIn signal	Input	Output	Output/Hi-Z	Input	Output
MISOn signal	Output/Hi-Z	Input	Input	Output	Input
SSLn0 signal	Input	Output	Input	Hi-Z*1	Hi-Z*1
SSLn1 to SSLn3 signals	Hi-Z*1	Output	Output/Hi-Z	Hi-Z*1	Hi-Z*1

Table 31.4 Relationship between SPI modes and SPCR settings and description of each mode (2 of 2)

Mode	Slave (SPI operation)	Single-master (SPI operation)	Multi-master (SPI operation)	Slave (clock synchronous operation)	Master (clock synchronous operation)
SSL polarity change function	Supported	Supported	Supported	—	—
Transfer rate	Up to PCLKB/6	Up to PCLKB/2	Up to PCLKB/2	Up to PCLKB/6	Up to PCLKB/2
Clock source	RSPCKn input	On-chip baud rate generator	On-chip baud rate generator	RSPCKn input	On-chip baud rate generator
Clock polarity	Two				
Clock phase	Two	Two	Two	One (CPHA = 1)	Two
First transfer bit	MSB/LSB				
Transfer data length	8 to 16, 20, 24, 32 bits				
RSPCK delay control	Not supported	Supported	Supported	Not supported	Supported
SSL negation delay control	Not supported	Supported	Supported	Not supported	Supported
Next-access delay control	Not supported	Supported	Supported	Not supported	Supported
Transfer activation method	SSL input active or RSPCK oscillation	Transmit buffer is written to on generation of transmit buffer empty interrupt request (SPTEF is 1)	Transmit buffer is written to on generation of transmit buffer empty interrupt request (SPTEF is 1)	RSPCK oscillation	Transmit buffer is written to on generation of a transmit buffer empty interrupt request (SPTEF is 1)
Transmit buffer empty detection	Supported				
Receive buffer full detection	Supported*2				
Overrun error detection	Supported*2	Supported*2, *4	Supported*2, *4	Supported*2	Supported*2
Parity error detection	Supported*2,*3				
Mode fault error detection	Supported (MODFEN = 1)	Not supported	Supported	Not supported	Not supported
Underrun error detection	Supported	Not supported	Not supported	Supported	Not supported

Note 1. This function is not supported in this mode.
Note 2. When the SPCR.TXMD bit is 1, detection of receiver buffer full, overrun error, and parity error are not performed.
Note 3. When the SPCR2.SPPE bit is 0, parity error detection is not performed.
Note 4. When the SPCR2.SCKASE bit is 1, overrun error detection does not proceed.

31.3.2 Controlling the SPI Pins

The SPI can switch pin states based on the MSTR, MODFEN, and SPMS bit settings in SPCR. Table 31.5 lists the relationship between the pin states and bit settings. The I/O port settings must follow this relationship.

Table 31.5 Relationship between pin states and bit settings (1 of 2)

Mode	Pin	Pin state*2
Single-master mode (SPI operation) (MSTR = 1, MODFEN = 0, SPMS = 0)	RSPCKn	CMOS output
	SSLn0 to SSLn3	CMOS output
	MOSIn	CMOS output
	MISOn	Input
Multi-master mode (SPI operation) (MSTR = 1, MODFEN = 1, SPMS = 0)	RSPCKn*3	CMOS output/Hi-Z
	SSLn0	Input
	SSLn1 to SSLn3*3	CMOS output/Hi-Z
	MOSIn*3	CMOS output/Hi-Z
	MISOn	Input

Table 31.5 Relationship between pin states and bit settings (2 of 2)

Mode	Pin	Pin state*2
Slave mode (SPI operation) (MSTR = 0, SPMS = 0)	RSPCKn	Input
	SSLn0	Input
	SSLn1 to SSLn3*5	Hi-Z*1
	MOSIn	Input
	MISOn*4	CMOS output/Hi-Z
Master mode (clock synchronous operation) (MSTR = 1, MODFEN = 0, SPMS = 1)	RSPCKn	CMOS output
	SSLn0 to SSLn3*5	Hi-Z*1
	MOSIn	CMOS output
	MISOn	Input
Slave mode (clock synchronous operation) (MSTR = 0, SPMS = 1)	RSPCKn	Input
	SSLn0 to SSLn3*5	Hi-Z*1
	MOSIn	Input
	MISOn	CMOS output

Note 1. This function is not supported in this mode.
Note 2. SPI settings are not reflected in multiplexed pins for which the SPI function is not selected.
Note 3. When SSLn0 is at the active level, the pin state is Hi-Z.
Note 4. When SSLn0 is at the non-active level or the SPCR.SPE bit is 0, the pin state is Hi-Z.
Note 5. These pins are available for use as I/O port pins.

The SPI in single-master mode (SPI operation) or multi-master mode (SPI operation) determines the MOSI signal values during the SSL negation period based on the MOIFE and MOIFV bit settings in SPPCR, as listed in Table 31.6.

Table 31.6 MOSI signal value determination during SSL negation period

MOIFE bit	MOIFV bit	MOSIn signal value during SSL negation period
0	0, 1	Final data from previous transfer
1	0	Low
1	1	High

31.3.3 SPI System Configuration Examples

31.3.3.1 Single master and single slave with the MCU as a master

Figure 31.5 shows a single-master and single-slave SPI system configuration example where the MCU is the master. In the single-master and single-slave configuration, the SSLn0 to SSLn3 outputs of the MCU (master) are not used. The SSL input of the SPI slave is fixed to the low level, and the SPI slave stays in the selected state.*1

The MCU (master) drives the RSPCKn and MOSIn signals. The SPI slave drives the MISO signals.

Note 1. In the transfer format used when SPCMD0.CPHA is 0, the SSL signal for some slave devices cannot be fixed to the active level. In this case, always connect the SSLni output of the MCU to the SSL input of the slave device.

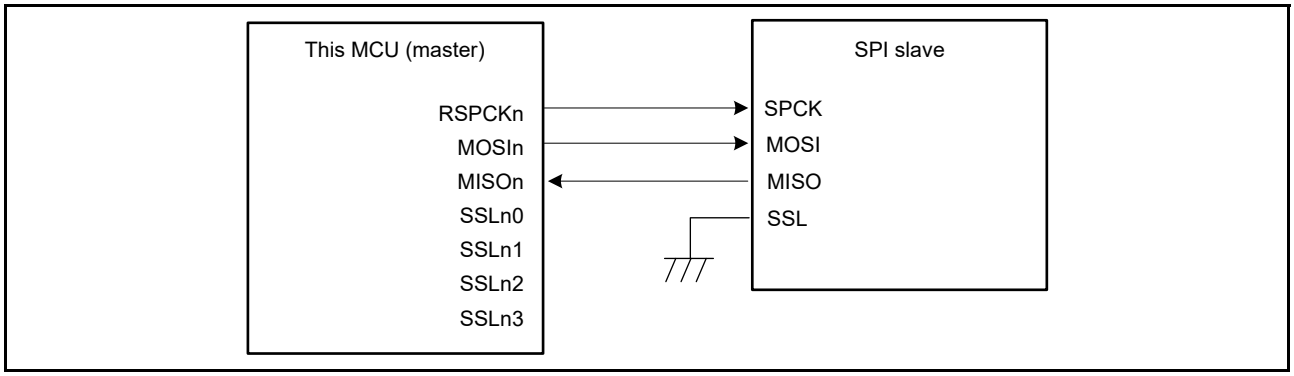


Figure 31.5 Single-master and single-slave configuration example with the MCU as the master

31.3.3.2 Single master and single slave with the MCU as a slave

Figure 31.6 shows a single-master and single-slave SPI system configuration example where the MCU is the slave. When the MCU is to operate as a slave, the SSLn0 pin is used as SSL input. The SPI master drives the RSPCK and MOSI signals. The MCU (slave) drives the MISOn signals.*1

In the single-slave configuration in which the SPCMD0.CPHA bit is set to 1, the SSLn0 input of the MCU (slave) is fixed to the low level, and the MCU (slave) stays in the selected state. This enables serial transfer (Figure 31.7).

Note 1. When SSLn0 is at the non-active level, the pin state is Hi-Z.

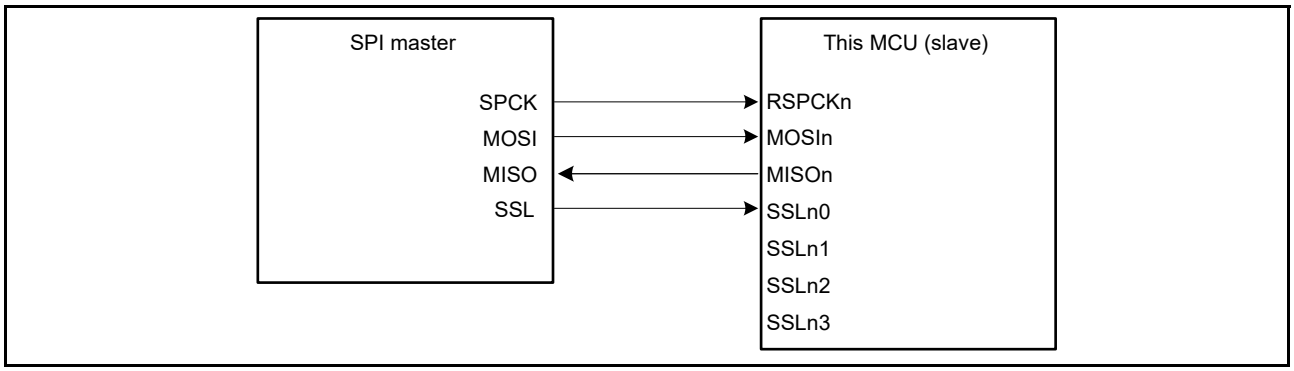


Figure 31.6 Single-master and single-slave configuration example with the MCU as a slave and CPHA = 0

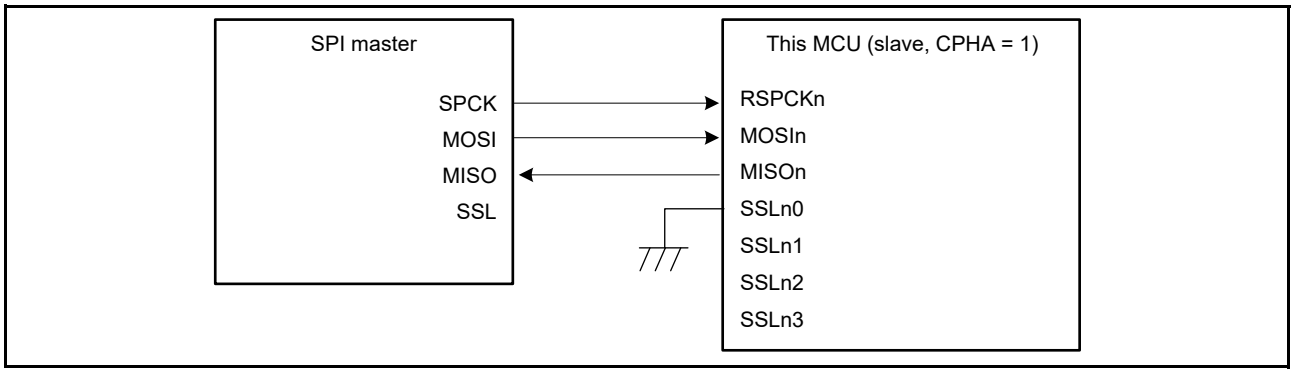


Figure 31.7 Single-master and single-slave configuration example with the MCU as a slave and CPHA = 1

31.3.3.3 Single master and multi-slave with the MCU as a master

Figure 31.8 shows a single-master/multi-slave SPI system configuration example where the MCU is the master. In the example, the SPI system includes the MCU (master) and four slaves (SPI slaves 0 to 3).

The RSPCKn and MOSIn outputs of the MCU (master) are connected to the RSPCK and MOSI inputs of SPI slaves 0 to 3. The MISO outputs of SPI slaves 0 to 3 are all connected to the MISOn input of the MCU (master). SSLn0 to SSLn3 outputs of the MCU (master) are connected to the SSL inputs of SPI slave 0 to SPI slave 3, respectively.

The MCU (master) drives RSPCKn, MOSIn, and SSLn0 to SSLn3. Of the SPI slaves 0 to 3, the slave that receives low-level input into the SSL input drives the MISO signal.

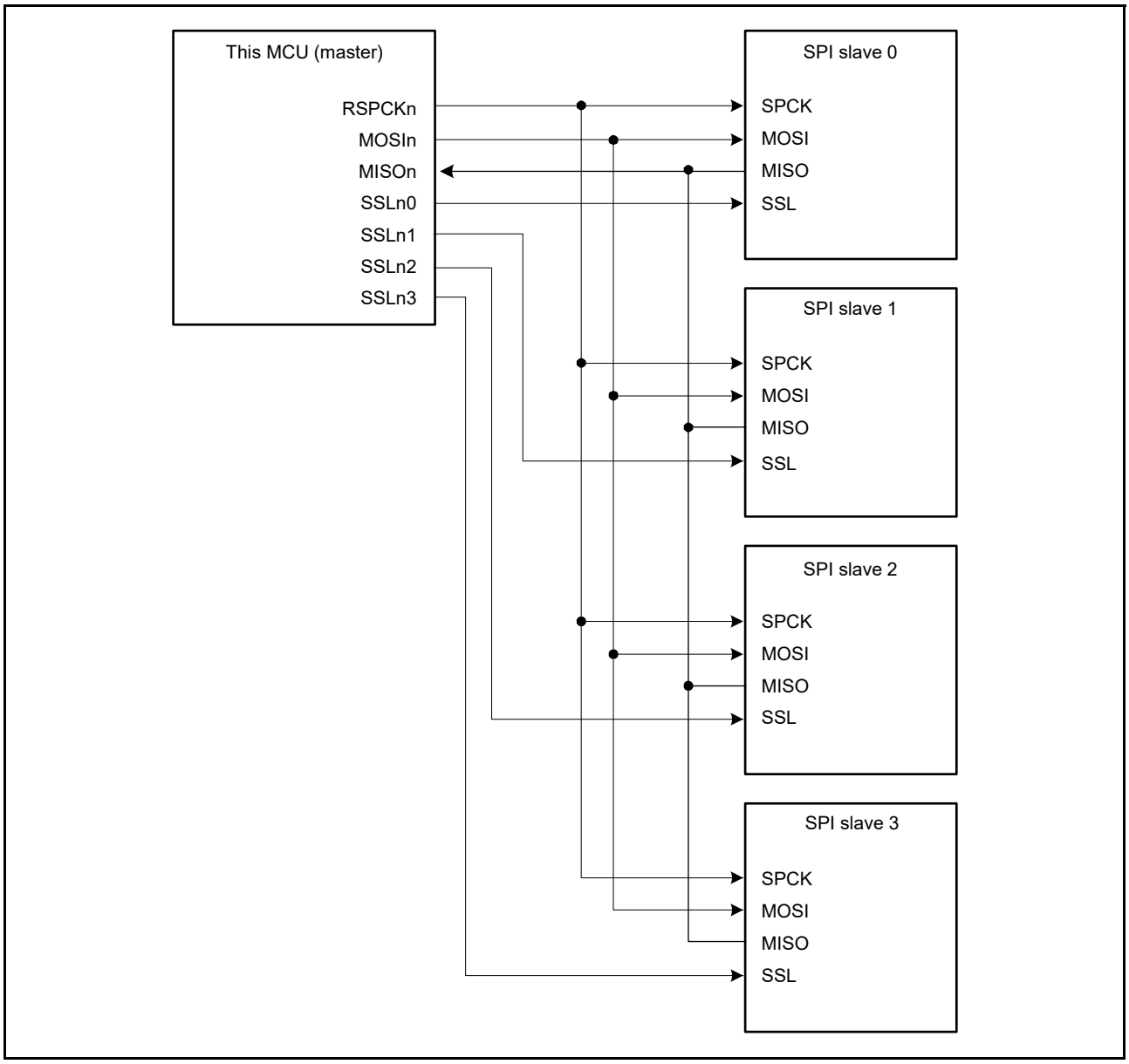


Figure 31.8 Single-master and multi-slave configuration example with the MCU as a master

31.3.3.4 Single master and multi-slave with the MCU as a slave

Figure 31.9 shows a single-master and multi-slave SPI system configuration example where the MCU is a slave. In the example, the SPI system includes an SPI master and two MCUs (slave X and slave Y).

The SPCK and MOSI outputs of the SPI master are connected to the RSPCKn and MOSIn inputs of the MCUs (slave X and slave Y). The MISOn outputs of the MCUs (slave X and slave Y) are all connected to the MISO input of the SPI master. SSLX and SSLY outputs of the SPI master are connected to the SSLn0 inputs of the MCUs (slave X and slave Y), respectively.

The SPI master drives SPCK, MOSI, SSLX, and SSLY. The MCU slave (X or Y) that receives low-level input into the SSLn0 input drives the MISOn signal.

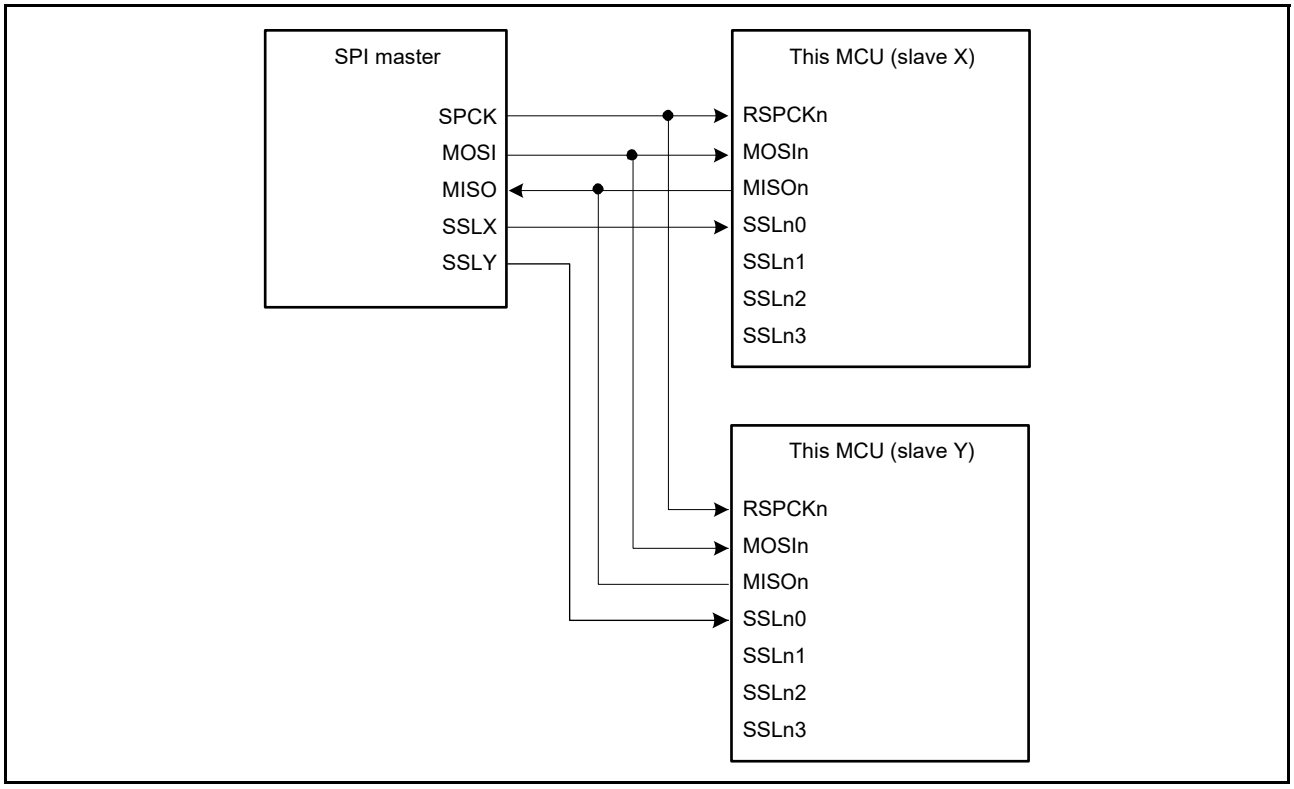


Figure 31.9 Single-master and multi-slave configuration example with the MCU as a slave

31.3.3.5 Multi-master and multi-slave with the MCU as a master

Figure 31.10 shows a multi-master/multi-slave SPI system configuration example where the MCU is a master. In the example, the SPI system includes two MCUs (master X and master Y) and two SPI slaves (SPI slave 1 and SPI slave 2).

The RSPCKn and MOSIn outputs of the MCUs (master X and master Y) are connected to the RSPCK and MOSI inputs of SPI slaves 1 and 2. The MISO outputs of SPI slaves 1 and 2 are connected to the MISOn inputs of the MCUs (master X and master Y). Any generic port Y output from the MCU (master X) is connected to the SSLn0 input of the MCU (master Y). Any generic port X output of the MCU (master Y) is connected to the SSLn0 input of the MCU (master X). The SSLn1 and SSLn2 outputs of the MCUs (master X and master Y) are connected to the SSL inputs of SPI slaves 1 and 2. In this configuration, because the system can be comprised solely of SSLn0 input, and SSLn1 and SSLn2 outputs for slave connections, the SSLn3 output of the MCU is not required.

The MCU drives RSPCKn, MOSIn, SSLn1, and SSLn2 when the SSLn0 input level is high. When the SSLn0 input level is low, the MCU detects a mode fault error, sets RSPCKn, MOSIn, SSLn1, and SSLn2 to Hi-Z, and releases the SPI bus directly to the other master. The SPI slave 1 or 2 that receives low-level input into the SSL input drives the MISO signal.

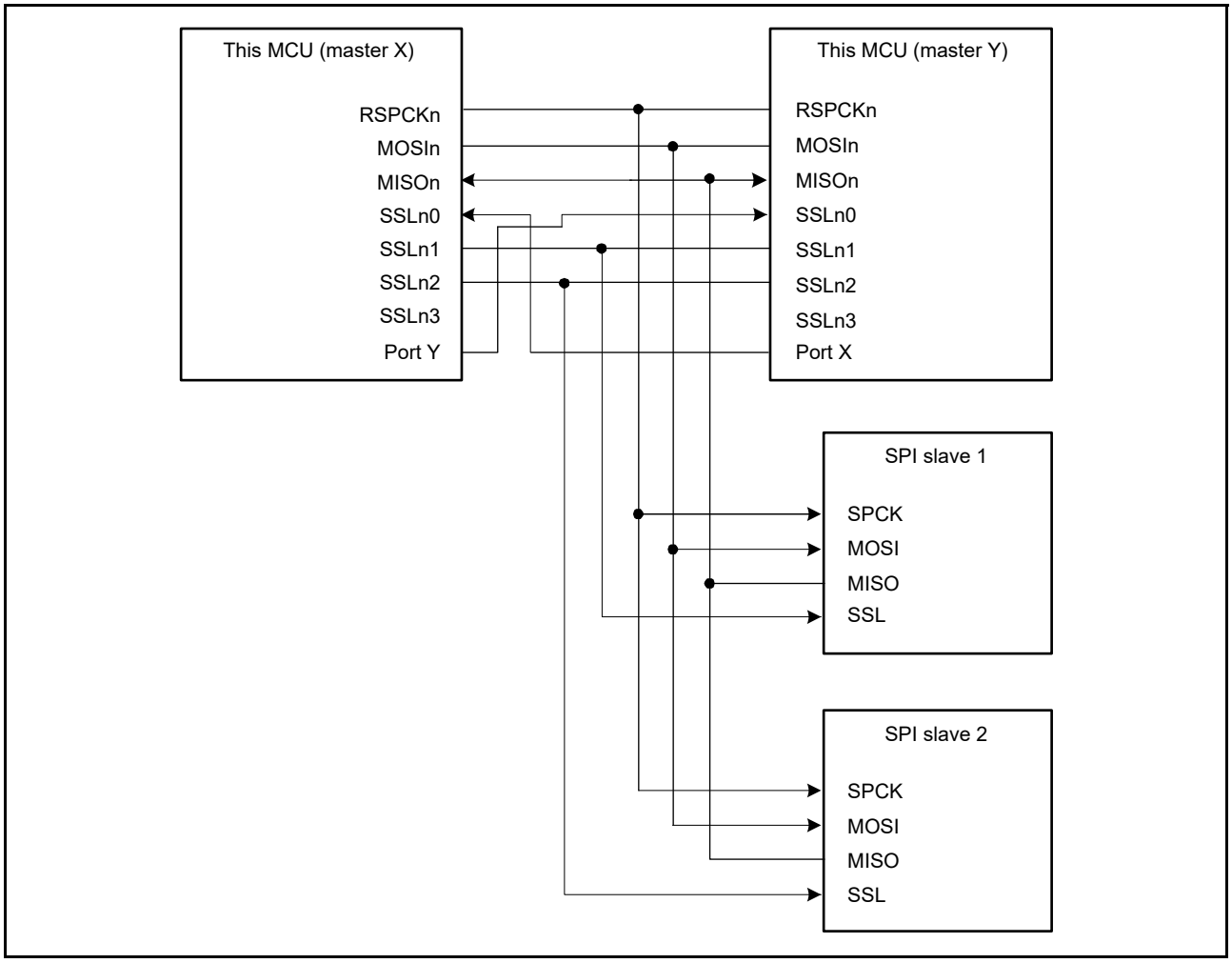


Figure 31.10 Multi-master and multi-slave configuration example with the MCU as a master

31.3.3.6 Master and slave in clock synchronous mode with the MCU as a master

Figure 31.11 shows a master and slave in clock synchronous mode configuration where the MCU is a master. In the master and slave clock synchronous mode, SSLn0 to SSLn3 of the MCU (master) are not used.

The MCU (master) drives RSPCKn and MOSIn. The SPI slave drives MISO.

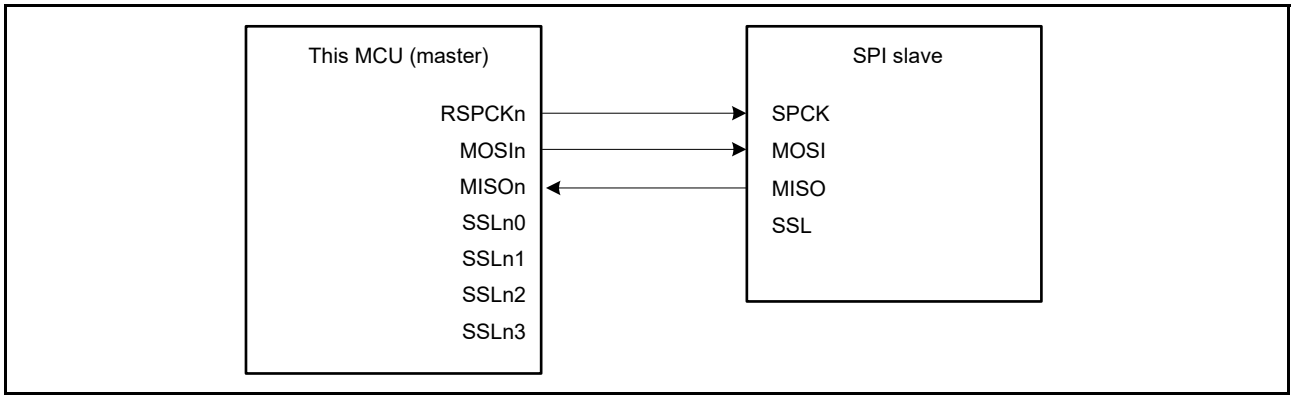


Figure 31.11 Configuration example of master and slave in clock synchronous mode with the MCU as a master

31.3.3.7 Master and slave in clock synchronous mode with the MCU as slave

Figure 31.12 shows a master and slave in clock synchronous mode configuration where the MCU is a slave. When the MCU is to operate as a slave in clock synchronous mode, the MCU (slave) drives MISOn and the SPI master drives SPCK and MOSI. In addition, SSLn0 to SSLn3 of the MCU (slave) are not used.

The MCU (slave) can only execute serial transfer in the single-slave configuration when SPCMD0.CPHA is set to 1.

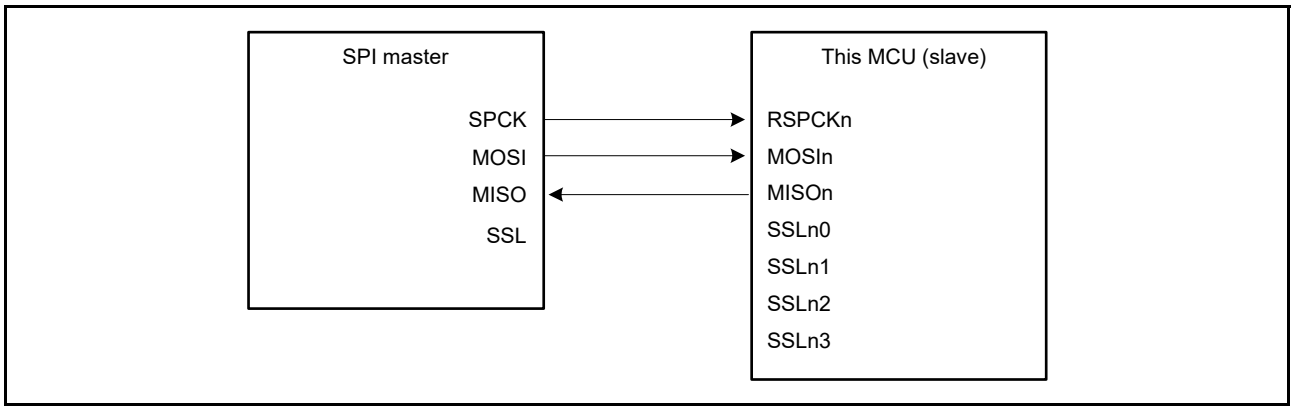


Figure 31.12 Configuration example of master and slave in clock synchronous mode with the MCU as a slave and CPHA = 1

31.3.4 Data Format

The data format of the SPI depends on the settings in SPI Command Register m (SPCMD0) and the parity enable bit in SPI Control Register 2 (SPCR2.SPPE). Regardless of whether the ordering is MSB- or LSB-first, the SPI treats the range from the LSB bit in the SPI Data Register (SPDR/SPDR_HA) to the bit corresponding to the selected data length as transfer data.

This section shows the format of one frame of data before or after transfer.

(a) Data format with parity disabled

When parity is disabled, transmission or reception of data proceeds with the length in bits selected in the SPI data length setting bits in SPI Command Register 0 (SPCMD0.SPB[3:0]).

(b) Data format with parity enabled

When parity is enabled, transmission or reception of data proceeds with the length in bits selected in the SPI data length setting bits in SPI Command Register 0 (SPCMD0.SPB[3:0]). In this case, however, the last bit is a parity bit.

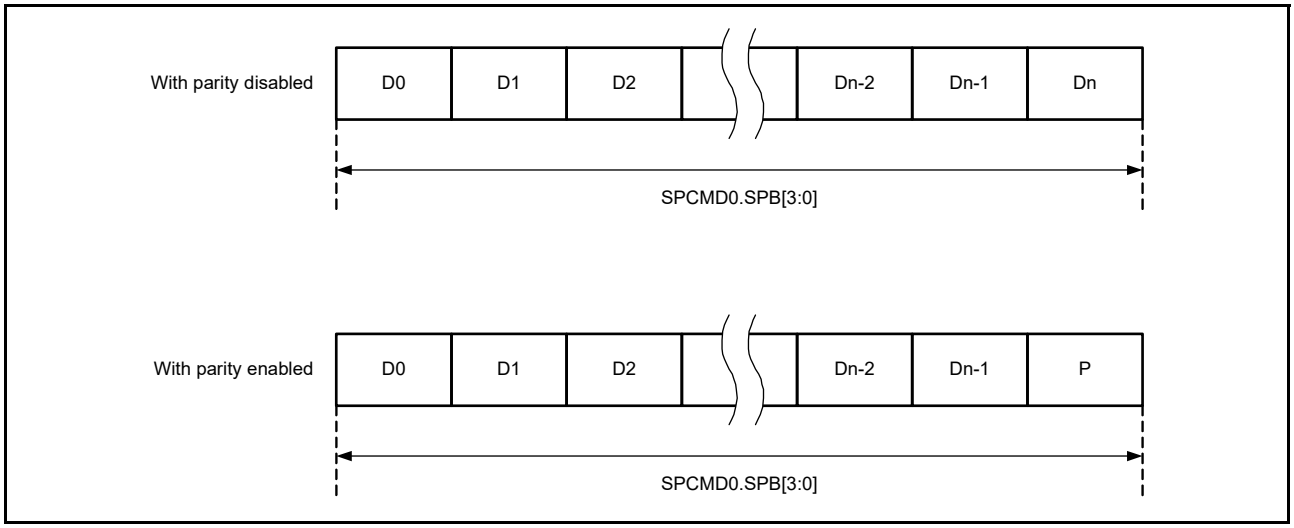


Figure 31.13 Data format with parity disabled and enabled

31.3.4.1 Operation when parity is disabled (SPCR2.SPPE = 0)

When parity is disabled, data for transmission is copied to the shift register with no prior processing. This section describes the connection between the SPI Data Register (SPDR/SPDR_HA) and the shift register in terms of the combination of MSB- or LSB-first order and data length.

(1) MSB-first transfer with 32-bit data

Figure 31.14 shows operations by the SPI Data Register (SPDR) and the shift register in transfers with parity disabled, an SPI data length of 32 bits, and MSB-first selected.

In transmission, bits T31 to T00 from the current stage of the transmit buffer are copied to the shift register. Data for transmission is shifted out from the shift register in order from T31 to T30, and continuing to T00.

In reception, received data is shifted in bit by bit through bit 0 of the shift register. When bits R31 to R00 are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer.

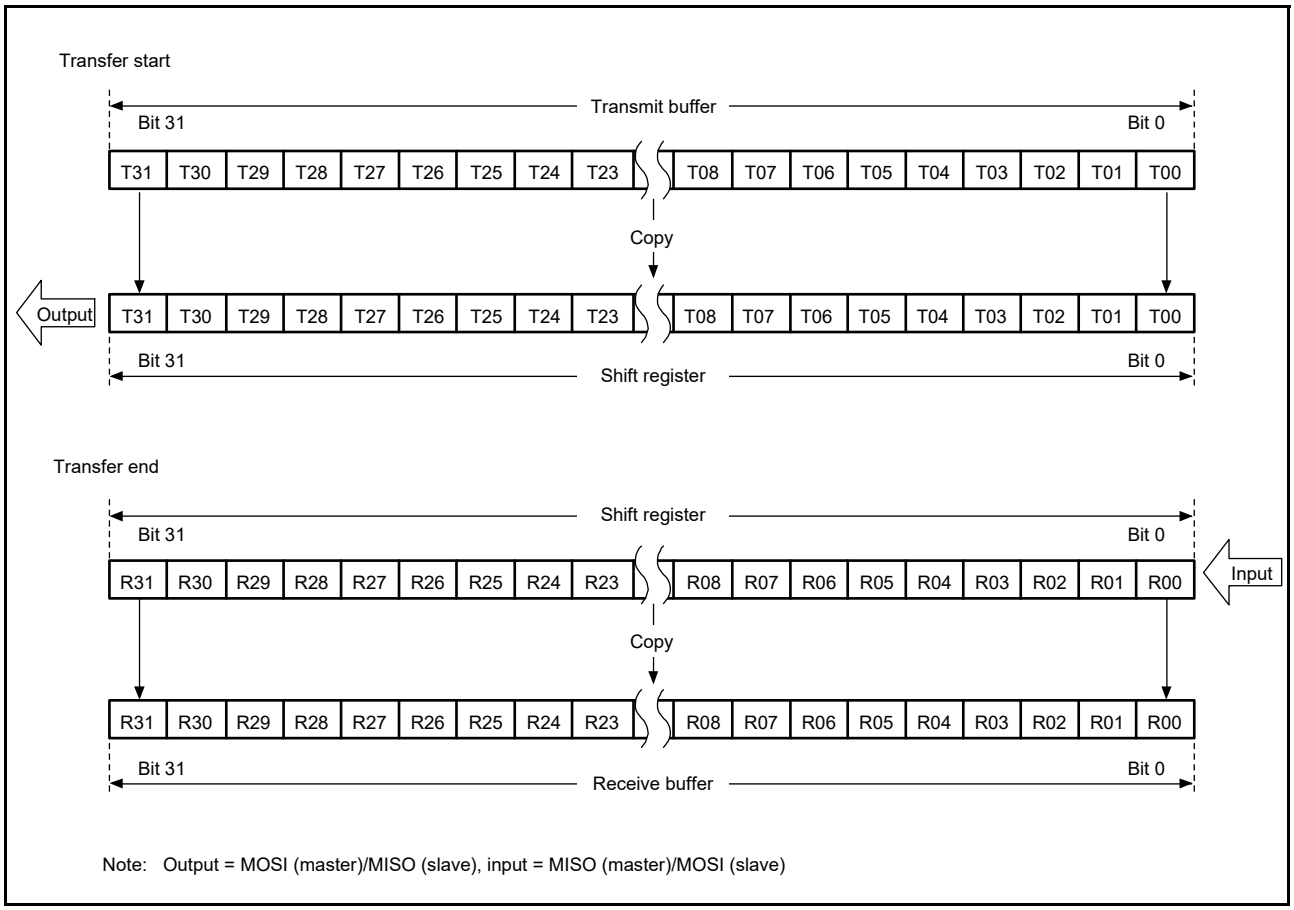


Figure 31.14 MSB-first transfer with 32-bit data and parity disabled

(2) MSB-first transfer with 24-bit data

Figure 31.15 shows operations by the SPI Data Register (SPDR) and the shift register in transfers with parity disabled, an SPI data length of 24 bits for an example that is not 32 bits, and MSB-first selected.

In transmission, the lower 24 bits (T23 to T00) from the current stage of the transmit buffer are copied to the shift register. Data for transmission is shifted out from the shift register in order from T23 to T22, and continuing to T00.

In reception, received data is shifted in bit by bit through bit 0 of the shift register. When bits R23 to R00 are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. The upper 8 bits of the transmit buffer are stored in the upper 8 bits of the receive buffer. Writing 0 to bits T31 to T24 during transmission results in 0 being inserted in the upper 8 bits of the receive buffer.

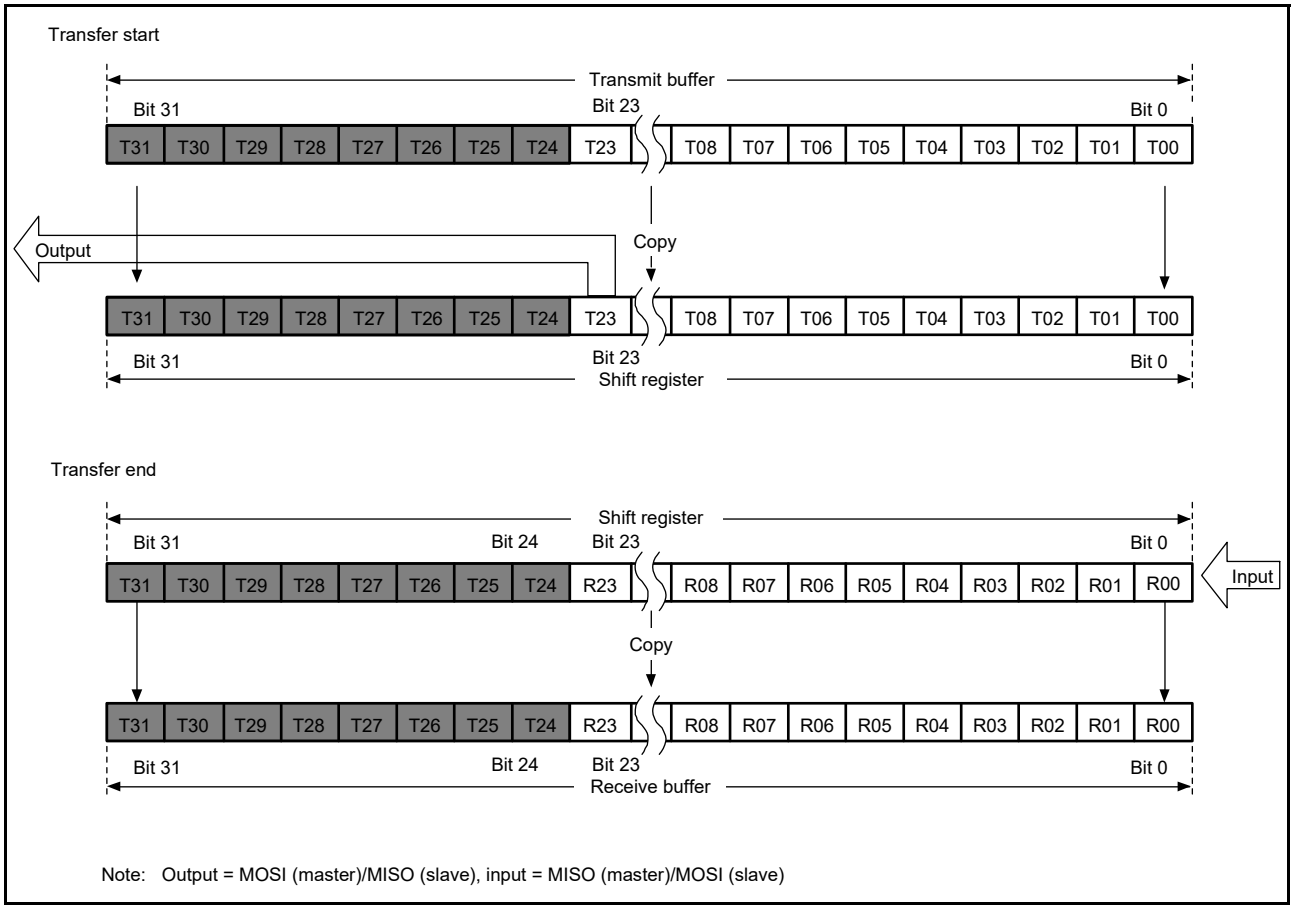


Figure 31.15 MSB-first transfer with 24-bit data and parity disabled

(3) LSB-first transfer with 32-bit data

Figure 31.16 shows operations by the SPI Data Register (SPDR) and the shift register in transfers with parity disabled, an SPI data length of 32 bits, and LSB-first selected.

In transmission, bits T31 to T00 from the current stage of the transmit buffer are reordered bit by bit to obtain the order T00 to T31 for copying to the shift register. Data for transmission is shifted out from the shift register in order from T00 to T01, and continuing to T31.

In reception, received data is shifted in bit by bit through bit 0 of the shift register. When bits R00 to R31 are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer.

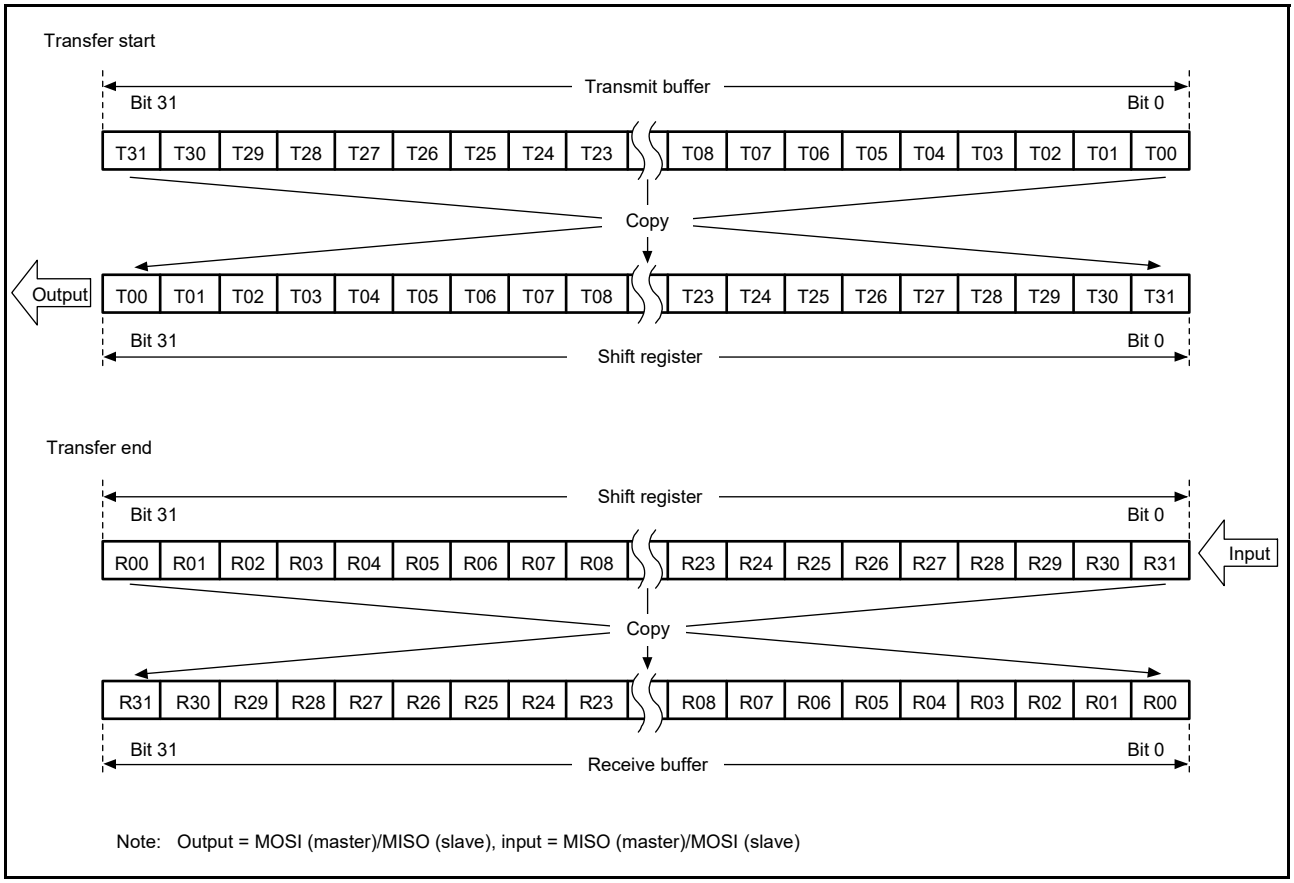


Figure 31.16 LSB-first transfer with 32-bit data and parity disabled

(4) LSB-first transfer with 24-bit data

Figure 31.17 shows operations by the SPI Data Register (SPDR) and the shift register in transfers with parity disabled, 24 bits as the SPI data length, for an example that is not 32 bits, and LSB-first selected.

In transmission, the lower 24 bits (T23 to T00) from the current stage of the transmit buffer are reordered bit by bit to obtain the order T00 to T23 for copying to the shift register. Data for transmission is shifted out from the shift register in order from T00 to T01, and continuing to T23.

In reception, received data is shifted in bit-by-bit through bit [8] of the shift register. When the R00 to R23 bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. The upper 8 bits of the transmit buffer are stored in the upper 8 bits of the receive buffer. Writing 0 to bits T31 to T24 during transmission leads to 0 being inserted in the upper 8 bits of the receive buffer.

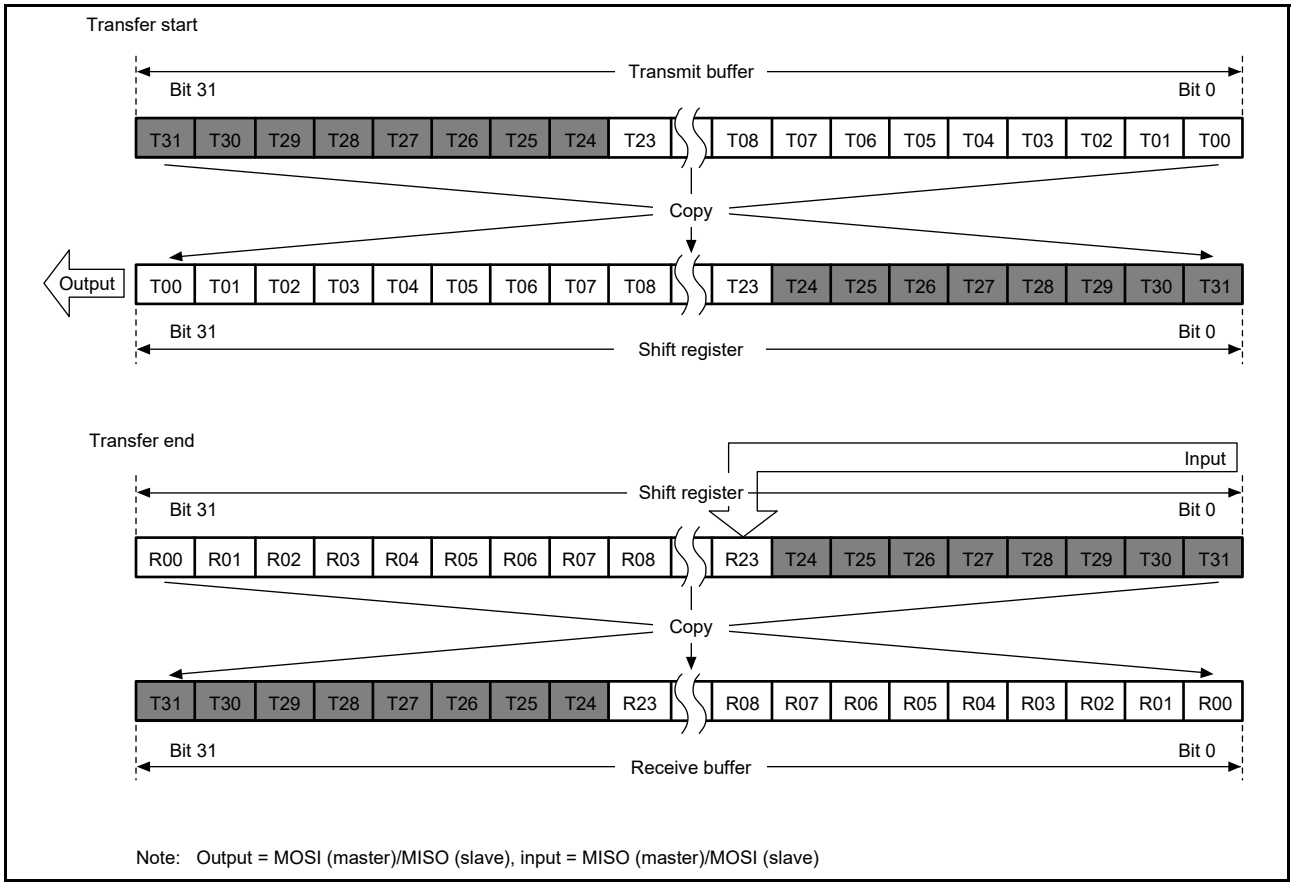


Figure 31.17 LSB-first transfer with 24-bit data and parity disabled

31.3.4.2 When parity is enabled (SPCR2.SPPE = 1)

When parity is enabled, the lowest-order bit of the data for transmission becomes a parity bit. Hardware calculates the value of the parity bit.

(1) MSB-first transfer with 32-bit data

Figure 31.18 shows operations by the SPI Data Register (SPDR) and the shift register in transfers with parity enabled, an SPI data length of 32 bits, and MSB-first selected.

In transmission, the value of the parity bit (P) is calculated from bits T31 to T01. This replaces the final bit, T00, and the whole is copied to the shift register. Data is transmitted from T31, T30, …, T01, and P.

In reception, received data is shifted in bit by bit through bit 0 of the shift register. When bits R31 to P are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. On copying of data to the shift register, the data from R31 to P is checked for parity.

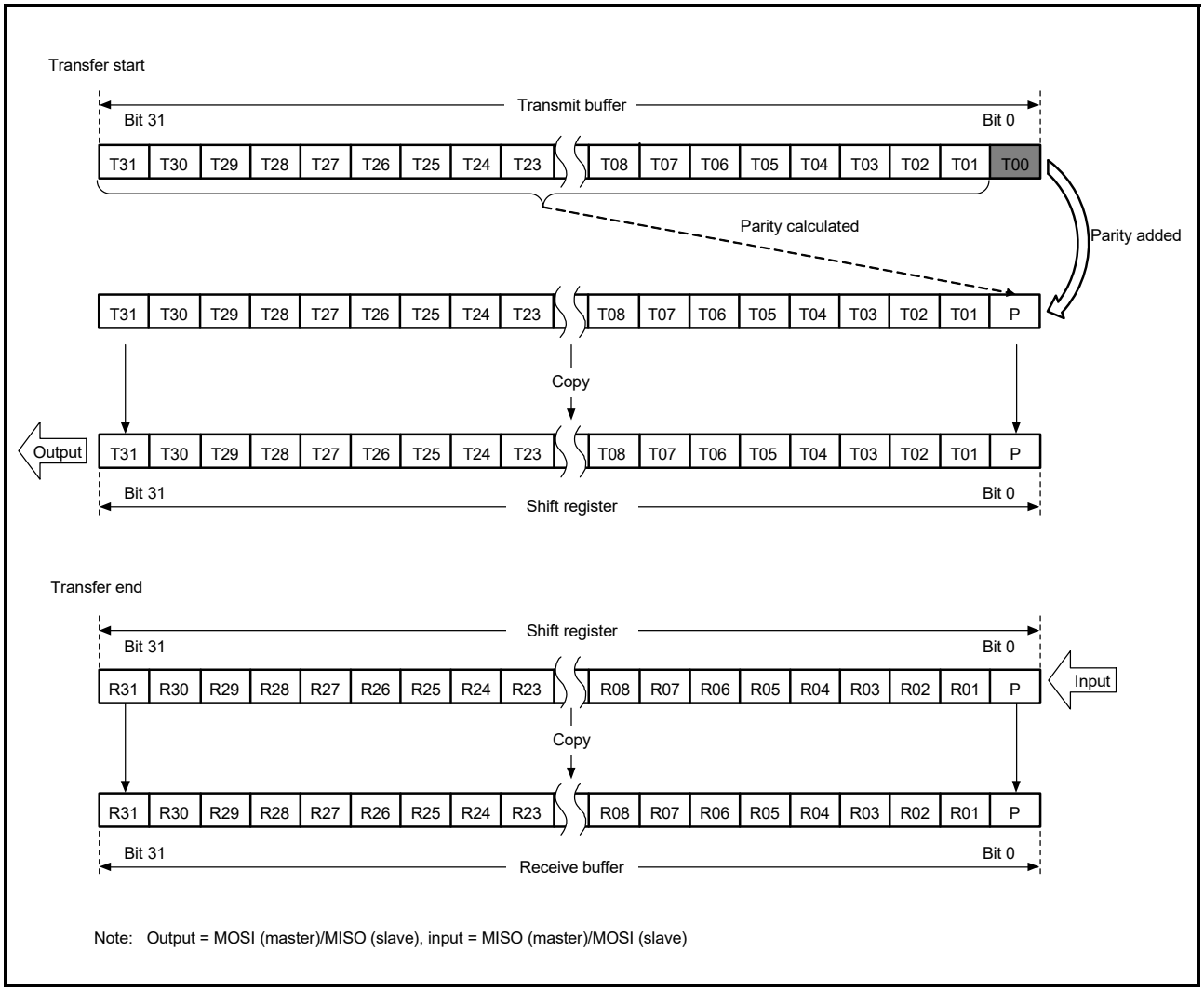


Figure 31.18 MSB-first transfer with 32-bit data and parity enabled

(2) MSB-first transfer with 24-bit data

Figure 31.19 shows operations by the SPI Data Register (SPDR) and the shift register in transfers with parity enabled, 24 bits as the SPI data length for an example that is not 32 bits, and MSB-first selected.

In transmission, the value of the parity bit (P) is calculated from bits T23 to T01. This replaces the final bit, T00, and the whole is copied to the shift register. Data is transmitted in the order T23, T22, …, T01, and P.

In reception, received data is shifted in bit by bit through bit 0 of the shift register. When bits R23 to P are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. On copying of data to the shift register, the data from R23 to P is checked for parity. The upper 8 bits of the transmit buffer are stored in the upper 8 bits of the receive buffer. Writing 0 to bits T31 to T24 during transmission results in 0 being inserted in the upper 8 bits of the receive buffer.

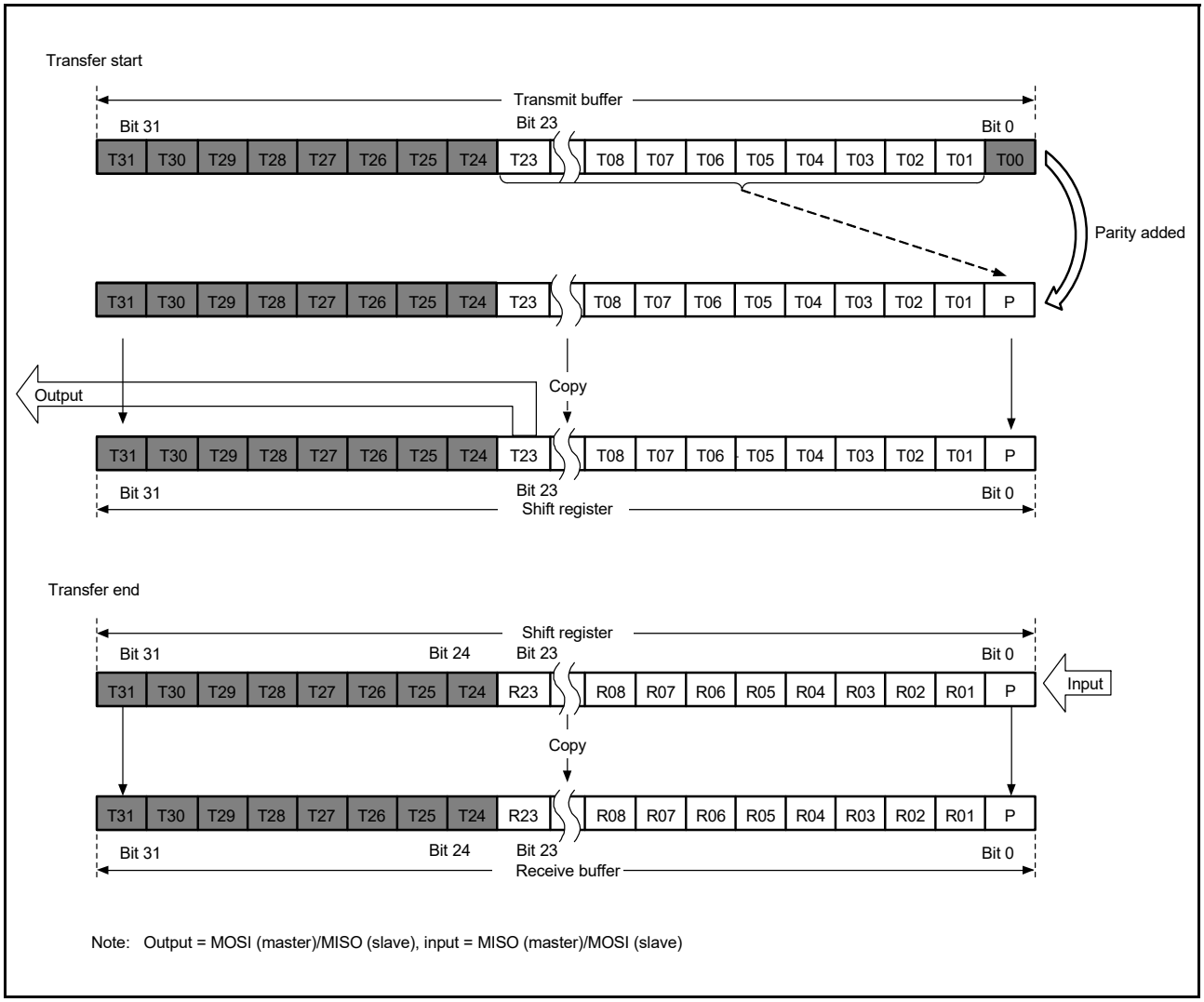


Figure 31.19 MSB-first transfer with 24-bit data and parity enabled

(3) LSB-first transfer with 32-bit data

Figure 31.20 shows operations by the SPI Data Register (SPDR) and the shift register in transfers with parity enabled, an SPI data length of 32 bits, and LSB-first selected.

In transmission, the value of the parity bit (P) is calculated from bits T30 to T00. This replaces the final bit, T31, and the whole value is copied to the shift register. Data is transmitted in the order T00, T01, …, T30, and P.

In reception, received data is shifted in bit by bit through bit 0 of the shift register. When bits R00 to P are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. On copying of data to the shift register, the data from R00 to P is checked for parity.

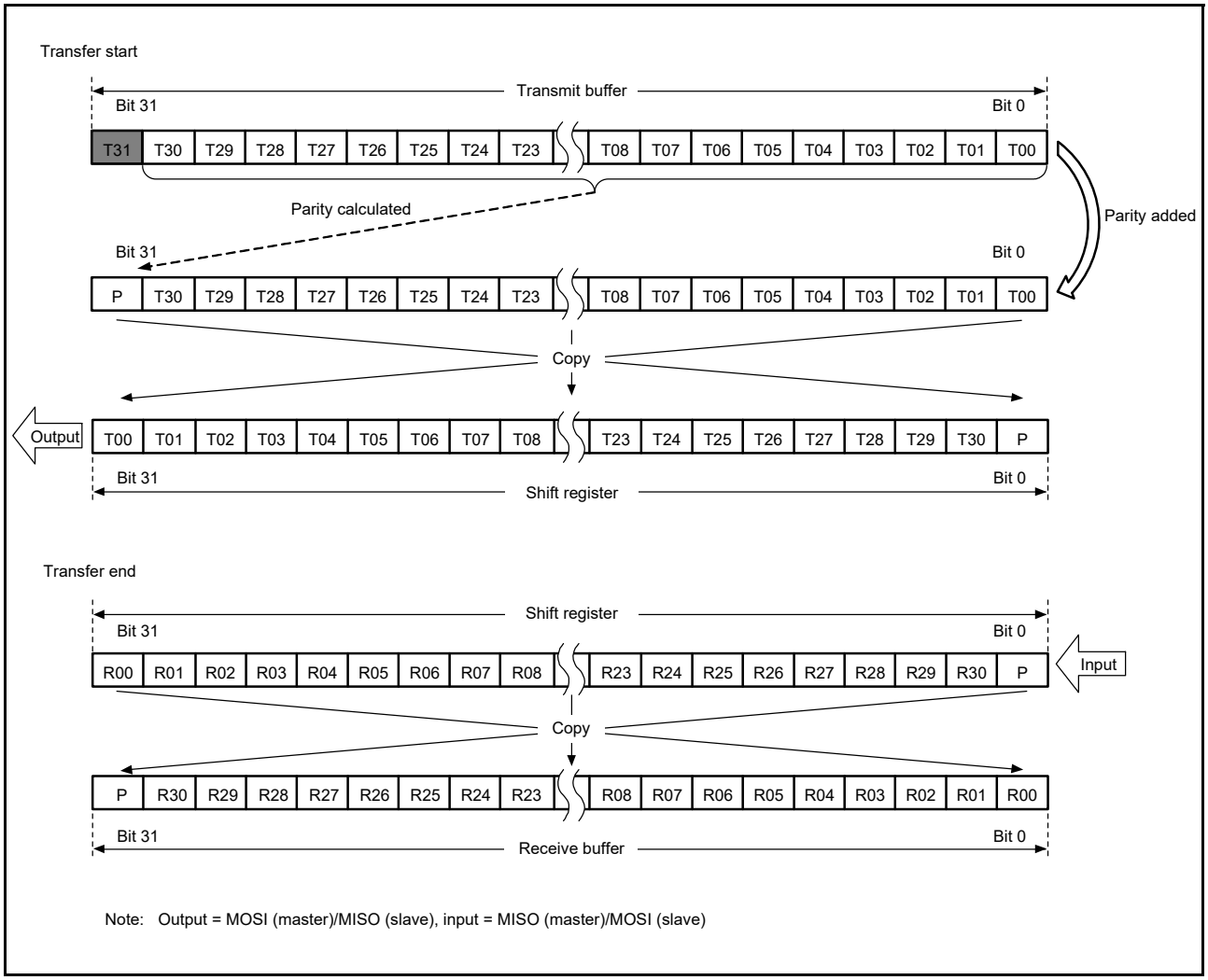


Figure 31.20 LSB-first transfer with 32-bit data and parity enabled

(4) LSB-first transfer with 24-bit data

Figure 31.21 shows operations by the SPI Data Register (SPDR) and the shift register in transfers with parity enabled, 24 bits as the SPI data length for an example that is not 32 bits, and LSB-first selected.

In transmission, the value of the parity bit (P) is calculated from bits T22 to T00. This replaces the final bit, T23, and the whole value is copied to the shift register. Data is transmitted in the order T00, T01, …, T22, and P.

In reception, received data is shifted in bit by bit through bit 8 of the shift register. When bits R00 to P are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. On copying of data to the shift register, the data from R00 to P is checked for parity. The upper 8 bits of the transmit buffer are stored in the upper 8 bits of the receive buffer. Writing 0 to bits T31 to T24 during transmission results in 0 being inserted in the upper 8 bits of the receive buffer.

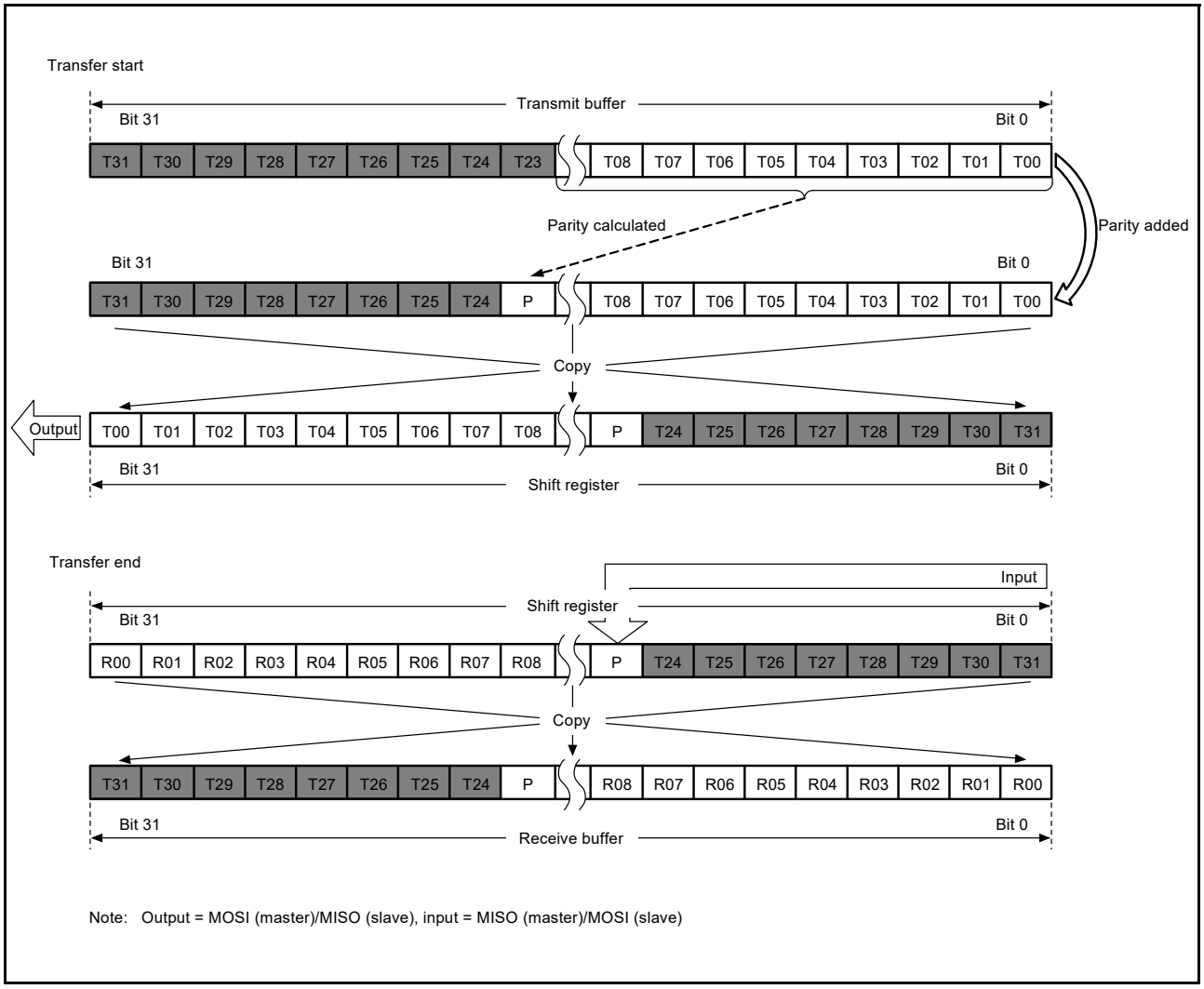


Figure 31.21 LSB-first transfer with 24-bit data and parity enabled

31.3.5 Transfer Formats

31.3.5.1 CPHA = 0

Figure 31.22 shows a sample transfer format for the serial transfer of 8-bit data when the SPCMD0.CPHA bit is 0. Do not perform clock synchronous operation (SPCR.SPMS bit is 1) when the SPI operates in slave mode (SPCR.MSTR = 0) and the CPHA bit is 0. In Figure 31.22, RSPCKn (CPOL = 0) indicates the RSPCKn signal waveform when the SPCMD0.CPOL bit is 0. RSPCKn (CPOL = 1) indicates the RSPCKn signal waveform when the CPOL bit is 1. The sampling timing represents the timing at which the SPI fetches serial transfer data into the shift register. The I/O directions of the signals depend on the SPI settings. For details, see section 31.3.2, Controlling the SPI Pins.

When the SPCMD0.CPHA bit is 0, the driving of valid data to the MOSIn and MISOn signals starts on an SSLni signal assertion. The first RSPCKn signal change that occurs after the SSLni signal assertion becomes the first transfer data fetch. After this, data is sampled on every 1 RSPCK cycle. The change timing for MOSIn and MISOn signals is 1/2 RSPCK cycle after the transfer data fetch timing. The CPOL bit setting does not affect the RSPCK signal operation timing. It only affects the signal polarity.

t1 denotes the RSPCK delay, the period from an SSLni signal assertion to RSPCKn oscillation. t2 denotes the SSL negation delay, the period from the termination of RSPCKn oscillation to an SSLni signal negation. t3 denotes the next-access delay, the period in which SSLni signal assertion is suppressed for the next transfer after the end of serial transfer. t1, t2, and t3 are controlled by a master device running on the SPI system. For a description of t1, t2, and t3 when the SPI of the MCU is in master mode, see section 31.3.10.1, Master mode operation.

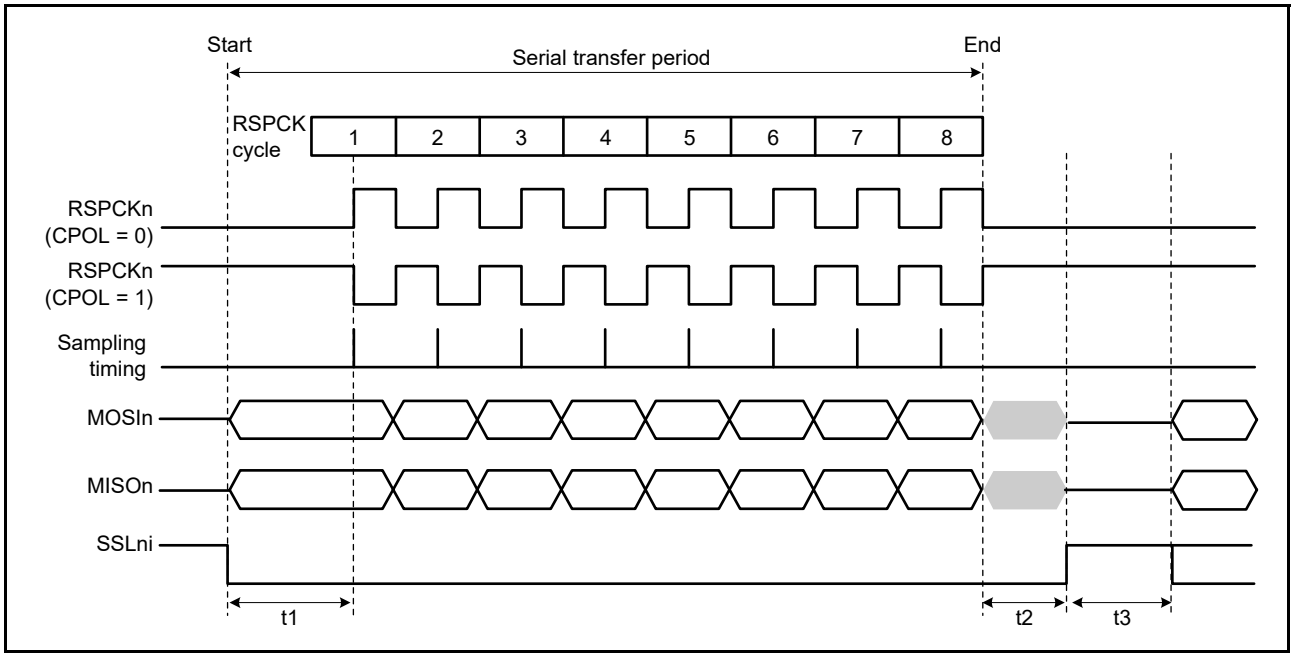


Figure 31.22 SPI transfer format when CPHA = 0

31.3.5.2 CPHA = 1

Figure 31.23 shows a sample transfer format for the serial transfer of 8-bit data when the SPCMD0.CPHA bit is 1. However, when the SPCR.SPMS bit is 1, the SSLni signals are not used, and only the three RSPCKn, MOSIn, and MISOn signals handle communications. In Figure 31.23, RSPCK (CPOL = 0) indicates the RSPCKn signal waveform when the SPCMD0.CPOL bit is 0. RSPCK (CPOL = 1) indicates the RSPCKn signal waveform when the CPOL bit is 1. The sampling timing represents the timing at which the SPI fetches serial transfer data into the shift register. The I/O directions of the signals depend on the SPI mode (master or slave). For details, see section 31.3.2, Controlling the SPI Pins.

When the SPCMD0.CPHA bit is 1, the driving of invalid data to the MISOn signal starts on an SSLni signal assertion. The output of valid data to the MOSIn and MISOn signals commences on the first RSPCKn signal change that occurs after the SSLni signal assertion. After this, data is updated every 1 RSPCK cycle. The transfer data fetch timing is 1/2 RSPCK cycle after the data update timing. The SPCMD0.CPOL bit setting does not affect the RSPCKn signal operation timing. It only affects the signal polarity.

t1, t2, and t3 are the same as those when CPHA = 0. For a description of t1, t2, and t3 when the SPI of the MCU is in master mode, see section 31.3.10.1, Master mode operation.

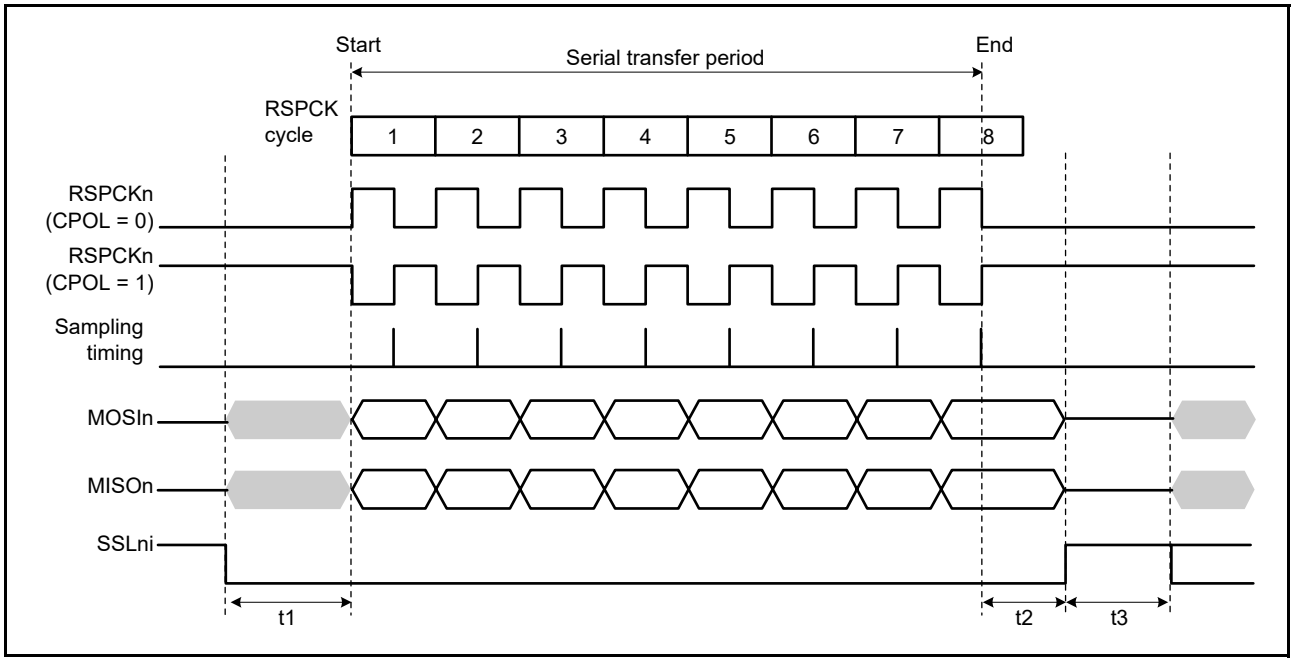


Figure 31.23 SPI transfer format when CPHA = 1

31.3.6 Data Transfer Modes

Full-duplex synchronous serial communications or transmit operations can only be selected in the communications operating mode select bit (SPCR.TXMD). The SPDR/SPDR_HA access shown in Figure 31.24 and Figure 31.25 indicate the condition of access to the SPDR/SPDR_HA register, where W denotes a write cycle.

31.3.6.1 Full-duplex synchronous serial communications (SPCR.TXMD = 0)

Figure 31.24 shows an example operation where the communications operating mode select bit (SPCR.TXMD) is set to 0. In the example, the SPI performs an 8-bit serial transfer in which the SPCMD0.CPHA bit is 1 and the SPCMD0.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, meaning the number of transferred bits.

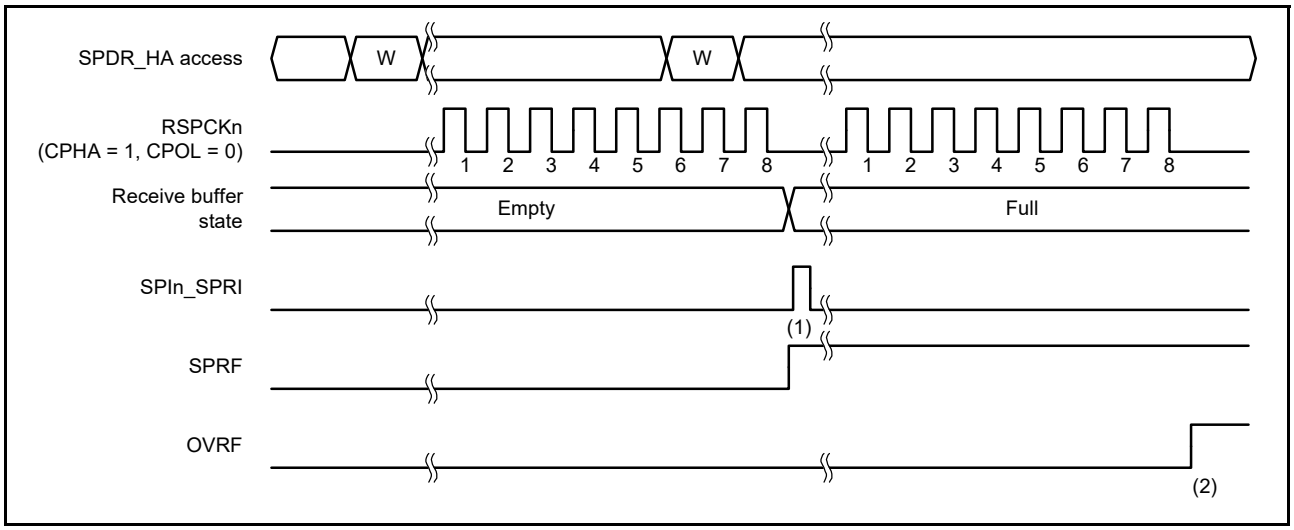


Figure 31.24 Operation example when SPCR.TXMD = 0

The operation of the flags at timings shown in (1) and (2) in the figure is as follows:

(1) When a serial transfer ends with the SPDR/SPDR_HA receive buffer empty, the SPI generates a receive buffer full interrupt request (SPIn_SPRI), the SPSR.SPRF flag is set to 1, and the received data is copied from the shift register

to the receive buffer.

(2) When a serial transfer ends with the SPDR/SPDR_HA receive buffer holding data that was received in the previous serial transfer, the SPI sets the SPSR.OVRF flag to 1 and discards the received data in the shift register.

31.3.6.2 Transmit-only operations (SPCR.TXMD = 1)

Figure 31.25 shows an example operation where the communications operating mode select bit (SPCR.TXMD) is set to 1. In the example, the SPI performs an 8-bit serial transfer in which the SPCMD0.CPHA bit is 1 and the SPCMD0.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, meaning the number of transferred bits.

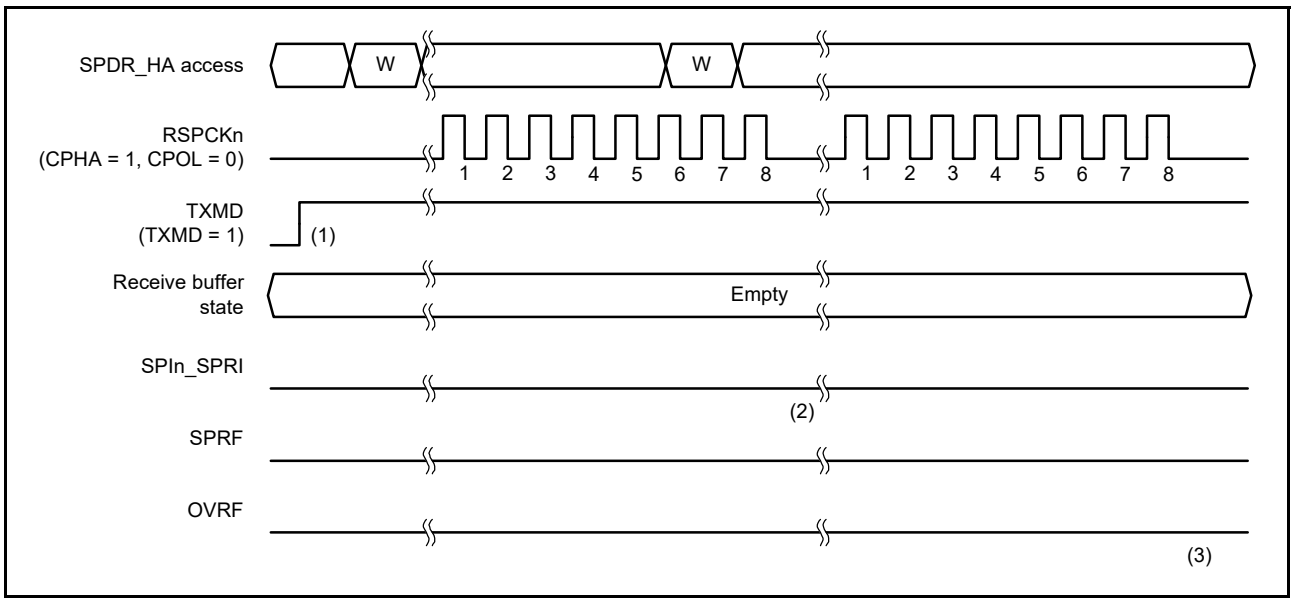


Figure 31.25 Operation example when SPCR.TXMD = 1

The operation of the flags at timings shown in (1) to (3) in the figure is as follows:

(1) Make sure there is no data left in the receive buffer (SPSR.SPRF flag is 0) and the SPSR.OVRF flag is 0 before entering the transmit-only operation mode (SPCR.TXMD = 1).

(2) When a serial transfer ends with the receive buffer of SPDR/SPDR_HA empty, if the transmit-only mode is selected (SPCR.TXMD = 1), the SPSR.SPRF flag retains the value of 0, and the SPI does not copy the data in the shift register to the receive buffer.

(3) Because the receive buffer of SPDR/SPDR_HA does not hold data that was received in the previous serial transfer, even when a serial transfer ends, the SPSR.OVRF flag retains the value of 0, and the data in the shift register is not copied to the receive buffer.

When performing transmit-only operations (SPCR.TXMD = 1), the SPI transmits but does not receive data. Therefore, the SPSR.SPRF and SPSR.OVRF flags remain 0 at timings (1) to (3).

31.3.7 Transmit Buffer Empty and Receive Buffer Full Interrupts

Figure 31.26 and Figure 31.27 show examples of operations of the transmit buffer empty interrupt (SPIn_SPTI) and the receive buffer full interrupt (SPIn_SPRI). The SPDR/SPDR_HA register accesses shown in these figures indicate the condition of access to the SPDR/SPDR_HA register, where W denotes a write cycle and R a read cycle. In Figure 31.27, the SPI performs an 8-bit serial transfer in which the SPCR.TXMD bit is 0, the SPCMD0.CPHA bit is 1, and the SPCMD0.CPOL bit is 0. In Figure 31.26, the SPI performs an 8-bit serial transfer in which the SPCR.TXMD bit is 0, the SPCMD0.CPHA bit is 0, and the SPCMD0.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, meaning the number of transferred bits.

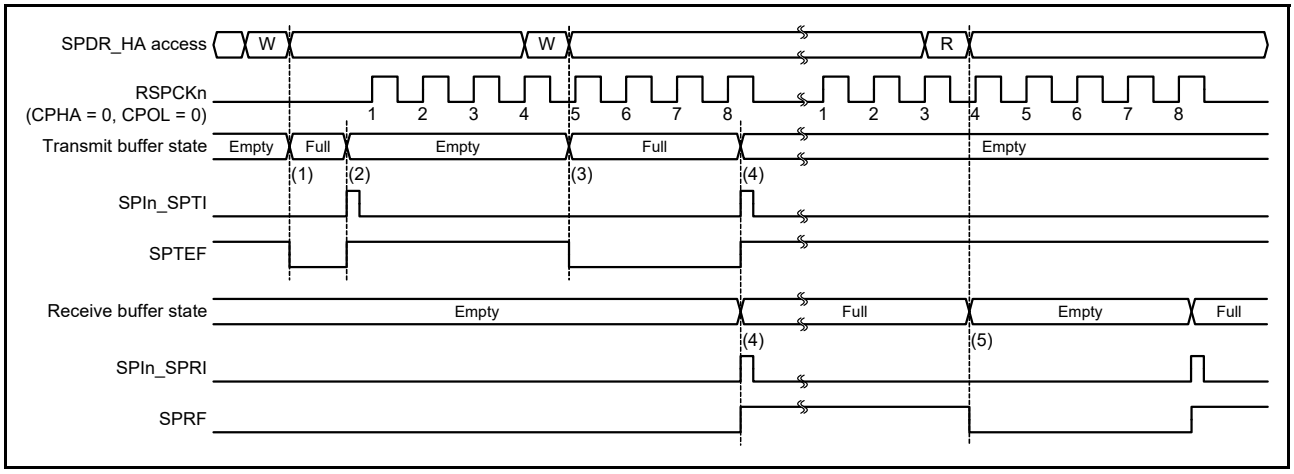


Figure 31.26 Operation example of SPIn_SPTI and SPIn_SPRI interrupts when CPHA = 0 and CPOL = 0

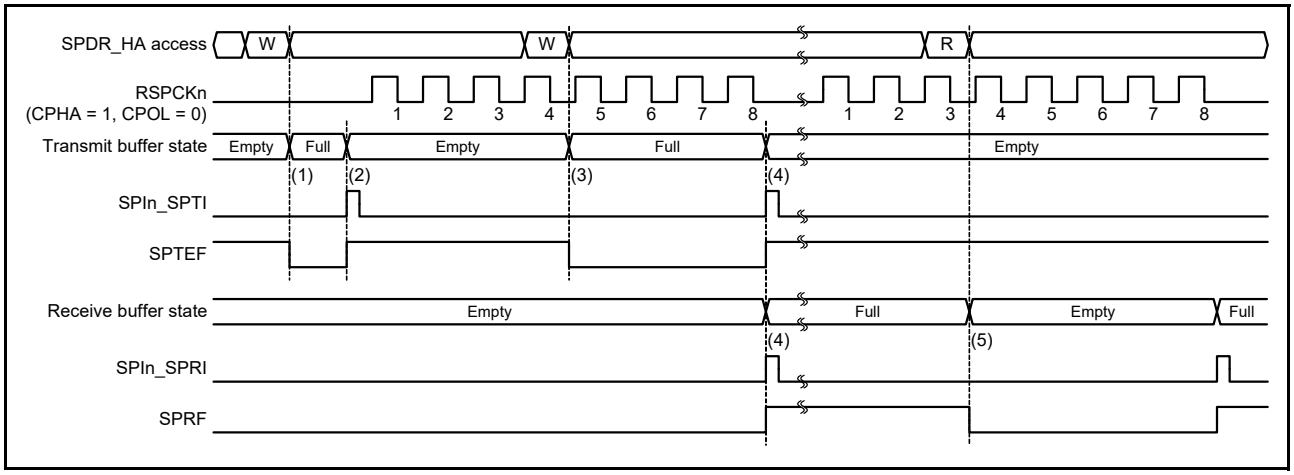


Figure 31.27 Operation example of SPIn_SPTI and SPIn_SPRI interrupts when CPHA = 1 and CPOL = 0

The operation of the SPI at timings shown in (1) to (5) in the figure is as follows:

(1) When transmit data is written to SPDR/SPDR_HA and when the transmit buffer of SPDR/SPDR_HA is empty (data for the next transfer is not set), the SPI writes data to the transmit buffer and clears the SPSR.SPTEF flag to 0.

(2) If the shift register is empty, the SPI copies the data in the transmit buffer to the shift register, generates a transmit buffer empty interrupt request (SPIn_SPTI), and sets the SPSR.SPTEF flag to 1. How a serial transfer is started depends on the mode of the SPI. For details, see section 31.3.10, SPI Operation, and section 31.3.11, Clock Synchronous Operation.

(3) When transmit data is written to SPDR/SPDR_HA either by the transmit buffer empty interrupt routine, or by the processing of transmit buffer empty using the SPTEF flag, the SPI writes data to the transmit buffer and clears the SPTEF flag to 0. Because the serially transferred data is stored in the shift register, the SPI does not copy the data in the transmit buffer to the shift register.

(4) When the serial transfer ends with the receive buffer of SPDR/SPDR_HA empty, the SPI copies the receive data in the shift register to the receive buffer, generates a receive buffer full interrupt request (SPIn_SPRI), and sets the SPRF flag to 1. Because the shift register is empty on completion of serial transfer, when the transmit buffer is full before the serial transfer ends, the SPI sets the SPTEF flag to 1 and copies the data in the transmit buffer to the shift register. Even when received data is not copied from the shift register to the receive buffer in an overrun error status, on completion of the serial transfer, the SPI determines that the shift register is empty, so data transfer from the transmit buffer to the shift register is enabled.

(5) When SPDR/SPDR_HA is read either by the receive buffer full interrupt routine or processing of the receive buffer full using the SPRF flag, the receive data can be read.

If SPDR/SPDR_HA is written to when the transmit buffer holds untransmitted data (the SPTEF flag is 0), the SPI does not update the data in the transmit buffer. When writing to SPDR/SPDR_HA, make sure to use a transmit buffer empty interrupt request or to process a transmit buffer empty interrupt using the SPTEF flag. To use a transmit buffer empty interrupt, set the SPTIE bit in SPCR to 1. If the SPI function is disabled (the SPCR.SPE bit is 0), set the SPTIE bit to 0.

When serial transfer ends with the receive buffer full (the SPRF flag is 1), the SPI does not copy data from the shift register to the receive buffer, and it detects an overrun error (see section 31.3.8, Error Detection). To prevent a receive data overrun error, read the received data using a receive buffer full interrupt request before the next serial transfer ends. To use an SPI receive buffer full interrupt, set the SPCR.SPRIE bit to 1.

Transmission and reception interrupts or the associated IELSRm.IR flags in the ICU, where m is the interrupt vector number, can be used to confirm the states of the transmit and receive buffers. Similarly, the SPTEF and SPRF flags can be used to confirm the states of the transmit and receive buffers. See section 12, Interrupt Controller Unit (ICU), for the interrupt vector numbers.

31.3.8 Error Detection

In normal SPI serial transfer, data written to the transmit buffer of SPDR/SPDR_HA is transmitted, and received data can be read from the receive buffer of SPDR/SPDR_HA. If access is made to SPDR/SPDR_HA, an abnormal transfer might occur, depending on the status of the transmit or receive buffer, or the status of the SPI at the beginning or end of serial transfer.

If a non-normal transfer occurs, the SPI detects the event as an underrun error, overrun error, parity error, or mode fault error. Table 31.7 lists the relationship between non-normal transfer operations and the SPI error detection function.

Table 31.7 Relationship between non-normal transfer operations and SPI error detection function

	Occurrence condition	SPI operation	Error detection
1	SPDR/SPDR_HA is written when the transmit buffer is full	• The contents of the transmit buffer are kept • Write data is missing.	None
2	SPDR/SPDR_HA is read when the receive buffer is empty	The contents of the receive buffer and previously received data are output	None
3	Serial transfer is started in slave mode when the SPI is not able to transmit data	• Serial transfer is suspended • Transmit or receive data is missing • Driving of the MISOA output signal is stopped • SPI function is disabled.	Underrun error
4	Serial transfer terminates when the receive buffer is full	• The contents of the receive buffer are kept • Missing receive data.	Overrun error
5	An incorrect parity bit is received during full-duplex synchronous serial communications with the parity function enabled	The parity error flag is asserted	Parity error
6	The SSLn0 input signal is asserted when the serial transfer is idle in multi-master mode	• Driving of the RSPCKn, MOSIn, and SSLn1 to SSLn3 output signals is stopped • SPI function is disabled.	Mode fault error
7	The SSLn0 input signal is asserted during serial transfer in multi-master mode	• Serial transfer is suspended • Transmit or receive data is missing • Driving of the RSPCKn, MOSIn, and SSLn1 to SSLn3 output signals is stopped • SPI function is disabled.	Mode fault error
8	The SSLn0 input signal is negated during serial transfer in slave mode	• Serial transfer is suspended • Transmit or receive data is missing • Driving of the MISOn output signal is stopped • SPI function is disabled.	Mode fault error

In operation 1 described in Table 31.7, the SPI does not detect an error. To prevent data omission during writes to SPDR/SPDR_HA, write operations must be executed using a transmit buffer empty interrupt request (when SPSR.SPTEF is 1). Similarly, the SPI does not detect an error in operation 2. To prevent extraneous data from being read, SPDR/SPDR_HA read operations must be executed using an SPI receive buffer full interrupt request (when SPSR.SPRF is 1).

For information on:

- Underrun errors, indicated in operation 3, see section 31.3.8.4, Underrun errors

- Overrun errors, indicated in operation 4, see section 31.3.8.1, Overrun errors
- Parity errors, indicated in operation 5, see section 31.3.8.2, Parity errors
- Mode fault errors indicated in operations 6 to 8, see section 31.3.8.3, Mode fault errors
- Transmit and receive interrupts, see section 31.3.7, Transmit Buffer Empty and Receive Buffer Full Interrupts.

31.3.8.1 Overrun errors

If a serial transfer ends when the receive buffer of SPDR/SPDR_HA is full, the SPI detects an overrun error and sets the SPSR.OVRF flag to 1. When the OVRF flag is 1, the SPI does not copy data from the shift register to the receive buffer, so the data before the error occurrence is saved in the receive buffer. To set the OVRF flag to 0, write 0 to it after the CPU reads SPSR with the OVRF flag set to 1.

Figure 31.28 shows an example operation of the OVRF and SPRF flags. The SPSR and SPDR/SPDR_HA accesses shown in the figure indicate the condition of access to SPSR and SPDR/SPDR_HA, respectively, where W denotes a write cycle, and R a read cycle. In the example, the SPI performs an 8-bit serial transfer in which the SPCMD0.CPHA bit is 1 and the SPCMD0.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, meaning the number of transferred bits.

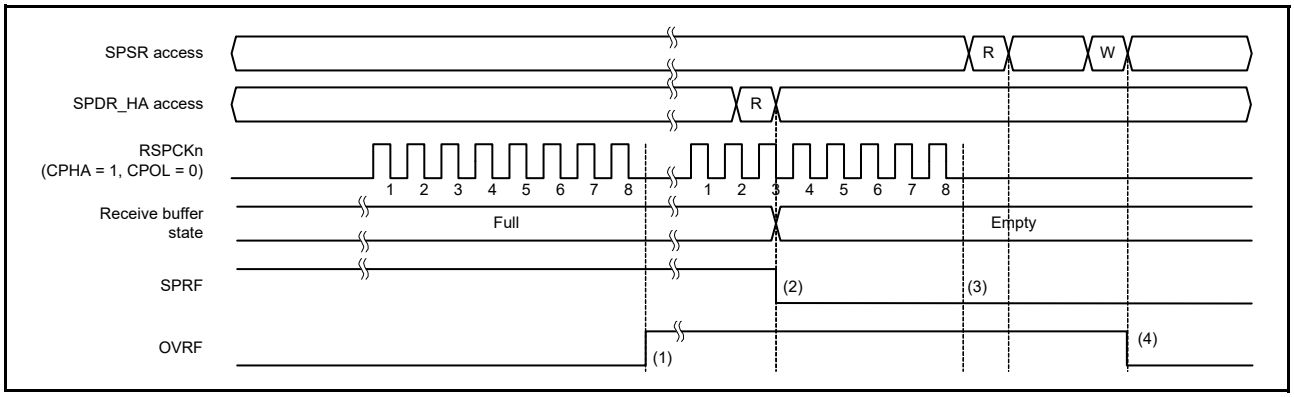


Figure 31.28 Operation example of OVRF and SPRF flags

The operation of the flags at timings shown in (1) to (4) in the figure is as follows:

(1) If a serial transfer terminates with the SPRF flag set to 1 (receive buffer full), the SPI detects an overrun error, and sets the OVRF flag to 1. The SPI does not copy the data in the shift register to the receive buffer. Even when the SPPE bit is 1, parity errors are not detected.

(2) When SPDR/SPDR_HA is read, the SPI outputs the data in the receive buffer. The SPRF flag is then set to 0. The receive buffer becoming empty does not set the OVRF flag to 0.

(3) If the serial transfer ends with the OVRF flag set to 1 (overrun error occurred), the SPI does not copy data in the shift register to the receive buffer (the SPRF flag does not set to 1). A receive buffer full interrupt is not generated. Even when the SPPE bit is 1, parity errors are not detected. In an overrun error state when the SPI does not copy the received data from the shift register to the receive buffer, on termination of the serial transfer, the SPI determines that the shift register is empty. This enables data transfer from the transmit buffer to the shift register.

(4) If 0 is written to the OVRF flag after SPSR is read when the OVRF flag is 1, the OVRF flag is set to 0.

The application can check for an overrun either by reading SPSR or by using an SPI error interrupt and reading SPSR. When executing a serial transfer, make sure that overrun errors are detected early, for instance by reading SPSR immediately after SPDR/SPDR_HA is read. If an overrun error occurs and the OVRF flag is set to 1, normal reception cannot be performed until OVRF is set to 0.

When the RSPCK auto-stop function is enabled in master mode, an overrun error does not occur. Figure 31.29 and Figure 31.30 show the clock stop waveform when a serial transfer continues while the receive buffer is full in master mode.

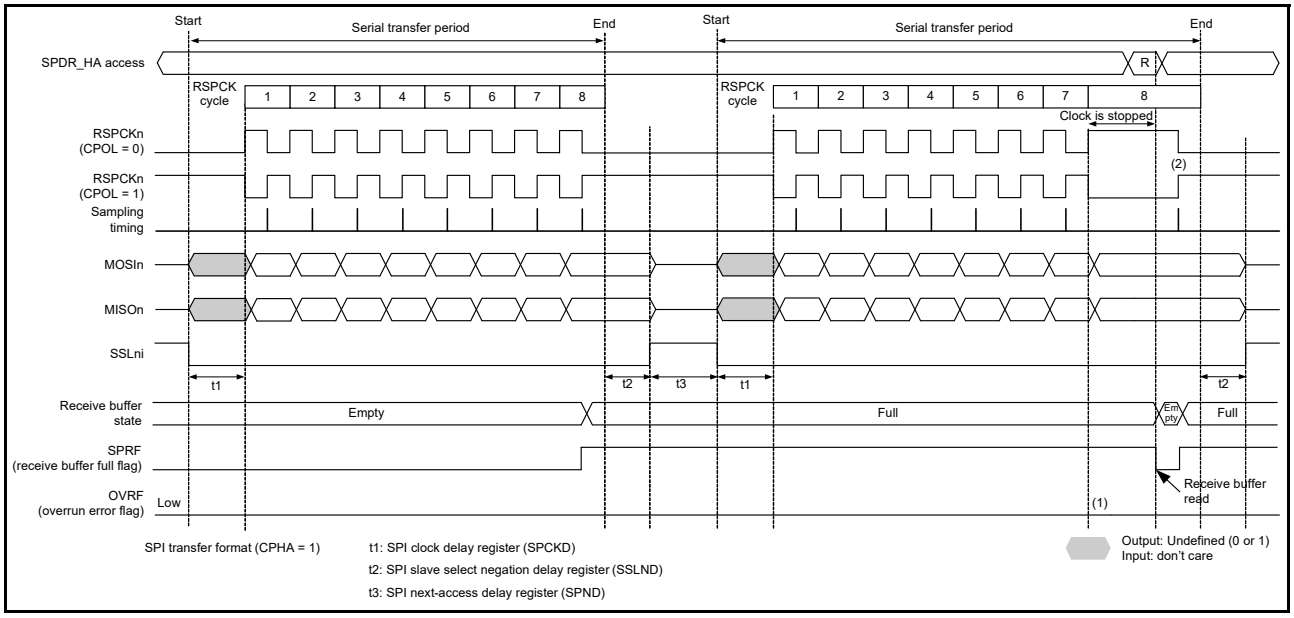


Figure 31.29 Clock stop waveform when serial transfer continues while receive buffer is full in master mode (CPHA = 1)

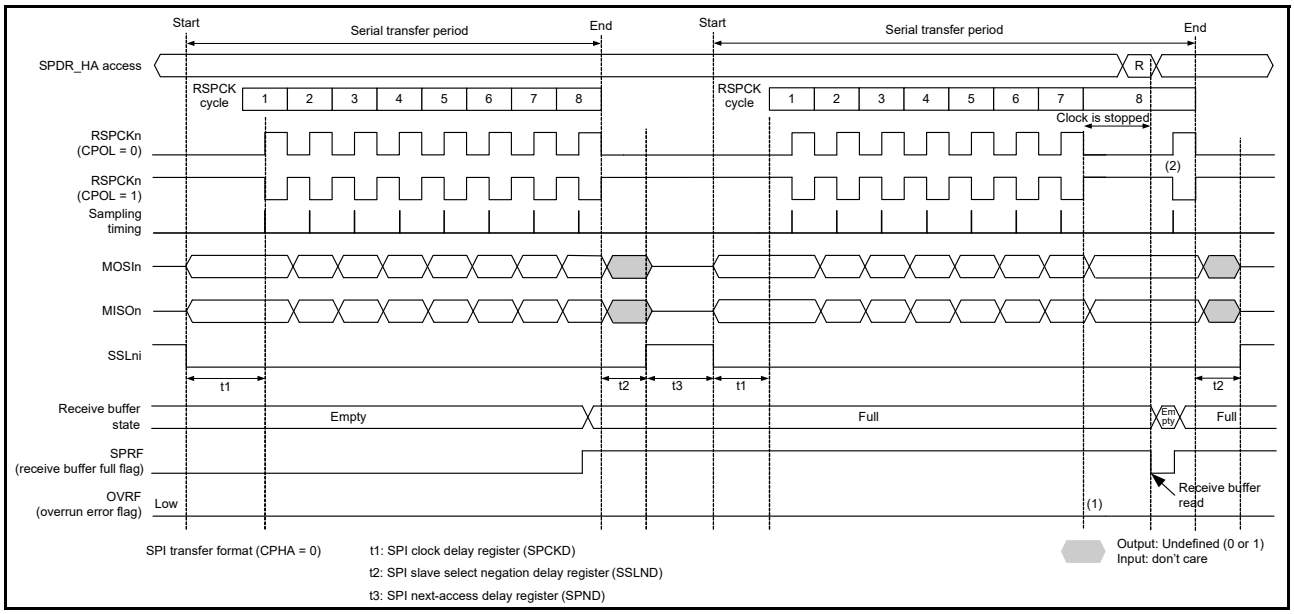


Figure 31.30 Clock stop waveform when serial transfer continues while receive buffer is full in master mode (CPHA = 0)

The operation of the flags at timings shown in (1) and (2) in the figure is as follows:

(1) When the receive buffer is full, an overrun error does not occur because the RSPCK clock is stopped.

(2) If SPDR/SPDR_HA is read while the clock is stopped, data in the receive buffer can be read. The RSPCK clock restarts after reading the receive buffer (after SPSR.SPRF is set to 0).

31.3.8.2 Parity errors

When full-duplex synchronous serial communications is performed with the SPCR.TXMD bit set to 0 and the SPCR2.SPPE bit set to 1, the SPI checks for parity errors when serial transfer ends. On detecting a parity error in the received data, the SPI sets the SPSR.PERF flag to 1. Because the SPI does not copy data in the shift register to the receive buffer when the SPSR.OVRF flag is set to 1, parity error detection is not performed for the received data. To set the PERF flag to 0, write 0 to the PERF flag after the SPSR register is read with the PERF flag set to 1.

Figure 31.31 shows an example operation of the OVRF and PERF flags. The SPSR access shown in Figure 31.31 indicates the condition of access to the SPSR register, where W denotes a write cycle, and R a read cycle. In the example of Figure 31.31, full-duplex synchronous serial communications is performed while the SPCR.TXMD bit is 0 and the SPCR2.SPPE bit is 1. The SPI performs an 8-bit serial transfer in which the SPCMD0.CPHA bit is 1 and the SPCMD0.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, meaning the number of transferred bits.

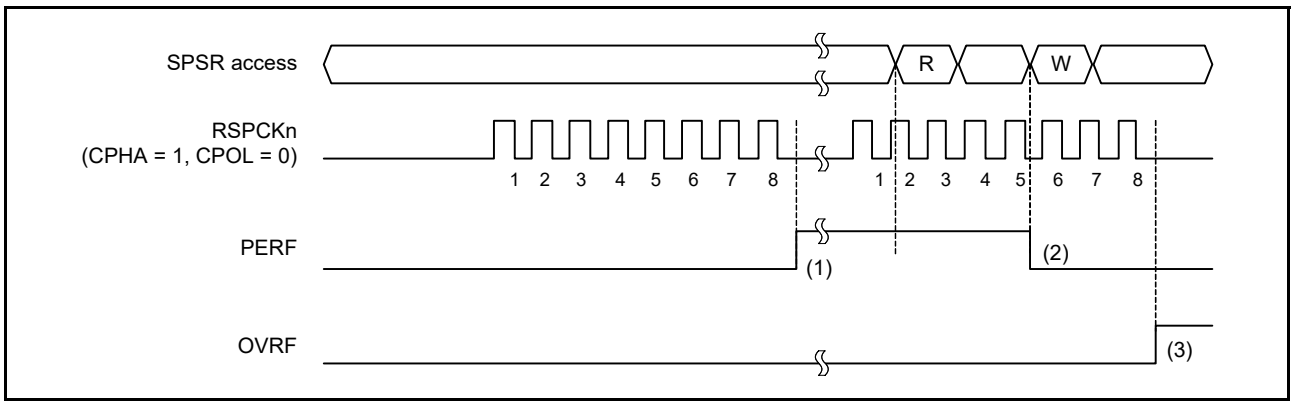


Figure 31.31 Operation example of PERF flag

The operation of the flags at timings shown in (1) to (3) in the figure is as follows:

(1) If a serial transfer terminates with the SPI not detecting an overrun error, the SPI copies the data in the shift register to the receive buffer. The SPI checks the received data at this timing and sets the PERF flag to 1 if a parity error is detected.

(2) If 0 is written to the PERF flag after the SPSR register is read when the PERF flag is 1, the PERF flag is set to 0.

(3) When the SPI detects an overrun error and serial transfer is terminated, the data in the shift register is not copied to the receive buffer. The SPI does not perform parity error detection at this time.

The application can check for a parity error by reading SPSR or by using an SPI error interrupt and reading SPSR. When executing a serial transfer, make sure that parity errors are detected early, for instance by reading SPSR.

31.3.8.3 Mode fault errors

The SPI operates in multi-master mode when the SPCR.MSTR bit is 1, the SPCR.SPMS bit is 0, and the SPCR.MODFEN bit is 1. If the active level is input for the SSLn0 input signal of the SPI in multi-master mode, the SPI detects a mode fault error regardless of the status of the serial transfer, and sets the SPSR.MODF flag to 1. The active level of the SSLn0 signal is determined by the SSLP.SSL0P bit.

When the MSTR bit is 0, the SPI operates in slave mode. The SPI detects a mode fault error if the MODFEN bit of the SPI in slave mode is 1, and the SPMS bit is 0, and if the SSLn0 input signal is negated during the serial transfer period (from the time the driving of valid data is started to the time the final valid data is fetched).

On detecting a mode fault error, the SPI stops driving the output signals and clears the SPCR.SPE bit to 0 (see section 31.3.9, Initializing SPI). For multi-master configuration, detection of a mode fault error is used to stop the driving of output signals and the SPI function, which allows the master to be released.

Mode fault errors can be checked by reading SPSR or by using an SPI error interrupt and reading SPSR. Detecting mode-fault errors without using the SPI error interrupt requires polling of SPSR.

When the MODF flag is 1, writing 1 to the SPE bit is ignored by the SPI. To enable the SPI function after the detection of a mode fault error, the MODF flag must be set to 0.

31.3.8.4 Underrun errors

When a serial transfer begins with the SPCR.MSTR bit set to 0 (slave mode), the SPCR.SPE bit is set to 1, and the transmission data not prepared, the SPI detects an underrun error. The SPI then sets SPSR.MODF flag and SPSR.UDRF flag to 1. On detecting an underrun error, the SPI stops the driving of output signals and clears the SPCR.SPE bit to 0 (see section 31.3.9, Initializing SPI).

Underrun errors can be checked by reading SPSR or by using an SPI error interrupt and reading SPSR. Detecting underrun errors without using the SPI error interrupt requires polling of SPSR.

When the MODF flag is 1, writing 1 to the SPE bit is ignored by the SPI. To enable the SPI function after the detection of an underrun error, the MODF flag must be set to 0.

31.3.9 Initializing SPI

If 0 is written to the SPCR.SPE bit or the SPI sets the SPE bit to 0 because it detected a mode fault error or an underrun error, the SPI disables the SPI function and initializes some of the module functions. When a system reset occurs, the SPI initializes all of the module functions. The following describes initialization by clearing of the SPCR.SPE bit and by a system reset.

31.3.9.1 Initialization by clearing the SPE bit

When the SPCR.SPE bit is set to 0, the SPI performs the following initialization:

- Suspends any serial transfer that is being executed
- Stops the driving of output signals (Hi-Z) in slave mode
- Initializes the internal state of the SPI
- Initializes the transmit buffer of the SPI (SPSR.SPTEF flag is set to 1).

Initialization by clearing of the SPE bit does not initialize the control bits of the SPI. For this reason, the SPI can be started in the same transfer mode in use before initialization when the SPE bit is set to 1 again.

The SPSR.SPRF, SPSR.OVRF, SPSR.MODF, SPSR.PERF, and SPSR.UDRF flags are not initialized. Therefore, even after the SPI is initialized, data from the receive buffer can be read to check the error status during an SPI transfer.

The transmit buffer is initialized to an empty state (SPSR.SPTEF flag is set to 1). Therefore, if the SPCR.SPTIE bit is set to 1 after SPI initialization, a transmit buffer empty interrupt is generated. To disable any transmit buffer empty interrupts when the SPI is initialized, write 0 to the SPTIE bit at the same time as writing 0 to the SPE bit.

31.3.9.2 Initialization by system reset

A system reset completely initializes the SPI by initializing all bits that control the SPI, the status bits, and the data registers, in addition to the actions described in section 31.3.9.1, Initialization by clearing the SPE bit.

31.3.10 SPI Operation

31.3.10.1 Master mode operation

The only difference between single-master and multi-master mode operation is the use of mode fault error detection (see section 31.3.8, Error Detection). In single-master mode, the SPI does not detect mode fault errors, while in multi-master mode, it does. This section explains operations that are common to both modes.

(1) Starting serial transfer

The SPI updates the data in the transmit buffer (SPTX) when data is written to the SPI Data Register (SPDR/SPDR_HA) with the SPI transmit buffer being empty (data for the next transfer is not set) (SPSR.SPTEF flag is 1). When the shift register is empty, the SPI copies data from the transmit buffer to the shift register and starts serial transfer. On copying transmit data to the shift register, the SPI changes the status of the shift register to full, and on termination of serial transfer, it changes the status of the shift register to empty. The status of the shift register cannot be referenced.

For details on the SPI transfer format, see section 31.3.5, Transfer Formats. The polarity of the SSLni output pins depends on the SSLP register settings.

(2) Terminating serial transfer

Regardless of the SPCMD0.CPHA bit setting, the SPI terminates a serial transfer after transmitting an RSPCKn edge associated with the final sampling timing. If free space is available in the receive buffer (SPRX) (SPSR.SPRF flag is 0), on termination of serial transfer, the SPI copies data from the shift register to the receive buffer of the SPDR/SPDR_HA register.

The final sampling timing varies depending on the bit length of the transfer data. In master mode, the SPI data length depends on the SPCMD0.SPB[3:0] bit setting. The polarity of the SSLni output pin depends on the SSLP register settings.

For details on the SPI transfer format, see section 31.3.5, Transfer Formats.

(3) RSPCK delay (t1)

The RSPCK delay in master mode depends on the SPCMD0.SCKDEN bit setting and the SPCKD register setting. The SPI determines an RSPCK delay during serial transfer using the SPCMD0.SCKDEN bit and SPCKD, as shown in Table 31.8. For a definition of RSPCK delay, see section 31.3.5, Transfer Formats.

Table 31.8 Relationship between the SCKDEN bit, SPCKD, and RSPCK delays

SPCMD0.SCKDEN bit	SPCKD.SCKDL[2:0] bits	RSPCK delay
0	000b to 111b	1 RSPCK
1	000b	1 RSPCK
	001b	2 RSPCK
	010b	3 RSPCK
	011b	4 RSPCK
	100b	5 RSPCK
	101b	6 RSPCK
	110b	7 RSPCK
	111b	8 RSPCK

(4) SSL negation delay (t2)

The SSL negation delay value in master mode depends on the SPCMD0.SLNDEN bit setting and the SSLND register setting. The SPI determines the SSL negation delay during serial transfer using the SPCMD0.SLNDEN bit and SSLND, as shown in Table 31.9. For a definition of SSL negation delay, see section 31.3.5, Transfer Formats.

Table 31.9 Relationship between the SLNDEN bit, SSLND, and SSL degation delays

SPCMD0.SLNDEN bit	SSLND.SLNDL[2:0] bits	SSL negation delay
0	000b to 111b	1 RSPCK
1	000b	1 RSPCK
	001b	2 RSPCK
	010b	3 RSPCK
	011b	4 RSPCK
	100b	5 RSPCK
	101b	6 RSPCK
	110b	7 RSPCK
	111b	8 RSPCK

(5) Next-access delay (t3)

The next-access delay in master mode depends on the SPCMD0.SPNDEN bit setting and the SPND register setting. The SPI determines the next-access delay during serial transfer using the SPCMD0.SPNDEN bit and SPND, as shown in Table 31.10. For a definition of next-access delay, see section 31.3.5, Transfer Formats.

Table 31.10 Relationship between the SPNDEN bit, SPND, and next-access delays

SPCMD0.SPNDEN bit	SPND.SPNDL[2:0] bits	Next-access delay
0	000b to 111b	1 RSPCK + 2 PCLKB
1	000b	1 RSPCK + 2 PCLKB
	001b	2 RSPCK + 2 PCLKB
	010b	3 RSPCK + 2 PCLKB
	011b	4 RSPCK + 2 PCLKB
	100b	5 RSPCK + 2 PCLKB
	101b	6 RSPCK + 2 PCLKB
	110b	7 RSPCK + 2 PCLKB
	111b	8 RSPCK + 2 PCLKB

(6) Initialization flow

The flow in Figure 31.32 provides an example of SPI initialization when the SPI is in master mode. For information on setting up the Interrupt Controller Unit, DTC, and I/O Ports, see the individual block descriptions.

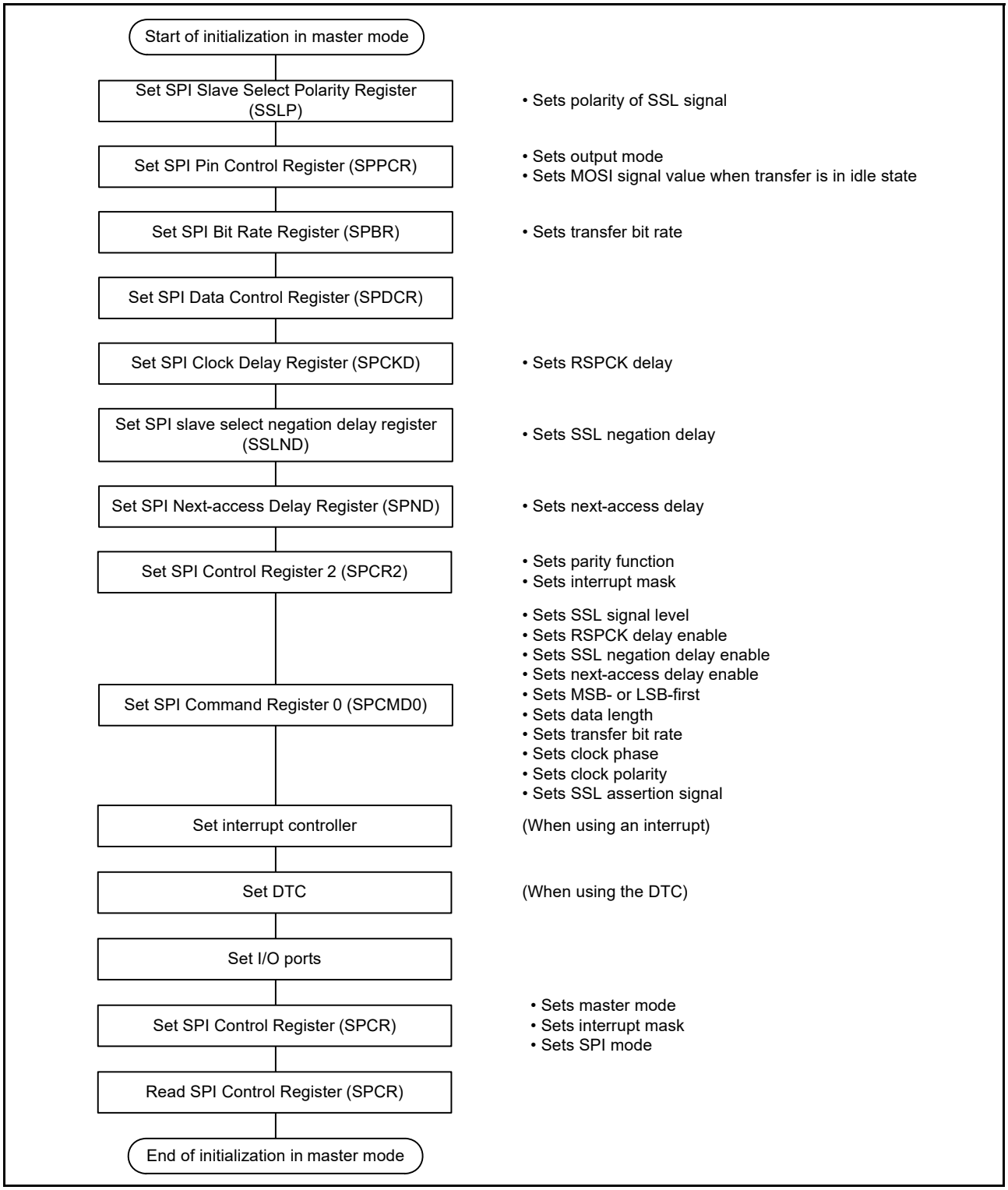


Figure 31.32 Example of initialization flow in master mode for SPI operation

(7) Software processing flow

Figure 31.33 to Figure 31.35 show example flows of software processing.

(a) Transmit processing flow

When transmitting data and when the idle interrupt (SPIn_SPII) is enabled, the CPU is notified of the completion of data transmission after the last data write for transmission.

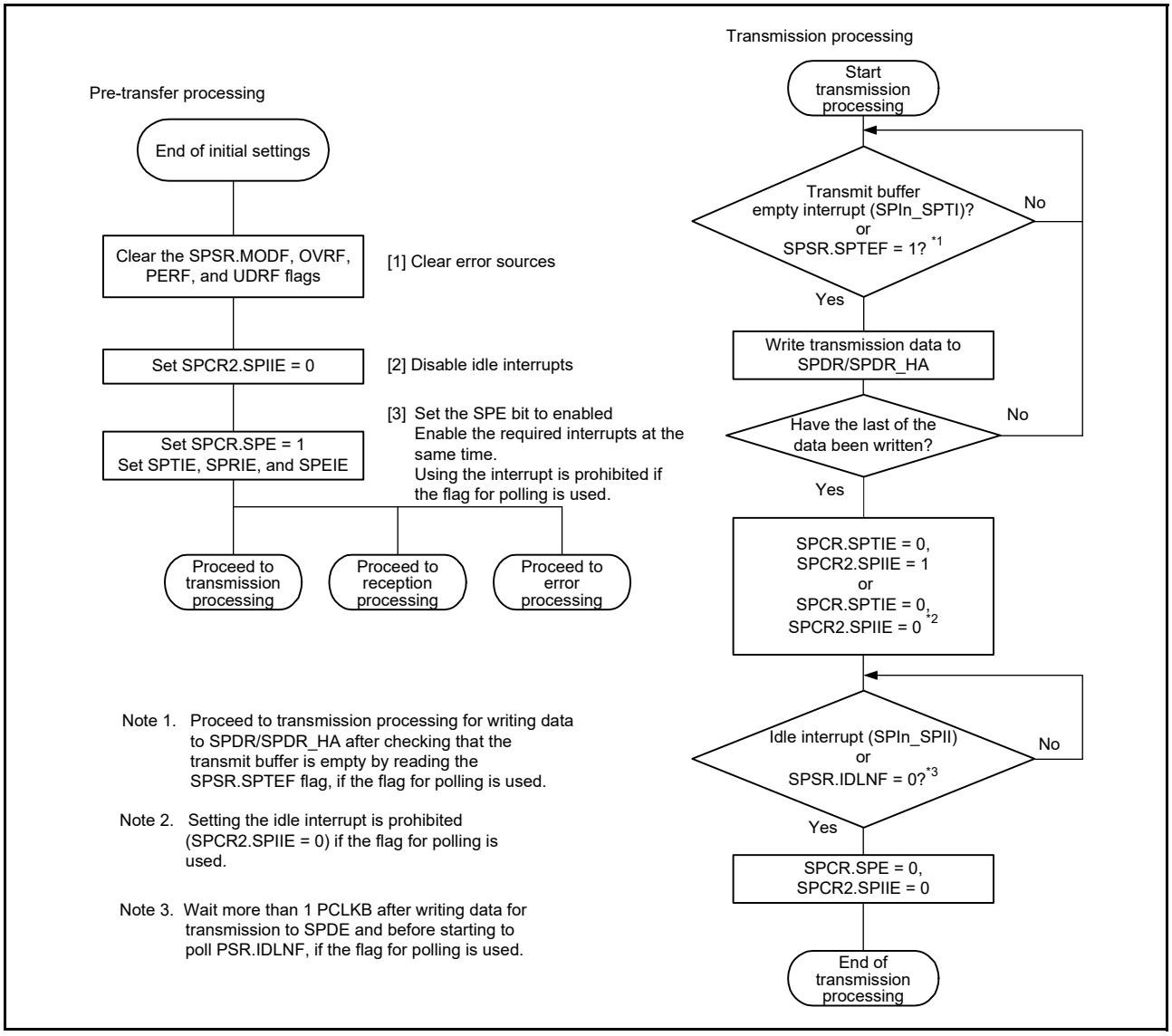


Figure 31.33 Transmission flow in master mode

(b) Receive processing flow

The SPI does not handle receive-only operations, therefore processing for transmission is required.

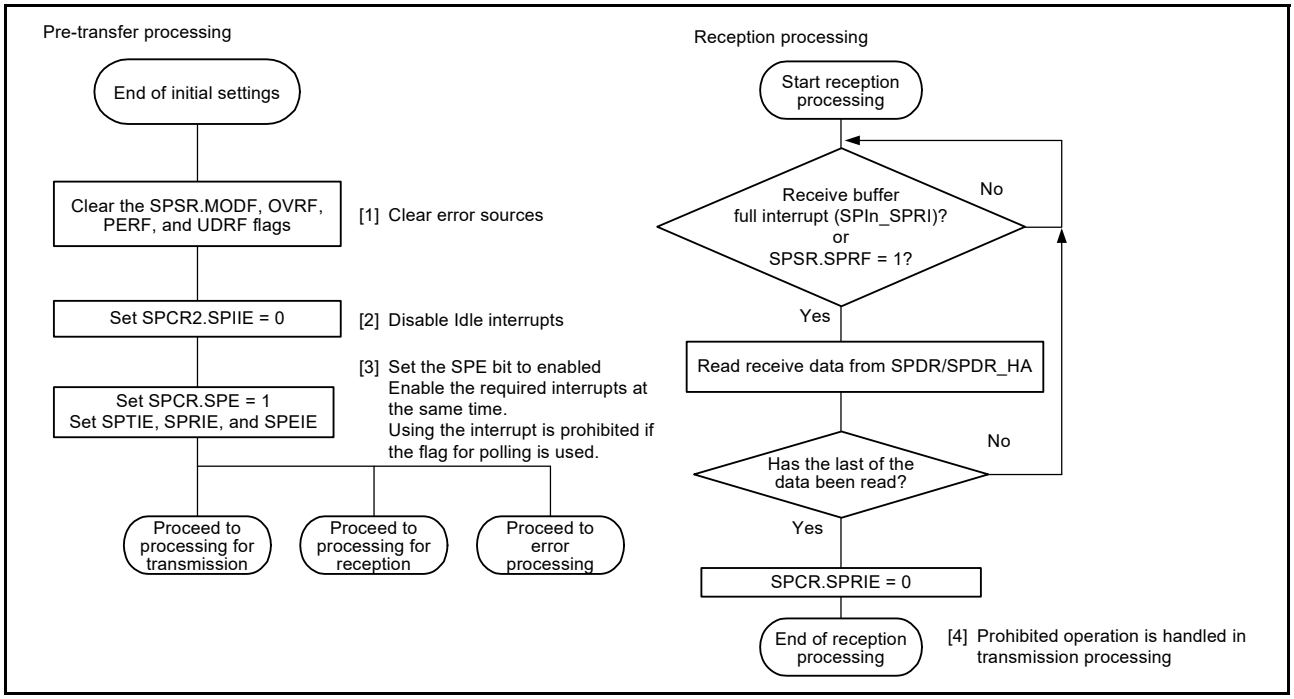


Figure 31.34 Reception flow in master mode

(c) Error processing flow

The SPI detects mode fault errors, underrun errors, overrun errors, and parity errors. When a mode fault error is generated, the SPCR.SPE bit is automatically cleared, stopping operations for transmission and reception. For errors from other sources, the SPCR.SPE bit is not cleared and operations for transmission and reception continue. Renesas recommends clearing the SPCR.SPE bit to stop operations for errors other than mode fault errors.

When an error is detected by using interrupt, clear the ICU.IELSRm.IR flag in the error processing routine. If this is not done, the ICU.IELSRm.IR flag might continue to indicate the transmit buffer empty or the receive buffer full interrupt request. If the SPRI interrupt request is indicated, read the receive buffer and initialize the sequencer in the SPI.

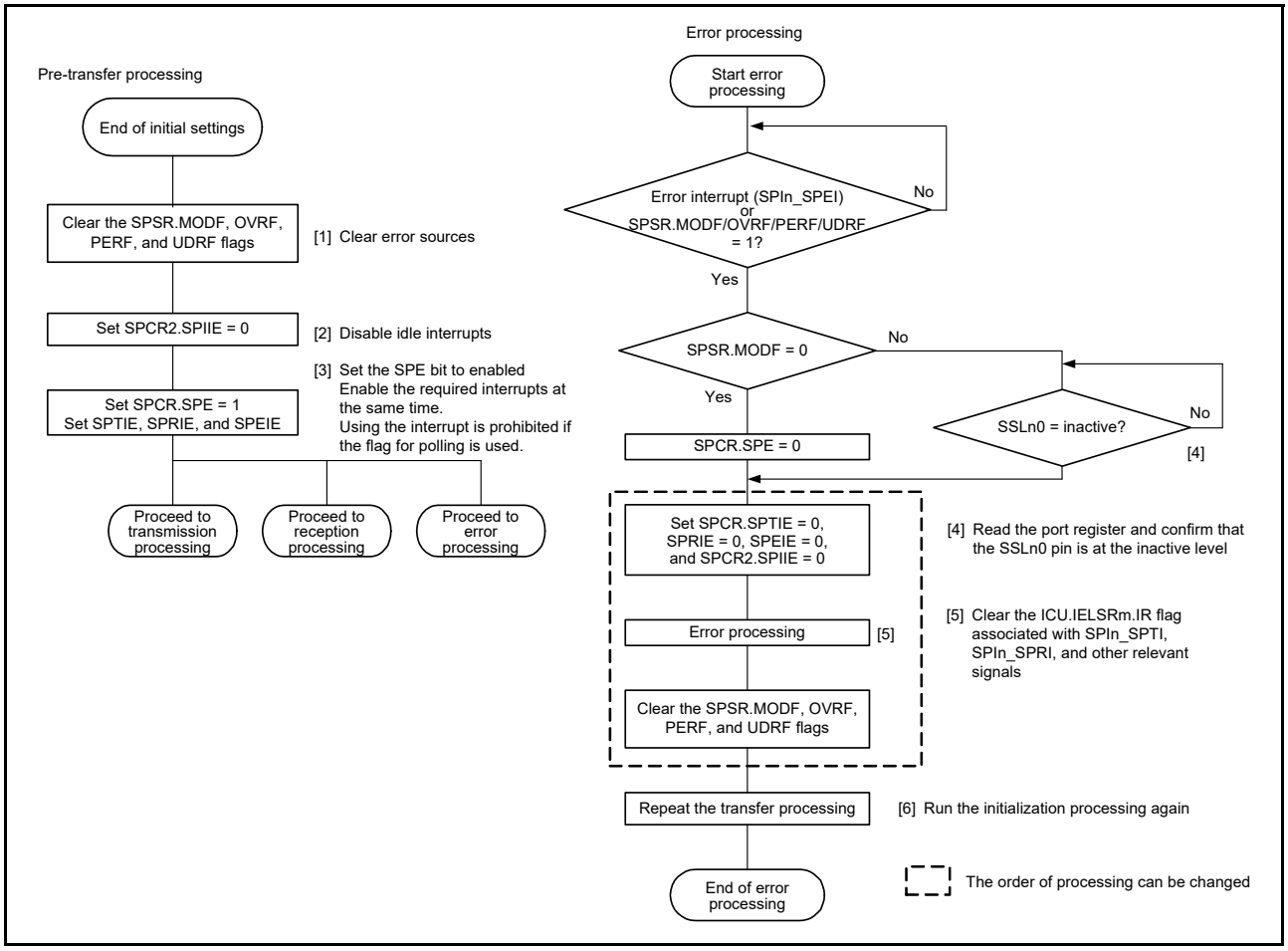


Figure 31.35 Error processing flow in master mode

31.3.10.2 Slave mode operation

(1) Starting a serial transfer

When the SPCMD0.CPHA bit is 0, if the SPI detects an SSLn0 input signal assertion, it must drive valid data to the MISOn output signal. For this reason, when the CPHA bit is 0, the assertion of the SSLn0 input signal triggers the start of a serial transfer.

When the CPHA bit is 1, if the SPI detects the first RSPCKn edge in an SSLn0 signal asserted condition, it must drive valid data to the MISOn output signal. For this reason, when the CPHA bit is 1, the first RSPCKn edge in an SSLn0 signal asserted condition triggers the start of a serial transfer.

Regardless of the CPHA bit setting, the SPI drives the MISOn output signal on SSLn0 signal assertion. The data that is output by the SPI is either valid or invalid, depending on the CPHA bit setting.

For details on the SPI transfer format, see section 31.3.5, Transfer Formats. The polarity of the SSLn0 input signal depends on the SSLP.SSL0P setting.

(2) Terminating a serial transfer

Regardless of the SPCMD0.CPHA bit setting, the SPI terminates the serial transfer after detecting an RSPCKn edge corresponding to the final sampling timing. When free space is available in the receive buffer (the SPSR.SPRF flag is 0), on termination of serial transfer the SPI copies received data from the shift register to the receive buffer of the SPDR/SPDR_HA register. On termination of a serial transfer, the SPI changes the status of the shift register to empty, regardless of the receive buffer state. A mode fault error occurs if the SPI detects an SSLn0 input signal negation from the beginning of serial transfer to the end of serial transfer (see section 31.3.8, Error Detection).

The final sampling timing changes depending on the bit length of transfer data. In slave mode, the SPI data length

depends on the SPCMD0.SPB[3:0] bit setting. The polarity of the SSLn0 input signal depends on the SSLP.SSL0P bit setting. For details on the SPI transfer format, see section 31.3.5, Transfer Formats.

(3) Notes on single-slave operations

If the SPCMD0.CPHA bit is 0, the SPI starts serial transfers when it detects the assertion edge for an SSLn0 input signal. In the type of configuration shown in Figure 31.7 as an example, if the SPI is used in single-slave mode, the SSLn0 signal is fixed at the active state. Therefore, when the CPHA bit is set to 0, the SPI cannot correctly start a serial transfer. To correctly execute transmit and receive operations by the SPI in slave mode when the SSLn0 input signal is fixed at the active state, the CPHA bit must be set to 1. Do not fix the SSLn0 input signal if there is a requirement for setting the CPHA bit to 0.

(4) Initialization flow

Figure 31.36 shows an example of initialization flow for SPI operation when the SPI is in slave mode. For information on how to set up the Interrupt Controller Unit, DTC, and I/O Ports, see the individual block descriptions.

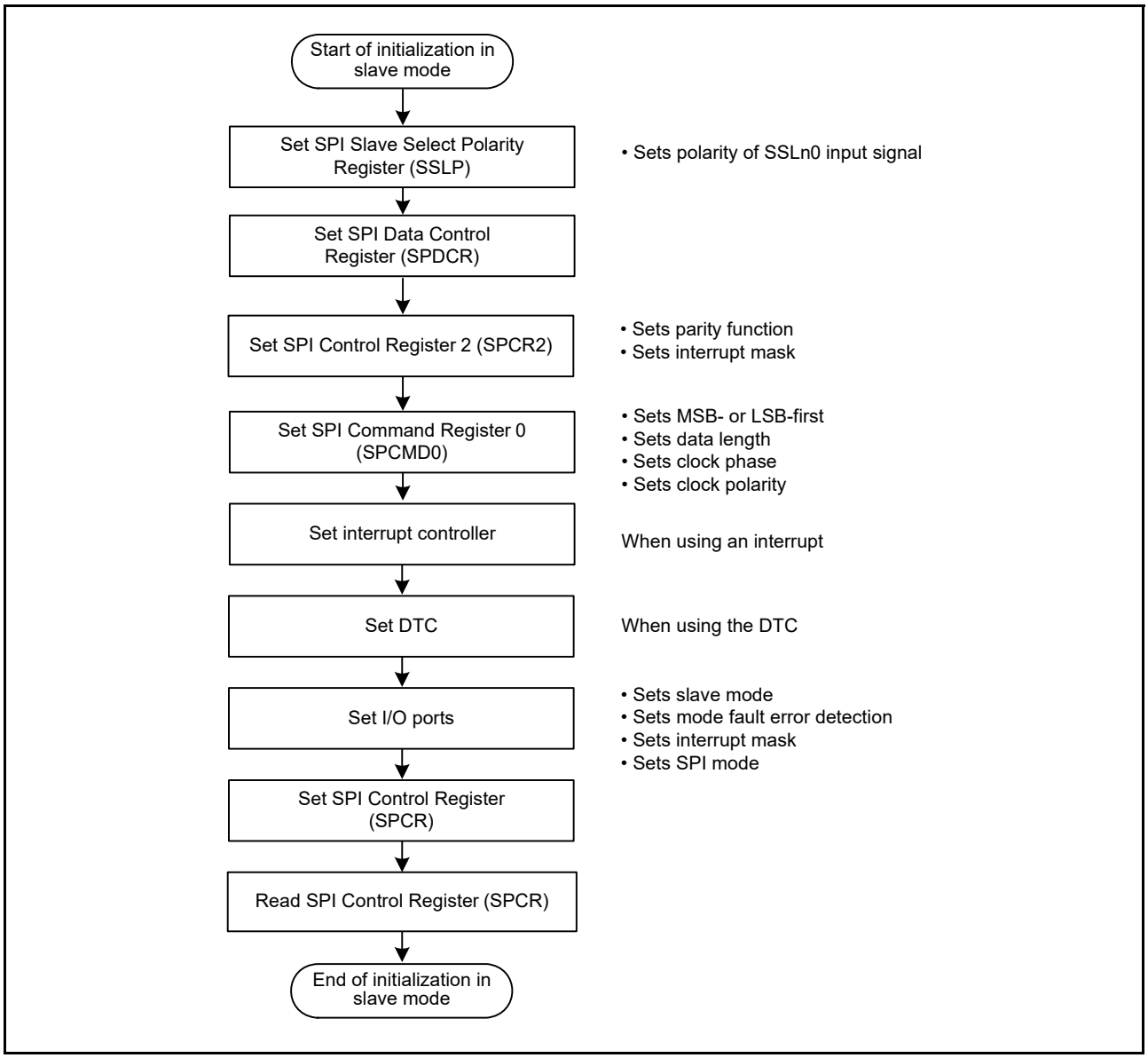


Figure 31.36 Example of initialization flow in slave mode for SPI operation

(5) Software processing flow

Figure 31.37 to Figure 31.39 show example flows of software processing.

(a) Transmit processing flow

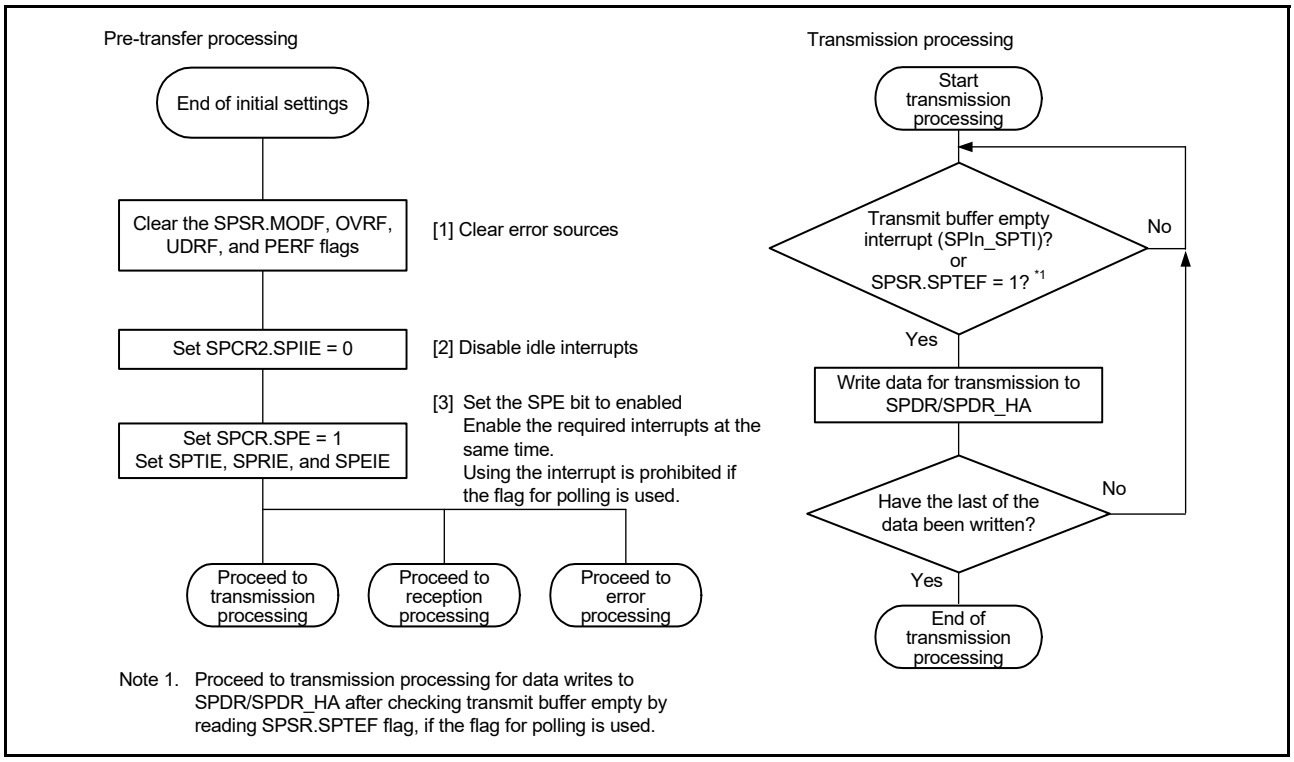


Figure 31.37 Transmission flow in slave mode

(b) Receive processing flow

The SPI does not handle receive-only operation, therefore processing for transmission is required.

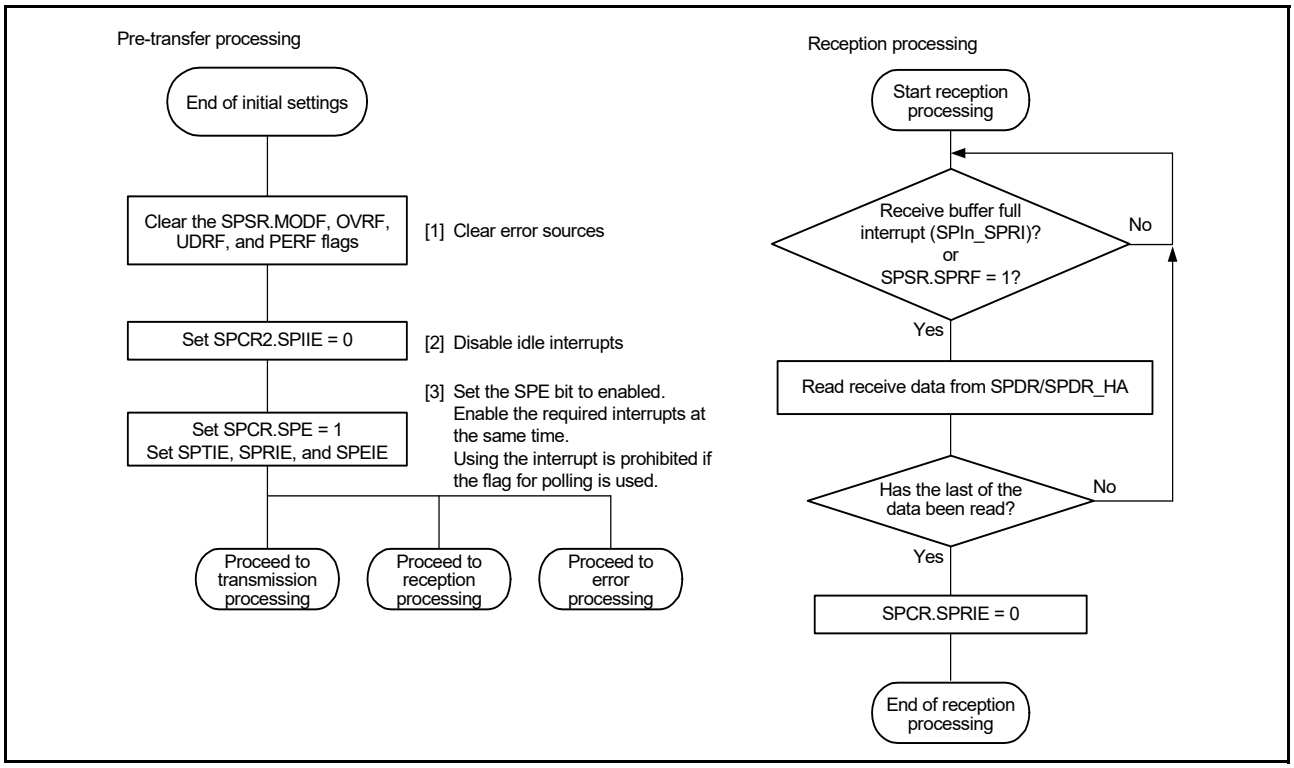


Figure 31.38 Reception flow in slave mode

(c) Error processing flow

In slave operation, even when a mode-fault error is generated, the SPSR.MODF flag can be cleared regardless of the state of the SSLn0 pin.

When an error is detected by using an interrupt, clear the ICU.IELSRm.IR flag in the error processing routine. If this is not done, the ICU.IELSRm.IR flag might continue to indicate the transmit buffer empty or receive buffer full interrupt request. If the receive buffer full request is indicated, read the receive buffer and initialize the sequencer in the SPI.

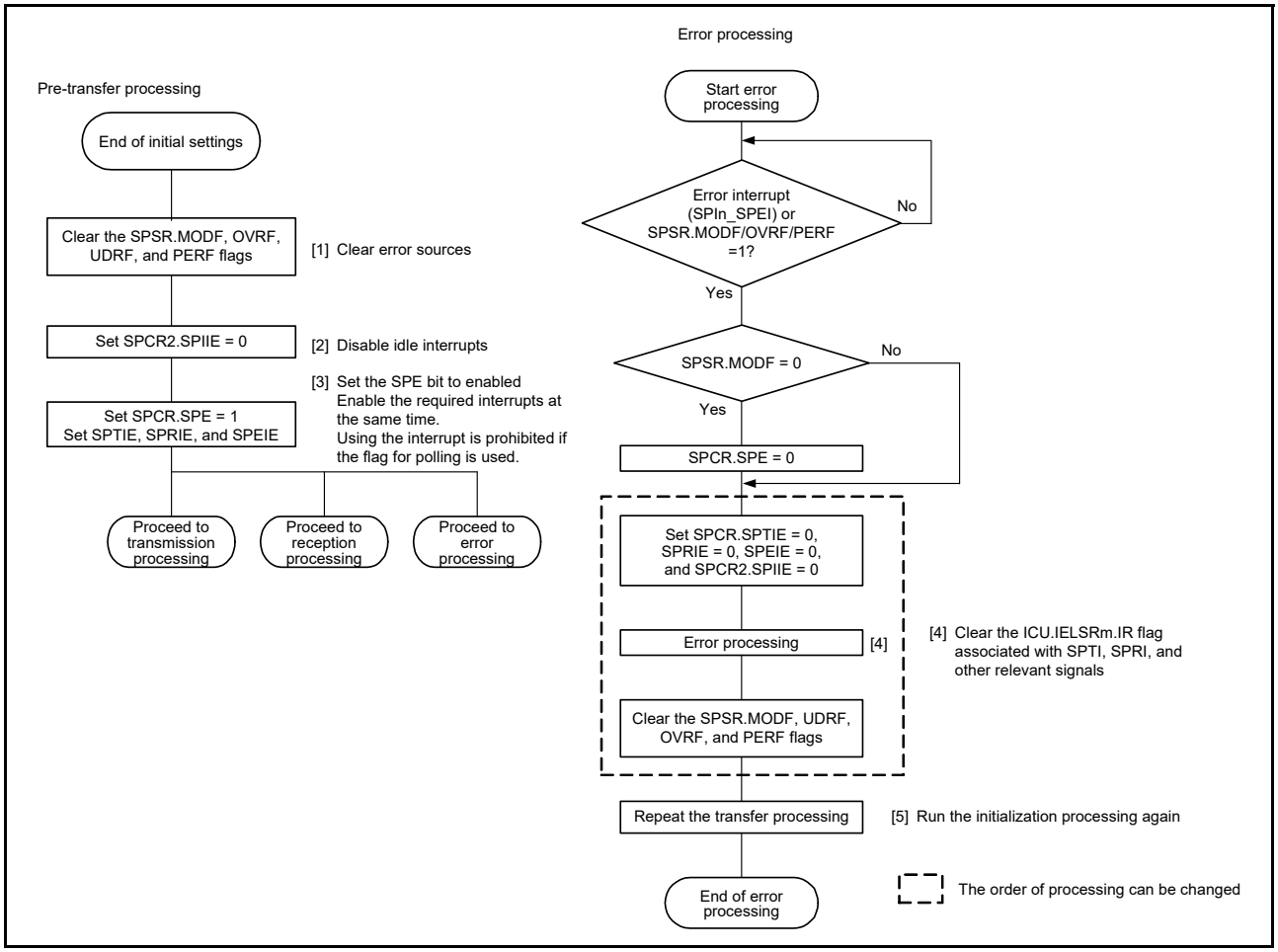


Figure 31.39 Error processing flow for slave mode

31.3.11 Clock Synchronous Operation

Setting the SPCR.SPMS bit to 1 selects clock synchronous operation of the SPI. In clock synchronous operation, the SSLni pin is not used, and the RSPCKn, MOSIn, and MISOn pins handle communications. All SSLni pins are available as I/O port pins.

Although clock synchronous operation does not require the use of the SSLni pin, operation of the module is the same as in SPI operation. In both master and slave operations, communications can be performed with the same flow as in SPI operation. However, mode fault errors are not detected because the SSLni pin is not used.

Additionally, do not perform operation if clock synchronous operation enabled when the SPCMD0.CPHA bit is set to 0 in slave mode (SPCR.MSTR = 0).

31.3.11.1 Master mode operation

(1) Starting serial transfer

The SPI updates the data in the transmit buffer (SPTX) of SPDR/SPDR_HA when data is written to the SPDR/SPDR_HA register with the transmit buffer being empty, that is, data for the next transfer is not set and the SPSR.SPTEF

flag is 1. When the shift register is empty after data is written to SPDR/SPDR_HA, the SPI copies data from the transmission buffer to the shift register and starts serial transmission. On copying transmit data to the shift register, the SPI changes the status of the shift register to full, and on termination of serial transfer, it changes the status of the shift register to empty. The status of the shift register cannot be referenced.

Transfer in clock synchronous operation is conducted without the SSLn0 output signal. For details on the SPI transfer format, see section 31.3.5, Transfer Formats.

(2) Terminating serial transfer

The SPI terminates the serial transfer after transmitting an RSPCKn edge corresponding to the sampling timing. If free space is available in the receive buffer (the SPSR.SPRF flag is 0), on termination of serial transfer, the SPI copies data from the shift register to the receive buffer of the SPI Data Register (SPDR/SPDR_HA).

The final sampling timing varies depending on the bit length of transfer data. In master mode, the SPI data length depends on the SPCMD0.SPB[3:0] bit setting.

Transfer in clock synchronous operation is conducted without the SSLn0 output signal. For details on the SPI transfer format, see section 31.3.5, Transfer Formats.

(3) Initialization flow

Figure 31.40 shows an example of initialization flow for clock synchronous operation when the SPI is in master mode. For information on how to set up the Interrupt Controller Unit, DTC, and I/O Ports, see the individual block descriptions.

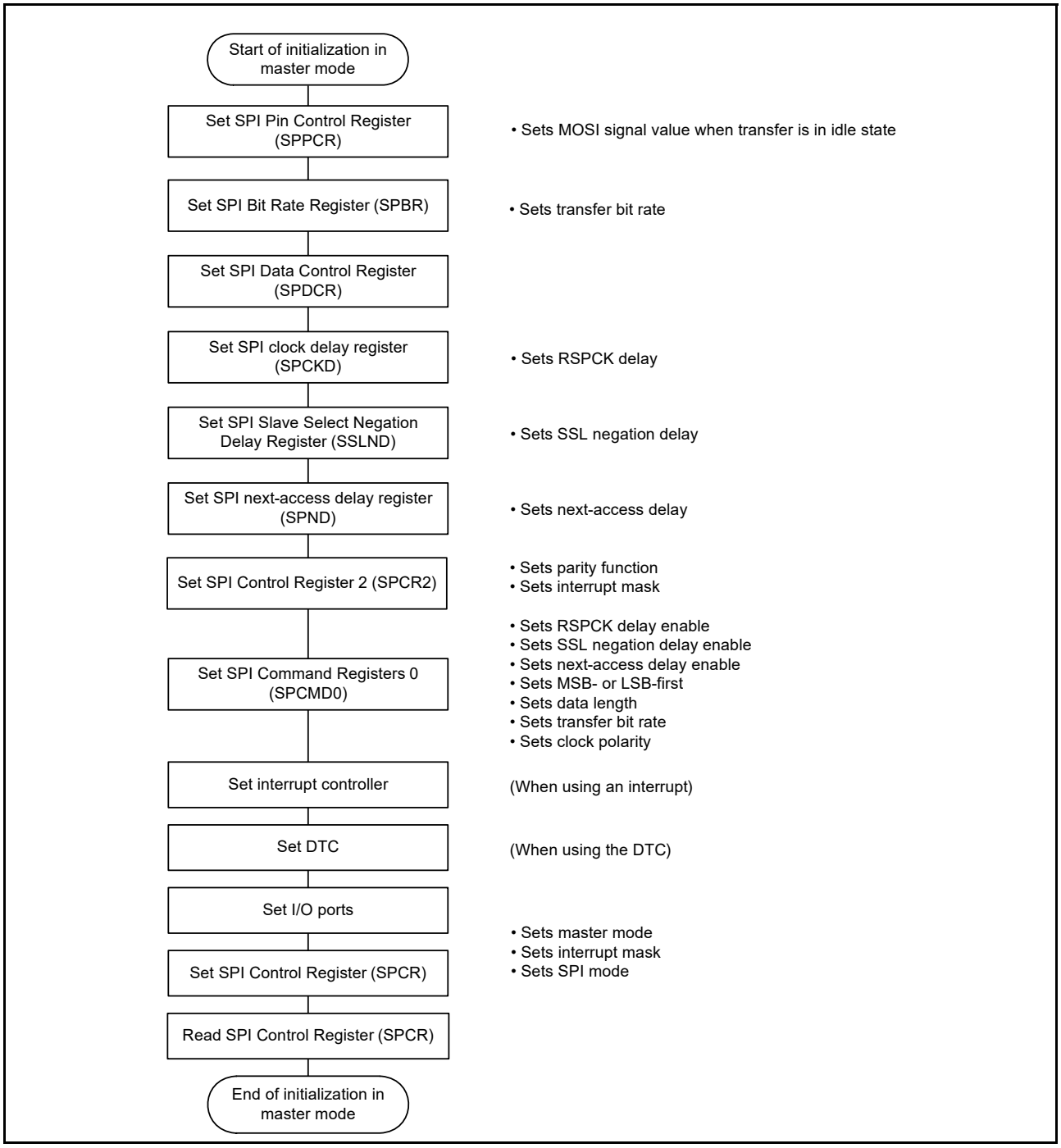


Figure 31.40 Example of initialization flow in master mode for clock synchronous operation

(4) Software processing flow

Software processing during clock synchronous master operation is the same as that for SPI master operation. For details, see section 31.3.10.1, (7) Software processing flow. Mode fault errors do not occur in clock synchronous operation.

31.3.11.2 Slave mode operation

(1) Starting serial transfer

When the SPCR.SPMS bit is 1, the first RSPCKn edge triggers the start of a serial transfer in the SPI and the SPI drives the MISOn output signal. The SSLn0 input signal is not used in clock synchronous operation. For details on the SPI transfer format, see section 31.3.5, Transfer Formats.

(2) Terminating serial transfer

The SPI terminates the serial transfer after detecting an RSPCKn edge corresponding to the final sampling timing. When free space is available in the receive buffer (the SPSR.SPRF flag is 0), on termination of a serial transfer, the SPI copies received data from the shift register to the receive buffer of the SPDR/SPDR_HA register. On termination of a serial transfer, the SPI changes the status of the shift register to empty regardless of the receive buffer. The final sampling timing changes depending on the bit length of transfer data. In slave mode, the SPI data length depends on the SPCMD0.SPB[3:0] bit setting.

For details on the SPI transfer format, see section 31.3.5, Transfer Formats.

(3) Initialization flow

Figure 31.41 shows an example of initialization flow for clock synchronous operation when the SPI is in slave mode. For information on how to set up the Interrupt Controller Unit, DTC, and I/O Ports, see the individual block descriptions.

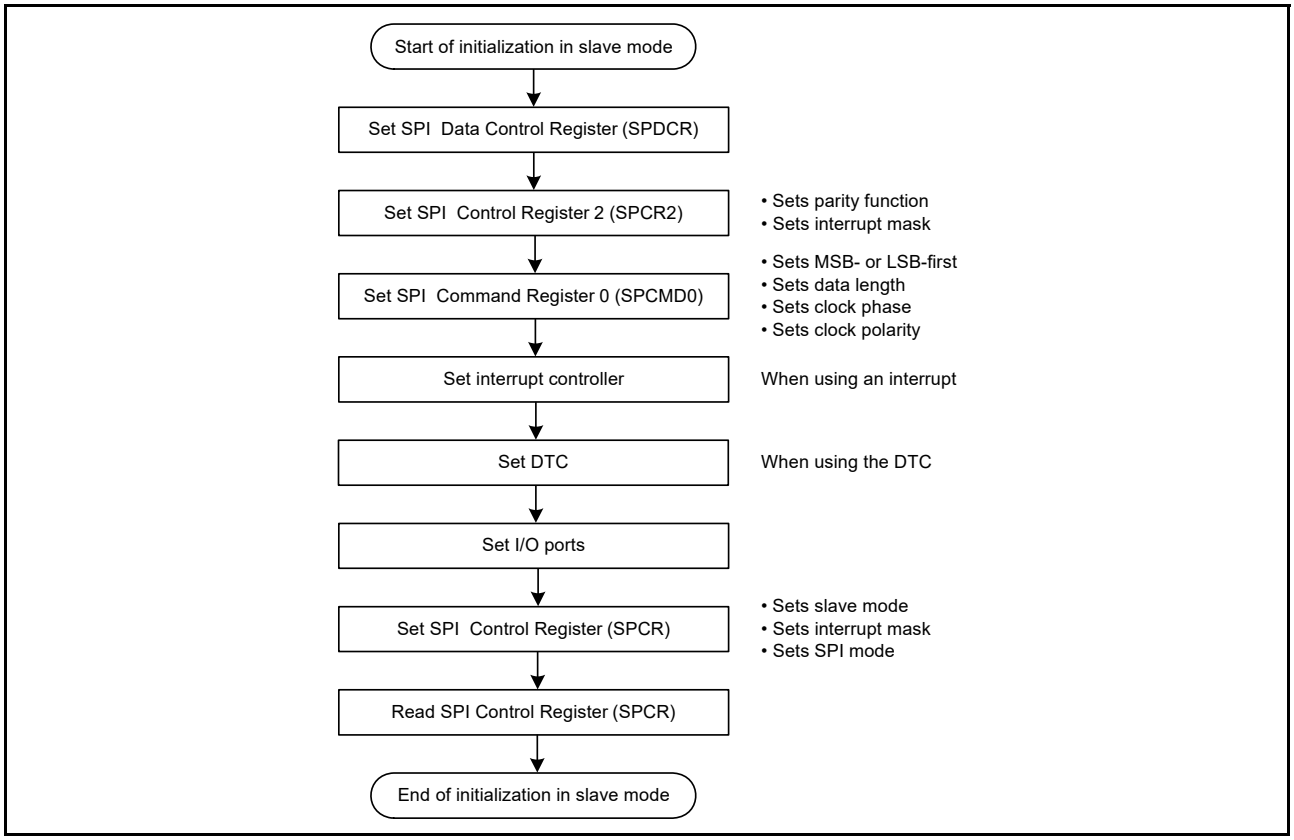


Figure 31.41 Example of initialization flow in slave mode for clock synchronous operation

(4) Software processing flow

Software processing during clock-synchronous slave operation is the same as that for SPI slave operation. For details, see section 31.3.10.2, (5) Software processing flow. Mode fault errors do not occur in clock synchronous mode.

31.3.12 Loopback Mode

When 1 is written to the SPPCR.SPLP2 bit or SPPCR.SPLP bit, the SPI shuts off the path between the MISOn pin and the shift register if the SPCR.MSTR bit is 1, or between the MOSIn pin and the shift register if the SPCR.MSTR bit is 0, and connects the input path and output path of the shift register. The SPI does not shut off the path between the MOSIn pin and the shift register if the SPCR.MSTR bit is 1, or between the MISOn pin and the shift register if the SPCR.MSTR bit is 0. This is called loopback mode. When a serial transfer is executed in loopback mode, the transmit data for the SPI or the reversed transmit data becomes the received data for the SPI.

Table 31.11 shows the relationship between the SPLP2 and SPLP bits and the received data. Figure 31.42 shows the configuration of the shift register I/O paths when the SPI in master mode is set in loopback mode (SPPCR.SPLP2 = 1, SPPCR.SPLP = 0 or 1).

Table 31.11 SPLP2 and SPLP bit settings and received data

SPPCR.SPLP2 bit	SPPCR.SPLP bit	Received data
0	0	Input data from the MOSIn or MISOn pin
0	1	Inverted transmit data
1	0	Transmit data
1	1	Transmit data

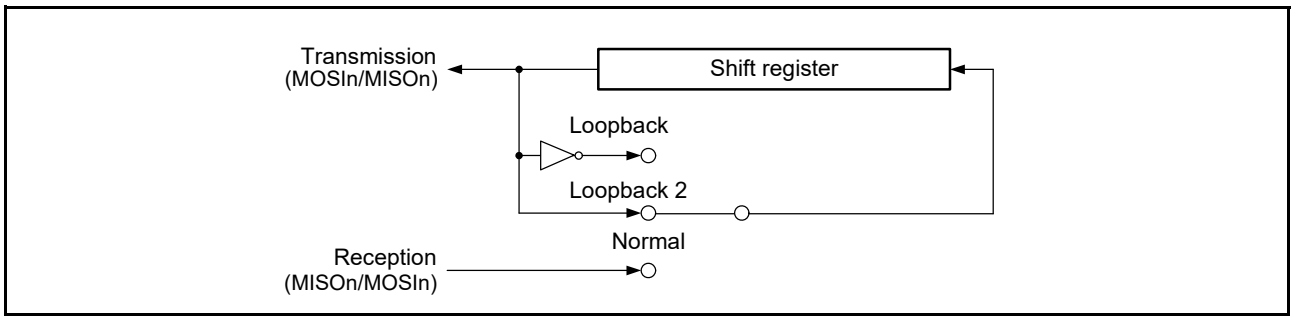


Figure 31.42 Configuration of shift register I/O paths in loopback mode for master mode

31.3.13 Self-Diagnosis of Parity Bit Function

The parity circuit consists of a parity bit adding unit for transmit data and an error detecting unit for received data. To detect defects in these units, the parity circuit performs self-diagnosis as shown in Figure 31.43.

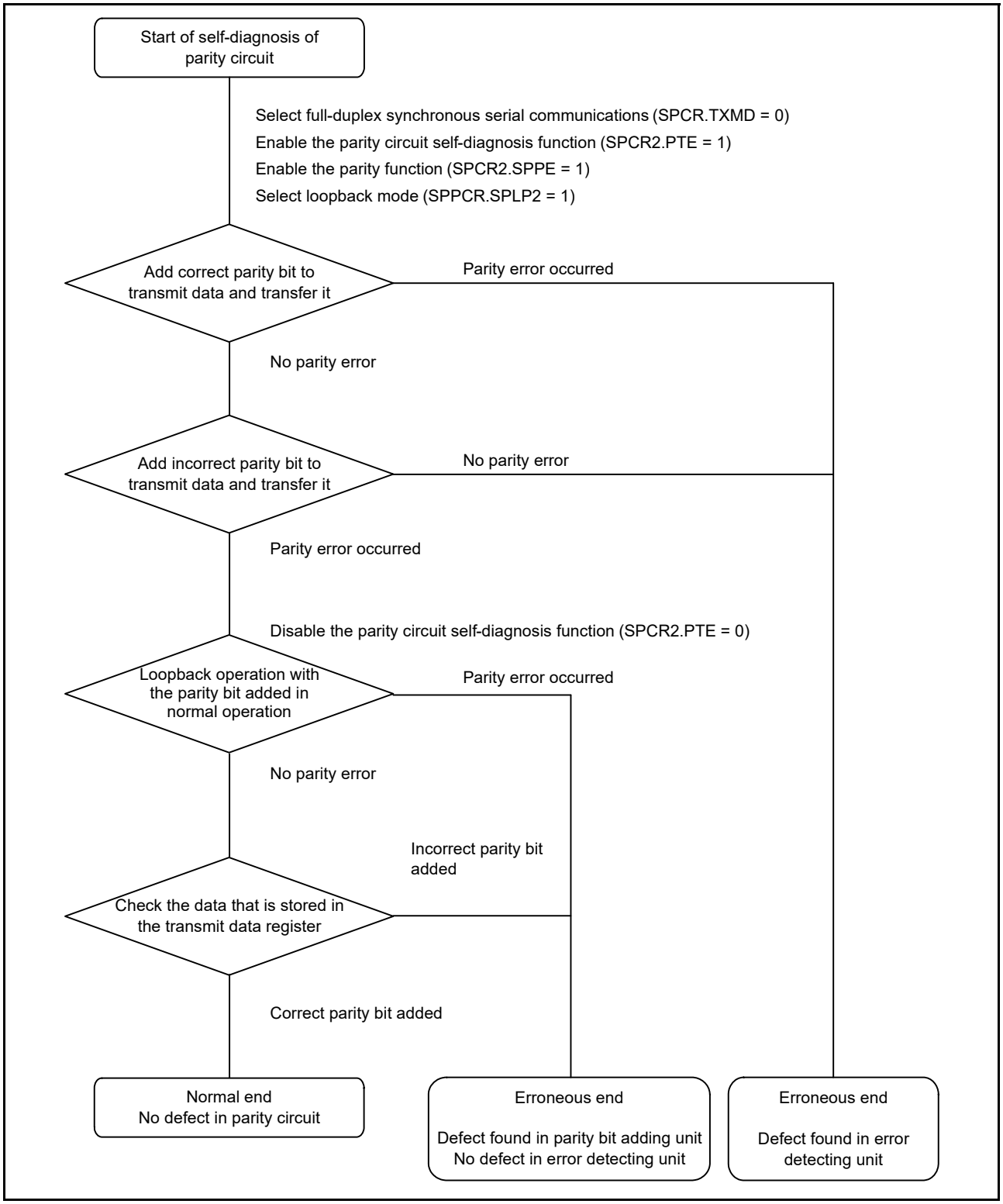


Figure 31.43 Self-diagnosis flow for parity circuit

31.3.14 Interrupt Sources

The SPI has eight interrupt sources:

- Receive buffer full
- Transmit buffer empty
- Transmission complete
- Mode fault
- Underrun
- Overrun
- Parity error
- SPI idle.

The DTC can be activated by the receive buffer full or transmit buffer empty interrupt to perform data transfer.

Because the vector address for SPIn_SPEI is allocated to interrupt requests triggered by mode-fault, underrun, overrun, and parity errors, the actual interrupt source must be determined from the flags. Table 31.12 lists the flags associated with the interrupt sources for the SPI. An interrupt is generated on satisfaction of an interrupt condition in Table 31.12. Clear the receive buffer full and transmit buffer empty sources through a data transfer.

When using the DTC to perform data transmission or reception, you must first set up the DTC to a transfer-enabled status before making the SPI settings. For information on setting the DTC, see section 15, Data Transfer Controller (DTC).

If the conditions for generating a transmit buffer empty or receive buffer full interrupt occur while the ICU.IELSRm.IR flag is 1, the interrupt is not output as a request for the ICU but is saved internally (the capacity for retention is one request per source). A saved interrupt request is output when the ICU.IELSRm.IR flag becomes 0. A saved interrupt request is automatically discarded when it is output as an actual interrupt request. The interrupt enable bit (SPCR.SPTIE or SPCR.SPRIE) for an internally saved interrupt request can also be cleared to 0.

Table 31.12 SPI interrupt sources

Interrupt source	Symbol	Interrupt condition	DTC activation
Receive buffer full	SPIn_SPRI	The receive buffer becomes full (SPSR.SPRF flag is 1) while the SPCR.SPRIE bit is 1.	Possible
Transmit buffer empty	SPIn_SPTI	The transmit buffer becomes empty (SPSR.SPTEF flag is 1) while the SPCR.SPTIE bit is 1.	Possible
SPI errors (mode fault, underrun, overrun, and parity error)	SPIn_SPEI	The SPSR.MODF, OVRF, PERF, or UDRF flag is set to 1 while the SPCR.SPEIE bit is 1.	Impossible
SPI idle	SPIn_SPII	The SPSR.IDLNF flag is set to 0 while the SPCR2.SPIIE bit is 1.	Impossible
Transmission complete	SPIn_SPTEND	In master mode, an interrupt is generated when the IDLNF flag (SPI idle flag) changes from 1 to 0. In slave mode, an interrupt occurs on conditions shown in Table 31.14.	Impossible

31.4 Event Link Operation

The Event Link Controller (ELC) can produce the following event output signals:

- Receive buffer full event output
- Transmit buffer empty event output
- Mode fault, underrun, overrun, or parity event output
- SPI idle event output
- Transmission-complete event output.

The event link output signal is output regardless of the interrupt enable bit setting.

31.4.1 Receive Buffer Full Event Output

This event signal is output when received data is transferred from the shift register to the SPDR/SPDR_HA on completion of a serial transfer.

31.4.2 Transmit Buffer Empty Event Output

This event signal is output when data for transmission is transferred from the transmission buffer to the shift register and when the value of the SPE bit changed from 0 to 1.

31.4.3 Mode Fault, Underrun, Overrun, or Parity Error Event Output

This event signal is output when mode fault, underrun, overrun, or parity error is detected. See section 31.5.4, Restrictions on Mode Fault, Underrun, Overrun, or Parity Error Event Output if using this event signal.

(1) Mode fault

Table 31.13 lists the conditions for occurrence of a mode fault event.

Table 31.13 Conditions for mode fault occurrence

Conditions	SPCR.MODFEN bit	SSLn0 pin	Remarks
SPI operation (SPMS = 0) Slave (SPCR.MSTR bit = 0)	1	Not active	Event is output only when the pin is deactivated during transmission

(2) Underrun

This event signal is output in response to an underrun when a serial transfer starts while the transmission data is not ready, and the value of the SPCR.MSTR bit is 0, and SPCR.SPE bit is 1. Under these conditions, the MODF and UDRF flags are set to 1.

(3) Overrun

This event signal is output in response to an overrun when a serial transfer completes while the reception buffer contains unread data, and the value of the SPCR.TXMD bit is 0. Under these conditions, the OVRF flag is set to 1.

(4) Parity error

This event signal is output in response to a parity error detected on completion of a serial transfer while the value in the TXMD bit in SPCR is 0 and the value of the SPPE bit in SPCR2 is 1.

31.4.4 SPI Idle Event Output

(1) In master mode

In master mode, an event is output when the condition for setting the IDLNF flag (SPI idle flag) to 0 is satisfied.

(2) In slave mode

In slave mode, an event is output when the SPCR.SPE bit is set to 0 (SPI is initialized).

31.4.5 Transmission-Complete Event Output

During both SPI operation and clock synchronous operation in master mode, an event is output when the IDLNF flag (SPI idle flag) changes from 1 to 0. lists the conditions for occurrence of a mode fault event.

Table 31.14 Conditions for generation of transmission-complete event in slave mode

Conditions	Transmit buffer state	Shift register state	Others
SPI operation (SPMS = 0)	Empty	Empty	Negation of SSLn0 input
Clock synchronous operation (SPMS = 1)	Empty	Empty	Edge detection of the last RSPCKn

Whether the operation is in master or slave mode, an event is not output if 0 is written to the SPCR.SPE bit in

transmission or the SPCR.SPE bit is cleared by the mode fault or underrun error.

31.5 Usage Notes

31.5.1 Settings for the Module-Stop Function

The Module-Stop Control Register B (MSTPCRB) can enable or disable SPI operation. The SPI is initially stopped after a reset. The registers become accessible on release from the module-stop state. For details on the Module-Stop Control Register B, see section 10, Low Power Modes.

31.5.2 Restrictions on Low Power Function

When using the module-stop function and entering a low power mode other than Sleep mode, set the SPCR.SPE bit to 0 before completing communication.

31.5.3 Restrictions on Starting Transfer

If the ICU.IELSRm.IR flag is 1 when transfer starts, the interrupt request is internally saved, which can lead to unanticipated behavior of the ICU.IELSRm.IR flag. To prevent this, use the following procedure to clear interrupt requests before enabling operations (by setting the SPCR.SPE bit to 1).

1. Confirm that transfer stopped (SPCR.SPE is 0).
2. Set the relevant interrupt enable bit (SPCR.SPTIE or SPCR.SPRIE) to 0.
3. Read the relevant interrupt enable bit (SPCR.SPTIE or SPCR.SPRIE) and confirm that its value is 0.
4. Set the ICU.IELSRm.IR flag to 0.

31.5.4 Restrictions on Mode Fault, Underrun, Overrun, or Parity Error Event Output

Using the mode fault, underrun, overrun, or parity error event is prohibited if the SPI is in multi-master mode (when the SPCR.SPMS bit is 0, the SPCR.MSTR bit is 1, and the SPCR.MODFEN bit is 1).

31.5.5 Constraints on the SPRF and SPTEF Flags

If the polling flags, SPRF and SPTEF, are used, using the interrupts are prohibited, and you must set the SPCR.SPRIE and SPCR.SPTIE bits to 0. Either the interrupts or the flags can be used, but not both.

32. Cyclic Redundancy Check (CRC) Calculator

32.1 Overview

The Cyclic Redundancy Check (CRC) calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB first or MSB first communication. Additionally, various CRC generation polynomials are available. The snoop function allows monitoring reads from and writes to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer.

Table 32.1 lists the specifications of the CRC calculator, and Figure 32.1 shows a block diagram.

Table 32.1 CRC calculator specifications

Parameter	Description	
Data size	8-bit	32-bit
Data for CRC calculation*1	CRC code generated for any desired data in 8n-bit units (where n is a whole number)	CRC code generated for data in 32n-bit units (where n is a whole number)
CRC processor unit	Operation executed on 8 bits in parallel	Operation executed on 32 bits in parallel
CRC generating polynomial	One of three generating polynomials that is selectable: [8-bit CRC] • $X^8 + X^2 + X + 1$ (CRC-8) [16-bit CRC] • $X^{16} + X^{15} + X^2 + 1$ (CRC-16) • $X^{16} + X^{12} + X^5 + 1$ (CRC-CCITT)	One of two generating polynomials that is selectable: [32-bit CRC] • $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ (CRC-32) • $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$ (CRC-32C)
CRC calculation switching	The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication	
Module-stop function	Module-stop state can be set	
CRC snoop	Monitor reads from and writes to a certain register address	—

Note 1. The circuit does not have functionality to divide data used in CRC calculations. Write data in 8-bit or 32-bit units.

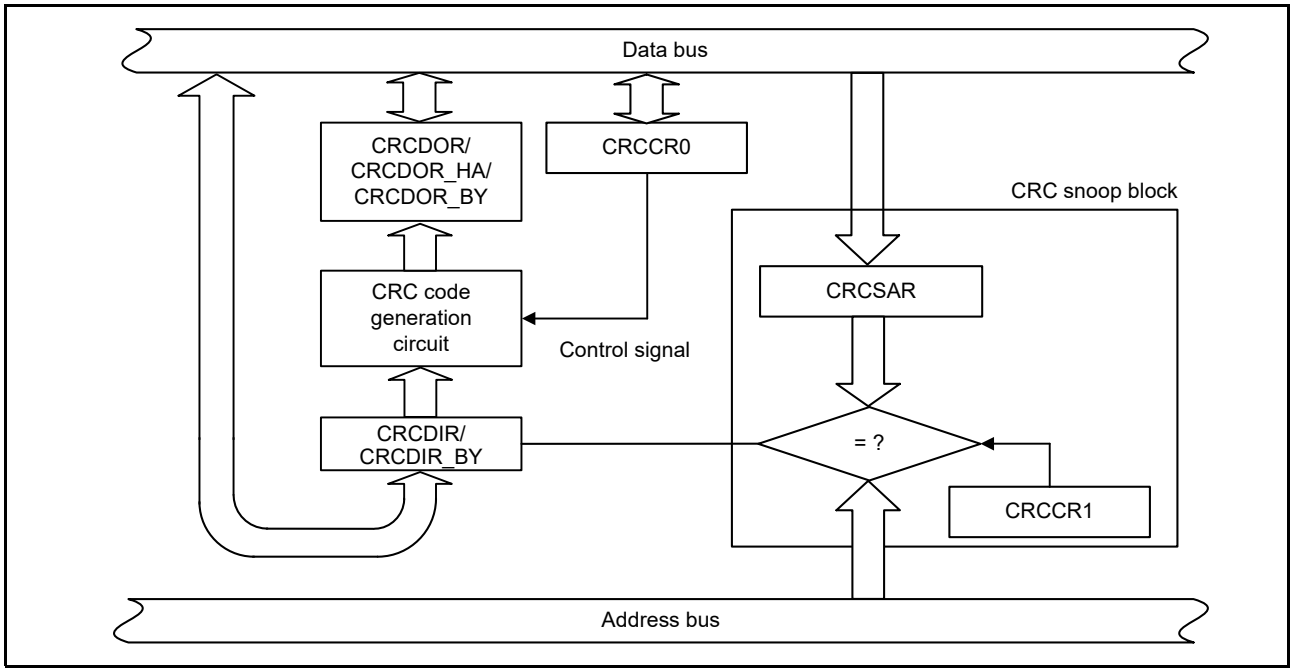


Figure 32.1 CRC calculator block diagram

32.2 Register Descriptions

32.2.1 CRC Control Register 0 (CRCCR0)

Address(es): CRC.CRCCR0 4007 4000h

	b7	b6	b5	b4	b3	b2	b1	b0
	DORCLR	LMS	—	—	—	GPS[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	GPS[2:0]	CRC Generating Polynomial Switching	b2 b0 0 0 0: No calculation is executed 0 0 1: 8-bit CRC-8 ($X^8 + X^2 + X + 1$) 0 1 0: 16-bit CRC-16 ($X^{16} + X^{15} + X^2 + 1$) 0 1 1: 16-bit CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) 1 0 0: 32-bit CRC-32 ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$) 1 0 1: 32-bit CRC-32C ($X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$) Other: No calculation is executed.	R/W
b5 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	LMS	CRC Calculation Switching	0: Generates CRC for LSB-first communication 1: Generates CRC for MSB-first communication.	R/W
b7	DORCLR	CRCDOR/CRCDOR_HA/ CRCDOR_BY Register Clear	1: Clears the CRCDOR/CRCDOR_HA/CRCDOR_BY register. This bit is read as 0.	W*1

Note 1. Always set this bit to 1 when writing to this register.

DORCLR bit (CRCDOR/CRCDOR_HA/CRCDOR_BY)

Write 1 to this bit so that the CRCDOR/CRCDOR_HA/CRCDOR_BY register is set to 0000 0000h.

This bit is read as 0. Only 1 can be written.

LMS bit (CRC Calculation Switching)

Set this bit to select the bit order of generated CRC code. Transmit the lower-order byte of the CRC code first for LSB-first communication and the upper-order byte first for MSB-first communication. For details on transmitting and receiving CRC code, see section 32.3, Operation.

GPS[2:0] bits (CRC Generating Polynomial Switching)

Set the GPS[2:0] bits to select the CRC Generating Polynomial.

32.2.2 CRC Control Register 1 (CRCCR1)

Address(es): CRC.CRCCR1 4007 4001h

	b7	b6	b5	b4	b3	b2	b1	b0
	CRCSEN	CRCSWR	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit name	Description	R/W
b6	CRCSWR	Snoop-On-Write/Read Switch	0: Snoop-on-read 1: Snoop-on-write.	R/W
b7	CRCSEN	Snoop Enable	0: Disabled 1: Enabled.	R/W

CRCSWR bit (Snoop-On-Write/Read Switch)

The CRCSWR bit selects the direction of the access in the address monitoring function.

When this bit is set to 0, the CRC snoop operation to read a specific register address is valid. When this bit is set to 1, the CRC snoop operation to write a specific register address is valid.

CRCSEN bit (Snoop Enable)

When setting this bit to 1, the CRC snoop operation is valid. When setting this bit to 0, the CRC snoop operation is invalid.

32.2.3 CRC Data Input Register (CRCDIR/CRCDIR_BY)

Address(es): CRC.CRCDIR/CRCDIR_BY 4007 4004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The CRCDIR register is a read/write 32-bit register to write data for CRC-32 or CRC-32C calculation. The CRCDIR_BY register is a read/write 8-bit register to write data for CRC-8, CRC-16, or CRC-CCITT calculation.

32.2.4 CRC Data Output Register (CRCDOR/CRCDOR_HA/CRCDOR_BY)

Address(es): CRC.CRCDOR/CRCDOR_HA/CRCDOR_BY 4007 4008h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The CRCDOR register is a read/write 32-bit register for CRC-32 or CRC-32C.

The CRCDOR_HA register is a read/write 16-bit register for CRC-16 or CRC-CCITT.

The CRCDOR_BY register is a read/write 8-bit register for CRC-8.

Because its initial value is 0000 0000h, rewrite the CRCDOR/CRCDOR_HA/CRCDOR_BY register to perform the calculation using a value other than the initial value.

Data written to the CRCDIR/CRCDIR_BY register is CRC calculated and the result is stored in the CRCDOR/CRCDOR_HA/CRCDOR_BY register. If the CRC code is calculated following transferred data and the result is 0000 0000h, there is no CRC error.

When an 8-bit CRC ($X^8 + X^2 + X + 1$ polynomial) is in use, the valid CRC code is obtained in CRCDOR_BY.

When a 16-bit CRC ($X^{16} + X^{15} + X^2 + 1$ or $X^{16} + X^{12} + X^5 + 1$ polynomial) is in use, the valid CRC code is obtained in CRCDOR_HA.

32.2.5 Snoop Address Register (CRCSAR)

Address(es): CRC.CRCSAR 4007 400Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CRCSA[13:0]													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b13 to b0	CRCSA[13:0]	Register Snoop Address	Set the TDR or RDR address in the SCI module to snoop	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CRCSA[13:0] bits (Register Snoop Address)

Set the CRCSA[13:0] bits to the lower 14-bit of register address monitored by the CRC snoop operation.

Only the following address can be used for the CRCSA[13:0] bits:

- 4007 0003h: SCI0.TDR, 4007 0005h: SCI0.RDR
- 4007 0023h: SCI1.TDR, 4007 0025h: SCI1.RDR
- 4007 0123h: SCI9.TDR, 4007 0125h: SCI9.RDR
- 4007 000Fh: SCI0.FTDRL, 4007 0011h: SCI0.FRDRL.

32.3 Operation

32.3.1 Basic Operation

The CRC calculator generates CRC codes for use in LSB-first or MSB-first transfer.

The following examples show CRC code generation for input data (F0h) using the 16-bit CRC-CCITT generating polynomial ($X^{16} + X^{12} + X^5 + 1$). In these examples, the value of the CRC data output register (CRCDOR_HA) is cleared before CRC calculation.

When an 8-bit CRC (with the polynomial $X^8 + X^2 + X + 1$) is in use, the valid bits of the CRC code are obtained in CRCDOR_BY. When an 32-bit CRC is in use, the valid bits of the CRC code are obtained in CRCDOR.

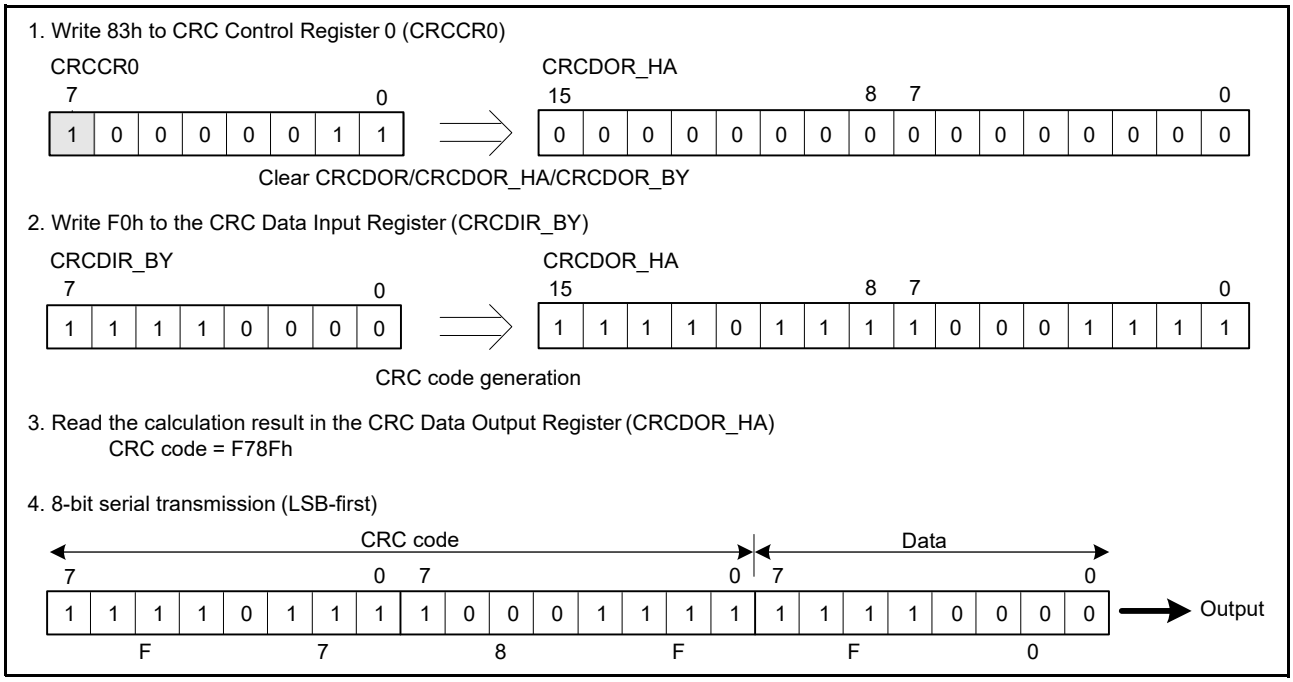


Figure 32.2 LSB-first data transmission

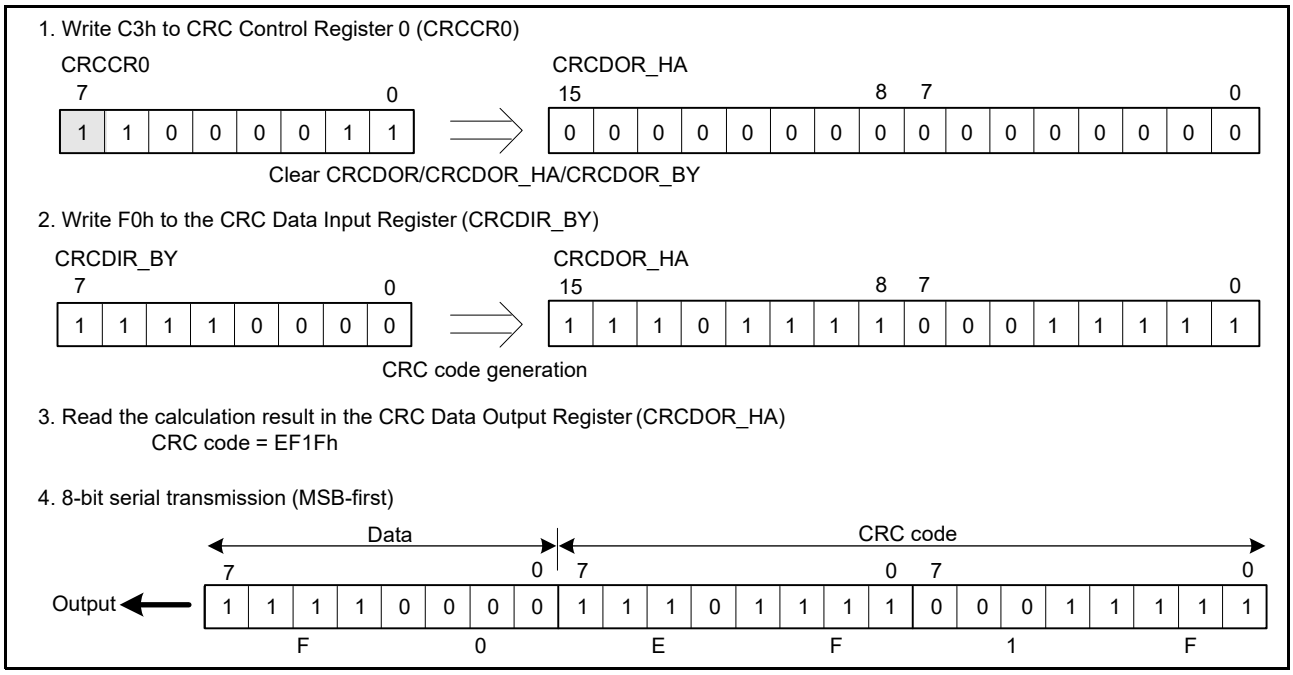


Figure 32.3 MSB-first data transmission

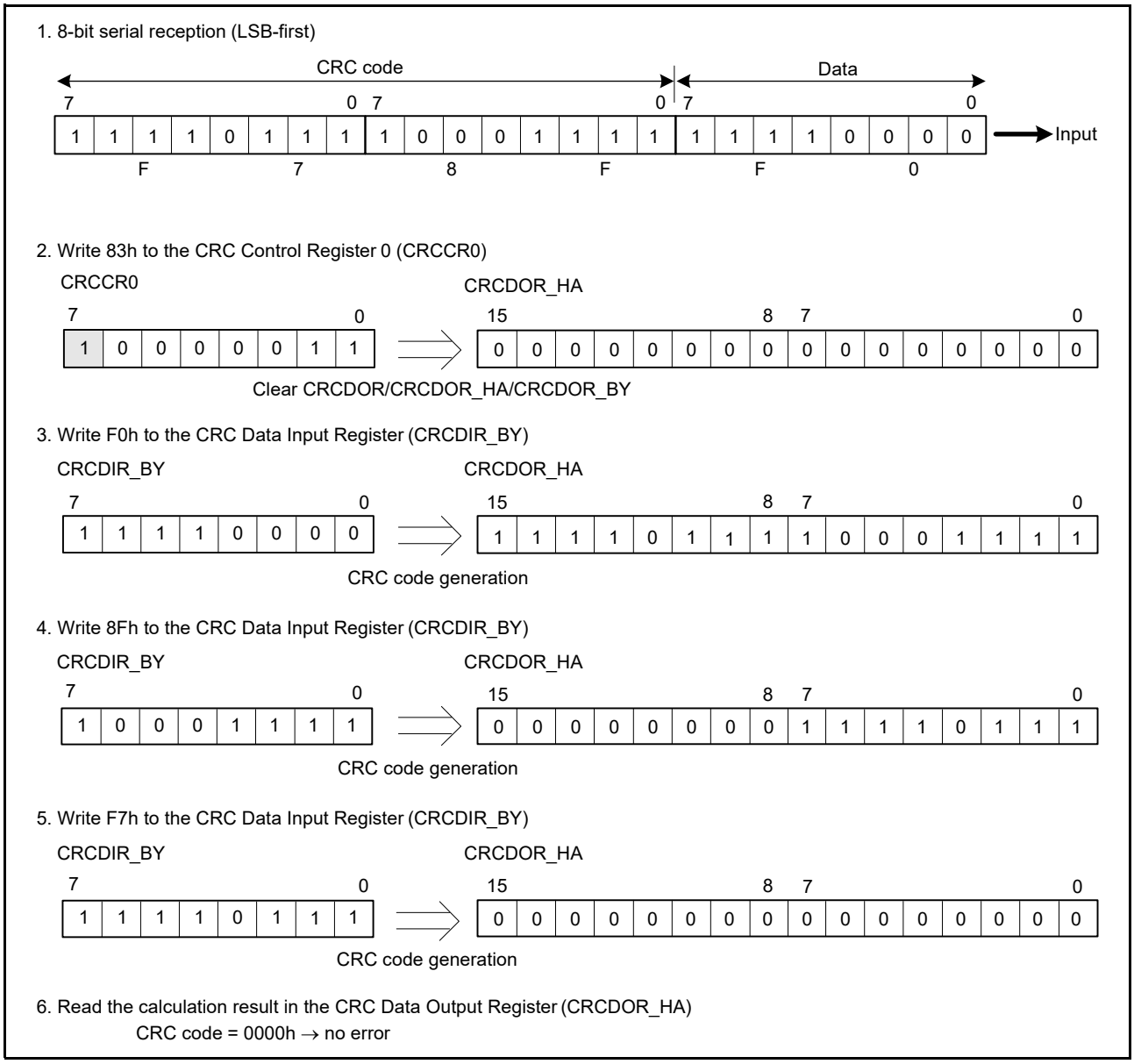


Figure 32.4 LSB-first data reception

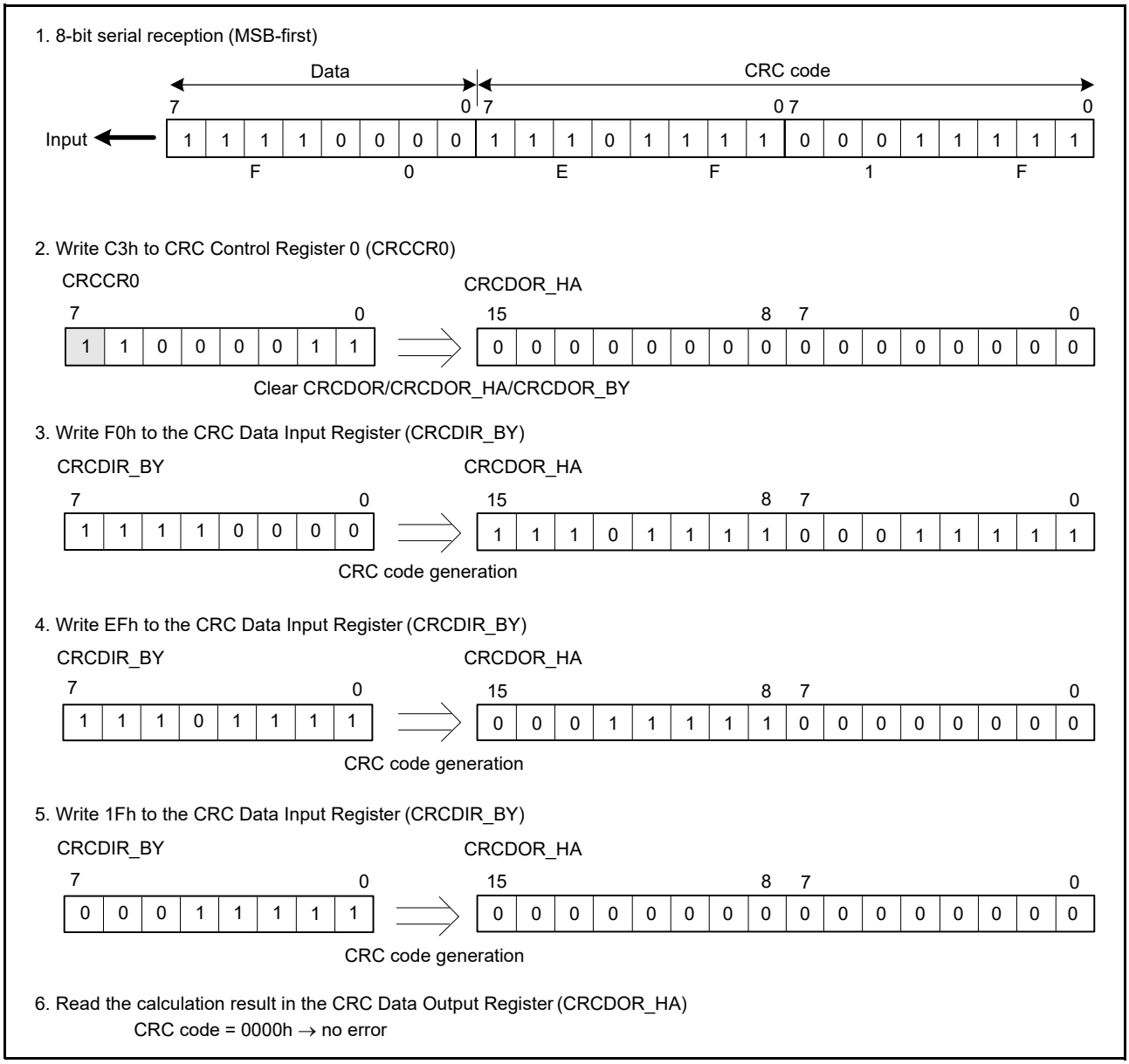


Figure 32.5 MSB-first data reception

32.3.2 CRC Snoop

The CRC snoop function monitors reads from and writes to a specific register address and performs CRC calculation on the data read from and written to that register address automatically. Because the CRC snoop recognizes writes to and reads from a specific register address as a trigger to automatically perform CRC calculation, there is no need to write data to the CRCDIR_BY register. All I/O register addresses specified in the Snoop Address Register (CRCSAR) are subject to the CRC snoop. The CRC snoop is useful in monitoring writes to the serial transmit buffer, and reads from the serial receive buffer.

To use this function, write a target I/O register address to bits CRCSA13 to CRCSA0 in the CRCSAR register, and set CRCSEN bit in the CRCCR1 register to 1. Then, set the CRCSWR bit in the CRCCR1 register to 1 to enable snooping on writes to the target address, or set the CRCSWR bit in the CRCCR1 register to 0 to enable snooping on reads from the target address.

When setting the CRCSEN bit to 1, CRCSWR bit to 1 and writing data to a target I/O register address in a bus master module such as CPU and DTC, the CRC calculator stores the data in the CRCDIR_BY register and performs CRC calculation. Similarly, when setting the CRCSEN bit to 1, CRCSWR bit to 0 and reading data in a target I/O register address in a bus master module such as CPU and DTC, the CRC calculator stores the data in the CRCDIR_BY register

and performs CRC calculation.

CRC calculation is performed 1-byte at a time. When the target I/O register address is accessed in words (16 bits) or long words (32 bits), CRC code is generated on the lower byte (1 byte) of data.

32.4 Usage Notes

32.4.1 Settings for the Module-Stop State

The Module Stop Control Register C (MSTPCRC) can enable or disable CRC calculator operation. The CRC is stopped after a reset. The registers become accessible on release from the module-stop state. For details, see section 10, Low Power Modes.

32.4.2 Note on Transmission

The sequence of transmission for the CRC code differs according to whether transmission is LSB-first or MSB-first.

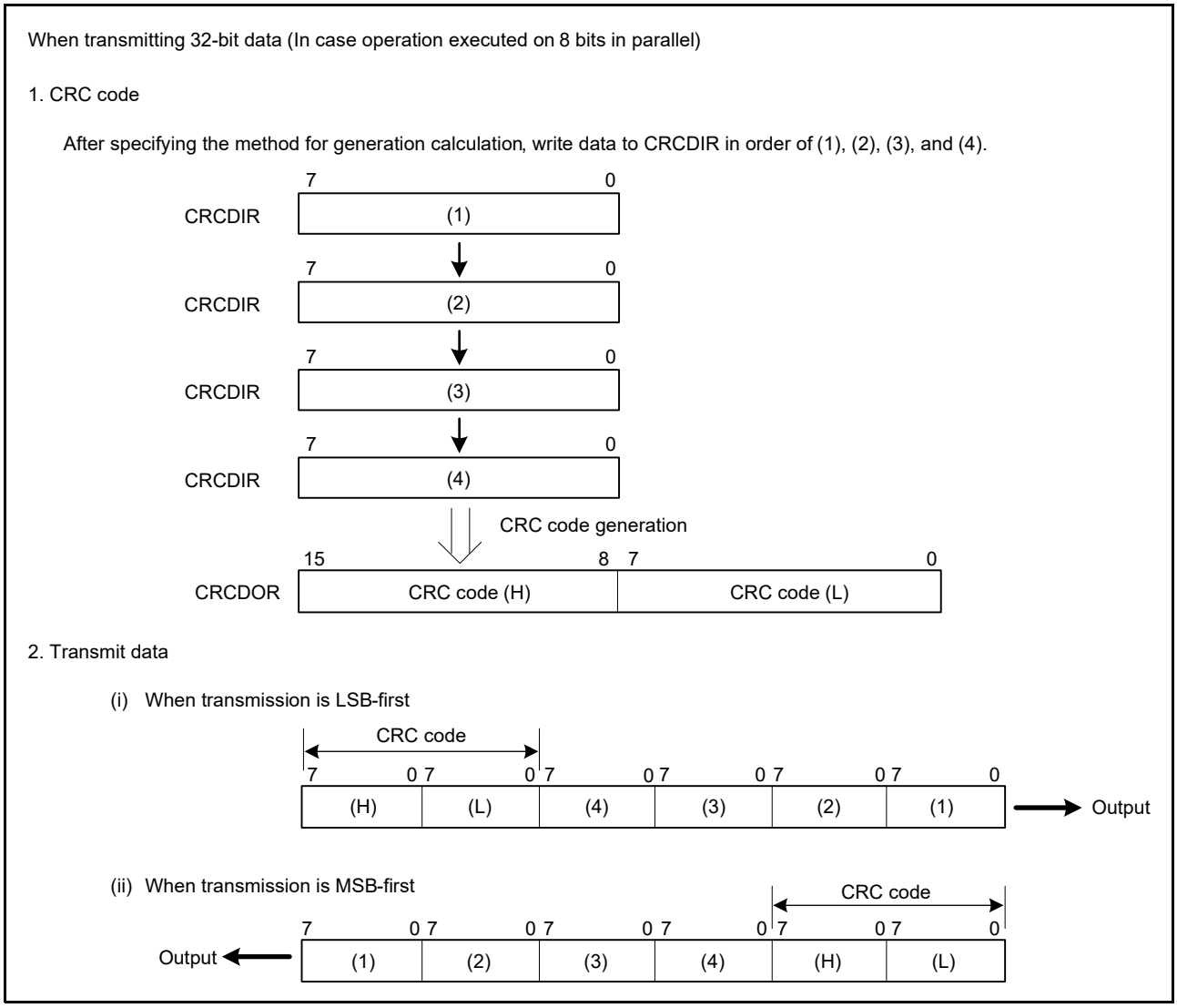


Figure 32.6 LSB-first and MSB-first data transmission

33. 14-Bit A/D Converter (ADC14)

33.1 Overview

The MCU includes a 14-bit successive approximation A/D converter (ADC14). Up to 21 analog input channels are selectable. Temperature sensor output and internal reference voltage are selectable for conversion. The A/D conversion accuracy is selectable from 14-bit conversion, making it possible to optimize the trade-off between speed and resolution in generating a digital value.

The ADC14 supports the following operating modes:

- Single scan mode to convert the analog inputs of arbitrarily selected channels in ascending order of channel number
- Continuous scan mode to sequentially convert the analog inputs of arbitrarily selected channels continuously in ascending order of channel number
- Group scan mode to arbitrarily divide the analog inputs of channels into two groups (group A and group B) and convert the analog input of the selected channel for each group in ascending order of channel number.

In group scan mode, you can start group A and group B A/D conversion at different times by individually selecting their scan start conditions. In addition, when a priority control operation for group A is set, the ADC14 accepts group A scan start during group B A/D conversion, suspending group B conversion. This allows you to assign higher priority to A/D conversion start for group A.

In double trigger mode, the analog input of an arbitrarily selected channel is converted in single scan mode or group scan mode (group A), and the data converted by the first and second A/D conversion start triggers is stored in different registers, providing duplexing of A/D converted data.

Self-diagnosis is performed once at the beginning of each scan, and one of the three voltage values generated in the ADC14 is A/D converted.

The temperature sensor output and internal reference voltage cannot be selected for conversion simultaneously. The temperature sensor output and the internal reference voltage are converted independently.

The ADC14 provides a compare function (window A and window B). This compare function specifies the upper reference value for window A and lower reference value for window B, and outputs an interrupt when the A/D converted value of the selected channel meets the comparison conditions.

The reference power supply pin (VREFH0), the analog block power supply pin (AVCC0), or the internal reference voltage is selectable as the reference voltage on the high-potential side. The reference power supply ground pin (VREFL0) or the analog block power supply ground pin (AVSS0) is selectable as the reference voltage on the low-potential side. If the internal reference voltage is selected as the reference voltage on the high-potential side, A/D conversion of the temperature sensor or the internal reference voltage is prohibited.

Table 33.1 lists the ADC14 specifications, Table 33.2 lists the functions, Figure 33.1 shows a block diagram, and Table 33.3 lists the I/O pins.

Table 33.1 ADC14 specifications (1 of 3)

Parameter	Specifications
Number of units	One unit
Input channels	Up to 21 channels (AN000 to AN013, AN016 to AN022)
Extended analog function	Temperature sensor output, internal reference voltage
A/D conversion method	Successive approximation method
Resolution	14 bits, selectable to 14-bit or 12-bit conversion
Conversion time	0.79 μs/channel, when A/D conversion clock PCLKD (ADCLK) operates at 64 MHz
A/D conversion clock	Peripheral module clock PCLKB*1 and A/D conversion clock PCLKD (ADCLK)*1 can be set with the following division ratios: PCLKB to PCLKD (ADCLK) frequency ratio = 1:1, 1:2, 1:4

Table 33.1 ADC14 specifications (2 of 3)

Parameter	Specifications
Data registers	• 21 registers for analog input: - One register for A/D-converted data duplication in double trigger mode - Two registers for A/D-converted data duplication during extended operation in double trigger mode • One register for temperature sensor output • One register for internal reference voltage • One register for self-diagnosis • The results of A/D conversion are stored in A/D data registers • 12-bit and 14-bit accuracy output for A/D conversion results • A/D-converted value addition mode, in which the sum of all A/D-converted results is stored in the A/D data registers as the conversion accuracy bit count + 2 bits*4 • Double trigger mode, selectable in single scan and group scan modes: - The first unit of A/D-converted analog input data on one selected channel is stored in the data register for the channel, and the second unit is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers): - A/D-converted analog input data on one selected channel is stored in the duplication register provided for the associated trigger.
Operating modes	• Single scan mode: - A/D conversion is performed only once on the analog inputs of arbitrarily selected channels, on the temperature sensor output, and on the internal reference voltage. • Continuous scan mode: - A/D conversion is performed repeatedly on the analog inputs of arbitrarily selected channels, on the temperature sensor output, and on the internal reference voltage. • Group scan mode: - A/D conversion is performed only once on the analog inputs of arbitrarily selected channels on a group basis. - The scan start conditions can be independently selected for group A and group B, allowing A/D conversion of group A and group B to be started independently. • Group scan mode (when group A is given priority): - If a group A trigger is input during A/D conversion on group B, the A/D conversion on group B stops and A/D conversion is performed on group A. - Restart (rescan) of group B conversion after completion of group A conversion can be set.
Conditions for A/D conversion start	• Software trigger • Synchronous trigger from the Event Link Controller (ELC) • Asynchronous trigger from the external trigger pins, ADTRG0.
Functions	• Variable sampling state count • Self-diagnosis of ADC14 • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (discharge and precharge functions) • Double trigger mode (duplication of A/D conversion data) • Switching function of 12-bit and 14-bit conversion*2 • Automatic clear function for A/D data registers • Digital comparison of values in the comparison register and data registers, and between values in the data registers.
Interrupt sources	• In single scan mode (double trigger deselected), an A/D scan end interrupt request and ELC event signal (ADC140_ADI) can be generated on completion of a single scan. - A compare interrupt request (ADC140_CMPAI/ADC140_CMPBI) can be generated in response to matches with a condition for digital comparison. - A window compare ELC event signal (ADC140_WCMPM) can be generated in response to matches with a condition for digital comparison. - A window compare ELC event signal (ADC140_WCMPUM) can be generated in response to mismatches with a condition for digital comparison. • In single scan mode (double trigger selected), an A/D scan end interrupt request and ELC event signal (ADC140_ADI) can be generated on completion of two scans • In continuous scan mode, an A/D scan end interrupt request and ELC event signal (ADC140_ADI) can be generated on completion of all the selected channel scans. • In group scan mode (double trigger deselected), an A/D scan end interrupt request and ELC event signal (ADC140_ADI) can be generated on completion of group A scan, whereas an A/D scan end interrupt request for group B (ADC140_GBADI) can be generated on completion of group B scan • In group scan mode (double trigger selected), an A/D scan end interrupt request and ELC event signal (ADC140_ADI) can be generated on completion of two group A scans, and an A/D scan end interrupt request for group B (ADC140_GBADI) can be generated on completion of group B scan • The ADC140_ADI, ADC140_GBADI, ADC140_WCMPM, and ADC140_WCMPUM can activate the Data Transfer Controller (DTC).
ELC interface	Scan can be started by a trigger from the ELC

Table 33.1 ADC14 specifications (3 of 3)

Parameter	Specifications
Reference voltage	• VREFH0, AVCC0, or internal reference voltage can be selected as the high potential-side reference voltage • VREFL0 or AVSS0 can be selected as the low potential-side reference voltage.
Module-stop function	Module-stop state can be specified*3

Note: When selecting the temperature sensor output or the internal reference voltage, do not use continuous scan mode or group scan mode.

Note 1. Peripheral module clock PCLKB is set in the SCKDIVCR.PCKB[2:0] bits and A/D conversion clock ADCLK is set in the SCKDIVCR.PCKD[2:0] bits. Maximum frequency of PCLKB is 32 MHz and maximum frequency of PCLKD (ADCLK) is 64 MHz.

Note 2. Changing the A/D conversion accuracy also changes the A/D conversion time. For details, see section 33.3.6, Analog Input Sampling and Scan Conversion Time.

Note 3. For details, see section 10, Low Power Modes.

Note 4. The number of extended bits for addition varies with the A/D conversion accuracy and the number of addition times. A 2-bit extension is up to 4 times conversion (3 times addition) when the A/D conversion accuracy is 12 or 14 bits.

Table 33.2 ADC14 functions

Parameter			ADC140
Analog input channel			AN000 to AN013, AN016 to AN022 Internal reference voltage Temperature sensor output
Conditions for A/D conversion start	Software	Software trigger	Enabled
	External trigger	Trigger input pin	ADTRG0
	Synchronous trigger (trigger from ELC)	ELC trigger	ELC_AD00 ELC_AD01
Interrupt			ADC140_ADI ADC140_GBADI ADC140_CMPAI ADC140_CMPBI
Output to ELC			ADC140_ADI ADC140_WCMPM ADC140_WCMPUM
Setting of module stop function*1, *2			MSTPCRD.MSTPD16 bit

Note 1. For details, see section 10, Low Power Modes.

Note 2. Wait for 1 μs or longer to start A/D conversion after release from the module-stop state.

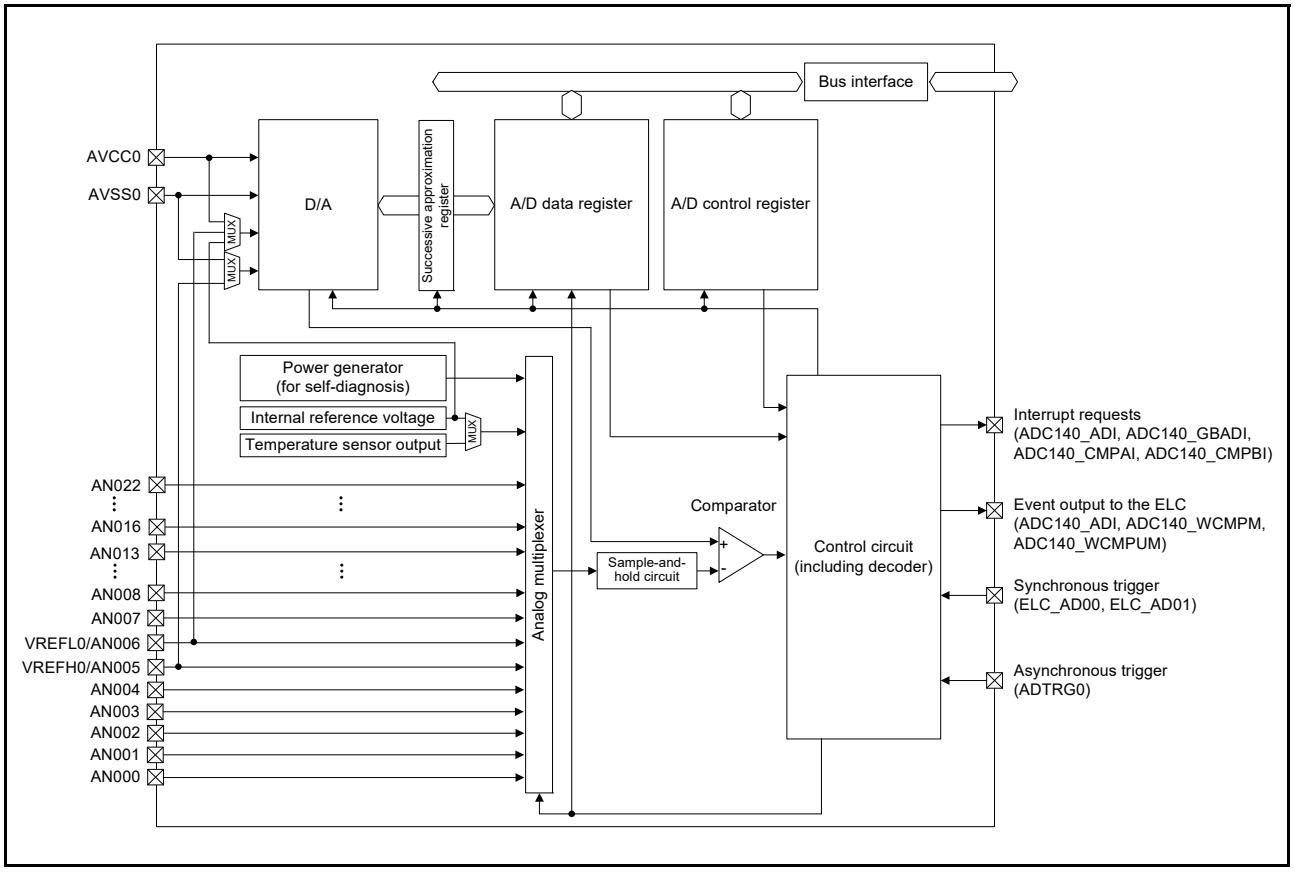


Figure 33.1 ADC14 block diagram

Table 33.3 IADC14 I/O pins

Pin name	I/O	Function
AVCC0	Input	Analog block power supply pin
AVSS0	Input	Analog block power supply ground pin
VREFH0	Input	Reference power supply pin
VREFL0	Input	Reference power supply ground pin
AN000 to AN013, AN016 to AN022	Input	Analog input pins 0 to 13, 16 to 22
ADTRG0	Input	External trigger input pin for starting A/D conversion

33.2 Register Descriptions

33.2.1 A/D Data Registers y (ADDRy), A/D Data Duplexing Register (ADDBLDR), A/D Data Duplexing Register A (ADDBLDRA), A/D Data Duplexing Register B (ADDBLDRB), A/D Temperature Sensor Data Register (ADTSDR), A/D Internal Reference Voltage Data Register (ADOCDR)

The data registers include:

- ADDRy registers (y = 0 to 13, 16 to 22): 16-bit read-only registers for storing the A/D conversion results
- ADDBLDR register: 16-bit read-only register for storing the A/D conversion results in response to the second trigger in double trigger mode
- ADDBLDRA and ADDBLDRB registers: 16-bit read-only registers for storing the A/D conversion results in response to the triggers during extended operation in double trigger mode

- ADTSDR register: 16-bit read-only register for storing the A/D conversion result of temperature sensor output
- ADOCDR register: 16-bit read-only register for storing the A/D conversion result of internal reference voltage.

The following conditions determine the formats for data in these registers:

- The setting in the A/D Data Register Format Select bit (ADCER.ADRFMT) (flush-left or flush-right)
- The setting in the A/D Data Conversion Accuracy Specify bits (ADCER.ADPRC[1:0]) (12- or 14-bit)
- The setting of the Addition/Average Count Select bits (ADADC.ADC[2:0]) (once, twice, three times, four times, or 16 times)
- The setting of the Average Mode Enable bit (ADADC.AVEE) (addition or average).

This section describes the data formats for these conditions in different modes.

(1) When A/D-converted value addition/average mode is not selected

Settings for flush-right data with 14-bit accuracy

Address(es): ADC140.ADDR0 4005 C020h to ADC140.ADDR13 4005 C03Ah, ADC140.ADDR16 4005 C040h to ADC140.ADDR22 4005 C04Ch, ADC140.ADDBLDR 4005 C018h, ADC140.ADDBLDRA 4005 C084h, ADC140.ADDBLDRB 4005 C086h, ADC140.ADTSDR 4005 C01Ah, ADC140.ADOCDR 4005 C01Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	AD[13:0]													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b13 to b0	AD[13:0]	Converted Value 13 to 0	14-bit A/D-converted value	R
b15, b14	—	Reserved	These bits are read as 0	R

Settings for flush-right data with 12-bit accuracy

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	AD[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b11 to b0	AD[11:0]	Converted Value 11 to 0	12-bit A/D-converted value	R
b15 to b12	—	Reserved	These bits are read as 0	R

Settings for flush-left data with 14-bit accuracy

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[13:0]														—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0	R
b15 to b2	AD[13:0]	Converted Value 13 to 0	14-bit A/D-converted value	R

Settings for flush-left data with 12-bit accuracy

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[11:0]												—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0	R
b15 to b4	AD[11:0]	Converted Value 11 to 0	12-bit A/D-converted value	R

(2) When A/D-converted value average mode is selected

A/D-converted value average mode can be selected when 2 or 4 times is specified in the A/D-converted value addition mode. When the A/D-converted value average mode is selected, this register indicates the mean of A/D-converted values on a specific channel. The value is stored in the A/D data register based on the settings of the A/D Data Register Format Select bit in the same way as for normal A/D conversion.

(3) When A/D-converted value addition mode is selected

For 12-bit and 14-bit accuracy (ADPRC bit setting), 1, 2, 3, or 4 times can be selected in the A/D-converted value addition mode. A/D conversion results are stored in the A/D data register as a 2-bit-extended value of the specified conversion accuracy.

When selecting 12-bit accuracy, 16 times can also be selected in the A/D-converted value addition mode. In A/D-converted value addition mode, this register indicates the value that is obtained by adding up A/D converted values on a specific channel. A/D conversion results are stored in the A/D data register as a 4-bit-extended value of the specified conversion accuracy.

When A/D-converted value addition mode is selected, the value is stored in the A/D data register based on the settings of the A/D Data Register Format Select bits.

This section describes the data formats for each condition.

Settings for flush-right data with 14-bit accuracy in A/D-converted value addition mode

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	AD[15:0]	Added Value 15 to 0	16-bit sum of A/D conversion results	R

Settings for flush-right data with 12-bit accuracy in A/D-converted value addition mode

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[15:0]*1															
	—	—	AD[13:0]*2													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	AD[15:0]*1	Added Value 15 to 0	16-bit sum of A/D conversion results	R

Bit	Symbol	Bit name	Description	R/W
b13 to b0	AD[13:0]*2	Added Value 13 to 0	14-bit sum of A/D conversion results	R
b15, b14	—	Reserved	These bits are read as 0	R

Note 1. Used when selecting 16 conversion times in A/D-converted value addition mode.
Note 2. Used when selecting 1, 2, 3 or 4 conversion times in A/D-converted value addition mode.

Settings for flush-left data with 14-bit accuracy in A/D-converted value addition mode

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	AD[15:0]	Added Value 15 to 0	16-bit value sum of A/D conversion results	R

Settings for flush-left data with 12-bit accuracy in A/D-converted value addition mode

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[15:0]*1															
	AD[13:0]*2														—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	AD[15:0]*1	Added Value 15 to 0	16-bit sum of A/D conversion results	R

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0	R
b15 to b2	AD[13:0]*2	Added Value 13 to 0	14-bit sum of A/D conversion results	R

Note 1. Used when selecting 16 conversion times in A/D-converted value addition mode.
Note 2. Used when selecting 1, 2, 3 or 4 conversion times in A/D-converted value addition mode.

33.2.2 A/D Self-Diagnosis Data Register (ADRD)

The ADRD register is a 16-bit read-only register that holds the A/D conversion results based on the self-diagnosis of the ADC14. In addition to the AD[13:0] bits that indicate the A/D-converted value, the ADRD register includes the Self-Diagnosis Status bit (DIAGST).

The following conditions determine the format for data in this register:

- The setting of the A/D Data Register Format Select bit (ADCER.ADRFMT) (flush-left or flush-right)
- The setting of the A/D Data Conversion Accuracy Specify bits (ADCER.ADPRC[1:0]) (12-bit or 14-bit).

The A/D-converted value addition and average modes cannot be applied to the A/D self-diagnosis function. For details on self-diagnosis, see section 33.2.11, A/D Control Extended Register (ADCER).

This section describes the data formats for each condition.

Settings for flush-right data with 14-bit accuracy

Address(es): ADC140.ADRD 4005 C01Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DIAGST[1:0]		AD[13:0]													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b13 to b0	AD[13:0]	Converted Value 13 to 0	14-bit A/D-converted value	R
b15, b14	DIAGST[1:0]	Self-Diagnosis Status	b15 b14 0 0: Self-diagnosis has not been executed since power-on 0 1: Self-diagnosis was execute using 0 volts 1 0: Self-diagnosis was executed using the reference power supply*1 voltage × 1/2 1 1: Self-diagnosis was executed using the reference power supply*1 voltage. For details on self-diagnosis, see section 33.2.11, A/D Control Extended Register (ADCER).	R

Note 1. Reference voltage refers to VREFH0.

Settings for flush-right data with 12-bit accuracy

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DIAGST[1:0]		—	—	AD[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b11 to b0	AD[11:0]	Converted Value 11 to 0	12-bit A/D-converted value	R
b13, b12	—	Reserved	These bits are read as 0	R
b15, b14	DIAGST[1:0]	Self-Diagnosis Status	b15 b14 0 0: Self-diagnosis has not been executed since power-on 0 1: Self-diagnosis was executed using the voltage of 0 V 1 0: Self-diagnosis was executed using the voltage of reference power supply*1 × 1/2 1 1: Self-diagnosis was executed using the voltage of reference power supply*1. For details on self-diagnosis, see section 33.2.11, A/D Control Extended Register (ADCER).	R

Note 1. Reference voltage refers to VREFH0.

Settings for flush-left data with 14-bit accuracy

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[13:0]														DIAGST[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	DIAGST[1:0]	Self-Diagnosis Status	b1 b0 0 0: Self-diagnosis has not been executed since power-on 0 1: Self-diagnosis was executed using the voltage of 0 V 1 0: Self-diagnosis was executed using the voltage of reference power supply*1 × 1/2 1 1: Self-diagnosis was executed using the voltage of reference power supply*1. For details on self-diagnosis, see section 33.2.11, A/D Control Extended Register (ADCER).	R
b15 to b2	AD[13:0]	Converted Value 13 to 0	14-bit A/D-converted value	R

Note 1. Reference voltage refers to VREFH0.

Settings for flush-left data with 12-bit accuracy

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[11:0]												—	—	DIAGST[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	DIAGST[1:0]	Self-Diagnosis Status	b1 b0 0 0: Self-diagnosis has not been executed since power-on 0 1: Self-diagnosis was executed using the voltage of 0 V 1 0: Self-diagnosis was executed using the voltage of reference power supply*1 × 1/2 1 1: Self-diagnosis was executed using the voltage of reference power supply*1. For details on self-diagnosis, see section 33.2.11, A/D Control Extended Register (ADCER).	R
b3, b2	—	Reserved	These bits are read as 0	R
b15 to b4	AD[11:0]	Converted Value 11 to 0	12-bit A/D-converted value	R

Note 1. Reference voltage refers to VREFH0.

33.2.3 A/D Control Register (ADCSR)

Address(es): ADC140.ADCSR 4005 C000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ADST	ADCS[1:0]		—	—	ADHSC	TRGE	EXTRG	DBLE	GBADIE	—	DBLANS[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	DBLANS[4:0]	Double Trigger Channel Select	These bits select one analog input channel for double triggered operation. The setting is only valid in double trigger mode.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	GBADIE	Group B Scan End Interrupt Enable	0: Disable ADC140_GBADI interrupt generation on group B scan completion 1: Enable ADC140_GBADI interrupt generation on group B scan completion. Group B scan works only in group scan mode.	R/W
b7	DBLE	Double Trigger Mode Select	0: Deselect double trigger mode 1: Select double trigger mode.	R/W
b8	EXTRG	Trigger Select*1	0: Start A/D conversion by a synchronous trigger (ELC) 1: Start A/D conversion by the asynchronous trigger (ADTRG0).	R/W
b9	TRGE	Trigger Start Enable	0: Disable A/D conversion to be started by a synchronous or asynchronous trigger 1: Enable A/D conversion to be started by a synchronous or asynchronous trigger.	R/W
b10	ADHSC	A/D Conversion Mode Select	0: High-speed A/D conversion mode 1: Low-power A/D conversion mode.	R/W
b12, b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b14, b13	ADCS[1:0]	Scan Mode Select	b14 b13 0 0: Single scan mode 0 1: Group scan mode 1 0: Continuous scan mode 1 1: Setting prohibited.	R/W
b15	ADST	A/D Conversion Start	0: Stop A/D conversion process 1: Start A/D conversion process.	R/W

Note 1. To start A/D conversion using an external pin (asynchronous trigger):
After a high-level signal is input to the external pin (ADTRG0), write 1 to both the TRGE and EXTRG bits in the ADCSR register and drive the ADTRG0 signals low. With these settings, the scan conversion process starts on detection of the falling edge on ADTRG0. The pulse width of the low-level input must be at least 1.5 clock cycles of PCLKB.

DBLANS[4:0] bits (Double Trigger Channel Select)

The DBLANS[4:0] bits select one of the channels for A/D conversion data duplication in double trigger mode. The A/D conversion results of the analog input of the channel selected in the DBLANS[4:0] bits are stored in the A/D Data Register y when conversion is started by the first trigger, and in the A/D Data Duplexing Register when conversion is tarted by the second trigger. Table 33.4 shows the channel selection settings for double triggered operation.

A/D-converted value addition/average mode with double trigger mode can be set by selecting the channel using the DBLANS[4:0] bits of the ADADS0/1 register. In double trigger mode, the channels selected in the ADANSA0 and ADANSA1 registers are invalid, and the channel selected by the DBLANS[4:0] bits is subjected to A/D conversion instead.

When double trigger mode is used in group scan mode, double trigger control is only applied to group A and not to group B. Therefore, multiple channel analog input can be selected for group B even in double trigger mode.

Only set the DBLANS[4:0] bits when the ADST bit is 0. Do not set the DBLANS[4:0] bits at the same time that you write 1 to the ADST bit.

To enter A/D-converted value addition/average mode when in double trigger mode, select the channel using the DBLANS[4:0] bits in the ADANSA0 and ADANSA1 registers.

Table 33.4 Relationship between DBLANS bit settings and double-trigger enabled channels

DBLANS[4:0]	Duplication channel	DBLANS[4:0]	Duplication channel
00000	AN000	10000	AN016
00001	AN001	10001	AN017
00010	AN002	10010	AN018
00011	AN003	10011	AN019
00100	AN004	10100	AN020
00101	AN005	10101	AN021
00110	AN006	10110	AN022
00111	AN007	10111	—
01000	AN008	11000	—
01001	AN009	11001	—
01010	AN010	11010	—
01011	AN011	11011	—
01100	AN012	11100	—
01101	AN013	11101	—
01110	—	11110	—
01111	—	11111	—

Note 1. A/D-converted data from the self-diagnosis function, temperature sensor output, and internal reference voltage cannot be used in double trigger mode.

GBADIE bit (Group B Scan End Interrupt Enable)

The GBADIE bit enables or disables group B scan end interrupt (ADC140_GBADI) in group scan mode.

DBLE bit (Double Trigger Mode Select)

The DBLE bit selects or deselects double trigger mode. Double trigger mode can only be operated by the synchronous trigger (ELC) selected in the ADSTRGR.TRSA[5:0] bits. The operation of double trigger mode is as follows:

1. The ADC140_ADI interrupt is output not on completion of the first conversion but on completion of the second conversion.
2. The A/D conversion results from the duplication channel (selected in DBLANS[4:0] bits) started by the first trigger are stored in the A/D Data Register y and those started by the second trigger are stored in the A/D Data Duplication register.

When the DBLE bit is set (double trigger mode is selected), the channels specified in the ADANSA0 and ADANSA1 registers are invalid. Double trigger mode is deselected by setting DBLE to 0. When DBLE is set to 1 again, the double trigger mode operation is the same as the first time scanning with the first trigger.

Do not select double trigger mode in continuous scan mode. Software triggering cannot be used in double trigger mode. Always set the ADST bit to 0 before setting the DBLE bit. Do not set the DBLE bit at the same time as writing 1 to the ADST bit.

EXTRG bit (Trigger Select)

The EXTRG bit selects the synchronous trigger or asynchronous trigger as the trigger for starting A/D conversion.

TRGE bit (Trigger Start Enable)

The TRGE bit enables or disables A/D conversion by the synchronous trigger and the asynchronous trigger. In group scan mode, set this bit to 1.

ADHSC bit (A/D Conversion Mode Select)

The ADHSC bit selects either high speed mode or low current mode for A/D conversion.

For details on how to rewrite this bit, see section 33.8.8, ADHSC Bit Rewriting Procedure.

ADCS[1:0] bits (Scan Mode Select)

The ADCS [1:0] bits select the scan mode.

In single scan mode, A/D conversion is performed for the analog inputs of a maximum of 21 channels selected with the ADANSA0 and ADANSA1 registers, in ascending order of channel number. When 1 cycle of A/D conversion completes for all the selected channels, the scan conversion stops.

In continuous scan mode, when the ADST bit in ADCSR is 1, A/D conversion is performed for the analog inputs of the channels selected with the ADANSA0 and ADANSA1 registers, in ascending order of channel number. When 1 cycle of A/D conversion completes for all the selected channels, A/D conversion repeats from the first channel. If the ADST bit in ADCSR is set to 0 during continuous scan, A/D conversion stops even when scanning is in progress.

In group scan mode:

- Group A scanning is started by the synchronous trigger (ELC) selected in the TRSA[5:0] bits in the ADSTRGR register. A/D conversion is performed on group A analog inputs of a maximum numbers of channels selected with the ADANSA0 and ADANSA1 registers, in ascending order of channel number. When 1 cycle of A/D conversion completes for all the selected channels, A/D conversion stops.
- Group B scanning is started by the synchronous trigger (ELC) selected by the TRSB[5:0] bits in the ADSTRGR register. A/D conversion is performed on group B analog inputs of a maximum of 21 channels selected with the ADANSB0 and ADANSB1 registers, in ascending order of channel number. When 1 cycle of A/D conversion completes for all the selected channels, A/D conversion stops.

If the conversion processes in group A and B occur at the same time, those conversions cannot be controlled separately. In this case, set the group A priority control setting bit (ADGSPCR.PGS) in the A/D group Scan Priority Control Register (ADGSPCR) to 1, to assign a priority to group A conversion.

In group scan mode, select different channels and triggers for group A and group B.

When selecting temperature sensor output or internal reference voltage, select single scan mode, and perform A/D conversion after deselecting all analog input channels in the ADANSA0 and ADANSA1 registers. When A/D conversion of the temperature sensor output or internal reference voltage completes, A/D conversion stops.

Only set the ADCS[1:0] bits when the ADST bit is 0. Do not set the ADCS[1:0] bits at the same time that you write 1 to the ADST bit.

Table 33.5 Selectable targets for A/D Conversion depending on settings of scan mode and double trigger mode

Scan mode setting	Double trigger mode setting	Targets for A/D conversion				
		Self-diagnosis	Analog input (including group A)	Analog input (group B)	Temperature sensor output	Internal reference voltage
Single scan	DBLE = 0	✓	✓	×	✓	✓
	DBLE = 1	×	✓ (1 ch only)	×	×	×
Continuous scan	DBLE = 0	✓	✓	×	×	×
	DBLE = 1	×	×	×	×	×
Group scan	DBLE = 0	✓	✓	✓	×	×
	DBLE = 1	×	✓ (1 ch only)	✓	×	×

✓: Selectable. ×: Not selectable.

ADST bit (A/D Conversion Start)

The ADST bit starts or stops the A/D conversion process. Before the ADST bit is set to 1, set the A/D conversion clock, the conversion mode, and conversion target analog input.

[Setting conditions]

- 1 is written by software
- The synchronous trigger (ELC) selected in the ADSTRGR.TRSA[5:0] bits is detected when the ADCSR.EXTRG bit is 0 and the ADCSR.TRGE bit is 1
- The synchronous trigger (ELC) selected in the ADSTRGR.TRSB[5:0] bits is detected when the ADCSR.TRGE bit is set to 1 in group scan mode
- The asynchronous trigger is detected when the ADCSR.TRGE and ADCSR.EXTRG bits are set to 1 and the ADSTRGR.TRSA[5:0] bits set to 000000b
- With group A priority control operation mode enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), the ADGSPCR.GBRP bit is set to 1 and each time A/D conversion of group B starts.

[Clearing conditions]

- 0 is written by software
- A/D conversion of all the selected channels, the temperature sensor output, or the internal reference voltage completes in single scan mode
- Group A scan completes in group scan mode
- Group B scan completes in group scan mode
- With group A priority control operation mode enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1) the ADGSPCR.GBRP bit is set to 1 and each time a scanning of group B completes.

Note: When group A priority control operation mode is enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), do not set the ADST bit to 1.

Note: When group A priority control operation mode is enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), do not set the ADST bit to 0. When forcing A/D conversion to terminate, follow the procedure for clearing the ADST bit.

Note: If the single scan continuous function is used (ADGSPCR.GBRP = 1) when the group priority operation mode is enabled (ADCSR.ADCS[1:0] = 01b and ADGSPCR.PGS = 1), the ADST bit remains 1.

33.2.4 A/D Channel Select Register A0 (ADANSA0)

Address(es): ADC140.ADANSA0 4005 C004h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	ANSA13	ANSA12	ANSA11	ANSA10	ANSA09	ANSA08	ANSA07	ANSA06	ANSA05	ANSA04	ANSA03	ANSA02	ANSA01	ANSA00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b13 to b0	ANSA13 to ANSA00	A/D Conversion Channels Select	0: Associated input channel not selected 1: Associated input channel selected. Bit [13] (ANSA13) is associated with AN013 and bit [0] (ANSA00) is associated with AN000.	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ANSAn bits (n = 00 to 13) (A/D Conversion Channels Select)

The ADANSA0 register selects any combination of analog input channels from AN000 to AN013 for A/D conversion. The channels and the number of channels can be arbitrarily set. The ANSA00 bit is associated with AN000 and the ANSA13 bit is associated with AN013.

When performing A/D conversion of temperature sensor output or internal reference voltage, set the ADANSA0 register to 0000h to deselect all analog input channels.

In double trigger mode, the channel selected by the ADANSA0 register is invalid, and the channel selected by the ADCSR.DBLANS[4:0] bits is selected in group A instead.

When group scan mode is selected, do not select the channels specified in A/D channel select register B0 (ADANSB0) and A/D channel select register B1 (ADANSB1).

Only set the ADANSA0 register when the ADCSR.ADST bit is 0.

33.2.5 A/D Channel Select Register A1 (ADANSA1)

Address(es): ADC140.ADANSA1 4005 C006h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	ANSA22	ANSA21	ANSA20	ANSA19	ANSA18	ANSA17	ANSA16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b6 to b0	ANSA22 to ANSA16	A/D Conversion Channels Select	0: Associated input channel not selected 1: Associated input channel selected. Bit [6] (ANSA22) is associated with AN022 and bit [0] (ANSA16) is associated with AN016.	R/W
b15 to b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ANSAn bits (n = 16 to 22) (A/D Conversion Channels Select)

The ADANSA1 register selects any combination of analog input channels from AN016 to AN022 for A/D conversion. The channels and the number of channels can be arbitrarily set. The ANSA16 bit is associated with AN016 and the ANSA22 bit is associated with AN022. In double trigger mode, the ANSA1[15:7] bits are invalid, and the channel selected by the ADCSR.DBLANS[4:0] bits is selected in group A instead.

When performing A/D conversion of temperature sensor output or internal reference voltage, set the ADANSA1 register to 0000h to deselect all analog input channels.

When group scan mode is selected, do not select the channels specified in A/D Channel Select Register B0 (ADANSB0) and A/D Channel Select Register B1 (ADANSB1).

Only set the ADANSA1 register when the ADCSR.ADST bit is 0.

33.2.6 A/D Channel Select Register B0 (ADANSB0)

Address(es): ADC140.ADANSB0 4005 C014h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	ANSB13	ANSB12	ANSB11	ANSB10	ANSB09	ANSB08	ANSB07	ANSB06	ANSB05	ANSB04	ANSB03	ANSB02	ANSB01	ANSB00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b13 to b0	ANSB13 to ANSB00	A/D Conversion Channels Select	0: Associated input channel not selected 1: Associated input channel selected. Bit [13] (ANSB13) is associated with AN013 and bit [0] (ANSB00) is associated with AN000.	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ANSBn bits (n = 00 to 13) (A/D Conversion Channels Select)

The ADANSB0 register selects any combination of analog input channels from AN000 to AN013 for A/D conversion in group B when group scan mode is selected. The ADANSB0 register is used for group scan mode only and not for any

other modes.

Do not select channels specified in group A as selected in the ADANSA0 and ADANSA1 registers and the ADCSR.DBLANS[4:0] bits in double trigger mode.

The ANSB00 bit is associated with AN000, the ANSB07 bit is associated with AN007, and the ANSB13 bit is associated with AN013.

When selecting temperature sensor output or internal reference voltage, set the ADANSB0 register to 0000h to deselect all analog input channels.

Only set the ADANSB register when the ADCSR.ADST bit is 0.

33.2.7 A/D Channel Select Register B1 (ADANSB1)

Address(es): ADC140.ADANSB1 4005 C016h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	ANSB22	ANSB21	ANSB20	ANSB19	ANSB18	ANSB17	ANSB16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b6 to b0	ANSB22 to ANSB16	A/D Conversion Channels Select	0: Associated input channel not selected 1: Associated input channel selected. Bit [6] (ANSB22) is associated with AN022 and bit [0] (ANSB16) is associated with AN016.	R/W
b15 to b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ANSBn bits (n = 16 to 22) (A/D Conversion Channels Select)

The ADANSB1 register selects any combination of analog input channels from AN016 to AN022 for A/D conversion in group B when group scan mode is selected. The ADANSB1 register is used for group scan mode only and not for any other modes.

Do not select channels specified in group A (as selected with the ADANSA0 and ADANSA1 registers and the ADCSR.DBLANS[4:0] bits in double trigger mode).

The ANSB16 bit is associated with AN016, the ANSB20 bit is associated with AN020, and the ANSB22 bit is associated with AN022.

When selecting temperature sensor output or internal reference voltage, set the ADANSB1 register to 0000h to deselect all analog input channels.

Only set the ADANSB1 register bits when the ADST bit is 0.

33.2.8 A/D-Converted Value Addition/Average Channel Select Register 0 (ADADS0)

Address(es): ADC140.ADADS0 4005 C008h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	ADS13	ADS12	ADS11	ADS10	ADS09	ADS08	ADS07	ADS06	ADS05	ADS04	ADS03	ADS02	ADS01	ADS00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b13 to b0	ADS13 to ADS00	A/D-Converted Value Addition/ Average Channel Select	0: Associated input channel not selected 1: Associated input channel selected. Bit [13] (ADS13) is associated with AN013 and bit [0] (ADS00) is associated with AN000.	R/W

Bit	Symbol	Bit name	Description	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ADSn bits (n = 00 to 13) (A/D-Converted Value Addition/Average Channel Select)

The ADSn bits determine which A/D-converted channels from AN000 to AN013 are subject to A/D-converted value addition/averaging. When an ADSn bit associated with a channel selected for A/D conversion is set to 1, A/D conversion of the analog input of the selected channels is performed successively 1 to 16 times, as specified in the ADC[2:0] bits in the ADADC register.

When the ADADC.AVEE bit is 0, the value obtained by addition is stored in the A/D data register. When the ADADC.AVEE bit is 1, the mean value of the results obtained by addition is stored in the A/D data register.

The ADSn bits apply only to channels that are selected for A/D conversion in:

- The ANSAn bits (n = 00 to 13) in the ADANSA0 register or the DBLANS[4:0] bits in the ADCSR register
- The ANSBn bits (n = 00 to 13) in the ADANSB0 register.

For channels on which the A/D conversion is performed and for which addition/average mode is not selected, a normal 1-time conversion is executed and the conversion result is stored in the A/D data register.

Only set the ADADS0 register bits when the ADCSR.ADST bit is 0.

33.2.9 A/D-Converted Value Addition/Average Channel Select Register 1 (ADADS1)

Address(es): ADC140.ADADS1 4005 C00Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	ADS22	ADS21	ADS20	ADS19	ADS18	ADS17	ADS16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b6 to b0	ADS22 to ADS16	A/D-Converted Value Addition/Average Channel Select	0: Associated input channel not selected 1: Associated input channel selected. Bit [6] (ADS22) is associated with AN022 and bit [0] (ADS16) is associated with AN016.	R/W
b15 to b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ADSn bits (n = 16 to 22) (A/D-Converted Value Addition/Average Channel Select)

The ADSn bits determine which A/D-converted channels from AN016 to AN022 are subject to A/D-converted value addition/averaging. When an ADSn bit associated with a channel selected for A/D conversion is set to 1, A/D conversion of the analog input of the selected channels is performed successively 1 to 16 times, as specified in the ADC[2:0] bits in the ADADC register.

When the ADADC.AVEE bit is 0, the value obtained by addition is stored in the A/D data register. When the ADADC.AVEE bit is 1, the mean value of the results obtained by addition is stored in the A/D data register.

The ADSn bits apply only to channels that are selected for A/D conversion in:

- The ANSAn bits (n = 16 to 22) in the ADANSA1 register or the DBLANS[4:0] bits in the ADCSR register
- The ANSBn bits (n = 16 to 22) in the ADANSB1 register.

For channels on which the A/D conversion is performed and for which addition/average mode is not selected, a normal 1-time conversion is executed and the conversion result is stored in the A/D data register.

Only set the ADADS1 register when the ADCSR.ADST bit is 0.

Figure 33.2 shows a scanning operation sequence in which both the ADADS0.ADS02 and ADADS0.ADS06 bits are set to 1. In this figure:

- Addition mode is selected (ADADS.AVEE = 0)

- The number of conversions is set to 4 (ADADC.ADC[1:0] = 11b)
- Channels AN000 to AN007 are selected (ADANSA0.ANSA0[15:0] = 00FFh) in continuous scan mode (ADCSR.ADCS[1:0] = 10b).

The conversion process begins with AN000. The AN002 conversion is performed successively 4 times and the added value is returned to A/ D Data Register 2 (ADDR2). Next, the AN003 conversion process is started. The AN006 conversion is performed successively 4 times and the added value is returned to A/D Data Register 6 (ADDR6). After conversion of AN007, the conversion operation repeats in the same sequence with AN000.

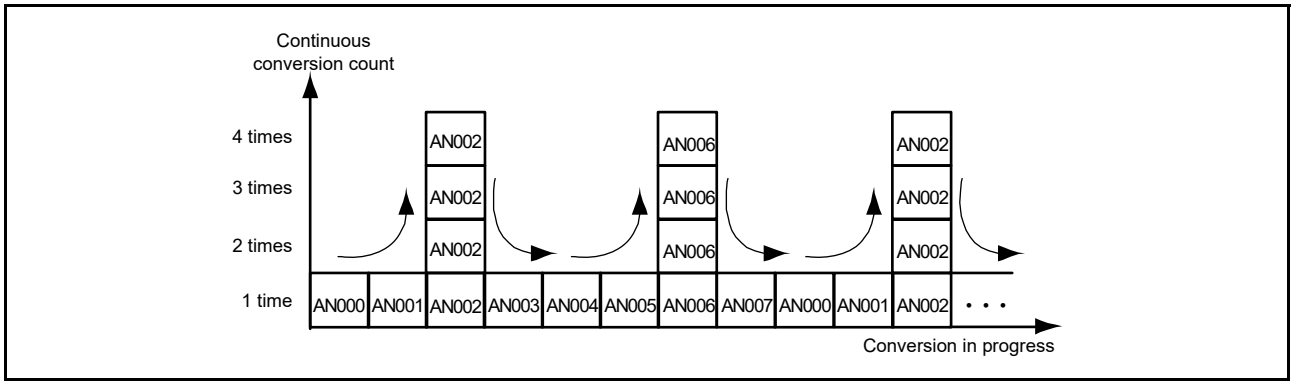


Figure 33.2 Scan conversion sequence with ADADC.ADC[2:0] = 011b, ADADS0.ADS02 = 1, ADADS0.ADS06 = 1

33.2.10 A/D-Converted Value Addition/Average Count Select Register (ADADC)

Address(es): ADC140.ADADC 4005 C00Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	AVEE	—	—	—	—	ADC[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	ADC[2:0]	Count Select	b2 b0 0 0 0: 1-time conversion (no addition: same as normal conversion) 0 0 1: 2-time conversion (one addition) 0 1 0: 3-time conversion (two additions) 0 1 1: 4-time conversion (three additions) 1 0 1: 16-time conversion (15 additions). Other settings are prohibited.	R/W
b6 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	AVEE	Average Mode Enable	0: Average mode disabled*1 1: Average mode enabled.*2	R/W

Note 1. When average mode is deselected by setting the ADADC.AVEE bit to 0, set addition count to 1, 2, 3, 4 or 16-time conversion. 16-time conversion can only be used in 12-bit accuracy.

Note 2. When average mode is selected by setting the ADADC.AVEE bit to 1, set addition count to 2-time or 4-time conversion. Do not set the addition count to 3-time or 16-time conversion (ADC[2:0] = 010b and 101b).

ADC[2:0] bits (Count Select)

The ADC[2:0] bits set the addition count for all channels for which A/D conversion and A/D-converted value addition/average mode are selected, including the channels selected in double trigger mode with the ADCSR.DBLANS[4:0] bits. The count also applies to A/D conversion of the temperature sensor output and internal reference voltage.

The following restrictions apply to the setting of the ADC[2:0] bits:

- When average mode is selected by setting the ADADC.AVEE bit to 1, do not set the addition count to 3-time conversion (ADADC.ADC[2:0] = 010b)
- The combination of the addition count 16-time conversion (ADADC.ADC[2:0] = 101b) with the 14-bit conversion accuracy (ADCER.ADPRC[1:0] = 11b) is not allowed as described in section 33.2.1
- When self-diagnosis is executed (ADCER.DIAGM = 1), do not set the ADC[2:0] bits to any value other than 000b
- For 14-bit conversion accuracy (ADCER.ADPRC[1:0] = 11b), do not set the ADC[2:0] bits to 101b.

Only set the ADC[2:0] bits when the ADCSR.ADST bit is 0.

AVEE bit (Average Mode Enable)

The AVEE bit selects addition or average mode for all channels for which A/D conversion and A/D-converted value addition/average mode are selected, including the channels selected for double trigger mode in the ADCSR.DBLANS[4:0] bits, temperature sensor output, and internal reference voltage.

When average mode is selected by setting the ADADC.AVEE bit to 1, do not set the addition count to 3-time conversion (ADADC.ADC[2:0] = 010b).

Only set the AVEE bits when the ADCSR.ADST bit is 0.

33.2.11 A/D Control Extended Register (ADCER)

Address(es): ADC140.ADCER 4005 C00Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ADRFMT	—	—	—	DIAGM	DIAGLD	DIAGVAL[1:0]		—	—	ACE	—	—	ADPRC[1:0]		—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b2, b1	ADPRC[1:0]	A/D Conversion Accuracy Specify	b2 b1 0 0: 12-bit accuracy 0 1: Setting Prohibited 1 0: Setting Prohibited 1 1: 14-bit accuracy.	R/W
b4, b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	ACE	A/D Data Register Automatic Clearing Enable	0: Automatic clearing disabled 1: Automatic clearing enabled.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9, b8	DIAGVAL[1:0]	Self-Diagnosis Conversion Voltage Select	b9 b8 0 0: Setting prohibited when self-diagnosis is enabled 0 1: 0 volts 1 0: Reference power supply*1 voltage × 1/2 1 1: Reference power supply*1 voltage.	R/W
b10	DIAGLD	Self-Diagnosis Mode Select	0: Rotation mode for self-diagnosis voltage 1: Fixed mode for self-diagnosis voltage.	R/W
b11	DIAGM	Self-Diagnosis Enable	0: Self-diagnosis of ADC14 disabled 1: Self-diagnosis of ADC14 enabled.	R/W
b14 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	ADRFMT	A/D Data Register Format Select	0: Flush-right selected for the A/D data register format 1: Flush-left selected for the A/D data register format.	R/W

Note 1. Reference voltage refers to VREFH0.

ADPRC[1:0] bits (A/D Conversion Accuracy Specify)

The ADPRC[1:0] bits select either 12 bits or 14 bits for the A/D conversion accuracy. Changing the A/D conversion

accuracy also changes the bit width of the effective data stored in the result register and A/D conversion time. For details, see section 33.3.6, Analog Input Sampling and Scan Conversion Time.

Only set the ADPRC[1:0] bits when the ADCSR.ADST bit is 0.

ACE bit (A/D Data Register Automatic Clearing Enable)

The ACE bit enables or disables automatic clearing (all 0) of the ADDRy, ADRD, ADDBLDR, ADDBLDRA, ADDBLDRB, ADTSDR, or ADOCDR register after any of these registers is read by the CPU or DTC. Automatic clearing of the A/D data registers enables detection of failures that are not updated in the A/D data registers. For details, see section 33.3.7, Usage Example of A/D Data Register Automatic Clearing Function.

DIAGVAL[1:0] bits (Self-Diagnosis Conversion Voltage Select)

The DIAGVAL[1:0] bits select the voltage value used in self-diagnosis voltage fixed mode. For details, see the ADCER.DIAGLD bit description.

Do not execute self-diagnosis by setting the ADCER.DIAGLD bit to 1 when the ADCER.DIAGVAL[1:0] bits are set to 00b.

DIAGLD bit (Self-Diagnosis Mode Select)

The DIAGLD bit selects whether the three voltage values are rotated or the fixed voltage is used in self-diagnosis.

Setting the DIAGLD bit to 0 selects conversion of the voltages in rotation mode where 0 V, the reference power supply voltage × 1/2, and the reference power supply voltage are converted, in that order. After reset and when the self-diagnosis voltage rotation mode is selected, self-diagnosis is executed from 0 V. The self-diagnosis voltage value does not return to 0 V when scan conversion completes. When scan conversion is restarted, rotation starts at the voltage value following the previous value.

Setting the DIAGLD bit to 1 selects fixed voltage, in which the fixed voltage specified in the ADCER.DIAGVAL[1:0] bits is converted. If fixed mode is switched to rotation mode, rotation starts at the fixed voltage value

Only set the DIAGLD bit when the ADCSR.ADST bit is 0.

DIAGM bit (Self-Diagnosis Enable)

The DIAGM bit enables or disables self-diagnosis.

Self-diagnosis is used to detect a failure of the ADC14. In self-diagnosis mode, one of the three voltage values (0 V, the reference power supply voltage × 1/2, or the reference power supply voltage) is converted. When conversion completes, information on the converted voltage and the conversion result is stored in the A/D Self-Diagnosis Data Register (ADRD). The ADRD register can be read out by software to determine whether the conversion result falls within the normal or abnormal range.

Self-diagnosis is executed once at the beginning of each scan, and one of the three voltages is converted. In double trigger mode (ADCSR.DBLE = 1), self-diagnosis (DIAGM = 0) is deselected. When self-diagnosis is selected in group scan mode, self-diagnosis is executed separately for group A and group B.

Only set the DIAGM bit when the ADCSR.ADST bit is 0.

ADRFMT bit (A/D Data Register Format Select)

The ADRFMT bit specifies flush-right or flush-left for data to be stored in the ADDRy, ADDBLDR, ADDBLDRA, ADDBLDRB, ADTSDR, ADOCDR, ADCMPDR0/1, ADWINLLB, ADWINULB or ADRD register.

Only set the ADRFMT bit when the ADCSR.ADST bit is 0.

33.2.12 A/D Conversion Start Trigger Select Register (ADSTRGR)

Address(es): ADC140.ADSTRGR 4005 C010h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	TRSA[5:0]						—	—	TRSB[5:0]					
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b5 to b0	TRSB[5:0]	A/D Conversion Start Trigger Select for Group B	Select the A/D conversion start trigger for group B in group scan mode	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13 to b8	TRSA[5:0]	A/D Conversion Start Trigger Select	Select the A/D conversion start trigger in single scan mode and continuous mode. In group scan mode, the A/D conversion start trigger for group A is selected.	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TRSB[5:0] bits (A/D Conversion Start Trigger Select for Group B)

The TRSB[5:0] bits select the trigger to start scanning of the analog input selected in group B. The TRSB[5:0] bits must only be set in group scan mode and are not used in any other scan mode. Software trigger or asynchronous trigger cannot be used as the scan conversion start trigger for group B. In group scan mode, set the TRSB[5:0] bits to a value other than 000000b and set the ADCSR.TRGE bit to 1.

When group A is given priority in group scan mode, setting the ADGSPCR.GBRP bit to 1 allows group B to continuously operate in single scan mode. When setting the ADGSPCR.GBRP bit to 1, set the TRSB[5:0] bits to 3Fh. The issuance period for a conversion trigger must be more than or equal to the actual scan conversion time (tSCAN). If the issuance period is less than tSCAN, A/D conversion by the trigger might have no effect.

When the GPT module is selected as an A/D conversion start trigger, a delay for synchronization processing occurs. For details, see section 33.3.6, Analog Input Sampling and Scan Conversion Time.

Table 33.6 lists the A/D conversion startup sources selected in the TRSB[5:0] bits.

Table 33.6 Selection of A/D activation sources by TRSB[5:0] bits

Source	Remarks	TRSB[5]	TRSB[4]	TRSB[3]	TRSB[2]	TRSB[1]	TRSB[0]
Trigger source de-selection state		1	1	1	1	1	1
ELC_AD00	ELC	0	0	1	0	0	1
ELC_AD01	ELC	0	0	1	0	1	0
ELC_AD00/ELC_AD01	ELC	0	0	1	0	1	1

TRSA[5:0] bits (A/D Conversion Start Trigger Select)

The TRSA[5:0] bits select the trigger to start A/D conversion in single scan mode and continuous scan mode. In group scan mode, the trigger to start scanning of the analog input selected in group A is selected. When scanning is executed in group scan mode or double trigger mode, software trigger or asynchronous trigger is prohibited.

- When using a synchronous trigger (ELC), set the TRGE bit in the ADCSR register to 1 and set the EXTRG bit in the ADCSR register to 0
- When using the asynchronous trigger (ADTRG0), software trigger or asynchronous trigger is prohibited.
- Software trigger (ADCSR.ADST) is enabled regardless of the settings of the ADCSR.TRGE bit, the ADCSR.EXTRG bit, or the TRSA[5:0] bits.

The issuance period for a conversion trigger must be more than or equal to the actual scan conversion time (tSCAN). If the issuance period is less than tSCAN, A/D conversion by a trigger might have no effect. For details, see section 33.3.6, Analog Input Sampling and Scan Conversion Time.

Table 33.7 lists the A/D conversion start sources selected in the TRSA[5:0] bits.

Table 33.7 Selection of A/D activation sources by TRSA[5:0] bits

Source	Remarks	TRSA[5]	TRSA[4]	TRSA[3]	TRSA[2]	TRSA[1]	TRSA[0]
Trigger source deselection state		1	1	1	1	1	1
ADTRG0	Input pin for the trigger	0	0	0	0	0	0
ELC_AD00	ELC	0	0	1	0	0	1
ELC_AD01	ELC	0	0	1	0	1	0
ELC_AD00/ELC_AD01	ELC	0	0	1	0	1	1

33.2.13 A/D Conversion Extended Input Control Register (ADEXICR)

Address(es): ADC140.ADEXICR 4005 C012h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	OCSA	TSSA	—	—	—	—	—	—	OCSAD	TSSAD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TSSAD	Temperature Sensor Output A/D-Converted Value Addition/Average Mode Select	0: Temperature sensor output A/D-converted value addition/average mode not selected 1: Temperature sensor output A/D-converted value addition/average mode selected.	R/W
b1	OCSAD	Internal Reference Voltage A/D-Converted Value Addition/Average Mode Select	0: Internal reference voltage A/D-converted value addition/average mode not selected 1: Internal reference voltage A/D-converted value addition/average mode selected.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	TSSA	Temperature Sensor Output A/D Conversion Select	0: A/D conversion of temperature sensor output disabled 1: A/D conversion of temperature sensor output enabled.	R/W
b9	OCSA	Internal Reference Voltage A/D Conversion Select	0: A/D conversion of internal reference voltage disabled 1: A/D conversion of internal reference voltage enabled.	R/W
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TSSAD bit (Temperature Sensor Output A/D-Converted Value Addition/Average Mode Select)

When the TSSAD bit is set to 1, A/D conversion of the temperature sensor output is selected and performed successively the number of times specified in the ADC[2:0] bits in ADADC. The maximum addition count differs depending on the conversion accuracy, see section 33.2.1. When the ADADC.AVEE bit is 0, the value obtained by addition is returned to the A/D Temperature Sensor Data Register (ADTSDR). When the ADADC.AVEE bit is 1, the mean value is returned to the ADTSDR register.

Only set the TSSAD bit when the ADCSR.ADST bit is 0.

OCSAD bit (Internal Reference Voltage A/D-Converted Value Addition/Average Mode Select)

When the OCSAD bit is set to 1, A/D conversion of the internal reference voltage is selected and performed successively the number of times specified in the ADC[2:0] bits in the ADADC register. The maximum addition count differs depending on the conversion accuracy, see section 33.2.1. When the ADADC.AVEE bit is 0, the value obtained by addition is returned to the A/D Internal Reference Voltage Data Register (ADOCDR). When the ADADC.AVEE bit is 1, the mean value is returned to the ADOCDR register.

Only set the OCSAD bit while the ADCSR.ADST bit is 0.

TSSA bit (Temperature Sensor Output A/D Conversion Select)

The TSSA bit selects A/D conversion of the temperature sensor output. When executing the A/D conversion of the temperature sensor output:

1. Set all bits in the ADANSA0/1, ADANSB0/1 registers, ADCSR.DBLE and ADEXICR.OCSA bits to 0.
2. Execute the A/D conversion in single scan mode.

Only set the TSSA bit when the ADCSR.ADST bit is 0.

When executing the A/D conversion of the temperature sensor output, the ADDISCR register is set to 0Fh and the A/D converter executes discharge (15 ADCLK) before executing sampling. The required sampling time is 5 µs or more.

The A/D converter executes discharge each time A/D conversion is executed on the temperature sensor output.

OCSA bit (Internal Reference Voltage A/D Conversion Select)

The OCSA bit selects A/D conversion of the internal reference voltage. When executing the A/D conversion of the internal reference voltage:

1. Set all bits in the ADANSA0/1, ADANSB0/1 registers, ADCSR.DBLE and ADEXICR.TSSA bits to 0.
2. Execute the A/D conversion in single scan mode.

Only set the OCSA bit when the ADCSR.ADST bit is 0.

When executing the A/D conversion of the internal reference voltage, the ADDISCR register is set to 0Fh and the A/D converter executes discharge (15 ADCLK) before executing sampling. The required sampling time is 5 µs or more.

The A/D converter executes discharge each time A/D conversion is executed on the internal reference voltage.

33.2.14 A/D Sampling State Register n (ADSSTRn) (n = 00 to 13, L, T, O)

Address(es): ADC140.ADSSTR00 4005 C0E0h to ADC140.ADSSTR13 4005 C0EDh,
ADC140.ADSSTRL 4005 C0DDh, ADC140.ADSSTRT 4005 C0DEh, ADC140.ADSSTRO 4005 C0DFh

	b7	b6	b5	b4	b3	b2	b1	b0
	SST[7:0]							
Value after reset:	0	0	0	0	1	1	0	1

Bit	Symbol	Bit name	Description	R/W
b7 to b0	SST[7:0]	Sampling Time Setting	These bits set the sampling time in the range from 5 to 255 states	R/W

The ADSSTRn register sets the sampling time for analog input.

If one state is 1 A/D conversion clock cycle (ADCLK) and the ADCLK clock is 64 MHz, one state is 15.625 ns. The initial value is 13 states. The sampling time can be adjusted if the impedance of the analog input signal source is too high to secure sufficient sampling time, or if the ADCLK clock is slow.

The lower limit of the sampling time setting depends on the frequency ratio:

- If the frequency ratio of PCLKB to PCLKD (ADCLK) = 1:1, the sampling time must be set to a value of more than 5 states
- If the frequency ratio of PCLKB to PCLKD (ADCLK) = 1:2 or 1:4, the sampling time must be set to a value of more than 6 states.

Table 33.8 shows the relationship between the A/D Sampling State Register and the associated channels.

For details, see section 33.3.6, Analog Input Sampling and Scan Conversion Time.

Only set the SST[7:0] bits when the ADCSR.ADST bit is 0.

Table 33.8 Relationship between A/D Sampling State Register and associated channels

Bit name	Associated channels
ADSSTR00.SST[7:0] bits*1	AN000
ADSSTR01.SST[7:0] bits	AN001
ADSSTR02.SST[7:0] bits	AN002
ADSSTR03.SST[7:0] bits	AN003
ADSSTR04.SST[7:0] bits	AN004
ADSSTR05.SST[7:0] bits	AN005
ADSSTR06.SST[7:0] bits	AN006
ADSSTR07.SST[7:0] bits	AN007
ADSSTR08.SST[7:0] bits	AN008
ADSSTR09.SST[7:0] bits	AN009
ADSSTR10.SST[7:0] bits	AN010
ADSSTR11.SST[7:0] bits	AN011
ADSSTR12.SST[7:0] bits	AN012
ADSSTR13.SST[7:0] bits	AN013
ADSSTRL.SST[7:0] bits	AN016-AN022
ADSSTRT.SST[7:0] bits	Temperature sensor output*2
ADSSTRO.SST[7:0] bits	Internal reference voltage*2

Note 1. When the self-diagnosis function is selected, the sampling time set in the ADSSTR00.SST[7:0] bits is applied.
Note 2. When the temperature sensor output or the internal reference voltage is converted, set the sampling time to more than 5 μs. Because the maximum SST[7:0] value is 255 states, the ADCLK frequency must be 64 MHz or less to achieve 5 μs sampling time.

33.2.15 A/D Disconnection Detection Control Register (ADDISCR)

Address(es): ADC140.ADDISCR 4005 C07Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PCHG	ADNDIS[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	ADNDIS[3:0]	Precharge/Discharge Period	b3 b0 0000: The disconnection detection assist function is disabled 0001: Setting prohibited. Other values indicate the number of states for the period of discharge or precharge.	R/W
b4	PCHG	Precharge/Discharge Select	0: Discharge 1: Precharge.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The ADDISCR register selects either precharge or discharge and the period of precharge or discharge for the A/D disconnection detection assist function. Only set the ADDISCR register when the ADCSR.ADST bit is 0.

When the temperature sensor output or internal reference voltage is converted, the A/D converter executes discharge automatically. This operation is achieved by automatically setting the ADDISCR register to 0Fh (15 ADCLK) when ADEXICR.OCSA or TSSA is set to 1. After executing discharge, the A/D converter executes sampling. The required sampling time is 5 μs or more.

If any of the following functions are used, the disconnection detection assist function should be disabled:

- The temperature sensor
- The internal reference voltage
- A/D self-diagnosis.

ADNDIS[3:0] bits (Precharge/Discharge Period)

The ADNDIS[3:0] bits specify the period of precharge or discharge. When ADNDIS[3:0] = 0000b, the disconnection detection assist function is disabled. Setting the ADNDIS[3:0] bits to 0001b is prohibited. Except when ADNDIS[3:0] = 0000b or 0001b, the specified value indicates the number of states for the period of precharge or discharge. When the ADNDIS[3:0] bits are set to any values other than 0000b or 0001b, the disconnection detection assistance function is enabled.

PCHG bit (Precharge/Discharge Select)

Setting the PCHG bit to 1 selects precharge and setting the PCHG bit to 0 selects discharge.

33.2.16 A/D Group Scan Priority Control Register (ADGSPCR)

Address(es): ADC140.ADGSPCR 4005 C080h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	GBRP	—	—	—	—	—	—	—	—	—	—	—	—	—	GBRSCN	PGS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PGS	Group A Priority Control Setting*1	0: Operate without group A priority control 1: Operate with group A priority control.	R/W
b1	GBRSCN	Group B Restart Setting	Enabled only when PGS = 1, reserved when PGS = 0. 0: Do not restart group B scanning after it is stopped by group A priority control 1: Restart scanning for group B after it is stopped by group A priority control.	R/W
b14 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	GBRP	Group B Single Scan Continuous Start*2	Enabled only when PGS = 1, reserved when PGS = 0 0: Single scan for group B not continuously activated 1: Single scan for group B continuously activated.	R/W

Note 1. The ADCSR.ADCS[1:0] bits must be set to 01b (group scan mode) before setting the PGS bit to 1. Operation is not guaranteed if these bits are set to any other value.

Note 2. When the GBRP bit is set to 1, single scan is performed continuously for group B regardless of the GBRSCN bit.

PGS bit (Group A Priority Control Setting)

Set the PGS bit to 1 to give priority to operation on group A.

The ADCSR.ADCS[1:0] bits must be set to 01b (group scan mode) before setting the PGS bit to 1. Operation is not guaranteed if the bits are set to any other values.

When the PGS bit is set to 0, software must perform a clear operation as described in section 33.8.2, Notes on Stopping A/D Conversion. When the PGS bit is set to 1, use the settings as described in section 33.3.4.3, Operation under group A priority control.

GBRSCN bit (Group B Restart Setting)

The GBRSCN bit controls the restarting of scan operation on group B when operation on group A is given priority.

If a scan operation on group B is stopped by a group A trigger input when the GBRSCN bit is set to 1, the scan operation is restarted on completion of group A conversion. Also, if a group B trigger is input during A/D conversion on group A, the scan operation on group B is restarted on completion of group A conversion.

When the GBRSCN bit is set to 0, triggers input during A/D conversion are ignored. Additionally, the ADCSR.ADST bit must be 0 when the GBRSCN bit is set.

The setting of the GBRSCN bit is valid when the PGS bit is 1.

GBRP bit (Group B Single Scan Continuous Start)

Set the GBRP bit to perform a single scan operation continuously on group B.

Setting the GBRP bit to 1 starts a single scan on group B. On completion of the scan, another single scan on group B starts automatically. If a group B conversion stops because of an operation on group A, the group A operation takes priority, and single scan on group B automatically restarts on completion of group A conversion.

Disable group B trigger input before setting the GBRP bit to 1. Setting the GBRP bit to 1 invalidates the setting of the GBRSCN bit. The ADCSR.ADST bit must be 0 when the GBRP bit is set.

The setting of the GBRP bit is valid when the PGS bit is 1.

33.2.17 A/D Compare Function Control Register (ADCMPCR)

Address(es): ADC140.ADCMPCR 4005 C090h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CMPAIE	WCMPE	CMPBIE	—	CMPAE	—	CMPBE	—	—	—	—	—	—	—	CMPAB[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	CMPAB[1:0]	Window A/B Composite Conditions Setting	b1 b0 0 0: Output ADC140_WCMPM when window A OR window B comparison conditions are met, otherwise output ADC140_WCMPUM in other cases. 0 1: Output ADC140_WCMPM when window A EXOR window B comparison conditions are met, otherwise output ADC140_WCMPUM in other cases. 1 0: Output ADC140_WCMPM when window A AND window B comparison conditions are met, otherwise output ADC140_WCMPUM in other cases. 1 1: Setting prohibited. These bits are valid when both window A and window B are enabled (CMPAE = 1 and CMPBE = 1).	R/W
b8 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9	CMPBE	Compare Window B Operation Enable	0: Compare window B operation disabled. ADC140_WCMPM and ADC140_WCMPUM outputs are disabled. 1: Compare window B operation enabled.	R/W
b10	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b11	CMPAE	Compare Window A Operation Enable	0: Compare window A operation disabled. ADC140_WCMPM and ADC140_WCMPUM outputs are disabled. 1: Compare window A operation enabled.	R/W
b12	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b13	CMPBIE	Compare B Interrupt Enable	0: ADC140_CMPBI interrupt disabled when comparison conditions (window B) are met 1: ADC140_CMPBI interrupt enabled when comparison conditions (window B) are met.	R/W
b14	WCMPE	Window Function Setting	0: Window function disabled Window A and window B operate as a comparator to compare the single value on the lower side with the A/D conversion result. 1: Window function enabled Window A and window B operate as a comparator to compare the two values on the upper and lower sides with the A/D conversion result.	R/W

Bit	Symbol	Bit name	Description	R/W
b15	CMPAIE	Compare A Interrupt Enable	0: ADC140_CMPAI interrupt disabled when comparison conditions (window A) are met 1: ADC140_CMPAI interrupt enabled when comparison conditions (window A) are met.	R/W

CMPAB[1:0] bits (Window A/B Composite Conditions Setting)

The CMPAB[1:0] bits are valid when both window A and window B are enabled (CMPAE = 1 and CMPBE = 1) in single scan mode. These bits specify the compare function match/mismatch event output conditions and monitoring conditions of ADWINMON.MONCONB. Only set the CMPAB[1:0] bits when the ADCSR.ADST bit is 0.

CMPBE bit (Compare Window B Operation Enable)

The CMPBE bit enables or disables the compare window B operation. Set the CMPBE bit while the ADCSR.ADST bit is 0.

Set the CMPBE bit to 0 before setting the following registers:

- A/D channel select registers A0/A1/B0/B1 (ADANSA0, ADANSA1, ADANSB0, ADANSB1)
- OCSA, or TSSA in the A/D conversion extended input control register (ADEXICR.{OCSA, TSSA})
- CMPCHB[5:0] in the window B channel select register (ADCMPBNSR.CMPCHB[5:0]).

CMPAE bit (Compare Window A Operation Enable)

The CMPAE bit enables or disables the compare window A operation. Set the CMPAE bit when the ADCSR.ADST bit is 0.

Set this bit to 0 before setting the following registers:

- A/D channel select registers A0/A1/B0/B1 (ADANSA0, ADANSA1, ADANSB0, ADANSB1)
- OCSA, or TSSA in the A/D conversion extended input control register (ADEXICR.{OCSA, TSSA})
- Window A channel select registers 0/1 (ADCMPANSR0, ADCMPANSR1)
- Window A extended input select register (ADCMPANSER).

CMPBIE bit (Compare B Interrupt Enable)

The CMPBIE bit enables or disables the ADC140_CMPBI interrupt output when the comparison conditions (window B) are met.

WCMPE bit (Window Function Setting)

The WCMPE bit enables or disables the window function. Set the WCMPE bit when the ADCSR.ADST bit is 0.

CMPAIE bit (Compare A Interrupt Enable)

The CMPAIE bit enables or disables the ADC140_CMPAI interrupt output when the comparison conditions (window A) are met.

33.2.18 A/D Compare Function Window A Channel Select Register 0 (ADCMPANSR0)

Address(es): ADC140.ADCMPANSR0 4005 C094h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CMPCHA13	CMPCHA12	CMPCHA11	CMPCHA10	CMPCHA09	CMPCHA08	CMPCHA07	CMPCHA06	CMPCHA05	CMPCHA04	CMPCHA03	CMPCHA02	CMPCHA01	CMPCHA00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b13 to b0	CMPCHA13 to CMPCHA00	Compare Window A Channel Select	0: Compare function disabled for associated input channel 1: Compare function enabled for associated input channel. Bit [13] (CHPCHA13) is associated with AN013 and bit [0] (CMPCHA00) is associated with AN000.	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPCHAn bits (n = 00 to 13) (Compare Window A Channel Select)

The compare function is enabled by writing 1 to the CMPCHAn bit with the same number as the A/D conversion channel selected in the ADANSA0.ANSAn bits (n = 00 to 13) and the ADANSB0.ANSBn bits (n = 00 to 13).

Set the CMPCHAn bits when the ADCSR.ADST bit is 0.

33.2.19 A/D Compare Function Window A Channel Select Register 1 (ADCMPANSR1)

Address(es): ADC140.ADCMPANSR1 4005 C096h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	CMPCHA22	CMPCHA21	CMPCHA20	CMPCHA19	CMPCHA18	CMPCHA17	CMPCHA16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b6 to b0	CMPCHA22 to CMPCHA16	Compare Window A Channel Select	0: Compare function disabled for associated input channel 1: Compare function enabled for associated input channel Bit [6] (CMPCHA22) is associated with AN022 and bit [0] (CMPCHA16) is associated with AN016.	R/W
b15 to b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPCHAn bits (n = 16 to 22) (Compare Window A Channel Select)

The compare function is enabled by writing 1 to the CMPCHAn bit of the same number as the A/D conversion channel selected by the ADANSA1.ANSAn bits (n = 16 to 22) and the ADANSB1.ANSBn bits (n = 16 to 22).

Set the CMPCHAn bits when the ADCSR.ADST bit is 0.

33.2.20 A/D Compare Function Window A Extended Input Select Register (ADCMPANSER)

Address(es): ADC140.ADCMPANSER 4005 C092h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	CMPOCA	CMPTSA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CMPTSA	Temperature Sensor Output Compare Select	0: Exclude the temperature sensor output from the compare window A target range 1: Include the temperature sensor output in the compare window A target range.	R/W
b1	CMPOCA	Internal Reference Voltage Compare Select	0: Exclude the internal reference voltage from the compare window A target range 1: Include the internal reference voltage in the compare window A target range.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPTSA bit (Temperature Sensor Output Compare Select)

The compare window A function is enabled by setting the CMPTSA bit to 1 when the ADEXICR.TSSA bit is 1. Set the CMPTSA bit when the ADCSR.ADST bit is 0.

CMPOCA bit (Internal Reference Voltage Compare Select)

The compare window A function is enabled by setting the CMPOCA bit to 1 when the ADEXICR.OCSA bit is 1. Set the CMPOCA bit when the ADCSR.ADST bit is 0.

33.2.21 A/D Compare Function Window A Comparison Condition Setting Register 0 (ADCMPLR0)

Address(es): ADC140.ADCMPLR0 4005 C098h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CMPLCHA13	CMPLCHA12	CMPLCHA11	CMPLCHA10	CMPLCHA09	CMPLCHA08	CMPLCHA07	CMPLCHA06	CMPLCHA05	CMPLCHA04	CMPLCHA03	CMPLCHA02	CMPLCHA01	CMPLCHA00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b13 to b0	CMPLCHA13 to CMPLCHA00	Compare Window A Comparison Condition Select	These bits set comparison conditions for channels AN000 to AN013 to which window A comparison conditions are applied. Comparison conditions are shown in Figure 33.3. • When window function is disabled (ADCMPCR.WCMPE bit = 0): 0: ADCMPDR0 value > A/D converted value 1: ADCMPDR0 value < A/D converted value. • When the window function is enabled (ADCMPCR.WCMPE bit = 1): 0: A/D converted value < ADCMPDR0 value or ADCMPDR1 value < A/D converted value 1: ADCMPDR0 value < A/D converted value < ADCMPDR1 value.	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPLCHAn bits (n = 00 to 13) (Compare Window A Comparison Condition Select)

The CMPLCHAn bits specify the comparison conditions for channels AN000 to AN013 to which window A comparison conditions are applied. These bits can be set for each analog input to be compared. CMPLCHA00 is associated with

AN000, CMPLCHA07 is associated with AN007, and CMPLCHA13 is associated with AN013. When the comparison result of each analog input meets the set condition, the ADCMPSR0.CMPSTCHAn bit is set to 1 and a compare interrupt (ADC140_CMPAI) is generated.

Comparison conditions when the window function is disabled

CMPLCHAn = 0

ADCMPDR0 value ≤ A/D converted value	Not met
ADCMPDR0 value > A/D converted value	Met

CMPLCHAn = 1

ADCMPDR0 value < A/D converted value	Met
ADCMPDR0 value ≥ A/D converted value	Not met

Comparison conditions when the window function is enabled

CMPLCHAn = 0

ADCMPDR1 value < A/D converted value	Met
ADCMPDR0 value ≤ A/D converted value ≤ ADCMPDR1 value	Not met
A/D converted value < ADCMPDR0 value	Met

CMPLCHAn = 1

ADCMPDR1 value ≤ A/D converted value	Not met
ADCMPDR0 value < A/D converted value < ADCMPDR1 value	Met
A/D converted value ≤ ADCMPDR0 value	Not met

Figure 33.3 Comparison conditions for compare function window A

33.2.22 A/D Compare Function Window A Comparison Condition Setting Register 1 (ADCMPLR1)

Address(es): ADC140.ADCMPLR1 4005 C09Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	CMPLCHA22	CMPLCHA21	CMPLCHA20	CMPLCHA19	CMPLCHA18	CMPLCHA17	CMPLCHA16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b6 to b0	CMPLCHA22 to CMPLCHA16	Compare Window A Comparison Condition Select	These bits set comparison conditions for channels AN016 to AN022 to which window A comparison conditions are applied. Comparison conditions are shown in Figure 33.3. • When window function is disabled (ADCMPCR.WCMPE bit = 0): 0: ADCMPDR0 value > A/D converted value 1: ADCMPDR0 value < A/D converted value. • When window function is enabled (ADCMPCR.WCMPE bit = 1): 0: A/D converted value < ADCMPDR0 value or ADCMPDR1 value < A/D converted value 1: ADCMPDR0 value < A/D converted value < ADCMPDR1 value.	R/W
b15 to b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPLCHAn bits (n = 16 to 22) (Compare Window A Comparison Condition Select)

The CMPLCHAn bits specify the comparison conditions for channels AN016 to AN022 to which window A comparison conditions are applied. These bits can be set for each analog input to be compared. CMPLCHA16 is associated with AN016 and CMPLCHA22 is associated with AN022. When the comparison result of each analog input meets the set condition, the ADCMPSR1.CMPSTCHAn bit is set to 1 and a compare interrupt (ADC140_CMPAI) is generated.

33.2.23 A/D Compare Function Window A Extended Input Comparison Condition Setting Register (ADCMPLER)

Address(es): ADC140.ADCMPLER 4005 C093h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	CMPLOCA	CMPLTSA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CMPLTSA	Compare Window A Temperature Sensor Output Comparison Condition Select	Comparison conditions are shown in Figure 33.3. • When window A function is disabled (ADCMPCR.WCMPE bit = 0): 0: ADCMPDR0 value > A/D converted value 1: ADCMPDR0 value < A/D converted value. • When window A function is enabled (ADCMPCR.WCMPE bit = 1): 0: A/D converted value < ADCMPDR0 value or A/D converted value > ADCMPDR1 value 1: ADCMPDR0 value < A/D converted value < ADCMPDR1 value.	R/W
b1	CMPLOCA	Compare Window A Internal Reference Voltage Comparison Condition Select	Comparison conditions are shown in Figure 33.3. • When window A function is disabled (ADCMPCR.WCMPE bit = 0): 0: ADCMPDR0 register value > A/D-converted value 1: ADCMPDR0 register value < A/D-converted value. • When window A function is enabled (ADCMPCR.WCMPE bit = 1): 0: A/D-converted value < ADCMPDR0 register value or A/D-converted value > ADCMPDR1 register value 1: ADCMPDR0 register value < A/D-converted value < ADCMPDR1 register value.	R/W

Bit	Symbol	Bit name	Description	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPLTSA bit (Compare Window A Temperature Sensor Output Comparison Condition Select)

The CMPLTSA bit specifies the comparison conditions when the temperature sensor output is the target of the window A comparison condition. When the temperature sensor output comparison result meets the set condition, the ADCMPSER.CMPSTTSA bit is set to 1 and a compare interrupt (ADC140_CMPAI) is generated.

CMPLOCA bit (Compare Window A Internal Reference Voltage Comparison Condition Select)

The CMPLOCA bit specifies the comparison conditions when the internal reference voltage is the target of the window A comparison condition. When the internal reference voltage comparison result meets the set condition, the ADCMPSER.CMPSTOCA bit is set to 1 and a compare interrupt (ADC140_CMPAI) is generated.

33.2.24 A/D Compare Function Window A Lower-Side Level Setting Register (ADCMPDR0), A/D Compare Function Window A Upper-Side Level Setting Register (ADCMPDR1), A/D Compare Function Window B Lower-Side Level Setting Register (ADWINLLB), A/D Compare Function Window B Upper-Side Level Setting Register (ADWINULB)

Address(es): ADC140.ADCMPDR0 4005 C09Ch, ADC140.ADCMPDR1 4005 C09Eh, ADC140.ADWINLLB 4005 C0A8h, ADC140.ADWINULB 4005 C0AAh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	—	—	Reference value	R/W

The ADCMPDRy (y = 0,1) register specifies the reference data when the compare window A function is used. ADCMPDR0 sets the lower reference for window A, and ADCMPDR1 sets the upper reference for window A.

The ADWINULB and ADWINLLB registers specify the reference data when the compare window B function is used. ADWINLLB sets the lower reference for window B, and ADWINULB sets the upper reference for window B.

ADCMPDRy, ADWINULB, and ADWINLLB are read/write registers.

ADCMPDRy, ADWINULB, and ADWINLLB are writable even during A/D conversion. The reference data can be dynamically modified by rewriting register values during A/D conversion*1.

Set these registers so that the upper reference is not less than the lower reference (ADCMPDR1 ≥ ADCMPDR0 and ADWINULB ≥ ADWINLLB). ADCMPDR1 and ADWINULB are not used when the window function is disabled.

Note 1. The lower and the upper references are changed when each register is written. For example, when the upper reference value and the lower reference value are changed, the MCU compares the upper reference (after rewrite), and the lower reference (before rewrite) with the A/D conversion result. See Figure 33.4. If the comparison during the rewriting of these two references is erroneous, then rewrite these reference values when both ADCSR.ADST and the target Compare Window Operation Enable bit (ADCMPCR.CMPAE or ADCMPCR.CMPBE) is 0.

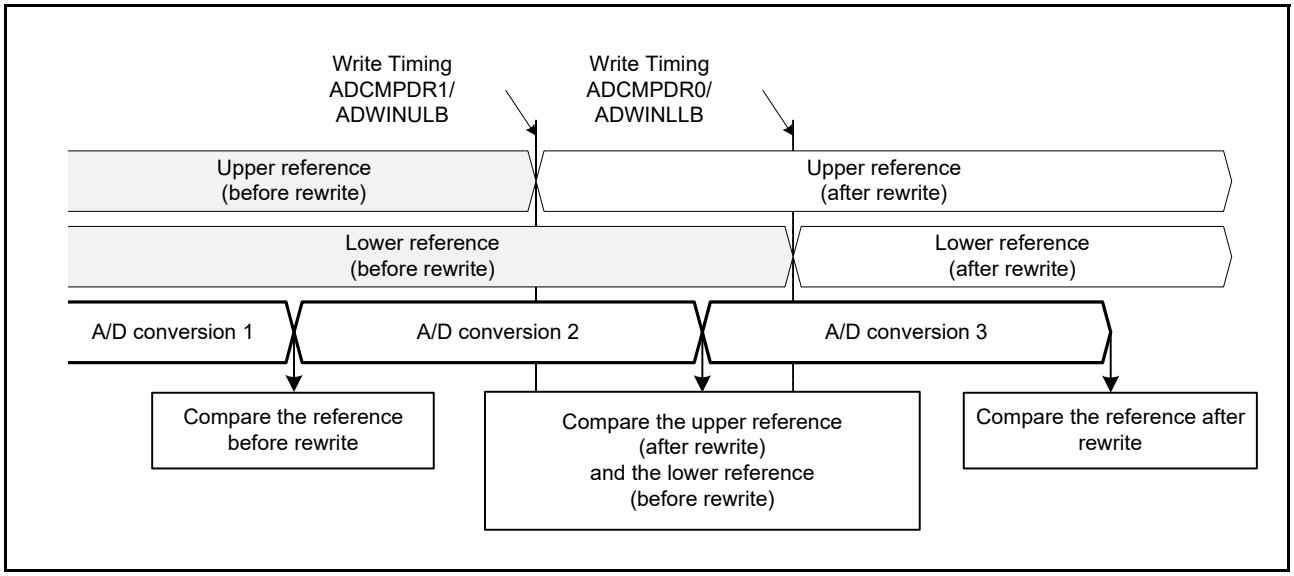


Figure 33.4 Comparison between upper reference and lower reference before and after a rewrite

The ADCMPDRy, ADWINLLB, and ADWINULB registers use different formats depending on the following conditions:

- The value of A/D Data Register Format Select bit (flush-right or flush-left)
- The value of A/D-Conversion Accuracy Specify bit (14-bit, 12-bit)
- The value of A/D-Converted Value Addition/Average Channel Select bits (A/D-converted value addition mode selected or not selected).

The data formats for each given condition are shown as follows:

(1) When A/D-Converted Value Addition Mode is not selected

- Flush-right data with 14-bit accuracy — Lower 14-bit ([13:0]) are valid
- Flush-right data with 12-bit accuracy — Lower 12-bit ([11:0]) are valid
- Flush-left data with 14-bit accuracy — Upper 14-bit ([15:2]) are valid
- Flush-left data with 12-bit accuracy — Upper 12-bit ([15:4]) are valid.

(2) When A/D-Converted Value Addition Mode is selected

- Flush-right data with 14-bit accuracy — All bit ([15:0]) are valid
- Flush-right data with 12-bit accuracy — Lower 14-bit ([13:0]) are valid
- Flush-left data with 14-bit accuracy — All bit ([15:0]) are valid
- Flush-left data with 12-bit accuracy — Upper 14-bit ([15:2]) are valid.

33.2.25 A/D Compare Function Window A Channel Status Register 0 (ADCMPSR0)

Address(es): ADC140.ADCMPSR0 4005 C0A0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CMPSTCHA13	CMPSTCHA12	CMPSTCHA11	CMPSTCHA10	CMPSTCHA09	CMPSTCHA08	CMPSTCHA07	CMPSTCHA06	CMPSTCHA05	CMPSTCHA04	CMPSTCHA03	CMPSTCHA02	CMPSTCHA01	CMPSTCHA00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b13 to b0	CMPSTCHA13 to CMPSTCHA00	Compare Window A Flag	When window A operation is enabled (ADCMPCR.CMPAE = 1b), these bits indicate the comparison result of channels AN000 to AN013 to which window A comparison conditions are applied. 0: Comparison conditions not met 1: Comparison conditions met.	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPSTCHAn bits (n = 00 to 13) (Compare Window A Flag)

The CMPSTCHAn bits are comparison result status flags of channels AN000 to AN013 to which window A comparison conditions are applied. When the comparison condition set by ADCMPLR0.CMPLCHAn is met at the end of A/D conversion, the associated CMPSTCHAn bit is set to 1. When the ADCMPCR.CMPAIE bit is 1, a compare interrupt (ADC140_CMPAI) request is generated when a CMPSTCHAn bit is set to 1. CMPSTCHA00 is associated with AN000, CMPSTCHA07 is associated with AN007, and CMPSTCHA13 is associated with AN013.

Writing 1 to the CMPSTCHAn bits is disabled.

[Setting condition]

- The condition set in ADCMPLR0.CMPLCHAn is met when ADCMPCR.CMPAE = 1.

[Clearing condition]

- Writing 0 after reading 1.

33.2.26 A/D Compare Function Window A Channel Status Register1 (ADCMPSR1)

Address(es): ADC140.ADCMPSR1 4005 C0A2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	CMPSTCHA22	CMPSTCHA21	CMPSTCHA20	CMPSTCHA19	CMPSTCHA18	CMPSTCHA17	CMPSTCHA16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b6 to b0	CMPSTCHA22 to CMPSTCHA16	Compare Window A Flag	When window A operation is enabled (ADCMPCR.CMPAE = 1), these bits indicate the comparison result of channels AN016 to AN022 to which window A comparison conditions are applied. 0: Comparison conditions not met 1: Comparison conditions met.	R/W
b15 to b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPSTCHAn bits (n = 16 to 22) (Compare Window A Flag)

The CMPSTCHAn bits are comparison result status flags of channels AN016 to AN022 to which window A comparison conditions are applied. When the comparison condition set by ADCMPLR1.CMPLCHAn is met at the end of A/D conversion, the associated CMPSTCHAn bit is set to 1. When the ADCMPCR.CMPAIE bit is 1, a compare interrupt (ADC140_CMPAI) request is generated when a CMPSTCHAn bit is set to 1. CMPSTCHA16 is associated with AN016, and CMPSTCHA22 is associated with AN022.

Writing 1 to the CMPSTCHAn bits is disabled.

[Setting condition]

- The condition set in ADCMPLR1.CMPLCHAn is met when ADCMPCR.CMPAE = 1.

[Clearing condition]

- Writing 0 after reading 1.

33.2.27 A/D Compare Function Window A Extended Input Channel Status Register (ADCMPSER)

Address(es): ADC140.ADCMPSER 4005 C0A4h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	CMPSTOCA	CMPSTTSA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CMPSTTSA	Compare Window A Temperature Sensor Output Compare Flag	When window A operation is enabled (ADCMPCR.CMPAE = 1), this bit indicates the temperature sensor output comparison result. 0: Comparison conditions not met 1: Comparison conditions met.	R/W
b1	CMPSTOCA	Compare Window A Internal Reference Voltage Compare Flag	When window A operation is enabled (ADCMPCR.CMPAE = 1), this bit indicates the internal reference voltage comparison result. 0: Comparison conditions not met 1: Comparison conditions met.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPSTTSA bit (Compare Window A Temperature Sensor Output Compare Flag)

The CMPSTTSA bit is a status flag that indicates the temperature sensor output comparison result. When the comparison condition set in the ADCMPLER.CMPLTSA bit is met at the end of A/D conversion, the CMPSTTSA bit is set to 1. When the ADCMPCR.CMPAIE bit is 1, a compare interrupt (ADC140_CMPAI) request is generated when the CMPSTTSA bit is set to 1.

Writing 1 to the CMPSTTSA bit is disabled.

[Setting condition]

- The condition set in ADCMPLER.CMPLTSA is met when ADCMPCR.CMPAE = 1.

[Clearing condition]

- Writing 0 after reading 1.

CMPSTOCA bit (Compare Window A Internal Reference Voltage Compare Flag)

The CMPSTOCA bit is a status flag that indicates the internal reference voltage comparison result. When the comparison condition set by ADCMPLER.CMPLOCA is met at the end of A/D conversion, the CMPSTOCA bit is set to 1. When the ADCMPCR.CMPAIE bit is 1, a compare interrupt (ADC140_CMPAI) request is generated when the CMPSTOCA bit is set to 1.

Writing 1 to the CMPSTOCA bit is disabled.

[Setting condition]

- The condition set in ADCMPLER.CMPLOCA is met when ADCMPCR.CMPAE = 1.

[Clearing condition]

- Writing 0 after reading 1.

33.2.28 A/D Compare Function Window B Channel Select Register (ADCMPBNSR)

Address(es): ADC140.ADCMPBNSR 4005 C0A6h

	b7	b6	b5	b4	b3	b2	b1	b0
	CMPLB	—	CMPCHB[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b5 to b0	CMPCHB[5:0]	Compare Window B Channel Select	These bits select channels to be compared with the compare window B conditions. The maximum channel is AN022. b5 b0 0 0 0 0 0 0: AN000 0 0 0 0 0 1: AN001 0 0 0 0 1 0: AN002 : 0 0 1 1 0 1: AN013 0 1 0 0 0 0: AN016 : : 0 1 0 1 0 0: AN020 0 1 0 1 0 1: AN021 0 1 0 1 1 0: AN022 1 0 0 0 0 0: Temperature sensor 1 0 0 0 0 1: Internal reference voltage 1 1 1 1 1 1: Not select. Other settings are prohibited.	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	CMPLB	Compare Window B Comparison Condition Setting	This bit sets comparison conditions of channels for window B. The comparison conditions are shown in 33.2.29. • When the window function is disabled (ADCMPCR.WCMPE bit = 0) 0: CMPLLB value > A/D converted value 1: CMPLLB value < A/D converted value. • When the window function is enabled (ADCMPCR.WCMPE bit = 1) 0: (A/D converted value < CMPLLB value) or (CMPULB value < A/D converted value) 1: CMPLLB value < A/D converted value < CMPULB value.	R/W

CMPCHB[5:0] bits (Compare Window B Channel Select)

The CMPCHB[5:0] bits select channels to be compared with the compare window B conditions from AN000 to AN013, AN016 to AN022, the temperature sensor, and the internal reference voltage. The compare window B function is enabled by specifying the hexadecimal number of an A/D conversion channel selected in the ADANSA0.ANSAn bits (n = 0 to 13), ADANSA1.ANSAn bits (n = 16 to 22), ADANSB0.ANSBn bits (n = 0 to 13), and ADANSB1.ANSBn bits (n = 16 to 22).

Set CMPCHB[5:0] bits when the ADCSR.ADST bit is 0.

CMPLB bit (Compare Window B Comparison Condition Setting)

The CMPLB bit sets comparison conditions of channels for window B. When the comparison result of each analog input meets the set condition, the ADCMPBSR.CMPSTB bit is set to 1 and a compare interrupt ADC140_CMPBI request is generated.

Compare conditions when the window function is disabled

CMPLB = 0

ADWINLLB value ≤ A/D converted value	Not met
ADWINLLB value > A/D converted value	Met

CMPLB = 1

ADWINLLB value < A/D converted value	Met
ADWINLLB value ≥ A/D converted value	Not met

Compare conditions when the window function is enabled

CMPLB = 0

A/D converted value > ADWINULB value	Met
ADWINLLB value ≤ A/D converted value ≤ ADWINULB value	Not met
A/D converted value < ADWINLLB value	Met

CMPLB = 1

A/D converted value ≥ ADWINULB value	Not met
ADWINLLB value <A/D converted value < ADWINULB value	Met
A/D converted value ≤ ADWINLLB value	Not met

Figure 33.5 Compare conditions for compare function window B

33.2.29 A/D Compare Function Window B Status Register (ADCMPBSR)

Address(es): ADC140.ADCMPBSR 4005 C0ACh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CMPSTB
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CMPSTB	Compare Window B Flag	When window B operation is enabled (ADCMPCR.CMPBE = 1), this bit indicates the comparison result of channels AN000 to AN013, AN016 to AN022, temperature sensor output, and internal reference voltage to which window B comparison conditions are applied. 0: Comparison conditions not met 1: Comparison conditions met.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPSTB bit (Compare Window B Flag)

The CMPSTB bit is a status flag that indicates the comparison result of channels AN000 to AN013, AN016 to AN022, the temperature sensor, and the internal reference voltage to which window B comparison conditions are applied. When the comparison condition set by ADCMPBNSR.CMPLB is met at the end of A/D conversion, the CMPSTB bit is set to 1. When the ADCMPCR.CMPBIE bit is 1, a compare interrupt ADC140_CMPBI request is generated when the CMPSTB bit is set to 1.

Writing 1 to the CMPSTB bit is disabled.

[Setting condition]

- The condition set in ADCMPBNSR.CMPLB is met when ADCMPCR.CMPBE = 1.

[Clearing condition]

- Writing 0 after reading 1.

33.2.30 A/D Compare Function Window A/B Status Monitor Register (ADWINMON)

Address(es): ADC140.ADWINMON 4005 C08Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	MONCMPB	MONCMPA	—	—	—	MONCOMB
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	MONCOMB	Combination Result Monitor	This bit indicates the combination result. This bit is valid when both window A operation and window B operation are enabled. 0: Window A/window B composite conditions not met 1: Window A/window B composite conditions met.	R
b3 to b1	—	Reserved	These bits are read as 0.	R
b4	MONCMPA	Comparison Result Monitor A	0: Window A comparison conditions not met 1: Window A comparison conditions met.	R
b5	MONCMPB	Comparison Result Monitor B	0: Window B comparison conditions not met 1: Window B comparison conditions met.	R
b7, b6	—	Reserved	These bits are read as 0	R

MONCOMB bit (Combination Result Monitor)

The read-only bit MONCOMB indicates the combined result of comparison condition results A and B with the combination condition set in the ADCMPCR.CMPAB[1:0] bits.

[Setting condition]

- The combined result meets the combination condition set in the ADCMPCR.CMPAB[1:0] bits when ADCMPCR.CMPAE = 1 and ADCMPCR.CMPBE = 1.

[Clearing conditions]

- The combined result does not meet the combination condition set in the ADCMPCR.CMPAB[1:0] bits.
- ADCMPCR.CMPAE = 0 or ADCMPCR.CMPBE = 0.

MONCMPA bit (Comparison Result Monitor A)

The read-only bit MONCMPA is 1 when the A/D converted value of the window A target channel meets the condition set in the ADCMPLR0/ADCMPLR1 and ADCMPLER registers. Otherwise it is read as 0.

[Setting condition]

- The A/D converted value meets the condition set in the ADCMPLR0/ADCMPLR1 and ADCMPLER registers when ADCMPCR.CMPAE = 1.

[Clearing conditions]

- The A/D converted value does not meet the condition set in the ADCMPLR0/ADCMPLR1 and ADCMPLER registers when ADCMPCR.CMPAE = 1
- ADCMPCR.CMPAE = 0 (automatically cleared when the ADCMPCR.CMPAE value changes from 1 to 0).

MONCMPB bit (Comparison Result Monitor B)

The read-only bit MONCMPB is 1 when the A/D converted value of the window B target channel meets the condition set in the ADCMPBNSR.CMPLB bit. Otherwise it is read as 0.

[Setting condition]

- The A/D converted value meets the condition set by ADCMPBNSR.CMPLB when ADCMPCR.CMPBE = 1.

[Clearing conditions]

- The A/D converted value does not meet the condition set by ADCMPBNSR.CMPLB when ADCMPCR.CMPBE = 1
- ADCMPCR.CMPBE = 0 (automatically cleared when the ADCMPCR.CMPBE value changes from 1 to 0).

33.2.31 A/D High-Potential/Low-Potential Reference Voltage Control Register (ADHVREFCNT)

Address(es): ADC140.ADHVREFCNT 4005 C08Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	ADSLP	—	—	LVSEL	—	—	HVSEL[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	HVSEL[1:0]	High-Potential Reference Voltage Select	b1 b0 0 0: AVCC0 is selected as the high-potential reference voltage 0 1: VREFH0 is selected as the high-potential reference voltage 1 0: Internal reference voltage is selected as the high-potential reference voltage 1 1: Internal node discharged (no reference voltage pin is selected).	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	LVSEL	Low-Potential Reference Voltage Select	0: AVSS0 is selected as the low-potential reference voltage 1: VREFL0 is selected as the low-potential reference voltage.	R/W
b6, b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	ADSLP	Sleep	0: Normal operation 1: Standby state.	R/W

HVSEL[1:0] bits (High-Potential Reference Voltage Select)

The HVSEL[1:0] bits specify the high-potential reference voltage as AVCC0, VREFH0, or the internal reference voltage (1.45 V).

Before selecting the internal reference voltage (HVSEL[1:0] = 10b), set HVSEL[1:0] = 11b to discharge the path of the high-potential reference voltage. After the discharge completes, set HVSEL[1:0] = 10b and start the A/D conversion.

When the internal reference voltage is selected as the high-potential reference voltage (HVSEL[1:0] = 10b), A/D conversion is possible for channels AN000 to AN010, AN016 to AN022, but A/D conversion of the internal reference voltage and the temperature sensor output is prohibited.

LVSEL bit (Low-Potential Reference Voltage Select)

The LVSEL bit specifies the low-potential reference voltage as AVSS0 or VREFL0.

ADSLP bit (Sleep)

The ADSLP bit transitions the A/D converter to the standby state. Set the ADSLP bit to 1 only when modifying the ADCSR.ADHSC bit. In other cases, setting the ADSLP bit to 1 is prohibited.

After the ADSLP bit is set to 1, wait at least 5 µs before clearing this bit to 0. Additionally, after the ADSLP bit is set to 0, wait at least 1 µs, then start the A/D conversion.

For the ADHSC bit rewriting procedure, see section 33.8.8, ADHSC Bit Rewriting Procedure.

33.3 Operation

33.3.1 Scanning Operation

In scanning, A/D conversion is performed sequentially on the analog inputs of the specified channels.

A scan conversion is performed in any of the three operating modes and two conversion modes:

- Single scan mode
- Continuous scan mode
- Group scan mode
- High-speed A/D conversion mode
- Low-power A/D conversion mode.

In single scan mode, one or more specified channels are scanned once. In continuous scan mode, one or more specified channels are scanned repeatedly until software sets the ADST bit in ADCSR to 0. In group scan mode, the selected channels in group A and the selected channels in group B are scanned once after scan starts in response to the respective synchronous trigger (ELC).

In single scan mode and continuous scan mode, A/D conversion is performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n. In group scan mode, A/D conversion is performed for ANn channels in group A selected in the ADANSA0 and ADANSA1 registers first, and for the ANn channels in group B selected in the ADANSB0 and ADANSB1 registers, starting from the channel with the smallest number n.

When self-diagnosis is selected, it is executed once at the beginning of each scan and one of the three reference voltages is converted.

It is prohibited to simultaneously select both temperature sensor output and internal reference voltage. If the internal reference voltage is selected as the reference voltage on the high potential side, A/D conversion of the temperature sensor or the internal reference voltage is also prohibited. When temperature sensor output or internal reference voltage is selected for A/D conversion, single scan mode should be used.

Double trigger mode can be used with single scan mode or group scan mode. With double trigger mode enabled (ADCSR.DBLE is 1), A/D conversion data of a channel selected in the DBLANS[4:0] bits in ADCSR is duplicated only if the conversion is started by the synchronous trigger (ELC) selected in the TRSA[5:0] bits in ADSTRGR. In group scan mode, only group A can use double trigger mode.

In the extended operation of double trigger mode, the A/D conversion operation is generated from the synchronous trigger combination selected in the ADSTRGR.TRSA[5:0] bits. In addition to normal double trigger mode operation, A/D conversion data with odd number trigger (ELC_AD00) is stored in A/D Data Duplexing Register A (ADDBLDRA), and A/D conversion data with even number trigger (ELC_AD01) is stored in A/D Data Duplexing Register B (ADDBLDRB). In the extended operation of double trigger mode, when one of the trigger combination occurs at the same time, the data duplexing register settings for the specified triggers do not work, and A/D conversion data is stored in A/D Data Duplexing Register B (ADDBLDRB).

The ADC14 ignores a synchronous trigger that occurs during the A/D conversion started by another synchronous trigger.

33.3.2 Single Scan Mode

33.3.2.1 Basic operation

In basic operation of single scan mode, A/D conversion is performed once on the analog input of the specified channels as follows:

1. When the ADST bit in ADCSR is set to 1 (A/D conversion start) by a software trigger, a synchronous trigger input (ELC), or an asynchronous trigger input, A/D conversion is performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
2. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register (ADDRy).
3. When A/D conversion of all the selected channels completes, an ADC140_ADI interrupt request is generated.
4. The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically set to 0 when A/D conversion of all the selected channels completes. The ADC14 then enters a wait state.

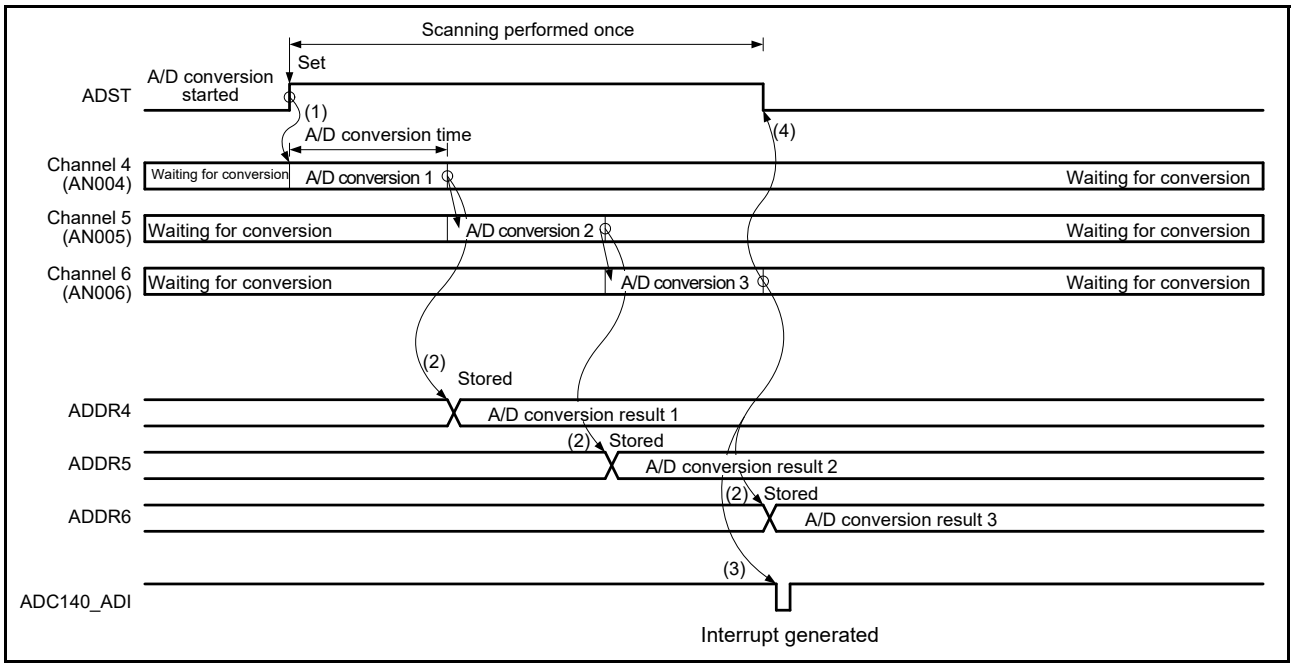


Figure 33.6 Example basic operation in single scan mode when AN004 to AN006 are selected

33.3.2.2 Channel selection and self-diagnosis

When channels and self-diagnosis are selected, A/D conversion is first performed for the reference voltage VREFH0 (×0, ×1/2, or ×1) supplied to the A/D converter, then A/D conversion is performed once on the analog input of the selected channels as follows:

1. A/D conversion for self-diagnosis is first started when the ADST bit in ADCSR is set to 1 (A/D conversion start) by a software trigger, a synchronous trigger input (ELC), or an asynchronous trigger input.
2. When A/D conversion for self-diagnosis completes, the A/D conversion result is stored in the A/D Self-Diagnosis Data Register (ADRD). A/D conversion is then performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
3. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register (ADDRy).
4. When A/D conversion of all the selected channels completes, an ADC140_ADI interrupt request is generated.
5. The ADST bit remains 1 (A/D conversion start) during A/D conversion and is automatically set to 0 when A/D conversion of all the selected channels completes. The ADC14 then enters a wait state.

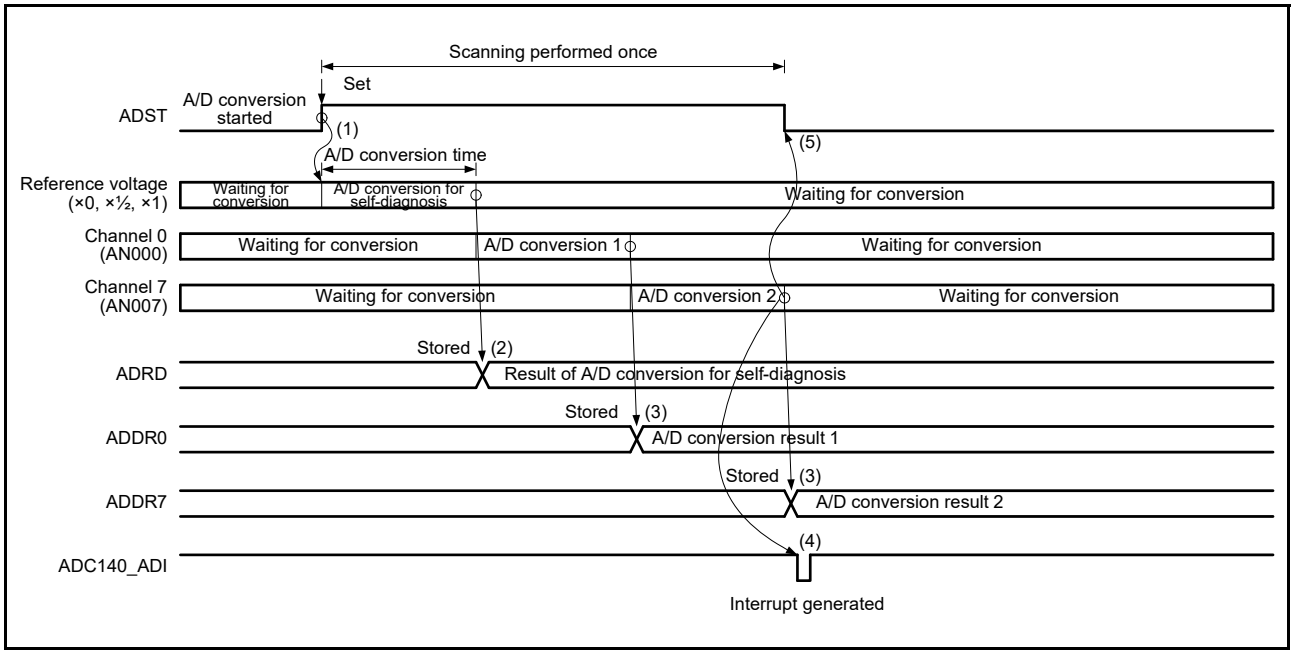


Figure 33.7 Example basic operation in single scan mode when AN000 and AN007 are selected with self-diagnosis

33.3.2.3 A/D conversion of temperature sensor output/internal reference voltage

A/D conversion is performed on the temperature sensor output or the internal reference voltage in single scan mode as described in this section.

When selecting A/D conversion of the temperature sensor output or the internal reference voltage, deselect all analog input channels by setting the ADANSA0 and ADANSA01 registers to all 0's and the ADCSR.DBLE bit to 0.

When selecting A/D conversion of temperature sensor output, set the Internal Reference Voltage A/D Conversion Select bit (ADEXICR.OCSA) to 0 (deselected). When selecting A/D conversion of internal reference voltage, set the Temperature Sensor Output A/D Conversion Select bit (ADEXICR.TSSA) to 0 (deselected).

The operation is as follows:

1. Set the sampling time to 5 µs or longer. Take note of the A/D Sampling State Register settings (ADSSTRT/ADSSTRO) and ADCLK frequency.
2. After switching to A/D conversion of internal reference voltage or temperature sensor output, set the ADST bit to 1 to start conversion.
3. On completion of A/D conversion, the result is stored in the associated A/D Temperature Sensor Data Register (ADTSDR) or A/D Internal Reference Voltage Data Register (ADOCDR), and an ADC140_ADI interrupt request is generated.
4. The ADST bit remains 1 during A/D conversion and is automatically set to 0 on completion of A/D conversion. The ADC14 then enters a wait state.

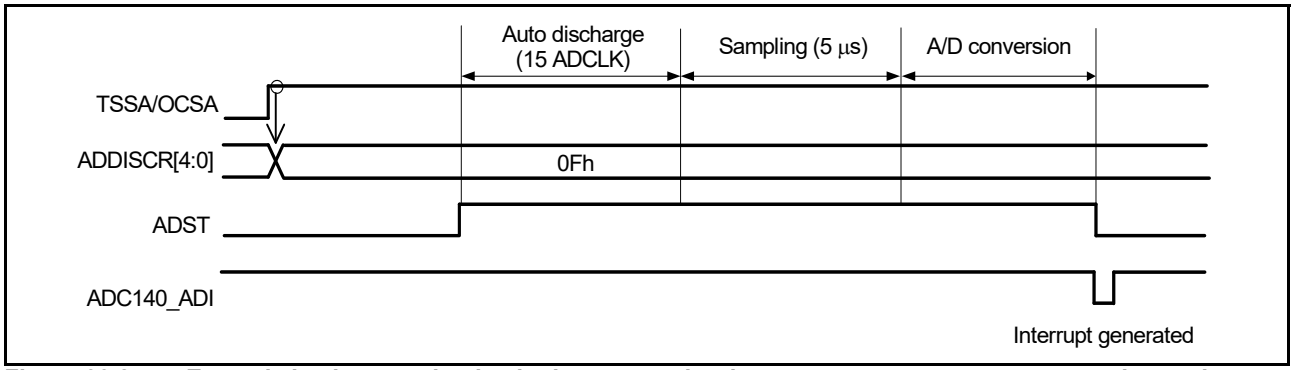


Figure 33.8 Example basic operation in single scan mode when temperature sensor output or internal reference voltage is selected

33.3.2.4 A/D conversion in double trigger mode

When double trigger mode is selected in single scan mode, two rounds of single scan operation started by a synchronous trigger (ELC) are performed in sequence as described in this section.

Deselect self-diagnosis and set the Temperature Sensor Output A/D Conversion Select bit (ADEXICR.TSSA) and the Internal Reference Voltage A/D Conversion Select bit (ADEXICR.OCSA) to 0.

Duplication of A/D conversion data is enabled by setting the channel numbers to be duplicated in the DBLANS[4:0] bits in ADCSR and setting the DBLE bit in ADCSR to 1. When the DBLE bit in ADCSR is set to 1, channel selection using the ADANSA0 and ADANSA1 registers is invalid.

In double trigger mode, select a synchronous trigger (ELC) with the TRSA[5:0] bits in ADSTRGR. Additionally, set the ADCSR.EXTRG bit to 0 and the ADCSR.TRGE bit to 1 Do not use software trigger.

1. When the ADST bit in ADCSR is set to 1 (A/D conversion start) by a synchronous trigger input (ELC), A/D conversion starts on the single channel selected in the DBLANS[4:0] bits in ADCSR.
2. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register (ADDRy).
3. The ADST bit is automatically set to 0 and the ADC14 enters a wait state, but an ADC140_ADI interrupt request is not generated.
4. When the ADST bit in ADCSR is set to 1 (A/D conversion start) by the second trigger input, A/D conversion starts on the single channel selected in the DBLANS[4:0] bits in ADCSR.
5. When A/D conversion completes, the A/D conversion result is stored in the A/D Data Duplexing Register (ADDBLDR), which is only used in double trigger mode.
6. An ADC140_ADI interrupt request is generated.
7. The ADST bit remains 1 (A/D conversion start) during A/D conversion and is automatically set to 0 when A/D conversion completes. The ADC14 then enters a wait state.

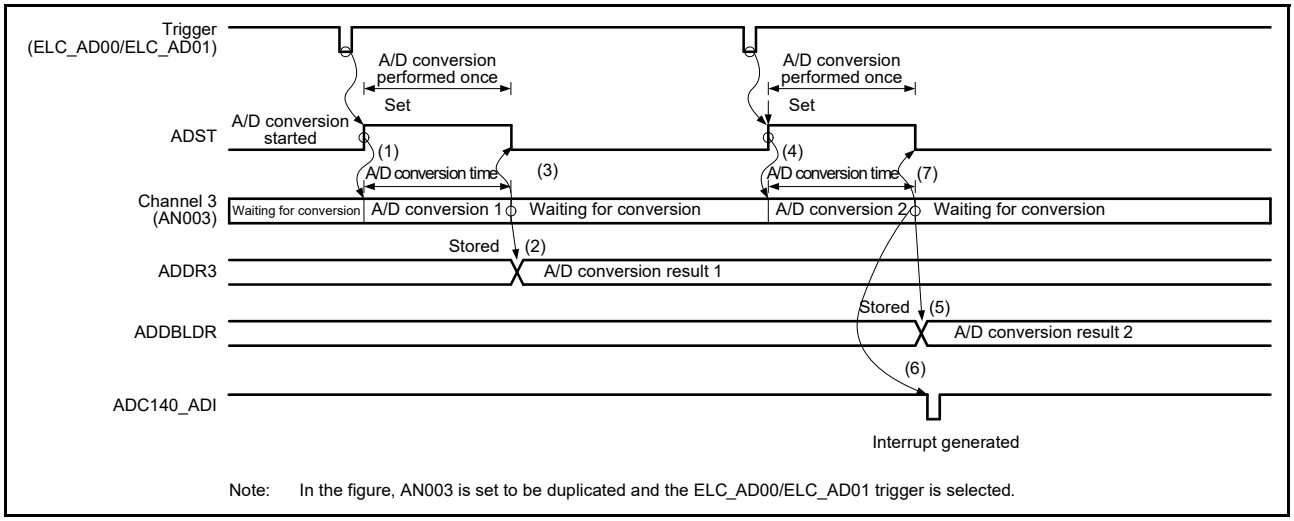


Figure 33.9 Example operation in single scan mode when double trigger mode is selected and AN003 is duplicated

33.3.2.5 Extended operations when double trigger mode is selected

When double trigger mode is selected in single scan mode, and a synchronous trigger ELC_AD00/ELC_AD01 is selected as the trigger for the start of A/D conversion, two rounds of single scan operation are performed.

Deselect self-diagnosis and set the Temperature Sensor Output A/D Conversion Select bit (ADEXICR.TSSA), and the Internal Reference Voltage A/D Conversion Select bit (ADEXICR.OCSA) to 0.

Duplication of A/D conversion data is enabled by setting the channel numbers to be duplicated in the ADCSR.DBLANS[4:0] bits and setting the ADCSR.DBLE bit to 1. When the ADCSR.DBLE bit is set to 1, channel selection using the ADANSA0 and ADANSA1 registers is invalid.

In extended double trigger mode, select a synchronous trigger ELC_AD00/ELC_AD01 by setting the ADSTRGR.TRSA[5:0] bits to 0Bh, set the ADCSR.EXTRG bit to 0, and set the ADCSR.TRGE bit to 1. Do not use a software trigger.

The operation is as follows:

1. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by a synchronous trigger input (ELC_AD00/ELC_AD01), A/D conversion starts on the single channel selected in the ADCSR.DBLANS[4:0] bits.
2. When A/D conversion completes, the A/D conversion result is stored in the associated A/D Data Register (ADDRy) and in A/D Data Duplexing Register A (ADDBLDRA) or A/D Data Duplexing Register B (ADDBLDRB) when the trigger of ELC_ADi0 or ELC_ADi1 is input respectively (i = 0, 1).
3. The ADCSR.ADST bit is automatically set to 0 and the ADC14 enters a wait state. An ADC140_ADI interrupt is not generated.
4. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by the second trigger (ELC_AD00/ELC_AD01), A/D conversion starts on the single channel selected in the ADCSR.DBLANS[4:0] bits.
5. When A/D conversion completes, the A/D conversion result is stored in the A/D Data Duplexing Register (ADDBLDR) and in A/D Data Duplexing Register A (ADDBLDRA) or A/D Data Duplexing Register B (ADDBLDRB) when the trigger of ELC_ADi0 or ELC_ADi1 is input respectively (i = 0, 1).
6. An ADC140_ADI interrupt request is generated.
7. The ADCSR.ADST bit remains 1 (A/D conversion start) during A/D conversion and is automatically set to 0 when A/D conversion completes. The ADC14 then enters a wait state.

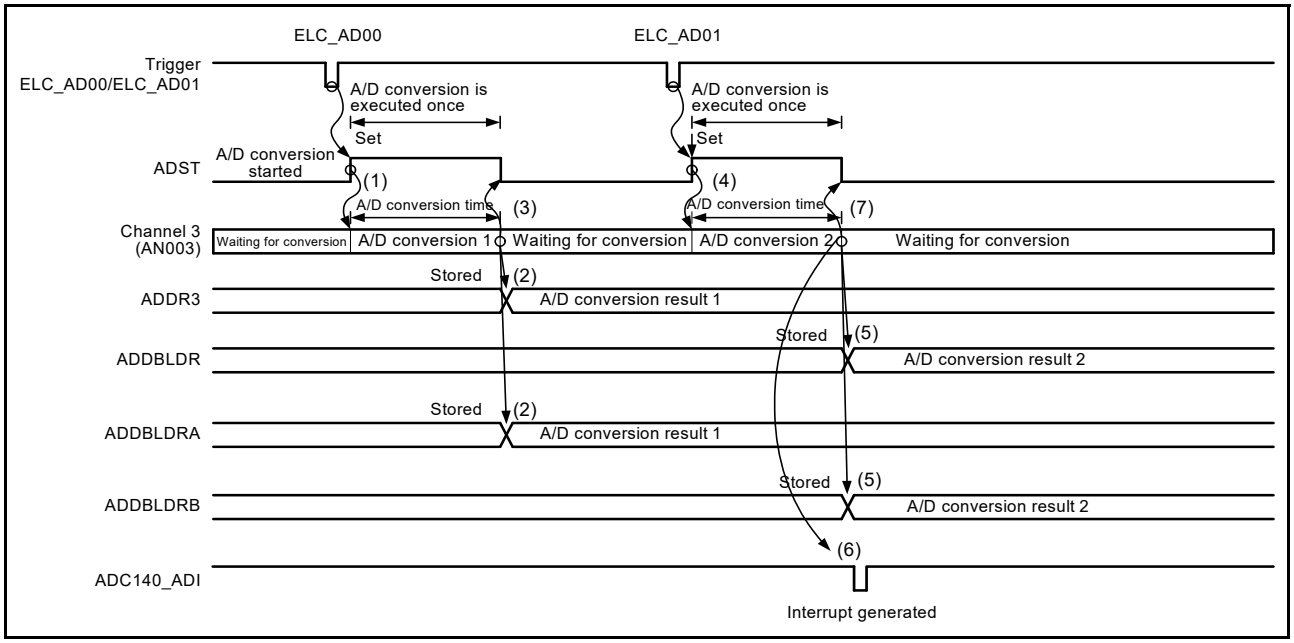


Figure 33.10 Example of extended operation in double trigger mode (1) with duplication selected for AN003 and ELC_AD00/ELC_AD01

33.3.3 Continuous Scan Mode

33.3.3.1 Basic operation

In continuous scan mode, A/D conversion is performed repeatedly on the analog input of the specified channels. In this mode, deselect the temperature sensor output A/D conversion and the internal reference voltage A/D conversion by setting the ADEXICR.TSSA and ADEXICR.OCSA bits to 0.

The operation is as follows:

1. When the ADST bit in ADCSR is set to 1 (A/D conversion start) by a software trigger, a synchronous trigger input (ELC), or an asynchronous trigger input, A/D conversion is performed for ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
2. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register (ADDRy).
3. When A/D conversion of all the selected channels completes, an ADC140_ADI interrupt request is generated. The ADC14 sequentially starts A/D conversion for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
4. The ADST bit in ADCSR is not automatically cleared, and steps 2. and 3. are repeated as long as the bit remains 1 (A/D conversion start). When the ADCSR.ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the ADC14 enters a wait state.
5. When the ADST bit is later set to 1 (A/D conversion start), A/D conversion starts again for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.

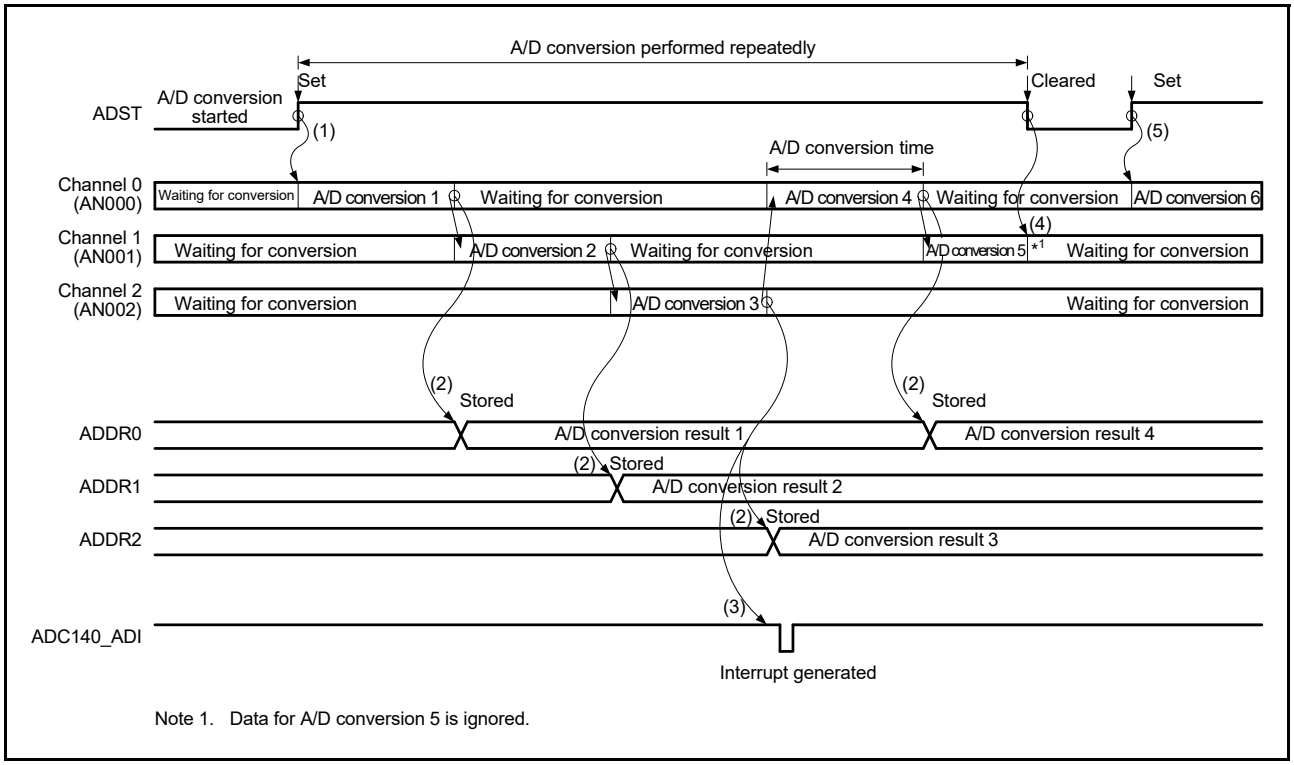


Figure 33.11 Example basic operation in continuous scan mode when AN000 to AN002 are selected

33.3.3.2 Channel selection and self-diagnosis

When channels and self-diagnosis are selected at the same time, A/D conversion is first performed for the reference voltage VREFH0 (×0, ×1/2, or ×1) supplied to the ADC14, and A/D conversion is performed on the analog input of the selected channels. This sequence is repeated as described in the section that follows.

In continuous scan mode, deselect the temperature sensor output A/D conversion and the internal reference voltage A/D conversion by setting the ADEXICR.TSSA and ADEXICR.OCSA bits to 0.

The operation is as follows:

1. A/D conversion for self-diagnosis is first started when the ADST bit in ADCSR is set to 1 (A/D conversion start) by a software trigger, a synchronous trigger input (ELC), or an asynchronous trigger input.
2. When A/D conversion for self-diagnosis completes, the A/D conversion result is stored in the A/D Self-Diagnosis Data Register (ADRD). A/D conversion is then performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
3. Each time A/D conversion of a single channel completes, the A/D conversion result is stored into the associated A/D Data Register (ADDRy).
4. When A/D conversion of all the selected channels completes, an ADC140_ADI interrupt request is generated. At the same time, the ADC14 starts A/D conversion for self-diagnosis and then on the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
5. The ADST bit is not automatically cleared and steps 2. to 4. are repeated as long as the bit remains 1. When the ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the ADC14 enters a wait state.
6. When the ADST bit is later set to 1 (A/D conversion start), the A/D conversion for self-diagnosis is started again.

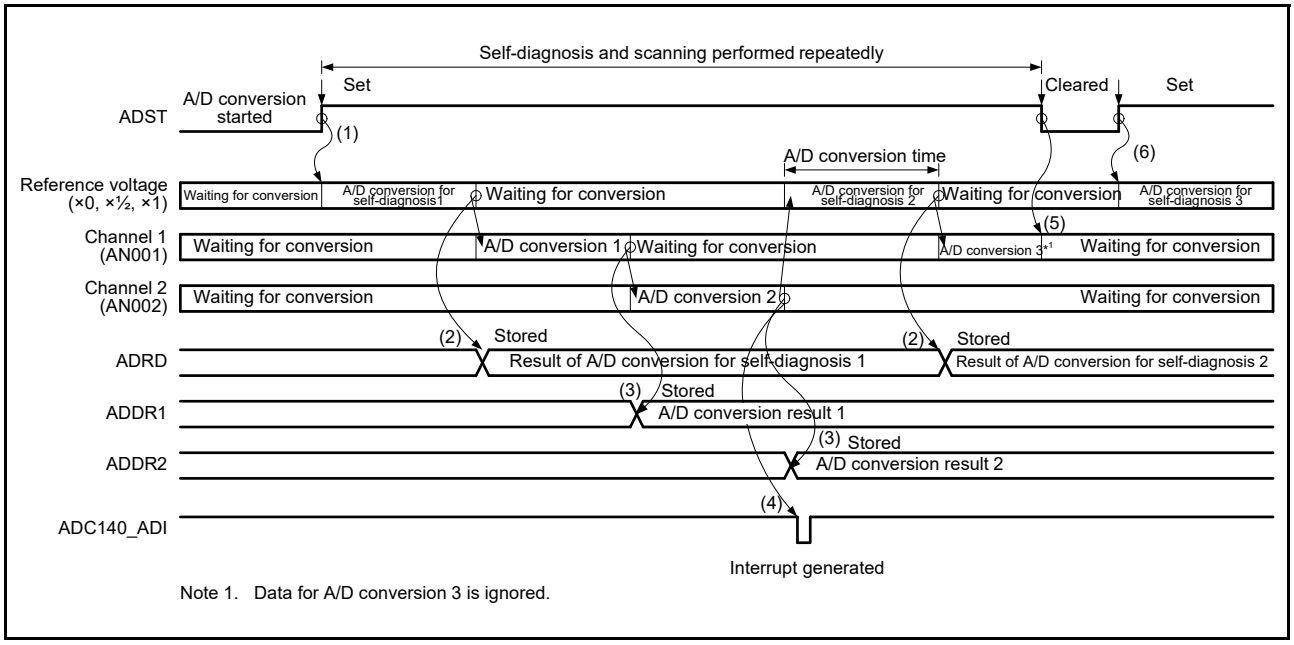


Figure 33.12 Example basic operation in continuous scan mode when AN001 and AN002 are selected with self-diagnosis

33.3.4 Group Scan Mode

33.3.4.1 Basic operation

In group scan mode, A/D conversion is performed once on the analog inputs of all the specified channels in group A or group B after scanning is started by a synchronous trigger (ELC). The scan operation of each group is similar to the scan operation in single scan mode.

The synchronous triggers of group A and B can be selected in the ADSTRGR.TRSA[5:0] bits for group A and in the ADSTRGR.TRSB[5:0] bits for group B. Use different triggers for group A and group B to prevent simultaneous A/D conversion of the two groups. Do not use a software trigger.

Group A channels to be A/D-converted are selected using the ADANSA0 and ADANSA1 registers, while group B channels to be A/D-converted are selected using the ADANSB0 and ADANSB1 registers. Group A and group B cannot use the same channels.

In group scan mode, deselect the temperature sensor output A/D conversion and the internal reference voltage A/D conversion by setting the ADEXICR.TSSA and ADEXICR.OCSA bits to 0. When self-diagnosis is selected in group scan mode, self-diagnosis is separately executed for group A and group B.

The following sequence describes operation in group scan mode using a synchronous trigger from the ELC. In this example, the ELC_AD00 trigger from the ELC is used to start conversion of group A and the ELC_AD01 trigger from the ELC is used to start conversion of group B. In addition, the ELC_AD00 and ELC_AD01 are selected for the GPT event in the associated ELC.ELSRn registers.

The operation is as follows:

1. Scanning of group A is started by ELC_AD00.
2. When group A scanning completes, an ADC140_ADI interrupt is generated.
3. Scanning of group B is started by ELC_AD01.
4. When group B scanning completes, an ADC140_GBADI interrupt is generated if the ADCSR.GBADIE bit is 1 (group B scan end interrupt is enabled).

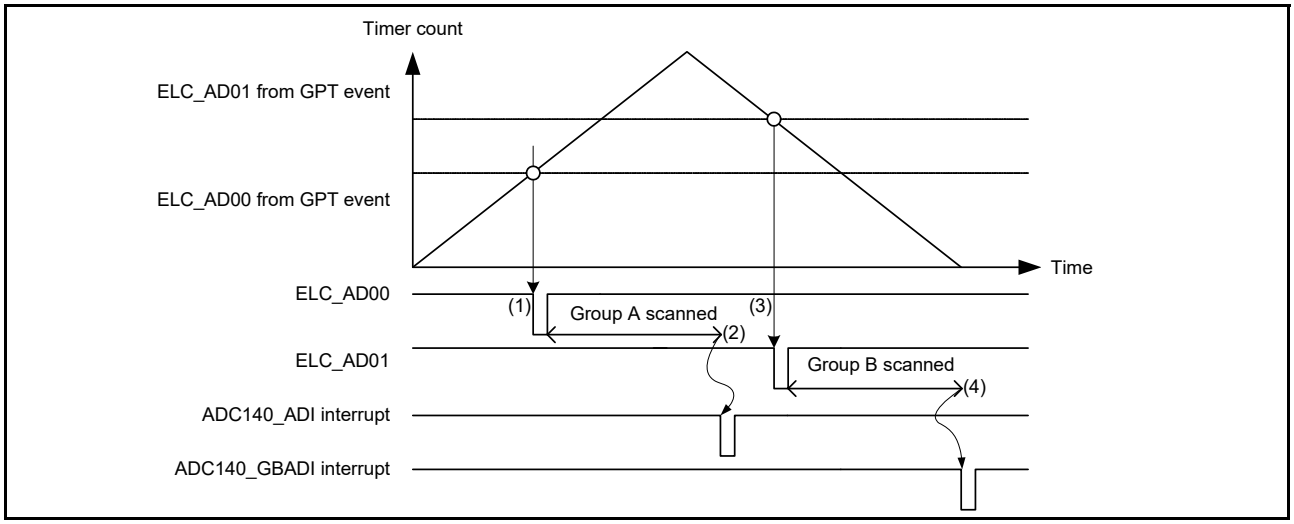


Figure 33.13 Example basic operation in group scan mode when synchronous triggers from the ELC are used

33.3.4.2 A/D conversion in double trigger mode

When double trigger mode is selected in group scan mode, two rounds of single scan operation started by a synchronous trigger (ELC) are performed as a sequence for group A. For group B, single scan operation started by a synchronous trigger (ELC) is performed once.

In group scan mode, the synchronous triggers of group A and B can be selected in the ADSTRGR.TRSA[5:0] bits for group A and in the ADSTRGR.TRSB[5:0] bits for group B. Use different triggers for group A and group B to prevent simultaneous A/D conversion of the two groups. Do not use a software trigger or an asynchronous trigger (ADTRG0).

When an ELC_AD00/ELC_AD01 is selected as group A synchronous triggers by setting the ADSTRGR.TRSA[5:0] bits to 0Bh, operation proceeds in extended double trigger mode.

Group A channel to be A/D-converted is selected using the DBLANS[4:0] bits in the ADCSR register, while group B channels to be A/D-converted are selected using the ADANSB0 and ADANSB1 registers. Group A and group B cannot use the same channels.

In group scan mode, deselect the temperature sensor output A/D conversion and the internal reference voltage A/D conversion by setting the ADEXICR.TSSA and ADEXICR.OCSA bits to 0.

Self-diagnosis cannot be selected when double trigger mode is selected in group scan mode.

Duplication of A/D conversion data is enabled by setting the channel numbers to be duplicated in the DBLANS[4:0] bits in ADCSR and setting the DBLE bit in ADCSR to 1.

The following sequence describes operation in group scan mode with double trigger mode and using a synchronous trigger from the ELC. In this example, the ELC_AD00 trigger is used to start conversion of group A and the ELC_AD01 trigger is used to start conversion of group B. Also, the ELC_AD00 and ELC_AD01 are selected for the GPT event in the associated ELC.ELSRn registers.

The operation is as follows:

1. Scanning of group B is started by the ELC_AD00 trigger from the ELC.
2. When group B scanning completes, an ADC140_GBADI interrupt is generated if the GBADIE bit in ADCSR is 1 (group B scan end interrupt is enabled).
3. The first scanning of group A is started by the first ELC_AD01 trigger.
4. When the first scanning of group A completes, the conversion result is stored in the associated A/D Data Register (ADDRy). An ADC140_ADI interrupt request is not generated.
5. The second scanning of group A is started by the second ELC_AD01 trigger.
6. When the second scanning of group A completes, the conversion result is stored in the ADDBLDR register. An ADC140_ADI interrupt is generated.

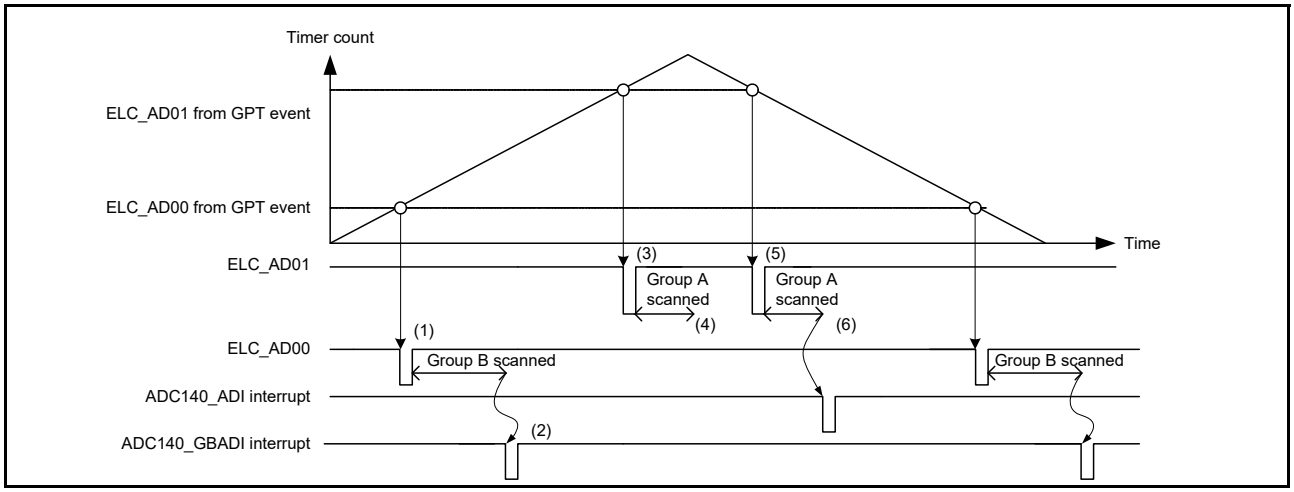


Figure 33.14 Example of operation in group scan mode with double trigger mode using synchronous triggers from the ELC

33.3.4.3 Operation under group A priority control

Setting the ADGSPCR.PGS bit to 1 in group scan mode enables operation to proceed under group A priority control. When setting the PGS bit in the ADGSPCR register to 1, follow the procedure described in Figure 33.15. If the procedure is not followed, A/D conversion operation and stored data are not guaranteed.

In basic group scan mode, while A/D conversion is underway for group A or group B, input of the trigger for A/D conversion for the other group is ignored. Under group A priority control, if a group A trigger is input during A/D conversion for group B, A/D conversion for group B is discontinued and A/D conversion for group A proceeds. If the setting of the ADGSPCR.GBRSCN bit is 0, the ADC14 enters wait state on completion of the A/D conversion for group A. If the setting of the ADGSPCR.GBRSCN bit is 1, the ADC14 automatically restarts scanning for group B from the start of the group after completion of the A/D conversion for group A. Table 33.9 summarizes operations in response to the input of a trigger during A/D conversion with the ADGSPCR.GBRSCN bit.

Scan operations in group A or group B are the same in single scan mode. Additionally, single scanning continues to proceed when the ADGSPCR.GBRP bit is set to 1 during scanning operations for group B.

For the trigger settings in group scan mode, select a synchronous trigger for group A using the ADSTRGR.TRSA[5:0] bits and select a synchronous trigger for group B, different from that of group A, using the ADSTRGR.TRSB[5:0] bits. Set the ADSTRGR.TRSB[5:0] bits to 3Fh when setting the ADGSPCR.GBRP bit to 1.

Additionally, as targets for A/D conversion, select channels for group A using the ADANSA0 and ADANSA1 registers. For group B, select channels different from those for group A, using the ADANSB0 and ADANSB1 registers.

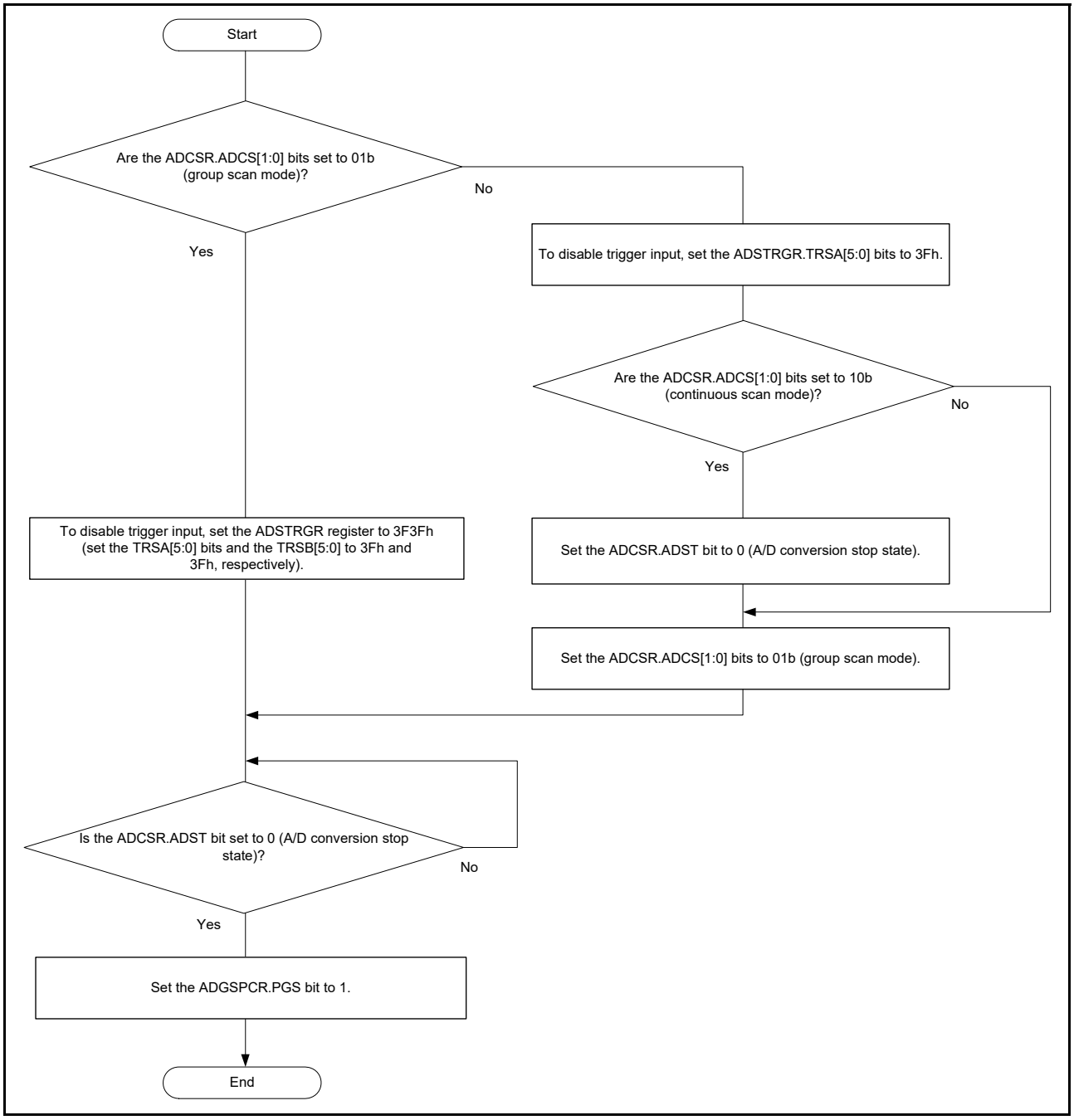


Figure 33.15 Flow for setting ADGSPCR.PGS bit

Table 33.9 Control of A/D conversion operations according to settings of ADGSPCR.GBRSCN bit (1 of 2)

A/D conversion operation	Trigger input	ADGSPCR.GBRSCN = 0	ADGSPCR.GBRSCN = 1
When A/D conversion for group A is in progress	Input of trigger for group A	Trigger input is ineffective	Trigger input is ineffective
	Input of trigger for group B	Trigger input is ineffective	A/D conversion is performed on group B after A/D conversion on group A completes

Table 33.9 Control of A/D conversion operations according to settings of ADGSPCR.GBRSCN bit (2 of 2)

A/D conversion operation	Trigger input	ADGSPCR.GBRSCN = 0	ADGSPCR.GBRSCN = 1
When A/D conversion for group B is in progress	Input of trigger for group A	Conversion for group B that is in progress is discontinued and conversion for group A starts	• Conversion in progress for group B is discontinued and conversion for group A starts • Conversion for group B starts after conversion for group A completes.
	Input of trigger for group B	Trigger input is ineffective	Trigger input is ineffective

The following sequence describes the operations in group scan mode under group A priority control (ADGSPCR.GBRSCN = 1 and ADGSPCR.GBRP = 0) when channel 0 is selected for group A and channels 1 to 3 are selected for group B.

1. When input of a trigger for group B sets the ADCSR.ADST bit to 1 (A/D conversion start), conversion for the ANn channels selected in the ADANSB0 and ADANSB1 registers starts in order from the channel with the smallest number n.
2. On completion of A/D conversion, the result is stored in the associated A/D Data Register (ADDRy).
3. When a group A trigger is input while A/D conversion for group B is in progress, and A/D conversion for group B is discontinued with the ADCSR.ADST bit remains 1, A/D conversion for the ANn channels selected in the ADANSA0 and ADANSA1 registers starts in order from the channel with the smallest number n. If A/D conversion is not complete when the A/D conversion of group B is interrupted, the A/D conversion result is not stored in the A/D Data Register (ADDRy).
4. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register (ADDRy).
5. An ADC140_ADI interrupt request is generated.
6. A/D conversion for the ANn channels in group B selected in the ADANSB0 and ADANSB1 registers restarts in order from the channel with the smallest number n with the ADCSR.ADST bit remains 1.
7. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register (ADDRy).
8. An ADC140_GBADI interrupt request is generated if the setting of the ADCSR.GBADIE bit is 1 (group B scan end interrupt is enabled).
9. The ADCSR.ADST bit is automatically cleared and the 16-bit A/D converter enters the wait state when A/D conversion completes.

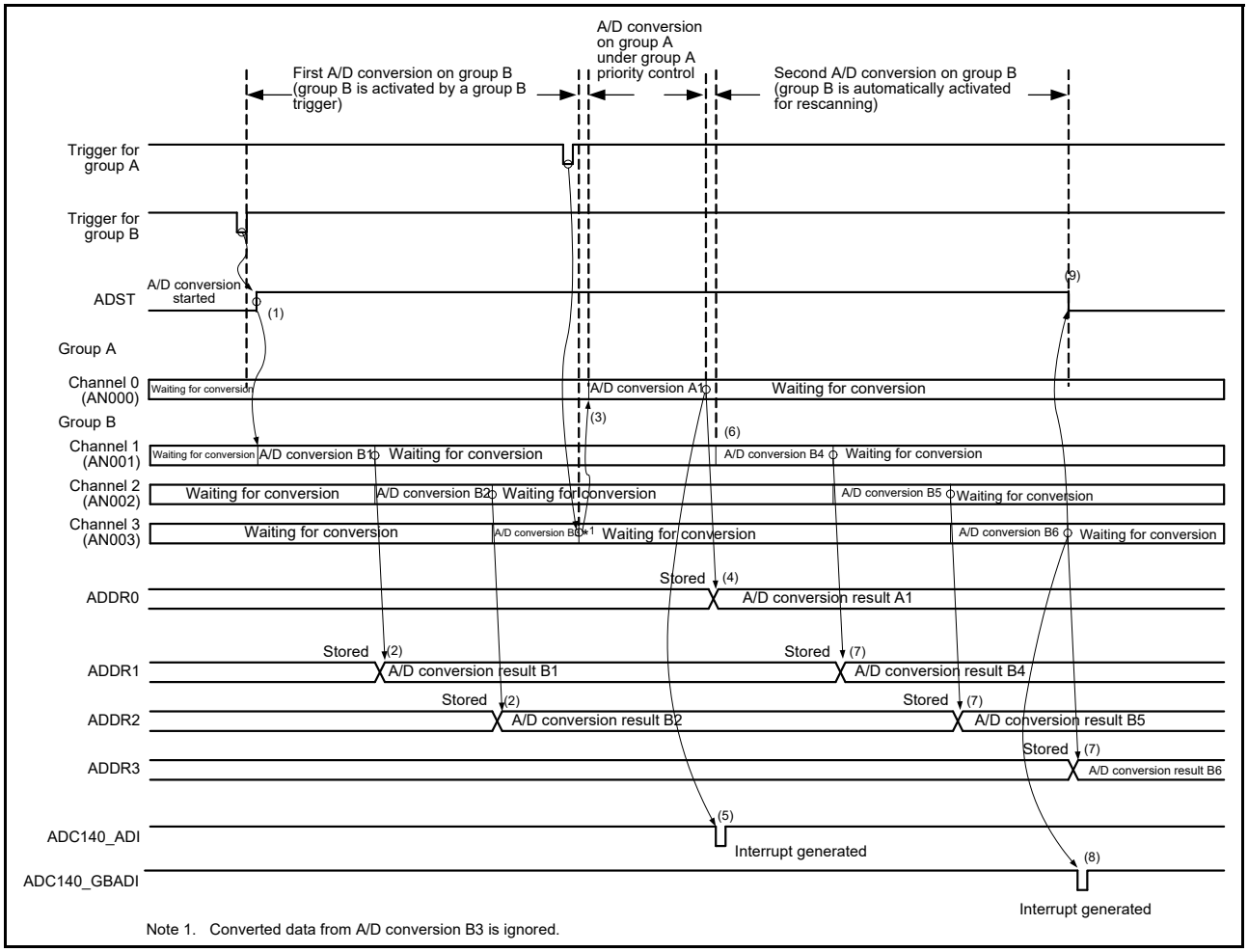


Figure 33.16 Example operation with group A priority control (1) when ADGSPCR.GBRSCN = 1 and ADGSPCR.GBRP = 0

The following sequence is an example when a group A trigger is input again during rescanning operation on group B. In this example, channel 0 is selected for group A and channels 1 to 3 are selected for group B when operation on group A is given priority (ADGSPCR.GBRSCN = 1, ADGSPCR.GBRP = 0).

1. When a group B trigger input sets the ADCSR.ADST bit to 1 (A/D conversion start), conversion for the ANn channels of group B selected in the ADANSB0 and ADANSB1 registers starts in order from the channel with the smallest number n.
2. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register (ADDRy).
3. When a group A trigger is input while A/D conversion for group B is in progress, and A/D conversion for group B is discontinued with the ADCSR.ADST bit remains 1. If A/D conversion is not complete when the A/D conversion of group B is interrupted, A/D conversion result is not stored in the A/D Data Register (ADDRy).
4. A/D conversion for the ANn group A channels selected in the ADANSA0 and ADANSA1 registers starts in order from the channel with the smallest number n.
5. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register (ADDRy).
6. An ADC140_ADI interrupt request is generated.
7. On completion of A/D conversion on group A, rescanning operation on group B sets the ADCSR.ADST bit to 1 automatically if the ADGSPCR.GBRSCN bit is 1 (enabling rescanning operation). A/D conversion for the ANn group B channels selected in the ADANSB0 and ADANSB1 registers then starts again in order from the channel with the smallest number n.

8. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register (ADDRy).
9. If the ADGSPCR.GBRSCN bit is 1 when the A/D conversion of group A completes, the ADCSR.ADST bit remains 1 and the group B is rescanned. A/D conversion for the ANn group B channels selected in the ADANSB0 and ADANSB1 registers starts again in order from the channel with the smallest number n.
10. A/D conversion for the ANn group A channels selected in the ADANSA0 and ADANSA1 registers starts in order from the channel with the smallest number n.
11. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register (ADDRy).
12. An ADC140_ADI interrupt request is generated.
13. If the ADGSPCR.GBRSCN bit is 1 when the A/D conversion of group A completes, the ADCSR.ADST bit remains 1 and group B is rescanned. A/D conversion for the ANn group B channels selected in the ADANSB0 and ADANSB1 registers starts again in order from the channel with the smallest number n.
14. If a group A trigger is input during A/D conversion on group B for rescanning, steps 9. to 13. are repeated. If a group A trigger is not input, the ADCSR.ADST bit is cleared automatically on completion of A/D conversion on group B and the ADC14 enters a wait state.

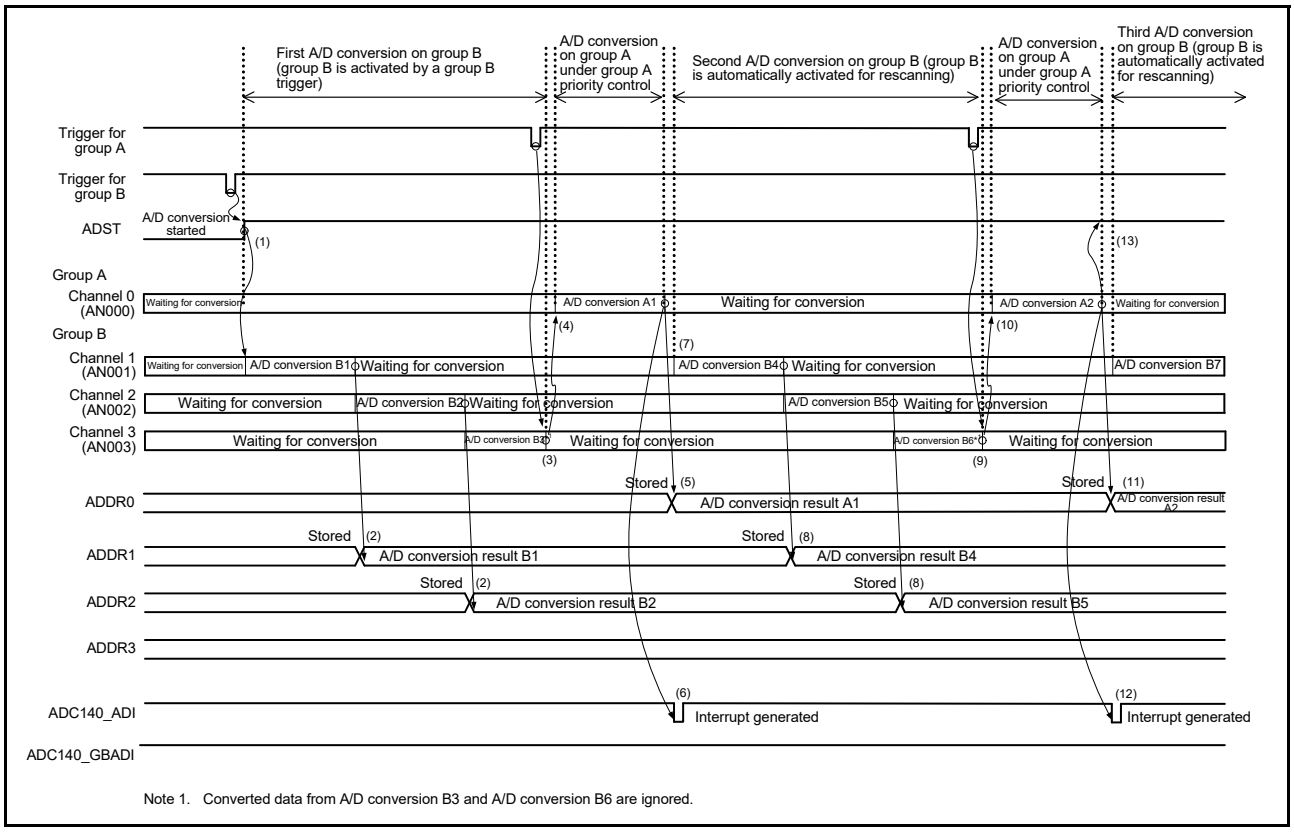


Figure 33.17 Example operation with group A priority control (2) when ADGSPCR.GBRSCN = 1 and ADGSPCR.GBRP = 0

The following sequence is an example of a rescanning operation in which a group B trigger is input during A/D conversion on group A. In this example, channels 1 to 3 are selected for group A and channel 0 is selected for group B when operation on group A is given priority (ADGSPCR.GBRSCN = 1, ADGSPCR.GBRP = 0).

1. When input of a group A trigger sets the ADCSR.ADST bit to 1 (A/D conversion start), conversion for the ANn channels selected in the ADANSA0 and ADANSA1 registers starts in order from the channel with the smallest number n.
2. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register (ADDRy).

3. If a group B trigger is input during A/D conversion on group A, A/D conversion on group B can be performed after the A/D conversion on group A completes. However, if group A triggers are input continuously, the scan operation on group B is canceled by group A and is not performed.
4. On completion of the A/D conversion on the group A, an ADC140_ADI interrupt request is generated without register setting.
5. On completion of group A conversion, the ADCSR.ADST bit remains 1 and group B is rescanned. A/D conversion for the ANn channels of group B selected in the ADANSB0 and ADANSB1 registers starts in order from the channel with the smallest number n.
6. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register (ADDRy).
7. On completion of the rescanning operation on group B, an ADC140_GBADI interrupt request is generated if the setting of the ADCSR.GBADIE bit is 1 (group B scan end interrupt is enabled).
8. The ADCSR.ADST bit is automatically cleared and the 16-bit A/D converter enters the wait state when A/D conversion completes.

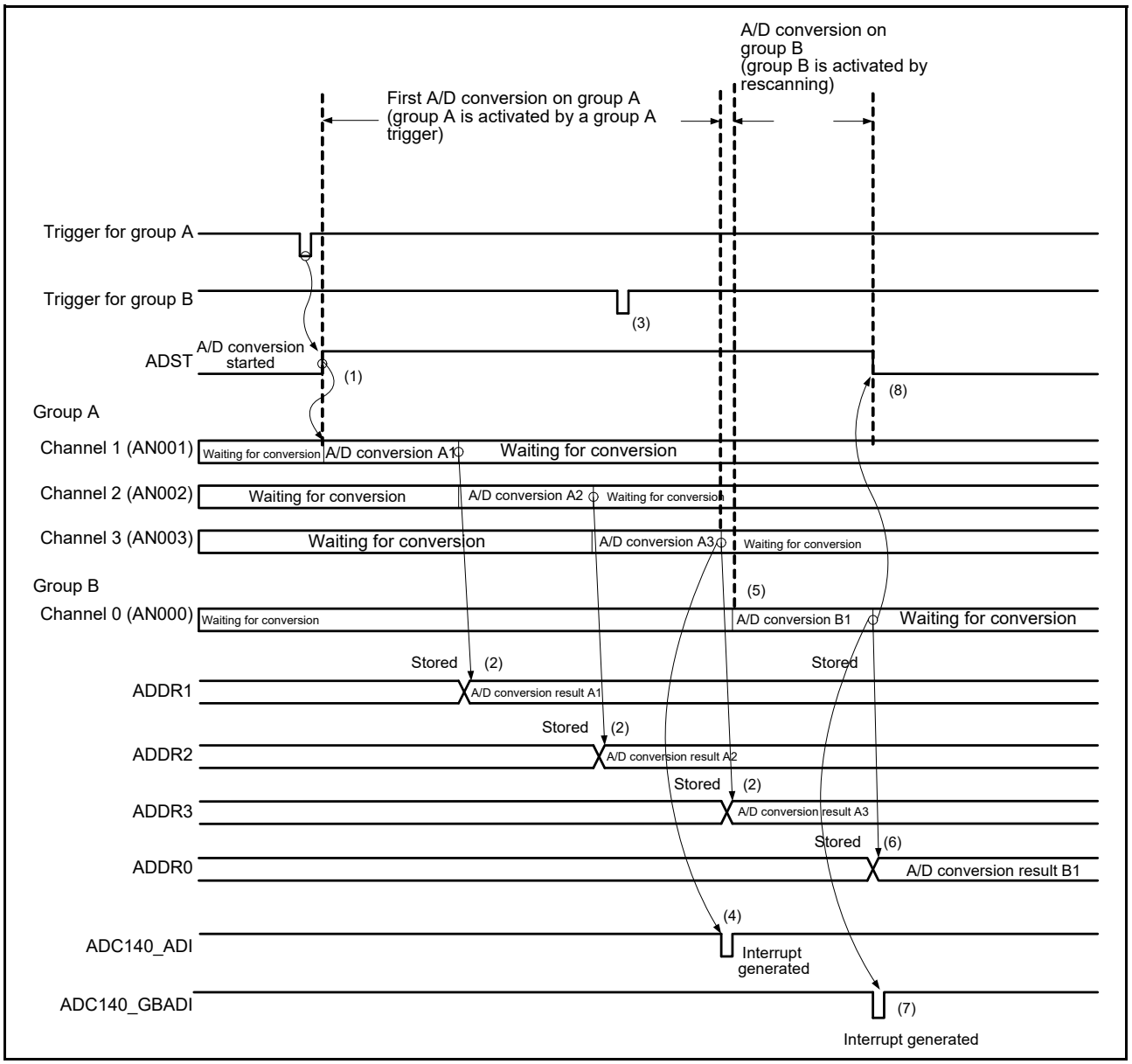


Figure 33.18 Example operation with group A priority control (3) when ADGSPCR.GBRSCN = 1 and ADGSPCR.GBRP = 0

The following sequence is an example of operation under group A priority control in which channel 0 is selected for group A and channels 1 to 3 are selected for group B (ADGSPCR.GBRSCN = 0, ADGSPCR.GBRP = 0).

1. When input of a trigger for group B sets the ADCSR.ADST bit to 1 (A/D conversion start), conversion for the ANn channels selected in the ADANSB0 and ADANSB1 registers starts in order from the channel with the smallest number n.
2. On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D Data Register (ADDRy).
3. If a group A trigger is input while A/D conversion for group B is in progress, and A/D conversion for group B is discontinued with the ADCSR.ADST bit remains 1. A/D conversion for the ANn channels selected in the ADANSA0 and ADANSA1 registers starts in order from the channel with the smallest number n.
4. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register (ADDRy).
5. An ADC140_ADI interrupt request is generated.
6. The ADCSR.ADST bit is automatically cleared and the 16-bit A/D converter enters the wait state when A/D conversion completes.

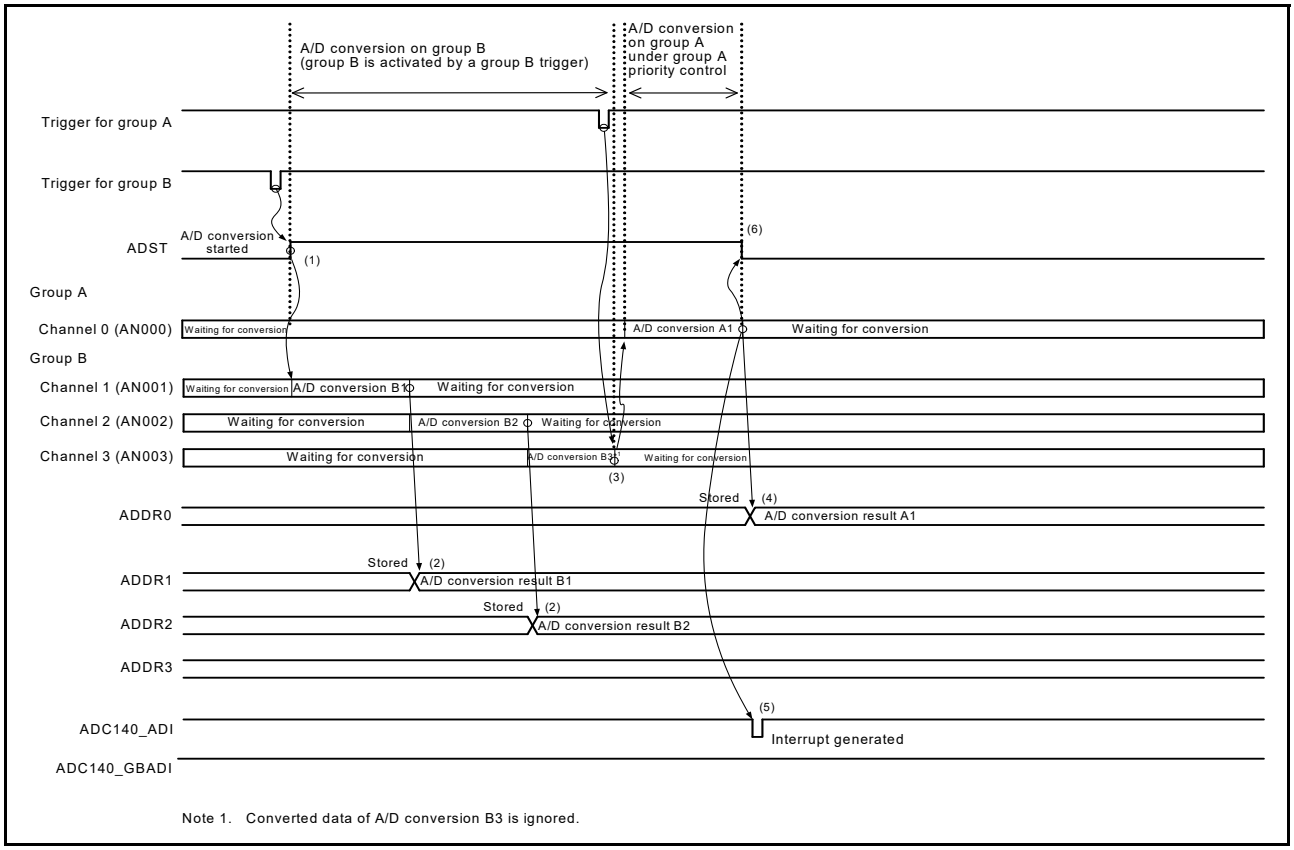


Figure 33.19 Example operation with group A priority control (4) when ADGSPCR.GBRSCN = 0 and ADGSPCR.GBRP = 0

The following sequence is an example of operation under group A priority control in which channel 0 is selected for group A and channels 1 to 3 are selected for group B (ADGSPCR.GBRP = 1).

1. The ADCSR.ADST bit is set to 1 (A/D conversion start) when ADGSPCR.GBRP is set to 1, and conversion for the ANn channels selected in the ADANSB0 and ADANSB1 registers starts in order from the channel with the smallest number n.
2. On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D Data Register (ADDRy).
3. If a group A trigger is input while A/D conversion for group B is in progress, and A/D conversion for group B is

discontinued with the ADCSR.ADST bit remains 1. A/D conversion for the ANn channels selected in the ADANSA0 and ADANSA1 registers starts in order from the channel with the smallest number n.

4. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register (ADDRy).
5. An ADC140_ADI interrupt request is generated.
6. A/D conversion for the ANn channels in group B selected in the ADANSB0 and ADANSB1 registers restarts in order from the channel with the smallest number n with the ADCSR.ADST bit remains 1.
7. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register (ADDRy).
8. An ADC140_GBADI interrupt request is generated if the ADCSR.GBADIE bit is 1.
9. A/D conversion for the ANn channels selected in the ADANSB0 and ADANSB1 registers starts in order from the channel with the smallest number n. Steps 6. to 9. are repeated as long as the ADGSPCR.GBRP bit remains 1. Setting the ADCSR.ADST bit to 0 is prohibited while the ADGSPCR.GBRP bit is set to 1. To forcibly stop A/D conversion when ADGSPCR.GBRP = 1, follow the procedure shown in Figure 33.31.

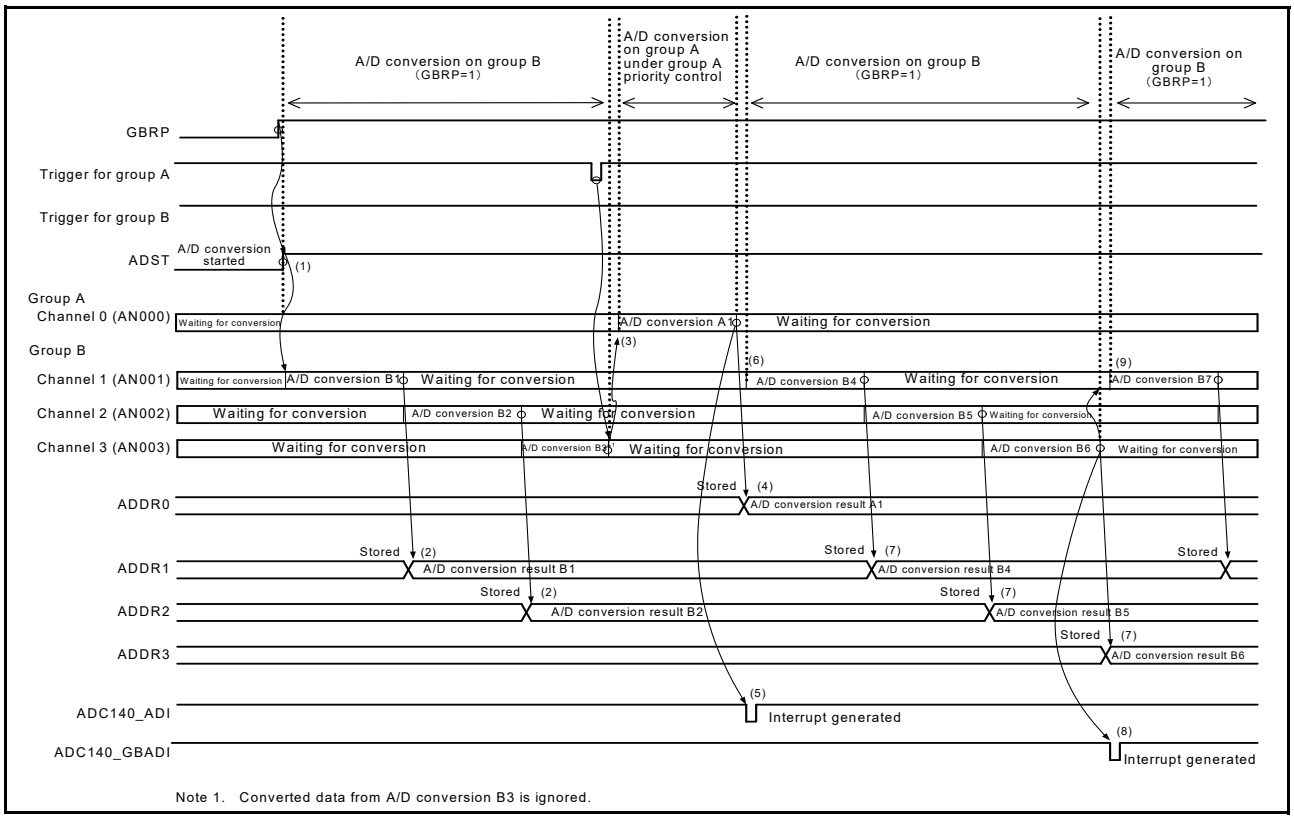


Figure 33.20 Example operation with group A priority control (5) when ADGSPCR.GBRP = 1

33.3.5 Compare Function (Window A, Window B)

33.3.5.1 Compare function window A and window B

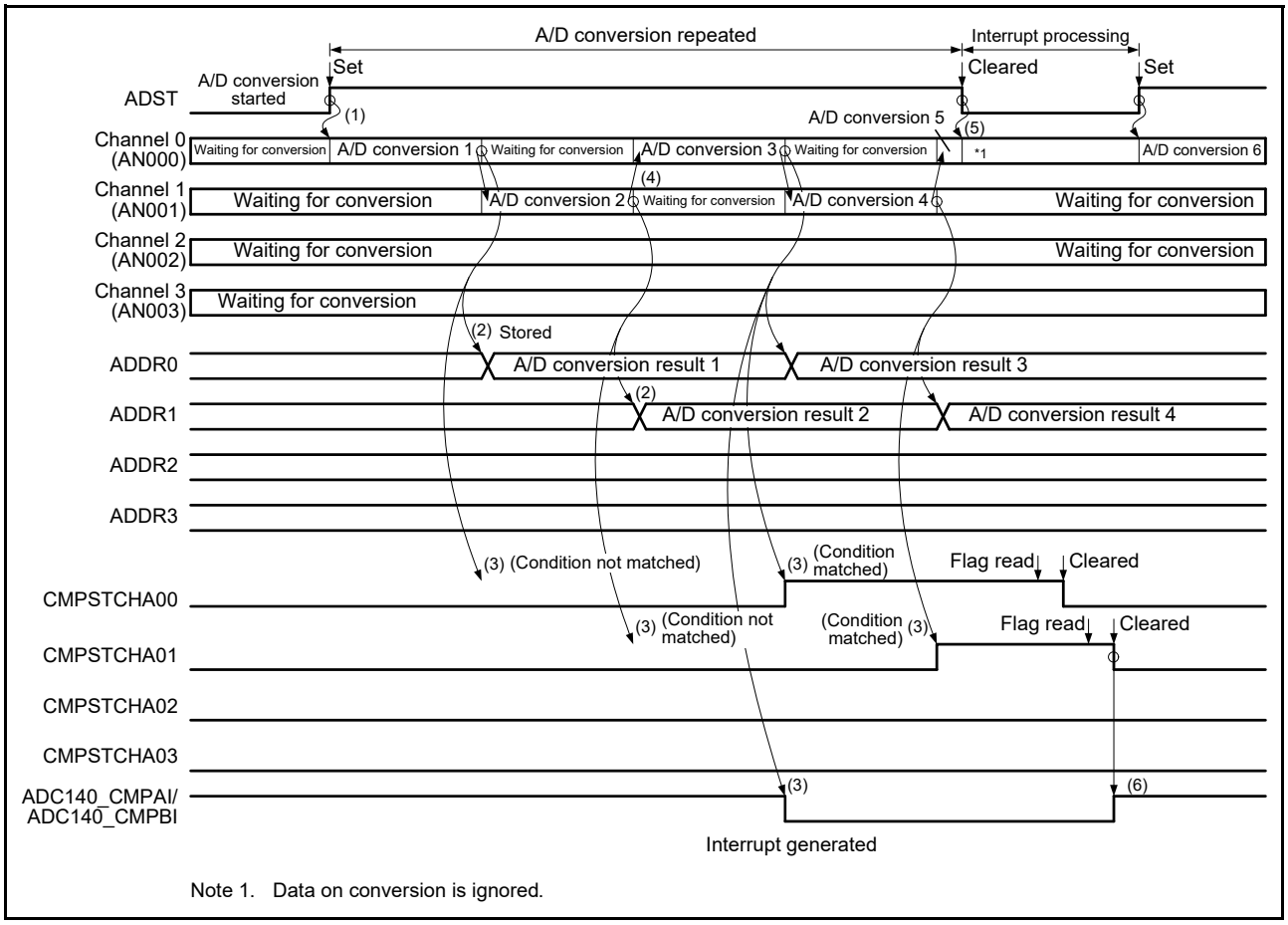
The compare function compares a reference value with the A/D conversion result. The reference value can be set for window A and window B independently. When the compare function is in use, the self-diagnosis function and double trigger mode cannot be used. The main differences between window A and window B are their different interrupt output signals and the limitation that window B can select only one channel.

The following sequence describes an example operation that combines continuous scan mode and the compare function.

1. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by software, a synchronous trigger (ELC) or an asynchronous trigger, A/D conversion starts in the order of the selected channel. Both temperature sensor and

internal reference voltage are not selectable at the same time. Additionally, when the internal reference voltage is selected as the high-potential reference voltage, A/D conversion of the temperature sensor or internal reference voltage is prohibited.

2. On completion of A/D conversion, the A/D conversion result is stored in the associated A/D Data Register (ADDRy, ADTSDR, or ADOCDR). When ADCMPCR.CMPAE is 1, if bits in the ADCMPANSRy register or the ADCMPANSER register are set for window A, the A/D conversion result is compared with the ADCMPDR0/1 register value. When ADCMPCR.CMPBE is 1, if bits in the ADCMPBNSR register are set for window B, the A/D conversion result is compared with the ADWINULB/ADWINLLB register value.
3. As a result of the comparison, when window A meets the condition set in ADCMPLR0/1 or ADCMPLER, the Compare Window A Flag (ADCMPSR0.CMPSTCHAn, ADCMPSR1.CMPSTCHAn, ADCMPSER.CMPSTTSA, or ADCMPSER.CMPSTOCA) is set to 1. If the ADCMPCR.CMPAIE bit is 1, an ADC140_CMPAI interrupt request (level) is generated. In the same way, when window B meets the condition set in ADCMPBNSR.CMPLB, the Compare Window B Flag (ADCMPBSR.CMPSTB) is set to 1. If the ADCMPCR.CMPBIE bit is 1, an ADC140_CMPBI interrupt request (level) is generated.
4. On completion of all selected A/D conversions and comparisons, scan restarts.
5. After the ADC140_CMPAI and ADC140_CMPBI interrupts are accepted, the ADCSR.ADST bit is set to 0 (A/D conversion stop) and processing is performed for channels in which the compare flag is set to 1.
6. When all compare flags of window A are cleared, the ADC140_CMPAI interrupt request is canceled. In the same way, when all compare flags of window B are cleared, the ADC140_CMPBI interrupt request is canceled. To perform comparison again, restart the A/D conversion.



Note 1. Data on conversion is ignored.

Figure 33.21 Example of compare function operation when AN000 to AN003 are compared

33.3.5.2 Event output of compare function

The event output of the compare function specifies the upper reference voltage value and the lower reference voltage value for window A and window B, respectively. The output compares the A/D converted value of the selected channel with the upper and lower side reference voltage value and outputs events (ADC140_WCMPM/ADC140_WCMPUM) based on event conditions (A or B, A and B, A xor B) and comparison result of window A and window B.

If more than one channel is selected for window A, and even when one channel in window A meets the comparison condition, the comparison result of window A is met. When using this function, perform A/D conversion in single scan mode.

Any channels from AN000 to AN013, AN016 to AN022, internal reference voltage, and temperature sensor output are selectable for window A. However, neither the internal reference voltage nor the temperature sensor output can be selected together with any other channel. Additionally, if the internal reference voltage is selected as the high-potential reference voltage of the A/D converter, the internal reference voltage or the temperature sensor output cannot be A/D converted.

One channel from AN000 to AN013, AN016 to AN022, internal reference voltage, and temperature sensor output is selectable for window B. Additionally, if the internal reference voltage is selected as the high-potential reference voltage, the internal reference voltage or the temperature sensor output cannot be A/D converted.

The following sequence is an example of how to set up and use the event output of the compare function.

1. Confirm that the value of the ADCSR.ADCS[1:0] bits is 00b (single scan mode).
2. Select the channel for window A in the ADCMPANSR0/1 and ADCMPANSER registers. Set the window comparison conditions in registers the ADCMPLR0/1, ADCMPLER registers. Set the upper and lower reference values in the ADCMPDR0/1 registers.
3. Select the channel and comparison conditions for window B in the ADCMPBNSR register, and set the upper and lower reference values in the ADWINULB/ADWINLLB registers.
4. Set the composite conditions for window A/B, window A/B operation enable, and interrupt output enable in the ADCMPCR register.

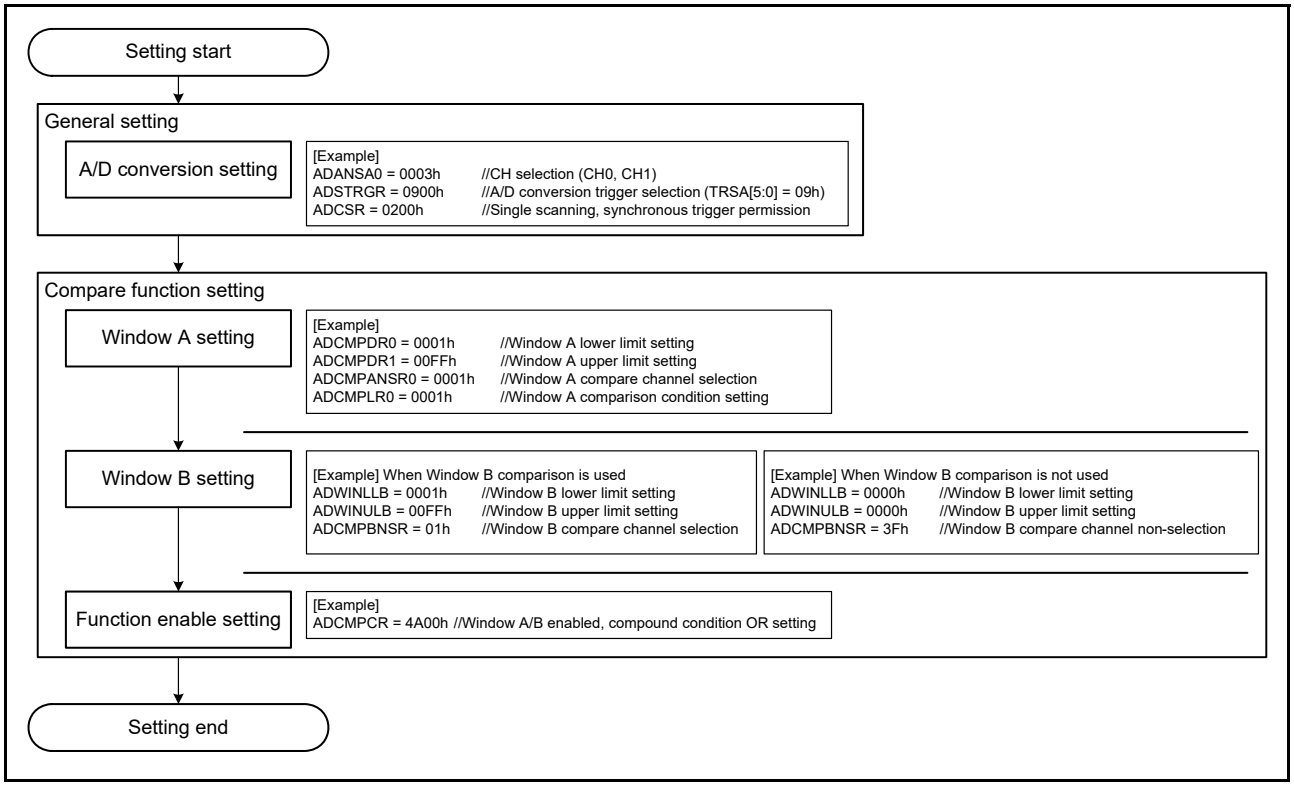


Figure 33.22 Setting example when using event output of the compare function

For event output usage when using only window A for the compare function, note the following:

- Enable both window A and window B (ADCMPCR.CMPAE = 1, ADCMPCR.CMPBE = 1)
- Set the compound condition of window A and B to the OR condition (ADCMPCR.CMPAB[1:0] = 00b)
- Set the compared channel of window B to Do not select (ADCMPBNSR.CMPCHB[5:0] = 111111b)
- Set the compare condition of window B to 0 < results < 0 means always mismatch (ADCMPCR.WCMPE = 1, ADWINLLB.CMPLLB[15:0] = ADWINULB.CMPULB[15:0] = 0000h, and ADCMPBNSR.CMPLB = 1).

Figure 33.23 shows an event output operation example of the compare function.

A scan end event (ADC140_ADI) is output with the same timing as single scan completion. A match or mismatch event (ADC140_WCMPM/ADC140_WCMPUM) is output with 1 PCLKB cycle delay depending on the ADCMPCR.CMPAB[1:0] settings.

Note: The match and mismatch events are exclusive, so both events do not output simultaneously.

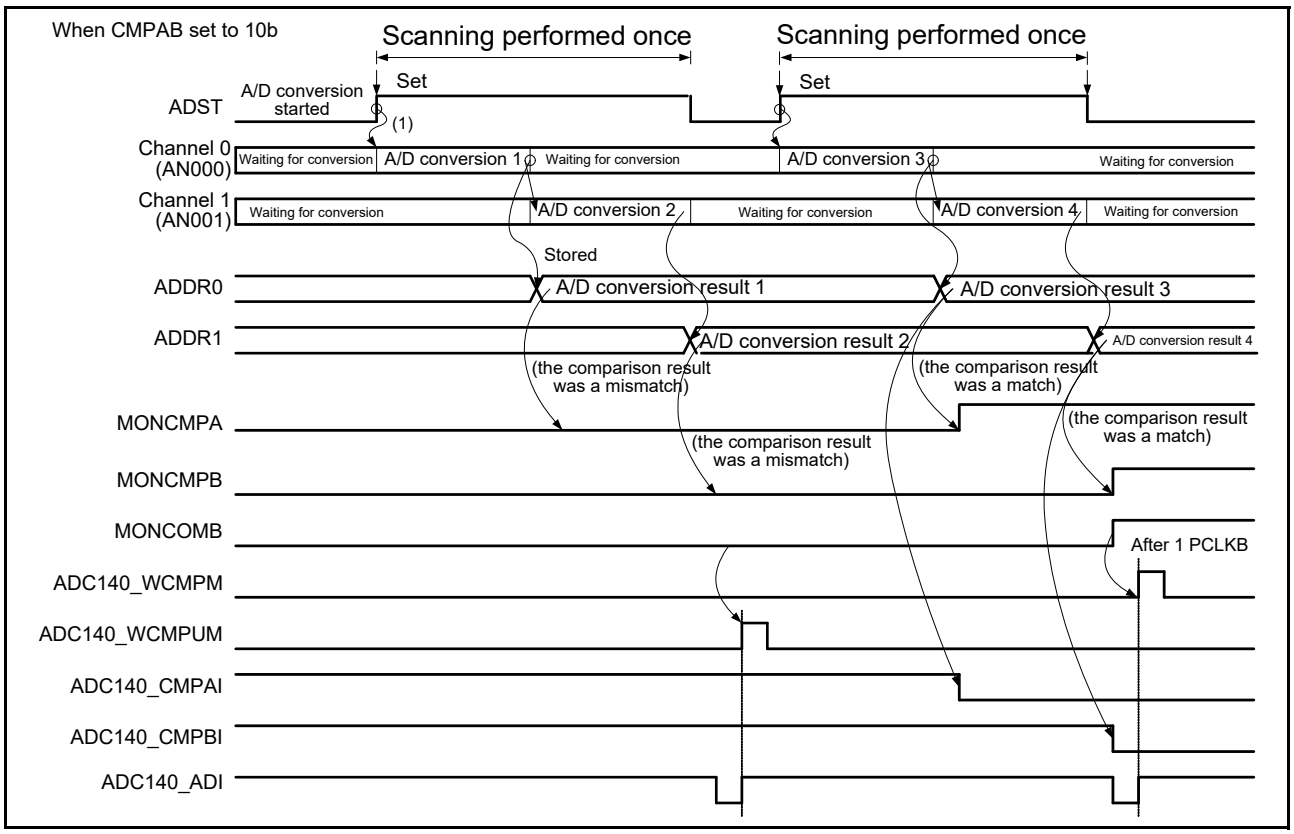


Figure 33.23 Event output operation example of the compare function when AN000 to AN001 are compared

Note: Event output of compare function outputs match/mismatch from the comparison results of window A and window B, according to the ADCMPCR.CMPAB[1:0] settings.

Note: The comparison result of window A is the logical addition of the comparison results of comparison target channels of window A. The comparison results of window A and B are updated by each A/D conversion, and are kept even when single scan ends. Set ADCMPCR.CMPAE and ADCMPCR.CMPBE to 0 to clear the comparison results to 0.

33.3.5.3 Restrictions for compare function

The following restrictions apply to the compare function:

- The compare function cannot be used together with the self-diagnosis function or double trigger mode. The compare function is not available for ADRD, ADDBLDR, ADDBLDRA, and ADDBLDRB.
- Specify single scan mode when using match/mismatch event outputs

- When the temperature sensor or internal reference voltage is selected for window A, window B operations are disabled
- When the temperature sensor or internal reference voltage is selected for window B, window A operations are disabled
- Setting the same channel for window A and window B is prohibited
- Set the reference voltage values so that the high-potential reference voltage value is equal or larger than the low-potential reference voltage value.

33.3.6 Analog Input Sampling and Scan Conversion Time

Scan conversion can be activated either by a software trigger, a synchronous trigger (ELC), or an asynchronous trigger (ADTRG0). After the start-of-scanning-delay time (t_D) has elapsed, processing for disconnection detection assistance, and processing of conversion for self-diagnosis all proceed, followed by processing for A/D conversion.

Figure 33.24 shows the scan conversion timing, in which scan conversion is activated by a software trigger or a synchronous trigger (ELC). Figure 33.25 shows the scan conversion timing, in which scan conversion is activated by an asynchronous trigger ADTRG0. The scan conversion time (t_{SCAN}) includes the start-of-scanning-delay time (t_D), disconnection detection assistance processing time (t_{DIS})*1, self-diagnosis A/D conversion processing time (t_{DIAG} and t_{DSD})*2, A/D conversion processing time (t_{CONV}), and end-of-scanning-delay time (t_{ED}).

The A/D conversion processing time (t_{CONV}) consists of input sampling time (t_{SPL}) and time for conversion by successive approximation (t_{SAM}). The sampling time (t_{SPL}) is used to charge sample-and-hold circuits in the A/D converter. If there is not sufficient sampling time due to the high impedance of an analog input signal source, or if the A/D conversion clock (ADCLK) is slow, sampling time can be adjusted using the ADSSTR register.

The time for conversion by successive approximation (t_{SAM}) is of the following:

- 37.5 ADCLK states with 14-bit accuracy and high-speed mode selected
- 46.5 ADCLK states with 14-bit accuracy and low-current mode selected
- 31.5 ADCLK states with 12-bit accuracy and high-speed mode selected
- 40.5 ADCLK states with 12-bit accuracy and low-current mode selected.

Table 33.10 shows the scan conversion time.

The scan conversion time (t_{SCAN}) in single scan mode for which the number of selected channels is *n* can be determined as follows:

$$t_{SCAN} = t_D + (t_{DIS} \times n) + t_{DIAG} + t_{DSD} + (t_{CONV}{}^{*3} \times n) + t_{ED}$$

The scan conversion time for the first cycle in continuous scan mode is t_{SCAN} for single scan minus t_{ED}. The scan conversion time for the second and subsequent cycles in continuous scan mode is fixed at $(t_{DIS} \times n) + t_{DIAG} + t_{DSD} + (t_{CONV}{}^{*3} \times n)$.

Note 1. When disconnection detection assistance is not selected, $t_{DIS} = 0$.
Only when the temperature sensor or internal reference voltage is A/D-converted, the auto-discharge period of 15 ADCLK states is inserted.

Note 2. When the self-diagnosis function is not used, $t_{DIAG} = 0$, $t_{DSD} = 0$.

Note 3. When input sampling time (tSPL) of all selected channels are the same, this element equals tCONV × n. If each channel has a different sampling time, this element equals the sum of t_{SPL} and t_{SAM} for each selected channel.

Table 33.10 shows the times for conversion during scanning.

Table 33.10 Times for conversion during scanning in numbers of ADCLK and PCLKB cycles

Parameter			Symbol		Type/Conditions			Unit
					Synchronous trigger*5	Asynchronous trigger	Software trigger	
Scan start processing time*1, *2	A/D conversion on group A under group A priority control	Group B is to be stopped (group A is activated after group B is stopped due to an A/D conversion source of group A)	t_D		3 PCLKB + 6 ADCLK, 5 PCLKB + 3 ADCLK*6	—	—	Cycle
		Group B is not to be stopped (activation by an A/D conversion source of group A)			2 PCLKB + 4 ADCLK	—	—	
	A/D conversion when self-diagnosis is enabled	A/D conversion for self-diagnosis is to be started			2 PCLKB + 6 ADCLK	4 PCLKB + 6 ADCLK	6 ADCLK	
	Other than above				2 PCLKB + 4 ADCLK	2 PCLKB + 4 ADCLK	4 ADCLK	
Disconnection detection assistance processing time			t_{DIS}		The setting of ADNDIS[3:0] (initial value = 00h) × ADCLK*3			
Self-diagnosis conversion processing time*1	Sampling time		t_{DIAG}	t_{SPL}	The setting of ADSSTR00 (initial value: 0Dh) × ADCLK*4 + 0.5 ADCLK*4			
	Time for conversion by successive approximation	12-bit conversion accuracy		t_{SAM}	31.5 ADCLK at high-speed mode 40.5 ADCLK at Low-current mode			
		14-bit conversion accuracy			37.5 ADCLK at high-speed mode 46.5 ADCLK at Low-current mode			
	Wait time between self-diagnosis conversion end and analog channel sampling start			t_{DED}	2 ADCLK			
	Wait time between last channel conversion end and self-diagnosis sampling start in continuous scan mode			t_{DSD}	2 ADCLK			
A/D conversion processing time*1	Sampling time		t_{CONV}	t_{SPL}	The setting of ADSSTRn (n = 0 to 13, L, T, O) (initial value = 0Dh) × ADCLK + 0.5 ADCLK			
	Time for conversion by successive approximation	12-bit conversion accuracy		t_{SAM}	31.5 ADCLK at high-speed mode 40.5 ADCLK at Low-current mode			
		14-bit conversion			37.5 ADCLK at high-speed mode 46.5 ADCLK at Low-current mode			
Scan end processing time*1			t_{ED}		1 PCLKB + 3 ADCLK, 2 PCLKB + 3 ADCLK*6			

Note 1. See Figure 33.24 and Figure 33.25 for example of times t_D, t_{DIAG}, t_{CONV}, and t_{ED}.

Note 2. This is the maximum time required from software writing or trigger input to A/D conversion start.

Note 3. The value is fixed to 0Fh (15 ADCLK) when the temperature sensor output or internal reference voltage is A/D-converted.

Note 4. The required sampling time (ns) is specified according to the voltage conditions. The sampling time setting must satisfy the electrical characteristics.

Note 5. This does not include the time consumed in the path from timer output to trigger input.

Note 6. If ADCLK is faster than PCLKB (PCLKB to ADCLK frequency ratio = 1:2 or 1:4).

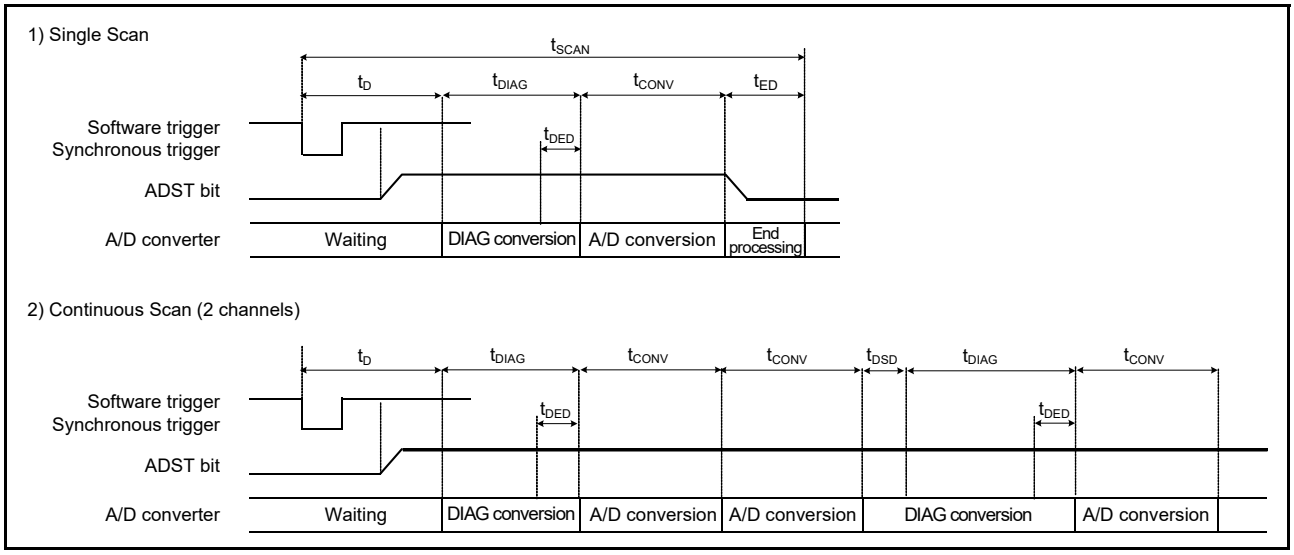


Figure 33.24 Scan conversion timing when activated by software or synchronous trigger input (ELC)

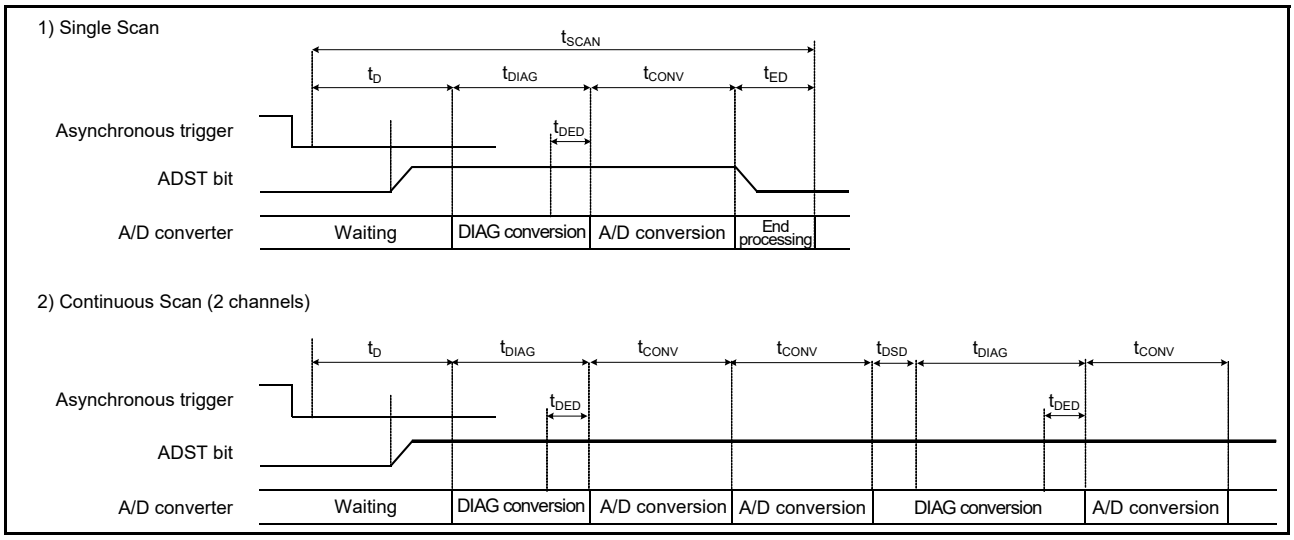


Figure 33.25 Scan conversion timing when activated by asynchronous trigger input (ADTRG0)

33.3.7 Usage Example of A/D Data Register Automatic Clearing Function

Setting the ACE bit in ADCER to 1 automatically clears the A/D data registers (ADDRy, ADRD, ADDBLDR, ADDBLDRA, ADDBLDRB, ADTSDR, ADOCDR) to 0000h when the A/D data registers are read by the CPU or DTC.

This function enables detection of update failures of the A/D data registers (ADDRy, ADRD, ADDBLDR, ADDBLDRA, ADDBLDRB, ADTSDR, ADOCDR). This section describes examples in which the function to automatically clear the ADDRy register is enabled and disabled.

- If the ACE bit in ADCER is 0 (automatic clearing is disabled) and for some reason, if the A/D conversion result (0222h) is not written to the ADDRy register, the ADDRy value retains the old data (0111h). In addition, when this ADDRy value is read into a general-purpose register using an A/D scan end interrupt, the old data (0111h) can be saved in the general-purpose register. When checking whether there is an update failure, it is necessary to frequently save the old data in SRAM or in a general-purpose register.
- If the ACE bit in ADCER is 1 (automatic clearing is enabled), if ADDRy = 0111h is read by the CPU or DTC, ADDRy is automatically cleared to 0000h. Next, if the A/D conversion result of 0222h cannot be transferred to ADDRy for some reason, the cleared data (0000h) remains as the ADDRy value. If this ADDRy value is read into a general-purpose register using an A/D scan end interrupt at this point, 0000h is saved in the general-purpose register. Occurrence of an ADDRy update failure can be determined by checking that the read data value is 0000h.

33.3.8 A/D-Converted Value Addition/Average Mode

A/D-converted value addition/average mode can be used when A/D conversion of the analog input of the selected channels, A/D conversion of the temperature sensor output, or A/D conversion of the internal reference voltage is selected.

In A/D-converted value addition mode, the same channel is A/D-converted 1, 2, 3, 4, or 16*1 consecutive times and the sum of the converted values is stored in the data register. In A/D-converted value average mode, the same channel is A/D-converted 2 or 4 consecutive times and the mean of the converted values is stored in the data register. The use of the average of these results can improve the accuracy of A/D conversion, depending on the types of noise components that are present. This function, however, cannot always guarantee an improvement in A/D conversion accuracy.

Note 1. The addition count can be set to 16 only when 12-bit accuracy is selected.

33.3.9 Disconnection Detection Assist Function

The ADC14 incorporates a function to fix the charge for sampling capacitance to the specified state VREFH0 or VREFL0 before the start of A/D conversion. This function enables disconnection detection in wiring of analog inputs.

If any of the following functions are used, the disconnection detection assist function should be disabled:

- The temperature sensor
- The internal reference voltage
- A/D Self-diagnosis.

Figure 33.26 shows the A/D conversion operation when the disconnection detection assist function is used. Figure 33.27 shows an example of disconnection detection when precharge is selected. Figure 33.28 shows an example of disconnection detection when discharge is selected.

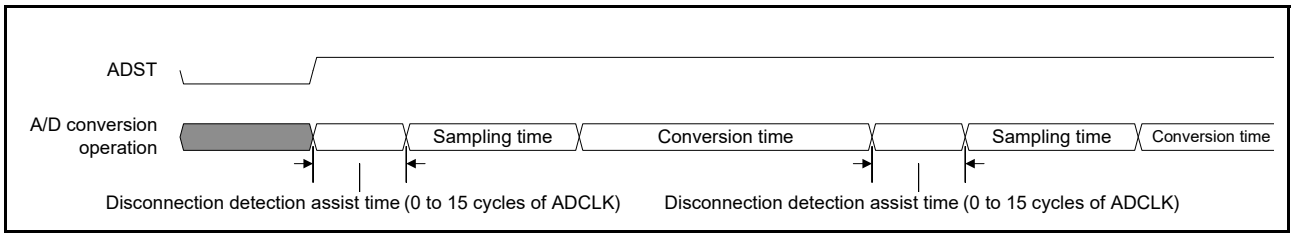
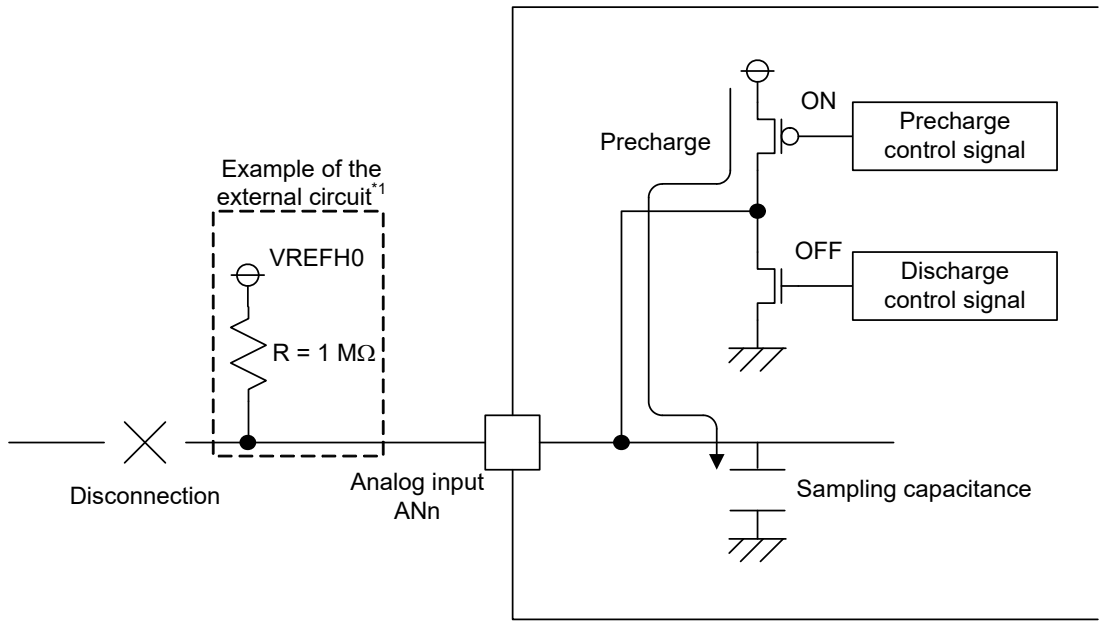
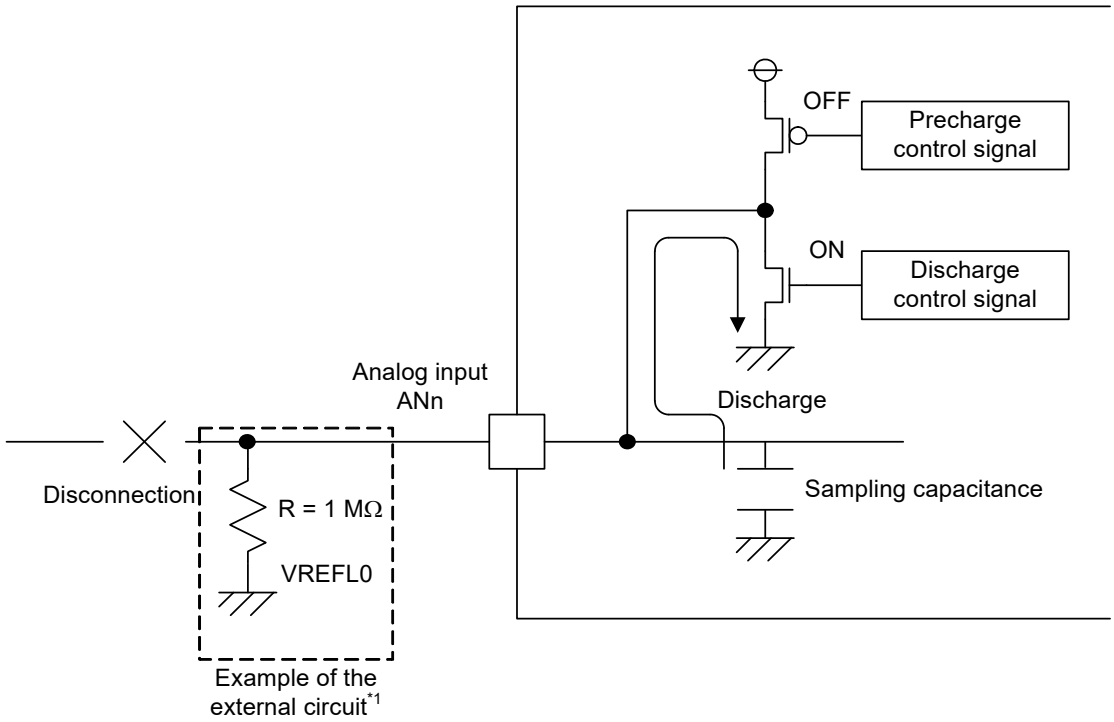


Figure 33.26 Operation of A/D conversion when disconnection detection assist function is used



Note 1. The converted result should be used after it is fully evaluated because the result data when disconnection occurs varies depending on the external circuit.

Figure 33.27 Example of disconnection detection when precharge is selected



Note 1. The converted result should be used after it is fully evaluated because the result data when disconnection occurs varies depending on the external circuit.

Figure 33.28 Example of disconnection detection when discharge is selected

33.3.10 Starting A/D Conversion with Asynchronous Trigger

A/D conversion can be started by the input of an asynchronous trigger. To start A/D conversion by an asynchronous trigger, set the pin function in the PmnPFS register, set the A/D Conversion Start Trigger Select bits (ADSTRGR.TRSA[5:0]) to 000000b, then input a high-level signal to the asynchronous trigger (ADTRG0 pin). Finally, set both the ADCSR.TRGE and ADCSR.EXTRG bits to 1. Figure 33.29 shows timing of the asynchronous trigger input.

An asynchronous trigger cannot be selected by the A/D Conversion Start Trigger Select bits (ADSTRGR.TRSB[5:0]) for group B in group scan mode. For details on setting the pin function, see section 17, I/O Ports.

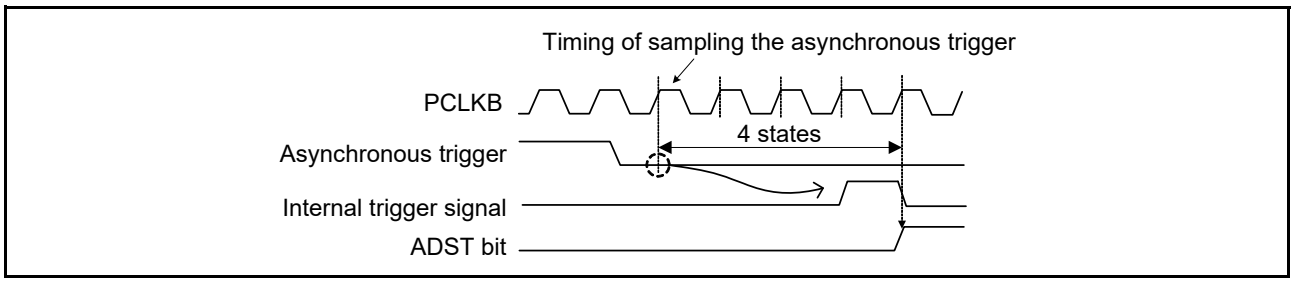


Figure 33.29 Asynchronous trigger input timing

33.3.11 Starting A/D Conversion with Synchronous Trigger from Peripheral Module

A/D conversion can be started by a synchronous trigger (ELC). To do this, set the ADCSR.TRGE bit to 1 and the ADCSR.EXTRG bit to 0, and select the relevant sources in the ADSTRGR.TRSA[5:0] and ADSTRGR.TRSB[5:0] bits.

33.4 Interrupt Sources and DTC Transfer Requests

33.4.1 Interrupt Requests

The ADC14 can send scan end interrupt requests ADC140_ADI and ADC140_GBADI to the CPU. The ADC14 also generates the ADC140_CMPAI/ADC140_CMPBI interrupt for the CPU in response to matches with a condition for comparison.

An ADC140_ADI interrupt is always generated and an ADC140_GBADI interrupt can be generated by setting the ADCSR.GBADIE bit to 1. Similarly, ADC140_CMPAI and ADC140_CMPBI interrupts can be generated by setting the ADCMPCR.CMPAIE and ADCMPCR.CMPBIE bits to 1.

In addition, the DTC can be started when an ADC140_ADI or an ADC140_GBADI interrupt is generated. Using an ADC140_ADI or an ADC140_GBADI interrupt to allow the DTC to read the converted data enables continuous conversion without a burden on software.

Table 33.11 The interrupt source and ELC event of ADC14 (1 of 2)

Operation			Interrupt request or ELC event	Interrupt request	DTC activation	ELC event request	Function
Scan mode	Double trigger mode	Compare Function Window A/B					
Single Scan mode	deselect	deselect	ADC140_ADI	✓	✓	✓	ADC140_ADI is generated at the end of single scan
		select	ADC140_ADI	✓	✓	✓	ADC140_ADI is generated at the end of single scan
			ADC140_CMPAI	✓	×	×	ADC140_CMPAI is generated in the match comparison condition of window A
			ADC140_CMPBI	✓	×	×	ADC140_CMPBI is generated in the match comparison condition of window B
			ADC140_WCMPM	×	✓	✓	ADC140_WCMPM is generated in the match conditions of the window A/B compare function
			ADC140_WCMPUM	×	✓	✓	ADC140_WCMPUM is generated in the mismatch conditions of the window A/B compare function
	select	deselect	ADC140_ADI	✓	✓	✓	ADC140_ADI is generated at the end of scans in even-numbered times

Table 33.11 The interrupt source and ELC event of ADC14 (2 of 2)

Operation			Interrupt request or ELC event	Interrupt request	DTC activation	ELC event request	Function
Scan mode	Double trigger mode	Compare Function Window A/B					
Continuous Scan mode	deselect	deselect	ADC140_ADI	✓	✓	✓	ADC140_ADI is generated at the end of all the selected channels scan
		select	ADC140_CMPAI	✓	×	×	ADC140_CMPAI is generated in the match comparison condition of window A
			ADC140_CMPBI	✓	×	×	ADC140_CMPBI is generated in the match comparison condition of window B
Group Scan Mode	deselect	deselect	ADC140_ADI	✓	✓	✓	ADC140_ADI is generated at the end of group A scan
			ADC140_GBADI	✓	✓	×	ADC140_GBADI dedicated to group B is generated at the end of group B scan
		select	ADC140_ADI	✓	✓	✓	ADC140_ADI is generated at the end of group A scan
			ADC140_GBADI	✓	✓	×	ADC140_GBADI dedicated to group B is generated at the end of group B scan
			ADC140_CMPAI	✓	×	×	ADC140_CMPAI is generated in the match comparison condition of window A
			ADC140_CMPBI	✓	×	×	ADC140_CMPBI is generated in the match comparison condition of window B
	select	deselect	ADC140_ADI	✓	✓	✓	ADC140_ADI is generated at the end of Group A scans in the even-numbered times
			ADC140_GBADI	✓	✓	×	ADC140_GBADI dedicated to group B is generated at the end of Group A scans in even-numbered times

For details on DTC settings, see section 15, Data Transfer Controller (DTC).

33.5 Event Link Function

33.5.1 Event Output to the ELC

The ELC uses the ADC140_ADI interrupt request signal as an event signal, enabling link operation for the preset module. The ADC140_GBADI interrupt and ADC140_CMPAI/ADC140_CMPBI interrupts cannot be used as an event signal. For details, see Table 33.11.

33.5.2 ADC14 Operation through an event from the ELC

The ADC14 can start A/D conversion by the preset event signal (ELC_AD00 and ELC_AD01) specified in the ELSRn setting of the ELC.

ELC_AD00 is the signal that is selected by ELC.ELSR8 register and ELC_AD01 is the signal that is selected by ELC.ELSR9 register.

If an event ELC_AD00/ELC_AD01 occurs during A/D conversion, the event is ignored.

33.6 Selecting Reference Voltage

The ADC14 can select VREFH0 or AVCC0 as the high-potential reference voltage, and can select VREFL0 or AVSS0 as the internal reference voltage and the low-potential reference voltage. Set these reference voltages before starting A/D conversion.

33.7 A/D Conversion Procedure when Selecting Internal Reference Voltage as High-Potential Reference Voltage

The following sequence describes the A/D conversion procedure after selecting the internal reference voltage as the high-potential reference voltage. In this case, A/D conversion is possible for channels AN000 to AN013 and AN016 to AN022, but A/D conversion of the internal reference voltage and the temperature sensor output is prohibited.

1. Set ADHVREFCNT.HVSEL[1:0] to 11b to discharge the high-potential reference voltage path in the ADC14.
2. Wait for a 1 μs discharge period in the software.
3. Set ADHVREFCNT.HVSEL[1:0] to 10b to select internal reference voltage as the high-potential reference voltage.

Note: The ADC14 has a protection function that disables selection of internal reference voltage

(ADHVREFCNT.HVSEL[1:0] = 10b) without discharge (ADHVREFCNT.HVSEL[1:0] = 11b) from the selection of VREFH0 (ADHVREFCNT.HVSEL[1:0] = 01b) or AVCC0 (ADHVREFCNT.HVSEL[1:0] = 00b). If the internal reference voltage is selected without discharge, discharge is forcibly set. Select the internal reference voltage again 1 μs later.

4. Wait until the internal reference voltage is stabilized (for 5 μs) in the software, then perform A/D conversion.

Figure 33.30 shows a waveform for the procedure to select internal reference voltage as the high-potential reference voltage.

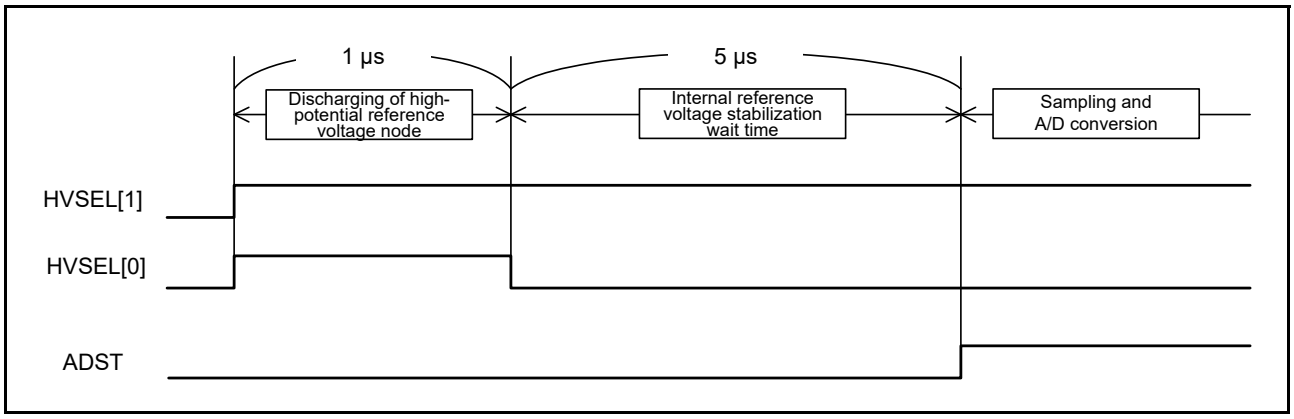


Figure 33.30 Procedure to select internal reference voltage as high-potential reference voltage

33.8 Usage Notes

33.8.1 Notes on Reading Data Registers

The following registers must be read in halfword units:

- A/D Data Registers
- A/D Data Duplexing Registers
- A/D Data Duplexing Register A
- A/D Data Duplexing Register B
- A/D Temperature Sensor Data Register
- A/D Internal Reference Voltage Register
- A/D Self-Diagnosis Data Register.

If a register is read twice in byte units, that is, the upper byte and lower byte are read separately, the A/D-converted value initially read might not match with the subsequent A/D-converted value read. To prevent this, do not read the data registers in byte units.

33.8.2 Notes on Stopping A/D Conversion

To stop A/D conversion when an asynchronous trigger or a synchronous trigger is selected as the condition for starting A/D conversion, follow the procedure in Figure 33.31.

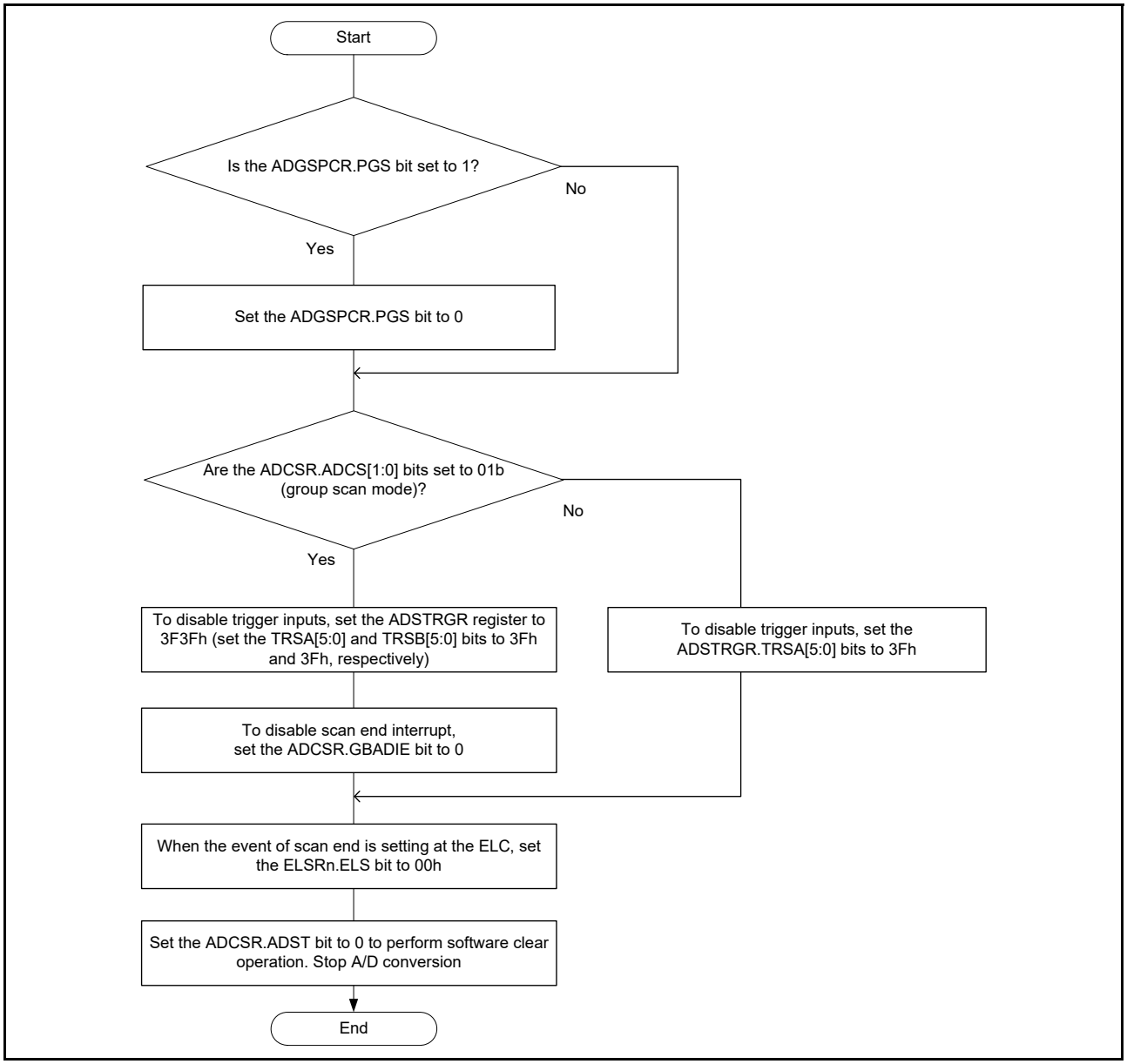


Figure 33.31 Procedure for clearing the ADCSR.ADST bit by software

33.8.3 A/D Conversion Restart Timing and Termination Timing

A maximum of 6 ADCLK cycles is required for the idle analog unit of the ADC14 to restart on setting the ADST bit in ADCSR to 1. A maximum of 3 ADCLK cycles is required for the operating analog unit of the ADC14 to terminate on setting the ADST bit in ADCSR to 0.

33.8.4 Constraints on Scan End Interrupt Handling

When scanning the same analog input twice using any trigger, the first A/D-converted data is overwritten with the second A/D-converted data. This occurs when the CPU does not complete the reading of the A/D-converted data by the time the A/D conversion of the first analog input for the second scan ends after the first scan end interrupt is generated.

33.8.5 Settings for the Module-Stop State

The Module Stop Control Register can enable or disable ADC14 operation. The ADC14 is initially stopped after a reset. The registers are accessible on release from the module-stop state. After release from the module-stop state, wait for at least 1 μs before starting A/D conversion. For details, see section 10, Low Power Modes.

33.8.6 Constraints on Entering the Low Power States

Before entering the module-stop state or Software Standby mode, be sure to stop A/D conversion. Set the ADST bit in ADCSR to 0 and secure a period of time until the analog unit of the ADC14 stops. Follow the procedure shown in Figure 33.31 to clear the ADCSR.ADST bit with software. Then wait for 3 ADCLK clock cycles before entering the module-stop state or Software Standby mode.

33.8.7 Error in Absolute Accuracy When Disconnection Detection Assistance is in Use

Using disconnection detection assistance leads to an error in absolute accuracy of the A/D converter. This error arises because an erroneous voltage is input to the analog input pins due to the resistive voltage division between the pull-up or pull-down resistor (Rp) and the resistance of the signal source (Rs). This error in absolute accuracy is calculated from the following formula:

Maximum error in absolute accuracy (LSB) = 4095 × Rs / (Rs + Rp)

Only use disconnection detection assistance after thorough evaluation.

33.8.8 ADHSC Bit Rewriting Procedure

Before changing the A/D Conversion Select bit (ADCSR.ADHSC) from 0 to 1 or from 1 to 0, the ADC14 must be in the standby state. Use the following procedure to modify the ADCSR.ADHSC bit. After the Sleep bit (ADHVREFCNT.ADSLP) is set to 0, wait for at least 1 μs then start the A/D conversion.

1. Set the Sleep bit (ADHVREFCNT.ADSLP) to 1.
2. Wait for at least 0.2 μs, then modify the A/D Conversion Select bit (ADCSR.ADHSC).
3. Wait for at least 4.8 μs, then set the Sleep bit (ADHVREFCNT.ADSLP) to 0.

Note 1. Do not set the Sleep bit (ADHVREFCNT.ADSLP) to 1 except when modifying the A/D Conversion Select bit (ADCSR.ADHSC).

Note 2. Do not reset the Sleep bit while the A/D Conversion Select bit (ADCSR.ADHSC) is 1. After this bit is set to 0 or the operating mode transitions to the module-stop mode, reset the Sleep bit using the ADCSR.ADHSC bit rewriting procedure.

33.8.9 Operating Modes and Status Bits

Initialize or set again individually, if necessary, the voltage values in self-diagnosis, the value of the first scan or second scan in double trigger mode, the data buffer pointer, and status monitor in the compare function.

- Select the voltage values in self-diagnosis ADCER.DIAGVAL[1:0] after setting ADCER.DIAGLD to 1
- The double trigger mode operates as the first scan after setting ADCSR.DBLE from 0 to 1
- The status monitor bits (MONCMPA, MONCMPB, MONCOMB) in the compare function are initialized after setting ADCMPCR.CMPAE and ADCMPCR.CMPBE to 0.

33.8.10 Notes on Board Design

The board should be designed so that digital circuits and analog circuits are separated from each other as far as possible.

In addition, digital circuit signal lines and analog circuit signal lines should not intersect or placed near each other. If these rules are not followed, noise can occur on analog signals and A/D conversion accuracy is affected. The analog input pins (AN000 to AN013, AN016 to AN022), reference power supply pin (VREFH0), reference ground pin (VREFL0), and analog power supply (AVCC0) should be separated from digital circuits using the analog ground (AVSS0). The analog ground (AVSS0) should be connected to a stable digital ground (VSS) on the board (single-point ground plane connection).

33.8.11 Noise Reduction

To prevent the analog input pins (AN000 to AN013, AN016 to AN022) from being destroyed by abnormal voltage such as excessive surge, insert a capacitor between AVCC0 and AVSS0 and between VREFH0 and VREFL0. Additionally, connect a protection circuit to protect the analog input pins (AN000 to AN013, AN016 to AN022) as shown Figure 33.32.

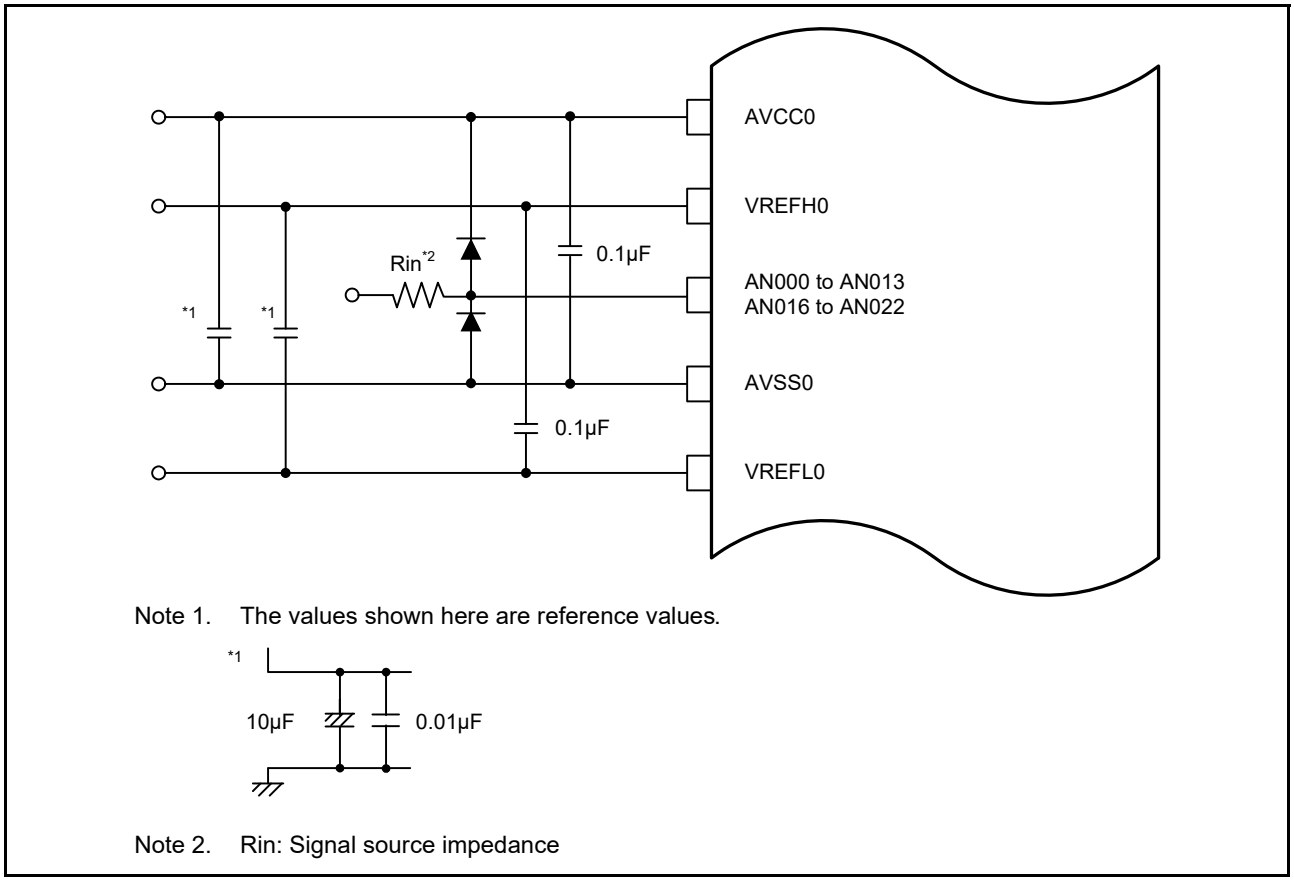


Figure 33.32 Example protection circuit for analog inputs

33.8.12 Port Setting when Using the ADC14 Input

When using the high-precision channels, do not use PORT0 and PORT5 as general I/O, IRQ2 inputs, and TS transmission. Renesas recommends that you do not use the digital output that is also used as the A/D analog input, if normal-precision channel is used. If the digital output that is also used as the A/D analog input is used for output signals, perform A/D conversion several times, eliminate the maximum and minimum values, and obtain the average of the other results.

33.8.13 Relationship between the A/D converter, OPAMP, ACMPHS, and ACMPLP

Table 33.12 lists the A/D conversion targets that should not be selected as OPAMP, ACMPHS, and ACMPLP inputs during A/D conversion.

Table 33.12 OPAMP, ACMPHS, and ACMPLP pins that should not be selected during A/D conversion (1 of 2)

Target of A/D conversion	OPAMP	ACMPHS	ACMPLP
AN000	AMP0+	IVCMP2	—
AN001	AMP0-	IVREF2	—
AN007	AMP1-	IVREF0	—
AN008	AMP1+	IVCMP0	—
AN009	AMP2-	IVREF1	—
AN010	AMP2+	IVCMP1	—
AN011	AMP3-	—	—
AN012	AMP3+	—	—
AN019	—	—	CMPREF1
AN020	—	—	CMPIN1

Table 33.12 OPAMP, ACMPHS, and ACMPLP pins that should not be selected during A/D conversion (2 of 2)

Target of A/D conversion	OPAMP	ACMPHS	ACMPLP
AN021	—	—	CMPREF0
AN022	—	—	CMPIN0

33.8.14 Notes on Canceling Software Standby Mode

After transitioning from Software Standby mode to Normal mode, wait 1 μs before starting A/D conversion.

34. 8-Bit D/A Converter (DAC8)

34.1 Overview

The MCU provides an 8-bit D/A Converter (DAC8).

Table 34.1 lists the DAC8 specifications and Figure 34.1 shows a block diagram.

Table 34.1 DAC8 specifications

Parameter	Specifications
Resolution	8 bits
Output channels	3 channels
Interference reduction between analog modules	Not supported
Module-stop function	The module-stop state can be set to reduce power consumption
Event link function (input)	D/A conversion can be started on input of an event signal

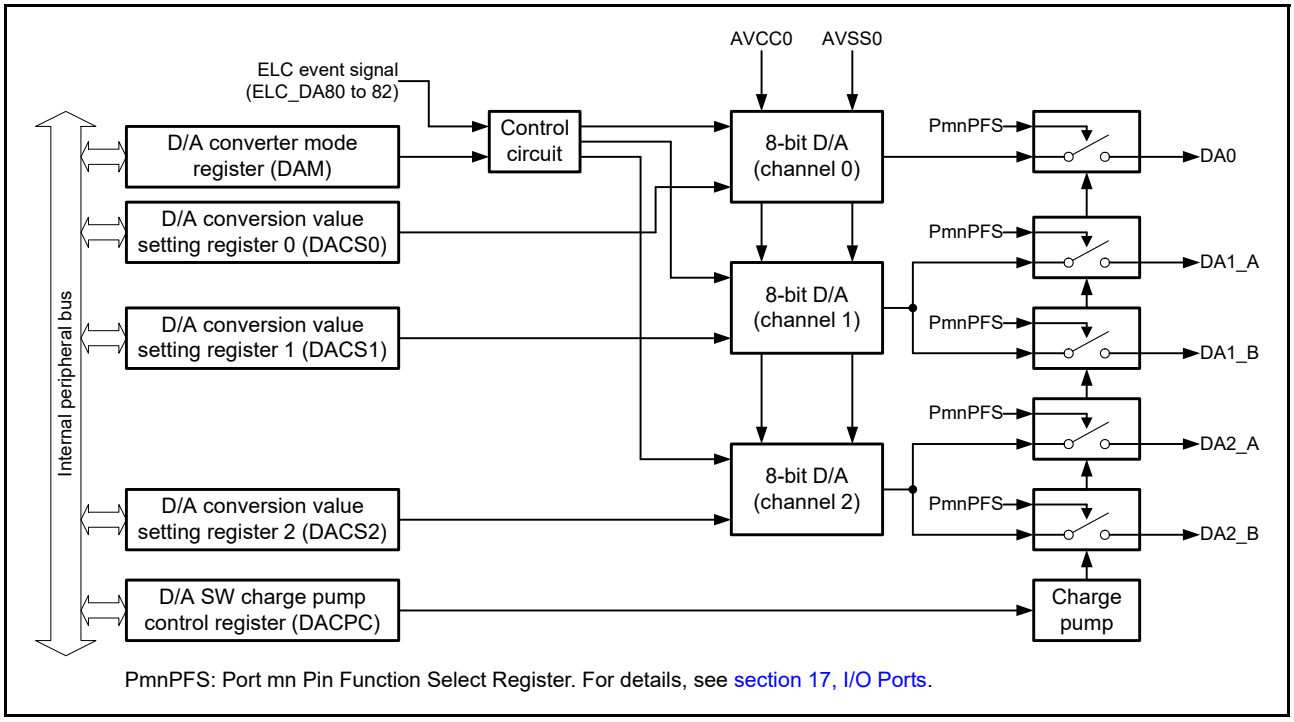


Figure 34.1 DAC8 block diagram

Table 34.2 lists the pin configuration of the DAC8.

Table 34.2 DAC8 pin configurations

Pin name	I/O	Function
AVCC0	Input	• Analog power and analog reference top voltage supply pin for ADC14, DAC8, operational amplifier, and high-speed analog comparator • Connect to VCC when these modules are not used.
AVSS0	Input	• Analog ground and analog reference ground supply pin for ADC14, DAC8, operational amplifier, and high-speed analog comparator • Connect to VSS when these modules are not used.
DA0	Output	Channel 0 analog output pin
DA1	Output	Channel 1 analog output pin
DA2	Output	Channel 2 analog output pin

34.2 Register Descriptions

34.2.1 D/A Conversion Value Setting Register n (DACSn) (n = 0 to 2)

Address(es): DAC8.DACS0 4009 E000h, DAC8.DACS1 4009 E001h, DAC8.DACS2 4009 E002h

	b7	b6	b5	b4	b3	b2	b1	b0
	DACS[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

The DACSn register is an 8-bit read/write register to store data for D/A conversion. When D/A conversion is enabled, the value in the DACSn register is converted and output to an analog output pin.

34.2.2 D/A Converter Mode Register (DAM)

Address(es): DAC8.DAM 4009 E003h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	DACE2	DACE1	DACE0	—	DAMD2	DAMD1	DAMD0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DAMD0	D/A Operation Mode Select 0	0: Channel 0 for normal operation mode 1: Channel 0 for real-time output mode (event link).	R/W
b1	DAMD1	D/A Operation Mode Select 1	0: Channel 1 for normal operation mode 1: Channel 1 for real-time output mode (event link).	R/W
b2	DAMD2	D/A Operation Mode Select 2	0: Channel 2 for normal operation mode 1: Channel 2 for real-time output mode (event link).	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	DACE0	D/A Operation Enable 0	0: D/A conversion disabled for channel 0 1: D/A conversion enabled for channel 0.	R/W
b5	DACE1	D/A Operation Enable 1	0: D/A conversion disabled for channel 1 1: D/A conversion enabled for channel 1.	R/W
b6	DACE2	D/A Operation Enable 2	0: D/A conversion disabled for channel 2 1: D/A conversion enabled for channel 2.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

DAMDn bit (D/A Operation Mode Select n) (n = 0 to 2)

The DAMDn bit selects operation mode of D/A conversion.

DACEn bit (D/A Operation Enable n) (n = 0 to 2)

The DACEn bit enables or disables D/A conversion.

34.2.3 D/A SW Charge Pump Control Register (DACPC)

Address(es): DAC8.DACPC 4009 E007h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	PUMPEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PUMPEN	Charge Pump Enable	0: Charge pump disabled 1: Charge pump enabled.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

PUMPEN bit (Charge Pump Enable)

The PUMPEN bit enables or disables charge pump. When the DAC8 output level is output to a pin, set the MOCOCR.MCSTP bit to 0 and then set the DACPC.PUMPEN bit to 1. When using DAC8 output as ACMPHS/ACMPLP input, set the DACPC.PUMPEN bit to 0. Setting the MOCOCR.MCSTP bit is optional.

Note: Set the DACPC register while no D/A output is selected by the Peripheral Select bit (PSEL[4:0] bits) in the Port mn Pin Function Select register. For details on the PSEL[4:0] bits, see section 17, I/O Ports.

34.3 Operation

34.3.1 Normal Mode

D/A conversion is performed using write operation to the DACSn (n = 0, 1, 2) register as a trigger.

The following procedure describes an operation example when performing D/A conversion for channel 0.

1. Set the MOCOCR.MCSTP bit to 0 (MOCO operating).
2. Set the DACPC.PUMPEN bit to 1 (charge pump enabled). If you want to operate in subosc-speed mode, the following steps are required:
   a. Set the MOCOCR.MCSTP bit to 1.
   b. Change the power control mode to Subosc-speed mode.
3. Wait for the charge pump stabilization time*4.
4. Select the D/A output terminal (controlled by the PmnPFS.PMR and PmnPFS.PSEL bit settings).
5. Set the DAM.DAMD0 bit to 0 (normal mode).
6. Set the data for D/A conversion to the DACS0 register.
7. When the DAM.DACE0 bit is set to 1 (D/A conversion enabled), D/A conversion is started. After the settling time elapses, the conversion result is output to analog output pin DA0. The conversion result is continuously being output until the DACS0 is rewritten or the DAM.DACE0 bit is set to 0 (D/A conversion disabled).
   The output value (reference) is calculated with the following formula:

$$\frac{\text{DACS0 register}}{256} \times \text{Reference voltage}$$

8. To perform subsequent D/A conversion, write the value for next D/A conversion to the DACS0 register.
9. When the DAM.DACE0 bit is set to 0 (D/A conversion disabled), D/A conversion is stopped.

Note 1. If the DAM.DACE0 bit is set to 1, 0, and then 1 in order, after the last 1 is set and the settling time elapses, an analog voltage is output to the DA0 pin.

Note 2. If the DACS0 register is rewritten during the settling time, the current D/A conversion is canceled and conversion is started again with the rewritten value.

Note 3. Steps 1. to 4. are for when the DAC8 output level is output to a pin. The procedure must not be performed when using DAC8 output as ACMPHS/ACMPLP input. The MOCOCR.MCSTP bit setting is optional.
Note 4. See section 46, Electrical Characteristics for details on the charge pump stabilization time.

34.3.2 Real-Time Output Mode (Event Link)

D/A conversion is performed on each channel using an event signal from the ELC as a trigger.

The following procedure describes an operation example when performing D/A conversion for channel 0:

1. Set the MOCOCR.MCSTP bit to 0 (MOCO operating).
2. Set the DACPC.PUMPEN bit to 1 (charge pump enabled). If you want to operate in subosc-speed mode, the following steps are required:
   a. Set the MOCOCR.MCSTP bit to 1.
   b. Change the power control mode to Subosc-speed mode.
3. Wait for the charge pump stabilization time*4.
4. Select D/A output terminal (controlled by PmnPFS.PMR and PmnPFS.PSEL bit settings).
5. Set the DAM.DAMD0 bit to 0 (normal mode).
6. Set the data for D/A conversion to the DACS0 register.
7. When the DAM.DACE0 bit is set to 1 (D/A conversion enabled), D/A conversion starts. After the settling time elapses, the conversion result is output to analog output pin DA0.
8. Specify the trigger signal for real-time output mode with the ELSR19 register of the ELC.
9. Set the DAM.DAMD0 bit to 1 (real-time output mode).
10. Start the event source operation.

Note: Steps 1. to 10. are performed as the initial settings.

11. On generation of the trigger signal for real-time output mode, D/A conversion starts, and after the settling time elapses, an analog voltage is output to the DA0 pin. The data for D/A conversion must be set to the DACS0 register before the next D/A conversion starts (before generation of the trigger signal for real-time output mode). When the DAM.DACE0 bit is set to 0 (D/A conversion disabled), D/A conversion stops.

Note 1. If the DAM.DACE0 bit is set to 1, 0, and then 1 in order, after the last 1 is set and the settling time elapses, an analog voltage is output to the DA0 pin.
Note 2. When setting the trigger signal generation interval for the real-time output mode on the same channel, set the interval to the value longer than the settling time. If the trigger signal is generated during the settling time, current D/A conversion is canceled, and then D/A conversion is restarted.
Note 3. Steps 1. to 4. are for when the DAC8 output level is output to a pin. The procedure must not be performed when using DAC8 output as ACMPHS/ACMPLP input. The MOCOCR.MCSTP bit setting is optional.
Note 4. See section 46, Electrical Characteristics for details on the charge pump stabilization time.

34.3.3 MOCO Stop Procedure after D/A Conversion Disabled

The following procedure describes how to stop MOCO after D/A conversion disabled (DAM.DACE0 =0):

1. Set the D/A output terminal to the port function or to another function. If operating in subosc-speed mode, the following steps are required:
   a. Change the power control Subosc-speed mode to another mode.
   b. Set the MOCOCR.MCSTP bit to 0.
2. Set the DACPC.PUMPEN bit to 0 (charge pump disabled).
3. Set the MOCOCR.MCSTP bit to 1 (MOCO stopped).

34.3.4 Output Start Timing of the D/A Conversion Value

Figure 34.2 shows the output start timing of the D/A conversion value.

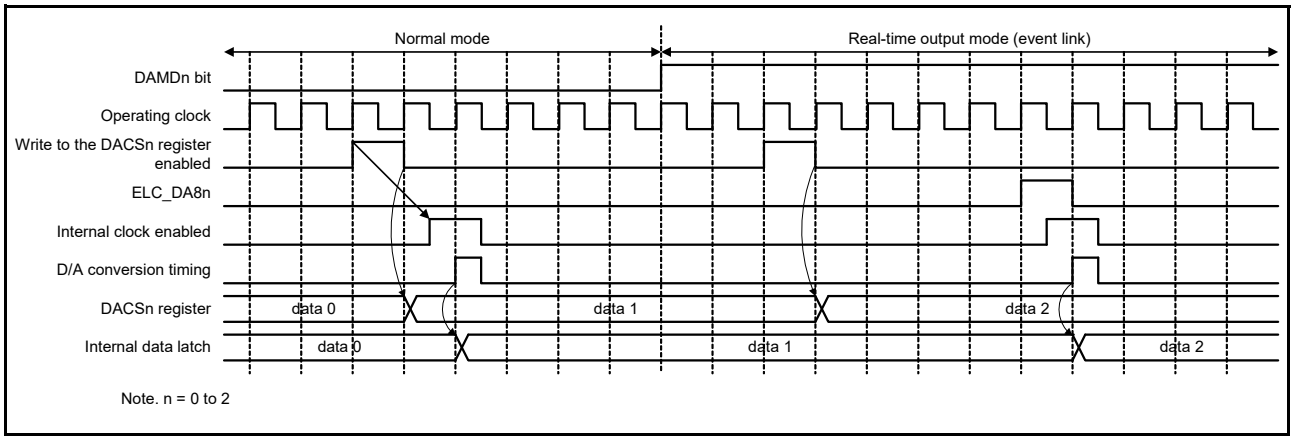


Figure 34.2 Output start timing of the D/A conversion value

Output start timing in normal mode:

- After the DACSn register is written, the internal data latch is set after 1 operating clock cycle. After the settling time elapses, an analog voltage is output to the DAn pin.

Output start timing in Real-time output mode:

- After an event signal (ELC_DA8n) is received from the ELC, the internal data latch is set after 1 operating clock cycle. After the settling time elapses, an analog voltage is output to the DAn pin.

34.4 Usage Notes

34.4.1 Module-Stop State

The Module Stop Control Register can enable or disable DAC8 operation. The DAC8 is stopped after a reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

34.4.2 DAC8 Operation in Module-Stop State

When the MCU enters the module-stop state with D/A conversion enabled, D/A outputs are retained. The analog power supply current is the same as the one during D/A conversion. If the analog power supply current must be reduced in the module-stop state, disable D/A conversion by setting the DAM.DACEn bits to 0 and the DACPC.PUMPEN bit to 0.

34.4.3 DAC8 Operation in Software Standby Mode

When the MCU enters Software Standby mode with D/A conversion enabled, D/A outputs are retained. The analog power supply current is the same as the one during D/A conversion. If the analog power supply current must be reduced in Software Standby mode, disable D/A conversion by setting the DAM.DACEn bits to 0 and the DACPC.PUMPEN bit to 0.

34.4.4 Real-Time Output of the D/A Converter

In real-time output mode:

- Set the value to the DACSn register before the trigger signal for real-time output mode is generated. Do not change the setting value in the DACSn register while the trigger signal is being output.

When the MCU enters Software Standby mode in real-time output mode:

- Disable the ELC_DA8n before entering Software Standby mode. For details, see section 16, Event Link Controller (ELC).

34.4.5 D/A Converter Output

Currents on pins DA0, DA1, and DA2 cannot be obtained because the output impedance of the D/A converter is high. If the load input impedance is low, insert a follower amplifier between the load and pins DA0, DA1, and DA2. Also make the wiring to the follower amplifier and the load as short as possible because the output impedance is high. If the wiring becomes long, consider shielding the wiring with the ground pattern.

34.4.6 When Not Using the D/A Converter

When not using the D/A converter, set the DAM.DACEn bit to 0 (output disabled), the DACSn register to 00h, and the DACPC.PUMPEN bit to 0, so that current does not flow and the current consumption can be reduced.

35. Temperature Sensor (TSN)

35.1 Overview

The on-chip temperature sensor can determine and monitor the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is linear.

The output voltage is provided to the ADC14 for conversion and can also be used by the end application.

Table 35.1 lists the temperature sensor specifications and Figure 35.1 shows a block diagram.

Table 35.1 Temperature sensor specifications

Parameter	Description
Temperature sensor voltage output	Temperature sensor outputs a voltage to the 14-bit A/D converter

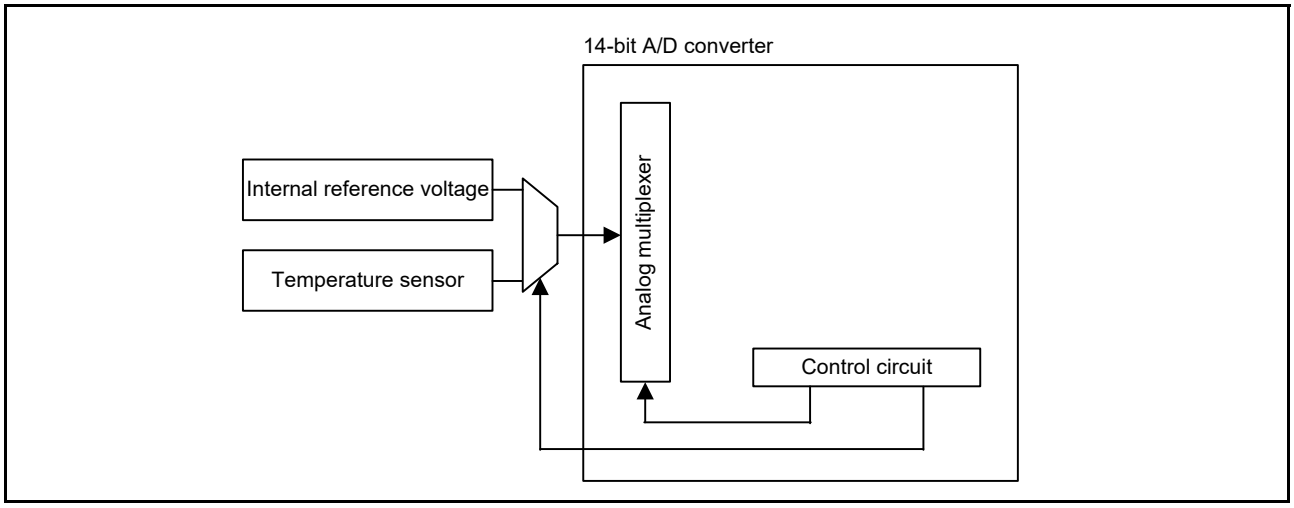


Figure 35.1 Temperature sensor block diagram

35.2 Register Descriptions

35.2.1 Temperature Sensor Calibration Data Register H (TSCDRH)

Address(es): TSN.TSCDRH 407E C229h

	b7	b6	b5	b4	b3	b2	b1	b0
	TSCDRH[7:0]							
Value after reset:	Unique value for each chip							

Bit	Symbol	Bit name	Description	R/W
b7 to b0	TSCDRH[7:0]	Temperature Sensor Calibration Data	The calibration data stores the upper 4 bits of the converted value	R

35.2.2 Temperature Sensor Calibration Data Register L (TSCDRL)

Address(es): TSN.TSCDRL 407E C228h

	b7	b6	b5	b4	b3	b2	b1	b0
	TSCDRL[7:0]							
Value after reset:	Unique value for each chip							

Bit	Symbol	Bit name	Description	R/W
b7 to b0	TSCDRL[7:0]	Temperature Sensor Calibration Data	The calibration data stores the lower 8 bits of the converted value	R

At factory shipment, the TSCDRH and TSCDRL registers store temperature sensor calibration data measured for each MCU. Temperature sensor calibration data is a digital value obtained using the 14-bit A/D converter to convert the voltage output by the temperature sensor under the condition Ta = Tj = 125°C and AVCC0 = 3.3 V. The TSCDRH register stores the upper 4 bits of the converted value, and the TSCDRL register stores the lower 8 bits.

35.3 Using the Temperature Sensor

The temperature sensor outputs a voltage that varies with the temperature. This voltage is converted to a digital value by the ADC14. To obtain the die temperature, convert this value into the temperature.

35.3.1 Preparation for Using the Temperature Sensor

The temperature (T) is proportional to the sensor voltage output (Vs), so temperature is calculated with the following formula:

T = (Vs - V1) / Slope + T1

T: Measured temperature (°C)

Vs: Voltage output by the temperature sensor on temperature measurement (V)

T1: Temperature experimentally measured at one point (°C)

V1: Voltage output by the temperature sensor on measurement of T1 (V)

T2: Temperature experimentally measured at a second point (°C)

V2: Voltage output by the temperature sensor on measurement of T2 (V)

Slope: Temperature gradient of the temperature sensor (V/°C), Slope = (V2 - V1) / (T2 - T1).

Characteristics vary between sensors, so Renesas recommends measuring two different sample temperatures as follows:

1. Use the ADC14 to measure the voltage V1 output by the temperature sensor at temperature T1.
2. Use the ADC14 to measure the voltage V2 output by the temperature sensor at a different temperature T2.
3. Obtain the temperature gradient (Slope = (V2 - V1) / (T2 - T1)) from these results.
4. Subsequently, obtain temperatures by substituting the slope into the formula for the temperature characteristic (T = (Vs -V1) / Slope + T1).

If you are using the temperature gradient given in Table 46.52 of section 46, Electrical Characteristics, use the ADC14 to measure the voltage V1 output by the temperature sensor at temperature T1, then calculate the temperature characteristic using the following formula:

T = (Vs - V1) / Slope + T1

Note: This method produces less accurate temperatures than measurement at two points.

In the MCU, the TSCDRH and TSCDRL registers store the temperature value (CAL125) of the temperature sensor measured under the condition Ta = Tj = 125°C and AVCC0 = 3.3 V. If you use this value as the sample measurement result at the first point, you can omit the preparation before using the temperature sensor.

This measured value CAL125 can be calculated as follows:

CAL125 = TSCDRH register value << 8) + TSCDRL register value

V1 is calculated from CAL125 as follows:

V1 = 3.3 × CAL125 / 4096 [V]

Using this value, the measured temperature can be calculated according to the following formula:

T = (Vs - V1) / Slope + 125 [°C]

T: Measured temperature (°C)

Vs: Voltage output by the temperature sensor when the temperature is measured (V)

V1: Voltage output by the temperature sensor when Ta = Tj = 125°C and AVCC0 = 3.3 V (V)

Slope: Temperature gradient of the temperature sensor ÷ 1,000 (V / °C).

Figure 35.2 shows the error in the measured temperature. The variation range is 3σ.

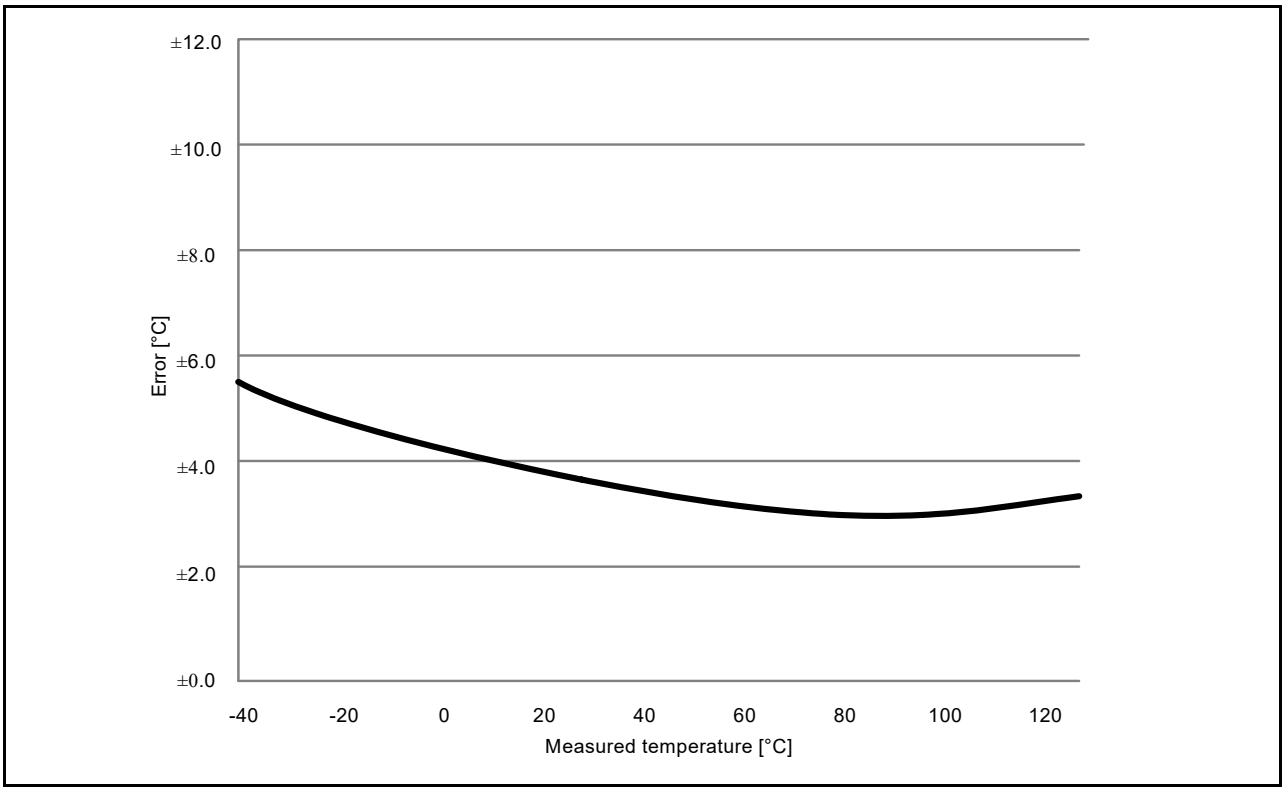


Figure 35.2 Error in the measured temperature (designed values)

35.3.2 Procedures for Using the Temperature Sensor

For details, see section 33, 14-Bit A/D Converter (ADC14).

36. Operational Amplifier (OPAMP)

36.1 Overview

Operational amplifiers can be used to amplify small analog input voltages and output the amplified voltages. The MCU has a total of four differential operational amplifier units with two input pins and one output pin.

The operational amplifiers have the following functions:

- Operational amplifiers 1 and 2 of the four units can be used to input signals to the Low-Power Analog Comparator (ACMPLP)
- The output signals from all units can be used for the input signals to the A/D converter
- High-speed mode (high-current consumption) and low-power mode (slow-speed response) are supported and either mode can be selected based on trade-offs between the response speed and current consumption
- Operation can be started by a trigger from the Low Power Asynchronous General purpose Timer (AGT)
- Operation can be stopped by an A/D conversion end trigger.

The number of operational amplifier input and output pins differs depending on the product.

Figure 36.1 shows a block diagram of operational amplifier and Table 36.1 lists the unit configuration.

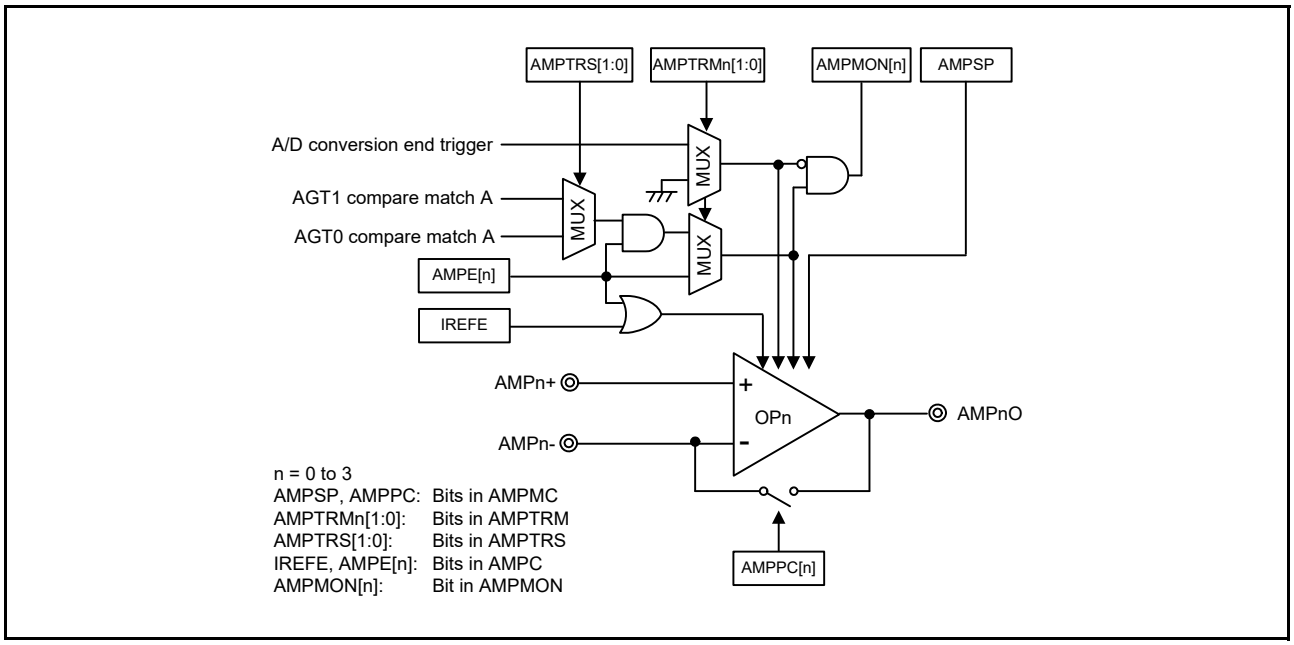


Figure 36.1 Operational amplifier block diagram

Table 36.1 OPAMP unit configuration

Unit	I/O pin	I/O	Function
Unit 0 (Operational amplifier 0)	AMP0+, AMP0-	Input	Input pin of operational amplifier 0 (+, -)
	AMP0O	Output	Output pin of operational amplifier 0
Unit 1 (Operational amplifier 1)	AMP1+, AMP1-	Input	Input pin of operational amplifier 1 (+, -)
	AMP1O	Output	Output pin of operational amplifier 1
Unit 2 (Operational amplifier 2)	AMP2+, AMP2-	Input	Input pin of operational amplifier 2 (+, -)
	AMP2O	Output	Output pin of operational amplifier 2
Unit 3 (Operational amplifier 3)	AMP3+, AMP3-	Input	Input pin of operational amplifier 3 (+, -)
	AMP3O	Output	Output pin of operational amplifier 3

36.2 Register Descriptions

36.2.1 Operational Amplifier Mode Control Register (AMPMC)

Address(es): OPAMP.AMPMC 4008 6008h

	b7	b6	b5	b4	b3	b2	b1	b0
	AMPSP	—	—	—	AMPPC[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	AMPPC[3:0]	Operational Amplifier Precharge Control	AMPPC[n] (n = 0 to 3) 0: Precharging of operational amplifier n is stopped 1: Precharging of operational amplifier n is enabled.	R/W
b6 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	AMPSP	OPAMP Operation Mode Selection	0: Low-power mode (low speed) 1: High-speed mode.	R/W

Note: Set the AMPSP bit while the value of the AMPC register is 00h (operational amplifier and reference current generator are stopped). Set bits that are not used in this register to the initial value.

36.2.2 Operational Amplifier Trigger Mode Control Register (AMPTRM)

Address(es): OPAMP.AMPTRM 4008 6009h

	b7	b6	b5	b4	b3	b2	b1	b0
	AMPTRM3[1:0]		AMPTRM2[1:0]		AMPTRM1[1:0]		AMPTRM0[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	AMPTRM0[1:0]	OPAMP Function Activation/ Stop Trigger Control n*2	AMPTRMn[1] AMPTRMn[0] (n = 0 to 3) 0 0: Software trigger mode: •The operational amplifier can be activated or stopped by setting the AMPC register •The operational amplifier cannot be activated by an activation trigger •The operational amplifier cannot be controlled by an A/D conversion end trigger. 0 1: Activation trigger mode: •The operational amplifier can be set to wait for an activation trigger or stopped by setting the AMPC register •The operational amplifier can be activated by an activation trigger *1 •The operational amplifier cannot be controlled by an A/D conversion end trigger. 1 0: Setting prohibited 1 1: Activation and A/D trigger mode: •The operational amplifier can be set to wait for an activation trigger or stopped by setting the AMPC register •The operational amplifier can be activated by an activation trigger*1 •The operational amplifier can be stopped by an A/D conversion end trigger. An A/D conversion end trigger is always generated at the end of A/D conversion.	R/W
b3, b2	AMPTRM1[1:0]			
b5, b4	AMPTRM2[1:0]			
b7, b6	AMPTRM3[1:0]			

Note: An A/D conversion end trigger is always generated at the end of A/D conversion.

Note 1. When using an activation trigger to activate the operational amplifier, first specify settings related to the AGT, set the AMPTRS register, then use the AMPC register to set the operation control bit of the operational amplifier to be activated to 1 (operational amplifier wait state is enabled).

Note 2. When changing the set values of AMPTRMn[1:0], make sure that the AMPE[n] bit in the AMPC register is 0 (operation amplifier is stopped).

36.2.3 Operational Amplifier Activation Trigger Select Register (AMPTRS)

Address(es): OPAMP.AMPTRS 4008 600Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	AMPTRS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	AMPTRS[1:0]	Activation Trigger Selection*1	b1 b0 0 0: Operational amplifier n: Operational amplifier activation trigger n (n = 0 to 3) 0 1: Operational amplifier m: Operational amplifier activation trigger 0 (m = 0, 1) Operational amplifier n: Operational amplifier activation trigger 1 (n = 2, 3) 1 0: Setting prohibited 1 1: Operational amplifier n: Operational amplifier activation trigger 0 (n = 0 to 3).	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set bits that are not used in this register to the initial value.
Note 1. Do not change the value of the AMPTRS register after setting the AMPTRM register.

Table 36.2 shows operational amplifier activation triggers associated with events.

Table 36.2 Operational amplifier activation triggers associated with events

Trigger	Event
Operational Amplifier activation trigger 0	AGT1 compare match A
Operational Amplifier activation trigger 1	AGT0 compare match A
Operational Amplifier activation trigger 2	AGT1 compare match A
Operational Amplifier activation trigger 3	AGT0 compare match A

36.2.4 Operational Amplifier Control Register (AMPC)

Address(es): OPAMP.AMPC 4008 600Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	IREFE	—	—	—	AMPE[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	AMPE[3:0]	OPAMP Operation Control	0: Operational amplifier n is stopped 1: Operation of operational amplifier n is enabled*1. Activation trigger mode or activation and A/D trigger mode: Wait for AGT is enabled (n = 0 to 3).	R/W
b6 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	IREFE	OPAMP Reference Current Circuit Operation Control	0: Operational amplifier reference current circuit is stopped 1: Operation of operational amplifier reference current circuit is enabled.	R/W

Note: Set bits that are not used in this register to the initial value.
Note 1. Operation of the operational amplifier reference current circuit is also enabled regardless of the IREFE bit setting.

Set the bits to 0 for a unit that is not used.

36.2.5 Operational Amplifier Monitor Register (AMPMON)

Address(es): OPAMP.AMPMON 4008 600Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	AMPMON[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	AMPMON[3:0]	Operational Amplifier n Status (n = 0 to 3)	0: Operational amplifier n is stopped 1: Operational amplifier n is operating.	R
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R

Note: This register is used to asynchronously reflect whether each operational amplifier is operating or stopped. To determine the operational amplifier state, read this register continuously and confirm that the bit state has changed. After that, read this register again to confirm whether the operational amplifier state has changed. When an activation trigger or A/D conversion end trigger synchronized with the clock or a software trigger in the other interrupt routine is used to control the operational amplifier, the timing to operate or stop the operational amplifier can be estimated, such as for checking normal operation. In this case, read this register after 1 CPU/peripheral clock cycle when the associated trigger or interrupt affecting the operational amplifier state occurred. Set bits that are not used in this register to the initial value.

36.3 Operation

36.3.1 State Transitions

Figure 36.2 shows state transitions when the operational amplifier and reference current circuit are activated or stopped using the operational amplifier control circuit.

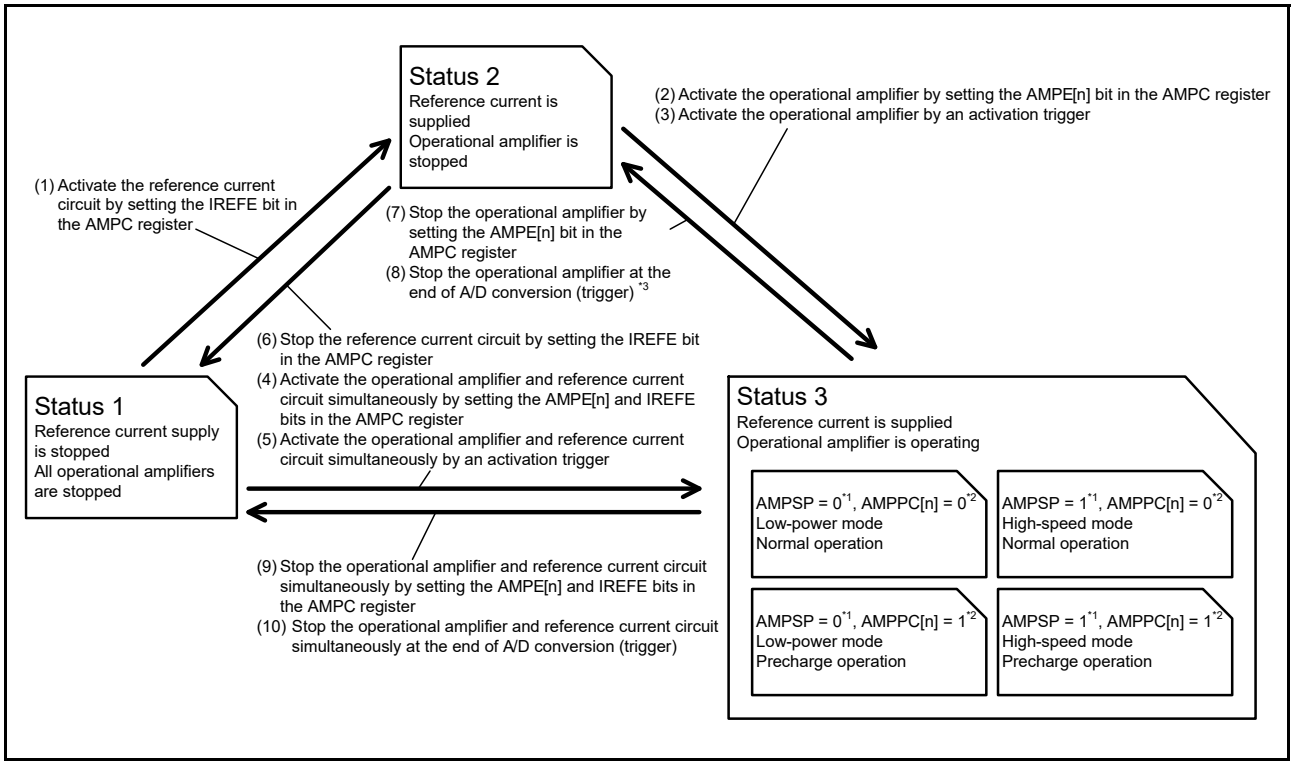


Figure 36.2 Operational amplifier state transitions

Note 1. Set the AMPSP bit in the AMPMC register and the AMPTRS and AMPTRM registers in status 1.
Note 2. Set the AMPPC[n] bit in the AMPMC register in status 3.
Note 3. To only stop the operational amplifier at the end of A/D conversion, preset operation of the reference current circuit to enabled (operate the operational amplifier by status 2).

A stabilization wait time is required after supply of the reference current and operation of the operational amplifier are set before each operation actually starts. For details on the stabilization wait time, see section 46, Electrical Characteristics.

The operational amplifier cannot be activated or stopped continuously in steps (2) → (8), (2) → (10), (3) → (10), and (4) → (10).

An activation trigger and end of A/D conversion are used to activate or stop only the operational amplifier that is preset for use by setting the AMPTRM register.

36.3.2 Operational Amplifier Control Operation

Figure 36.3 to Figure 36.6 show operational amplifier control operation.

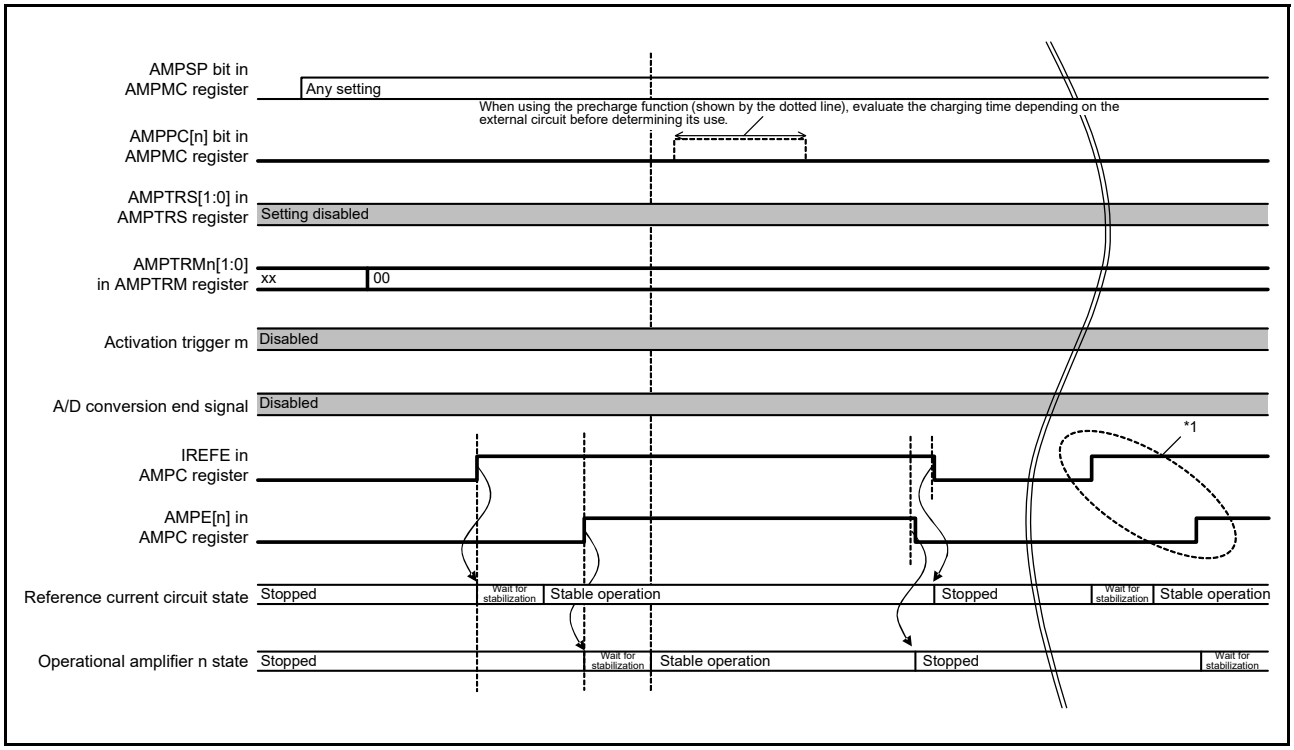


Figure 36.3 Operational amplifier control operation with software trigger mode used for control, and when the reference current circuit and operational amplifier are activated or stopped by software trigger mode

Note: n: Unit number (n = 0 to 3)
m: An activation trigger used to control operational amplifier unit n selected by the AMPTRS register.

Note 1. When operating or stopping the operational amplifier continuously, set the IREFE and AMPE[n] bits again as in the first setting after the operational amplifier is stopped.

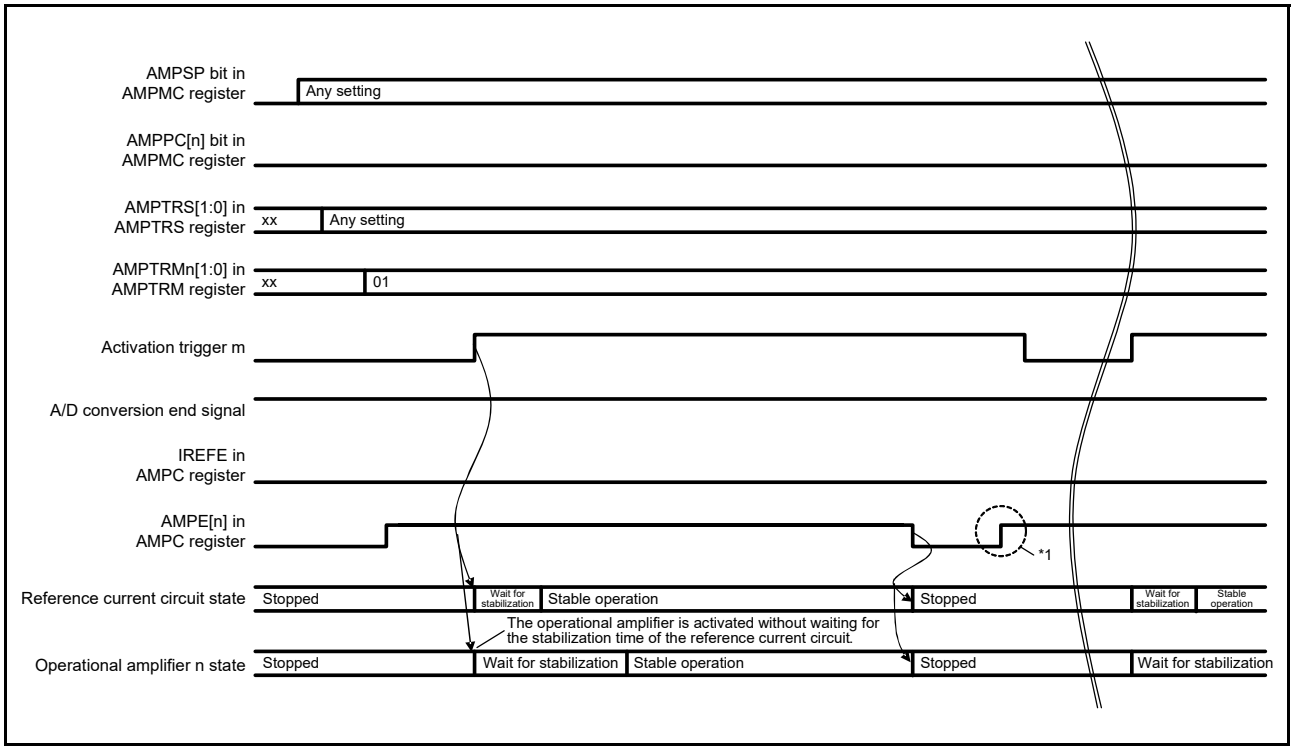


Figure 36.4 Operational amplifier control operation with activation trigger mode used for activation, and when the reference current circuit and operational amplifier are activated by an activation trigger and stopped by setting the AMPC register

Note: n: Unit number (n = 0 to 3)
m: An activation trigger used to control operational amplifier unit n selected by the AMPTRS register.
Set the AGT function.

Note 1. When operating/stopping the operational amplifier continuously, use the AMPE[n] bit again as in the first setting, and set the operational amplifier to wait for an activation trigger after it is stopped.

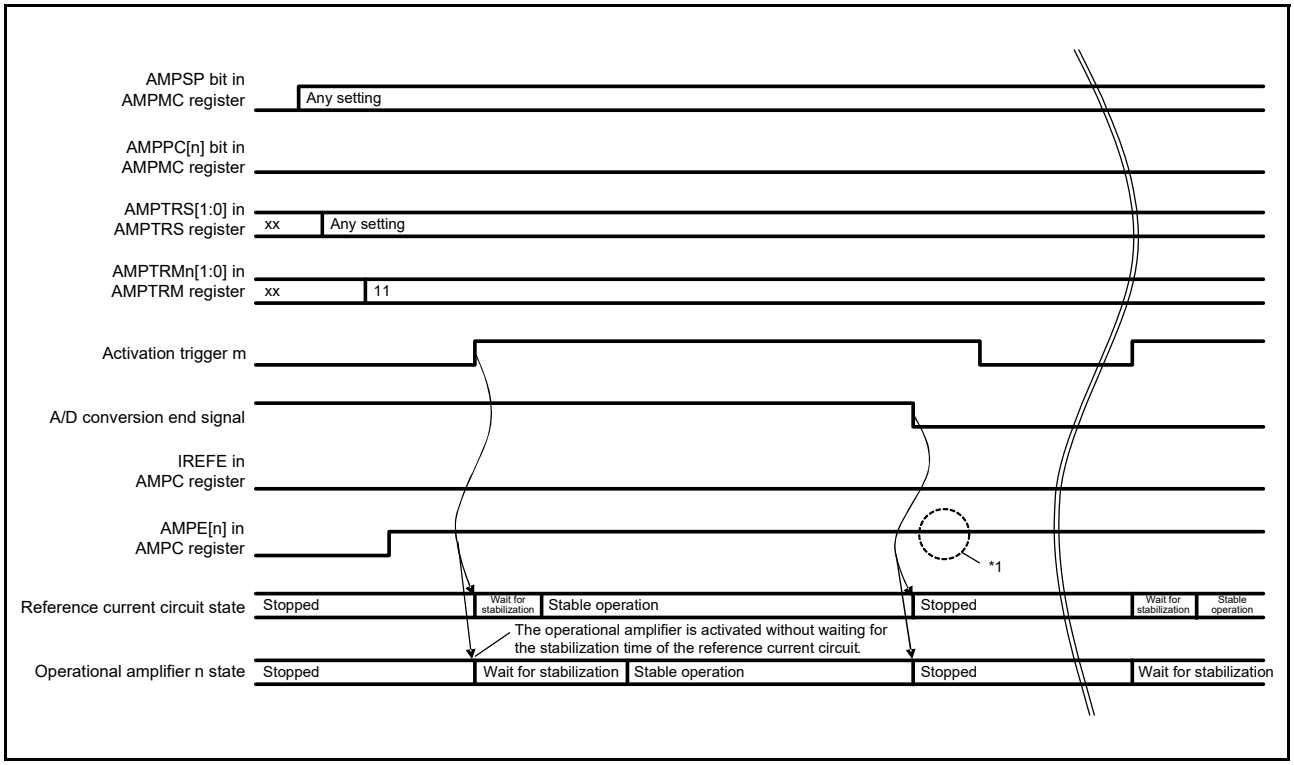


Figure 36.5 Operational amplifier control operation with activation and A/D trigger mode (1) and when the reference current circuit and operational amplifier are activated by an activation trigger and stopped by an A/D conversion end (trigger)

Note: n: Unit number (n = 0 to 3)
m: An activation trigger used to control operational amplifier unit n selected by the AMPTRS register.
Set the AGT function.

Note 1. When operating/stopping the operational amplifier continuously, it is not necessary to set the registers again because the operational amplifier waits for an activation trigger after it is stopped.

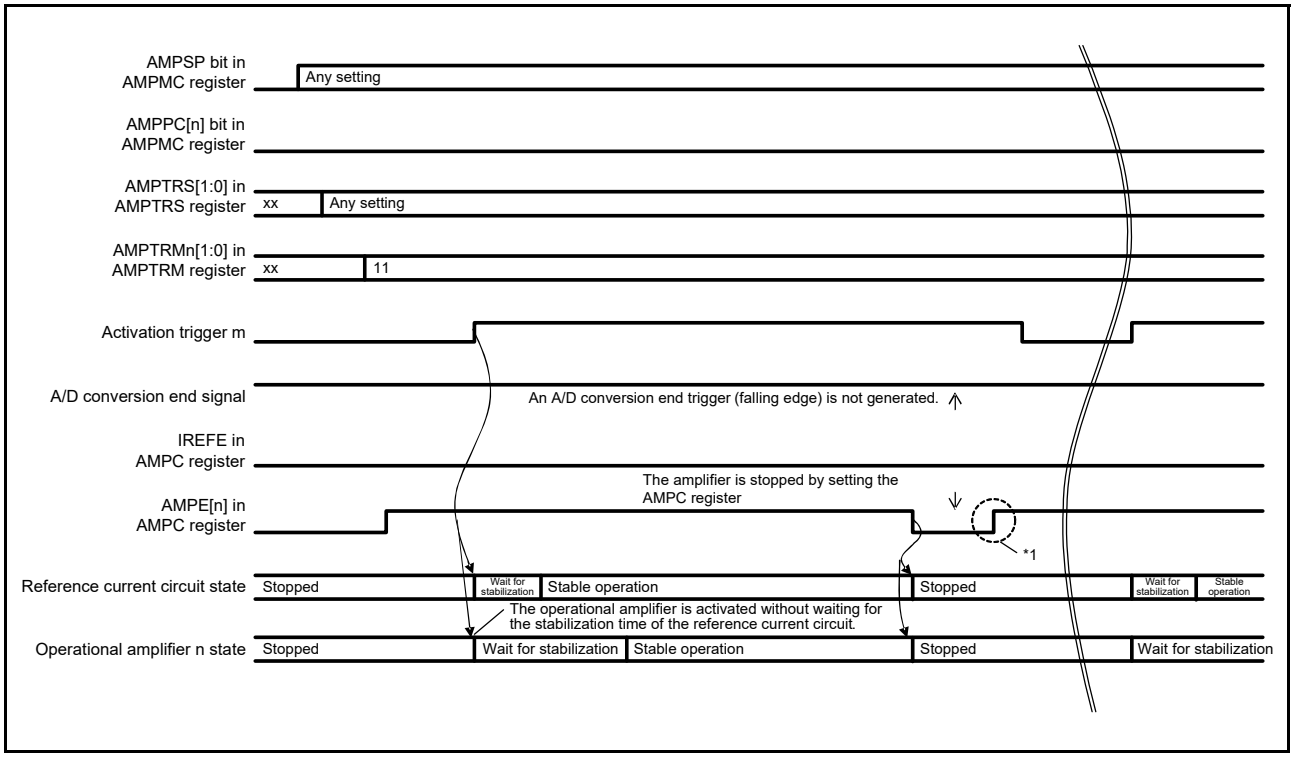


Figure 36.6 Operational amplifier control operation with activation and A/D trigger mode (2), and when the reference current circuit and operational amplifier are stopped by setting the AMPC register under the setting that they can be activated by an activation trigger and stopped by an A/D conversion end (trigger)

Note: n: Unit number (n = 0 to 3)
m: An activation trigger used to control operational amplifier unit n selected by the AMPTRS register.
Set the AGT function. See section 36.4, Software Trigger Mode for the procedure to activate the operational amplifier with an activation trigger.

Note 1. When operating/stopping the operational amplifier continuously, use the AMPE[n] bit again as in the first setting, and set the operational amplifier to wait for an activation trigger after it is stopped.

36.4 Software Trigger Mode

This section describes the procedure to activate and stop the operational amplifier using a software trigger. Figure 36.7 shows an example of each register setting.

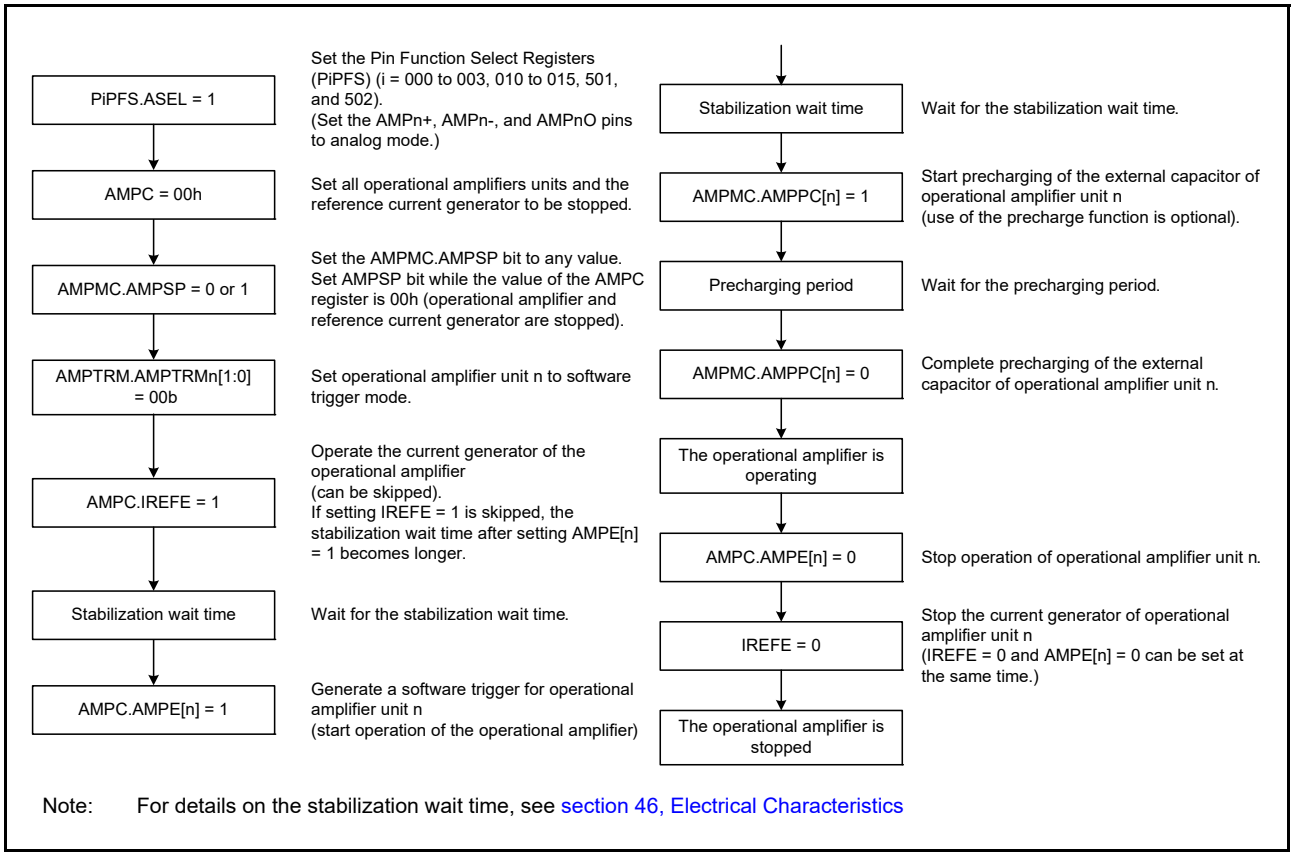


Figure 36.7 Procedure to start and stop OPAMP in software trigger mode

36.5 Activation Trigger Mode

This section describes the procedure to activate the operational amplifier using an activation trigger and to stop the amplifier with software. Figure 36.8 shows an example of each register setting.

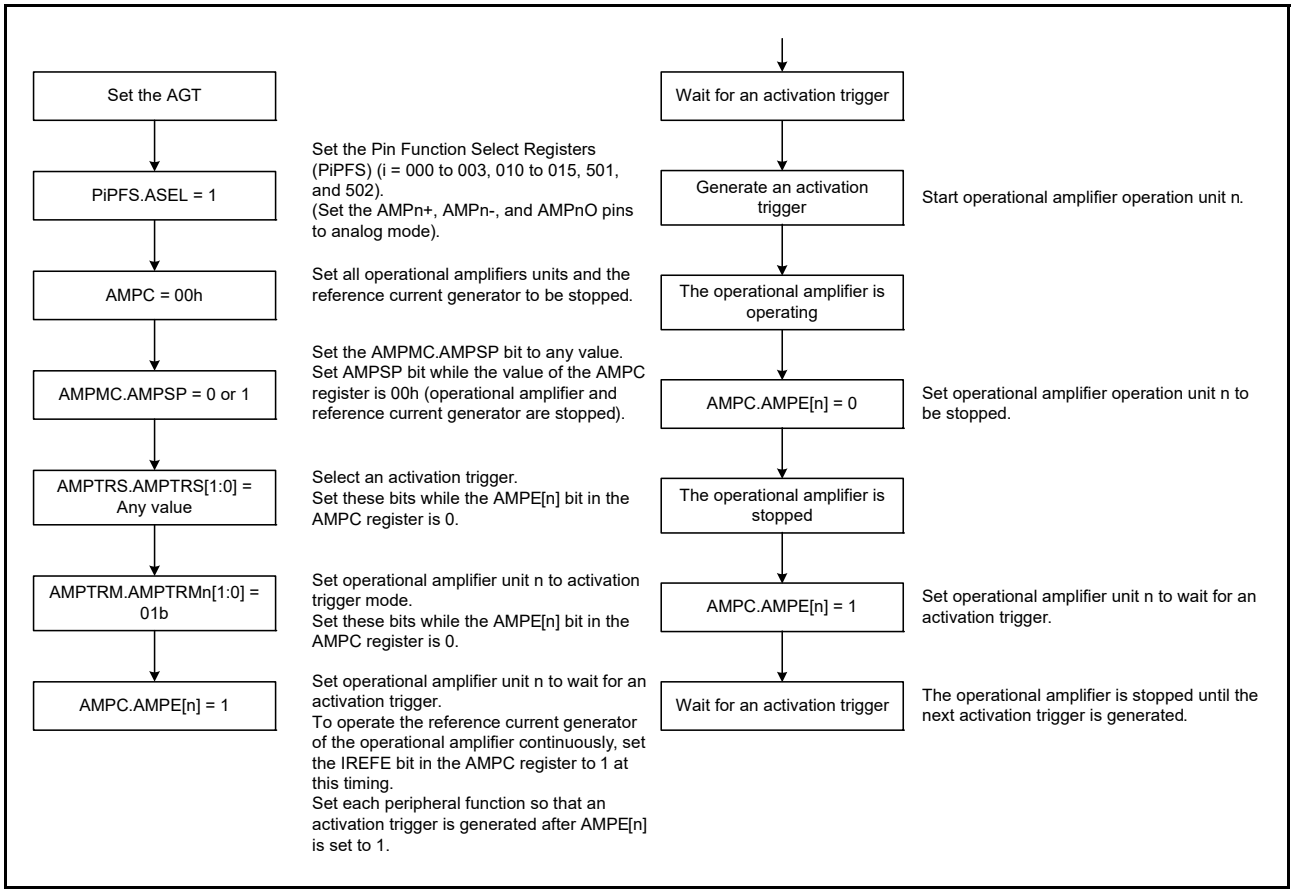


Figure 36.8 Procedure for starting and stopping the OPAMP in activation trigger mode

36.6 Activation and A/D Trigger Mode

This section describes the procedure to activate the operational amplifier using an activation trigger and to stop the amplifier with an A/D conversion end trigger. Figure 36.9 shows an example of each register setting.

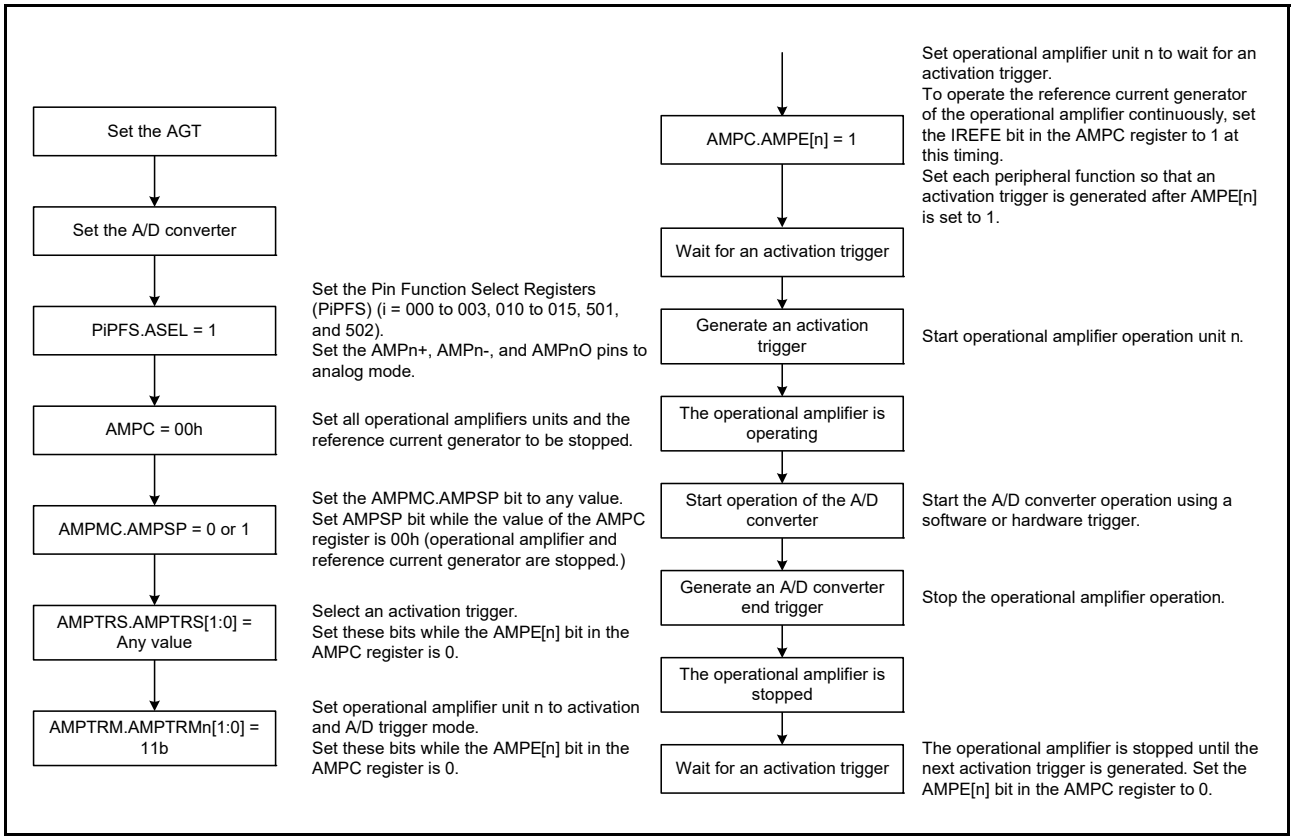


Figure 36.9 Procedure to activate the operational amplifier using an activation trigger and to stop the operational amplifier with an A/D conversion end trigger

36.7 Usage Notes

In addition to the AMPC register settings, the operational amplifier function can be activated by an activation trigger and stopped at the end of A/D conversion. The reference current circuit can be stopped at the end of A/D conversion. Design applications such as circuits and programs should conform to the operation flows to prevent these asynchronous triggers from causing conflicts between the activation and stop control.

Do not perform A/D conversion on pins that are used for positive and negative input of the operational amplifier because these pins are multiplexed with analog input for the A/D converter.

37. High-Speed Analog Comparator (ACMPHS)

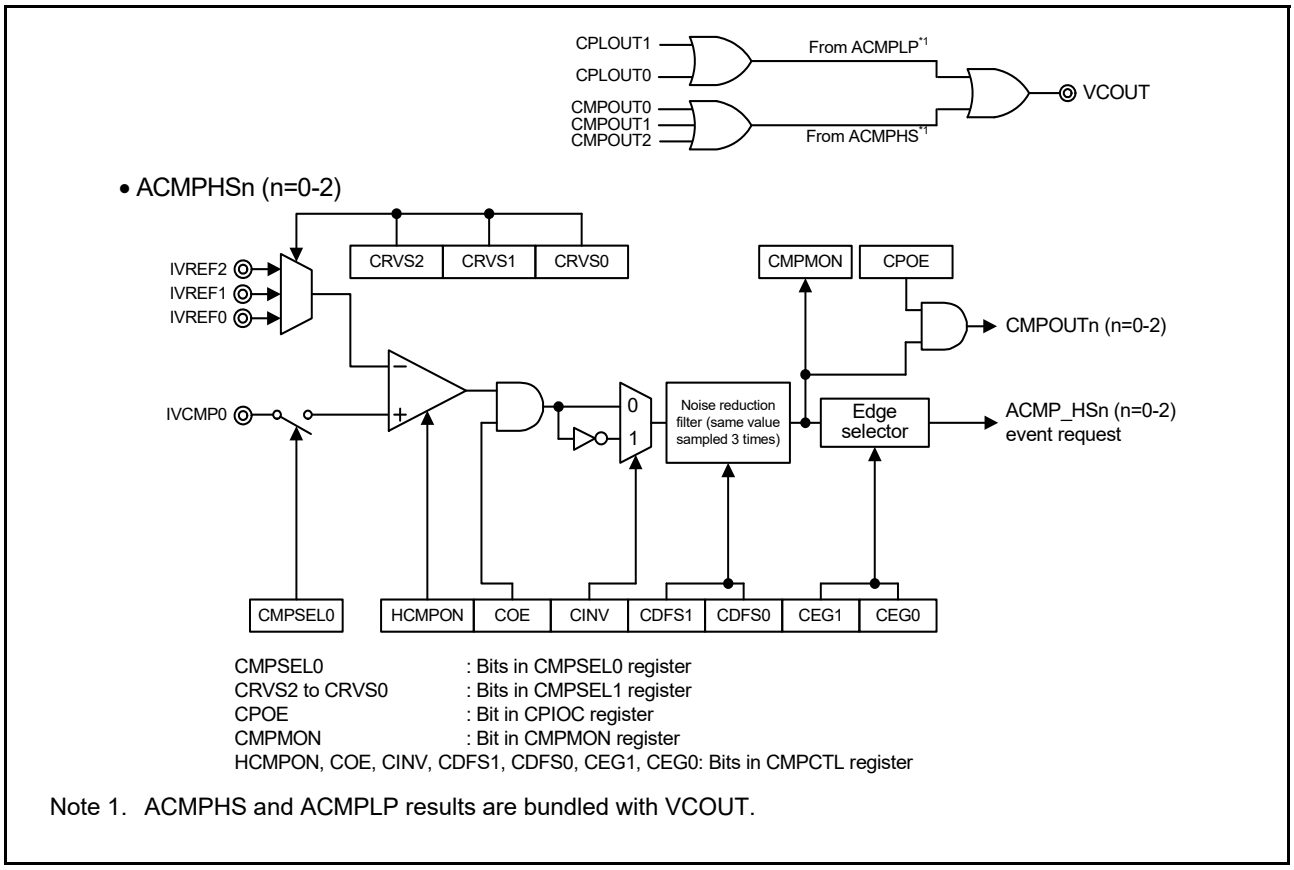
37.1 Overview

The High-Speed Analog Comparator (ACMPHS) compares a test voltage with a reference voltage and provides a digital output based on the result of conversion. Both the test voltage and the reference voltage are provided to the ACMPHS from the D/A converter output and an external source. This flexibility is useful in applications that require go/no-go comparisons to be performed between analog signals without requiring A/D conversion.

Table 37.1 lists the ACMPHS specifications, Figure 37.1 shows a block diagram, and Table 37.2 shows the input source configuration of the ACMPHS.

Table 37.1 ACMPHS specifications

Parameter	Description
Number of channels	3 channels (ACMPHS0, ACMPHS1 and ACMPHS2)
Analog input voltage	Input from internal A/D converter input pin
Reference voltage	• Output from internal D/A converter • Input from internal A/D converter input pin.
ACMPHS output	• Comparison result • Generation of ELC event output • Monitor output from register.
Interrupt request signal	• An interrupt request is generated on detecting a valid edge of comparison result • Rising edge, falling edge, or both edges can be selected.
Digital filter function	• One of three sampling frequencies can be selected • Not using the filter function can be selected.



Note 1. ACMPHS and ACMPLP results are bundled with VCOUT.

Figure 37.1 ACMPHS block diagram

Table 37.2 Input source configuration of the ACMPHS

Comparator	Reference voltage input source			Analog voltage input source	Output pin
	IVREF2	IVREF1	IVREF0	IVCMP0	
ACMPHS0	not exist	DA0*1	AN007	AN008	VCOUT*4
ACMPHS1	DA1*2	DA0*1	AN009	AN010	
ACMPHS2	DA2*3	DA0*1	AN001	AN000	

Note 1. When not using D/A converter 0 output (DA0), it can be used as AN009 analog input.
Note 2. When not using D/A converter 1 output (DA1), it can be used as AN010 and AN013 analog inputs.
Note 3. When not using D/A converter 2 output (DA2), it can be used as AN004 and AN006 analog inputs.
Note 4. ACMPHS0, ACMPHS1 and ACMPHS2 compare outputs are bundled with VCOUT pin.

37.2 Register Descriptions

37.2.1 Comparator Control Register (CMPCTL)

Address(es): ACMPHS0.CMPCTL 4008 5000h, ACMPHS1.CMPCTL 4008 5100h, ACMPHS2.CMPCTL 4008 5200h

	b7	b6	b5	b4	b3	b2	b1	b0
	HCMPON	CDFS[1:0]		CEG[1:0]		—	COE	CINV
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CINV	Comparator Output Polarity Selection*1, *2	0: Comparator output not inverted 1: Comparator output inverted.	R/W
b1	COE	Comparator Output Enable	0: Comparator output disabled (the output signal is low level) 1: Comparator output enabled.	R/W
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4, b3	CEG[1:0]	Selection of Valid Edge (Edge Selector)	b4 b3 0 0: No edge selection 0 1: Rising edge selection 1 0: Falling edge selection 1 1: Both-edge selection.	R/W
b6, b5	CDFS[1:0]	Noise Filter Selection*1, *2, *3	b6 b5 0 0: Noise filter not used 0 1: Noise filter sampling frequency is PCLKB/2^3 1 0: Noise filter sampling frequency is PCLKB/2^4 1 1: Noise filter sampling frequency is PCLKB/2^5.	R/W
b7	HCMPON	Comparator Operation Control*4	0: Operation stopped (the comparator outputs a low-level signal) 1: Operation enabled (input to the comparator pins is enabled).	R/W

Note 1. Change CDFS[1:0] and CINV bits only after disabling the ACMPHS output (COE = 0).
Note 2. If bits CDFS[1:0] and CINV are changed, an ACMPHS interrupt request and an ELC event can be generated. Change these bits only after setting the ELSRn register to 0 (the ACMPHS output is not linked). After changing these bits, initialize the IR flag bit in the IELSRn register to 0 (interrupt status flag cleared).
Note 3. If bits CDFS[1:0] are changed from 00b (noise filter is not used) to a value other than 00b (noise filter is used), perform sampling four times, update the filter output, then use the ACMPHS interrupt request or the ELC event.
Note 4. The operation stabilization wait time is required to permit ACMPHS operation after enabling ACMPHS operation (HCMPON = 1).
Operation stabilization wait time for ACMPHS0 to ACMPHS2 is 1 μs.

The CMPCTL register does the following:

- Controls the ACMPHS operation
- Enables or disables the ACMPHS output
- Selects the noise filter
- Selects the valid edge of the interrupt signal
- Selects the interrupt.

A reset clears this register to 00h.

37.2.2 Comparator Input Select Register (CMPSEL0)

Address(es): ACMPHS0.CMPSEL0 4008 5004h, ACMPHS1.CMPSEL0 4008 5104h, ACMPHS2.CMPSEL0 4008 5204h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CMPSEL0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CMPSEL0	Comparator Input Selection*1	0: No input 1: IVCMP0 selected*2.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Modify CMPSEL0 bits in the following procedure. Writing a value other than 0000 0000b while the value of CMPSEL0 register is not 0000 0000b is invalid. Writing 1 to two or more bits is also invalid. In both cases, the previous value is retained.
1. Set the CMPCTL.COE bit to 0.
2. Set CMPSEL0 register to 0000 0000b.
3. Set the CMPSEL0 bit to 1.
4. Wait for the input switching stabilization wait time (200 ns).
5. Set the CMPCTL.COE bit to 1.
6. Clear IR flag bit in the IELSRn register (interrupt status flag cleared).

Note 2. For details, see Table 37.2, Input source configuration of the ACMPHS.

37.2.3 Comparator Reference Voltage Select Register (CMPSEL1)

Address(es): ACMPHS0.CMPSEL1 4008 5008h, ACMPHS1.CMPSEL1 4008 5108h, ACMPHS2.CMPSEL1 4008 5208h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	CRVS[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	CRVS[2:0]	Reference Voltage Selection*1	b2 b0 0 0 0: No reference voltage 0 0 1: IVREF0 selected*2 0 1 0: IVREF1 selected*2 1 0 0: IVREF2 selected*2, *3. Other settings are prohibited.	R/W
b7to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Use the following procedure to modify the CRVS[5:0] bits. Writing a value other than 0000 0000b while the value of CMPSEL1 register is not 0000 0000b is invalid. Writing 1 to two or more bits is also invalid. In both cases, the previous value is retained.

To change the CRVS[5:0] bits:
1. Set the CMPCTL.COE bit to 0.
2. Set the CMPSEL1 register to 0000 0000b.
3. Set a new value to CRVS[2:0] bits (with 1 set in only one of the bits).
4. Wait for the input switching stabilization wait time of 200 ns.
5. Set the CMPCTL.COE bit to 1.
6. Set the IR flag in the IELSRn register to clear the interrupt status.

Note 2. For details, see Table 37.2, Input source configuration of the ACMPHS.

Note 3. This setting is prohibited in ACMPHS0.

37.2.4 Comparator Output Monitor Register (CMPMON)

Address(es): ACMPHS0.CMPMON 4008 500Ch, ACMPHS1.CMPMON 4008 510Ch, ACMPHS2, CMPMON 4008 520Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CMPMON
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CMPMON	Comparator Output Monitor*1	0: Comparator output low 1: Comparator output high.	R
b7 to b1	—	Reserved	These bits are read as 0	R

Note 1. When ACMPHS operation is enabled (HCMPON = COE = 1) but the noise filter is not in use (CDFS[1:0] = 00b), ensure that the CMPMON bit is read twice and the values are used only after the two consecutive values match.

37.2.5 Comparator Output Control Register (CPIOC)

Address(es): ACMPHS0.CPIOC 4008 5010h, ACMPHS1.CPIOC 4008 5110h, ACMPHS2.CPIOC 4008 5210h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CPOE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CPOE	Comparator Output Selection	0: VCOUT pin output of the comparator disabled (output signal is low) 1: VCOUT pin output of the comparator enabled.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R

37.3 Operation

The High-Speed Analog Comparator (ACMPHS) compares a reference voltage to an analog input voltage. Operation is not guaranteed when the register values are changed during ACMPHS operation. Table 37.3 shows the procedures for setting the registers associated with the ACMPHS.

Table 37.3 Procedure for setting registers associated with ACMPHS (1 of 2)

Step	Register	Bit	Setting
1	Associated MSTPCRD register	MSTPD26 to MSTPD28	0: Input clock supply
2	Associated Port mn Pin Function Select register (PmnPFS)	ASEL	1: Select the function of pins IVREF and IVCMP.

Table 37.3 Procedure for setting registers associated with ACMPHS (2 of 2)

Step	Register	Bit	Setting
3	Associated D/A converter		When using D/A convertor, set to the register.
4	ACMPHS0.CMPSEL0, CMPSEL1	CMPSEL0, CRVS0 to CRVS1	Select the ACMPHSn input, with 1 set in only one of the bits.
	ACMPHS1.CMPSEL0, CMPSEL1	CMPSEL0, CRVS0 to CRVS2	
	ACMPHS2.CMPSEL0, CMPSEL1	CMPSEL0, CRVS0 to CRVS2	
5	CMPCTL	CDFS[1:0], CEG1, CEG0, and CINV	Set the ACMPHSn control.
		HCMPON	1: Enable the ACMPHSn operation.
6	Waiting for the ACMPHS stabilization time (min. 1 μs).		
7	CMPCTL	COE	1: Enable the ACMPHSn output.
8	CPIOC	CPOE	1: Set the VCOUT output.
	Associated Port mn Pin Function Select register (PmnPFS)	PSEL, PMR	Select the VCOUT port function.
9	IELSRn	IR, IELS[7:0]	When using an interrupt, select the interrupt status flag and the ICU event link.*1
10	ELSRn	ELS[7:0]	When using an ELC, select the event link.*2
11	POEGGn	CDRE[2:0]	When using an POEG, enable the request from the ACMPHS.
12	Operation started		
13	CMPCTL	COE	0: When changing IVREF or IVCMP, disable ACMPHSn output.
14	ACMPHS0.CMPSEL1	CRVS0 to CRVS1	Modify CRVSn bits as follows: Set the CMPSEL1 register to 0000 0000b. Set a new value to CRVSn bits, with 1 set in only one of the bits.
	ACMPHS1.CMPSEL1	CRVS0 to CRVS2	
	ACMPHS2.CMPSEL1	CRVS0 to CRVS2	
15	Waiting for the ACMPHSn switching stabilization time (min. 200 ns).		
16	CMPCTL	COE	1: Enable the ACMPHSn output.
17	Operation restarted		

Note 1. After ACMPHSn is set, an unnecessary interrupt might occur until operation becomes stable, so initialize the interrupt flag.

Note 2. After ACMPHSn is set, an unnecessary interrupt might occur until operation becomes stable, so initialize the event link select.

Figure 37.2 shows an example of ACMPHS operation. The VCOUT output becomes 1 when the analog input voltage is higher than the ACMPHS reference input voltage, and the VCOUT output becomes 0 when the analog input voltage is lower than the reference voltage. When the ACMPHS output changes, an interrupt request and an ELC event are output.

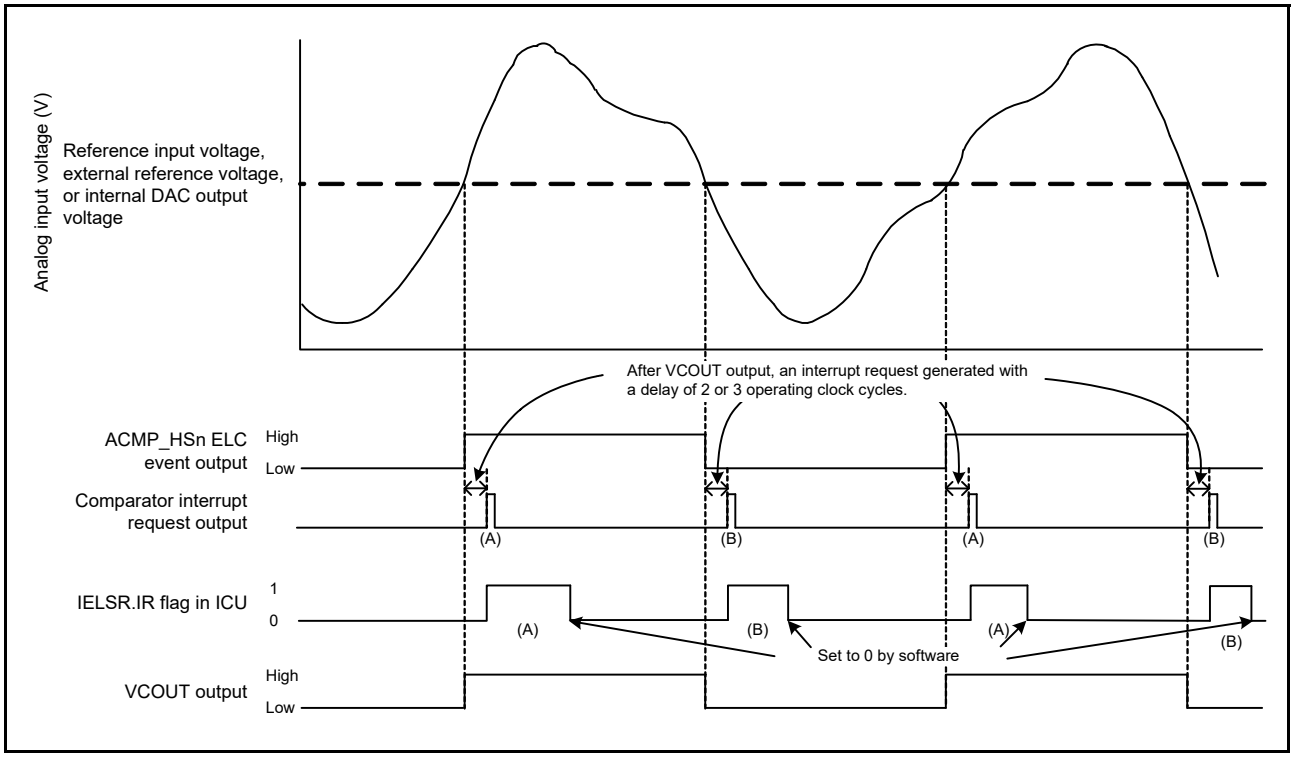


Figure 37.2 ACMPHS operation example

Figure 37.2 applies when CPOE = 1 (pin output enabled), CDFS[1:0] = 00b (filter not used), and CEG1 = CEG0 = 1 (both-edge selection). When CINV = 0, CEG0 = 1, and CEG1 = 0 (rising-edge selection for non-inversion output signal from the ACMPHS), IELSR.IR flag changes as shown by (A) only. When CINV = 0, CEG0 = 0, and CEG1 = 1 (falling-edge selection for non-inversion output signal from the ACMPHS), IR flag changes as shown by (B) only. When CPOE = 1, VCOUT directly outputs the ELC event output.

37.4 Noise Filter

The ACMPHS contains a noise filter. The sampling clock is selected by the CMPCTL.CDFS[1:0] bits. The ACMPHS signal is sampled on each sampling clock. If the same value is sampled three times, the noise filter output at the next sampling clock cycle is used as the ACMPHS output.

Figure 37.3 shows the configuration of the noise filter and edge detector and Figure 37.4 shows an example of noise filter and interrupt operation. When using an interrupt and ELC is in Software Standby mode, set the CMPCTL.CDFS[1:0] bits to 00b (noise filter not used).

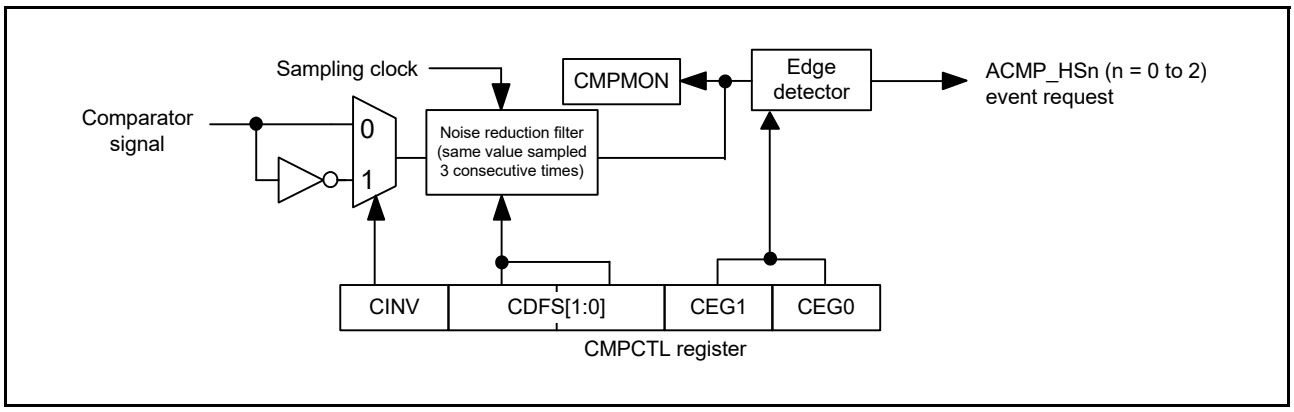


Figure 37.3 Noise filter and edge detection configuration

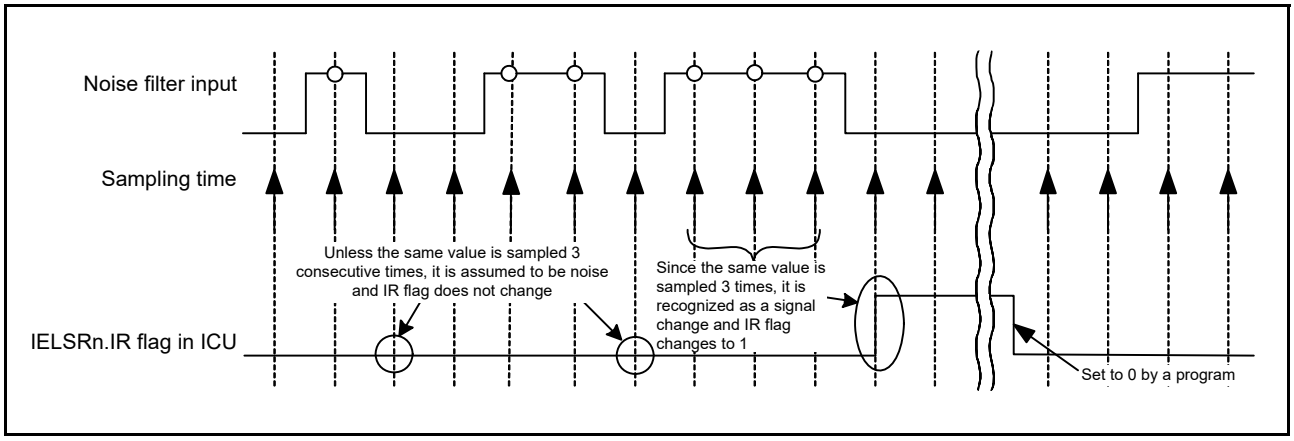


Figure 37.4 Noise filter and interrupt operation example

The operation example in Figure 37.4 applies when the CMPCTL.CDFS[1:0] bits are 01b, 10b, or 11b (noise filter used).

37.5 ACMPHS Interrupts

ACMPHS generates three interrupt requests from ACMPHS0, ACMPHS1 and ACMPHS2. To use an ACMPHS interrupt, select it in the IELSR register in the Interrupt Controller Unit (ICU). Set at least one of the CMPCTL.CEG0 or CMPCTL.CEG1 bits to 1, that is, to a value other than 00b for no edge selection.

For details on the register setting related to ACMPHS interrupt request, see section 37.2.1, Comparator Control Register (CMPCTL).

37.6 ACMPHS Output to the Event Link Controller (ELC)

The ELC uses the ACMPHS interrupt request signal as an ELC event signal, enabling link operation for the preset module. To use the ACMPHS ELC event, select it in the ELSR register in the ELC. When using the ELC event request, set at least one of the CMPCTL.CEG0 or CMPCTL.CEG1 bits to 1, that is, to a value other than 00b for no edge selection.

37.7 ACMPHS Pin Output

The comparison result from the ACMPHS can be output to external pins. Use the CMPCTL.CINV and CPIOC.CPOE bits to set the output polarity (non-inverted or inverted output) and enable or disable output. To output the ACMPHS comparison result to the VCOUT output pin, set the associated Port mn Pin Function Select register (PmnPFS) in the I/O register.

37.8 Usage Notes

37.8.1 Settings for the Module-Stop Function

The Module Stop Control Register can enable or disable ACMPHS operation. The ACMPHS is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

37.8.2 Relationship with ADC14

For information about the constraints on simultaneous use of ACMPHS analog input and A/D converter analog input, see section 33.8.13, Relationship between the A/D converter, OPAMP, ACMPHS, and ACMPLP.

38. Low-Power Analog Comparator (ACMPLP)

38.1 Overview

The Low-Power Analog Comparator (ACMPLP) compares a reference input voltage and an analog input voltage. ACMPLP0 and ACMPLP1 are independent of each other.

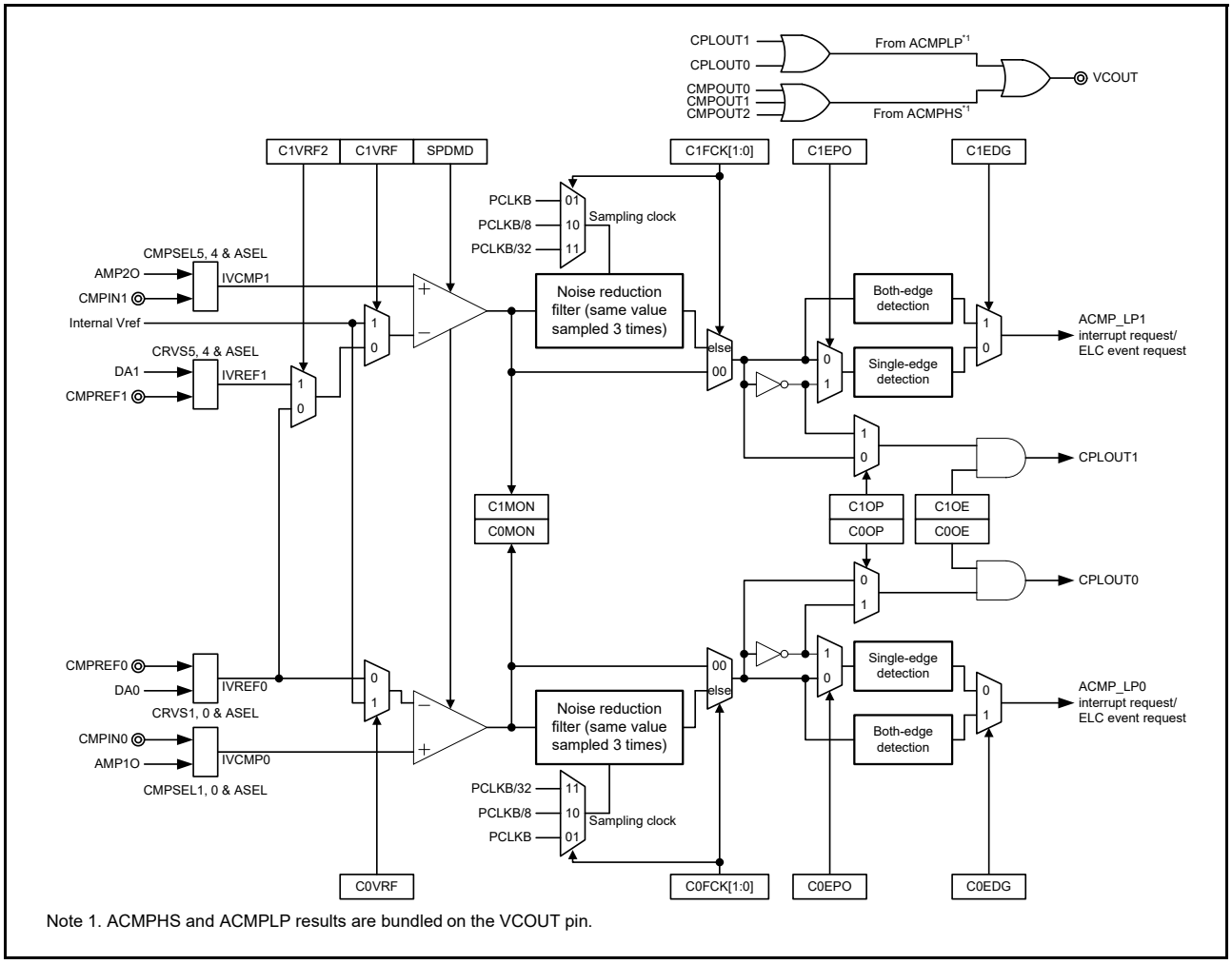
The comparison result of the reference input voltage and analog input voltage can be read by software. The comparison result can also be output externally. The reference input voltage can be selected from an input to the CMPREFi (i = 0, 1) pin, an output from internal D/A converter, and the internal reference voltage (Vref) generated internally in the MCU.

The ACMPLP response speed can be set before starting an operation. Setting high-speed mode decreases the response delay time, but increases current consumption. Setting low-speed mode increases the response delay time, but decreases current consumption.

Table 38.1 lists the ACMPLP specifications, Figure 38.1 shows a block diagram of the ACMPLP when the window function is disabled, and Figure 38.2 shows a block diagram of the ACMPLP when the window function is enabled. Table 38.2 lists the I/O pins of the ACMPLP.

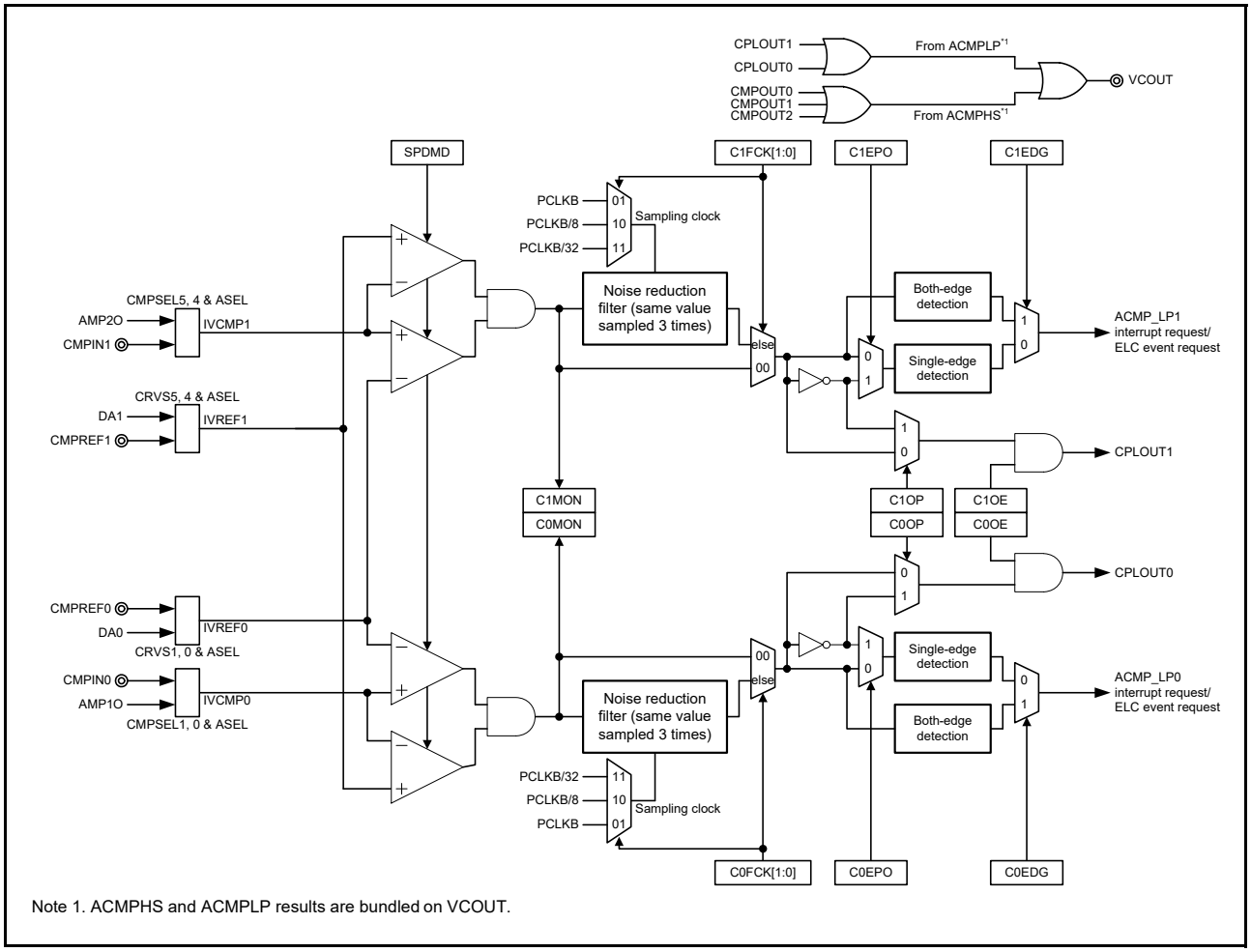
Table 38.1 ACMPLP specifications

Parameter	Description
Number of channels	2 channels (ACMPLP0 and ACMPLP1)
Analog input voltage	• Input from CMPINi (i = 0, 1) pin • Output from internal operational amplifier (AMP1O, AMP2O).
Reference voltage	• Standard mode Selectable from one of the following: - Internal reference voltage (Vref) - Input from CMPREFi (i = 0, 1) pin - Output from internal D/A converter. • Window mode Selectable from one of the following: - Input from CMPREFi (i = 0, 1) pin (CMPREF0: Low reference, CMPREF1: High reference) - Output from internal D/A converter.
Comparator output	• Comparison result • Generation of ELC event output • Monitor output from register.
Interrupt request signal	• An interrupt request is generated on detecting a valid edge of comparison result • Rising edge, falling edge, or both edges can be selected.
Selectable functions	• Noise filter function - One of three sampling frequencies can be selected - Not using the filter function can be selected. • Window function - Whether the window function is used or not can be selected. • Low-Power Analog Comparator response speed - High-speed mode or low-speed mode can be selected.



Note 1. ACMPHS and ACMPLP results are bundled on the VCOUT pin.

Figure 38.1 ACMPLP block diagram when window function is disabled in standard mode



Note 1. ACMPHS and ACMPLP results are bundled on VCOUT.

Figure 38.2 ACMPLP block diagram when window function is enabled in window function mode

Table 38.2 Comparator pin configuration

Comparator	Reference voltage input pin		Analog voltage input pin		Output pin
	Standard mode	Window function mode	Standard mode	Window function mode	
ACMPLP0	• IVREF0 (CMPREF0/DA0) • Internal Vref (selectable)	Low reference voltage: • IVREF0 (CMPREF0/DA0) High reference voltage: • IVREF1 (CMPREF1/DA1)	• IVCMP0 (CMPIN0/AMP1O)		VCOUT*1
ACMPLP1	• IVREF0 (CMPREF0/DA0) • IVREF1 (CMPREF1/DA1) • Internal Vref (selectable)		• IVCMP1 (CMPIN1/AMP2O)		

Note 1. ACMPHSm (m = 0 to 2) and ACMPLPn (n = 0, 1) results are bundled on the VCOUT pin.

38.2 Register Descriptions

38.2.1 ACMPLP Mode Setting Register (COMPMDR)

Address(es): ACMPLP.COMPMDR 4008 5E00h

	b7	b6	b5	b4	b3	b2	b1	b0
	C1MON	C1VRF	C1WDE	C1ENB	C0MON	C0VRF	C0WDE	C0ENB
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	C0ENB	ACMPLP0 Operation Enable	0: Disable comparator channel ACMPLP0 1: Enable comparator channel ACMPLP0.	R/W
b1	C0WDE	ACMPLP0 Window Function Mode Enable*1,*2	0: Disable window function for ACMPLP0 1: Enable window function for ACMPLP0.	R/W
b2	C0VRF	ACMPLP0 Reference Voltage Selection	0: IVREF0 input 1: internal reference voltage (Vref). *4	R/W
b3	C0MON	ACMPLP0 Monitor Flag*3	When the window function is disabled: 0: IVCMP0 < ACMPLP0 reference voltage 1: IVCMP0 > ACMPLP0 reference voltage. When the window function is enabled: 0: IVCMP0 < IVREF0 or IVCMP0 > IVREF1 1: IVREF0 < IVCMP0 < IVREF1.	R
b4	C1ENB	ACMPLP1 Operation Enable	0: Disabled 1: Enabled.	R/W
b5	C1WDE	ACMPLP1 Window Function Mode Enable*1,*2	0: Disable ACMPLP1 operation 1: Enable ACMPLP1 operation.	R/W
b6	C1VRF	ACMPLP1 Reference Voltage Selection	0: IVREF0 or IVREF1 1: internal reference voltage (Vref). *4	R/W
b7	C1MON	ACMPLP1 Monitor Flag*3	When the window function is disabled: 0: IVCMP1 < ACMPLP1 reference voltage 1: IVCMP1 > ACMPLP1 reference voltage. When the window function is enabled: 0: IVCMP1 < IVREF0 or IVCMP1 > IVREF1 1: IVREF0 < IVCMP1 < IVREF1.	R

Note 1. Window function mode cannot be set when low-speed mode is selected (the SPDMD bit in the COMPOCR register is 0).

Note 2. In window function mode, the reference voltage in the comparator is selected regardless of this bit setting.

Note 3. The initial value is 0 immediately after a reset is released. However, the value is undefined when C0ENB is set to 0 and C1ENB is set to 0 after operation of the comparator is enabled once.
When the reference level is equal to the input level, the bit value is undefined.

Note 4. The setting is effective only when in standard mode. When in window function mode, IVREF0 or IVREF1 is selected regardless of this bit setting.

38.2.2 ACMPLP Filter Control Register (COMPFIR)

Address(es): ACMPLP.COMPFIR 4008 5E01h

	b7	b6	b5	b4	b3	b2	b1	b0
	C1EDG	C1EPO	C1FCK[1:0]		C0EDG	C0EPO	C0FCK[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	C0FCK[1:0]	ACMPLP0 Filter Select*1	b1 b0 0 0: No sampling (bypass) 0 1: Sampling at PCLKB 1 0: Sampling at PCLKB/8 1 1: Sampling at PCLKB/32.	R/W
b2	C0EPO	ACMPLP0 Edge Polarity Switching*1	0: Interrupt and ELC event request on the rising edge 1: Interrupt and ELC event request on the falling edge.	R/W
b3	C0EDG	ACMPLP0 Edge Detection Selection*1	0: Interrupt and ELC event request by one-edge detection 1: Interrupt and ELC event request by both-edge detection.	R/W
b5, b4	C1FCK[1:0]	ACMPLP1 Filter Select*1	b5 b4 0 0: No sampling (bypass) 0 1: Sampling at PCLKB 1 0: Sampling at PCLKB/8 1 1: Sampling at PCLKB/32.	R/W
b6	C1EPO	ACMPLP1 Edge Polarity Switching*1	0: Interrupt and ELC event request on the rising edge 1: Interrupt and ELC event request on the falling edge.	R/W
b7	C1EDG	ACMPLP1 Edge Detection Selection*1	0: Interrupt and ELC event request by one-edge detection 1: Interrupt and ELC event request by both-edge detection.	R/W

Note 1. If bits CiFCK[1:0], CiEPO, and CiEDG (i = 0, 1) are modified, an ACMPLP interrupt request and an ELC event request can be generated. Change these bits only after setting event link to deselected. Also, be sure to clear the associated interrupt request flag.

38.2.3 ACMPLP Output Control Register (COMPOCR)

Address(es): ACMPLP.COMPOCR 4008 5E02h

	b7	b6	b5	b4	b3	b2	b1	b0
	SPDMD	C1OP	C1OE	—	—	C0OP	C0OE	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R
b1	C0OE	ACMPLP0 VCOUT Pin Output Enable*1	0: ACMPLP0 VCOUT pin output disabled 1: ACMPLP0 VCOUT pin output enabled.	R/W
b2	C0OP	ACMPLP0 VCOUT Output Polarity Selection*1	0: Non-inverted 1: Inverted.	R/W
b4, b3	—	Reserved	These bits are read as 0. The write value should be 0.	R
b5	C1OE	ACMPLP1 VCOUT Pin Output Enable*1	0: ACMPLP1 VCOUT pin output disabled 1: ACMPLP1 VCOUT pin output enabled.	R/W
b6	C1OP	ACMPLP1 VCOUT Output Polarity Selection*1	0: Non-inverted 1: Inverted.	R/W
b7	SPDMD	ACMPLP0/ACMPLP1 Speed Selection*2	0: Comparator low-speed mode 1: Comparator high-speed mode.	R/W

Note 1. ACMPHSm (m = 0 to 2) and ACMPLPn (n = 0, 1) results are bundled on the VCOUT pin.
Note 2. When rewriting the SPDMD bit, be sure to set the CiENB bit (i = 0, 1) in the COMPMDR register to 0 in advance.

38.2.4 Comparator Input Select Register (COMPSEL0)

Address(es): ACMPLP.COMPSEL0 4008 5E04h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CMPSEL[5:4]		—	—	CMPSEL[1:0]	
Value after reset:	0	0	0	1	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b1, b0	CMPSEL[1:0]	ACMPLP0 Input (IVCMP0) Selection	b1 b0 0 0: No input 0 1: CMPIN0 input selected 1 0: AMP1O output selected. Other settings are prohibited.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5, b4	CMPSEL[5:4]	ACMPLP1 Input (IVCMP1) Selection	b5 b4 0 0: No input 0 1: CMPIN1 input selected 1 0: AMP2O output selected. Other settings are prohibited.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

38.2.5 Comparator Reference Voltage Select Register (COMPSEL1)

Address(es): ACMPLP.COMPSEL1 4008 5E05h

	b7	b6	b5	b4	b3	b2	b1	b0
	C1VRF2	—	CRVS[5:4]		—	—	CRVS[1:0]	
Value after reset:	1	0	0	1	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b1, b0	CRVS[1:0]	ACMPLP0 Reference Voltage (IVREF0) Selection	b1 b0 0 0: No reference voltage 0 1: CMPREF0 selected 1 0: DA0 output selected. Other settings are prohibited.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5, b4	CRVS[5:4]	ACMPLP1 Reference Voltage (IVREF1) Selection	b5 b4 0 0: No reference voltage 0 1: CMPREF1 selected 1 0: DA1 output selected. Other settings are prohibited.	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	C1VRF2	ACMPLP1 Reference Voltage Selection 2	0: IVREF0 selected 1: IVREF1 selected.	R/W

38.3 Operation

ACMPLP0 and ACMPLP1 operate independently, and their operations are the same. Operation is not guaranteed when the values of their associated registers are changed during comparator operation. Table 38.3 shows the procedure for setting the ACMPLP associated registers.

Table 38.3 Procedure for setting the ACMPLP associated registers (i = 0, 1)

Step No.	Register	Bit	Setting	
1	MSTPCRD	MSTPD29	0: Input clock supply	
2	Corresponding Port mn Pin Function Select Register (PmnPFS)	ASEL	Select the analog input	
	COMPSEL0	CMPSEL[1:0], CMPSEL[5:4]		
3	COMPOCR	SPDMD	Select the comparator response speed (0: Low-speed mode / 1: High-speed mode)*1	
4	COMPMDR	CiWDE	0: Window function mode disable	1: Window function mode enable*2
		CiVRF	Select the reference voltage	Window comparator operation (reference = IVREF0 and IVREF1*3)
	COMPSEL1	CRVS[1:0], CRVS[5:4], C1VRF2		
	COMPMDR	CiENB	1: Operation enabled	
5	Waiting for the comparator stabilization time T_{cmp} (min. 100 μs).			
6	COMPFIR	CiFCK[1:0]	Select whether the digital filter is used or not and the sampling clock.	
		CiEPO, CiEDG	Select the edge detection condition for an interrupt request (rising edge/ falling edge/both edges).	
7	COMPOCR	CiOP, CiOE	Set the VCOUT output (select the polarity and set output enabled or disabled).	
	Corresponding Port mn Pin Function Select Register (PmnPFS)	PSEL, PMR	Select the VCOUT port function.	
8	IELSRn	IR, IELS[7:0]	When using an interrupt: select the interrupt status flag, ICU event link select.*3	
9	ELSRn	ELS[7:0]	When using an ELC: Select the Event Link Select.*4	
10	Operation started			

Note 1. ACMPLP0 and ACMPLP1 cannot be set independently.
Note 2. Can be set in high-speed mode (SPDMD = 1).
Note 3. After the comparator setting, an unnecessary interrupt might occur until operation becomes stable, therefore initialize the interrupt flag.
Note 4. After the comparator setting, an unnecessary interrupt might occur until operation becomes stable, therefore initialize the event link select.

Figure 38.3 shows an operating example of the ACMPLPi (i = 0, 1) when window function is disabled.

The reference input voltage (IVREFi) or internal reference voltage (Vref) and the analog input voltage (IVCMPi) are compared. If the analog input voltage is higher than the reference input voltage, the COMPMDR.CiMON bit is set to 1.

If the analog input voltage is lower than the reference input voltage, the CiMON bit is set to 0.

ACMPLPi outputs an interrupt to ICU. For details on the interrupt, see section 38.5, ACMPLP Interrupts.

ACMPLPi outputs an event signals to the ELC to activate other modules. For details on the ELC, see section 38.6, ELC Event Output.

The values of the registers should not be changed during comparison.

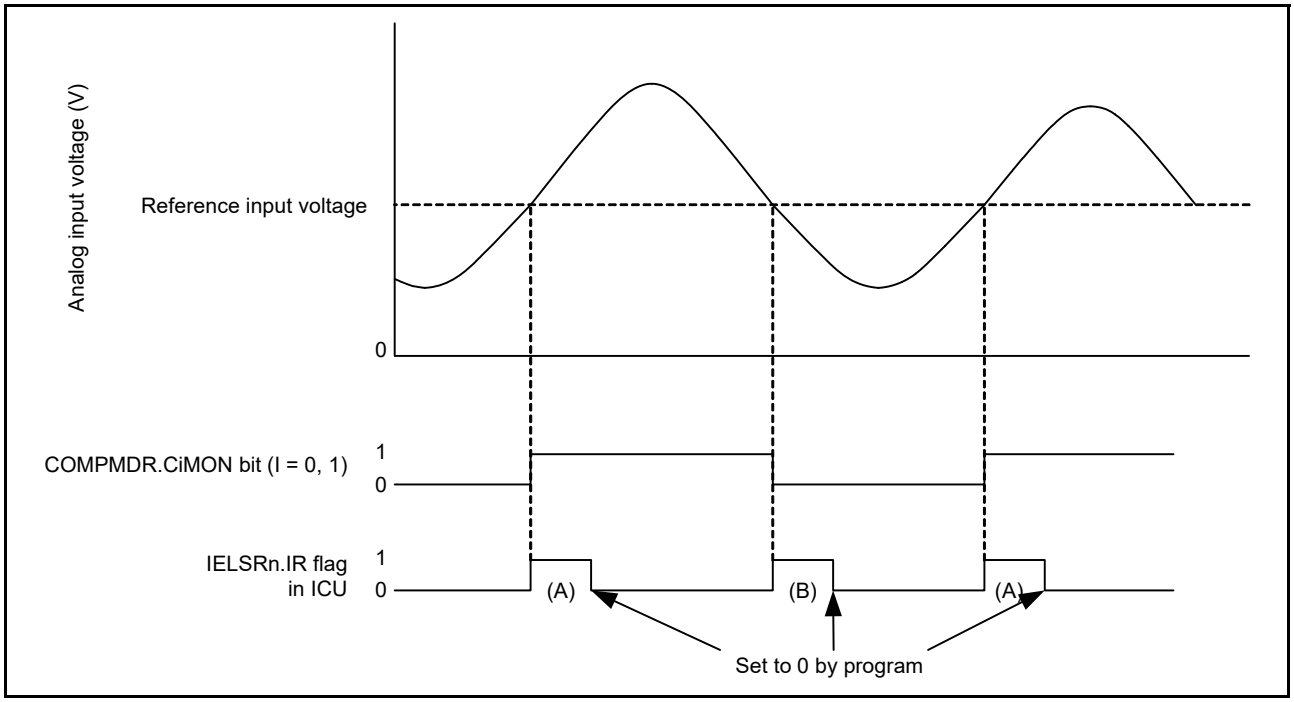


Figure 38.3 Operating example of ACMPLPi (i = 0, 1) when window function is disabled

Figure 38.3 applies when the following conditions are met.

CiFCK[1:0] = 00b (no sampling) and CiEDG = 1 (both edges).

When CiEDG = 0 and CiEPO = 0 (rising edge), IELSRn.IR changes as shown by (A) only.

When CiEDG = 0 and CiEPO = 1 (falling edge), IELSRn.IR changes as shown by (B) only.

Figure 38.4 shows an operation example of ACMPLPi (i = 0, 1) when the window function is enabled.

The reference voltage (IVREF0/IVREF1) and the analog input voltage are compared. The CiMON bit is set to 1 when IVREF0 < the analog input voltage < IVREF1, and the CiMON bit is set to 0 when the analog input voltage < IVREF0 or IVREF1 < the analog input voltage.

ACMPLPi outputs an interrupt to ICU. For details on the interrupt, see section 38.5, ACMPLP Interrupts. ACMPLPi also outputs an event signals to the ELC to activate other modules. For details on the ELC, see section 38.6, ELC Event Output. Do not change the values of the registers during comparison.

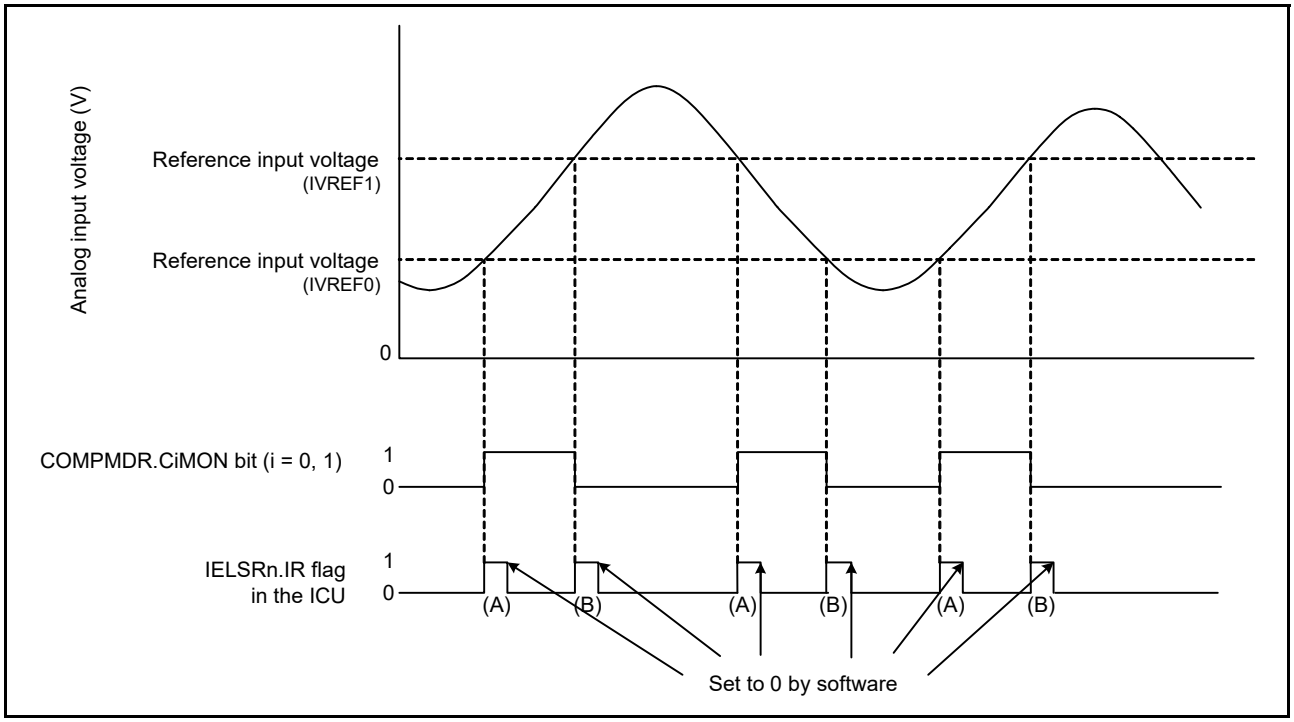


Figure 38.4 Operating example of ACMPLPi (i = 0, 1) when window function is enabled

Figure 38.4 applies when the following conditions are met.

CiFCK[1:0] = 00b (No sampling) and CiEDG = 1 (both edges).

When CiEDG = 0 and CiEPO = 0 (rising edge), IELSRn.IR changes as shown by (A) only.

When CiEDG = 0 and CiEPO = 1 (falling edge), IELSRn.IR changes as shown by (B) only.

38.4 Noise Filter

Figure 38.5 shows the configuration of the ACMPLPi noise filter and edge detection configuration, and Figure 38.6 shows an operating example of the ACMPLPi noise filter.

The sampling clock can be selected in the COMPFIR.CiFCK[1:0] bits. The ACMP_LPi signal (internal signal) output from ACMPLPi is sampled at every sampling clock cycle. When the level matches three times, the corresponding IELSRn.IR bit is set to 1 (interrupt requested) and an ELC event is output.

When using an interrupt and ELC in Software Standby mode, set the COMPFIR.CiFCK[1:0] bits to 00b (bypass).

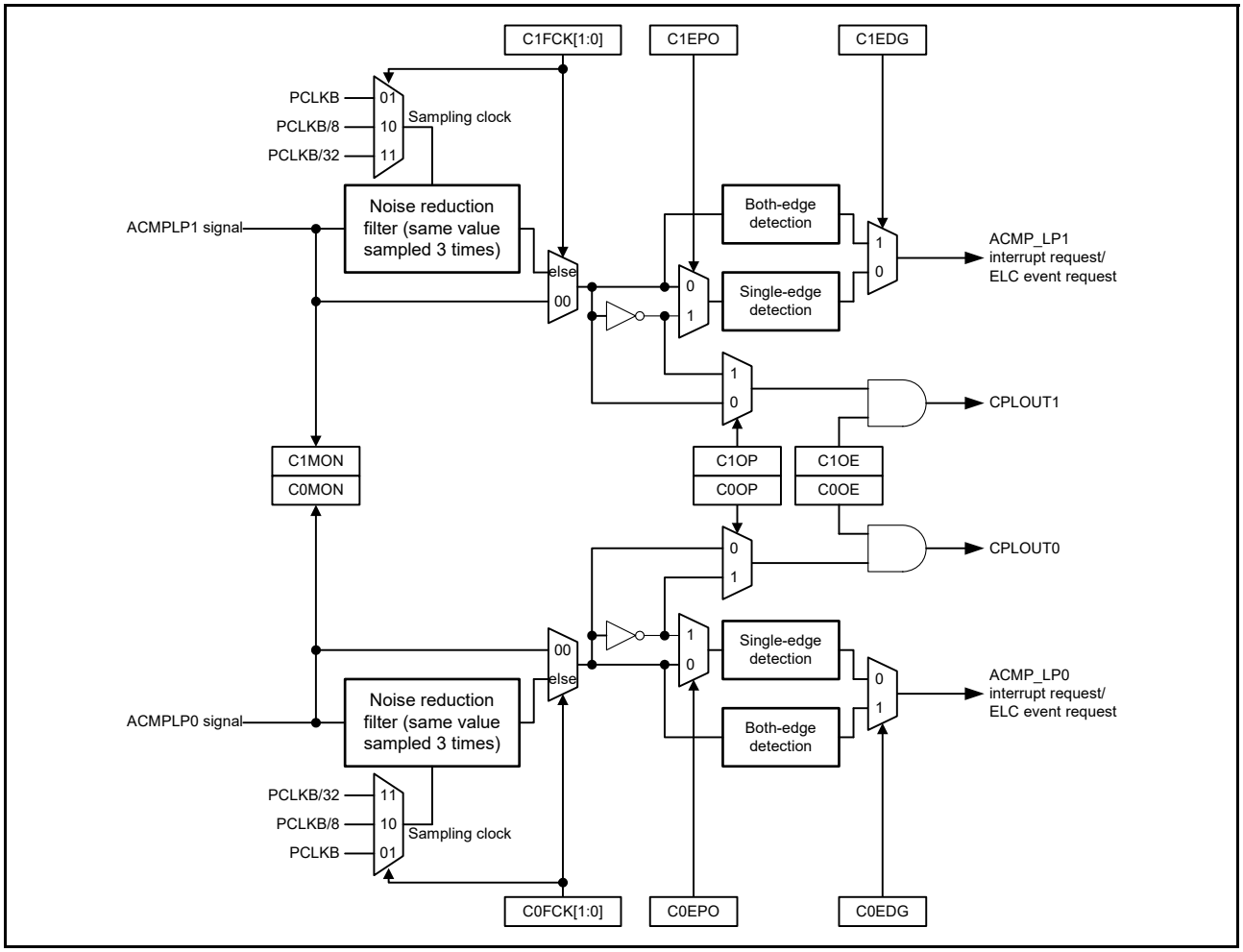


Figure 38.5 Noise filter and edge detection configuration

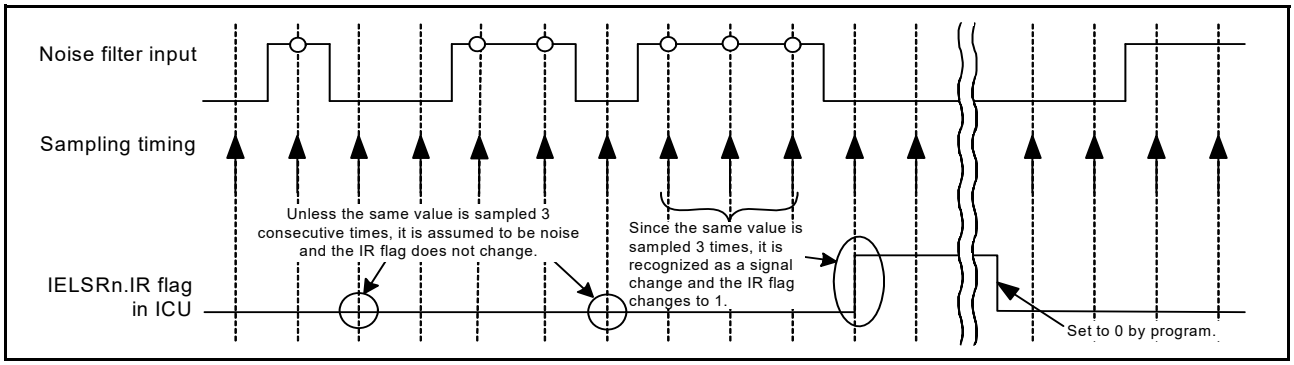


Figure 38.6 Noise filter and interrupt operation example

38.5 ACMPLP Interrupts

The ACMPLP generates two interrupt requests from ACMPLP0 and ACMPLP1 sources. The ACMPLPi (i = 0 and 1) interrupt can be used by selecting it in the IELSRn register in the ICU.

To use the ACMPLPi interrupt, select either single-edge detection or both-edge detection using the COMPFIR.CiEDG bit. When single-edge detection is selected, select the polarity using the CiEPO bit. The interrupt output can also be passed through the noise filter with four different sampling clocks. Set the COMPFIR.CiFCK[1:0] bits to 01b, 10b, or 11b to select the respective sampling clock. To use the ACMPLP0 interrupt request to release Software Standby mode and Snooze mode, set COMPFIR.CiFCK[1:0] to 00b to bypass the ACMPLP0 noise filter. The ACMPLP1 interrupt request cannot be used to release Software Standby mode or Snooze mode.

38.6 ELC Event Output

The ELC uses the ACMPLP interrupt request signal as an ELC event signal, enabling link operation for the preset module. The ELC event of ACMPLP can be used by selecting it in the ELSRn register in the ELC. When using ELC event request, set the COMPFIR.CiFCK[1:0] bits to 01b, 10b or 11b (otherwise no sampling).

38.7 Interrupt Handling and ELC Linking

ACMPLPi outputs event signals to the ELC to initiate operations of other modules selected in advance. In the same way as for the interrupt sources, the conditions for generation of the event signals output from ACMPLPi to the ELC can be selected as a single-edge detection or both-edge detection by setting the COMPFIR.CiEDG bit. When the single-edge detection is selected, the polarity can be selected in the CiEPO bit.

38.8 Comparator Pin Output

The comparison result from ACMPLPi can be output to external pins. The COMPOCR.CiOP and CiOE bits can be used to set the output polarity (non-inverted output or inverted output) and to output enable or disable. For the register settings and associated comparator output, see section 38.2.3, ACMPLP Output Control Register (COMPOCR).

To output the ACMPLP comparison result to the VCOUT output pin by the CPLOUTi, set the corresponding Port mn Pin Function Select Register (PmnPFS) in the I/O register.

38.9 Usage Notes

38.9.1 Settings for the Module-Stop State

The Module Stop Control Register can enable or disable the ACMPLP operation. The ACMPLP is initially stopped after a reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

38.9.2 Relationship with ADC14

There are restrictions on simultaneous use of ACMPLP analog input and A/D converter analog input. For details, see section 33.8.13, Relationship between the A/D converter, OPAMP, ACMPHS, and ACMPLP.

39. Capacitive Touch Sensing Unit (CTSU)

39.1 Overview

The Capacitive Touch Sensing Unit (CTSU) measures the electrostatic capacitance of the touch sensor. Changes in the electrostatic capacitance are determined by software that enables the CTSU to detect whether a finger is in contact with the touch sensor. The electrode surface of the touch sensor is usually enclosed with an electrical insulator so that fingers do not come into direct contact with the electrode.

As Figure 39.1 shows, electrostatic capacitance (parasitic capacitance) exists between the electrode and the surrounding insulators. Because the human body is an electrical conductor, when a finger is placed close to the electrode, the electrostatic capacitance increases.

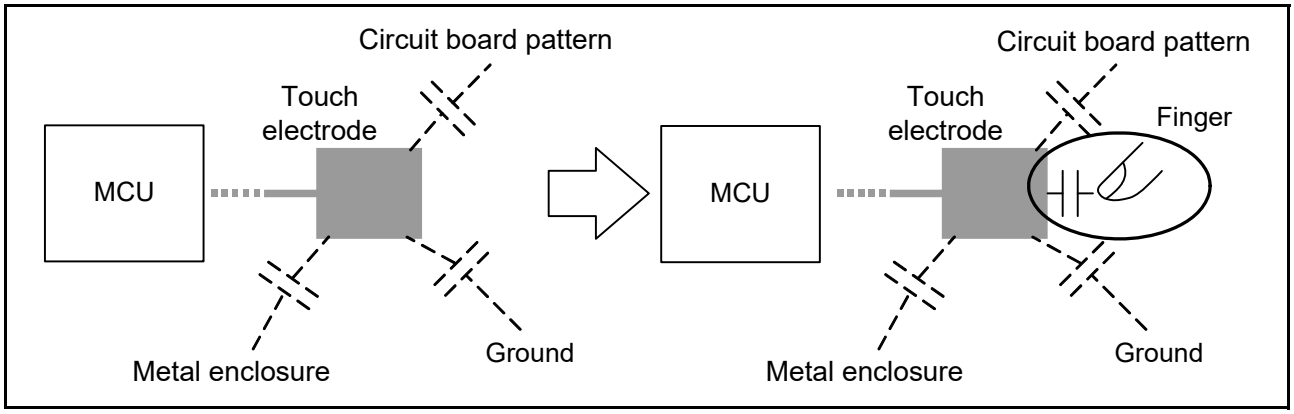


Figure 39.1 Increased electrostatic capacitance because of the presence of a finger

Electrostatic capacitance is detected by the self-capacitance and mutual capacitance methods. With self-capacitance, the CTSU detects electrostatic capacitance generated between a finger and a single electrode. With mutual capacitance, two electrodes are used as transmit and receive electrodes, and the CTSU detects the change in the electrostatic capacitance generated between the two when a finger is placed close to them.

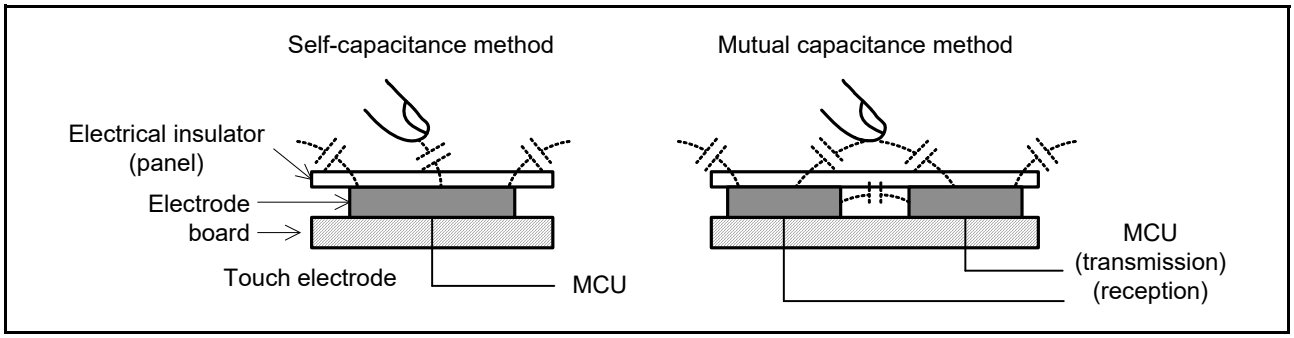


Figure 39.2 Self-capacitance and mutual capacitance methods

Electrostatic capacitance is measured by counting a clock signal whose frequency changes according to the amount of charged or discharged current, for a specified period. For details on the measurement principles of the CTSU, see section 39.3.1, Principles of Measurement Operation. Table 39.1 lists the CTSU specifications, and Figure 39.3 shows a block diagram.

Table 39.1 CTSU specifications (1 of 2)

Parameter		Description
Operating clocks		PCLKB, PCLKB/2, or PCLKB/4
Pins	Electrostatic capacitance measurement	28 channels (TS00 to TS22, TS25 to TS29)
	TSCAP	Low Pass Filter (LPF) connection pin

Table 39.1 CTSU specifications (2 of 2)

Parameter		Description
Measurement modes	Self-capacitance single scan mode	Electrostatic capacitance is measured on one channel using the self-capacitance method
	Self-capacitance multi-scan mode	Electrostatic capacitance is measured on multiple channels successively using the self-capacitance method
	Mutual capacitance full scan mode	Electrostatic capacitance is measured successively on multiple channels using the mutual capacitance method
Noise prevention		Synchronous noise prevention, high-pass noise prevention
Measurement start conditions		• Software trigger • External trigger (ELC_CTSU from the ELC)

As Figure 39.3 shows, the CTSU consists of the following components:

- Status control block
- Trigger control block
- Clock control block
- Channel control block
- Port control block
- Sensor drive pulse generator
- Measurement block
- Interrupt block
- I/O registers.

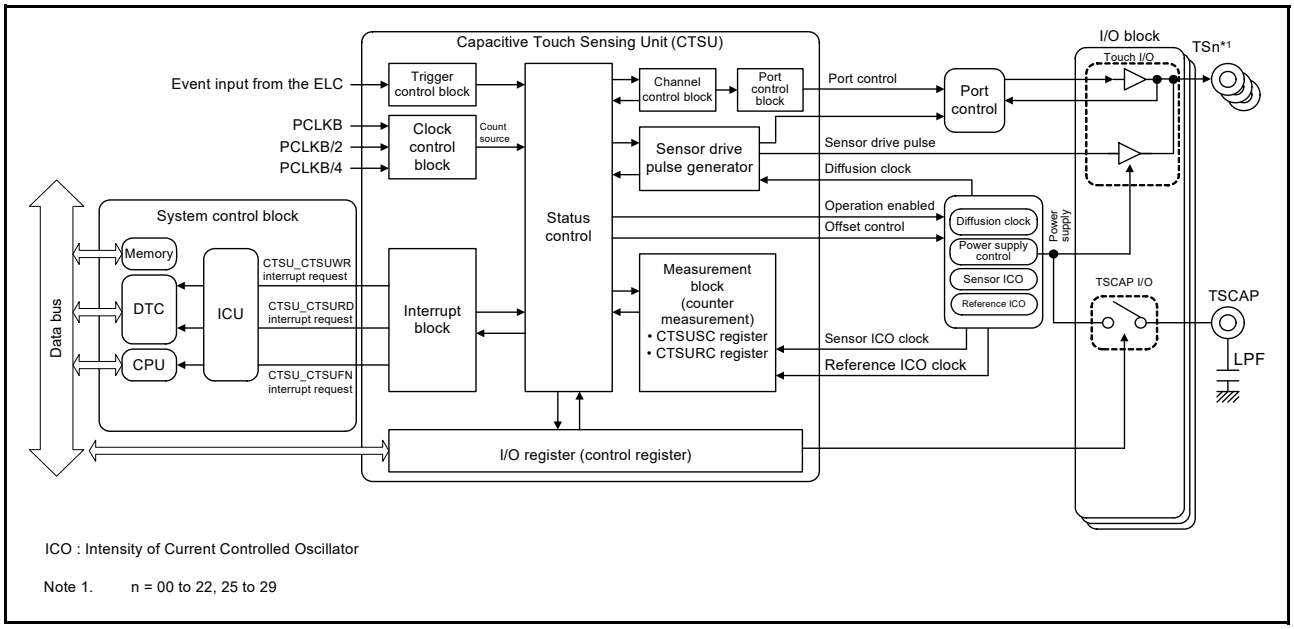


Figure 39.3 CTSU block diagram

Table 39.2 CTSU pin configuration

Pin name	I/O	Function
TS00 to TS22, TS25 to TS29	Input	Electrostatic capacitive measurement pins (touch pins)
TSCAP	—	LPF connection pin

39.2 Register Descriptions

39.2.1 CTSU Control Register 0 (CTSUCR0)

Address(es): CTSU.CTSUCR0 4008 1000h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	CTSUINIT	—	CTSUSNZ	CTSUCAP	CTSUSTRT
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CTSUSTRT	CTSU Measurement Operation Start	0: Stop measurement operation*1 1: Start measurement operation.	R/W
b1	CTSUCAP	CTSU Measurement Operation Start Trigger Select	0: Software trigger 1: External trigger.	R/W
b2	CTSUSNZ	CTSU Wait State Power-Saving Enable	0: Disable power-saving function during wait state 1: Enable power-saving function during wait state.	R/W
b3	—	Reserved	This bit read as 0. The write value should be 0.	R/W
b4	CTSUINIT	CTSU Control Block Initialization	Writing 1 to this bit initializes the CTSU control block and CTSUSC, CTSURC, CTSUMCH0, CTSUMCH1, and CTSUST registers. This bit is read as 0.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. When the CTSU is not used, set this bit to 0.

Only set the CTSUCAP and CTSUSNZ bits when the CTSUSTRT bit is 0. These bits can be set at the same time that measurement operation starts.

CTSUSTRT bit (CTSU Measurement Operation Start)

The CTSUSTRT bit specifies whether CTSU operation starts or stops.

When the CTSUCAP bit is 0, measurement starts when software writes 1 to the CTSUSTRT bit (software trigger) and stops when hardware clears the CTSUSTRT bit to 0. When the CTSUCAP bit is 1, the CTSU waits for an external trigger by writing 1 to the CTSUSTRT bit, and measurement starts on the rising edge of the external trigger. When measurement is stopped, the CTSU waits for the next external trigger and operation continues.

Table 39.3 lists the CTSU states.

Table 39.3 CTSU states

CTSUSTRT bit	CTSUCAP bit	CTSU state
0	0	Stopped
0	1	Stopped
1	0	Measurement in progress
1	1	Measurement in progress and waiting for an external trigger*1

Note 1. The state can be read from the CTSUST.CTSUSTC[2:0] flags as follows:
- During measurement: CTSUST.CTSUSTC[2:0] flags ≠ 000b
- While waiting for an external trigger: CTSUST.CTSUSTC[2:0] flags = 000b.

If software sets the CTSUSTRT bit to 1 when the bit is already 1, the write is ignored and operation continues. To force operation to stop through software when the CTSUSTRT bit is 1, set the CTSUSTRT bit to 0 and the CTSUINIT bit to 1 at the same time.

CTSUCAP bit (CTSU Measurement Operation Start Trigger Select)

The CTSUCAP bit specifies the measurement start condition. For details, see CTSUSTRT bit (CTSU Measurement Operation Start).

CTSUSNZ bit (CTSU Wait State Power-Saving Enable)

The CTSUSNZ bit enables or disables power-saving operation during a wait state. It can also suspend the CTSU power supply, which decreases power consumption during the wait state. In the suspended state, the CTSU power supply is turned off while the external TSCAP is still charged.

Table 39.4 shows the CTSU power supply state control.

Table 39.4 CTSU power supply state control

CTSUCR1.CTSUPON bit	CTSUSNZ bit	CTSUCAP bit	CTSUSTRT bit	CTSU power supply state
0	0	0	0	Stopped
1	0	—	—	Operating
1	1	0	0	Suspended

Note: Settings other than those listed in the table are prohibited.

To start measurement from the suspended state, set the CTSUSNZ bit to 0, and then set the CTSUSTRT bit to 1. To suspend the module after measurement stops, set the CTSUSNZ bit to 1.

CTSUINIT bit (CTSU Control Block Initialization)

Write 1 to the CTSUINIT bit to initialize the internal control registers. To force the current operation to stop, set the CTSUSTRT bit to 0 and the CTSUINIT bit to 1 at the same time. This stops the operation and initializes the internal control registers.

Do not write 1 to the CTSUINIT bit when the CTSUSTRT bit is 1.

39.2.2 CTSU Control Register 1 (CTSUCR1)

Address(es): CTSU.CTSUCR1 4008 1001h

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUMD[1:0]		CTSUCLK[1:0]		CTSUATUNE1	CTSUATUNE0	CTSUCSW	CTSUPON
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CTSUPON	CTSU Power Supply Enable	0: Power off the CTSU 1: Power on the CTSU.	R/W
b1	CTSUCSW	CTSU LPF Capacitance Charging Control	This bit controls charging of the LPF capacitance connected to the TSCAP pin. 0:Turn off capacitance switch 1: Turn on capacitance switch.	R/W
b2	CTSUATUNE0	CTSU Power Supply Operating Mode Setting	VCC ≥ 2.4 V: 0: Normal operating mode 1: Low-voltage operating mode. VCC < 2.4 V: 0: Setting prohibited 1: Low-voltage operating mode.	R/W
b3	CTSUATUNE1	CTSU Power Supply Capacity Adjustment	0: Normal output 1: High-current output.	R/W

Bit	Symbol	Bit name	Description	R/W
b5, b4	CTSUCLK[1:0]	CTSU Operating Clock Select	b5 b4 0 0: PCLKB 0 1: PCLKB/2 1 0: PCLKB/4 1 1: Setting prohibited.	R/W
b7, b6	CTSUMD[1:0]	CTSU Measurement Mode Select	b7 b6 0 0: Self-capacitance single scan mode 0 1: Self-capacitance multi-scan mode 1 0: Setting prohibited 1 1: Mutual capacitance full scan mode.	R/W

Only set the CTSUCR1 register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUPON bit (CTSU Power Supply Enable)

The CTSUPON bit controls the power supply to the CTSU. Set the CTSUPON and CTSUCSW bits to the same value.

CTSUCSW bit (CTSU LPF Capacitance Charging Control)

The CTSUCSW bit controls charging of the LPF capacitor connected to the TSCAP pin by turning the capacitance switch on or off.

After the capacitance switch is turned on, wait until the capacitance connected to the TSCAP pin is charged for the specified time before starting measurement by setting CTSUCR0.CTSUSTRT to 1. Before starting measurement, use an I/O port to output low to the TSCAP pin, and discharge the existing LPF capacitance. Set the CTSUPON and CTSUCSW bits to the same value.

CTSUATUNE0 bit (CTSU Power Supply Operating Mode Setting)

The CTSUATUNE0 bit sets the power supply operating mode. Set this bit according to the lower limit of VCC for operating the CTSU. For example, when using touch measurement in a system where VCC varies depending on the battery operation, set this bit to 1 regardless of the initial VCC voltage. The VCC voltage range is 2 to 3 V.

CTSUATUNE1 bit (CTSU Power Supply Capacity Adjustment)

The CTSUATUNE1 bit sets the capacity of the CTSU power supply. In general, a setting of 0 is recommended.

CTSUCLK[1:0] bits (CTSU Operating Clock Select)

The CTSUCLK[1:0] bits select the operating clock.

CTSUMD[1:0] bits (CTSU Measurement Mode Select)

The CTSUMD[1:0] bits set the measurement mode. For details, see section 39.3.2, Measurement Modes.

39.2.3 CTSU Synchronous Noise Reduction Setting Register (CTSUSDPRS)

Address(es): CTSU.CTSUSDPRS 4008 1002h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	CTSUSOFF	CTSUPRMODE[1:0]		CTSUPRRATIO[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	CTSUPRRATIO[3:0]	CTSU Measurement Time and Pulse Count Adjustment	These bits set the measurement time and measurement pulse count. The recommended setting is 3 (0011b).	R/W

Bit	Symbol	Bit name	Description	R/W
b5, b4	CTSUPRMODE [1:0]	CTSU Base Period and Pulse Count Setting	These bits set the base pulse count: b5 b4 0 0: 510 pulses 0 1: 126 pulses 1 0: 62 pulses (recommended setting) 1 1: Setting prohibited.	R/W
b6	CTSUSOFF	CTSU High-Pass Noise Reduction Function Off Setting	This bit controls spectrum diffusion, which can be used to reduce high-pass noise: 0: Turn spectrum diffusion on 1: Turn spectrum diffusion off.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Only set the CTSUSDPRS register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUPRRATIO[3:0] bits (CTSU Measurement Time and Pulse Count Adjustment)

The CTSUPRRATIO[3:0] bits set the measurement time and the number of measurement pulses using the following formulas, where the number of base pulses is determined by the CTSUPRMODE[1:0] setting:

Measurement pulse count = base pulse count × (CTSUPRRATIO[3:0] bits + 1)

Measurement time = (base pulse count × (CTSUPRRATIO[3:0] bits + 1) + base pulse count - 2) × 0.25 × base clock cycle

Note: For details on the base clock cycle, see section 39.2.19, CTSU Sensor Offset Register 1 (CTSUSO1).

CTSUPRMODE[1:0] bits (CTSU Base Period and Pulse Count Setting)

The CTSUPRMODE[1:0] bits select the number of base pulses that occur during measurement.

CTSUSOFF bit (CTSU High-Pass Noise Reduction Function Off Setting)

The CTSUSOFF bit turns on or off the function for reducing high-pass noise. Set this bit to 1 to turn the function off.

39.2.4 CTSU Sensor Stabilization Wait Control Register (CTSUSST)

Address(es): CTSU.CTSUSST 4008 1003h

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUSST[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	CTSUSST[7:0]	CTSU Sensor Stabilization Wait Control	Fix the value of these bits to 00010000b	R/W

Only set the CTSUSST register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUSST[7:0] bits (CTSU Sensor Stabilization Wait Control)

The CTSUSST[7:0] bits set the stabilization wait time for the TSCAP pin voltage. Always fix these bits to 00010000b. If these bits are not set, the TSCAP voltage is unstable at the start of measurement, and the CTSU is unable to produce the correct touch measurements.

39.2.5 CTSU Measurement Channel Register 0 (CTSUMCH0)

Address(es): CTSU.CTSUMCH0 4008 1004h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CTSUMCH0[5:0]					
Value after reset:	0	0	1	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b5 to b0	CTSUMCH0 [5:0]	CTSU Measurement Channel 0	In self-capacitance single scan mode, these bits set the channel to be measured: b5 b0 0 0 0 0 0 0: TS00 0 0 0 0 0 1: TS01 0 0 0 0 1 0: TS02 0 0 0 0 1 1: TS03 0 0 0 1 0 0: TS04 0 0 0 1 0 1: TS05 0 0 0 1 1 0: TS06 0 0 0 1 1 1: TS07 0 0 1 0 0 0: TS08 0 0 1 0 0 1: TS09 0 0 1 0 1 0: TS10 0 0 1 0 1 1: TS11 0 0 1 1 0 0: TS12 0 0 1 1 0 1: TS13 0 0 1 1 1 0: TS14 0 0 1 1 1 1: TS15 0 1 0 0 0 0: TS16 0 1 0 0 0 1: TS17 0 1 0 0 1 0: TS18 0 1 0 0 1 1: TS19 0 1 0 1 0 0: TS20 0 1 0 1 0 1: TS21 0 1 0 1 1 0: TS22 0 1 1 0 0 1: TS25 0 1 1 0 1 0: TS26 0 1 1 0 1 1: TS27 0 1 1 1 0 0: TS28 0 1 1 1 0 1: TS29. Other than when specified, starting measurement by setting CTSUCR0.CTSUSTRT to 1 is prohibited after these bits are set.	R/W*1

Bit	Symbol	Bit name	Description	R/W
			In other measurement modes, these bits indicate the channel that is currently being measured: b5 b0 0 0 0 0 0 0: TS00 0 0 0 0 0 1: TS01 0 0 0 0 1 0: TS02 0 0 0 0 1 1: TS03 0 0 0 1 0 0: TS04 0 0 0 1 0 1: TS05 0 0 0 1 1 0: TS06 0 0 0 1 1 1: TS07 0 0 1 0 0 0: TS08 0 0 1 0 0 1: TS09 0 0 1 0 1 0: TS10 0 0 1 0 1 1: TS11 0 0 1 1 0 0: TS12 0 0 1 1 0 1: TS13 0 0 1 1 1 0: TS14 0 0 1 1 1 1: TS15 0 1 0 0 0 0: TS16 0 1 0 0 0 1: TS17 0 1 0 0 1 0: TS18 0 1 0 0 1 1: TS19 0 1 0 1 0 0: TS20 0 1 0 1 0 1: TS21 0 1 0 1 1 0: TS22 0 1 1 0 0 1: TS25 0 1 1 0 1 0: TS26 0 1 1 0 1 1: TS27 0 1 1 1 0 0: TS28 0 1 1 1 0 1: TS29 1 1 1 1 1 1: Measurement is being stopped.	
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Writing to these bits is enabled only in self-capacitance single scan mode, when CTSUCR1.CTSUMD[1:0] = 00b.

Only set the CTSUMCH0 register when CTSUCR0.CTSUSTRT bit is 0.

CTSUMCH0[5:0] bits (CTSU Measurement Channel 0)

The CTSUMCH0[5:0] bits set the channel to be measured in self-capacitance single scan mode. In this mode, only specify enabled channels (000000b to 010110b, 011001b to 011101b). In all other modes, these bits indicate the receive channel that is being measured, and writing to these bits has no effect.

39.2.6 CTSU Measurement Channel Register 1 (CTSUMCH1)

Address(es): CTSU.CTSUMCH1 4008 1005h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CTSUMCH1[5:0]					
Value after reset:	0	0	1	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b5 to b0	CTSUMCH1[5:0]	CTSU Measurement Channel 1	b5 b0 0 0 0 0 0 0: TS00 0 0 0 0 0 1: TS01 0 0 0 0 1 0: TS02 0 0 0 0 1 1: TS03 0 0 0 1 0 0: TS04 0 0 0 1 0 1: TS05 0 0 0 1 1 0: TS06 0 0 0 1 1 1: TS07 0 0 1 0 0 0: TS08 0 0 1 0 0 1: TS09 0 0 1 0 1 0: TS10 0 0 1 0 1 1: TS11 0 0 1 1 0 0: TS12 0 0 1 1 0 1: TS13 0 0 1 1 1 0: TS14 0 0 1 1 1 1: TS15 0 1 0 0 0 0: TS16 0 1 0 0 0 1: TS17 0 1 0 0 1 0: TS18 0 1 0 0 1 1: TS19 0 1 0 1 0 0: TS20 0 1 0 1 0 1: TS21 0 1 0 1 1 0: TS22 0 1 1 0 0 1: TS25 0 1 1 0 1 0: TS26 0 1 1 0 1 1: TS27 0 1 1 1 0 0: TS28 0 1 1 1 0 1: TS29 1 1 1 1 1 1: Measurement is being stopped.	R
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CTSUMCH1[5:0] bits (CTSU Measurement Channel 1)

In full scan mode, the CTSUMCH1[5:0] bits indicate the transmit channel that is being measured. They are always 111111b when measurement is stopped, or in self-capacitance single scan and multi-scan modes.

39.2.7 CTSU Channel Enable Control Register 0 (CTSUCHAC0)

Address(es): CTSU.CTSUCHAC0 4008 1006h

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUCHAC0[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	CTSUCHAC0[7:0]	CTSU Channel Enable Control 0	These bits select whether the associated TS pin is measured: 0: Do not measure 1: Measure. These bits specify pins TS00 to TS07.	R/W

Only set the CTSUCHAC0 register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUCHAC0[7:0] bits (CTSU Channel Enable Control 0)

The CTSUCHAC0[7:0] bits select the receive and transmit pins whose electrostatic capacitance is to be measured. CTSUCHAC0[0] is associated with TS00 and CTSUCHAC0[7] with TS07.

39.2.8 CTSU Channel Enable Control Register 1 (CTSUCHAC1)

Address(es): CTSU.CTSUCHAC1 4008 1007h

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUCHAC1[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	CTSUCHAC1[7:0]	CTSU Channel Enable Control 1	These bits select whether the associated TS pin is measured: 0: Do not measure 1: Measure. These bits specify TS08 pins to TS15.	R/W

Only set the CTSUCHAC1 register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUCHAC1[7:0] bits (CTSU Channel Enable Control 1)

The CTSUCHAC1[7:0] bits select the receive and transmit pins whose electrostatic capacitance is to be measured. CTSUCHAC1[0] is associated with TS08 and CTSUCHAC1[7] with TS15.

39.2.9 CTSU Channel Enable Control Register 2 (CTSUCHAC2)

Address(es): CTSU.CTSUCHAC2 4008 1008h

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUCHAC2[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	CTSUCHAC2[7:0]	CTSU Channel Enable Control 2	These bits select whether the associated TS pin is measured: 0: Do not measure 1: Measure. These bits specify pins TS16 to TS22.	R/W

Note: The MCU does not support TS23 pin. Therefore, CTSUCHAC2[7]) is read as 0. The write value should be 0.

Only set the CTSUCHAC2 register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUCHAC2[7:0] bits (CTSU Channel Enable Control 2)

The CTSUCHAC2[7:0] bits select the receive and transmit pins whose electrostatic capacitance is to be measured. CTSUCHAC2[0] is associated with TS16 and CTSUCHAC2[6] with TS22.

39.2.10 CTSU Channel Enable Control Register 3 (CTSUCHAC3)

Address(es): CTSU.CTSUCHAC3 4008 1009h

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUCHAC3[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	CTSUCHAC3[7:0]	CTSU Channel Enable Control 3	These bits select whether the associated TS pin is measured: 0: Do not measure 1: Measure. These bits specify pins TS25 to TS29.	R/W

Note: The MCU does not support TS24, TS30 and TS31 pin. Therefore, CTSUCHAC3[0], CTSUCHAC3[6], and CTSUCHAC3[7]) are read as 0. The write value should be 0.

Only set the CTSUCHAC3 register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUCHAC3[7:0] bits (CTSU Channel Enable Control 3)

The CTSUCHAC3[7:0] bits select the receive and transmit pins whose electrostatic capacitance is to be measured. CTSUCHAC3[1] is associated with TS25 and CTSUCHAC3[5] with TS29.

39.2.11 CTSU Channel Transmit/Receive Control Register 0 (CTSUCHTRC0)

Address(es): CTSU.CTSUCHTRC0 4008 100Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUCHTRC0[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	CTSUCHTRC0[7:0]	CTSU Channel Transmit/Receive Control 0	0: Reception 1: Transmission. These bits specify pins TS00 to TS07.	R/W

Only set the CTSUCHTRC0 register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUCHTRC0[7:0] bits (CTSU Channel Transmit/Receive Control 0)

In full scan mode, the CTSUCHTRC0[7:0] bits assign the associated TS pins to reception or transmission. The setting is ignored in self-capacitance single scan and multi-scan modes. CTSUCHTRC0[0] is associated with TS00 and CTSUCHTRC0[7] with TS07.

39.2.12 CTSU Channel Transmit/Receive Control Register 1 (CTSUCHTRC1)

Address(es): CTSU.CTSUCHTRC1 4008 100Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUCHTRC1[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	CTSUCHTRC1[7:0]	CTSU Channel Transmit/Receive Control 1	0: Reception 1: Transmission. These bits specify the TS08 to TS15 pins.	R/W

Only set the CTSUCHTRC1 register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUCHTRC1[7:0] bits (CTSU Channel Transmit/Receive Control 1)

In full scan mode, the CTSUCHTRC1[7:0] bits assign the associated TS pins to reception or transmission. The setting is ignored in self-capacitance single scan and multi-scan modes. CTSUCHTRC1[0] is associated with TS08 and CTSUCHTRC1[7] with TS15.

39.2.13 CTSU Channel Transmit/Receive Control Register 2 (CTSUCHTRC2)

Address(es): CTSU.CTSUCHTRC2 4008 100Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUCHTRC2[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	CTSUCHTRC2[7:0]	CTSU Channel Transmit/Receive Control 2	0: Reception 1: Transmission. These bits specify the TS16 to TS22 pins.	R/W

Note: The MCU does not support the TS23 pin. Therefore, CTSUCHTRC2[7] is read as 0. The write value should be 0.

Only set the CTSUCHTRC2 register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUCHTRC2[7:0] bits (CTSU Channel Transmit/Receive Control 2)

In full scan mode, the CTSUCHTRC2[7:0] bits assign the associated TS pins to reception or transmission. The setting is ignored in self-capacitance single scan and multi-scan modes. CTSUCHTRC2[0] is associated with TS16 and CTSUCHTRC2[6] with TS22.

39.2.14 CTSU Channel Transmit/Receive Control Register 3 (CTSUCHTRC3)

Address(es): CTSU.CTSUCHTRC3 4008 100Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUCHTRC3[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	CTSUCHTRC3[7:0]	CTSU Channel Transmit/Receive Control 3	0: Reception 1: Transmission. These bits specify pins TS25 to TS29.	R/W

Note: The MCU does not support the TS24, TS30 and TS31 pins. Therefore, CTSUCHTRC3[0], CTSUCHTRC3[6], and CTSUCHTRC3[7]) are read as 0. The write value should be 0.

Only set the CTSUCHTRC3 register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUCHTRC3[7:0] bits (CTSU Channel Transmit/Receive Control 3)

In full scan mode, the CTSUCHTRC3[7:0] bits assign the associated TS pins to reception or transmission. The setting is ignored in self-capacitance single scan and multi-scan modes. CTSUCHTRC3[1] is associated with TS25 and CTSUCHTRC3[5] with TS29.

39.2.15 CTSU High-Pass Noise Reduction Control Register (CTSUDCLKC)

Address(es): CTSU.CTSUDCLKC 4008 1010h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CTSUSSCNT[1:0]		—	—	CTSUSSMOD[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	CTSUSSMOD[1:0]	CTSU Diffusion Clock Mode Select	These bits should be set to 00b	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5, b4	CTSUSSCNT[1:0]	CTSU Diffusion Clock Mode Control	These bits should be set to 11b	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Only set the CTSUDCLKC register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUSSMOD[1:0] bits (CTSU Diffusion Clock Mode Select)

The CTSUSSMOD[1:0] bits set the mode of the spectrum diffusion clock for high-pass noise reduction. When using the high-pass function, always fix these bits to 00b. If these bits are not set, the CTSU is unable to effectively reduce high-pass noise.

CTSUSSCNT[1:0] bits (CTSU Diffusion Clock Mode Control)

The CTSUSSCNT[1:0] bits adjust the amount of spectrum diffusion applied to reduce high-pass noise. When using the high-pass noise reduction function, always fix these bits to 11b. If these bits are not set, touch measurement might be performed incorrectly.

39.2.16 CTSU Status Register (CTSUST)

Address(es): CTSU.CTSUST 4008 1011h

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUPS	CTSUROVF	CTSUSOVF	CTSUDTSR	—	CTSUSTC[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	CTSUSTC[2:0]	CTSU Measurement Status Counter	These counters indicate the current measurement status: b2 b1 b0 0 0 0: Status 0 0 0 1: Status 1 0 1 0: Status 2 0 1 1: Status 3 1 0 0: Status 4 1 0 1: Status 5.	R
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	CTSUDTSR	CTSU Data Transfer Status Flag	This flag indicates whether the measurement result stored in the sensor counter and the reference counter was read: 0: Read 1: Not read.	R

Bit	Symbol	Bit name	Description	R/W
b5	CTSUSOVF	CTSU Sensor Counter Overflow Flag	This flag indicates an overflow on the sensor counter: 0: No overflow occurred 1: Overflow occurred.	R/W
b6	CTSUROVF	CTSU Reference Counter Overflow Flag	This flag indicates an overflow on the reference counter: 0: No overflow occurred 1: Overflow occurred.	R/W
b7	CTSUPS	CTSU Mutual Capacitance Status Flag	This flag indicates the measurement status in mutual capacitance full scan mode: 0: First measurement 1: Second measurement.	R

When using the CTSUCR0.CTSUINIT bit to clear an overflow flag, make sure that the CTSUCR0.CTSUSTRT bit is 0.

CTSUSTC[2:0] flags (CTSU Measurement Status Counter)

The CTSUSTC[2:0] flags are counters that indicate the current measurement status. For details on each status, see section 39.3.2.2, Status Counter.

CTSUDTSR flag (CTSU Data Transfer Status Flag)

The CTSUDTSR flag indicates whether the measurement result stored in the sensor counter and the reference counter was read. The flag is set to 1 when measurement completes and 0 when the reference counter is read by software or the DTC. The flag can also be cleared using the CTSUCR0.CTSUINIT bit.

CTSUSOVF flag (CTSU Sensor Counter Overflow Flag)

The CTSUSOVF flag is set to 1 when the sensor counter, CTSUSC, overflows. On overflow, the counter value reads as FFFFh. Measurement processing continues for the specified period.

No interrupt occurs on an overflow. To determine the channel on which the overflow occurred, read the measurement result of each channel after measurement completes, as signaled by a measurement end interrupt.

This flag is cleared when 0 is written after 1 is read by software. It can also be cleared using the CTSUCR0.CTSUINIT bit.

CTSUROVF flag (CTSU Reference Counter Overflow Flag)

The CTSUROVF flag is set to 1 when the reference counter, CTSURC, overflows. On overflow, the counter value reads as FFFFh. Measurement processing continues for the specified period.

No interrupt occurs on an overflow. To determine the channel on which the overflow occurred, read the measurement result of each channel after measurement completes, as signaled by a measurement end interrupt.

This flag is cleared when 0 is written after 1 is read by software. It can also be cleared using the CTSUCR0.CTSUINIT bit.

CTSUPS flag (CTSU Mutual Capacitance Status Flag)

In mutual capacitance full scan mode, when CTSUCR1.CTSUMD[1:0] = 11b, the CTSUPS flag indicates whether the measurement is the first or second of two measurements for each channel.

When measurement is stopped or in other measurement modes, the flag is always 0.

39.2.17 CTSU High-Pass Noise Reduction Spectrum Diffusion Control Register (CTSUSSC)

Address(es): CTSU.CTSUSSC 4008 1012h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	CTSUSSDIV[3:0]				—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b11 to b8	CTSUSSDIV[3:0]	CTSU Spectrum Diffusion Frequency Division Setting	These bits specify the spectrum diffusion frequency division setting based on the base clock frequency division setting	R/W
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CTSUSSDIV[3:0] bits (CTSU Spectrum Diffusion Frequency Division Setting)

The CTSUSSDIV[3:0] bits specify the spectrum diffusion frequency division setting, derived from the base clock frequency division setting. To calculate the correct setting for CTSUSSDIV[3:0], see the relationship between base clock frequencies and the settings in Table 39.5.

Table 39.5 Relationship between base clock frequencies and CTSUSSDIV[3:0] bit settings

Base clock frequency fb (MHz)	CTSUSSDIV[3:0] bit setting
4.00 ≤ fb	0000b
2.00 ≤ fb < 4.00	0001b
1.33 ≤ fb < 2.00	0010b
1.00 ≤ fb < 1.33	0011b
0.80 ≤ fb < 1.00	0100b
0.67 ≤ fb < 0.80	0101b
0.57 ≤ fb < 0.67	0110b
0.50 ≤ fb < 0.57	0111b
0.44 ≤ fb < 0.50	1000b
0.40 ≤ fb < 0.44	1001b
0.36 ≤ fb < 0.40	1010b
0.33 ≤ fb < 0.36	1011b
0.31 ≤ fb < 0.33	1100b
0.29 ≤ fb < 0.31	1101b
0.27 ≤ fb < 0.29	1110b
fb < 0.27	1111b

39.2.18 CTSU Sensor Offset Register 0 (CTSUSO0)

Address(es): CTSU.CTSUSO0 4008 1014h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUSNUM[5:0]						CTSUSO[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b9 to b0	CTSUSO[9:0]	CTSU Sensor Offset Adjustment	These bits adjust the electronic capacitance when the electrode is not being touched: b9 b0 0 0 0 0 0 0 0 0 0 0: Current offset is 0 0 0 0 0 0 0 0 0 0 1: Current offset is 1 0 0 0 0 0 0 0 0 1 0: Current offset is 2 : : 1 1 1 1 1 1 1 1 1 0: Current offset is 1022 1 1 1 1 1 1 1 1 1 1: Current offset is maximum.	R/W
b15 to b10	CTSUSNUM[5:0]	CTSU Measurement Count Setting	These bits set the number of measurements	R/W

CTSUSO[9:0] bits (CTSU Sensor Offset Adjustment)

The CTSUSO[9:0] bits offset the sensor ICO input current generated from electrostatic capacitance during touch measurement while the electrode is not being touched. This prevents the CTSU sensor counter from overflowing.

Set the TS pin that is to be measured next after a CTSU_CTSUWR interrupt occurs.

CTSUSNUM[5:0] bits (CTSU Measurement Count Setting)

The CTSUSNUM[5:0] bits set how many times the measurement pulse count specified in the CTSUSDPRS.CTSUPRRATIO[3:0] and CTSUSDPRS.CTSUPRMODE[1:0] bits is repeated during the measurement time. The measurement pulse count is repeated (CTSUSNUM[5:0] bits + 1) times.

Set the TS pin that is to be measured next after a CTSU_CTSUWR interrupt occurs.

39.2.19 CTSU Sensor Offset Register 1 (CTSUSO1)

Address(es): CTSU.CTSUSO1 4008 1016h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	CTSUICOG[1:0]		CTSUSDPA[4:0]					CTSURICOA[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	CTSURICOA[7:0]	CTSU Reference ICO Current Adjustment	These bits adjust the input current of the reference ICO. b7 b0 0 0 0 0 0 0 0 0: Current offset is 0 0 0 0 0 0 0 0 1: Current offset is 1 0 0 0 0 0 0 1 0: Current offset is 2 : : 1 1 1 1 1 1 1 0: Current offset is 254 1 1 1 1 1 1 1 1: Current offset is maximum.	R/W

Bit	Symbol	Bit name	Description	R/W
b12 to b8	CTSUSDPA[4:0]	CTSU Base Clock Setting	These bits generate the base clock: b12 b8 0 0 0 0 0: Operating clock divided by 2*1 0 0 0 0 1: Operating clock divided by 4 0 0 0 1 0: Operating clock divided by 6 0 0 0 1 1: Operating clock divided by 8 0 0 1 0 0: Operating clock divided by 10 0 0 1 0 1: Operating clock divided by 12 0 0 1 1 0: Operating clock divided by 14 0 0 1 1 1: Operating clock divided by 16 0 1 0 0 0: Operating clock divided by 18 0 1 0 0 1: Operating clock divided by 20 0 1 0 1 0: Operating clock divided by 22 0 1 0 1 1: Operating clock divided by 24 0 1 1 0 0: Operating clock divided by 26 0 1 1 0 1: Operating clock divided by 28 0 1 1 1 0: Operating clock divided by 30 0 1 1 1 1: Operating clock divided by 32 1 0 0 0 0: Operating clock divided by 34 1 0 0 0 1: Operating clock divided by 36 1 0 0 1 0: Operating clock divided by 38 1 0 0 1 1: Operating clock divided by 40 1 0 1 0 0: Operating clock divided by 42 1 0 1 0 1: Operating clock divided by 44 1 0 1 1 0: Operating clock divided by 46 1 0 1 1 1: Operating clock divided by 48 1 1 0 0 0: Operating clock divided by 50 1 1 0 0 1: Operating clock divided by 52 1 1 0 1 0: Operating clock divided by 54 1 1 0 1 1: Operating clock divided by 56 1 1 1 0 0: Operating clock divided by 58 1 1 1 0 1: Operating clock divided by 60 1 1 1 1 0: Operating clock divided by 62 1 1 1 1 1: Operating clock divided by 64.	R/W
b14, b13	CTSUICOG[1:0]	CTSU ICO Gain Adjustment	These bits adjust the output frequency gain of the sensor ICO and the reference ICO: b14 b13 0 0: 100% gain 0 1: 66% gain 1 0: 50% gain 1 1: 40% gain.	R/W
b15	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. Do not set the CTSUSDPA[4:0] bits to 00000b while the high-pass noise reduction function is turned off (CTSUSDPRS.CTSUSOFF = 1) in mutual capacitance full scan mode (CTSUCR1.CTSUMD[1:0] = 11b).

After a CTSU_CTSUWR interrupt occurs, write first to the CTSUSSC register, next to the CTSUSO0 register, and then to the CTSUSO1 register. The write to the CTSUSO1 register causes a transition to Status 3, see Table 39.6 and Table 39.7. Set all of the bits in a single operation when writing to the CTSUSO1 register.

CTSURICOA[7:0] bits (CTSU Reference ICO Current Adjustment)

The CTSURICOA[7:0] bits adjust the oscillation frequency using the input current of the reference ICO.

CTSUSDPA[4:0] bits (CTSU Base Clock Setting)

The CTSUSDPA[4:0] bits select the base clock used as the source for the sensor drive pulse by dividing the operating clock. For details on the setting procedure, see section 39.3.2.1, Initial Settings Flow.

CTSUICOG[1:0] bits (CTSU ICO Gain Adjustment)

The CTSUICOG[1:0] bits adjust the output frequency gain of the sensor ICO and the reference ICO. Normally, set these bits to 00b for the maximum gain. If changes in the capacitance between when the electrode is touched and when it is not touched greatly exceed the dynamic range of the sensor ICO, adjust the gain appropriately with this setting.

39.2.20 CTSU Sensor Counter (CTSUSC)

Address(es): CTSU.CTSUSC 4008 1018h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUSC[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	CTSUSC[15:0]	CTSU Sensor Counter	These bits indicate the measurement result of the sensor ICO. They read FFFFh when an overflow occurs.	R

After a CTSU_CTSURD interrupt occurs, read first from the CTSUSC counter then from the CTSURC counter.

CTSUSC[15:0] bits (CTSU Sensor Counter)

The CTSUSC[15:0] bits are configured as an increment counter for the sensor ICO.

Read these bits after a CTSU_CTSURD interrupt occurs. After the CTSURC counter is read, these bits are cleared immediately before the CTSU measurement status counter value changes to Status 4 (the CTSUST.CTSUSTC[2:0] flags change to 100b). They can also be cleared using the CTSUCR0.CTSUINIT bit.

39.2.21 CTSU Reference Counter (CTSURC)

Address(es): CTSU.CTSURC 4008 101Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CTSURC[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	CTSURC[15:0]	CTSU Reference Counter	These bits indicate the measurement result of the reference ICO. They read FFFFh when an overflow occurs.	R

After a CTSU_CTSURD interrupt occurs, read first from the CTSUSC counter then from the CTSURC counter. Status 3 continues until the CTSURC counter is read, even if the stabilization time specified for Status 3 elapses.

CTSURC[15:0] bits (CTSU Reference Counter)

The CTSURC[15:0] bits are configured as an increment counter for the reference ICO clock.

The reference ICO optimizes the touch measurement performed by the sensor ICO. There is some deviation depending on the internal sensor ICO and the reference ICO in the CTSU, but both ICOs have almost the same characteristics, including the dynamic range and the current-to-frequency characteristics. The range of current that can be set in the reference ICO current adjustment bits is about the same as the dynamic range of both ICOs, and the current input to the sensor ICO must be within this dynamic range. To ensure this, use the reference ICO to check the differences between the ICOs and measure the current-to-oscillation frequency characteristics. The reference ICO oscillation frequency can be obtained from the reference ICO counter, and the ICO oscillation frequency for the input current (counter value/ measurement time) can be measured by setting the value in the reference ICO current adjustment bits and measuring the reference ICO counter. The reference ICO counter value measured using the maximum value in the reference ICO current adjustment bits is the maximum value of the ICO dynamic range. The current to the sensor ICO needs to be offset in the offset adjustment bits so that the sensor ICO counter value does not exceed this value.

Read the CTSURC[15:0] bits after a CTSU_CTSURD interrupt occurs. After they read, they are cleared immediately before the CTSU measurement status counter value changes to Status 4 (the CTSUST.CTSUSTC[2:0] flags change to 100b). They can also be cleared using the CTSUCR0.CTSUINIT bit.

39.2.22 CTSU Error Status Register (CTSUERRS)

Address(es): CTSU.CTSUERRS 4008 101Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUICOMP	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b14 to b0	—	Reserved	These bits are read as 0	R
b15	CTSUICOMP	TSCAP Voltage Error Monitor	This bit monitors the error status of the TSCAP voltage: 0: Normal TSCAP voltage 1: Abnormal TSCAP voltage.	R

CTSUICOMP bit (TSCAP Voltage Error Monitor)

If the offset current amount set in the CTSUSO1 register exceeds the sensor ICO input current during touch measurement, the TSCAP voltage becomes abnormal and touch measurement cannot be correctly performed. The CTSUICOMP bit monitors the TSCAP voltage and is set to 1 if the voltage becomes abnormal. The sensor ICO counter value becomes undefined, but touch measurement completes normally, so it is difficult to detect an abnormality by reading the sensor ICO counter value. If the CTSU reference ICO current adjustment bits (CTSURICOA[7:0]) in the CTSUSO1 register are set to any value other than 0, always check this bit when touch measurement completes.

This bit is cleared by writing 0 to the CTSUCR1.CTSUPON bit and turning off the power supply.

39.3 Operation

39.3.1 Principles of Measurement Operation

Figure 39.4 shows the measurement circuit.

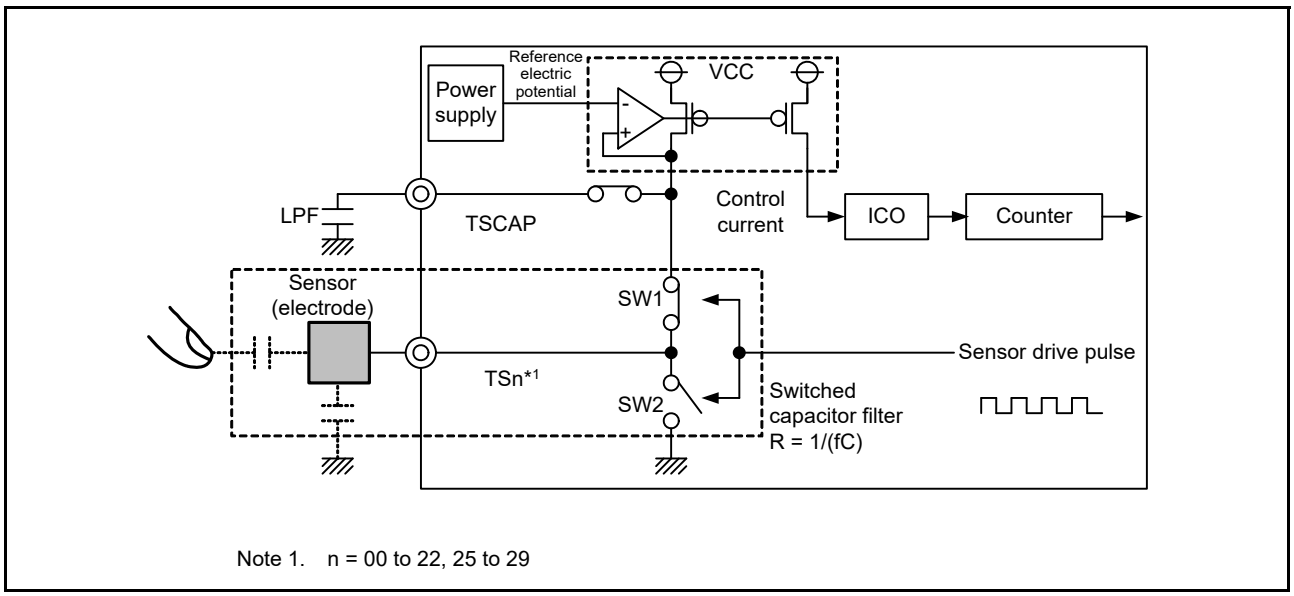


Figure 39.4 Measurement circuit

Figure 39.5 to Figure 39.7 explain the electrostatic capacitance measurement operation principles of the CTSU current frequency conversion. The operation is as follows:

1. The electrostatic capacitance of the electrode is charged by turning SW1 on and SW2 off. See Figure 39.5.
2. The charged capacitance is discharged by turning SW1 off and SW2 on. See Figure 39.6.

3. Current flows to the switched capacitor filter by repeatedly charging and discharging the electrodes as in steps 1. and 2. At this point, if a finger is in close proximity, the capacitance and the flowing current change. A clock is generated by supplying a control current that is proportional to the amount of the current flowing through the switched capacitor filter, from the circuit that generates the TSCAP power supply to the ICO. The counter measures the clock frequency that changes depending on whether a finger is in close proximity. Software uses the value read from the counter to determine contact with a finger. See Figure 39.7.

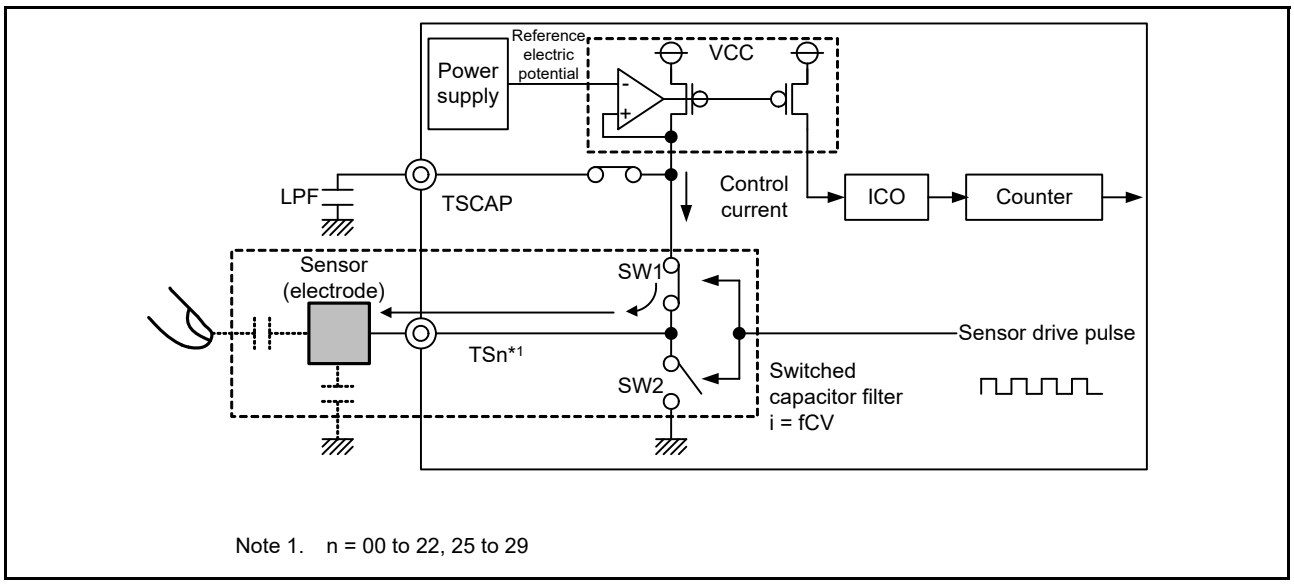


Figure 39.5 Charging operation

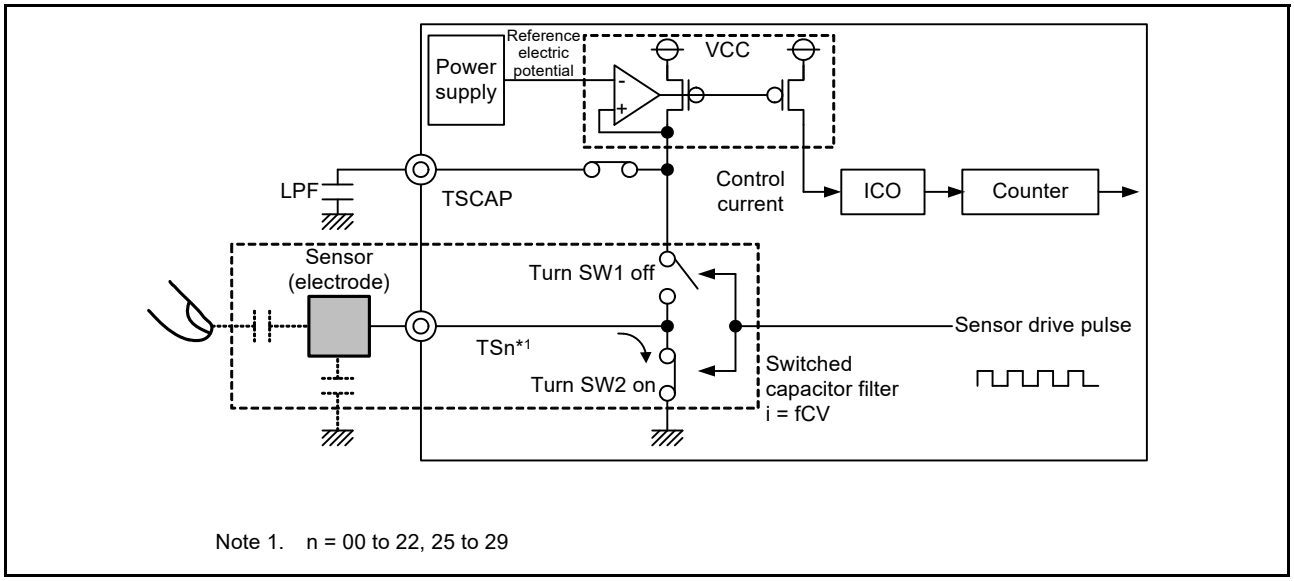


Figure 39.6 Discharging operation

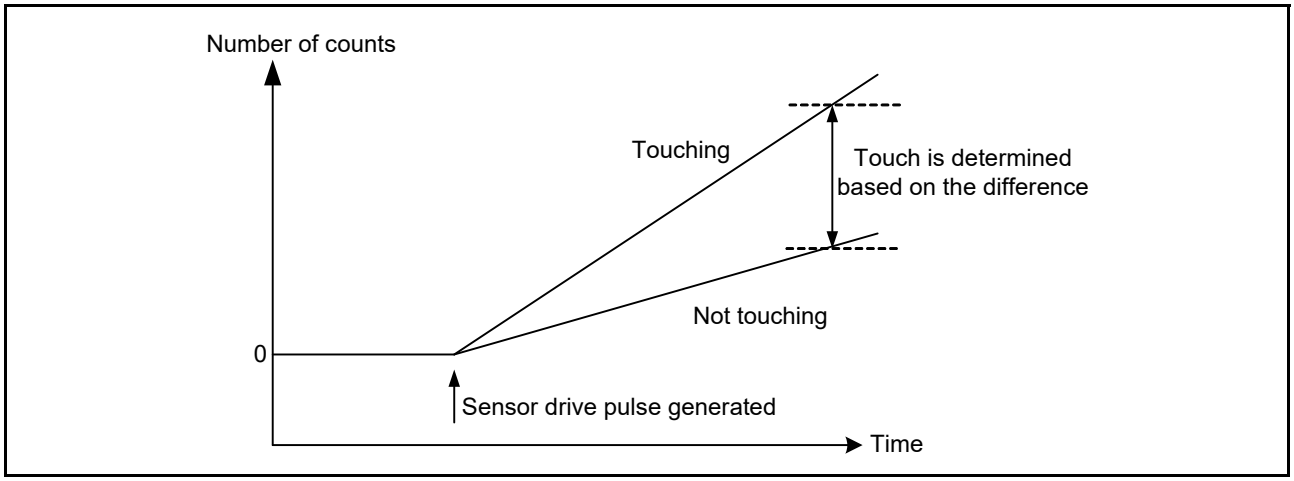


Figure 39.7 Change in measured value when finger is touching and not touching

39.3.2 Measurement Modes

The CTSU supports self-capacitance and mutual capacitance methods. Figure 39.8 shows these methods.

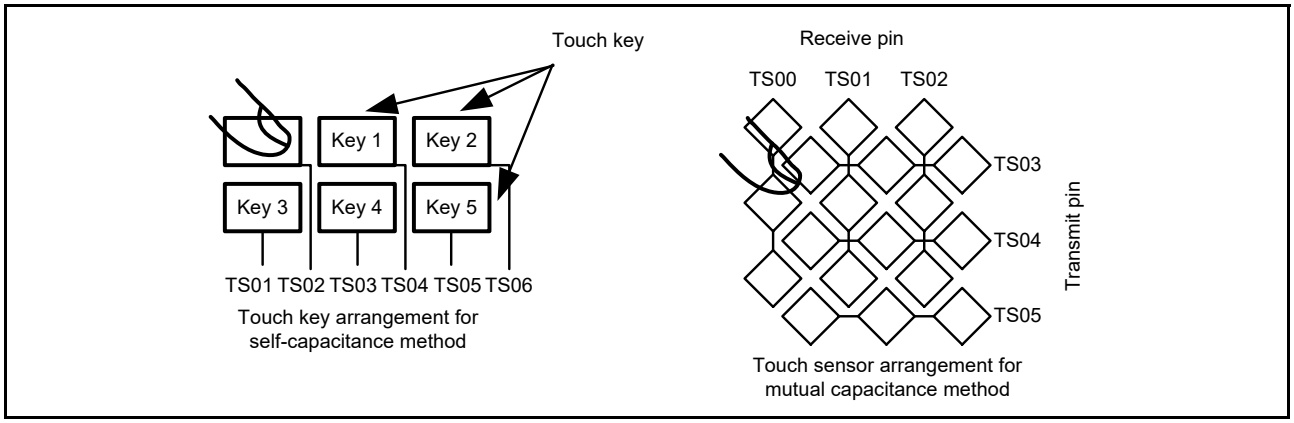


Figure 39.8 Overview of self-capacitance method and mutual capacitance method

In the self-capacitance method, a single touch pin is allocated to a single touch key to measure individual electrostatic capacitance when a finger is in close proximity. In this method, capacitance can be measured in both single scan and multi-scan modes.

In the mutual capacitance method, the capacitance between two opposing electrodes (transmit and receive pins) is measured.

39.3.2.1 Initial Settings Flow

Figure 39.9 shows the flow for the initial CTSU settings.

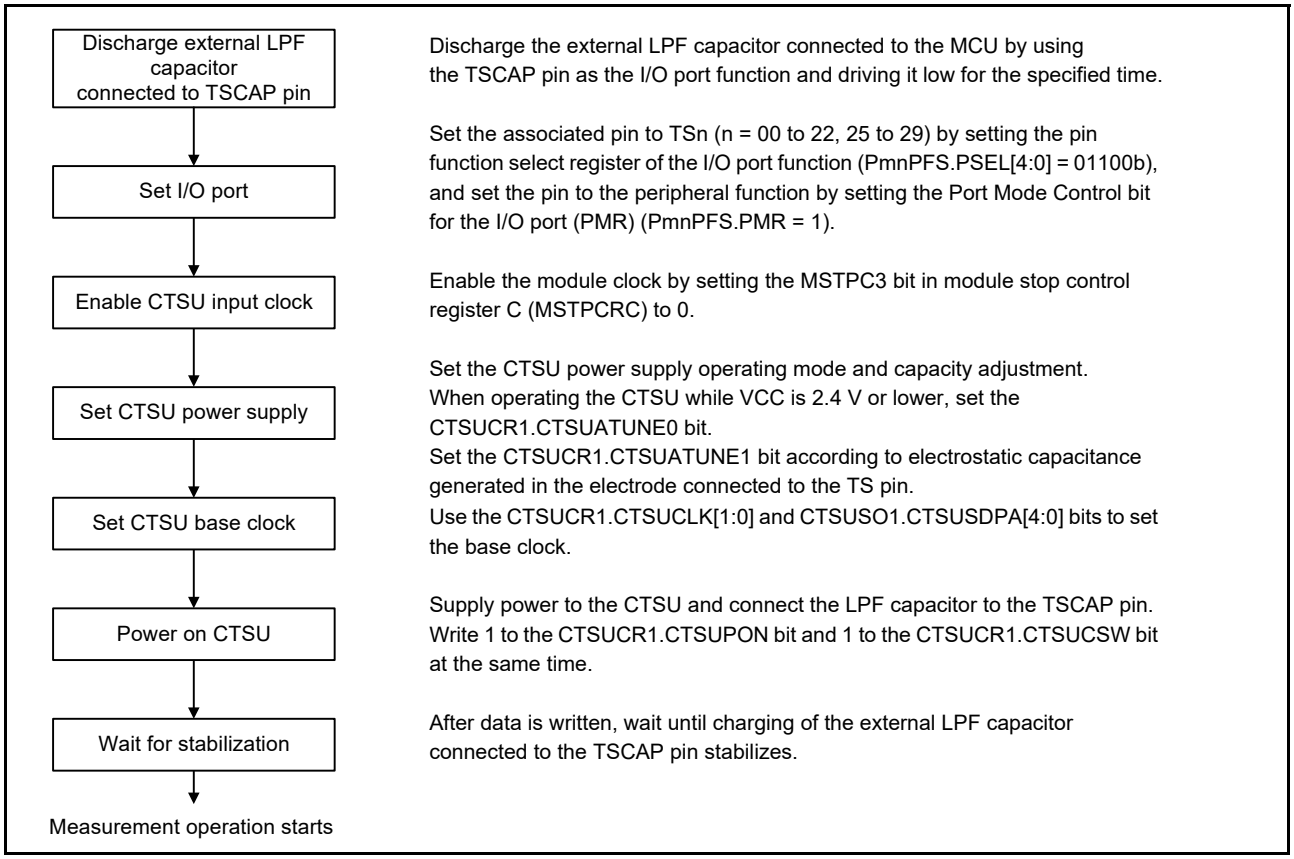


Figure 39.9 Initial CTSU settings flow

Figure 39.10 shows the flow for stopping CTSU operation and invoking the standby state.

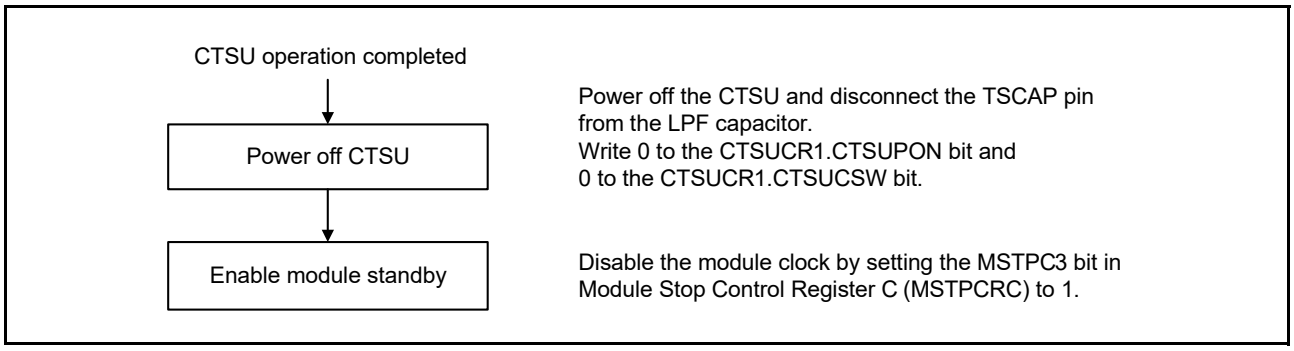


Figure 39.10 CTSU stopping flow

To restart operation, follow the initial setting flow shown in Figure 39.9.

39.3.2.2 Status Counter

The CTSU Status Register (CTSUST) indicates the current measurement status, which applies to all three modes. Figure 39.11 shows status operation transitions.

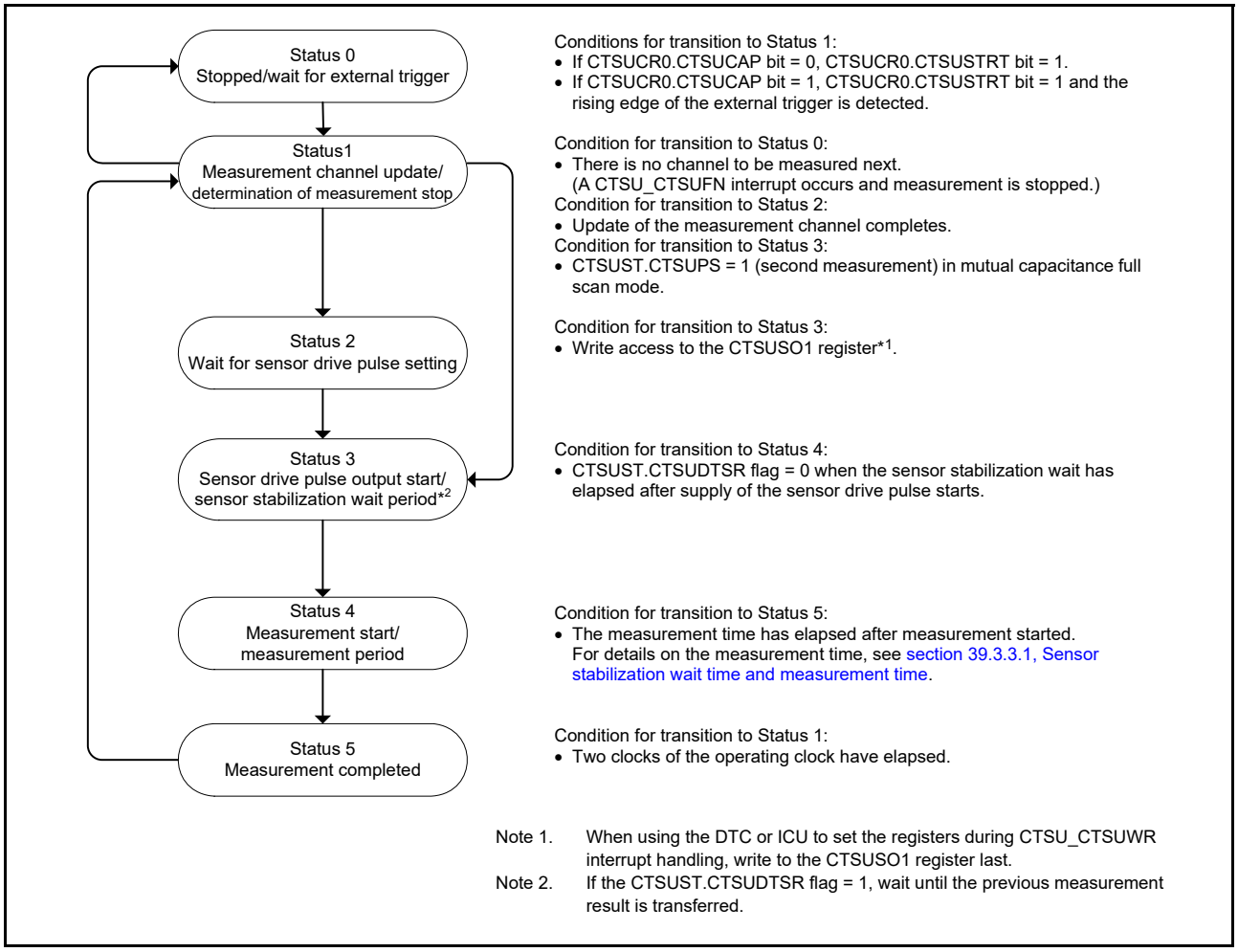


Figure 39.11 Status operation transitions

The status counter transitions to Status 0 when all of the specified measurement channels are measured.

The CTSUCR0.CTSUSTRT bit is set to 0 by hardware when a software trigger is used. When an external trigger is used, the value of 1 is retained, and the CTSU waits for the next trigger.

When operation is forced to stop during measurement or the trigger wait state, by a simultaneous 0 write to the CTSUCR0.CTSUSTRT bit and a 1 write to the CTSUCR0.CTSUINIT bit, the status transitions to Status 0 and measurement stops.

In the following cases, there is no channel to be measured:

- No target measurement channel is specified in the CTSUCHAC0 to CTSUCHAC3 registers
- In self-capacitance single scan mode, the channel specified in the CTSUMCH0 register is not a measurement target in the CTSUCHAC0 to CTSUCHAC3 registers
- In full scan modes, there is no transmit or receive channel to be measured based on the combined settings of the CTSUCHAC0 to CTSUCHAC3, and CTSUCHTRC0 to CTSUCHTRC3 registers.

If there is no channel to be measured based on these settings, a CTSU_CTSUFN interrupt occurs immediately after a transition to Status 1, and the counter transitions to Status 0.

39.3.2.3 Self-Capacitance Single Scan Mode Operation

In self-capacitance single scan mode, electrostatic capacitance is measured on one channel. Figure 39.12 shows the software flow and an operation example, and Figure 39.13 shows the timing.

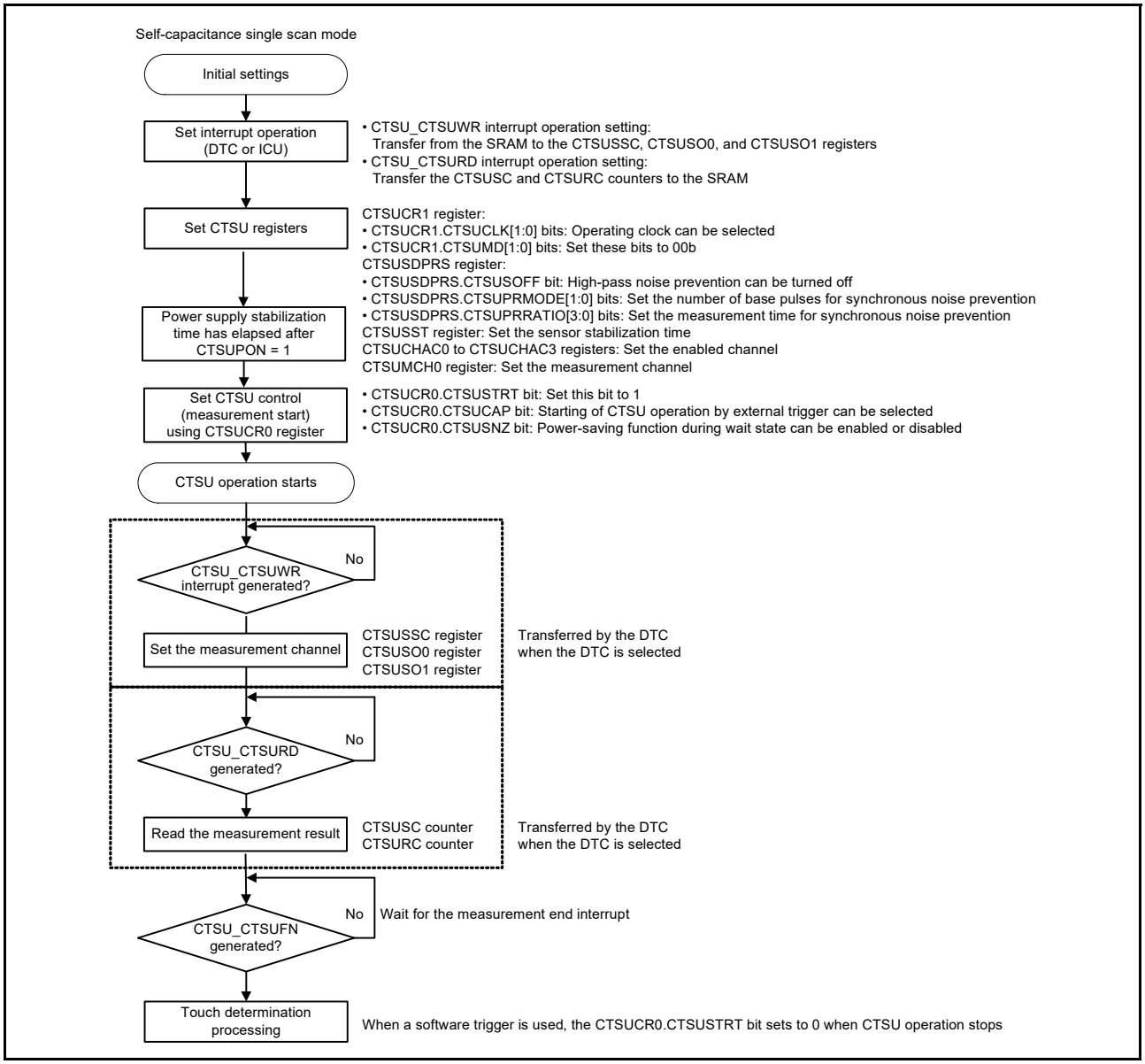


Figure 39.12 Software flow and operation example of self-capacitance single scan mode

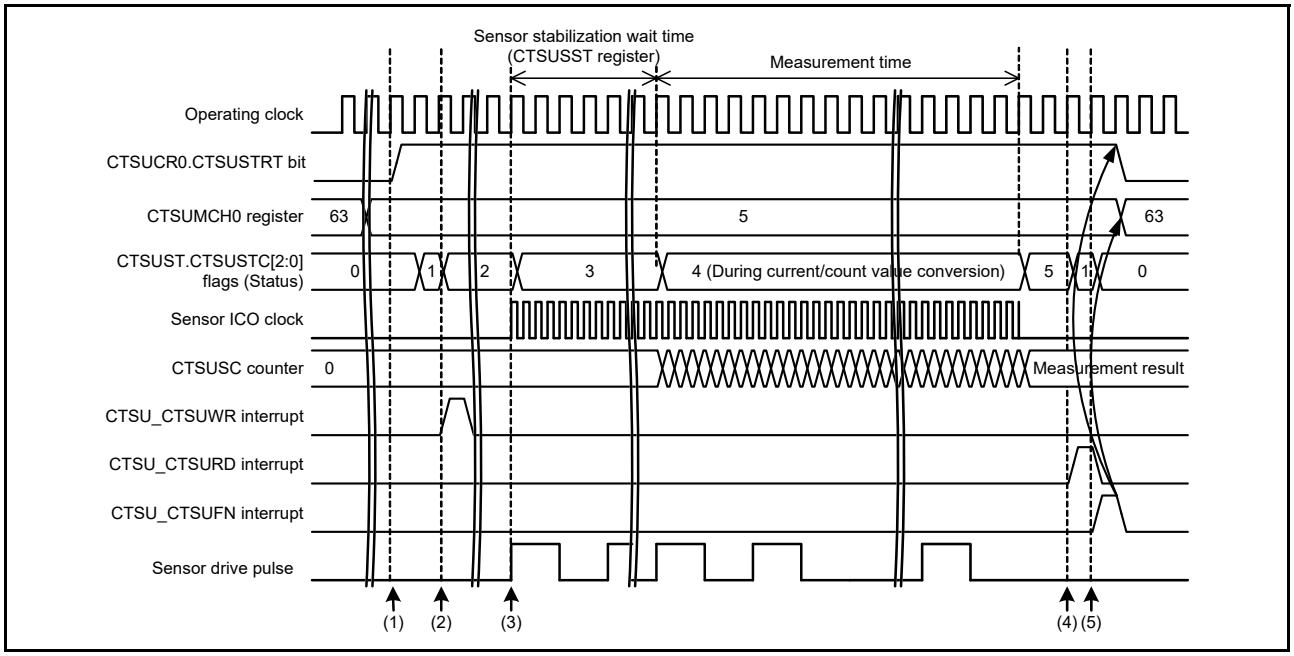


Figure 39.13 Timing of self-capacitance single scan mode when the measurement start condition is a software trigger

The following sequence describes the operation shown in Figure 39.13:

1. After initial settings are made, operation is started by writing 1 to the CTSUCR0.CTSUSTRT bit.
2. After the channel to be measured is determined according to the preset conditions, a request to set the associated channel (CTSU_CTSUWR) is output.
3. On completion of writing the measurement channel settings (CTSUSSC, CTSUSO0, and CTSUSO1 registers), the sensor drive pulse is output and the sensor ICO clock and the reference ICO clock operate.
4. After the sensor stabilization wait time and the measurement time have elapsed and measurement stops, a measurement result read request (CTSU_CTSURD) is output.
5. A measurement end interrupt (CTSU_CTSUFN) is output and measurement stops (transition to Status 0).

Table 39.6 lists the touch pin states in self-capacitance single scan mode.

Table 39.6 Touch pin states in self-capacitance single scan mode

	Touch pin	
Status	**Measured channel**	**Non-measured channel**
0	Low	Low
1	Low	Low
2	Low	Low
3	Pulse	Low
4	Pulse	Low
5	Low	Low

39.3.2.4 Self-Capacitance Multi-scan Mode Operation

In self-capacitance multi-scan mode, electrostatic capacitance on all channels that are specified as measurement targets in the CTSUCHAC0 to CTSUCHAC3 registers is measured sequentially in ascending order. Figure 39.14 shows the software flow and an operation example, and Figure 39.15 shows the timing.

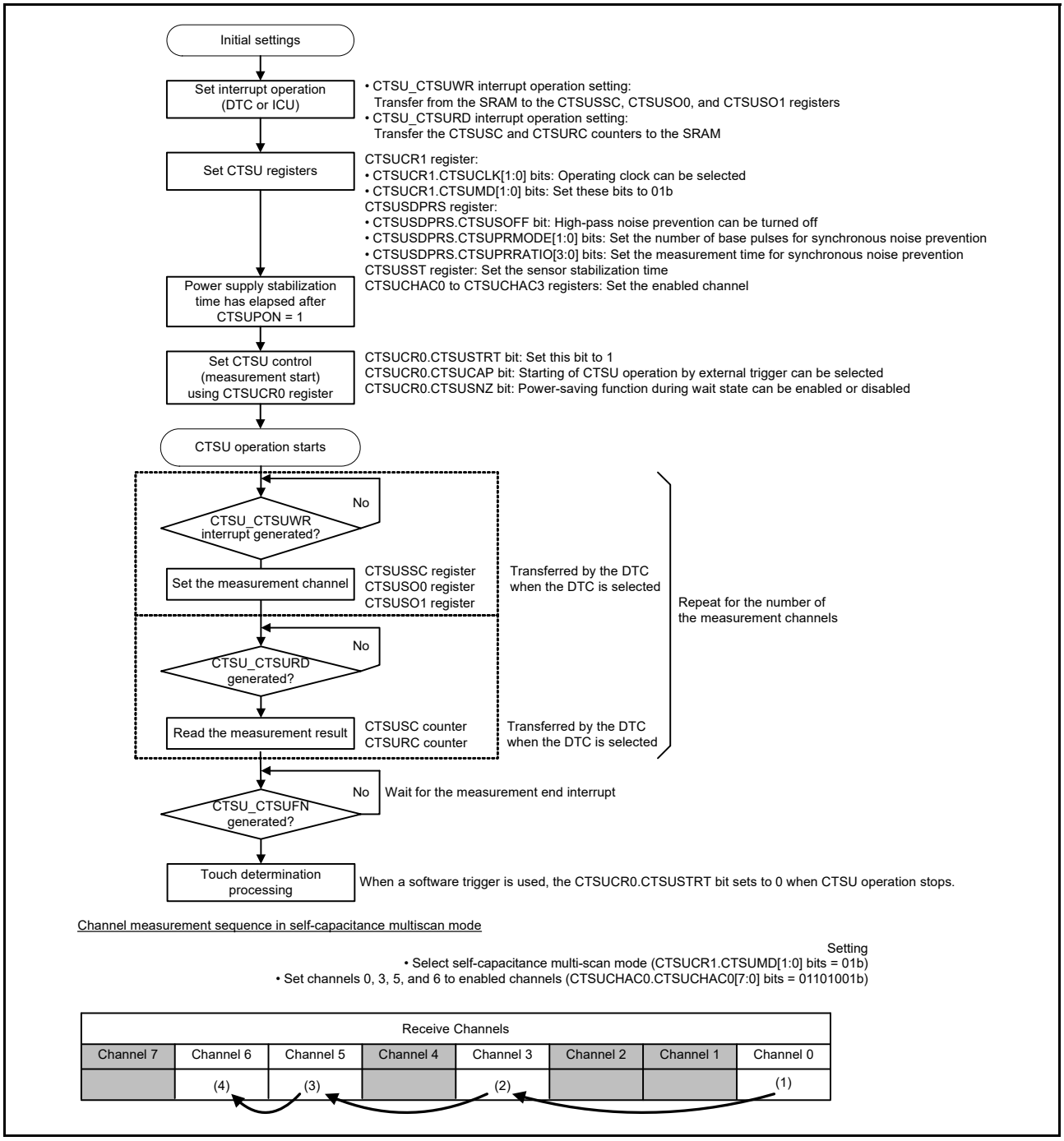


Figure 39.14 Software flow and operation example of self-capacitance multi-scan mode

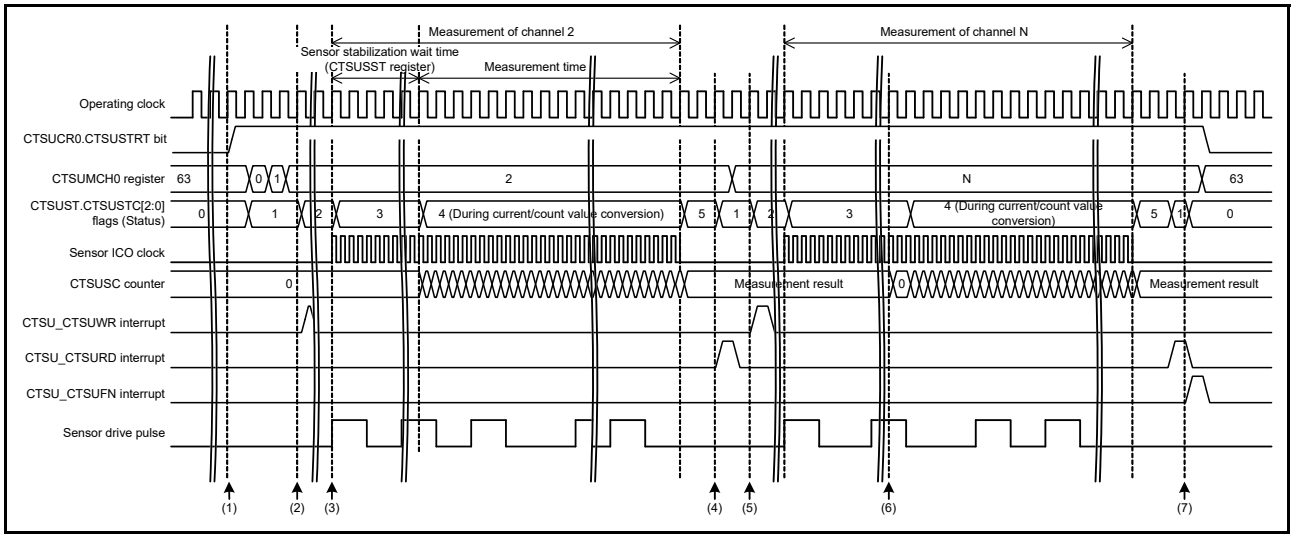


Figure 39.15 Timing of self-capacitance multi-scan mode when the measurement start condition is a software trigger

The following sequence describes the operation shown in Figure 39.15:

1. After initial settings are made, operation is started by writing 1 to the CTSUCR0.CTSUSTRT bit.
2. After the channel to be measured is determined according to the preset conditions, a request to set the associated channel (CTSU_CTSUWR) is output.
3. On completion of writing the measurement channel settings (CTSUSSC, CTSUSO0, and CTSUSO1 registers), the sensor drive pulse is output and the sensor ICO clock and the reference ICO clock operate.
4. After the sensor stabilization wait time and the measurement time have elapsed and measurement stops, a measurement result read request (CTSU_CTSURD) is output.
5. After the channel to be measured next is determined, a request to set the associated channel (CTSU_CTSUWR) is output.
6. After the stabilization wait time has elapsed and when the previous measurement is read, the result is cleared and measurement starts.
7. On completion of all channel measurements, a measurement end interrupt (CTSU_CTSUFN) is output and measurement stops (transition to Status 0).

Table 39.7 lists the touch pin states in self-capacitance multi-scan mode.

Table 39.7 Touch pin states in self-capacitance multi-scan mode

	Touch pin	
Status	**Measured channel**	**Non-measured channel**
0	Low	Low
1	Low	Low
2	Low	Low
3	Pulse	Low
4	Pulse	Low
5	Low	Low

39.3.2.5 Mutual Capacitance Full Scan Mode Operation

In mutual capacitance full scan mode, measurement is performed during the high-level period of the sensor drive pulse on the receive channel by applying the edge to the target transmit channel to be measured. A single measurement target is measured twice, on the rising and falling edges. The difference between the data of these two measurements determines

whether or not the electrode was touched. This creates higher touch sensitivity.

Electrostatic capacitance is measured sequentially on channels set to transmission or reception in the CTSUCHTRC0 to CTSUCHTRC3 registers and specified as measurement targets in the CTSUCHAC0 to CTSUCHAC3 registers. The capacitance is measured by combining these signals. Figure 39.16 shows the software flow and an operation example, and Figure 39.17 shows the timing.

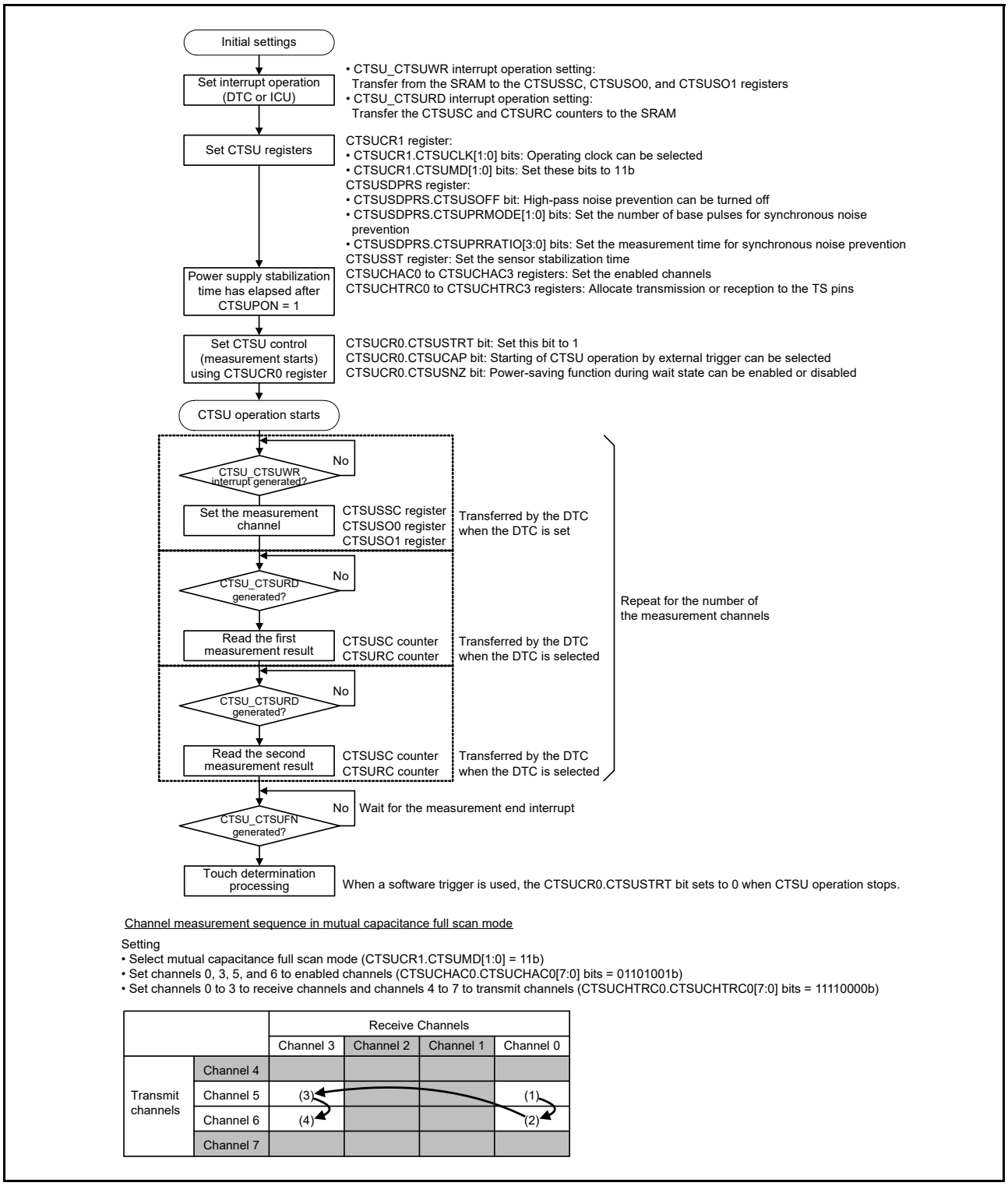


Figure 39.16 Software flow and operation example of mutual capacitance full scan mode

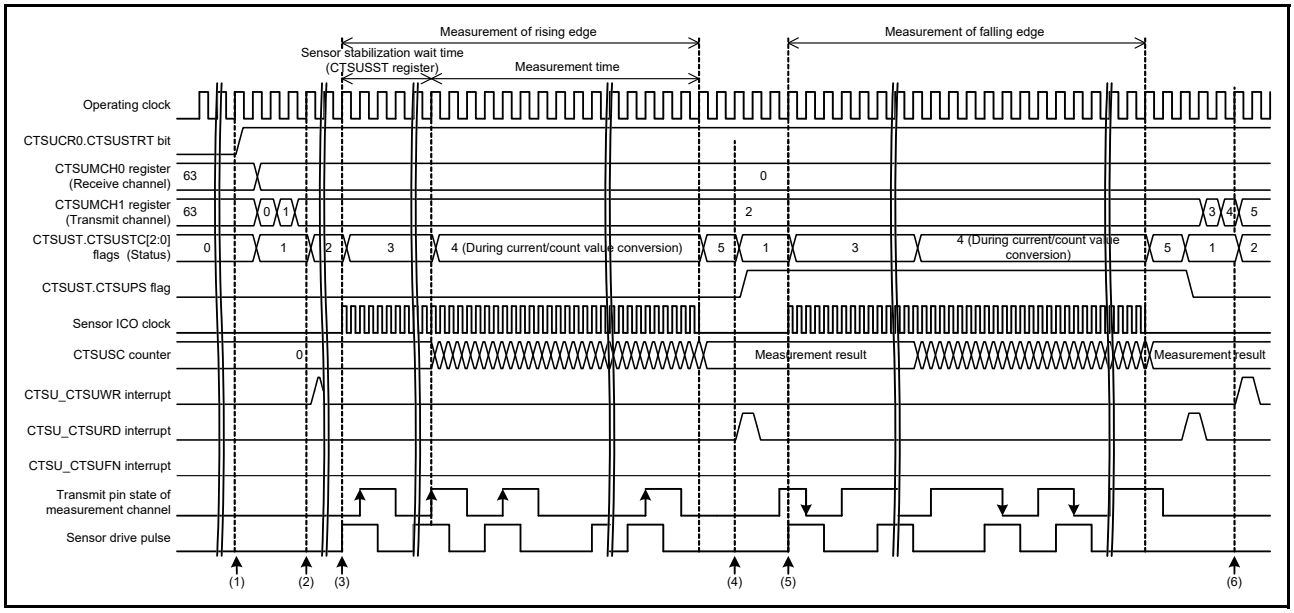


Figure 39.17 Timing of mutual capacitance full scan mode when the measurement start condition is a software trigger

The following sequence describes the operation shown in Figure 39.17:

1. After initial settings are made, operation is started by writing 1 to the CTSUCR0.CTSUSTRT bit.
2. After the channel to be measured is determined according to the preset conditions, a request to set the associated channel (CTSU_CTSUWR) is output.
3. On completion of writing the measurement channel settings (CTSUSSC, CTSUSO0, and CTSUSO1 registers), the sensor drive pulse is output and the sensor ICO clock and the reference ICO clock operate. At the same time, a pulse detected on the rising edge is output to the transmit pin on the measurement channel during the high-level period of the sensor drive pulse.
4. After the sensor stabilization wait time and the measurement time have elapsed and measurement stops, a measurement result read request (CTSU_CTSURD) is output.
5. The same channel is measured by outputting a pulse detected on the falling edge during the high-level period of the sensor drive pulse.
6. After the same channel is measured twice, the channel to be measured next is determined and measured in the same way.
7. On completion of all channel measurements, a measurement end interrupt (CTSU_CTSUFN) is output and measurement stops (transition to Status 0).

The CTSU Mutual Capacitance Status flag (CTSUST.CTSUPS bit) changes when Status 5 transitions to Status 1.

Table 39.8 lists the touch pin states in mutual capacitance full scan mode.

Table 39.8 Touch pin states in mutual capacitance full scan mode (1 of 2)

Status	Touch pins for receive channels		Touch pins for transmit channels		Remarks
	Measured channels	Non-measured channels	Measured channels	Non-measured channel	
0	Low	Low	Low	Low	-
1	Low	Low	Low/high	Low	-
2	Low	Low	Low	Low	-
3	Pulse	Low	Pulse	Low	The transmit pulse phase is the same as that of the receive channel on the first measurement and opposite on the second measurement

Table 39.8 Touch pin states in mutual capacitance full scan mode (2 of 2)

Status	Touch pins for receive channels		Touch pins for transmit channels		Remarks
	Measured channels	Non-measured channels	Measured channels	Non-measured channel	
4	Pulse	Low	Pulse	Low	-
5	Low	Low	Low	Low	-

39.3.3 Functions Common to Multiple Modes

39.3.3.1 Sensor stabilization wait time and measurement time

Figure 39.18 shows the timing of the sensor stabilization wait and measurement.

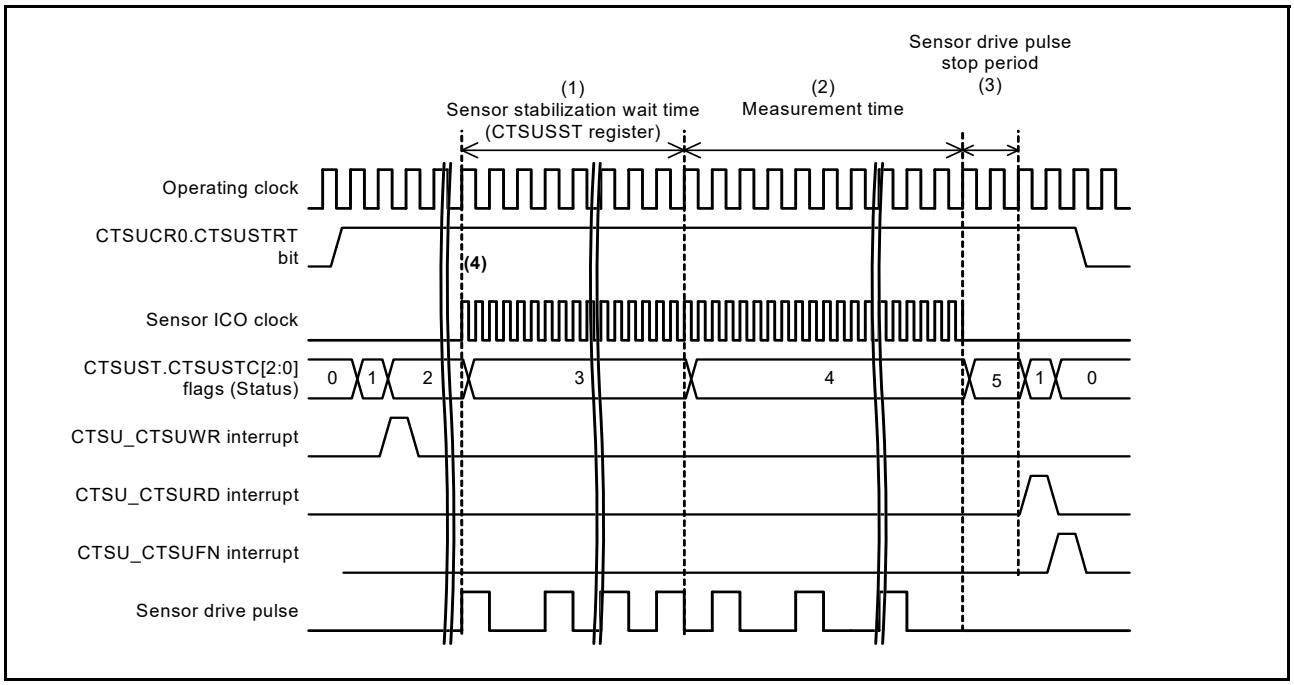


Figure 39.18 Sensor stabilization wait and measurement timing

The following sequence describes the operation shown in Figure 39.18:

1. In response to the CTSU_CTSUWR interrupt request, output of the sensor drive pulse is started by a write access to the CTSUSO1 register. The CTSU waits for the stabilization time set in the CTSUSST register.
2. When the sensor stabilization time has elapsed and the CTSUST.CTSUDTSR flag is set to 0, measurement starts on transition to Status 4. The measurement time is determined by the base clock cycle setting and the CTSUSDPRS.CTSUPRMODE[1:0], CTSUPRRATIO[3:0], and CTSUSO0.CTSUSNUM[5:0] bits. When the measurement time has elapsed, measurement of the associated channel stops.
3. After the measurement time elapses, the status transitions to Status 1 after 2 operating clock cycles and a CTSU_CTSURD interrupt occurs. Read the data from the CTSUSC and CTSURC counters. The sensor drive pulse is output at the low level. When measurement of all specified channels completes, the CTSUCR0.CTSUSTRT bit is set to 0.
4. The sensor ICO clock oscillates while the CTSUST.CTSUSTC[2:0] flags = 011b (Status 3) or 100b (Status 4).

39.3.3.2 Interrupts

The CTSU supports three interrupt sources:

- Write request interrupt for setting registers for each channel (CTSU_CTSUWR)
- Measurement data transfer request interrupt (CTSU_CTSURD)

- Measurement end interrupt (CTSU_CTSUFN).

(1) Write request interrupt for setting registers for each channel (CTSU_CTSUWR)

Store the settings for each measurement channel in the SRAM, and set up the DTC or ICU transfer associated with the CTSU_CTSUWR interrupt in advance. The CTSU_CTSUWR interrupt is output when Status 1 transitions to Status 2. Write the channel settings from the SRAM to the associated CTSUSSC, CTSUSO0, and CTSUSO1 registers (Figure 39.19). Because write access to the CTSUSO1 register controls a transition to the next status, be sure to set this register last.

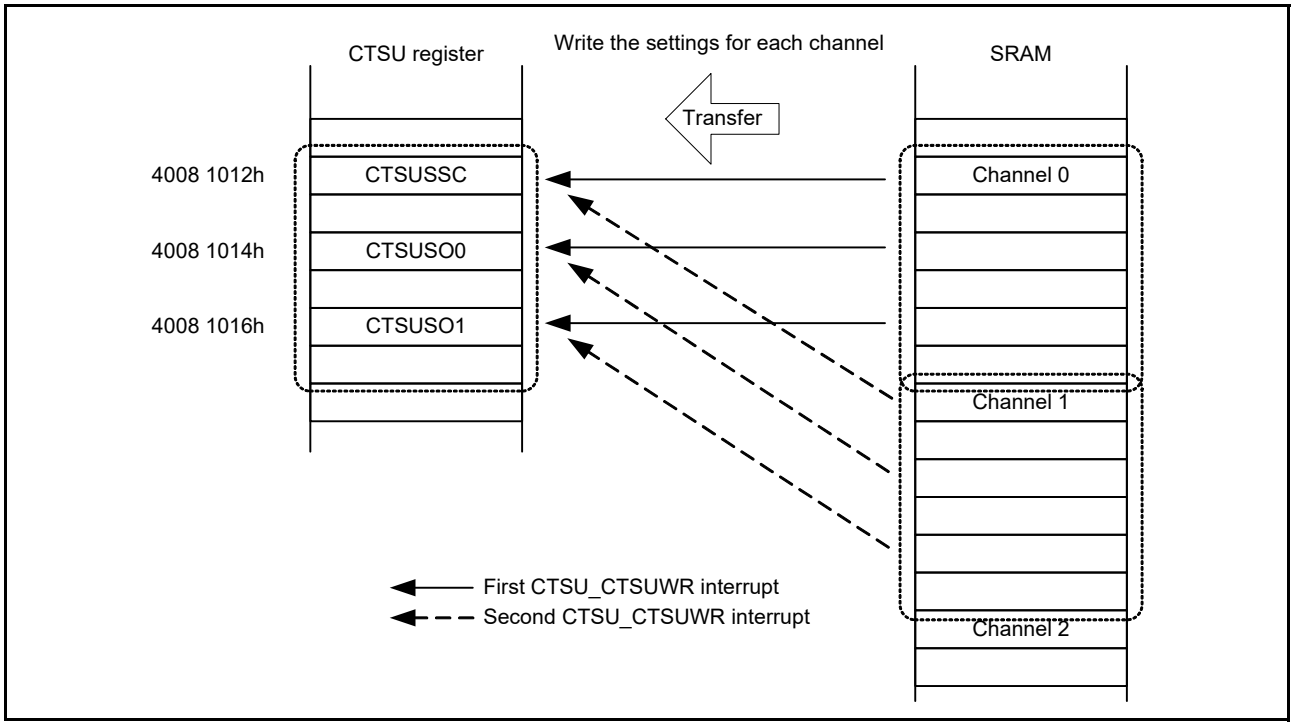


Figure 39.19 Example DTC transfer operation using the CTSU_CTSUWR interrupt

The registers to be set (CTSUSSC, CTSUSO0, and CTSUSO1) are allocated at sequential addresses. On CTSU_CTSUWR interrupt generation, set up the operation as follows:

- Transfer destination address: CTSUSSC register address
- Handling at the transfer destination address: Transfer 2-byte data three times for a single interrupt. The address of the start byte is fixed.
- Transfer source address: CTSUSSC register data storage address for the lowest number channel in the settings stored in the SRAM
- Handling at the transfer source address: Transfer 2-byte data three times for a single interrupt. The address of the first byte is continued from the previous interrupt handling.
- Number of transfers per interrupt: Specify the number of measurements.

(2) Measurement data transfer request interrupt (CTSU_CTSURD)

Set up the DTC or ICU transfer associated with the CTSU_CTSURD interrupt in advance. The CTSU_CTSURD interrupt is output when Status 5 transitions to Status 1. Read the measurement results from the CTSUSC and CTSURC counters (Figure 39.20).

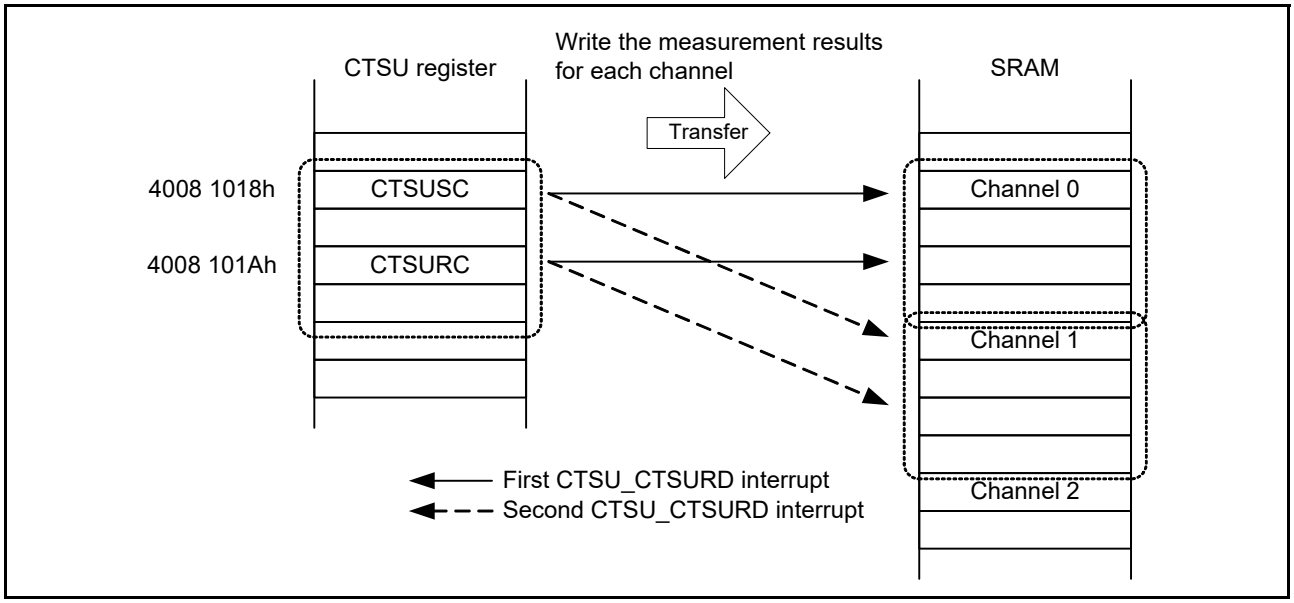


Figure 39.20 Example DTC transfer operation using the CTSU_CTSURD interrupt

The measurement result registers, CTSUSC and CTSURC counters, used as transfer sources are allocated at sequential addresses. On CTSU_CTSURD interrupt generation, set up the operation as follows:

- Transfer source address: CTSUSC counter address
- Handling at the transfer source address: Transfer 2-byte data twice for a single interrupt. The start address is fixed.
- Transfer destination address: CTSUSC counter data storage address for the lowest number channel in the settings stored in the SRAM
- Handling at the transfer destination address: Transfer 2-byte data twice for a single interrupt. The start address continues from the previous interrupt handling.
- Number of transfers per interrupt: Specify the number of measurements.

(3) Measurement end interrupt (CTSU_CTSUFN)

After all channels are measured, an interrupt occurs when Status 1 transitions to Status 0. In the software, check the overflow flags (CTSUST.CTSUSOVF and CTSUROVF) and read the measurement results to determine whether the electrode was touched. Interrupt requests are accepted or disabled in the interrupt control block.

39.4 Usage Notes

39.4.1 Measurement Result Data (CTSUSC and CTSURC Counters)

Read access during measurement is prohibited. If the measurement result data is accessed, an incorrect value might be read because of an asynchronous operation.

39.4.2 Software Trigger

When 10b (PCLKB/4) is selected in the CTSUCR1.CTSUCLK[1:0] bits, to restart measurement by writing 1 to the CTSUCR0.CTSUSTRT bit after measurement is complete, wait for at least 3 cycles to elapse after an interrupt occurs, and then write to the CTSUCR0.CTSUSTRT bit.

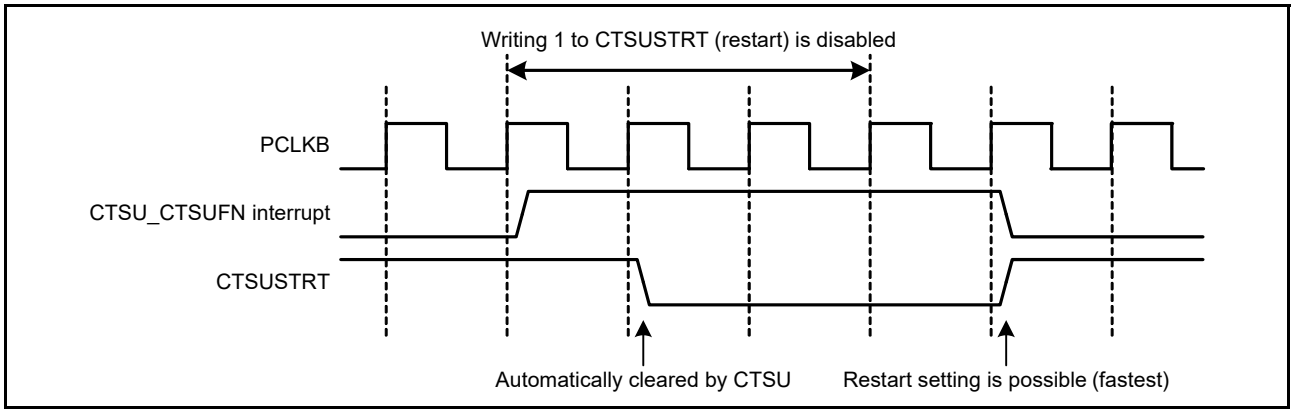


Figure 39.21 Notes on restarting measurement

39.4.3 External Trigger

- If an external trigger is input during the measurement time, measurement does not start. The next external event is enabled after 1 cycle of the operating clock when a CTSU_CTSUFN interrupt occurs.
- To stop external trigger mode, write 0 to the CTSUCR0.CTSUSTRT bit and 0 to the CTSUCR0.CTSUINIT bit at the same time (forced stop).

39.4.4 Notes on Forcing Operation Stop

To force the current operation to stop, write 0 to the CTSUCR0.CTSUSTRT bit and 1 to the CTSUCR0.CTSUINIT bit at the same time. After this setting, the operation is stopped and the internal control registers are initialized.

When the CTSUCR0.CTSUINIT bit is used for initialization, the following registers are initialized in addition to the internal measurement state:

- CTSUMCH0 register
- CTSUMCH1 register
- CTSUST register
- CTSUSC counter
- CTSURC counter.

If operation is forced to stop, an interrupt request might be generated depending on the internal state. After a forced stop, perform the processing for stopping or disabling the DTC or ICU. If a DTC transfer is stopped in an installed system for some reason, also perform the processing to force the stop and to initialize the CTSU.

39.4.5 TSCAP Pin

The TSCAP pin requires an external decoupling capacitor to stabilize the CTSU internal voltage. The traces between the TSCAP pin and the capacitor, and the capacitor and ground should be as short and wide as physically possible.

The capacitor connected to the TSCAP pin should be fully discharged using I/O port control to output low before turning on the switch (CTSUCR1.CTSUCSW bit = 1) to establish a connection.

39.4.6 Notes on Measurement Operation (CTSUCR0.CTSUSTRT Bit = 1)

During measurement (CTSUCR0.CTSUSTRT bit = 1), do not use the settings for stopping the peripheral clock or changing the port settings related to the touch pins (TSn and TSCAP) that are available in the higher layers of the system.

If control settings non-compliant with this constraint are made, after operation is forced to stop (CTSUCR0.CTSUSTRT bit = 0 and CTSUCR0.CTSUINIT bit = 1), write 0 to the CTSUCR1.CTSUPON bit and 0 to the CTSUCR1.CTSUCSW bit at the same time, and set the CTSUCR0.CTSUSNZ bit to 0. Next, restart from the initial settings flow shown in Figure 39.9.

40. Data Operation Circuit (DOC)

40.1 Overview

The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. An interrupt can be generated when a selected condition applies. Table 40.1 lists the DOC specifications and Figure 40.1 shows a block diagram.

Table 40.1 DOC specifications

Parameter	Description
Data operation function	16-bit data comparison, addition, and subtraction
Module-stop function	The module-stop state can be set
Interrupts and event link function (DOC_DOPCI)	An interrupt occurs on the following conditions: • The compared values either match or mismatch • The result of data addition is greater than FFFFh • The result of data subtraction is less than 0000h.

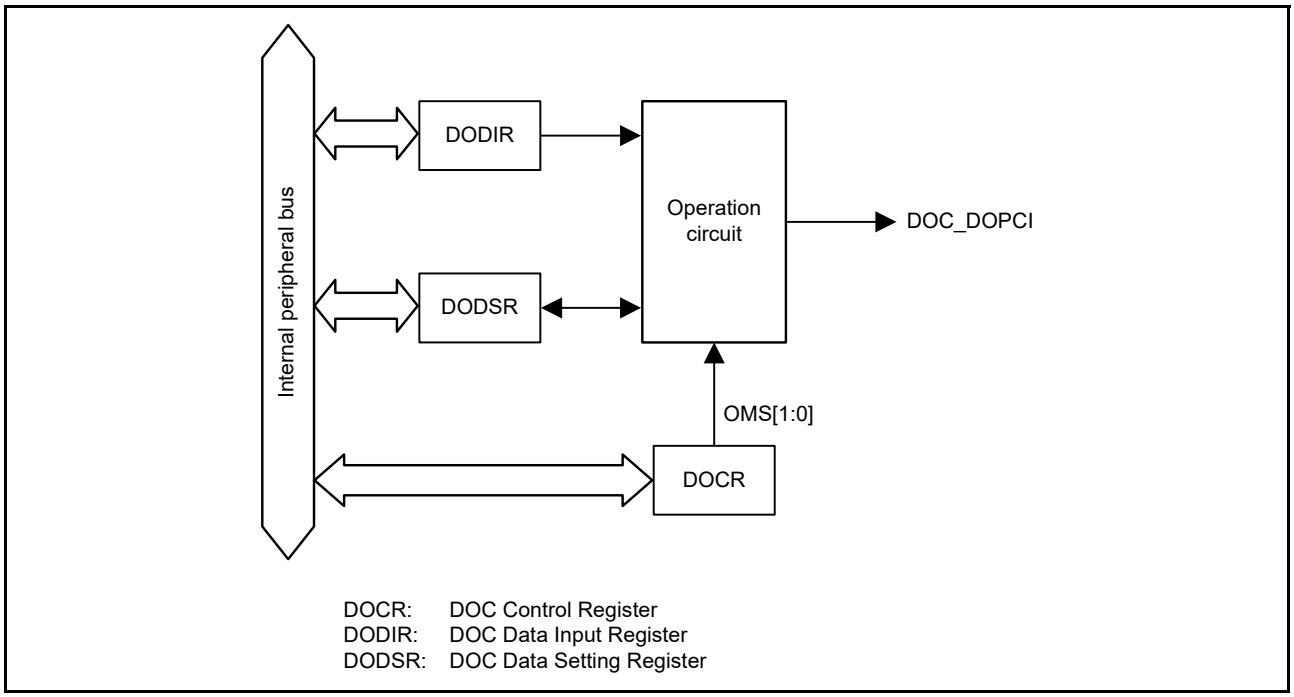


Figure 40.1 DOC block diagram

40.2 Register Descriptions

40.2.1 DOC Control Register (DOCR)

Address(es): DOC.DOCR 4005 4100h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	DOPCFCL	DOPCF	—	—	DCSEL	OMS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	OMS[1:0]	Operating Mode Select	b1 b0 0 0: Data comparison mode 0 1: Data addition mode 1 0: Data subtraction mode 1 1: Setting prohibited.	R/W
b2	DCSEL*1	Detection Condition Select	0: Set DOPCF when data mismatch is detected 1: Set DOPCF when data match is detected.	R/W
b4, b3	—	Reserved	There bits are read as 0. The write value should be 0.	R/W
b5	DOPCF	Data Operation Circuit Flag	Indicates the result of an operation.	R
b6	DOPCFCL	DOPCF Clear	0: Save DOPCF flag state 1: Clear DOPCF flag.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. Only valid when data comparison mode is selected.

OMS[1:0] bits (Operating Mode Select)

The OMS[1:0] bits select the operating mode of the DOC.

DCSEL bit (Detection Condition Select)

The DCSEL bit selects the detection condition in data comparison mode. This bit is only valid when data comparison mode is selected.

DOPCF flag (Data Operation Circuit Flag)

[Setting conditions]

- When the condition selected in the DCSEL bit is met
- When the result of data addition is greater than FFFFh
- When the result of data subtraction is less than 0000h.

[Clearing condition]

- Writing 1 to the DOPCFCL bit.

DOPCFCL bit (DOPCF Clear)

Setting the DOPCFCL bit to 1 clears the DOPCF flag. This bit is read as 0.

40.2.2 DOC Data Input Register (DODIR)

Address(es): DOC.DODIR 4005 4102h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DODIR is a 16-bit read/write register that stores 16-bit data for use in all operations.

40.2.3 DOC Data Setting Register (DODSR)

Address(es): DOC.DODSR 4005 4104h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The DODSR register is a 16-bit read/write register that stores 16-bit data used as a reference in data comparison mode. This register also stores the results of operations in data addition and subtraction modes.

40.3 Operation

40.3.1 Data Comparison Mode

Figure 40.2 shows an example DOC operation in data comparison mode. In this example, the DCSEL bit is set to 0 (data mismatch is detected as a result of data comparison). The steps are as follows:

1. Write 00b to the DOCR.OMS[1:0] bits to select data comparison mode.
2. Set the 16-bit reference data in the DODSR register.
3. Write the 16-bit data to be compared to the DODIR register.
4. Continue writing 16-bit data until all data to be compared is written to the DODIR register.
5. When DOCR.DCSEL = 0, if a value written to DODIR does not match that in DODSR, the DOCR.DOPCF flag is set to 1.

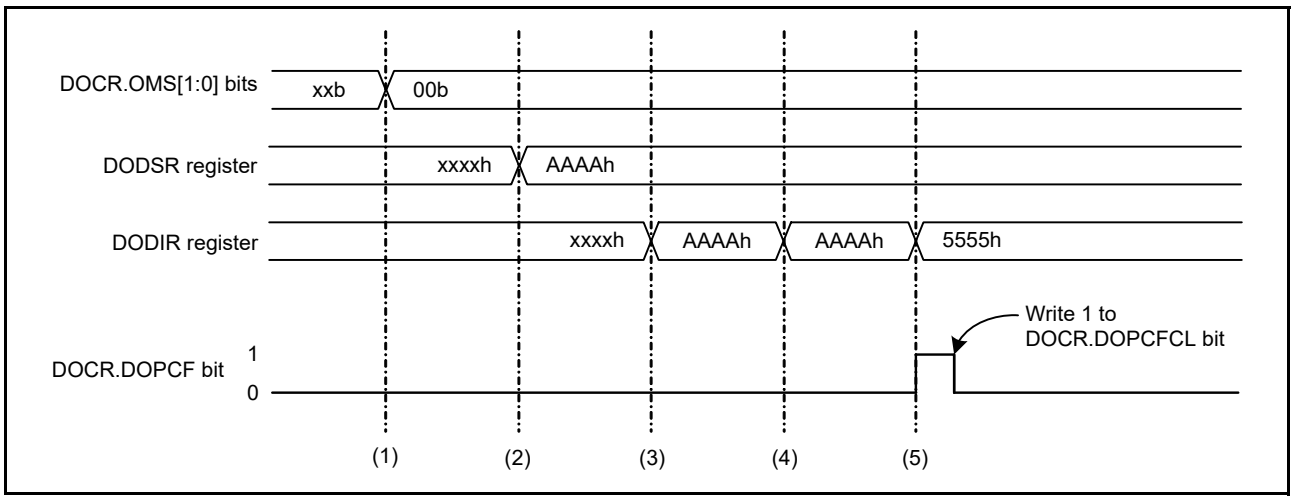


Figure 40.2 Example operation in data comparison mode

40.3.2 Data Addition Mode

Figure 40.3 shows an example DOC operation in data addition mode. The steps are as follows:

1. Write 01b to the DOCR.OMS[1:0] bits to select data addition mode.
2. Set 16-bit data as the initial value in the DODSR register.
3. Write the 16-bit data to be added to the DODIR register. The result of the operation is stored in the DODSR register.
4. Continue writing 16-bit data to the DODIR register until all data to be added is written.
5. If the result of an operation is greater than FFFFh, the DOCR.DOPCF flag is set to 1.

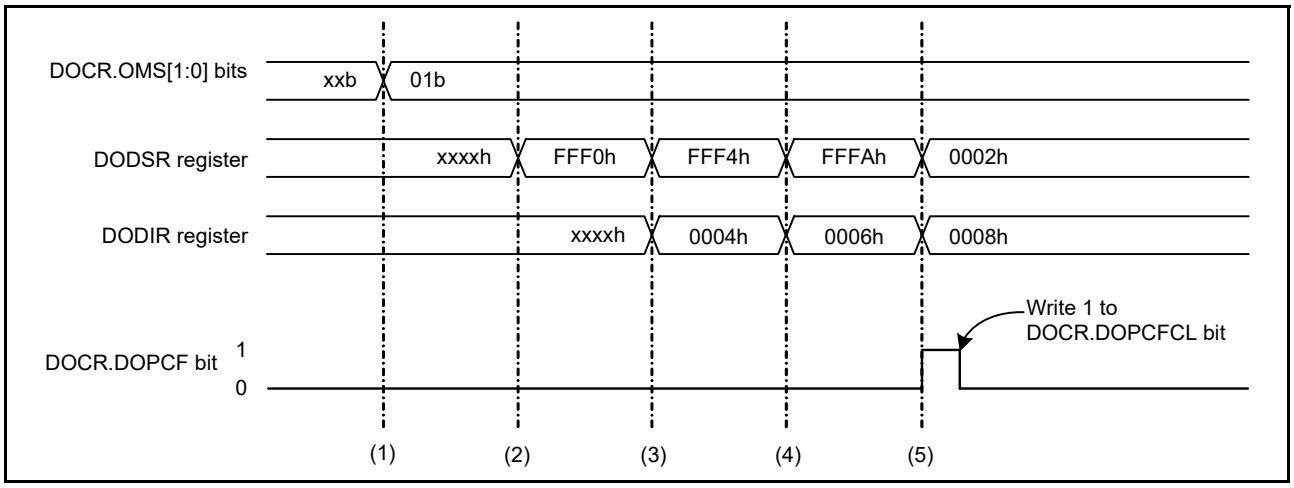


Figure 40.3 Example operation in data addition mode

40.3.3 Data Subtraction Mode

Figure 40.4 shows an example DOC operation in data subtraction mode. The steps are as follows:

1. Write 10b to the DOCR.OMS[1:0] bits to select data subtraction mode.
2. Set 16-bit data as the initial value in the DODSR register.
3. Write the 16-bit data to be subtracted to the DODIR register. The result of the operation is stored in the DODSR register.
4. Continue writing 16-bit data to the DODIR register until all data to be subtracted is written.
5. If the result of an operation is less than 0000h, the DOCR.DOPCF flag is set to 1.

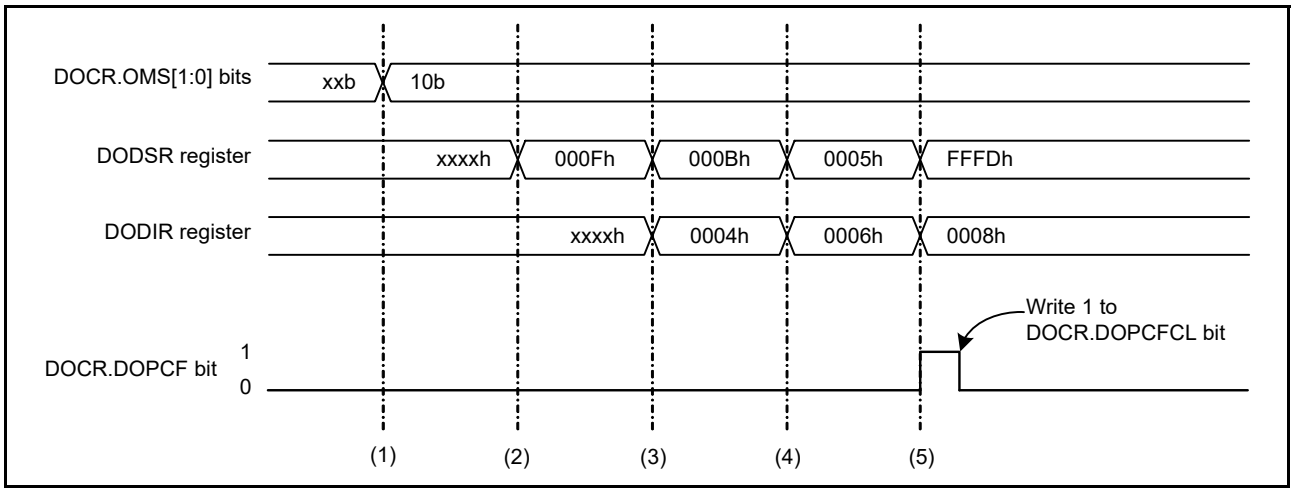


Figure 40.4 Example operation in data subtraction mode

40.4 Interrupt Request and Event Link Output

The DOC outputs an event signal to the ELC under the following conditions:

- Compared values either match or mismatch
- Data addition result is greater than FFFFh
- Data subtraction result is less than 0000h.

This signal can initiate operations by other modules selected in advance and can also serve as an interrupt request. When an event signal occurs, the data operation circuit flag (DOCR.DOPCF) is set to 1.

40.5 Usage Notes

40.5.1 Settings for the Module-Stop State

The Module-Stop Control Register C (MSTPCRC) can enable or disable DOC operation. The DOC is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

41. SRAM

The MCU provides on-chip, high-speed SRAMs with either parity-bit or Error Correction Code (ECC). The first 16-KB area of the SRAM0 is the ECC. Parity check is performed for the other areas.

41.1 Overview

Table 41.1 lists the SRAM specifications.

Table 41.1 SRAM specifications

Parameter	Without ECC	With ECC
SRAM capacity	SRAM0: 8 KB	SRAM0 (ECC area): 16 KB
SRAM address	SRAM0: 2000 4000h to 2000 5FFFh	SRAM0 (ECC area): 2000 0000h to 2000 3FFFh
Access*1	0 wait	
Module-stop function	Not available	
Parity	Even parity with 8-bit data and 1 parity bit	No parity
Error checking	Even parity error check	Detection of 1-bit and 2-bit errors, and correction of 1-bit error

Note: SRAM0 (without ECC) and Trace_RAM are shared. For the Trace_RAM specifications, see the *ARM® CoreSight™ MTB-M0+ Technical Reference Manual*.

Note 1. For details, see section 41.3.6, Access Cycle.

41.2 Register Descriptions

41.2.1 SRAM Parity Error Operation After Detection Register (PARIOAD)

Address(es): SRAM.PARIOAD 4000 2000h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	OAD
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	OAD	Operation After Detection	1: Reset 0: Non-maskable interrupt.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R

The SRAM Protection Register (SRAMPRCR) protects this register against writes. Always set the SRAMPRCR bit in SRAMPRCR to enabled before writing to this bit. Do not write to the PARIOAD register while accessing the SRAM.

OAD bit (Operation After Detection)

The OAD bit specifies either a reset or non-maskable interrupt when a parity error is detected. It applies to SRAM0 (without ECC).

41.2.2 SRAM Protection Register (SRAMPRCR)

Address(es): SRAM.SRAMPRCR 4000 2004h

	b7	b6	b5	b4	b3	b2	b1	b0
	KW[6:0]							SRAMPRCR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SRAMPRCR	Register Write Control	0: Disable writes to the protected registers 1: Enable writes to the protected registers.	R/W
b7 to b1	KW[6:0]	Write Key Code	These bits enable or disable writes to the SRAMPRCR bit	R/W

SRAMPRCR bit (Register Write Control)

The SRAMPRCR bit controls the write mode of the PARIOAD register. Setting the bit to 1 enables writes to the PARIOAD register. When you write to this bit, always write 78h to KW[6:0] at the same time.

KW[6:0] bits (Write Key Code)

The KW[6:0] bits enable or disable writes to the SRAMPRCR bit. When you write to SRAMPRCR bit, always write 78h to these bits at the same time. When any other value is written to KW[6:0], the SRAMPRCR bit is not updated. The KW[6:0] bits always read as 00h.

41.2.3 ECC Operating Mode Control Register (ECCMODE)

Address(es): SRAM.ECCMODE 4000 20C0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	ECCMOD[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	ECCMOD[1:0]	ECC Operating Mode Select	b1 b0 0 0: Disable ECC function 0 1: Setting prohibited 1 0: Enable ECC function without error checking 1 1: Enable ECC function with error checking.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The ECCMODE register specifies the ECC operating mode. The ECC Protection Register (ECCPRCR) protects this register against writes. Before writing to this register, set the ECCPRCR bit in the ECCPRCR register to 1 (write protection disabled). Do not write to the ECCMODE register while accessing the SRAM.

ECCMOD[1:0] bits (ECC Operating Mode Select)

The ECCMOD[1:0] bits set the access mode for the ECC area in SRAM0.

41.2.4 ECC 2-Bit Error Status Register (ECC2STS)

Address(es): SRAM.ECC2STS 4000 20C1h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ECC2ERR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ECC2ERR	ECC 2-Bit Error Status	0: No 2-bit ECC error occurred 1: 2-bit ECC error occurred.	R(/W) *1
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only 0 can be written to clear the bit.

ECC2ERR bit (ECC 2-Bit Error Status)

The ECC2ERR bit indicates whether a 2-bit ECC error occurred in the ECC area of SRAM0. When a 2-bit error is detected while ECC operations are enabled and error checking is selected, the ECC2ERR bit is set to 1. The SRAM error signal is also asserted at this time. The 2-bit ECC error can be cleared by writing 0 to the ECC2ERR bit. The SRAM error can be specified as a non-maskable interrupt or a reset in the ECCOAD register. Do not access the ECC area in SRAM0 while writing 0 to this register.

41.2.5 ECC 1-Bit Error Information Update Enable Register (ECC1STSEN)

Address(es): SRAM.ECC1STSEN 4000 20C2h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	E1STSEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	E1STSEN	ECC 1-Bit Error Information Update Enable	0: Disable updating of 1-bit ECC error information 1: Enable updating of 1-bit ECC error information.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The ECC1STSEN register enables or disables updating of the ECC 1-bit Error Status register (ECC1STS) in response to a 1-bit error ECC error in the SRAM0 (ECC area).

The ECC Protection Register (ECCPRCR) protects this register against writes. Before writing to this bit, set the ECCPRCR bit in the ECCPRCR register to 1 (write protection disabled).

E1STSEN bit (ECC 1-Bit Error Information Update Enable)

The E1STSEN bit enables or disables updating of the SRAM (ECC area) 1-Bit Error Status register (ECC1STS) in response to a 1-bit error in the ECC area of SRAM0. This register also functions as an interrupt or a reset mask.

41.2.6 ECC 1-Bit Error Status Register (ECC1STS)

Address(es): SRAM.ECC1STS 4000 20C3h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ECC1ERR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ECC1ERR	ECC 1-Bit Error Status	0: No 1-bit ECC error occurred 1: 1-bit ECC error occurred.	R(/W) *1
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only 0 can be written to clear the bit.

ECC1ERR bit (ECC 1-Bit Error Status)

The ECC1ERR bit indicates whether a 1-bit ECC error occurred in the ECC area of SRAM0. When a 1-bit error is detected while ECC operations are enabled, error correction is selected, and updating of the 1-bit error information is enabled. The ECC1ERR bit is set to 1 and the SRAM error signal is asserted at this time. The 1-bit ECC error can be cleared by writing 0 to the ECC1ERR bit.

The SRAM error can be specified as a non-maskable interrupt or a reset in the ECCOAD register. Do not access the ECC area in SRAM0 while writing 0 to this register.

41.2.7 ECC Protection Register (ECCPRCR)

Address(es): SRAM.ECCPRCR 4000 20C4h

	b7	b6	b5	b4	b3	b2	b1	b0
	KW[6:0]							ECCPRCR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ECCPRCR	Register Write Control	0: Disable writes to the protected registers 1: Enable writes to the protected registers.	R/W
b7 to b1	KW[6:0]	Write Key Code	These bits enable or disable writes to the ECCPRCR bit	R/W

ECCPRCR bit (Register Write Control)

The ECCPRCR bit controls write protection for registers ECCMODE, ECC1STSEN, and ECCOAD. When the ECCPRCR bit is set to 1, writing to registers ECCMODE, ECC1STSEN, and ECCOAD is enabled. When writing to this bit, write 78h to the KW[6:0] bits at the same time.

KW[6:0] bits (Write Key Code)

The KW[6:0] bits enable or disable writes to the ECCPRCR bit. When writing to ECCPRCR bit, always write 78h to the KW[6:0] bits at the same time. When any other value is written to the KW[6:0] bits, the ECCPRCR bit is not updated. The KW[6:0] bits are always read as 00h.

41.2.8 ECC Protection Register 2 (ECCPRCR2)

Address(es): SRAM.ECCPRCR2 4000 20D0h

	b7	b6	b5	b4	b3	b2	b1	b0
	KW2[6:0]							ECCPRCR2
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ECCPRCR2	Register Write Control	0: Disable writes to the protected registers 1: Enable writes to the protected registers.	R/W
b7 to b1	KW2[6:0]	Write Key Code	These bits enable or disable writing of the ECCPRCR2 bit.	R/W

ECCPRCR2 bit (Register Write Control)

The ECCPRCR2 bit controls write protection for the ECCETST register. When the ECCPRCR2 bit is set to 1, writes to the ECCETST register is enabled. When writing to this bit, write 78h to the KW2[6:0] bits at the same time.

KW2[6:0] bits (Write Key Code)

The KW2[6:0] bits enable or disable writes to the ECCPRCR2 bit. When writing to ECCPRCR2 bit, write 78h to the KW2[6:0] bits at the same time. When a value other than 78h is written to the KW2[6:0] bits, the ECCPRCR2 bit is not updated. The KW2[6:0] bits are always read as 00h.

41.2.9 ECC Test Control Register (ECCETST)

Address(es): SRAM.ECCETST 4000 20D4h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	TSTBYP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TSTBYP	ECC Bypass Select	0: Disable ECC bypass 1: Enable ECC bypass.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The ECC Protection Register 2 (ECCPRCR2) protects this register against writes. When writing to this bit, set the ECCPRCR2 bit in the ECCPRCR2 register to 1 (write protection disabled). Do not access the SRAM while writing to this register.

TSTBYP bit (ECC Bypass Select)

The TSTBYP bit enables direct access to the ECC code by bypassing the ECC function.

When the ECC bypass function is used, the ECCMOD[1:0] bits in the ECCMODE register are set to 00b. The ECC must be accessed in 32 bits using the same address for 32-bit data. The ECC code is assigned to the lower 7 bits of the 32-bit data. When writing the ECC code, the upper 25 bits are ignored. When reading the ECC code, the upper 25 bits are undefined.

Note: For details on the ECC test, see section 41.3.3, ECC Decoder Testing.

41.2.10 SRAM ECC Error Operation After Detection Register (ECCOAD)

Address(es): SRAM.ECCOAD 4000 20D8h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	OAD
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	OAD	Operation After Detection	1: Reset 0: Non-maskable interrupt.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The ECC Protection Register (ECCPRCR) protects this register against writes. Before writing to this bit, set the ECCPRCR bit in the ECCPRCR register to 1 (write protection disabled). Do not write to this register while accessing the SRAM.

OAD bit (Operation After Detection)

The OAD bit selects whether to generate either a reset or a non-maskable interrupt when an ECC error is detected. The OAD bit in the ECCOAD register is used for SRAM0 (ECC area).

41.2.11 Trace Control (for the MTB)

The Micro Trace Buffer (MTB) has programmable registers to control the behavior of the trace features and the POSITION, MASTER, FLOW, and BASE registers. The following shows the registers in offset order from the base address:

MTB_BASE: 4001 9000h
MTB_BASE + 000h: POSITION value on reset: Bits [31:0] = UNKNOWN
MTB_BASE + 004h: MASTER value on reset: Bits [31] = 0, Bits [30:10] = UNKNOWN,
Bits [9:8] = 0, Bits [7]=1, Bits [6:5] = 0,
Bits [4:0] = UNKNOWN
MTB_BASE + 008h: FLOW value after reset: Bits [31:2] = UNKNOWN, Bits[1:0] = 0
MTB_BASE + 00Ch: BASE value after reset: Bits [31:0] = 2000 4000h

For more information on these registers, see the *ARM® CoreSight™ MTB-M0+ Technical Reference Manual* (revision: r0p1).

Note: Do not attempt to access reserved or unused address locations. This can result in UNPREDICTABLE behavior.

The MTB for trace is limited from 2000_4000H to 2000_5FFFH.

41.2.12 CoreSight™ (for MTB)

See the *ARM® CoreSight™ Architecture Specification* for more information about the registers and access types. The following shows the registers in offset order from the base address:

MTB_BASE: 4001 9000h
MTB_BASE + FF0h to FFCh: Component ID
MTB_BASE + FE0h to FDCh: Peripheral ID
MTB_BASE + FCCh: Device Type Identifier
MTB_BASE + FC8h: Device Configuration
MTB_BASE + FBCh: Device Architecture
MTB_BASE + FB8h: Authentication Status
MTB_BASE + FB4h: Lock Status
MTB_BASE + FB0h: Lock Access

For more information on these registers, see the *ARM® CoreSight™ MTB-M0+ Technical Reference Manual* (Revision:

r0p1).

Note: Do not attempt to access reserved or unused address locations. This can result in UNPREDICTABLE behavior.

41.3 Operation

41.3.1 ECC Function

You can enable or disable the ECC function by setting the ECCMODE register. By default, the ECC function is disabled and the ECC check type is SEC-DED (Single-Error Correction and Double-Error Detection).

When the ECC function is enabled, 7-bit check bits are appended to 32-bit data for writes. For reads, 39-bit data (32-bit data and 7-bit check bits) is read from the SRAM (ECC area).

When the ECC function and error checking are both enabled, an error correction is performed if a 1-bit error occurs, and the ECC1ERR bit in the ECC1STS register is set to 1 if the E1STSEN bit in the ECC1STSEN register is 1. If a 2-bit error occurs, the error is detected without error correction, and the ECC2ERR bit in the ECC2STS register is set to 1.

When the ECC function is enabled and error checking is disabled, error correction is performed if a 1-bit error occurs but the ECC1ERR bit in the ECC1STS register is not updated even if the E1STSEN bit in the ECC1STSEN register is 1. If a 2-bit error occurs, the error is detected but the ECC2ERR bit in the ECC2STS register is not updated, and error correction is not performed.

When the ECC function is disabled, neither error correction nor error detection is performed even when 1-bit or 2-bit error occurs. Therefore, the ECC1ERR bit or the ECC2ERR bit is not updated.

It is not possible to confirm the location where the error is detected. Therefore, after an error occurred, update all the data by writing 32-bit data to the SRAM.

The SRAM data is undefined after a power on. If the SRAM is accessed when the ECC function and error checking are both enabled, an ECC error might occur. To avoid this, write 32-bit data to the area used in the SRAM before using the ECC function.

When a read access is performed consecutively after a write access, the read access has priority. Therefore, during initialization, do not perform a read access successively after a write access.

41.3.2 ECC Error Generation

When the ECC function is enabled and error checking is applied to SRAM0 (ECC area), an ECC error occurs when either the ECC2ERR bit in the ECC2STS register or the ECC1ERR bit in the ECC1STS register becomes 1 to indicate that a 2-bit error or a 1-bit error has occurred.

To mask ECC 1-bit errors, set the ECC1STSEN.E1STSEN bit to 0 to disable ECC1ERR bit update. An ECC error is not generated when the ECC function is disabled or enabled without error checking.

An ECC error can generate a non-maskable interrupt or a reset, as selected in the ECCOAD register. When the OAD bit in the ECCOAD register is set to 1, an ECC error is output to the reset function. When the OAD bit in the ECCOAD register is set to 0, an ECC error is output to the ICU as a non-maskable interrupt.

41.3.3 ECC Decoder Testing

Figure 41.1 shows the ECC decoder testing.

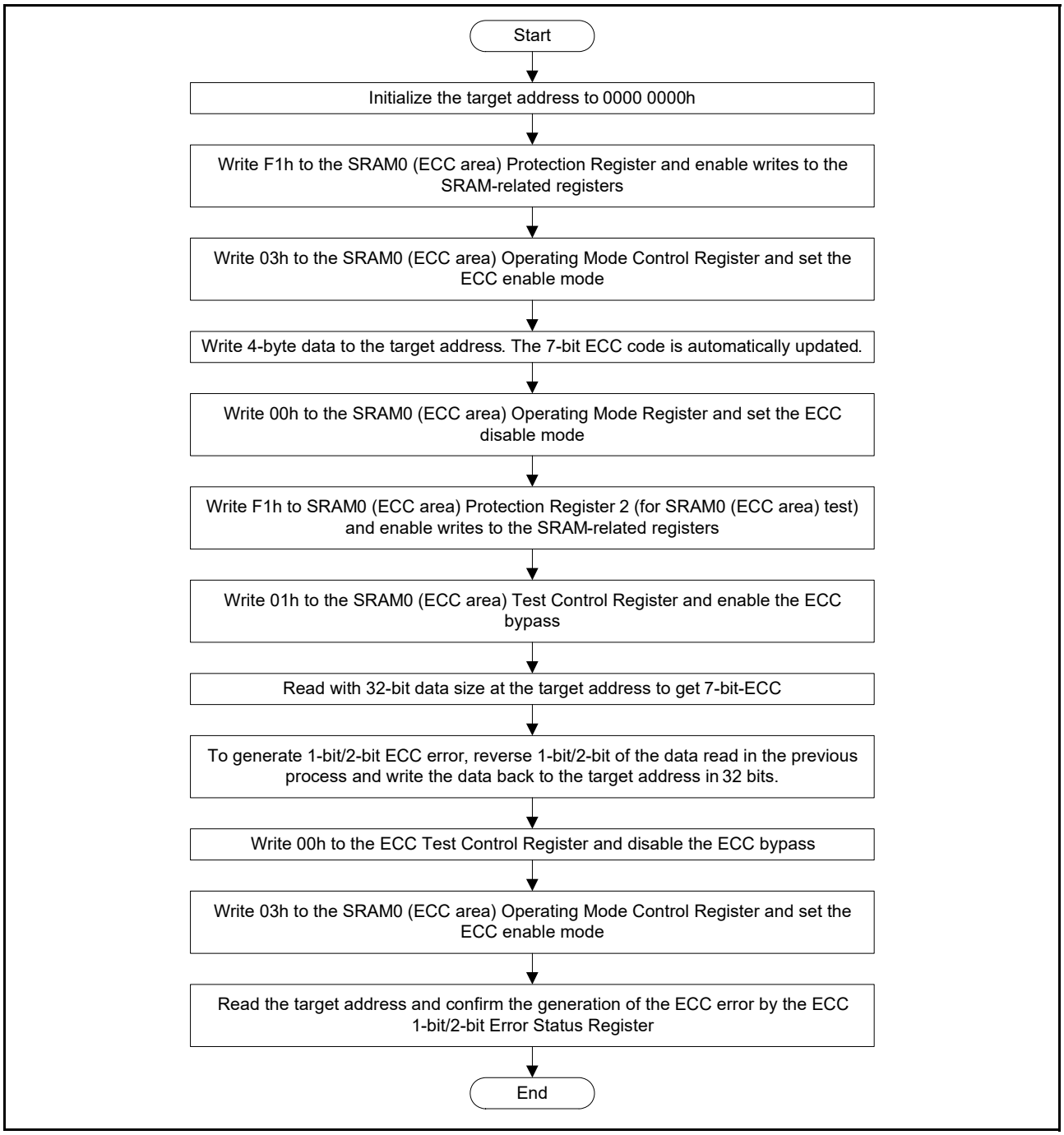


Figure 41.1 ECC decoder testing

41.3.4 Parity Calculation Function

The IEC60730 standard requires the checking of SRAM data. A parity bit is therefore added to every 8-bit data in the SRAM which has 32-bit data width. The parity bit is appended when data is written, and the parity is checked when the data is read. When a parity error occurs, a parity-error notification is generated. This function can also be used to trigger a reset. Specification of SRAM0 without ECC is even parity.

Parity-error notification can be specified as either a non-maskable interrupt or a reset, in the OAD bit of the PARIOAD register. When OAD is 1, a parity error is output to the reset function. When OAD is 0, a parity error is output to the ICU as a non-maskable interrupt.

Parity errors often occur because of noise. To confirm whether the cause is noise or corruption, follow the parity check flows shown in Figure 41.2 and Figure 41.3.

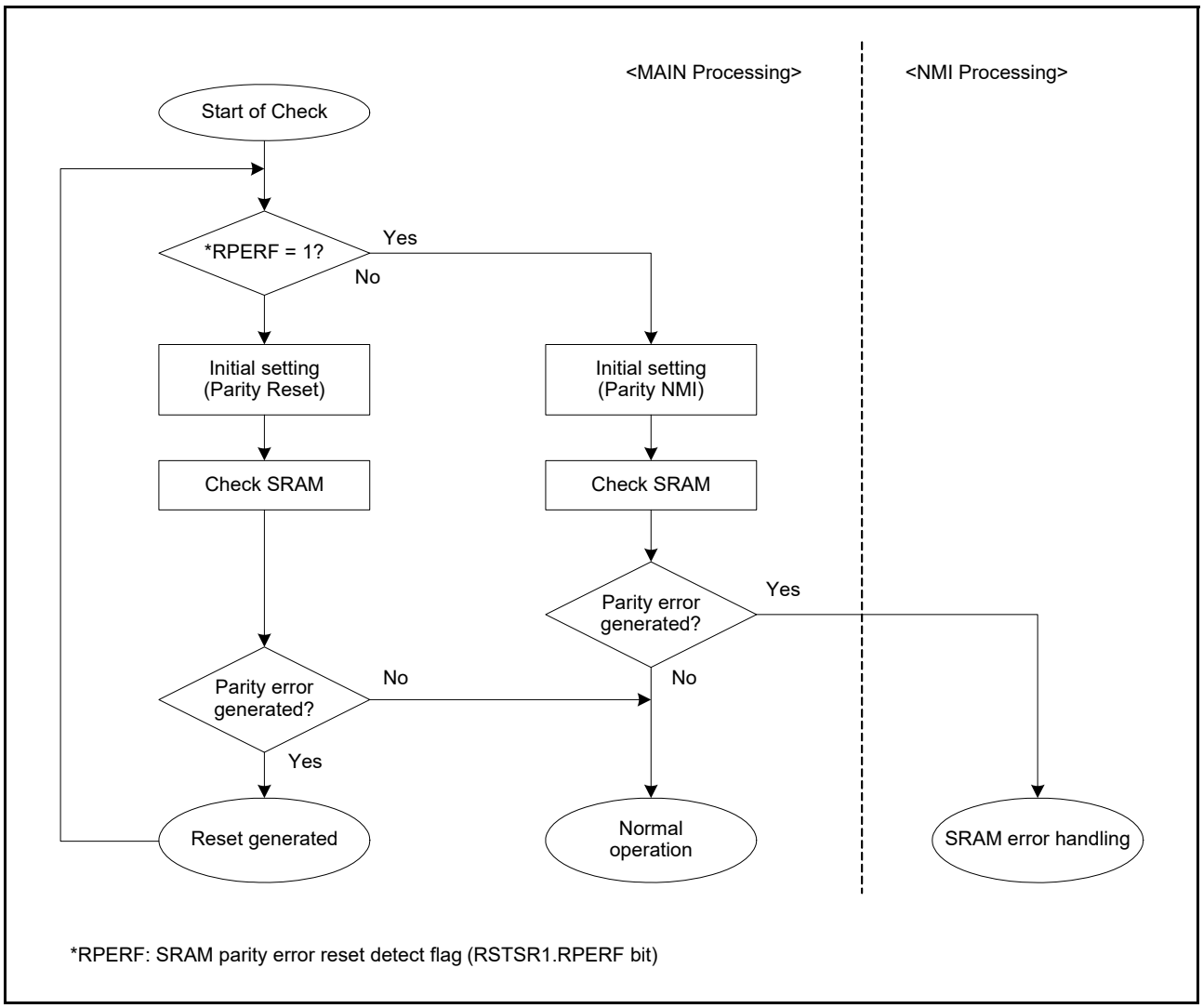


Figure 41.2 Flow of SRAM parity check when SRAM parity reset is enabled

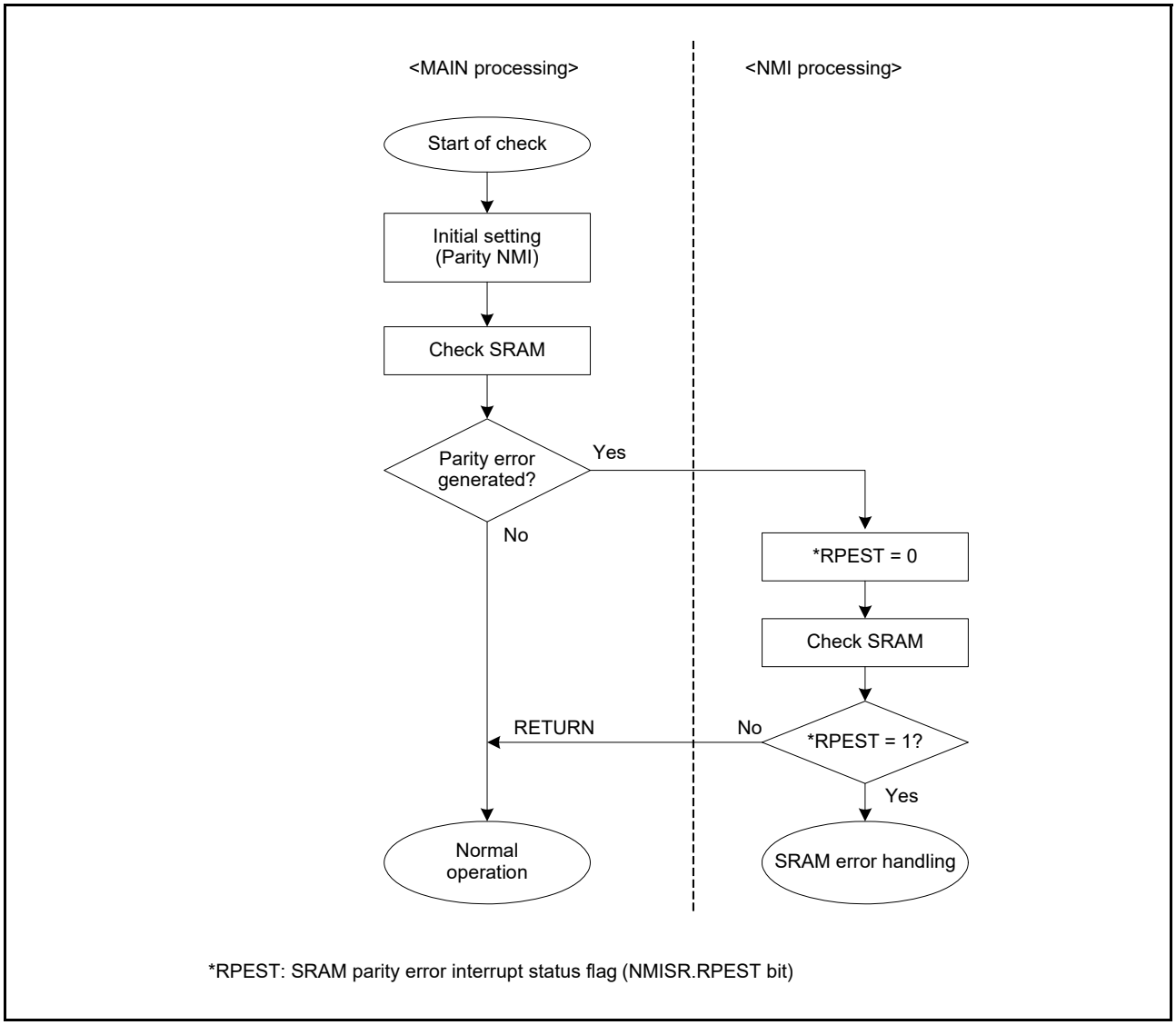


Figure 41.3 Flow of SRAM parity check when SRAM parity interrupt is enabled

41.3.5 SRAM Error Sources

An SRAM error is caused by either an ECC error or a parity error. ECC error or parity error can generate either a non-maskable interrupt or a reset, as selected with the OAD bit in the PARIOAD register. TDC activation is not supported for SRAM parity errors.

Table 41.2 SRAM error sources

SRAM error source	DTC activation
ECC error (SRAM0 area with ECC)	Not possible
Parity error (SRAM0 area without ECC)	Not possible

41.3.6 Access Cycle

Table 41.3 SRAM0 (ECC area 2000 0000h to 2000 3FFFh)

	Read (cycle)		Write (cycle)	
	Word access	Halfword/Byte access	Word access	Halfword/Byte access
ECC Off ECCMOD[1] = 0	2		2	
ECC On ECCMOD[1] = 1	2		2	4

Table 41.4 SRAM0 (Parity area 2000 4000h to 2000 5FFFh)

Read (cycles)		Write (cycles)	
Word access	Halfword/Byte access	Word access	Halfword/Byte access
2		2	

41.4 Usage Note

41.4.1 Instruction Fetch from the SRAM Area

When using SRAM0 to operate a program, initialize the SRAM area so that the CPU can correctly prefetch the data. If the CPU prefetches data from an uninitialized SRAM area, an ECC error or a parity error might occur. Initialize the additional 2-byte area from the end address of programs with a 4-byte boundary. Renesas recommends using a NOP instruction to initialize these areas.

41.4.2 Store Buffer of SRAM

For fast access between SRAM and CPU, a store buffer is used. When a load instruction is executed from the same address after a store instruction to SRAM, the load instruction might read out data from the buffer instead of data on the SRAM. To read data on the SRAM correctly, use either of the following procedures:

- After writing to the SRAM (address = A), use the NOP instruction, then read the SRAM (address = A)
- After writing to the SRAM (address = A), read data from area other than SRAM (address = A), then read the SRAM (address = A).

42. Flash Memory

42.1 Overview

The MCU provides up to 256-KB code flash memory and 4-KB data flash memory. The Flash Control Block (FCB) controls the programming commands.

This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc.

Table 42.1 lists the specifications of the code flash memory and data flash memory, and Figure 42.1 shows a block diagram of the related modules. Figure 42.2 shows the configuration of the code flash memory, and Figure 42.3 shows the configuration of the data flash memory.

Table 42.1 Specifications of code flash memory and data flash memory

Parameter	Code flash memory	Data flash memory
Memory capacity	• Up to 256 KB of user area	4 KB of data area
Read cycle	• ICLK frequency ≤ 32 MHz	• ICLK frequency ≤ 32 MHz • A read operation takes 6 ICLK cycles in bytes
Value after erasure	FFh	FFh
Programming and erasing method	• Programming and erasing of code and data flash memory through the FCB commands specified in the registers • Programming by dedicated flash-memory programmer through a serial interface (serial programming) • Programming of flash memory by a user program (self-programming).	
Security function	Protection against illicit tampering with or reading of data in flash memory	
Protection	Protection against erroneous overwriting of flash memory	
Background operations (BGOs)	Code flash memory can be read during data flash memory programming	
Programming and erasing units	• 32-bit units for programming in user area • 1-KB erasing units for the user area.	• 8-bit units for programming in data area • 1-KB units for erasure in data area.
Other functions	Interrupts accepted during self-programming	
	An expansion area of flash memory (option bytes) can be set in the initial MCU settings	
On-board programming	Programming in serial programming mode (SCI boot mode): • Asynchronous serial interface (SCI9) used • Transfer rate adjusted automatically. Programming in On-Chip Debug (OCD) mode: • SWD interface used • Dedicated hardware not required. Programming by a routine for code and data flash programming within the user program: • Allows code and data flash memory programming without resetting the system.	

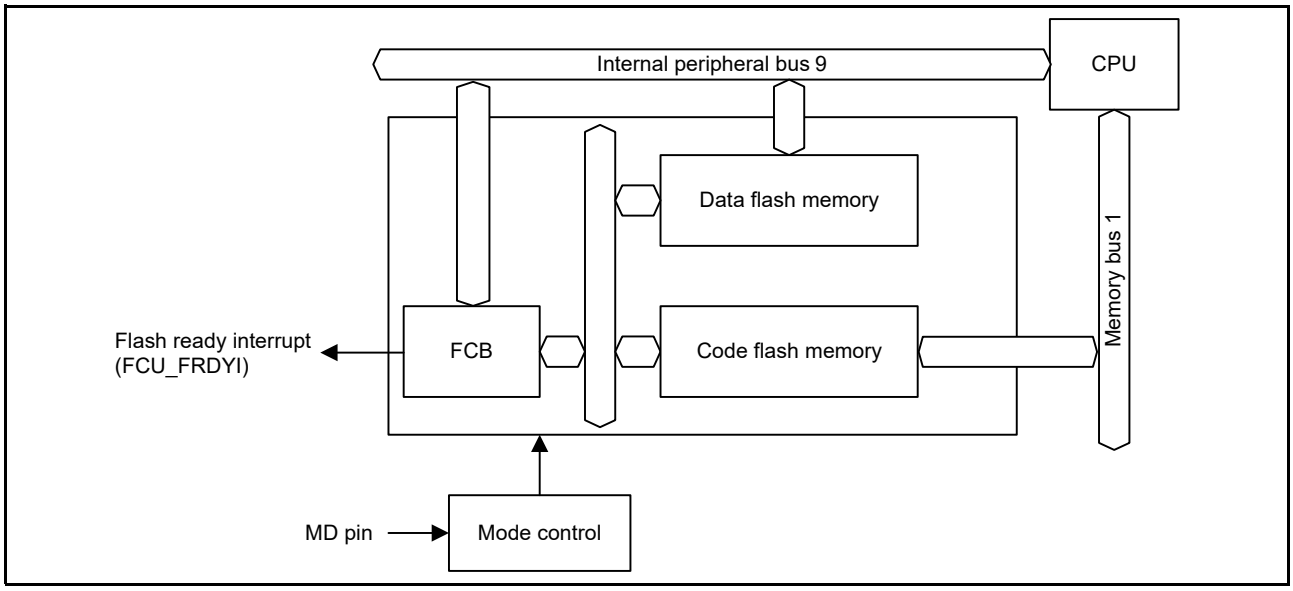


Figure 42.1 Block diagram of flash memory-related modules

42.2 Memory Structure

Figure 42.2 shows the mapping of the code flash memory, and Table 42.2 shows the read and programming/erasure addresses of the code flash memory. The user area of the code flash memory is divided into 1-KB blocks, which serves as the erasure units. The user area is available for storing user program.

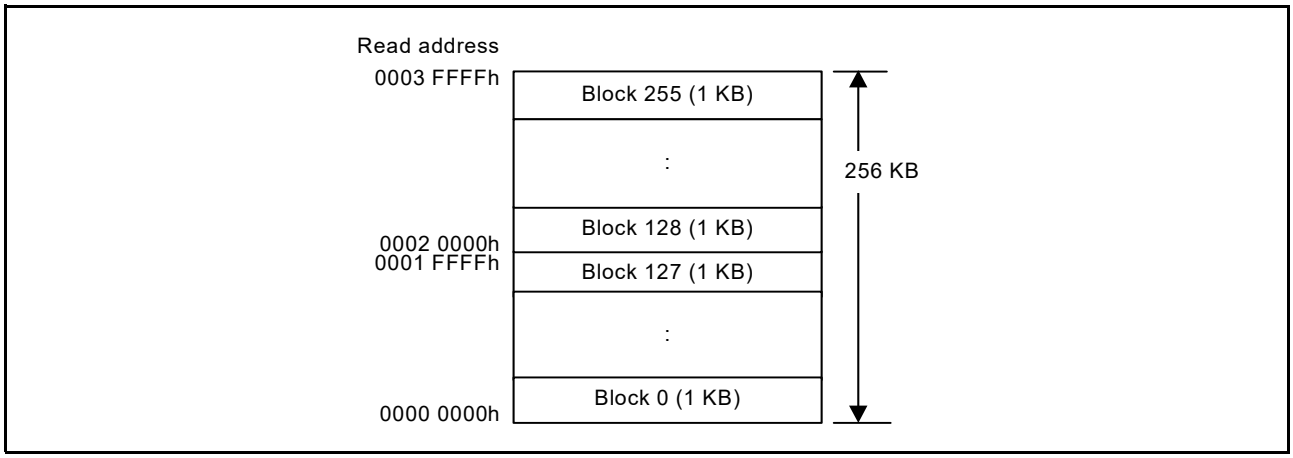


Figure 42.2 Mapping of the code flash memory

Table 42.2 Read and P/E addresses of the code flash memory

Size of code flash memory	Read address	P/E address	Number of blocks
256 KB	0000 0000h to 0003 FFFFh	0000 0000h to 0003 FFFFh	0 to 255

The data area of the data flash memory is divided into 1-KB blocks, with each being an erasure unit. Figure 42.3 shows the mapping of the data flash memory, and Table 42.3 shows the read and programming/erasure addresses of the data flash memory.

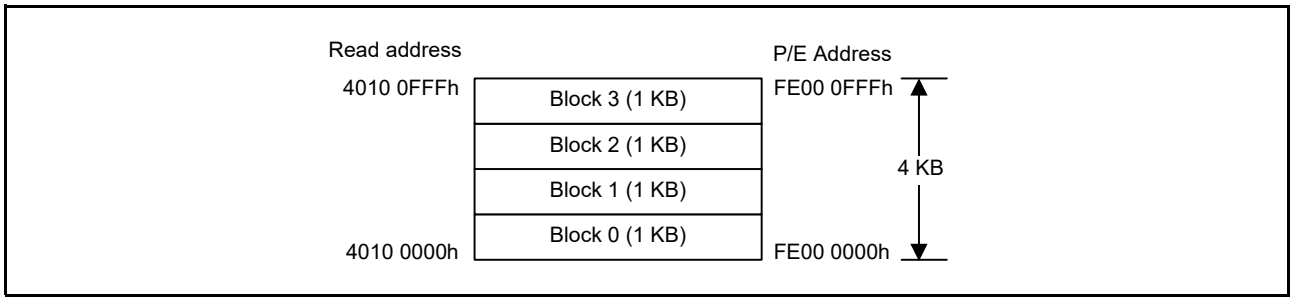


Figure 42.3 Mapping of data flash memory

Table 42.3 Read and P/E addresses of the data flash memory

Size of data flash memory	Read address	P/E address	Number of blocks
4 KB	4010 0000h to 4010 0FFFh	FE00 0000h to FE00 0FFFh	0 to 3

42.3 Operating Modes Associated with the Flash Memory

Figure 42.4 shows a diagram of the mode transitions associated with the flash memory. For information on setting up the modes, see section 3, Operating Modes.

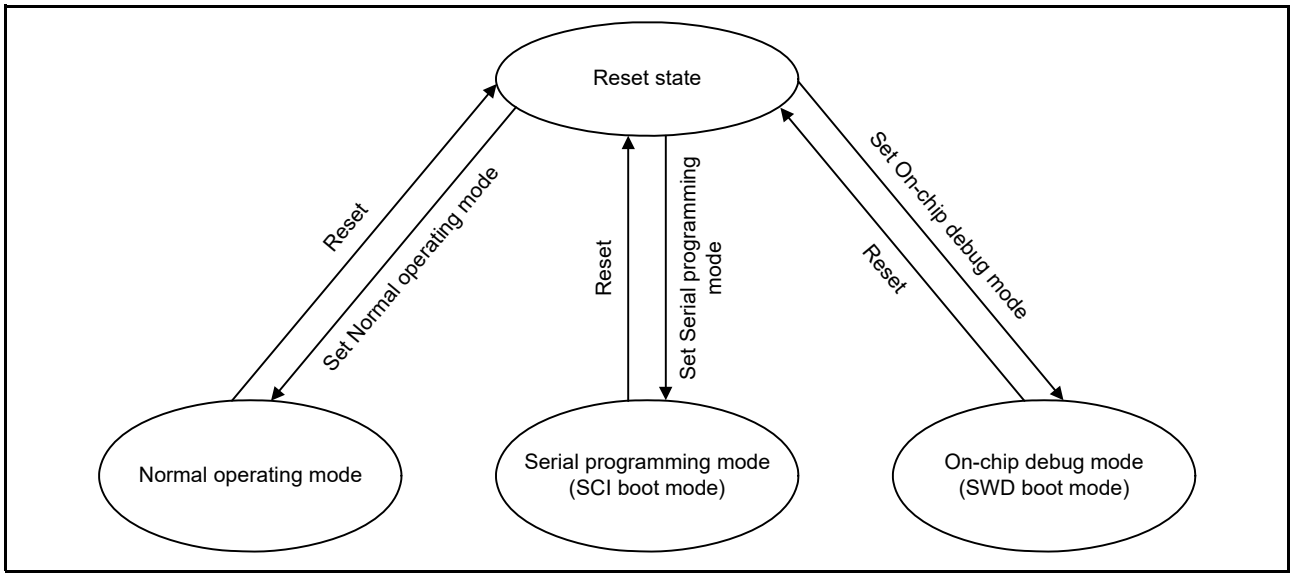


Figure 42.4 Mode transitions associated with the flash memory

The flash memory areas where programming and erasure are permitted and where the boot program executes after a reset differs with the mode. Table 42.4 shows the differences between the modes.

Table 42.4 Difference between modes

Parameter	Normal operating mode	Serial programming mode (SCI boot mode)	On-chip debug mode (SWD boot mode)
Programmable and erasable areas	• Code flash memory • Data flash memory	• Code flash memory • Data flash memory	• Code flash memory • Data flash memory
Erasure in block units	Possible	Possible	Possible
Boot program at a reset	User area program	Embedded program for serial programming	Depends on debug command

42.3.1 ID Code Protection

The ID code protection function prohibits programming and on-chip debugging. When ID code protection is enabled, the device validates or invalidates the ID code sent from the host by comparing it to the ID code stored in the flash memory. Programming and on-chip debugging are enabled only when the two match.

The ID code in the flash memory consists of four 32-bit words. ID code bits [127] and [126] determine whether ID code protection is enabled and the authentication method to use with the host. Table 42.5 shows how ID code determines the authentication method.

Table 42.5 Specifications for ID code protection

Operating mode on boot up	ID code	State of protection	Operations on connection with the programmer or on-chip debugger
Serial programming mode (SCI boot mode) On-chip debug mode (SWD boot mode)	FFh, …, FFh (all bytes FFh)	Protection disabled	The ID code is not checked, the ID code always matches, and the connection to the serial programmer or on-chip debugger is permitted.
	Bit [127] = 1, bit [126] = 1, and at least one of the 16 bytes is not FFh	Protection enabled	Matching ID code indicates that authentication is complete and connection to the serial programmer or the on-chip debugger is permitted. Mismatching ID code indicates transition to the ID code protection wait state. When the ID code sent from the serial programmer or the on-chip debugger is ALeRASE in ASCII code (0x414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFF), the content of the user flash area is erased and all bits in the OSIS register are 1. However, when the AWS.FSPR bit is 0 or security MPU is enabled, the content of the user flash area is not erased.
	bit [127] = 1 and bit [126] = 0	Protection enabled	Matching ID code indicates that authentication is complete and connection to the serial programmer or the on-chip debugger is permitted. Mismatching ID code indicates transition to the ID code protection wait state.
	Bit [127] = 0	Protection enabled	The ID code is not checked, the ID code is always mismatching, the connection to the serial programmer or the on-chip debugger is prohibited. When the ID code sent from the on-chip debugger is ALeRASE in ASCII code (0x414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFF), the content of the user flash area is erased and all bits in the OSIS register are 1. However, when the AWSC.FSPR bit is 0 or security MPU is enabled, the content of the user flash area is not erased.

42.4 Overview of Functions

By using a dedicated flash-memory programmer to program the on-chip flash memory through a serial interface for serial programming mode, or through an SWD interface for on-chip debug mode, the device can be programmed before or after it is mounted on the target system. Additionally, security functions to prohibit overwriting of the user program prevent tampering by third parties.

Programming by the user program (self-programming) is available for applications that might require updating after system manufacturing or shipment. Protection features for safely overwriting the flash memory area are also provided. Additionally, interrupt processing during self-programming is supported so that programming can proceed while processing external communications and other functions. Table 42.6 lists the programming methods and the corresponding operating modes.

Table 42.6 Programming methods

Programming method	Functional overview	Operating mode
Serial programming	A dedicated flash-memory programmer connected through the SCI interface enables on-board programming of the flash memory after the device is mounted on the target system	Serial programming mode
	A dedicated flash-memory programmer connected through the SCI interface and a dedicated programming adapter board allow off-board programming of the flash memory, for example, programming of the device before it is mounted on the target system	
Self-programming	A user program written to memory in advance of serial programming execution can also program the flash memory. The background operation capability makes it possible to fetch instructions or otherwise read data from the code flash memory while the data flash memory is programmed. As a result, a program resident in code flash memory is able to program the data flash memory. Background operation can also be used to read the code flash memory while programming the data flash memory (see Table 42.11). While the code flash memory is being self-programmed, background fetching of instructions in the code flash memory and data access are not possible. In such cases, a program for programming from the internal SRAM or external memory must be transferred in advance and executed.	Normal operating mode
SWD programming	A dedicated flash-memory programmer or an on-chip debugger connected through SWD enables on-board programming of the flash memory after the device is mounted on the target system	On-chip debug mode
	A dedicated flash-memory programmer or an on-chip debugger connected through SWD and a dedicated programming adapter board allow off-board programming of the flash memory, before it is mounted on the target system	

Table 42.7 lists the functions of the on-chip flash memory. Use serial programmer commands for serial programming. For self-programming, use the programming commands to read the on-chip flash memory or run the user program.

Table 42.7 Basic functions

Function	Functional overview	Supported/not supported	
		Serial programming	Self-programming
Blank check	Checks a specified block to ensure that writing to it has not already proceeded. Results of reading from data flash memory to which nothing was written after erasure are not guaranteed, so use blank checking to confirm that writing to memory has not occurred after erasure.	Not supported	Supported
Block erasure	Erases the memory contents in the specified block	Supported	Supported
Programming	Writes to the specified address	Supported	Supported
Read	Reads data programmed to the flash memory	Supported	Not supported (read by user program is possible)
ID code check	Compares the ID code sent by the host with the code stored in the ROM, and if the two match, the FCB enters the wait state for programming and erasure commands from the host	Supported	Not supported (ID authentication is not performed)
Security configuration	Configures the security function for serial programming	Supported with conditions (only switching the configuration from enabled to disabled is possible)	Supported with conditions (only switching the configuration from enabled to disabled is possible)
Protection configuration	Configures access window for flash area protection in the code flash memory	Supported	Supported

The on-chip flash memory supports the ID code security function. Authentication of ID codes is a security function for use with serial programming and SWD programming. Table 42.8 lists the security functions supported by the on-chip flash memory, and Table 42.9 lists available operations and security settings.

Table 42.8 Security functions

Function	Description
ID authentication	The result of ID authentication can be used to control the connection of a serial programmer for serial programming

Table 42.9 Available operations and security settings

	All security settings and erasure, programming, and read operations		Constraints on the security setting configuration
Function	**Serial programming and on-chip debug mode**	**Self-programming mode**	**Self-programming mode**
ID authentication	When ID codes do not match: • Block erasure commands not supported • Programming commands not supported • Read commands not supported • Security configuration commands not supported • Protection configuration commands not supported. When ID codes match: • Block erasure commands supported • Programming commands supported • Read commands supported • Security configuration commands supported • Protection configuration commands supported.	ID authentication is not performed: • Blank check supported • Block erasure supported • Programming supported • Security configuration supported • Protection configuration supported.	ID authentication is not performed

42.4.1 Configuration Area Bit Map

The bits used for the ID authentication, startup area select, access window protection, and security configuration functions are mapped in Figure 42.5. The boot program must use these bits as hexadecimal data.

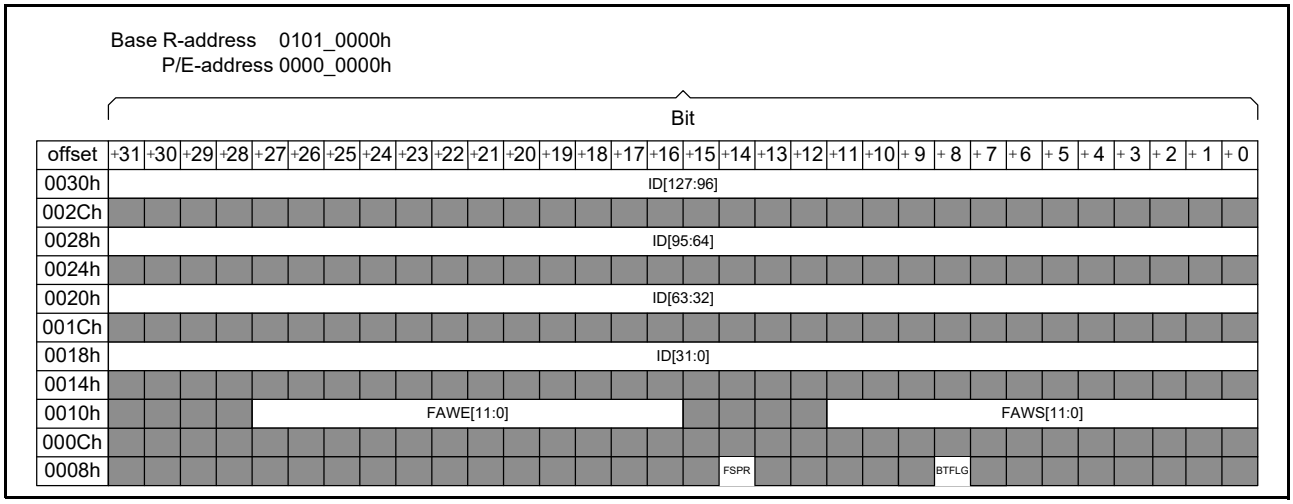


Figure 42.5 Configuration area bit map

42.4.2 Startup Area Select

The startup area select function allows the boot program to be safely updated. The size of the startup area is 8 KB and the startup area is located in the user area. The FCB controls the address based on the startup area select flag (BTFLG) that is located in the configuration area or the AWSC register. The startup area can be locked by the FSPR bit.

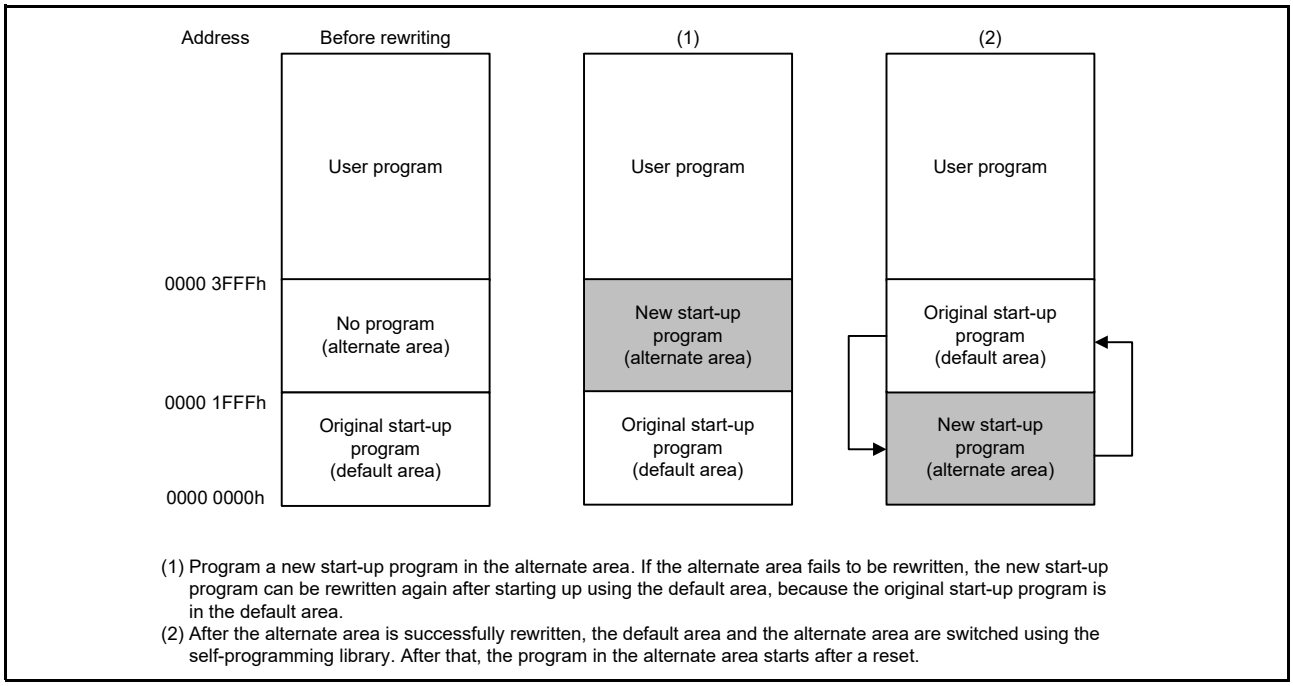


Figure 42.6 Overview of startup program protection

42.4.3 Protection with the Access Window

Issuing the program or block erase command to a flash memory area outside of the access window results in the command-locked state. The access window is only valid in the user area of the code flash memory. The access window provides protection in self-programming, serial programming, and on-chip debug modes.

The access window is specified in both the FAWS[11:0] and the FAWE[11:0] bits. The following describes how to set the FAWS and the FAWE[11:0] bits in different conditions:

- FAWE[11:0] = FAWS[11:0]: The P/E command can execute anywhere in the user area of the code flash memory
- FAWE[11:0] > FAWS[11:0]: The P/E command can only execute in the window from the block pointed to by the FAWS bits to one block lower than the block pointed to by the FAWE[11:0] bits.
- FAWE[11:0] < FAWS[11:0]: The P/E command cannot execute anywhere in the user area of the code flash memory.

Figure 42.7 shows an overview of flash area protection.

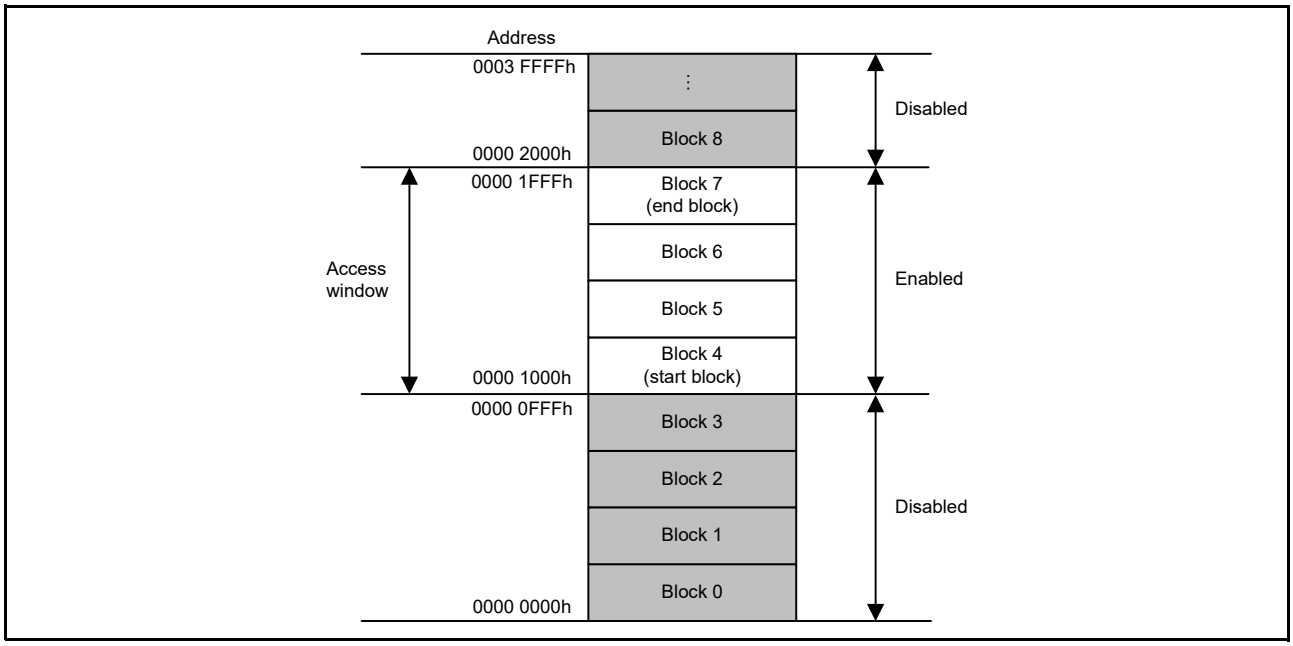


Figure 42.7 Flash area protection overview

42.5 Programming Commands

The FCB controls the programming commands.

42.6 Suspend Operation

The forced stop command forces the blank check or block erase command to stop. When a forced stop is executed, the stopped address values are stored in the registers. The command can restart from the stopped address after a reset to the registers for command execution by copying the saved addresses.

42.7 Protection

The types of protection include:

- Software protection
- Error protection
- Boot program protection.

42.8 Serial Programming Mode

The serial programming mode includes boot mode with SCI9. Table 42.10 lists the I/O pins for the flash memory-related modules.

Table 42.10 I/O pins for flash memory-related modules

Pin name	I/O	Applicable modes	Function
MD	Input	SCI boot mode (serial programming mode)	Selection of operating mode
P110/RXD9	Input	SCI boot mode	For host communication, to receive data through the SCI
P109/TXD9	Output		For host communication, to transmit data through the SCI

42.8.1 SCI Boot Mode

In boot mode, the host sends control commands and data for programming, and the code and data flash memory areas are programmed or erased accordingly. An on-chip SCI handles transfers between the host and the MCU in asynchronous mode. Tools for transmission of control commands and the programming data must be prepared in the host.

When the MCU is activated in boot mode, the embedded program for serial programming is executed. This program automatically adjusts the bit rate of the SCI and controls programming and erasure by receiving control commands from the host.

Figure 42.8 shows the system configuration for operations in boot mode.

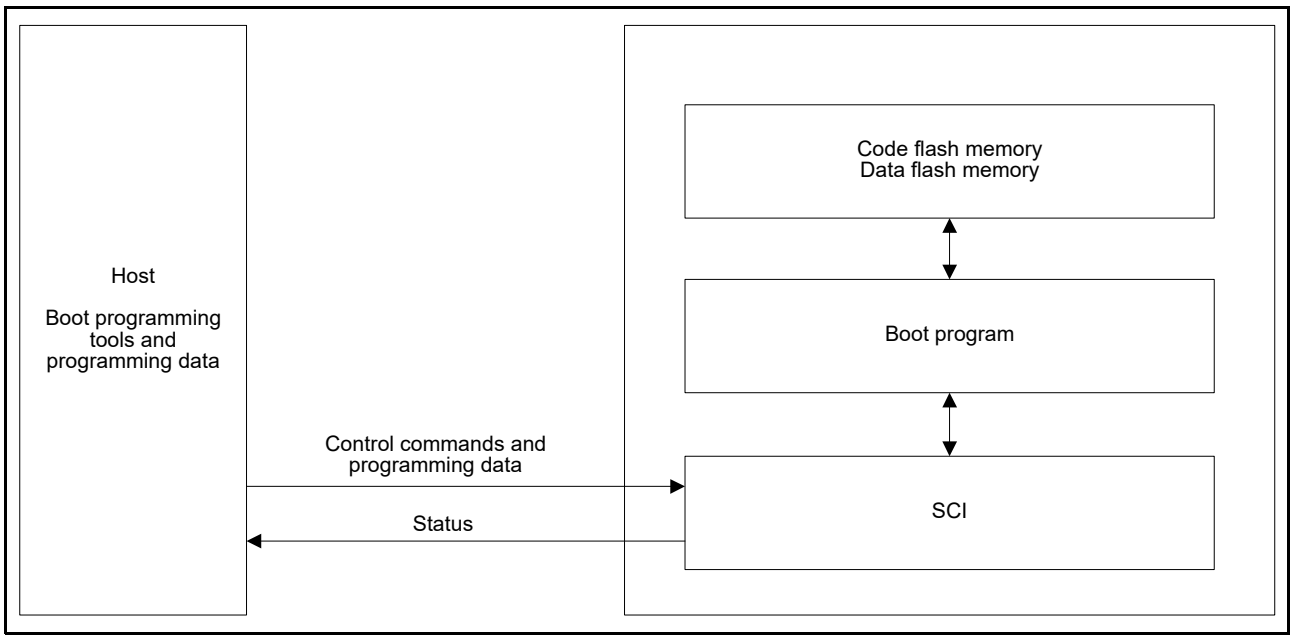


Figure 42.8 System configuration in SCI boot mode

42.9 Using a Serial Programmer

Use a dedicated flash memory programmer to program the flash memory in serial programming mode. The MCU is mounted on the system board for serial programming. A connector to the board enables programming by the flash memory programmer.

Figure 42.9 shows the recommended environment for programming the flash memory of the MCU with data.

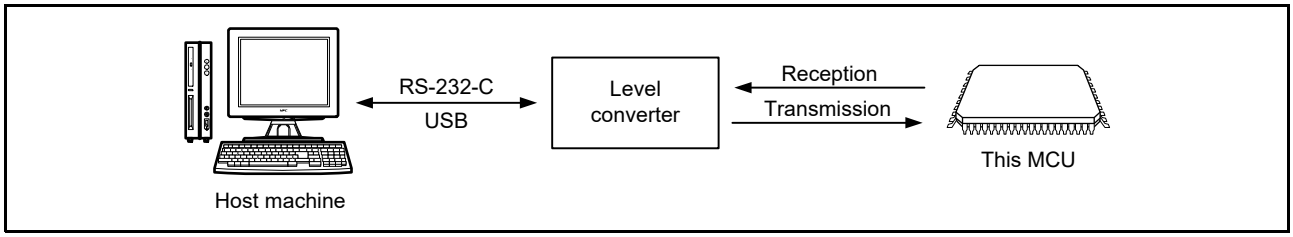


Figure 42.9 Environment for writing programs to the flash memory

42.10 Self-Programming

42.10.1 Overview

The MCU supports programming of the flash memory by the user program itself. The programming commands can be used with user programs for writing to the code and data flash memory. This enables updates to the user programs and overwriting of constant data fields.

The background operation facility makes it possible to execute a program from the code flash memory to program the data flash memory under the conditions shown in Table 42.11. This program can also be copied in advance to and executed from the internal SRAM. When executing from the internal SRAM, this program can also program the code flash memory area.

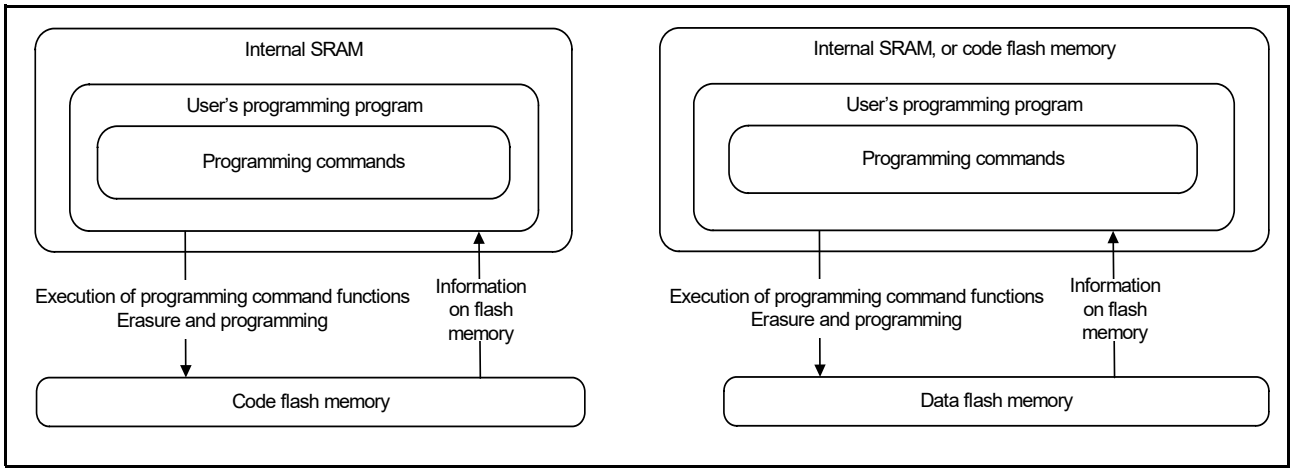


Figure 42.10 Schematic view of self-programming

42.10.2 Background Operation

Background operation can be used when a combination of the flash memory for writing and reading is any of those listed in Table 42.11.

Table 42.11 Conditions under which background operation is available

Product	Range for writing	Range for reading
Common to all products	Data flash memory	Code flash memory

42.11 Reading the Flash Memory

42.11.1 Reading the Code Flash Memory

No special settings are required to read the code flash memory in normal mode. Data can be read through access to addresses in the code flash memory. Values read from code flash memory that was erased but not yet reprogrammed, such as code flash memory in the non-programmed state, are all read as 1s.

42.11.2 Reading the Data Flash Memory

No special settings are required to read the data flash memory in normal mode, except when issuing a reset that causes the data flash access disable mode to disable reading. In this case, the application must transfer back to the data flash read mode. Values read from data flash memory that was erased but not yet reprogrammed, such as data flash memory in the non-programmed state, are all read as 1s.

42.12 Usage Notes

42.12.1 Erase Suspended Area

Data in areas where an erase operation is suspended is undefined. To avoid malfunctions caused by reading undefined data, do not execute commands or read data in an area where erase operation is suspended.

42.12.2 Suspension with Erase Suspend Commands

When suspending an erase operation with the erase suspend command, complete the operation with a resume command.

42.12.3 Constraint on Additional Writes

Other than the configuration area, no other area can be written twice. After a write to a flash memory area is complete, erase the area before attempting to overwrite data in that area. The configuration area can be overwritten.

42.12.4 Reset during Programming and Erasing

If inputting a reset from the RES pin, release the reset after a reset input time of at least tRESW (see section 46, Electrical Characteristics) within the range of the operating voltage defined in the electrical characteristics.

The IWDT reset and software reset do not require a tRESW input time.

42.12.5 Non-maskable Interrupt Disabled during Programming and Erasing

Do not enable non-maskable interrupts*1 during program and erase operations in the code flash memory. When a non-maskable interrupt occurs during a program or erase operation, the vectors are fetched from the code flash memory, and undefined data is read. This constraint only applies to the code flash memory.

Note 1. A non-maskable interrupts is an NMI pin interrupt, oscillation stop detection interrupt, WDT underflow or refresh error, IWDT underflow or refresh error, voltage monitor 1 interrupt, voltage monitor 2 interrupt, SRAM parity error, SRAM ECC error, MPU bus slave error, MPU bus master error, or CPU stack pointer monitor.

42.12.6 Location of Interrupt Vectors during Programming and Erasing

When an interrupt occurs during program and erase operations, the vector can be fetched from the code flash memory. To avoid fetching the vector from the code flash memory, set the fetching destination to an area other than the code flash memory with the interrupt table.

42.12.7 Programming and Erasing in Low-Speed Operating Mode

Do not program or erase the flash memory when low-speed operating mode is selected in the SOPCCR register for low-power consumption functions.

42.12.8 Abnormal Termination during Programming and Erasing

When the voltage exceeds the range of the operating voltage during program or erase operation, or when a program or erase operation did not complete successfully because of a reset or prohibited actions as described in section 42.12.9, Actions Prohibited during Programming and Erasing, erase the area again.

42.12.9 Actions Prohibited during Programming and Erasing

To prevent damage to the flash memory, comply with the following constraints during programming and erasing:

- Do not use an MCU power supply that is outside the operating voltage range
- Do not update the OPCCR.OPCM[1:0] bit value
- Do not update the SOPCCR.SOPCM bit value
- Do not change the division ratio of the flash interface clock (ICLK)
- Do not place the MCU in Software Standby mode
- Do not access the data flash memory during a program or erase operation to the code flash memory
- Do not update the DFLCTL.DFLEN bit value during a program or erase operation to the data flash memory.

43. AES Engine

Regarding the public release of this information, a non-disclosure agreement is required. For details, contact your Renesas sales office.

44. True Random Number Generator (TRNG)

Regarding the public release of this information, a non-disclosure agreement is required. For details, contact your Renesas sales office.

45. Internal Voltage Regulator

45.1 Overview

The MCU includes a linear regulator (LDO) that supplies voltage to the internal circuit and memory, except for I/O and the analog domain.

45.2 Operation

Table 45.1 lists the LDO mode pin settings, and Figure 45.1 shows the LDO mode settings. The internal voltage is generated from VCC.

Table 45.1 LDO mode pin settings

Pin	Settings
All VCC pins	• Connect each pin to the system power supply. • Connect each pin to VSS with a 0.1-µF multilayer ceramic capacitor. Place the capacitor close to the pin.
VCL pin	• Connect each pin to VSS with a 4.7-µF multilayer ceramic capacitor. Place the capacitor close to the pin.

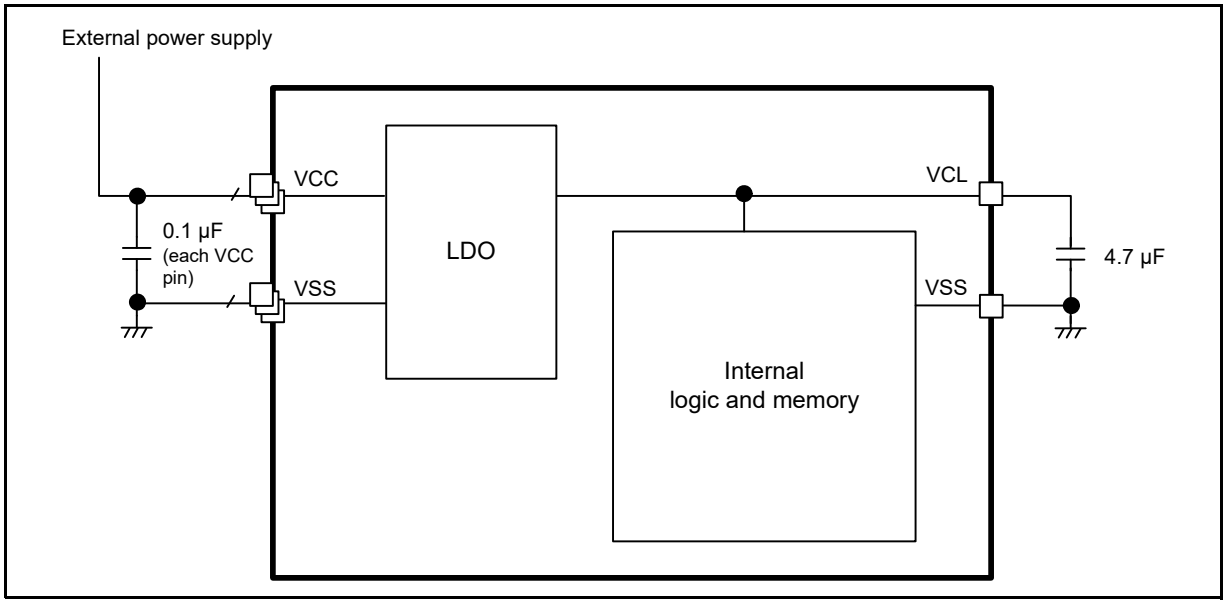


Figure 45.1 LDO mode settings

46. Electrical Characteristics

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

VCC*1 = AVCC0 = VCC_USB*2 = VCC_USB_LDO*2 = 1.6 to 5.5V, VREFH0 = 1.6 to AVCC0,

VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, Ta = T_{opr}

Note 1. The typical condition is set to VCC = 3.3V.
Note 2. When USBFS is not used.

Figure 46.1 shows the timing conditions.

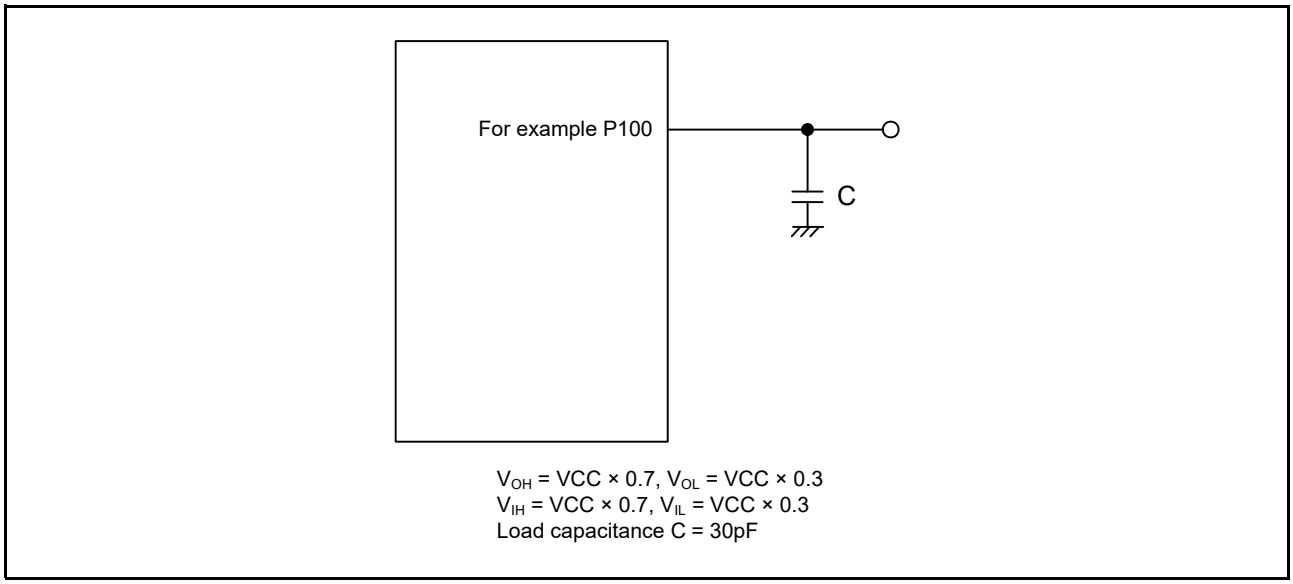


Figure 46.1 Input or output timing measurement conditions

The measurement conditions of the timing specifications for each peripheral are recommended for the best peripheral operation. However, make sure to adjust driving abilities for each pin to meet the conditions of your system.

Each function pin used for the same function must select the same drive ability. If the I/O drive ability of each function pin is mixed, the A/C specification of each function is not guaranteed.

46.1 Absolute Maximum Ratings

Table 46.1 Absolute maximum ratings

Parameter		Symbol	Value	Unit
Power supply voltage		VCC	-0.5 to +6.5	V
Input voltage	5 V tolerant ports*1	V_{in}	-0.3 to +6.5	V
	P000 to P004 P010 to P015 P500 to P502	V_{in}	-0.3 to AVCC0 + 0.3	V
	Others	V_{in}	-0.3 to VCC + 0.3	V
Reference power supply voltage		VREFH0	-0.3 to +6.5	V
Analog power supply voltage		AVCC0	-0.5 to +6.5	V
USB power supply voltage		VCC_USB	-0.5 to +6.5	V
		VCC_USB_LDO	-0.5 to +6.5	V
Analog input voltage	When AN000 to AN013 are used	V_{AN}	-0.3 to AVCC0 + 0.3	V
	When AN016 to AN022 are used		-0.3 to VCC + 0.3	V
Operating temperature*2 *3		T_{opr}	-40 to +85 -40 to +105	°C
Storage temperature		T_{stg}	-55 to +125	°C

Note: Contact Renesas Electronics sales office for information on derating operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for improved reliability.

Note 1. Ports P205, P206, P400, P401, and P407 are 5V-tolerant.
Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up might cause malfunction and the abnormal current that passes in the device at this time might cause degradation of internal elements.

Note 2. See section 46.2.1, Tj/Ta Definition.

Note 3. The upper limit of the operating temperature is 85°C or 105°C, depending on the product. For details, see section 1.3, Part Numbering.

Caution: Permanent damage to the MCU might result if absolute maximum ratings are exceeded.
To preclude any malfunctions due to noise interference, insert capacitors of high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, between the VCC_USB and VSS_USB pins, and between the VREFH0 and VREFL0 pins. Place capacitors of about 0.1 µF as close as possible to every power supply pin and use the shortest and heaviest possible traces. Also, connect capacitors as stabilization capacitance.
Connect the VCL pin to a VSS pin by a 4.7-µF capacitor. The capacitor must be placed close to the pin.

Table 46.2 Recommended operating conditions

Parameter	Symbol	Value	Min	Typ	Max	Unit
Power supply voltages	VCC*1, *2	When USBFS is not used	1.6	-	5.5	V
		When USBFS is used USB Regulator Disable	VCC_USB	-	3.6	V
		When USBFS is used USB Regulator Enable	VCC_USB _LDO	-	5.5	V
	VSS		-	0	-	V
USB power supply voltages	VCC_USB	When USBFS is not used	-	VCC	-	V
		When USBFS is used USB Regulator Disable (Input)	3.0	3.3	3.6	V
	VCC_USB_LDO	When USBFS is not used	-	VCC	-	V
		When USBFS is used USB Regulator Disable	-	VCC	-	V
		When USBFS is used USB Regulator Enable	3.8	-	5.5	V
	VSS_USB		-	0	-	V
Analog power supply voltages	AVCC0*1, *2		1.6	-	5.5	V
	AVSS0		-	0	-	V
	VREFH0	When used as ADC14 Reference	1.6	-	AVCC0	V
	VREFL0		-	0	-	V

Note 1. Use AVCC0 and VCC under the following conditions:
AVCC0 and VCC can be set individually within the operating range when VCC ≥ 2.2 V and AVCC0 ≥ 2.2 V.
AVCC0 = VCC when VCC < 2.2 V or AVCC0 < 2.2 V.

Note 2. When powering on the VCC and AVCC0 pins, power them on at the same time or the VCC pin first and then the AVCC0 pin.

46.2 DC Characteristics

46.2.1 Tj/Ta Definition

Table 46.3 DC characteristics
Conditions: Products with operating temperature (T_a) -40 to +105°C

Parameter	Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	Tj	-	125	°C	High-speed mode Middle-speed mode Low-voltage mode Low-speed mode SubOSC-speed mode
			105*1		

Note: Make sure that Tj = T_a + θja × total power consumption (W), where total power consumption = (VCC - V_{OH}) × ΣI_{OH} + V_{OL} × ΣI_{OL} + I_{CC}max × VCC.

Note 1. The upper limit of operating temperature is 85°C or 105°C, depending on the product. For details, see section 1.3, Part Numbering. If the part number shows an operation temperature to 85°C, then Tj max is 105°C, otherwise, it is 125°C.

46.2.2 I/O V_{IH}, V_{IL}

Table 46.4 I/O V_{IH}, V_{IL} (1)
Conditions: VCC = AVCC0 = VCC_USB = VCC_USB_LDO = 2.7 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	IIC (except for SMBus)*1	V_{IH}	VCC × 0.7	-	5.8	V	-
		V_{IL}	-	-	VCC × 0.3		
		ΔV_T	VCC × 0.05	-	-		
	RES, NMI Other peripheral input pins excluding IIC	V_{IH}	VCC × 0.8	-	-		
		V_{IL}	-	-	VCC × 0.2		
		ΔV_T	VCC × 0.1	-	-		
Input voltage (except for Schmitt trigger input pin)	IIC (SMBus)*2	V_{IH}	2.2	-	-		VCC = 3.6 to 5.5 V
		V_{IH}	2.0	-	-		VCC =2.7 to 3.6 V
		V_{IL}	-	-	0.8		-
	5V-tolerant ports*3	V_{IH}	VCC × 0.8	-	5.8		
		V_{IL}	-	-	VCC × 0.2		
	P000 to P004 P010 to P015 P500 to P502	V_{IH}	AVCC0 × 0.8	-	-		
		V_{IL}	-	-	AVCC0 × 0.2		
	P914, P915	V_{IH}	VCC_USB × 0.8	-	VCC_USB + 0.3		
		V_{IL}	-	-	VCC_USB × 0.2		
	EXTAL Input ports pins except for P000 to P004, P010 to P015, P500 to P502, P914, P915	V_{IH}	VCC × 0.8	-	-		
		V_{IL}	-	-	VCC × 0.2		

Note 1. SCL0_A, SDA0_A, SDA0_B, SCL1_A, SDA1_A (total 5 pins)
Note 2. SCL0_A, SDA0_A, SCL0_B, SDA0_B, SCL0_C, SCL1_A, SDA1_A, SCL1_B, SDA1_B (total 9 pins)
Note 3. P205, P206, P400, P401, P407 (total 5pins)

Table 46.5 I/O V_{IH}, V_{IL} (2)
Conditions: VCC = AVCC0 = VCC_USB = VCC_USB_LDO = 1.6 to 2.7 V

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	RES, NMI Peripheral input pins	V_{IH}	VCC × 0.8	-	-	V	-
		V_{IL}	-	-	VCC × 0.2		
		ΔV_T	VCC × 0.01	-	-		
Input voltage (except for Schmitt trigger input pin)	5V-tolerant ports*1	V_{IH}	VCC × 0.8	-	5.8		
		V_{IL}	-	-	VCC × 0.2		
	P000 to P004 P010 to P015 P500 to P502	V_{IH}	AVCC0 × 0.8	-	-		
		V_{IL}	-	-	AVCC0 × 0.2		
	P914, P915	V_{IH}	VCC_USB × 0.8	-	VCC_USB + 0.3		
		V_{IL}	-	-	VCC_USB × 0.2		
	EXTAL Input ports pins except for P000 to P004, P010 to P015, P500 to P502, P914, P915	V_{IH}	VCC × 0.8	-	-		
		V_{IL}	-	-	VCC × 0.2		

Note 1. P205, P206, P400, P401, P407 (total 5pins)

46.2.3 I/O I_{OH}, I_{OL}

Table 46.6 I/O I_{OH}, I_{OL}

Conditions: VCC = AVCC0 = VCC_USB = VCC_USB_LDO = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit
Permissible output current (average value per pin)	Ports P000 to P004, P010 to P015, P212, P213, P500 to P502	-	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
	Ports P408, P409	Low drive*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2 VCC = 2.7 to 3.0 V	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
		Middle drive*2 VCC = 3.0 to 5.5 V	I_{OH}	-	-	-20.0	mA
			I_{OL}	-	-	20.0	mA
	Ports P914, P915		I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
	Other output pins*3	Low drive*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
Permissible output current (max value per pin)	Ports P000 to P004, P010 to P015, P212, P213, P500 to P502	-	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
	Ports P408, P409	Low drive*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2 VCC = 2.7 to 3.0 V	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
		Middle drive*2 VCC = 3.0 to 5.5 V	I_{OH}	-	-	-20.0	mA
			I_{OL}	-	-	20.0	mA
	Ports P914, P915		I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
	Other output pins*3	Low drive*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
Permissible output current (max value total pins)	Total of ports P000 to P004, P010 to P015, P500 to P502		$\Sigma I_{OH\ (max)}$	-	-	-30	mA
			$\Sigma I_{OL\ (max)}$	-	-	30	mA
	Total of ports P914, P915		ΣI_{OH}	-	-	-4.0	mA
			ΣI_{OL}	-	-	4.0	mA
	Total of all output pin		$\Sigma I_{OH\ (max)}$	-	-	-60	mA
			$\Sigma I_{OL\ (max)}$	-	-	60	mA

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in this table. The average output current indicates the average value of current measured during 100 µs.

Note 1. This is the value when low driving ability is selected with the Port Drive Capability bit in the PmnPFS register.

Note 2. This is the value when middle driving ability is selected with the Port Drive Capability bit in the PmnPFS register.

Note 3. Except for Ports P200, P214, P215, which are input ports.

46.2.4 I/O V_{OH}, V_{OL}, and Other Characteristics

Table 46.7 I/O V_{OH}, V_{OL} (1)
Conditions: VCC = AVCC0 = VCC_USB = VCC_USB_LDO = 4.0 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	IIC*1, *2		V_{OL}	-	-	0.4	V	I_{OL} = 3.0 mA
			V_{OL}	-	-	0.6		I_{OL} = 6.0 mA
	Ports P408, P409*2, *3		V_{OH}	VCC - 1.0	-	-		I_{OH} = -20.0 mA
			V_{OL}	-	-	1.0		I_{OL} = 20 mA
	Ports P000 to P004, P010 to P015, P500 to P502	Low drive	V_{OH}	AVCC0 - 0.8	-	-		I_{OH} = -2.0 mA
			V_{OL}	-	-	0.8		I_{OL} = 2.0 mA
		Middle drive	V_{OH}	AVCC0 - 0.8	-	-		I_{OH} = -4.0 mA
			V_{OL}	-	-	0.8		I_{OL} = 4.0 mA
	Ports P914, P915		V_{OH}	VCC_USB - 0.8	-	-		I_{OH} = -2.0 mA
			V_{OL}	-	-	0.8		I_{OL} = 2.0 mA
	Other output pins*4	Low drive	V_{OH}	VCC - 0.8	-	-		I_{OH} = -2.0 mA
			V_{OL}	-	-	0.8		I_{OL} = 2.0 mA
		Middle drive*5	V_{OH}	VCC - 0.8	-	-		I_{OH} = -4.0 mA
			V_{OL}	-	-	0.8		I_{OL} = 4.0 mA

Note 1. SCL0_A, SDA0_A, SCL0_B, SDA0_B, SCL0_C, SCL1_A, SDA1_A, SCL1_B, SDA1_B (total 9 pins).
Note 2. This is the value when middle driving ability is selected with the Port Drive Capability bit in the PmnPFS register.
Note 3. Based on characterization data, not tested in production.
Note 4. Except for Ports P200, P214, P215, which are input ports.
Note 5. Except for P212, P213.

Table 46.8 I/O V_{OH}, V_{OL} (2)
Conditions: VCC = AVCC0 = VCC_USB = VCC_USB_LDO = 2.7 to 4.0 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	IIC*1, *2		V_{OL}	-	-	0.4	V	I_{OL} = 3.0 mA
			V_{OL}	-	-	0.6		I_{OL} = 6.0 mA
	Ports P408, P409*2, *3		V_{OH}	VCC - 1.0	-	-		I_{OH} = -20.0 mA VCC = 3.3 V
			V_{OL}	-	-	1.0		I_{OL} = 20 mA VCC = 3.3 V
	Ports P000 to P004, P010 to P015, P500 to P502	Low drive	V_{OH}	AVCC0 - 0.5	-	-		I_{OH} = -1.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 1.0 mA
		Middle drive	V_{OH}	AVCC0 - 0.5	-	-		I_{OH} = -2.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 2.0 mA
	Ports P914, P915		V_{OH}	VCC_USB - 0.5	-	-		I_{OH} = -1.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 1.0 mA
	Other output pins*4	Low drive	V_{OH}	VCC - 0.5	-	-		I_{OH} = -1.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 1.0 mA
		Middle drive*5	V_{OH}	VCC - 0.5	-	-		I_{OH} = -2.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 2.0 mA

Note 1. SCL0_A, SDA0_A, SCL0_B, SDA0_B, SCL0_C, SCL1_A, SDA1_A, SCL1_B, SDA1_B (total 9 pins).
Note 2. This is the value when middle driving ability is selected with the Port Drive Capability bit in the PmnPFS register.
Note 3. Based on characterization data, not tested in production.

Note 4. Except for Ports P200, P214, P215, which are input ports.
Note 5. Except for P212, P213.

Table 46.9 I/O V_{OH}, V_{OL} (3)
Conditions: VCC = AVCC0 = VCC_USB = VCC_USB_LDO = 1.6 to 2.7 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	Ports P000 to P004, P010 to P015, P500 to P502	Low drive	V_{OH}	AVCC0 - 0.3	-	-	V	I_{OH} = -0.5 mA
			V_{OL}	-	-	0.3		I_{OL} = 0.5 mA
		Middle drive	V_{OH}	AVCC0 - 0.3	-	-		I_{OH} = -1.0 mA
			V_{OL}	-	-	0.3		I_{OL} = 1.0 mA
	Ports P914, P915		V_{OH}	VCC_USB - 0.3	-	-		I_{OH} = -0.5 mA
			V_{OL}	-	-	0.3		I_{OL} = 0.5 mA
	Other output pins*1	Low drive	V_{OH}	VCC - 0.3	-	-		I_{OH} = -0.5 mA
			V_{OL}	-	-	0.3		I_{OL} = 0.5 mA
		Middle drive*2	V_{OH}	VCC - 0.3	-	-		I_{OH} = -1.0 mA
			V_{OL}	-	-	0.3		I_{OL} = 1.0 mA

Note 1. Except for Ports P200, P214, P215, which are input ports.
Note 2. Except for P212, P213.

Table 46.10 I/O other characteristics
Conditions: VCC = AVCC0 = VCC_USB = VCC_USB_LDO = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	RES, Ports P200, P214, P215	$\lvert I_{in} \rvert$	-	-	1.0	μA	V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	5V-tolerant ports	$\lvert I_{TSI} \rvert$	-	-	1.0	μA	V_{in} = 0 V V_{in} = 5.8 V
	Other ports		-	-	1.0		V_{in} = 0 V V_{in} = VCC
Input pull-up resistor	All ports (except for P200, P214, P215, P914, P915)	R_U	10	20	50	kΩ	V_{in} = 0 V
Input capacitance	USB_DP, USB_DM, P200	C_{in}	-	-	30	pF	V_{in} = 0 V f = 1 MHz T_a = 25°C
	Other input pins		-	-	15		

46.2.5 Output Characteristics for I/O Pins (Low Drive Capacity)

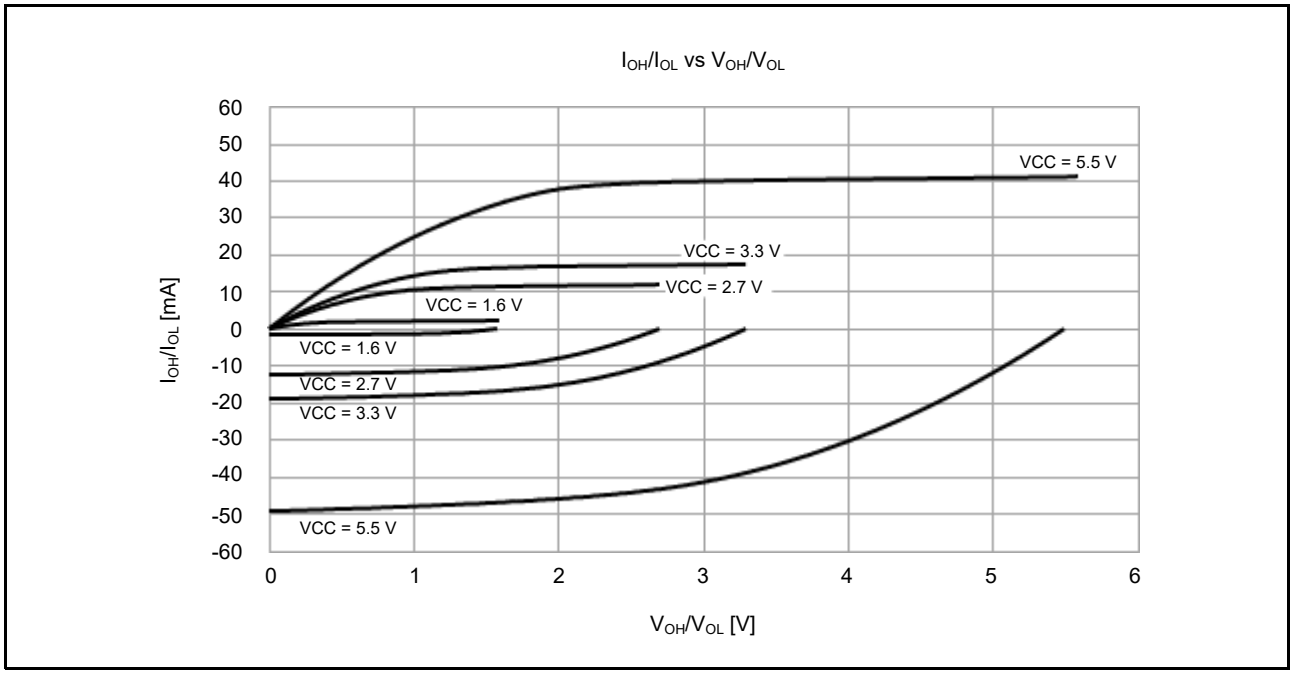


Figure 46.2 V_{OH}/V_{OL} and I_{OH}/I_{OL} voltage characteristics at Ta = 25°C when low drive output is selected (reference data, except for P914 and P915)

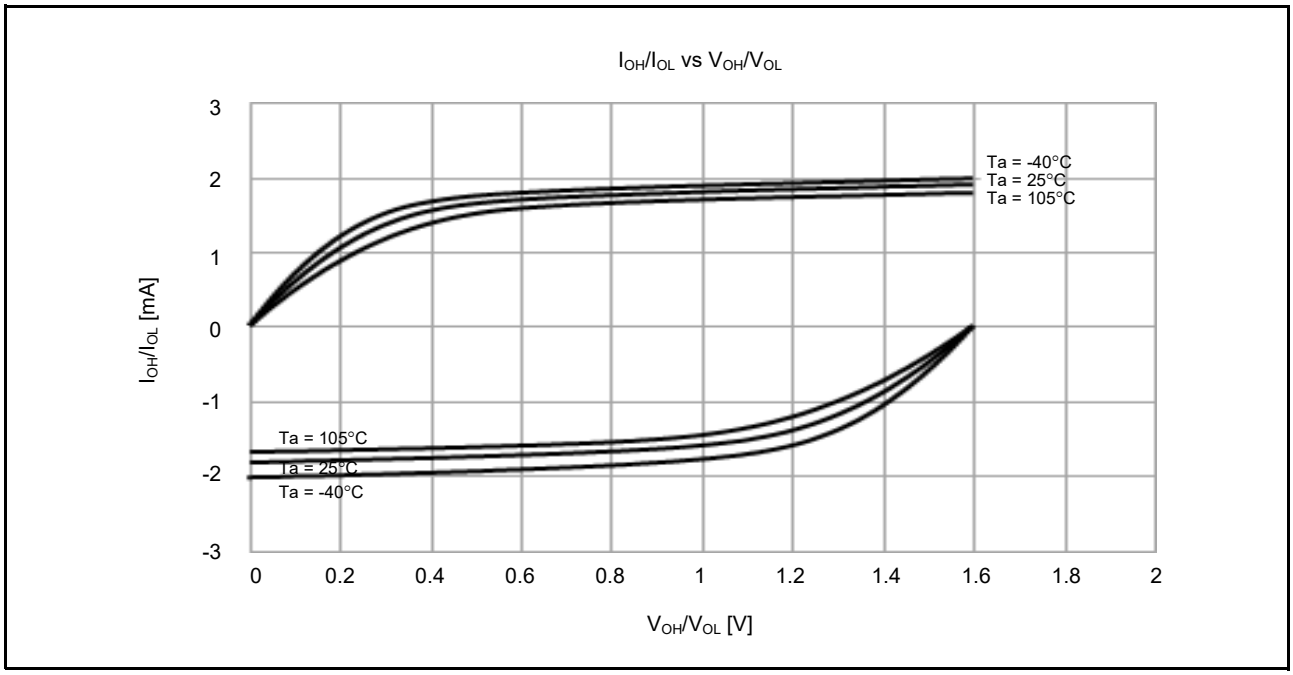


Figure 46.3 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 1.6 V when low drive output is selected (reference data, except for P914 and P915)**

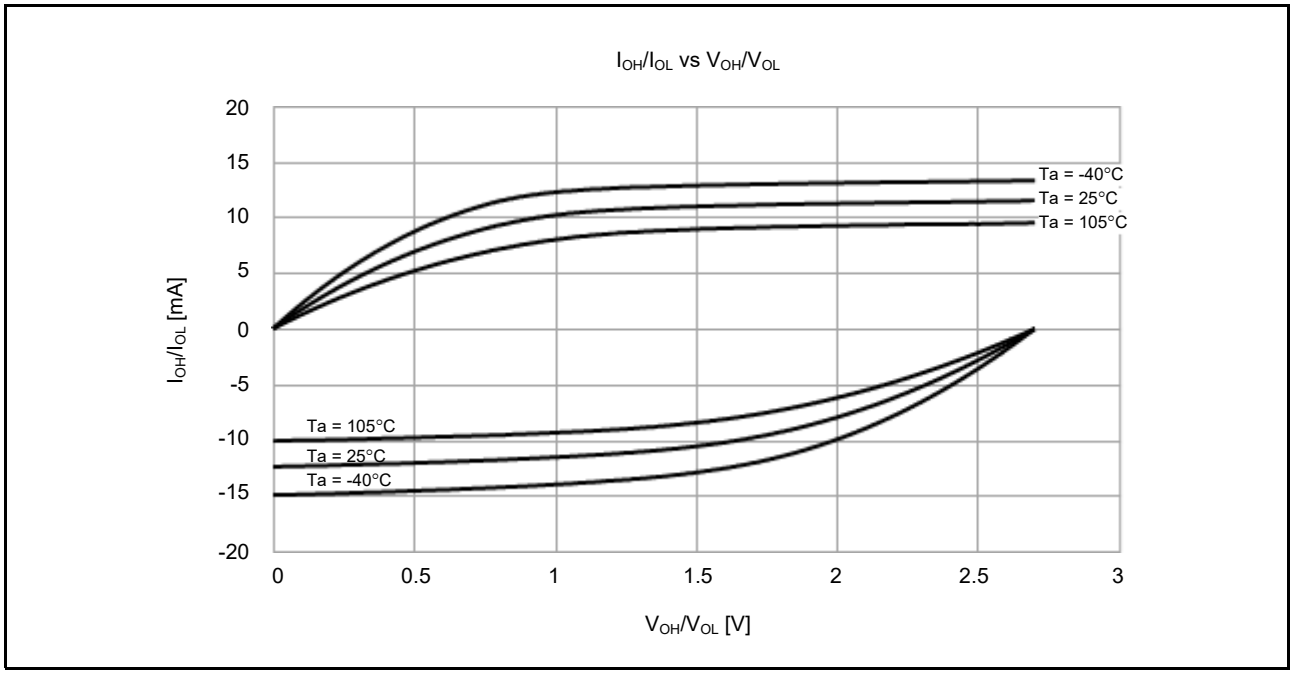


Figure 46.4 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 2.7 V when low drive output is selected (reference data, except for P914 and P915)**

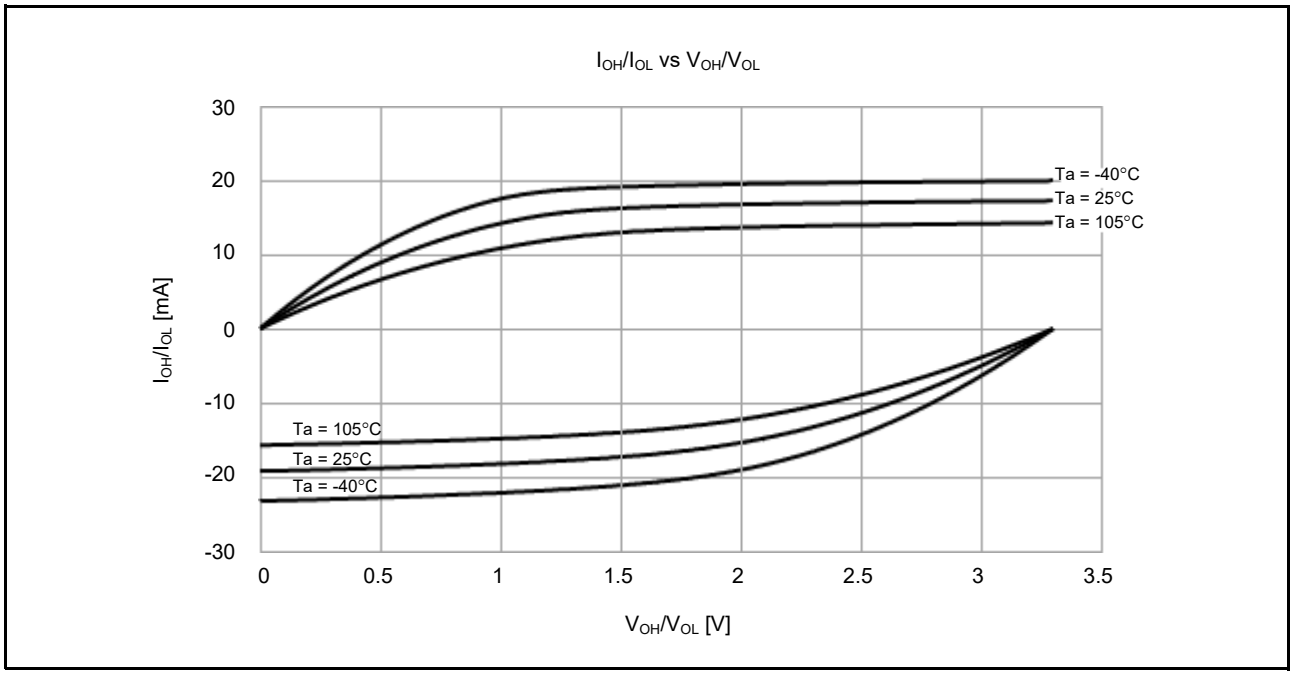


Figure 46.5 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 3.3 V when low drive output is selected (reference data, except for P914 and P915)**

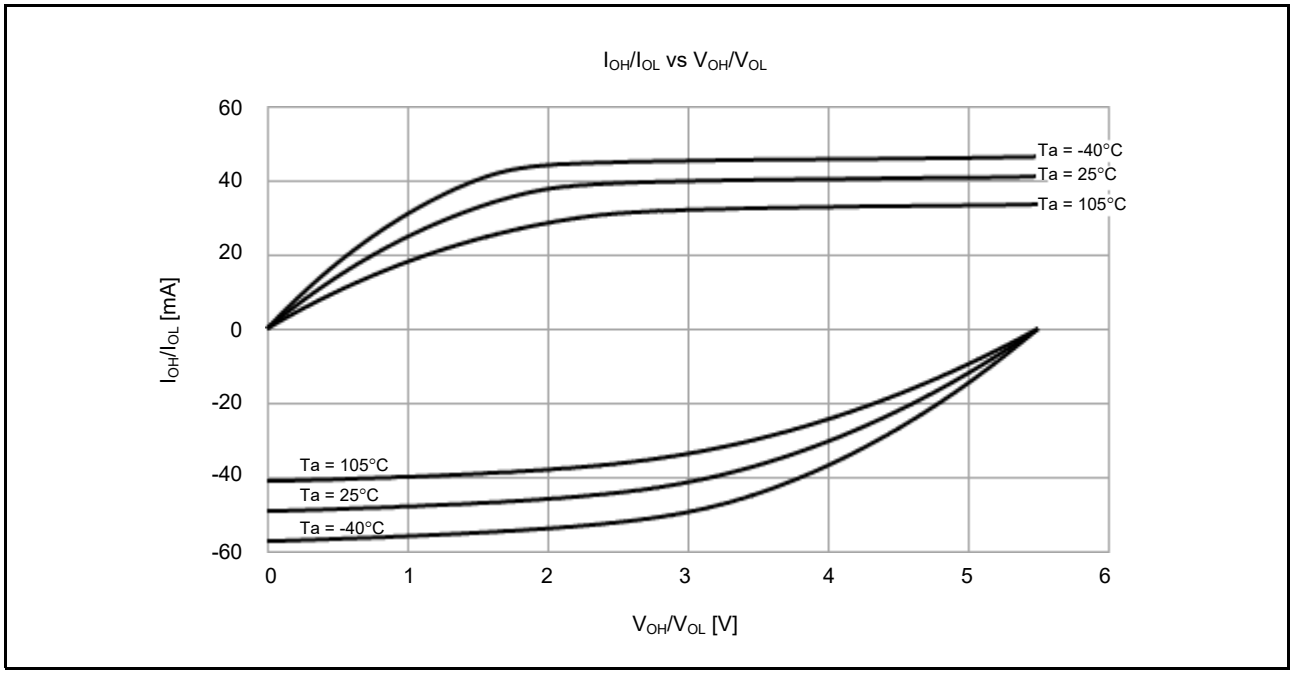


Figure 46.6 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 5.5 V when low drive output is selected (reference data, except for P914 and P915)**

46.2.6 Output Characteristics for I/O Pins (Middle Drive Capacity)

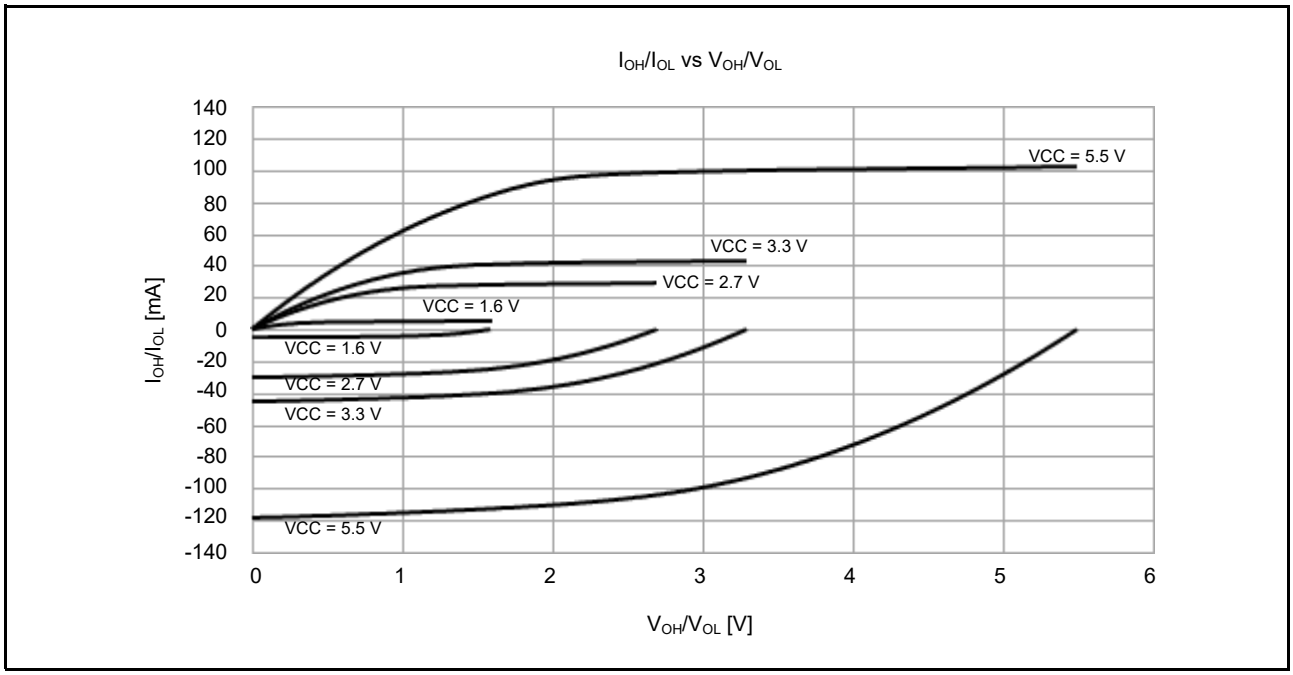


Figure 46.7 **V_{OH}/V_{OL} and I_{OH}/I_{OL} voltage characteristics at Ta = 25°C when middle drive output is selected (reference data, except for P914 and P915)**

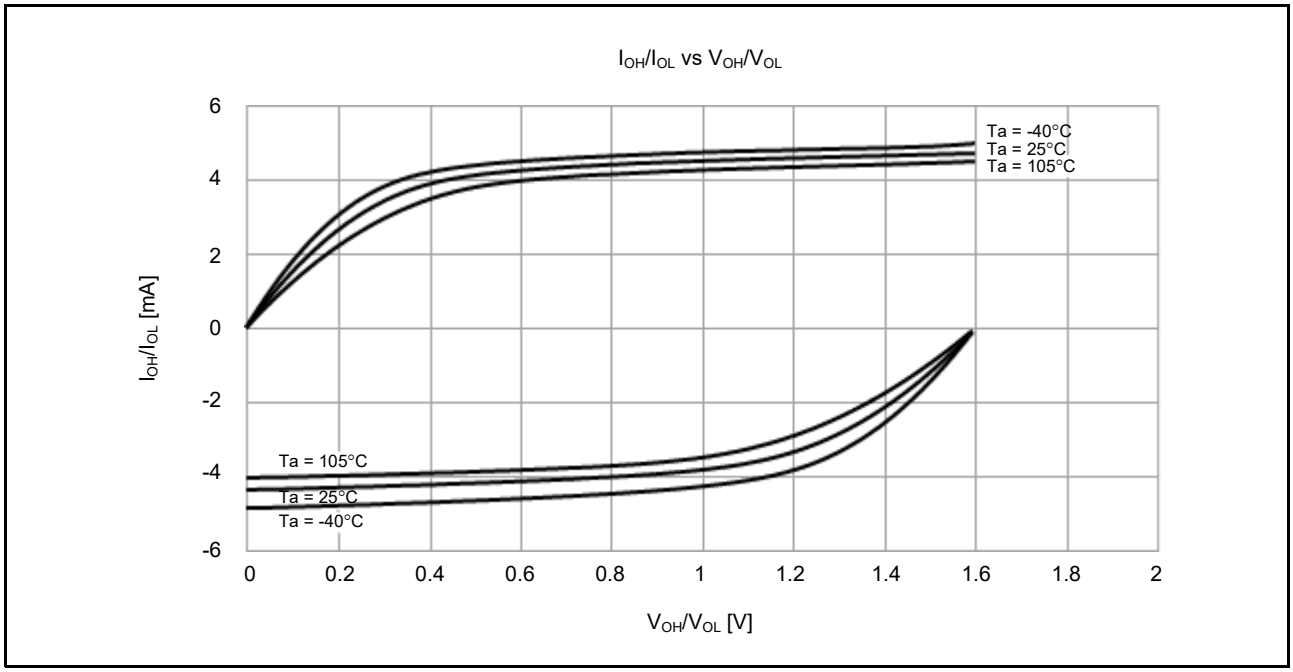


Figure 46.8 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 1.6 V when middle drive output is selected (reference data, except for P914 and P915)**

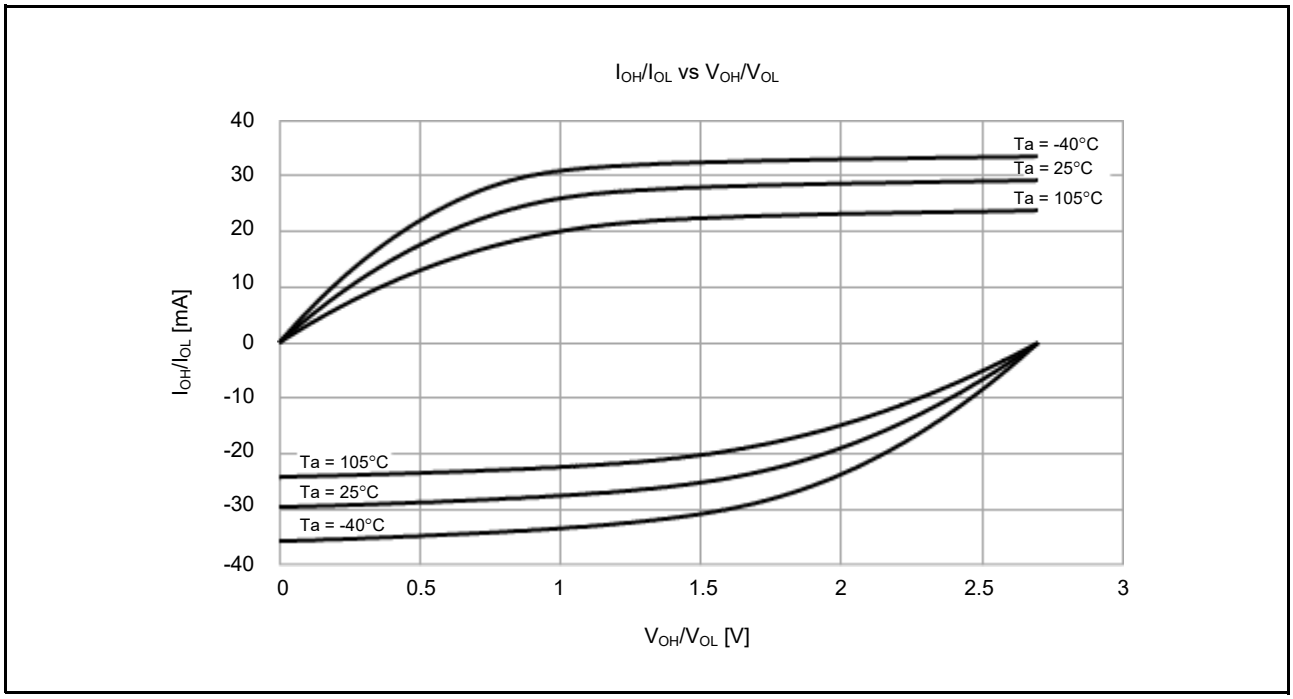


Figure 46.9 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 2.7 V when middle drive output is selected (reference data, except for P914 and P915)**

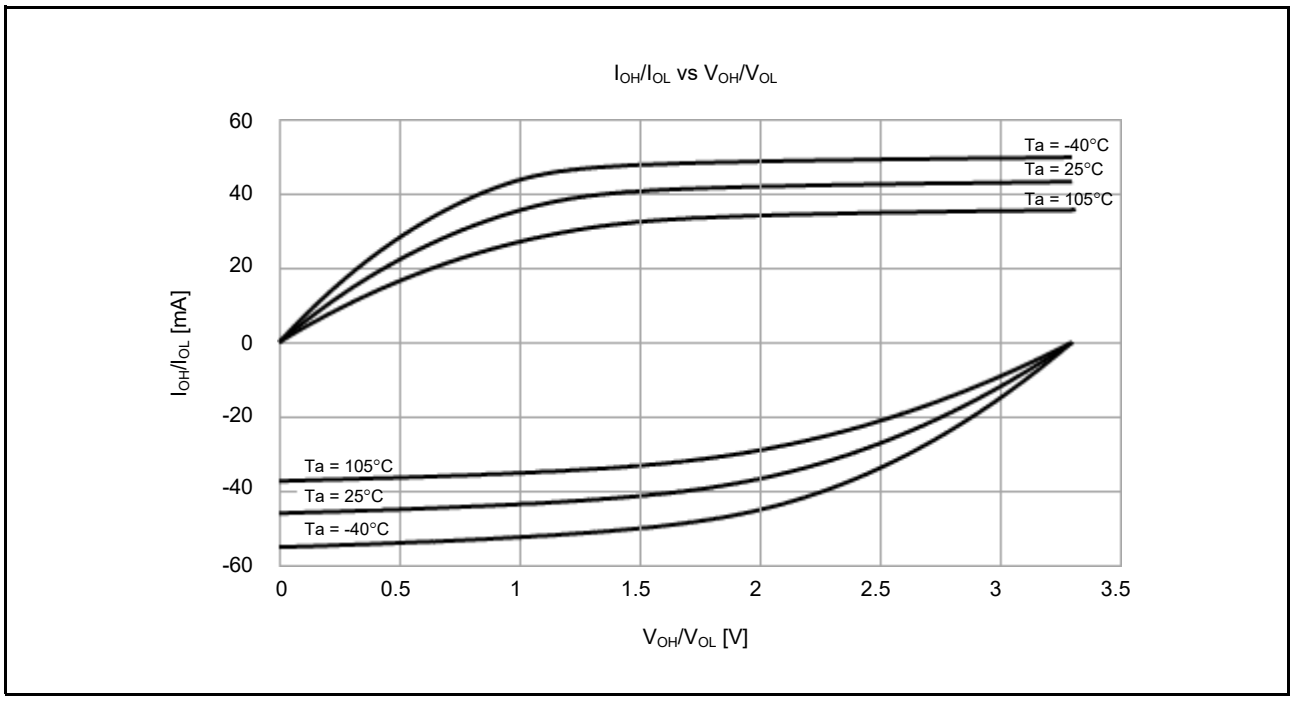


Figure 46.10 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 3.3 V when middle drive output is selected (reference data, except for P914 and P915)**

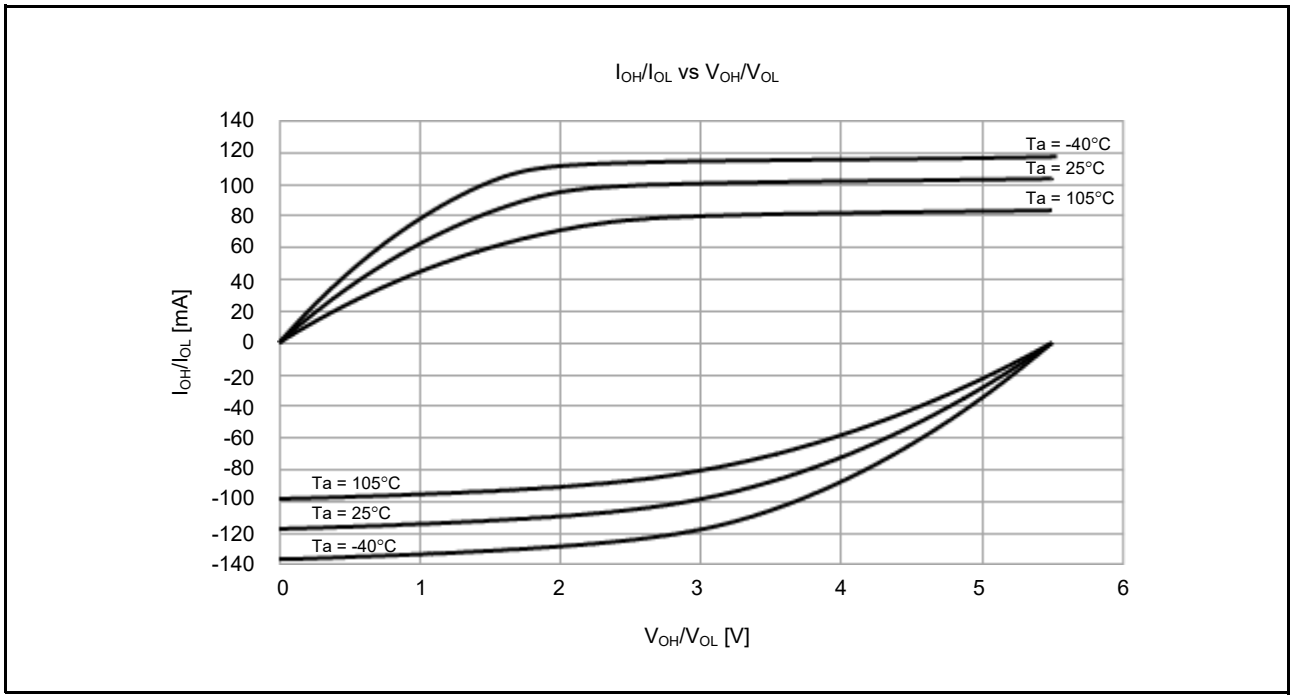


Figure 46.11 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 5.5 V when middle drive output is selected (reference data, except for P914 and P915)**

46.2.7 Output Characteristics for P408 and P409 I/O Pins (Middle Drive Capacity)

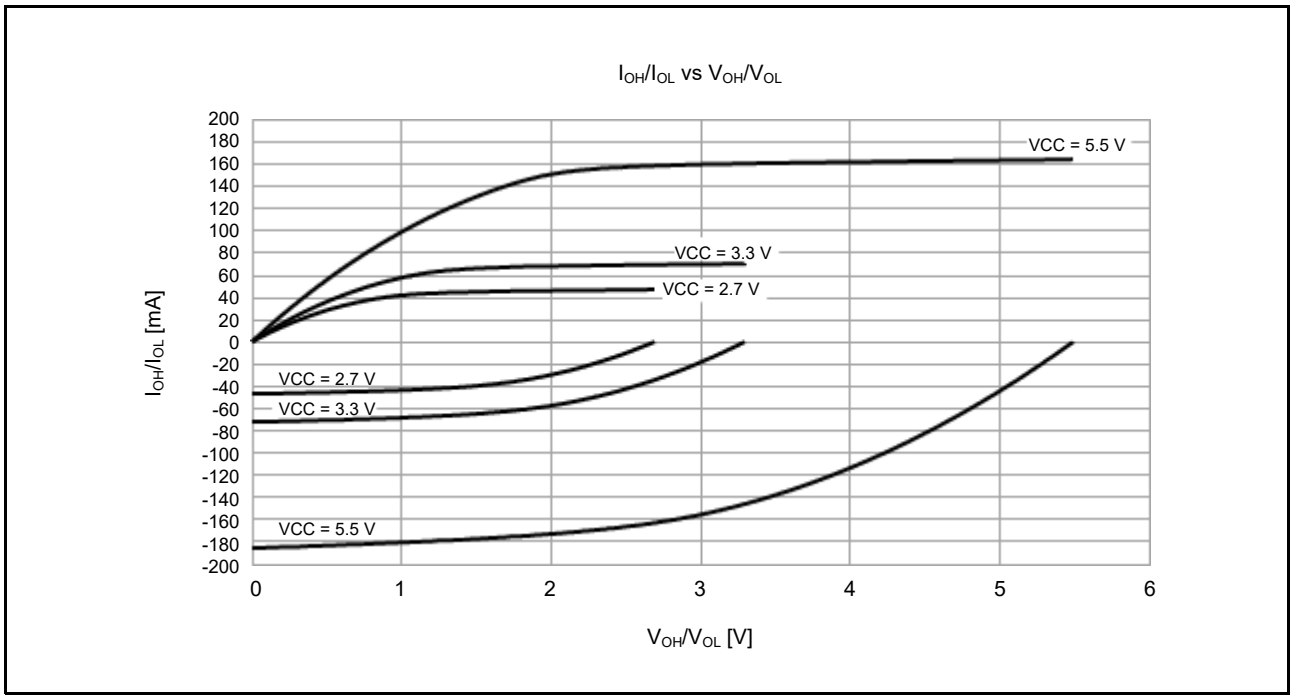


Figure 46.12 **V_{OH}/V_{OL} and I_{OH}/I_{OL} voltage characteristics at Ta = 25°C when middle drive output is selected (reference data)**

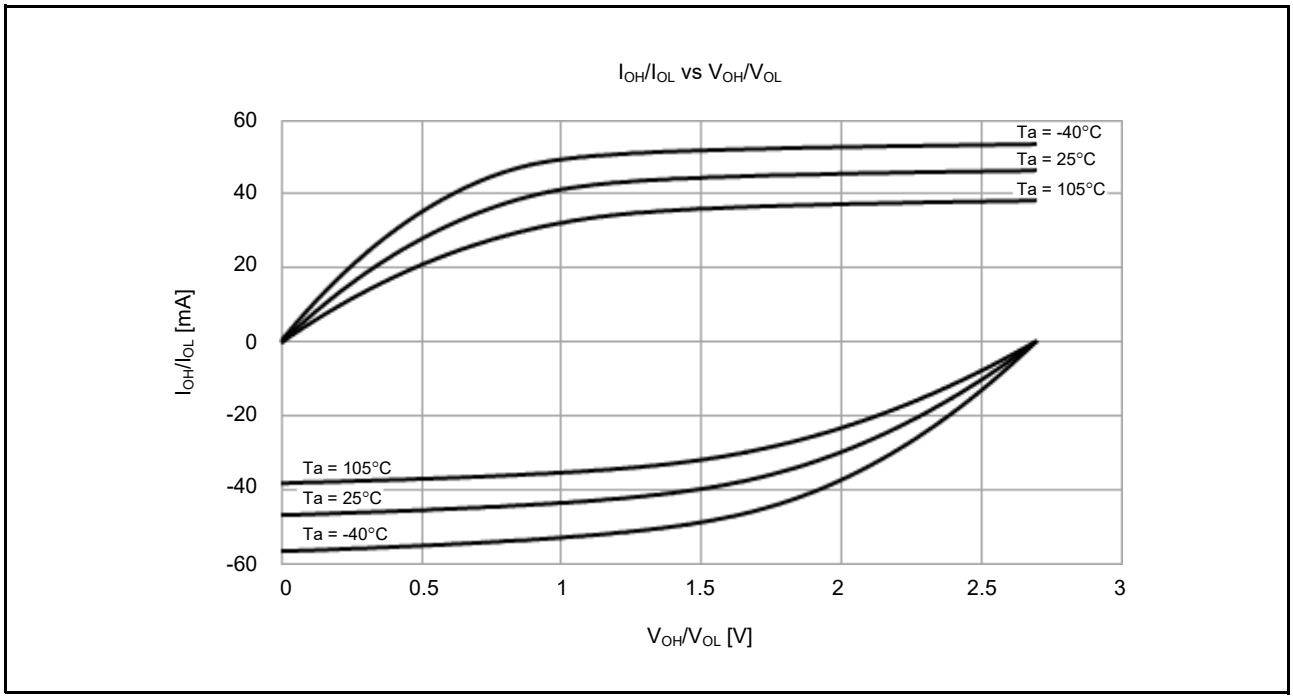


Figure 46.13 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 2.7 V when middle drive output is selected (reference data)**

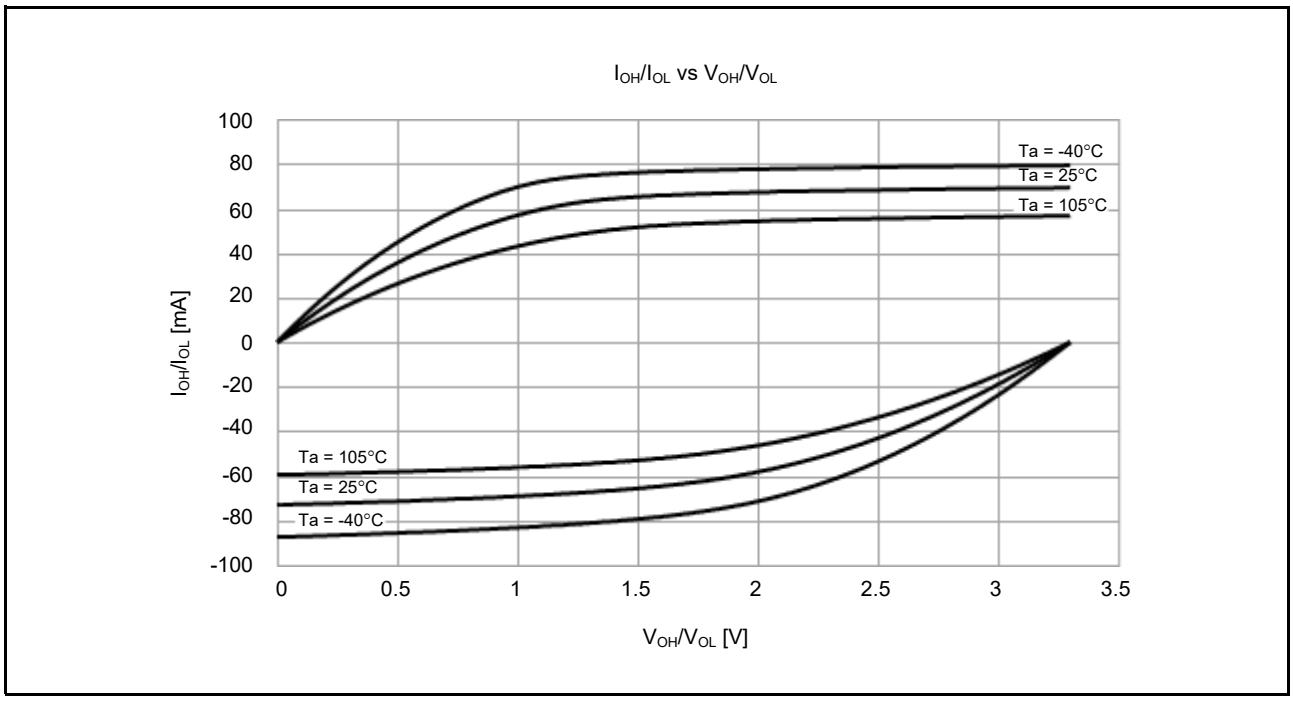


Figure 46.14 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 3.3 V when middle drive output is selected (reference data)**

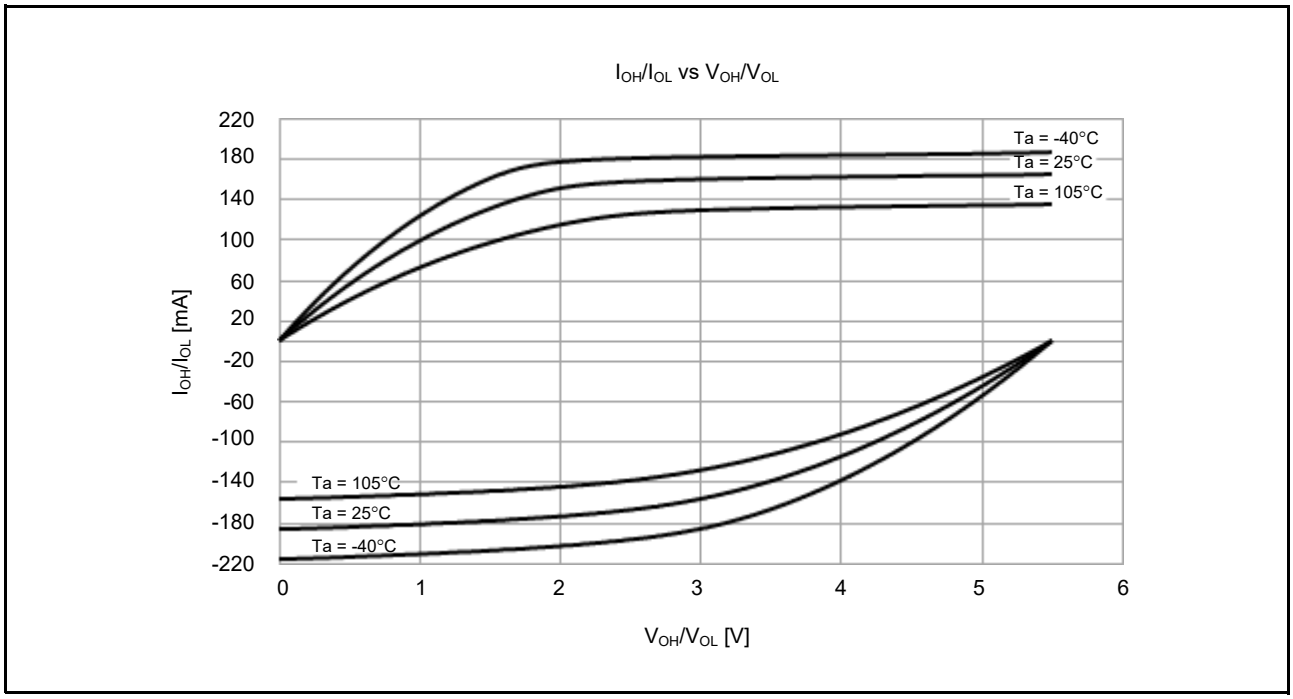


Figure 46.15 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 5.5 V when middle drive output is selected (reference data)**

46.2.8 Output Characteristics for IIC I/O Pins

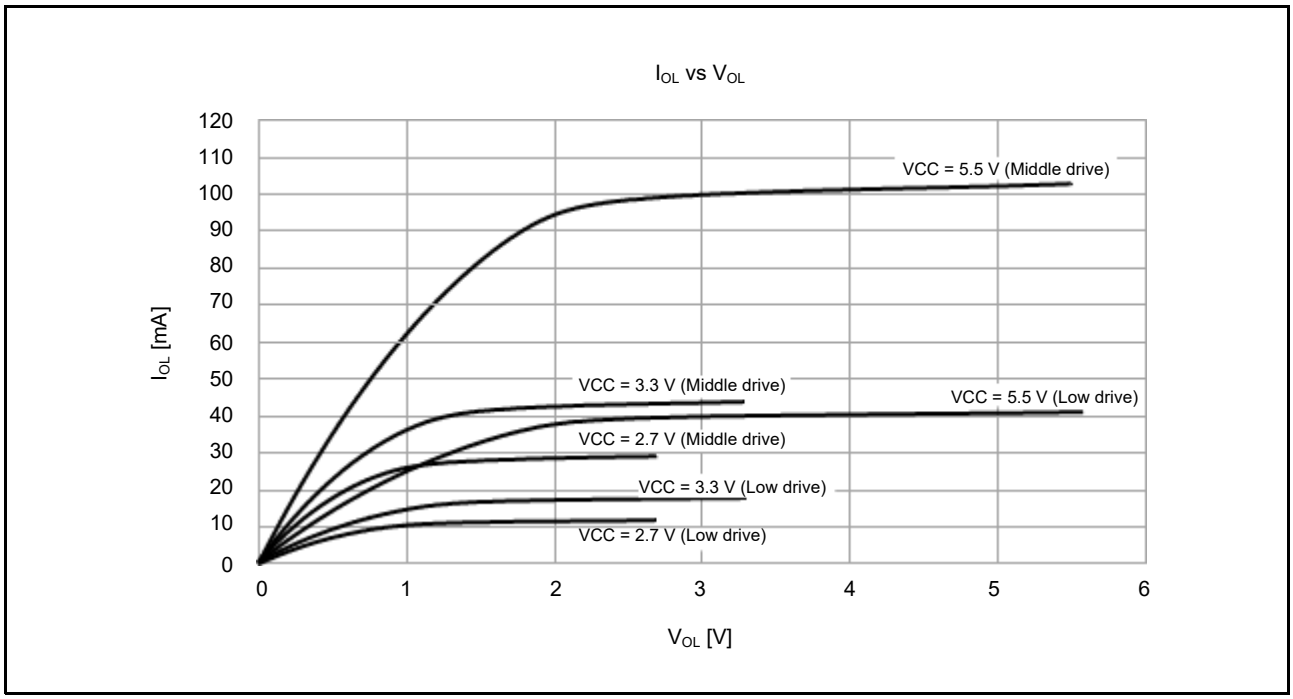


Figure 46.16 **V_{OH}/V_{OL} and I_{OH}/I_{OL} voltage characteristics at Ta = 25°C**

46.2.9 Operating and Standby Current

Table 46.11 Operating and standby current (1) (1 of 2)

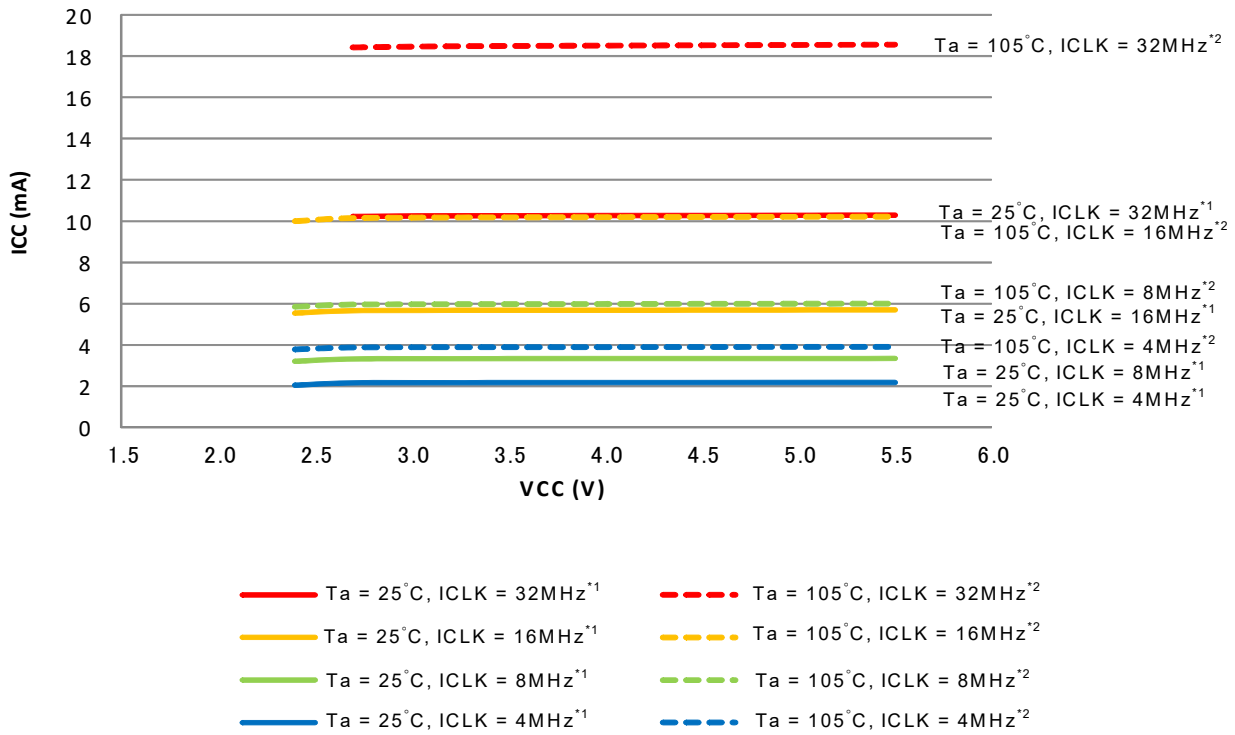
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter					Symbol	Typ*9	Max	Unit	Test Conditions
Supply current*1	High-speed mode*2	Normal mode	All peripheral clock disabled, while (1) code executing from flash*5	ICLK = 32 MHz	I_{CC}	4.2	-	mA	*7
				ICLK = 16 MHz		2.6	-		
				ICLK = 8 MHz		1.8	-		
			All peripheral clock disabled, CoreMark code executing from flash*5	ICLK = 32 MHz		6.2	-		
				ICLK = 16 MHz		3.6	-		
				ICLK = 8 MHz		2.4	-		
			All peripheral clock enabled, while (1) code executing from flash*5	ICLK = 32 MHz		10.5	-		*8
				ICLK = 16 MHz		5.8	-		
				ICLK = 8 MHz		3.4	-		
			All peripheral clock enabled, code executing from flash*5	ICLK = 32 MHz		-	22.1		
		Sleep mode	All peripheral clock disabled*5	ICLK = 32 MHz		1.6	-		*7
				ICLK = 16 MHz		1.2	-		
				ICLK = 8 MHz		0.9	-		
			All peripheral clock enabled*5	ICLK = 32 MHz		7.5	-		*8
				ICLK = 16 MHz		4.1	-		
				ICLK = 8 MHz		2.4	-		
		Increase during BGO operation*6				2.5	-		-
	Middle-speed mode*2	Normal mode	All peripheral clock disabled, while (1) code executing from flash*5	ICLK = 12 MHz	I_{CC}	1.9	-	mA	*7
				ICLK = 8 MHz		1.6	-		
			All peripheral clock disabled, CoreMark code executing from flash*5	ICLK = 12 MHz		2.7	-		
				ICLK = 8 MHz		2.1	-		
			All peripheral clock enabled, while (1) code executing from flash*5	ICLK = 12 MHz		4.3	-		*8
				ICLK = 8 MHz		3.1	-		
			All peripheral clock enabled, code executing from flash*5	ICLK = 12 MHz		-	8.1		
		Sleep mode	All peripheral clock disabled*5	ICLK = 12 MHz		0.8	-		*7
				ICLK = 8 MHz		0.8	-		
			All peripheral clock enabled*5	ICLK = 12 MHz		3.0	-		*8
				ICLK = 8 MHz		2.2	-		
		Increase during BGO operation*6				2.5	-		-
	Low-speed mode*3	Normal mode	All peripheral clock disabled, while (1) code executing from flash*5	ICLK = 1 MHz	I_{CC}	0.3	-	mA	*7
			All peripheral clock disabled, CoreMark code executing from flash*5	ICLK = 1 MHz		0.4	-		
			All peripheral clock enabled, while (1) code executing from flash*5	ICLK = 1 MHz		0.5	-		*8
			All peripheral clock enabled, code executing from flash*5	ICLK = 1 MHz		-	2.0		
		Sleep mode	All peripheral clock disabled*5	ICLK = 1 MHz		0.2	-		*7
			All peripheral clock enabled*5	ICLK = 1 MHz		0.4	-		*8

Table 46.11 Operating and standby current (1) (2 of 2)
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter					Symbol	Typ*9	Max	Unit	Test Conditions
Supply current*1	Low-voltage mode*3	Normal mode	All peripheral clock disabled, while (1) code executing from flash*5	ICLK = 4 MHz	I_{CC}	1.5	-	mA	*7
			All peripheral clock disabled, CoreMark code executing from flash*5	ICLK = 4 MHz		1.7	-		
			All peripheral clock enabled, while (1) code executing from flash*5	ICLK = 4 MHz		2.3	-		*8
			All peripheral clock enabled, code executing from flash*5	ICLK = 4 MHz		-	4.0		
		Sleep mode	All peripheral clock disabled*5	ICLK = 4 MHz		0.9	-		*7
			All peripheral clock enabled*5	ICLK = 4 MHz		1.7	-		*8
	Subosc-speed mode*4	Normal mode	All peripheral clock disabled, while (1) code executing from flash*5	ICLK = 32.768 kHz	I_{CC}	5.9	-	μA	*7
			All peripheral clock enabled, while (1) code executing from flash*5	ICLK = 32.768 kHz		13.0	-		*8
			All peripheral clock enabled, code executing from flash*5	ICLK = 32.768 kHz		128.3 (17.8)*10	163.7		
		Sleep mode	All peripheral clock disabled*5	ICLK = 32.768 kHz		3.2	-		*7
			All peripheral clock enabled*5	ICLK = 32.768 kHz		10.0	-		*8

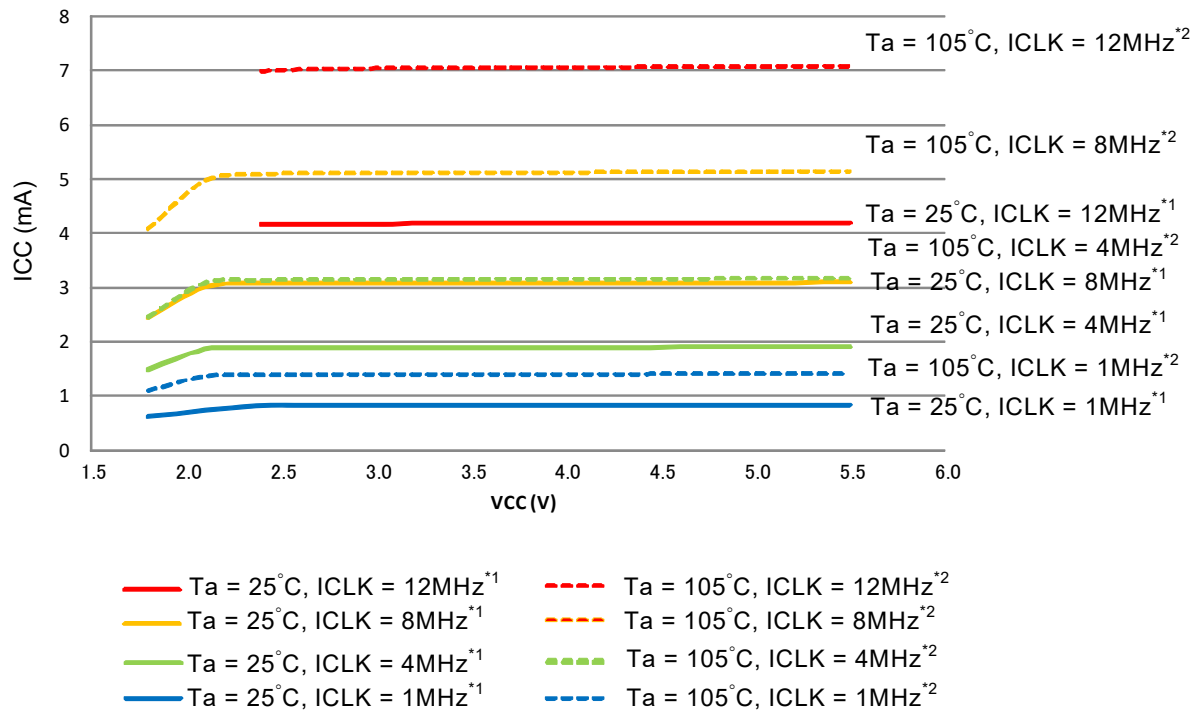
Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. The clock source is HOCO.
Note 3. The clock source is MOCO.
Note 4. The clock source is the sub-clock oscillator.
Note 5. This does not include BGO operation.
Note 6. This is the increase for programming or erasure of the flash memory for data storage during program execution.
Note 7. PCLKB and PCLKD are set to divided by 64.
Note 8. PCLKB and PCLKD are the same frequency as that of ICLK.
Note 9. VCC = 3.3 V.
Note 10. MOCO and DAC is stopped.



Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.

Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper-limit samples during product evaluation.

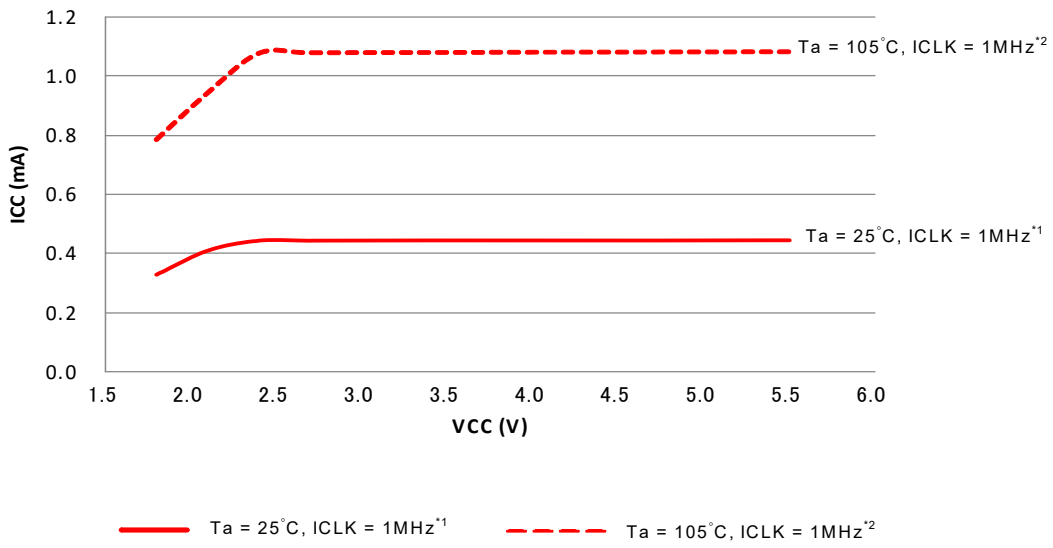
Figure 46.17 Voltage dependency in high-speed mode (reference data)



Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.

Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper-limit samples during product evaluation.

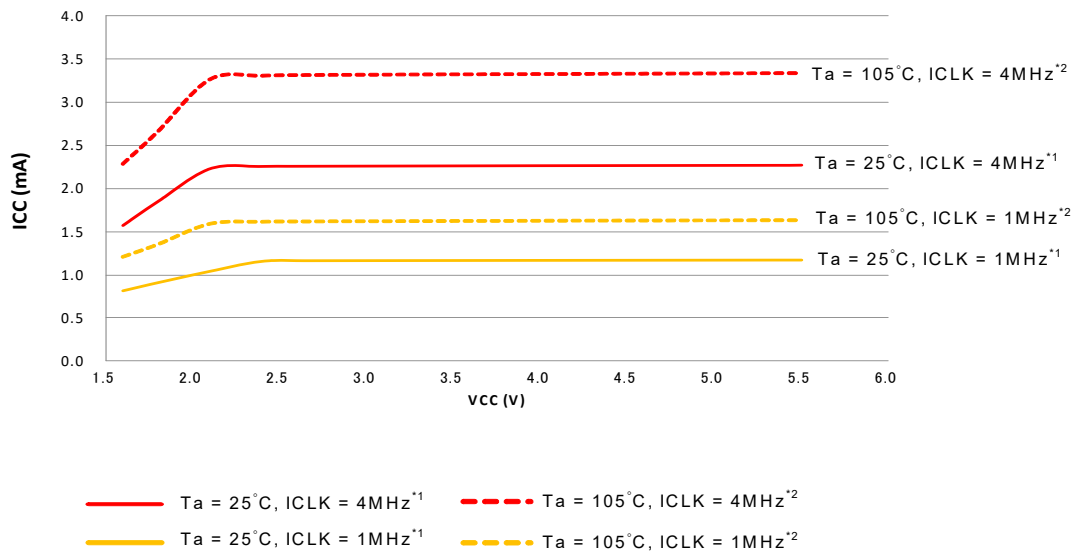
Figure 46.18 Voltage dependency in middle-speed mode (reference data)



Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.

Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper-limit samples during product evaluation.

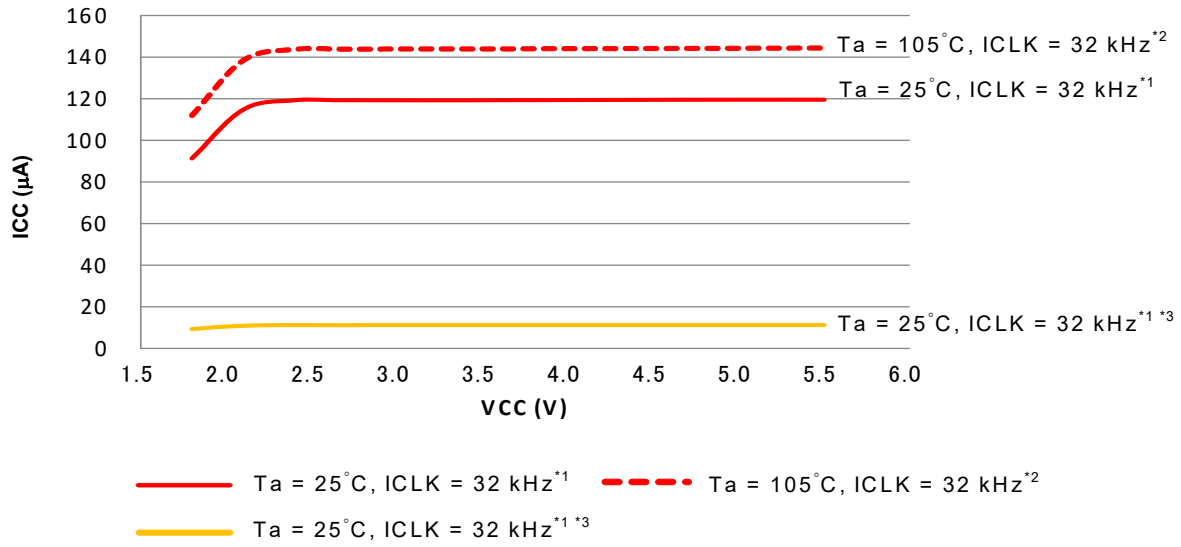
Figure 46.19 Voltage dependency in low-speed mode (reference data)



Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.

Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper-limit samples during product evaluation.

Figure 46.20 Voltage dependency in low-voltage mode (reference data)



Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.
Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper-limit samples during product evaluation.
Note 3. MOCO and DAC are stopped.

Figure 46.21 Voltage dependency in subosc-speed mode (reference data)

Table 46.12 Operating and standby current (2)
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Typ*3	Max	Unit	Test conditions
Supply current*1	Software Standby mode*2	T_a = 25°C	I_{CC}	0.5	2.0	μA	-
		T_a = 55°C		0.8	7.0		
		T_a = 85°C		2.9	12.0		
		T_a = 105°C		6.3	42.0		
	Increment for RTC operation with low-speed on-chip oscillator*4			0.4	-		-
	Increment for RTC operation with sub-clock oscillator*4			0.5	-		SOMCR.SODRV[1:0] are 11b (Low power mode 3)
				1.6	-		SOMCR.SODRV[1:0] are 00b (normal mode)

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOS transistors are in the off state.
Note 2. The IWDT and LVD are not operating.
Note 3. VCC = 3.3 V.
Note 4. Includes the current of low-speed on-chip oscillator or sub-oscillation circuit.

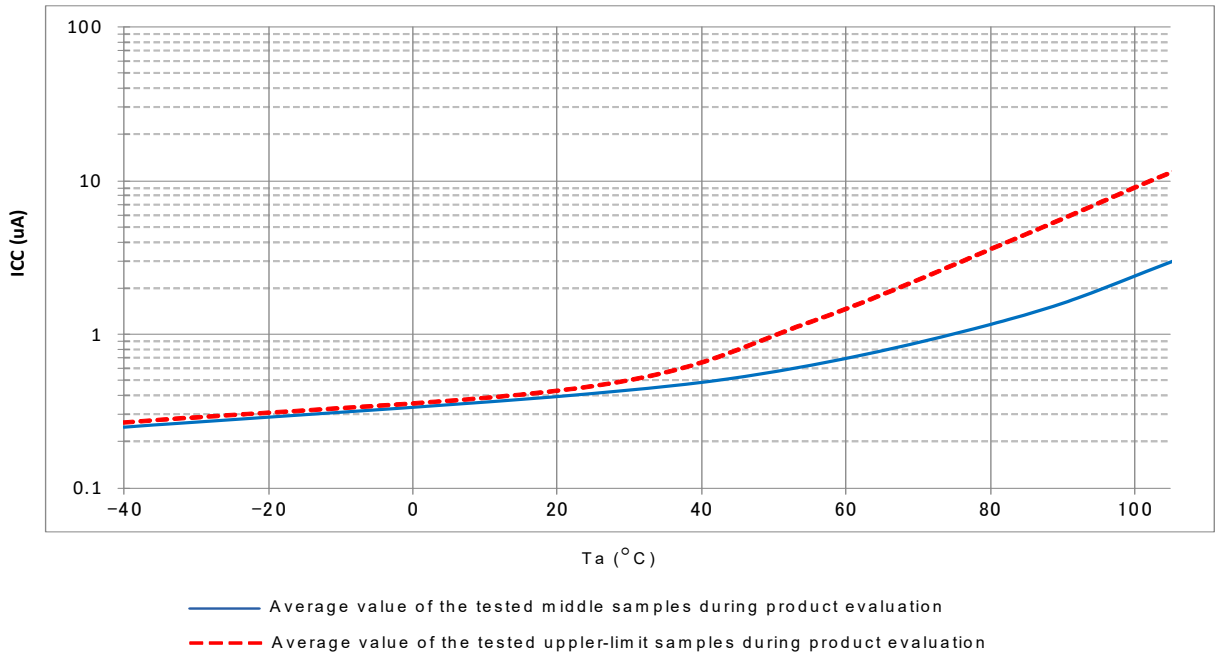
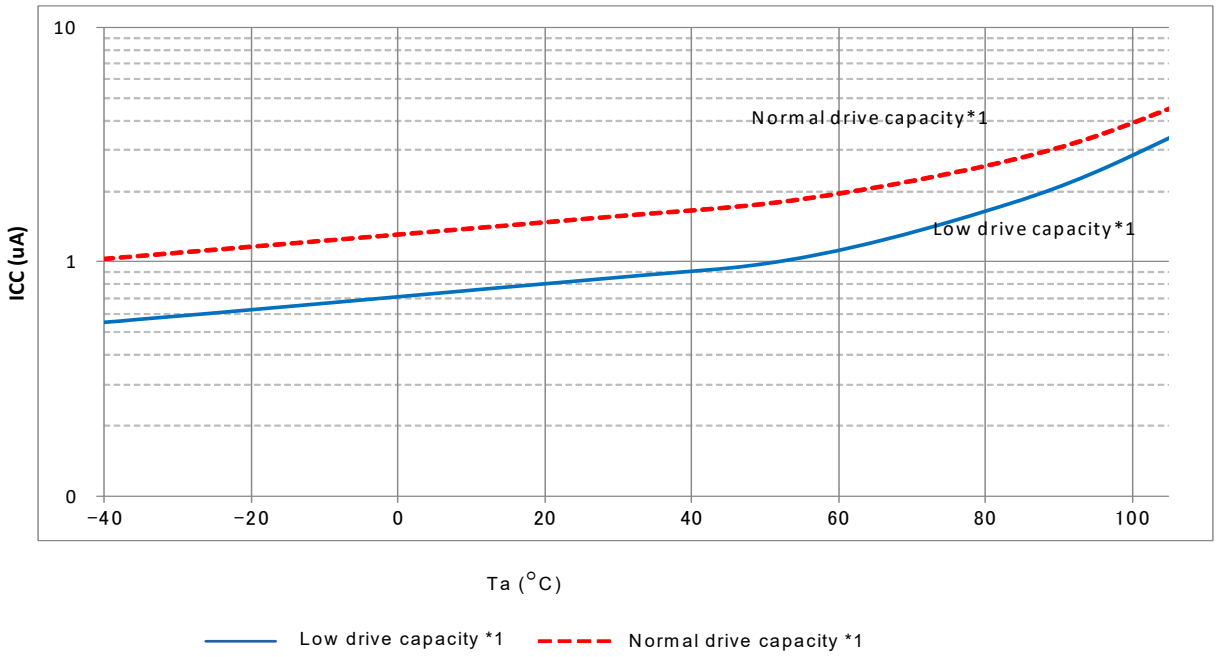


Figure 46.22 Temperature dependency in Software Standby mode (reference data)



Note 1. Average value of the tested middle sample during product evaluation.

Figure 46.23 Temperature dependency of RTC operation (reference data)

Table 46.13 Operating and standby current (3)
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Analog power supply current	During A/D conversion (at high-speed conversion)		I_{AVCC}	-	-	3.0	mA	-
	During A/D conversion (at low-power conversion)			-	-	1.0	mA	-
	During D/A conversion *1 (per channel)			-	-	1.6	mA	-
	Waiting for A/D and D/A conversion (all units)*5			-	-	1.0	μA	-
Reference power supply current	During A/D conversion		I_{REFH0}	-	-	150	μA	-
	Waiting for A/D conversion (all units)			-	-	60	nA	-
Temperature sensor			I_{TNS}	-	75	-	μA	-
Low-power analog comparator (ACMPLP) operating current	Window comparator (high-speed mode)		I_{CMPLP}	-	15	-	μA	-
	Window comparator (low-speed mode)			-	3	-	μA	-
	Comparator (high-speed mode)			-	10	-	μA	-
	Comparator (low-speed mode)			-	2	-	μA	-
High-speed analog comparator (ACMPHS) operating current			I_{CMPHS}	-	70	100	μA	AVCC0 ≥ 2.7V
Operational Amplifier operating current	Low power mode	1-unit operating	I_{AMP}	-	1.0	2.0	μA	-
		2-unit operating		-	1.5	3.0	μA	-
		3-unit operating		-	2.0	3.5	μA	-
		4-unit operating		-	2.5	4.5	μA	-
	High speed mode	1-unit operating		-	200	280	μA	-
		2-unit operating		-	320	450	μA	-
		3-unit operating		-	440	620	μA	-
		4-unit operating		-	560	790	μA	-
USB operating current	During USB communication under the following settings and conditions: • Function controller is in Full-Speed mode and - Bulk OUT transfer is (64 bytes) × 1 - Bulk IN transfer is (64 bytes) × 1 • Host device is connected by a 1-meter USB cable from the USB port.		I_{USBF}*2	-	3.6 (VCC) 1.1 (VCC_USB)*4	-	mA	-
	During suspended state under the following setting and conditions: • Function controller is in Full-Speed mode (the USB_DP pin is pulled up) • Software Standby mode • Host device is connected by a 1-meter USB cable from the USB port.		I_{SUSP}*3	-	0.35 (VCC) 170 (VCC_USB)*4	-	μA	-
PWM Delay Generation Circuit current	PCLKD = 64 MHz, DLL Mode = 5-bit mode		I_{CC}	-	3.3	4.6	mA	-
	PCLKD = 64 MHz, DLL Mode = 4-bit mode			-	3.0	4.2	mA	-
	PCLKD = 32 MHz, DLL Mode = 5-bit mode			-	2.0	2.8	mA	-

Note 1. The reference power supply current is included in the power supply current value for D/A conversion.
Note 2. Current is consumed only by the USBFS.
Note 3. Includes the current supplied from the pull-up resistor of the USB_DP pin to the pull-down resistor of the host device, in addition to the current consumed by the MCU in the suspended state.
Note 4. When VCC = VCC_USB = 3.3 V.

Note 5. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (ADC140 module-stop bit) is in the module-stop state.

46.2.10 VCC Rise and Fall Gradient and Ripple Frequency

Table 46.14 Rise and fall gradient characteristics

Conditions: VCC = AVCC0 = 0 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Power-on VCC rising gradient	Voltage monitor 0 reset disabled at startup	SrVCC	0.02	-	2	ms/V	-
	Voltage monitor 0 reset enabled at startup*1, *2				-		
	SCI boot mode*2				2		

Note 1. When OFS1.LVDAS = 0.

Note 2. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of OFS1.LVDAS bit.

Table 46.15 Rising and falling gradient and ripple frequency characteristics

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (5.5 V) and lower limit (1.6 V).

When the VCC change exceeds VCC ±10%, the allowable voltage change rising and falling gradient dt/dVCC must be met.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Allowable ripple frequency	$f_{r\ (VCC)}$	-	-	10	kHz	Figure 46.24 $V_{r\ (VCC)} \leq VCC \times 0.2$
		-	-	1	MHz	Figure 46.24 $V_{r\ (VCC)} \leq VCC \times 0.08$
		-	-	10	MHz	Figure 46.24 $V_{r\ (VCC)} \leq VCC \times 0.06$
Allowable voltage change rising and falling gradient	dt/dVCC	1.0	-	-	ms/V	When VCC change exceeds VCC ±10%

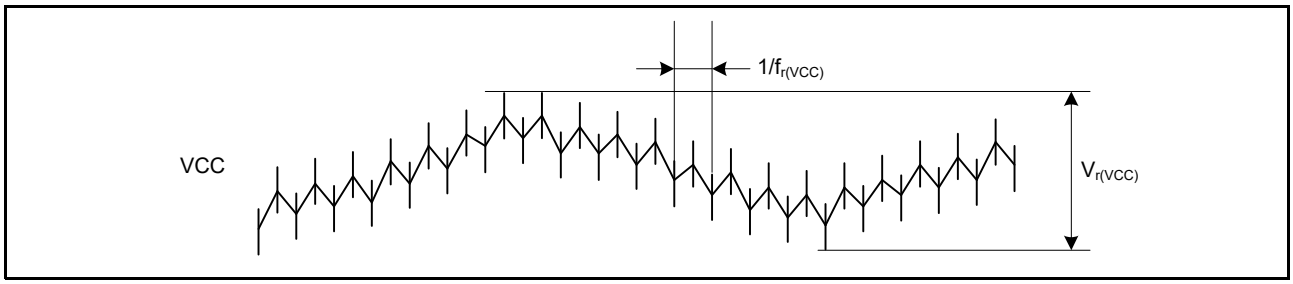


Figure 46.24 Ripple waveform

46.2.11 Thermal Characteristics

Maximum value of junction temperature (Tj) must not exceed the value of section 46.2.1, Tj/Ta Definition.

Tj is calculated by either of the following equations.

- Tj = Ta + θja × Total power consumption
- Tj = Tt + Ψjt × Total power consumption

  Tj : Junction temperature (°C)

  Ta : Ambient temperature (°C)

  Tt : Top center case temperature (°C)

  θja : Thermal resistance of "Junction"-to-"Ambient" (°C/W)

  Ψjt : Thermal resistance of "Junction"-to-"Top center case" (°C/W)
- Total power consumption = Voltage × (Leakage current + Dynamic current)
- Leakage current of IO = Σ (IOL × VOL) / Voltage + Σ (|IOH| × |VCC – VOH|) / Voltage

- Dynamic current of IO = Σ IO (Cin + Cload) × IO switching frequency × Voltage

  Cin: Input capacitance

  Cload: Output capacitance

Regarding θja and Ψjt, see Table 46.16.

Table 46.16 Thermal Resistance

Parameter	Package	Symbol	Value	Unit	Test conditions
Thermal Resistance	32-pin QFN	θja	24.2*1	°C/W	JESD 51-2 and 51-7compliant
	48-pin QFN		21.8*1		
	32-pin LQFP		56.2		
	48-pin LQFP		57.7		
	64-pin LQFP		48.9		
	36-pin LGA		32.9		JESD 51-2 and 51-9 compliant
	32-pin QFN	Ψjt	0.17*1	°C/W	JESD 51-2 and 51-7 compliant
	48-pin QFN		0.17*1		
	32-pin LQFP		1.71		
	48-pin LQFP		1.71		
	64-pin LQFP		1.22		
	36-pin LGA		0.10		JESD 51-2 and 51-9 compliant

Note: The values are reference values when the 4-layer board is used. Thermal resistance depends on the number of layers or size of the board. For details, refer to the JEDEC standards.

Note 1. This value applies when the Exposed die pad for this purpose is connected to VSS.

46.3 AC Characteristics

46.3.1 Frequency

Table 46.17 Operation frequency in high-speed operating mode
Conditions: VCC = AVCC0 = 2.4 to 5.5 V

Parameter			Symbol	Min	Typ	Max*5	Unit
Operation frequency	System clock (ICLK)*1, *2, *4	2.7 to 5.5 V	f	0.032768	-	32	MHz
		2.4 to 2.7 V		0.032768	-	16	
	Peripheral module clock (PCLKB)*4	2.7 to 5.5 V		-	-	32	
		2.4 to 2.7 V		-	-	16	
	Peripheral module clock (PCLKD)*3, *4	2.7 to 5.5 V		-	-	64	
		2.4 to 2.7 V		-	-	16	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory. When using ICLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of ICLK must be ±3.5% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the 14-bit A/D converter is in use.
Note 4. See section 8, Clock Generation Circuit for the relationship of frequencies between ICLK, PCLKB, and PCLKD.
Note 5. The maximum value of operation frequency does not include internal oscillator errors. For details on the range of guaranteed operation, see Table 46.22, Clock timing.

Table 46.18 Operation frequency in middle-speed mode
Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter			Symbol	Min	Typ	Max*5	Unit
Operation frequency	System clock (ICLK)*1, *2, *4	2.7 to 5.5 V	f	0.032768	-	12	MHz
		2.4 to 2.7 V		0.032768	-	12	
		1.8 to 2.4 V		0.032768	-	8	
	Peripheral module clock (PCLKB)*4	2.7 to 5.5 V		-	-	12	
		2.4 to 2.7 V		-	-	12	
		1.8 to 2.4 V		-	-	8	
	Peripheral module clock (PCLKD)*3, *4	2.7 to 5.5 V		-	-	12	
		2.4 to 2.7 V		-	-	12	
		1.8 to 2.4 V		-	-	8	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory. When using ICLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of ICLK must be ±3.5% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the 14-bit A/D converter is in use.
Note 4. See section 8, Clock Generation Circuit for the relationship of frequencies between ICLK, PCLKB, and PCLKD.
Note 5. The maximum value of operation frequency does not include internal oscillator errors. For details on the range of guaranteed operation, see Table 46.22, Clock timing.

Table 46.19 Operation frequency in low-speed mode
Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter			Symbol	Min	Typ	Max*5	Unit
Operation frequency	System clock (ICLK)*1, *2, *4	1.8 to 5.5 V	f	0.032768	-	1	MHz
	Peripheral module clock (PCLKB)*4	1.8 to 5.5 V		-	-	1	
	Peripheral module clock (PCLKD)*3, *4	1.8 to 5.5 V		-	-	1	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory.
Note 2. The frequency accuracy of ICLK must be ±3.5% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.
Note 4. See section 8, Clock Generation Circuit for the relationship of frequencies between ICLK, PCLKB, and PCLKD.
Note 5. The maximum value of operation frequency does not include internal oscillator errors. For details on the range of guaranteed operation, see Table 46.22, Clock timing.

Table 46.20 Operation frequency in low-voltage mode
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max*5	Unit
Operation frequency	System clock (ICLK)*1, *2, *4	1.6 to 5.5 V	f	0.032768	-	4	MHz
	Peripheral module clock (PCLKB)*4	1.6 to 5.5 V		-	-	4	
	Peripheral module clock (PCLKD)*3, *4	1.6 to 5.5 V		-	-	4	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory. When using ICLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of ICLK must be ±3.5% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the 14-bit A/D converter is in use.
Note 4. See section 8, Clock Generation Circuit for the relationship of frequencies between ICLK, PCLKB, and PCLKD.
Note 5. The maximum value of operation frequency does not include internal oscillator errors. For details on the range of guaranteed operation, see Table 46.22, Clock timing.

Table 46.21 Operation frequency in Subosc-speed mode
Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*1, *3	1.8 to 5.5 V	f	27.8528	32.768	37.6832	kHz
	Peripheral module clock (PCLKB)*3	1.8 to 5.5 V		-	-	37.6832	
	Peripheral module clock (PCLKD)*2, *3	1.8 to 5.5 V		-	-	37.6832	

Note 1. Programming and erasing the flash memory is not possible.
Note 2. The 14-bit A/D converter cannot be used.
Note 3. See section 8, Clock Generation Circuit for the relationship between ICLK, PCLKB, and PCLKD frequencies.

46.3.2 Clock Timing

Table 46.22 Clock timing (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
EXTAL external clock input cycle time		t_{Xcyc}	50	-	-	ns	Figure 46.25
EXTAL external clock input high pulse width		t_{XH}	20	-	-	ns	
EXTAL external clock input low pulse width		t_{XL}	20	-	-	ns	
EXTAL external clock rising time		t_{Xr}	-	-	5	ns	
EXTAL external clock falling time		t_{Xf}	-	-	5	ns	
EXTAL external clock input wait time*1		t_{EXWT}	0.3	-	-	μs	-
EXTAL external clock input frequency		f_{EXTAL}	-	-	20	MHz	2.4 ≤ VCC ≤ 5.5
			-	-	8		1.8 ≤ VCC < 2.4
			-	-	1		1.6 ≤ VCC < 1.8
Main clock oscillator oscillation frequency		f_{MAIN}	1	-	20	MHz	2.4 ≤ VCC ≤ 5.5
			1	-	8		1.8 ≤ VCC < 2.4
			1	-	4		1.6 ≤ VCC < 1.8
LOCO clock oscillation frequency		f_{LOCO}	27.8528	32.768	37.6832	kHz	-
LOCO clock oscillation stabilization time		t_{LOCO}	-	-	100	μs	Figure 46.26
IWDT-dedicated clock oscillation frequency		f_{ILOCO}	12.75	15	17.25	kHz	-
MOCO clock oscillation frequency		f_{MOCO}	6.8	8	9.2	MHz	-
MOCO clock oscillation stabilization time		t_{MOCO}	-	-	1	μs	-
HOCO clock oscillation frequency		f_{HOCO24}	23.64	24	24.36	MHz	Ta = -40 to -20°C 1.8 ≤ VCC ≤ 5.5
			22.68	24	25.32		Ta = -40 to 85°C 1.6 ≤ VCC < 1.8
			23.76	24	24.24		Ta = -20 to 85°C 1.8 ≤ VCC ≤ 5.5
			23.52	24	24.48		Ta = 85 to 105°C 2.4 ≤ VCC ≤ 5.5
		f_{HOCO32}	31.52	32	32.48		Ta = -40 to -20°C 1.8 ≤ VCC ≤ 5.5
			30.24	32	33.76		Ta = -40 to 85°C 1.6 ≤ VCC < 1.8
			31.68	32	32.32		Ta = -20 to 85°C 1.8 ≤ VCC ≤ 5.5
			31.36	32	32.64		Ta = 85 to 105°C 2.4 ≤ VCC ≤ 5.5
		f_{HOCO48}*3	47.28	48	48.72		Ta = -40 to -20°C 1.8 ≤ VCC ≤ 5.5
			47.52	48	48.48		Ta = -20 to 85°C 1.8 ≤ VCC ≤ 5.5
			47.04	48	48.96		Ta = 85 to 105°C 2.4 ≤ VCC ≤ 5.5
		f_{HOCO64}*4	63.04	64	64.96		Ta = -40 to -20°C 2.4 ≤ VCC ≤ 5.5
			63.36	64	64.64		Ta = -20 to 85°C 2.4 ≤ VCC ≤ 5.5
			62.72	64	65.28		Ta = 85 to 105°C 2.4 ≤ VCC ≤ 5.5
HOCO clock oscillation stabilization time*5, *6	Except low-voltage mode	t_{HOCO24} t_{HOCO32}	-	-	37.1	μs	Figure 46.27
		t_{HOCO48}	-	-	43.3		
		t_{HOCO64}	-	-	80.6		
	Low-voltage mode	t_{HOCO24} t_{HOCO32} t_{HOCO48} t_{HOCO64}	-	-	100.9		
Sub-clock oscillator oscillation frequency		f_{SUB}	-	32.768	-	kHz	-

Table 46.22 Clock timing (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Sub-clock oscillation stabilization time*2	t_{SUBOSC}	-	0.5	-	s	Figure 46.28

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating) when the external clock is stable.

Note 2. After changing the setting of the SOSCCR.SOSTP bit to start sub-clock oscillator operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization wait time elapsed. Use the oscillator wait time value recommended by the oscillator manufacturer.

Note 3. The 48-MHz HOCO can be used within a VCC range of 1.8 V to 5.5 V.

Note 4. The 64-MHz HOCO can be used within a VCC range of 2.4 V to 5.5 V.

Note 5. This is a characteristic when the HOCOCR.HCSTP bit is cleared to 0 (oscillation) in the MOCO stop state. When the HOCOCR.HCSTP bit is cleared to 0 (oscillation) during MOCO oscillation, this specification is shortened by 1 μs.

Note 6. Check OSCSF.HOCOSF to confirm whether stabilization time has elapsed.

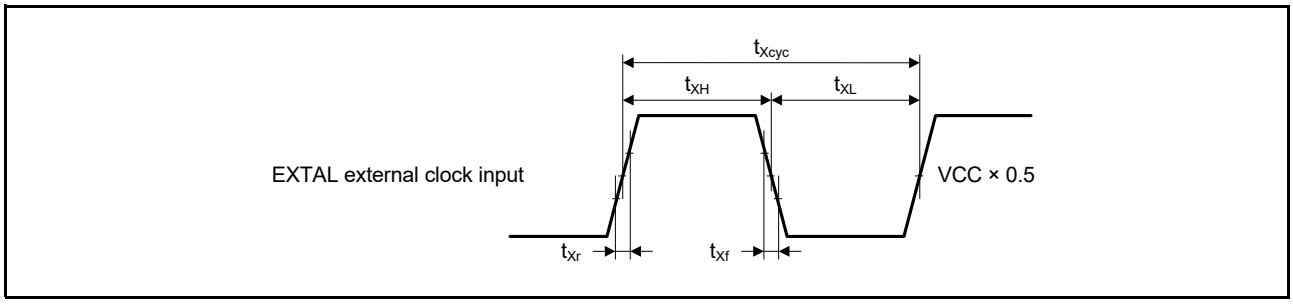


Figure 46.25 EXTAL external clock input timing

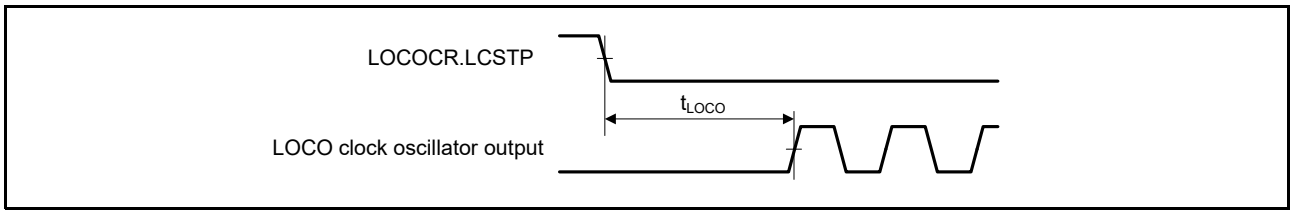


Figure 46.26 LOCO clock oscillation start timing

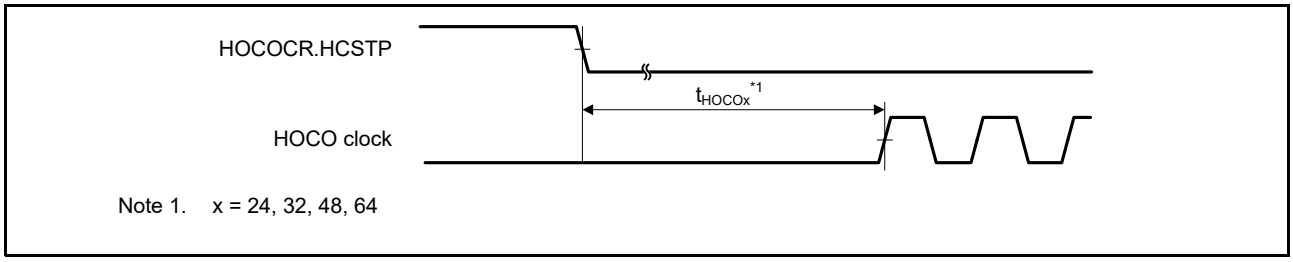


Figure 46.27 HOCO clock oscillation start timing (started by setting the HOCOCR.HCSTP bit)

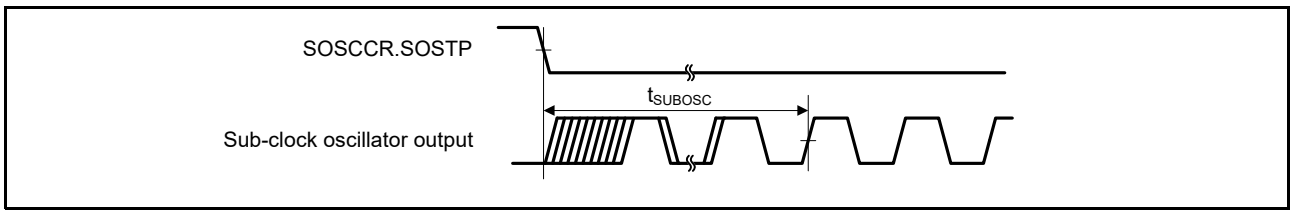


Figure 46.28 Sub-clock oscillation start timing

46.3.3 Reset Timing

Table 46.23 Reset timing

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	At power-on	t_{RESWP}	3	-	-	ms	Figure 46.29
	Not at power-on	t_{RESW}	30	-	-	μs	Figure 46.30
Wait time after RES cancellation (at power-on)	LVD0 enabled*1	t_{RESWT}	-	0.7	-	ms	Figure 46.29
	LVD0 disabled*2		-	0.3	-		
Wait time after RES cancellation (during powered-on state)	LVD0 enabled*1	t_{RESWT2}	-	0.5	-	ms	Figure 46.30
	LVD0 disabled*2		-	0.05	-		
Wait time after internal reset cancellation (watchdog timer reset, SRAM parity error reset, SRAM ECC error reset, bus master MPU error reset, bus slave MPU error reset, stack pointer error reset, software reset)	LVD0 enabled*1	t_{RESWT3}	-	0.6	-	ms	
	LVD0 disabled*2		-	0.15	-		

Note 1. When OFS1.LVDAS = 0.
Note 2. When OFS1.LVDAS = 1.

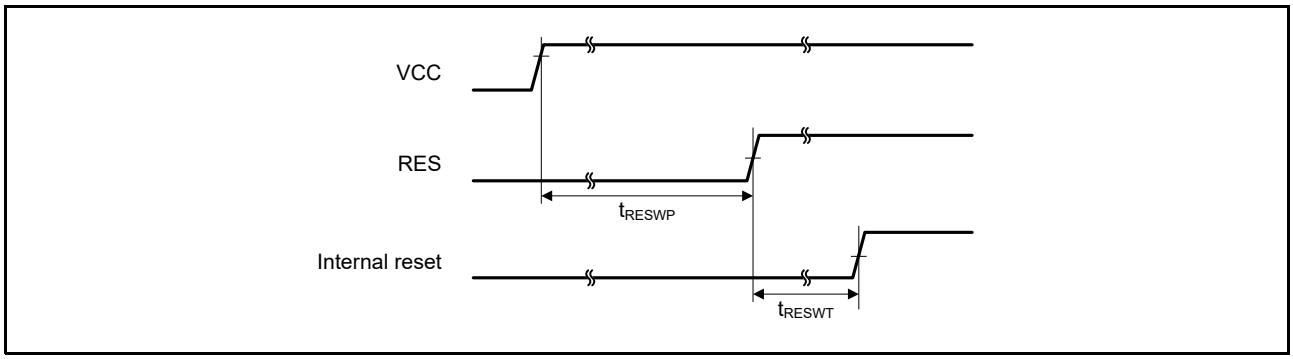


Figure 46.29 Reset input timing at power-on

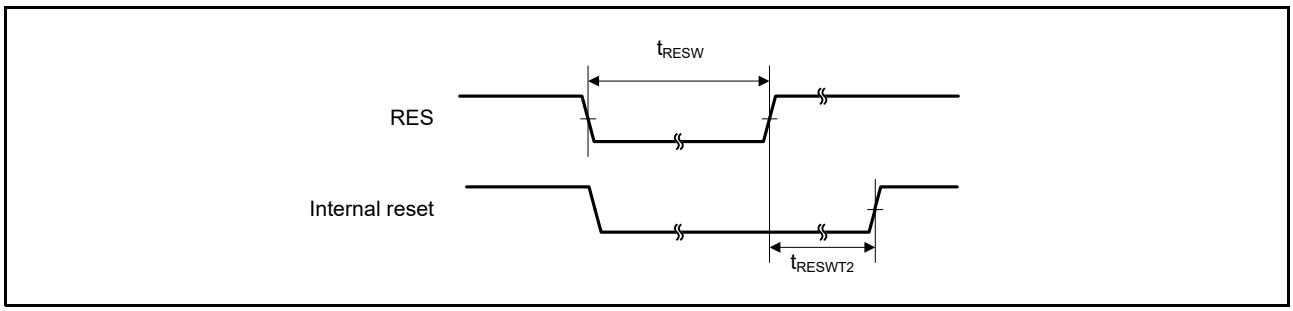


Figure 46.30 Reset input timing

46.3.4 Wakeup Time

Table 46.24 Timing of recovery from low power modes (1)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	High-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (20 MHz)*2	t_{SBYMC}	-	2	3	ms	Figure 46.31
		External clock input to main clock oscillator	System clock source is main clock oscillator (20 MHz)*3	t_{SBYEX}	-	14	25	μs	
		System clock source is HOCO*4 (HOCO clock is 32 MHz)		t_{SBYHO}	-	43	52	μs	
		System clock source is HOCO*4 (HOCO clock is 48 MHz)		t_{SBYHO}	-	44	52	μs	
		System clock source is HOCO*5 (HOCO clock is 64 MHz)		t_{SBYHO}	-	82	110	μs	
		System clock source is MOCO		t_{SBYMO}	-	16	25	μs	

Note 1. The division ratio of ICK and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.
Note 4. The HOCO clock wait control register (HOCOWTCR) is set to 05h.
Note 5. The HOCO clock wait control register (HOCOWTCR) is set to 06h.

Table 46.25 Timing of recovery from low power modes (2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Middle-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (12 MHz)*2	t_{SBYMC}	-	2	3	ms	Figure 46.31
		External clock input to main clock oscillator	System clock source is main clock oscillator (12 MHz)*3	t_{SBYEX}	-	2.9	10	μs	
		System clock source is HOCO*4		t_{SBYHO}	-	38	50	μs	
		System clock source is MOCO (8 MHz)		t_{SBYMO}	-	3.5	5.5	μs	

Note 1. The division ratio of ICK and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.
Note 4. The system clock is 12 MHz.

Table 46.26 Timing of recovery from low power modes (3)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (1 MHz)*2	t_{SBYMC}	-	2	3	ms	Figure 46.31
		External clock input to main clock oscillator	System clock source is main clock oscillator (1 MHz)*3	t_{SBYEX}	-	28	50	μs	
		System clock source is MOCO (1 MHz)		t_{SBYMO}	-	25	35	μs	

Note 1. The division ratio of ICK and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.

Table 46.27 Timing of recovery from low power modes (4)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low-voltage mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (4 MHz)*2	t_{SBYMC}	-	2	3	ms	Figure 46.31
		External clock input to main clock oscillator	System clock source is main clock oscillator (4 MHz)*3	t_{SBYEX}	-	108	130	μs	
		System clock source is HOCO (4 MHz)		t_{SBYHO}	-	108	130	μs	

Note 1. The division ratio of ICK and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.

Table 46.28 Timing of recovery from low power modes (5)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	SubOSC-speed mode	System clock source is sub-clock oscillator (32.768 kHz)	t_{SBYSC}	-	0.85	1	ms	Figure 46.31
		System clock source is LOCO (32.768 kHz)	t_{SBYLO}	-	0.85	1.2	ms	

Note 1. The sub-clock oscillator or LOCO itself continues oscillating in Software Standby mode during Subosc-speed mode.

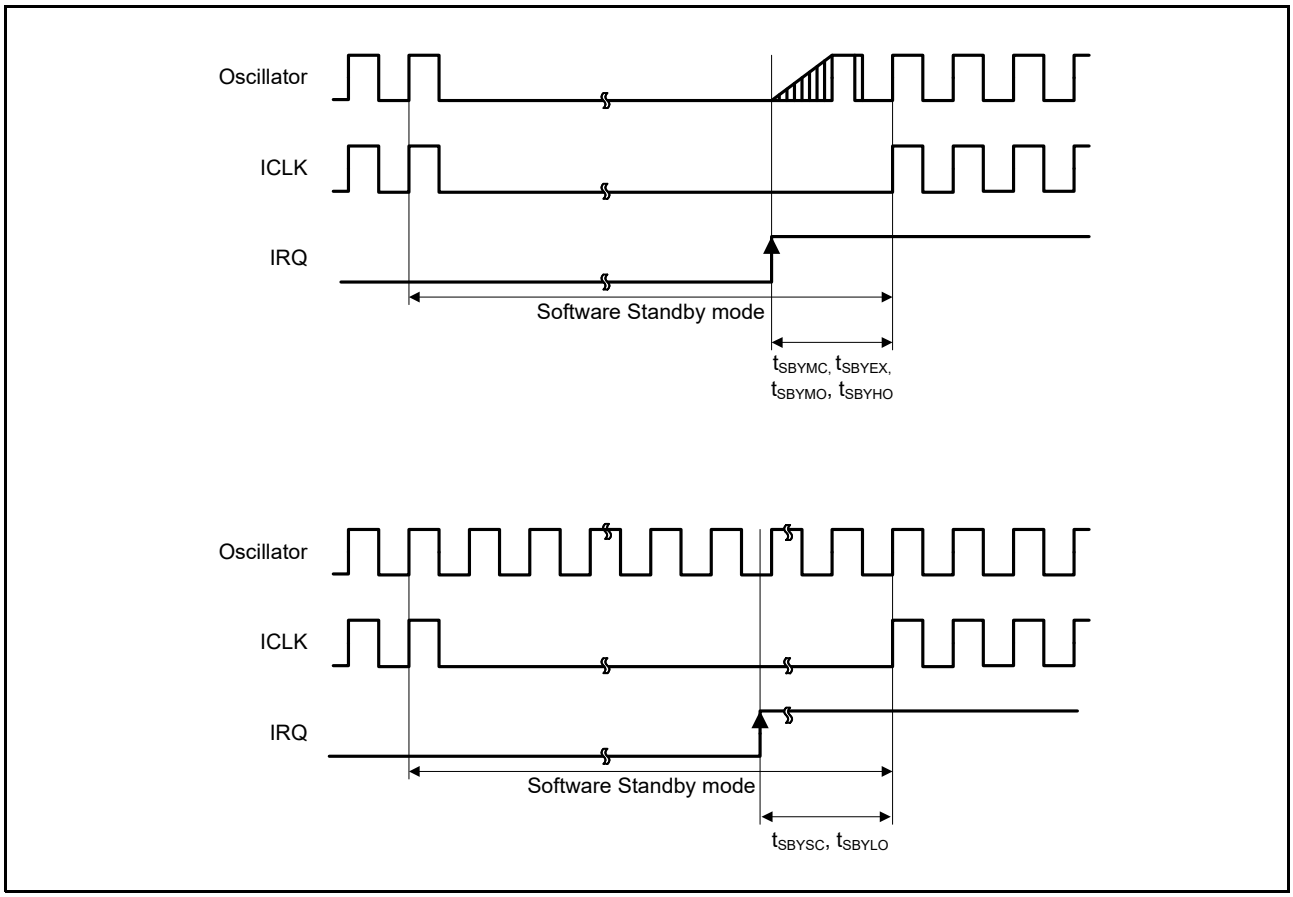
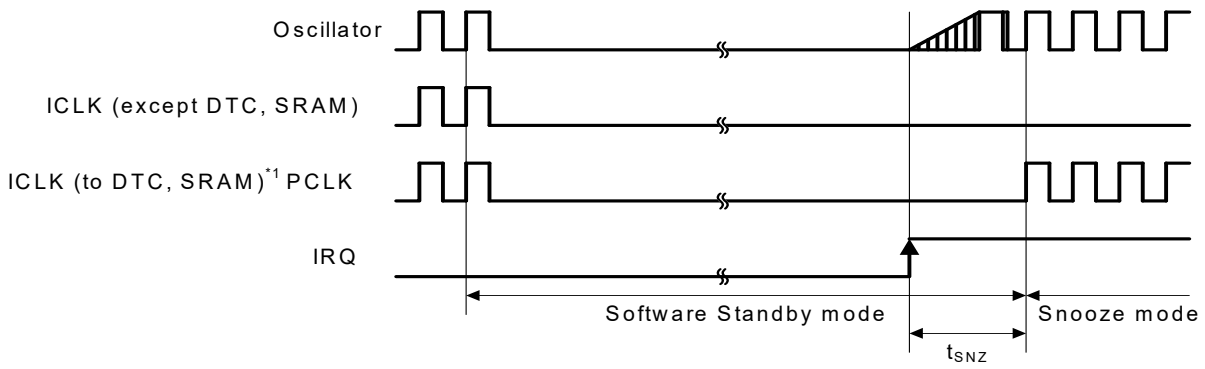


Figure 46.31 Software Standby mode cancellation timing

Table 46.29 Timing of recovery from low power modes (6)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode to Snooze mode	High-speed mode System clock source is HOCO	t_{SNZ}	-	36	45	μs	Figure 46.32
	Middle-speed mode System clock source is MOCO (8 MHz)	t_{SNZ}	-	1.3	3.6	μs	
	Low-speed mode System clock source is MOCO (1 MHz)	t_{SNZ}	-	10	13	μs	
	Low-voltage mode System clock source is HOCO (4 MHz)	t_{SNZ}	-	87	110	μs	



Note 1. When SNZCR.SNZDTCEN is set to 1, ICLK is supplied to DTC and SRAM.

Figure 46.32 Recovery timing from Software Standby mode to Snooze mode

46.3.5 NMI and IRQ Noise Filter

Table 46.30 NMI and IRQ noise filter

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	-	-	ns	NMI digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5$*2	-	-			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	-	-	ns	IRQ digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5$*3	-	-			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.
Note 1. t_{Pcyc} indicates the PCLKB cycle.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

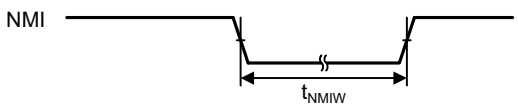


Figure 46.33 NMI interrupt input timing

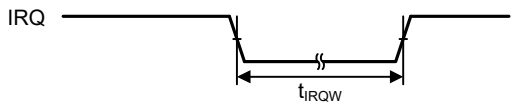


Figure 46.34 IRQ interrupt input timing

46.3.6 I/O Ports, POEG, GPT, AGT, KINT, and ADC14 Trigger Timing

Table 46.31 I/O Ports, POEG, GPT, AGT, KINT, and ADC14 trigger timing

Parameter			Symbol	Min	Max	Unit	Test conditions
I/O Ports	Input data pulse width		t_{PRW}	1.5	-	t_{Pcyc}	Figure 46.35
	Input/output data cycle (P002, P003, P010, P011)		t_{POcyc}	10	-	μs	-
POEG	POEG input trigger pulse width		t_{POEW}	3	-	t_{Pcyc}	Figure 46.36
GPT	Input capture pulse width	Single edge	t_{GTICW}	1.5	-	t_{PDcyc}	Figure 46.37
		Dual edge		2.5	-		
AGT	AGTIO, AGTEE input cycle	2.7 V ≤ VCC ≤ 5.5 V	t_{ACYC}*1	250	-	ns	Figure 46.38
		2.4 V ≤ VCC < 2.7 V		500	-	ns	
		1.8 V ≤ VCC < 2.4 V		1000	-	ns	
		1.6 V ≤ VCC < 1.8 V		2000	-	ns	
	AGTIO, AGTEE input high level width, low-level width	2.7 V ≤ VCC ≤ 5.5 V	t_{ACKWH}, t_{ACKWL}	100	-	ns	
		2.4 V ≤ VCC < 2.7 V		200	-	ns	
		1.8 V ≤ VCC < 2.4 V		400	-	ns	
		1.6 V ≤ VCC < 1.8 V		800	-	ns	
	AGTIO, AGTO, AGTOA, AGTOB output cycle	2.7 V ≤ VCC ≤ 5.5 V	t_{ACYC2}	62.5	-	ns	Figure 46.38
		2.4 V ≤ VCC < 2.7 V		125	-	ns	
		1.8 V ≤ VCC < 2.4 V		250	-	ns	
		1.6 V ≤ VCC < 1.8 V		500	-	ns	
ADC14	14-bit A/D converter trigger input pulse width		t_{TRGW}	1.5	-	t_{Pcyc}	Figure 46.39
KINT	KRn (n = 00 to 07) pulse width		t_{KR}	250	-	ns	Figure 46.40

Note 1. Constraints on AGTIO input: t_{Pcyc} × 2 (t_{Pcyc}: PCLKB cycle) < t_{ACYC}.

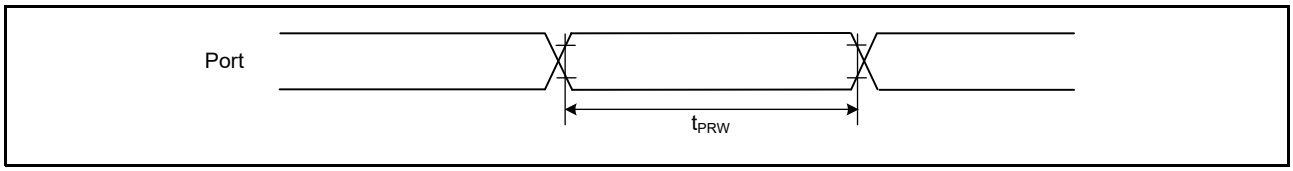


Figure 46.35 I/O ports input timing

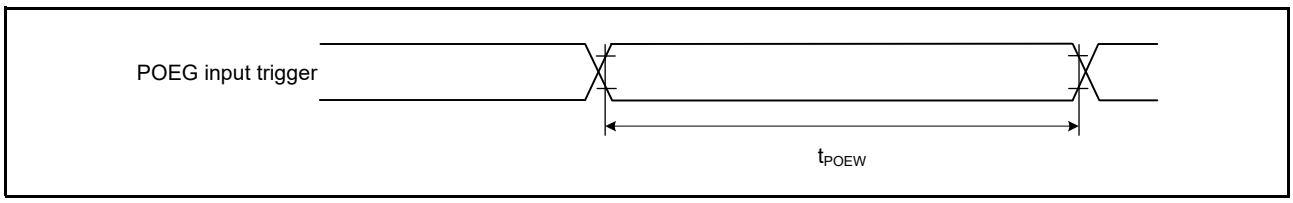


Figure 46.36 POEG input trigger timing

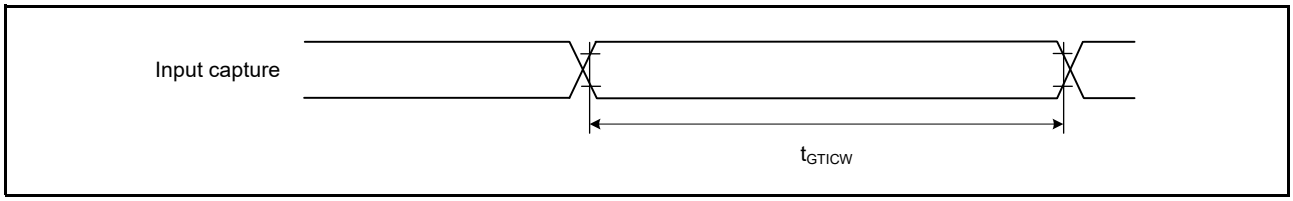


Figure 46.37 GPT input capture timing

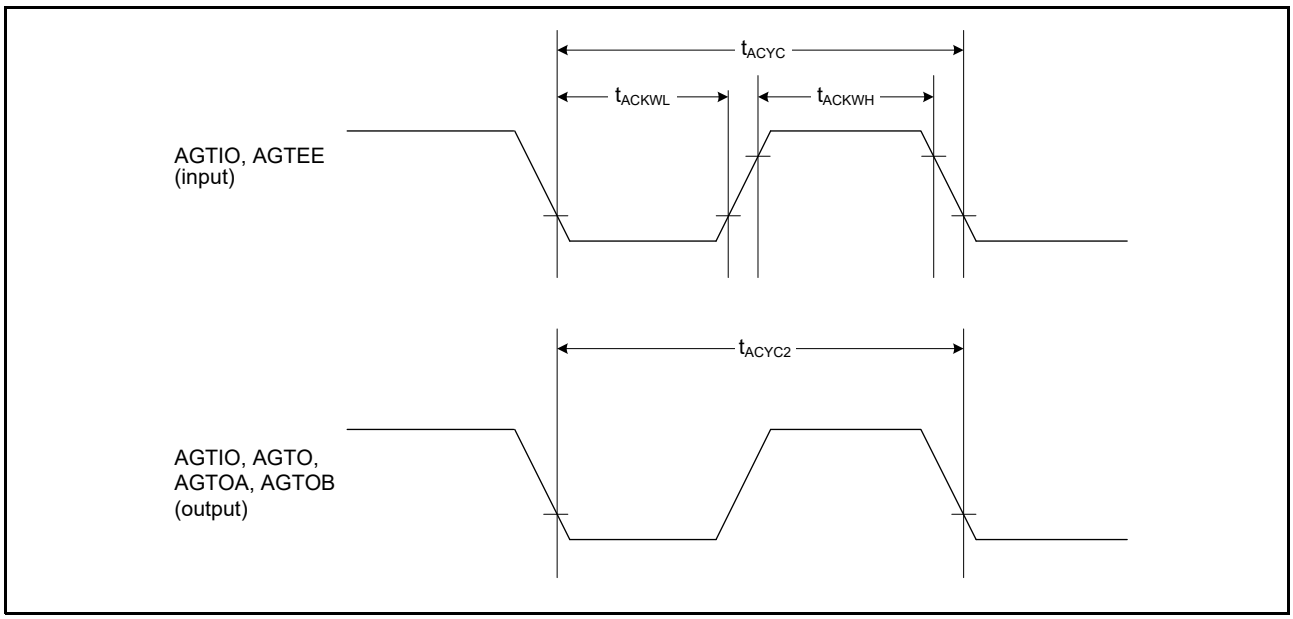


Figure 46.38 AGT I/O timing

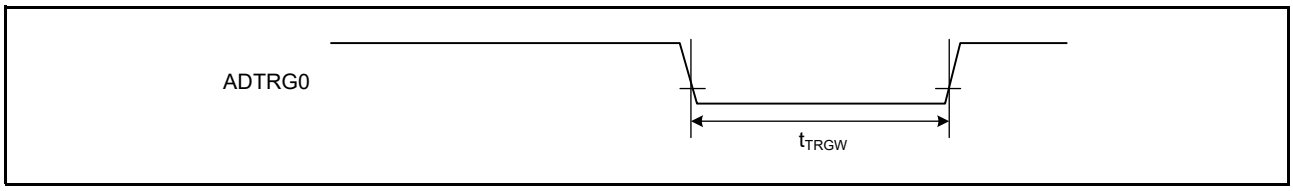


Figure 46.39 ADC14 trigger input timing

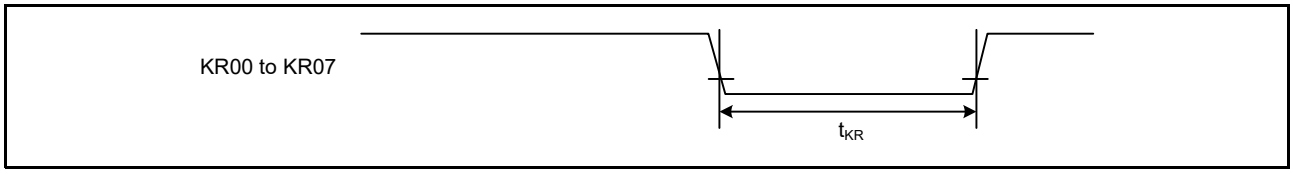


Figure 46.40 Key interrupt input timing

46.3.7 PWM Delay Generation Circuit Timing

Table 46.32 PWM delay generation circuit timing
Conditions: VCC = AVCC0 = 2.7 to 5.5 V 32 MHz ≤ PCLKD ≤ 64 MHz

Parameter		Min	Typ	Max	Unit	Test conditions
Resolution	PCLKD = 64 MHz, DLL Mode = 5-bit mode	-	488	-	ps	-
	PCLKD = 64 MHz, DLL Mode = 4-bit mode	-	976	-	ps	-
	PCLKD = 32 MHz, DLL Mode = 5-bit mode	-	976	-	ps	-
DNL*1, *2		-	5	-	LSB	-

Note 1. The differences among lines in 1-LSB resolution are normalized by this value.
Note 2. The drive capability of the PWM delay generation circuit output port is middle drive.

46.3.8 CAC Timing

Table 46.33 CAC timing

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
CAC	CACREF input pulse width	t_{Pcyc} *1 ≤ t_{cac}*2	t_{CACREF}	4.5 × t_{cac} + 3 × t_{Pcyc}	-	-	ns	-
		t_{Pcyc}*1 > t_{cac}*2		5 × t_{cac} + 6.5 × t_{Pcyc}	-	-	ns	

Note 1. t_{Pcyc}: PCLKB cycle.
Note 2. t_{cac}: CAC count clock source cycle.

46.3.9 SCI Timing

Table 46.34 SCI timing (1)
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter				Symbol	Min	Max	Unit*1	Test conditions
SCI	Input clock cycle	Asynchronous		t_{Scyc}	4	-	t_{Pcyc}	Figure 46.41
		Clock synchronous			6	-		
	Input clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time			t_{SCKr}	-	20	ns	
	Input clock fall time			t_{SCKf}	-	20	ns	
	Output clock cycle	Asynchronous		t_{Scyc}	6	-	t_{Pcyc}	
		Clock synchronous			4	-		
	Output clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		1.8V or above	t_{SCKr}	-	20	ns	
			1.6V or above		-	30		
	Output clock fall time		1.8V or above	t_{SCKf}	-	20	ns	
			1.6V or above		-	30		
	Transmit data delay (master)	Clock synchronous	1.8V or above	t_{TXD}	-	40	ns	Figure 46.42
			1.6V or above		-	45		
	Transmit data delay (slave)	Clock synchronous	2.7V or above		-	55	ns	
			2.4V or above		-	60		
			1.8V or above		-	100		
			1.6V or above		-	125		
	Receive data setup time (master)	Clock synchronous	2.7V or above	t_{RXS}	45	-	ns	
			2.4V or above		55	-		
			1.8V or above		90	-		
			1.6V or above		110	-		
	Receive data setup time (slave)	Clock synchronous	2.7V or above		40	-	ns	
			1.6V or above		45	-		
	Receive data hold time (master)	Clock synchronous		t_{RXH}	5	-	ns	
	Receive data hold time (slave)	Clock synchronous		t_{RXH}	40	-	ns	

Note 1. t_{Pcyc}: PCLKB cycle.

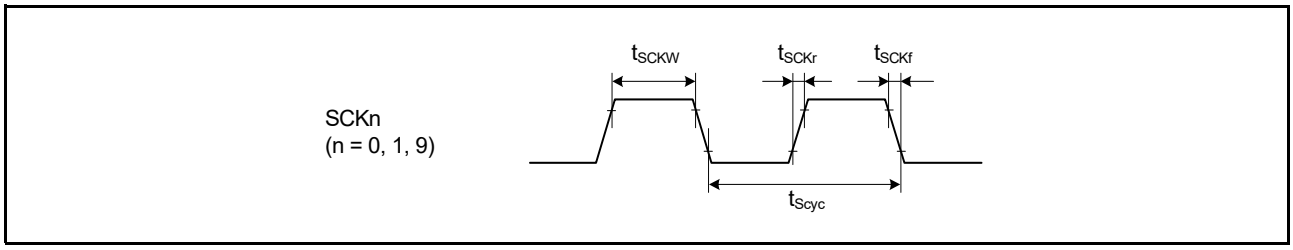


Figure 46.41 SCK clock input timing

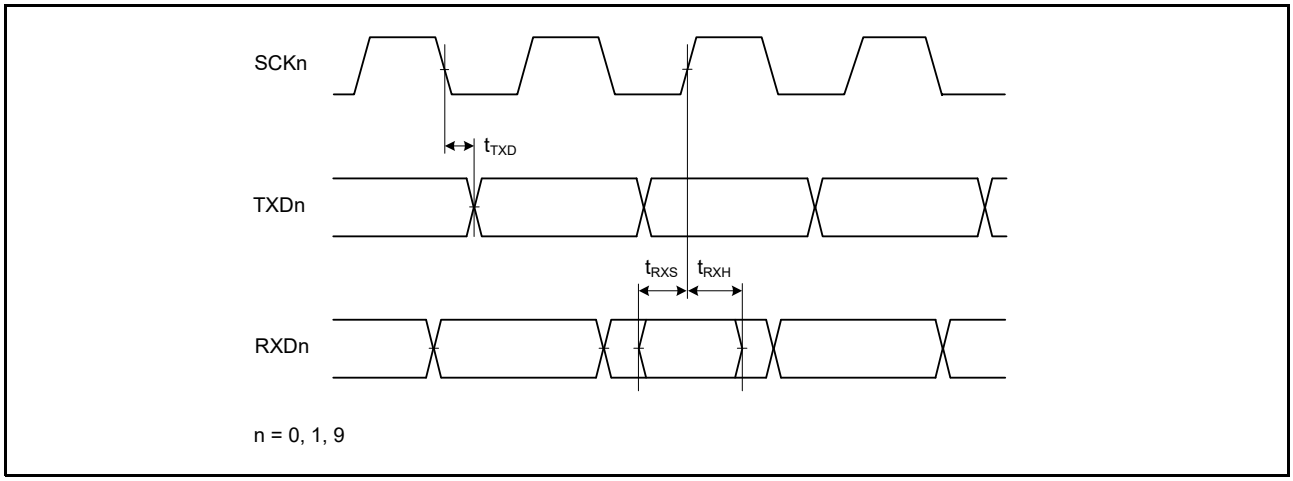


Figure 46.42 SCI input/output timing in clock synchronous mode

Table 46.35 SCI timing (2)
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter				Symbol	Min	Max	Unit*1	Test conditions
Simple SPI	SCK clock cycle output (master)			t_{SPcyc}	4	65536	t_{Pcyc}	Figure 46.43
	SCK clock cycle input (slave)				6	65536		
	SCK clock high pulse width			t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width			t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise and fall time		1.8V or above	t_{SPCKr}, t_{SPCKf}	-	20	ns	
			1.6V or above		-	30		
	Data input setup time	Master	2.7V or above	t_{SU}	45	-	ns	Figure 46.44 to Figure 46.47
			2.4V or above		55	-		
			1.8V or above		80	-		
			1.6V or above		110	-		
		Slave	2.7V or above		40	-		
			1.6V or above		45	-		
	Data input hold time	Master		t_H	33.3	-	ns	
		Slave			40	-		
	SS input setup time			t_{LEAD}	1	-	t_{SPcyc}	
	SS input hold time			t_{LAG}	1	-	t_{SPcyc}	
	Data output delay	Master	1.8V or above	t_{OD}	-	40	ns	
			1.6V or above		-	50		
		Slave	2.4V or above		-	65		
			1.8V or above		-	100		
			1.6V or above		-	125		
	Data output hold time	Master	2.7V or above	t_{OH}	-10	-	ns	
			2.4V or above		-20	-		
			1.8V or above		-30	-		
			1.6V or above		-40	-		
		Slave			-10	-		
	Data rise and fall time	Master		t_{Dr}, t_{Df}	-	20	ns	
		Slave	1.8V or above		-	20		
			1.6V or above		-	30		
Simple SPI	Slave access time			t_{SA}	-	6	t_{Pcyc}	Figure 46.47
	Slave output release time			t_{REL}	-	6	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLKB cycle.

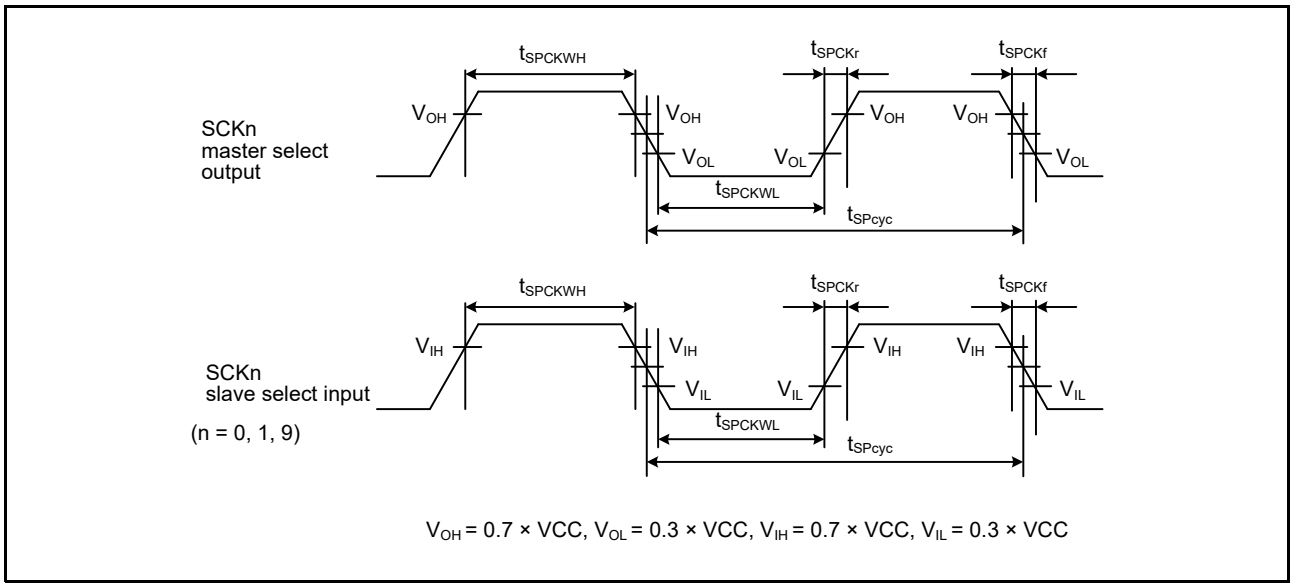


Figure 46.43 SCI simple SPI mode clock timing

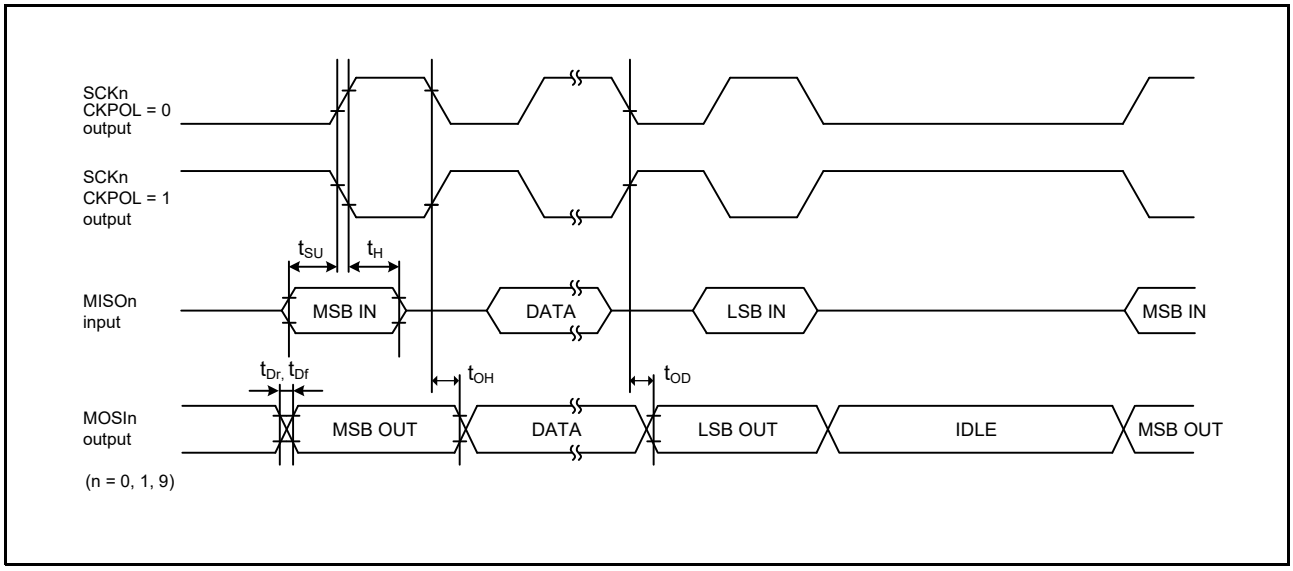


Figure 46.44 SCI simple SPI mode timing (master, CKPH = 1)

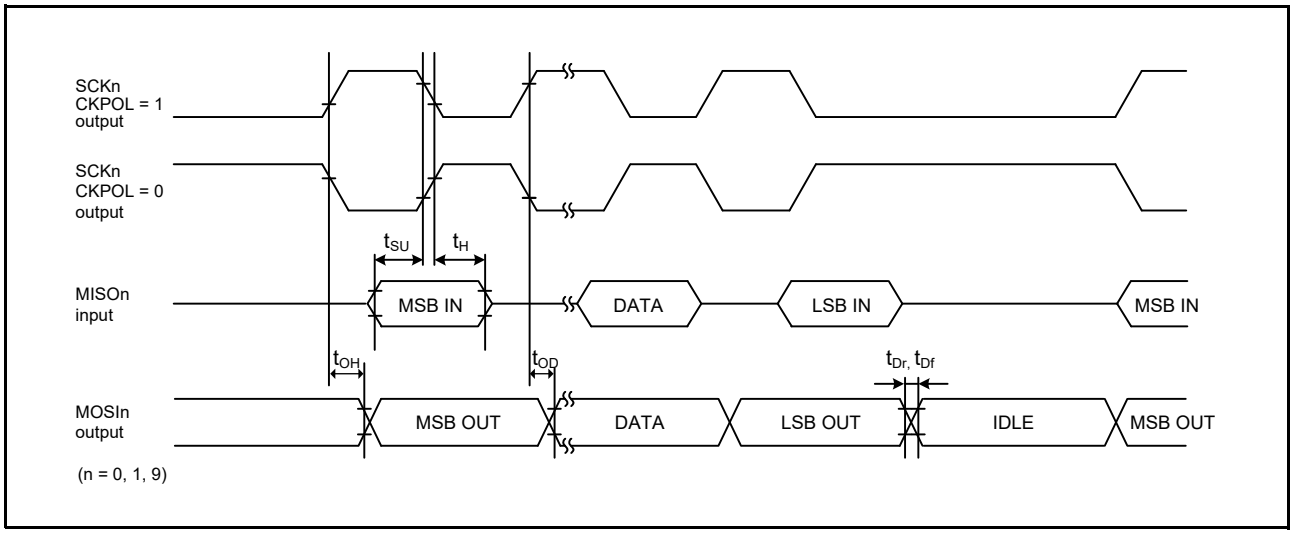


Figure 46.45 SCI simple SPI mode timing (master, CKPH = 0)

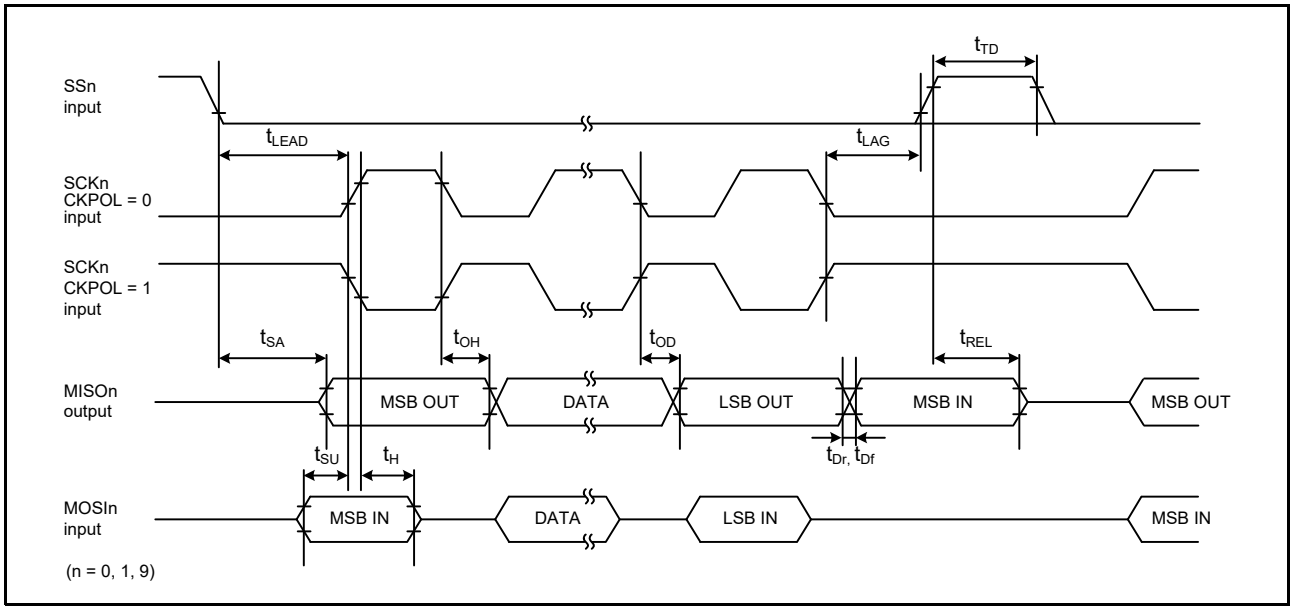


Figure 46.46 SCI simple SPI mode timing (slave, CKPH = 1)

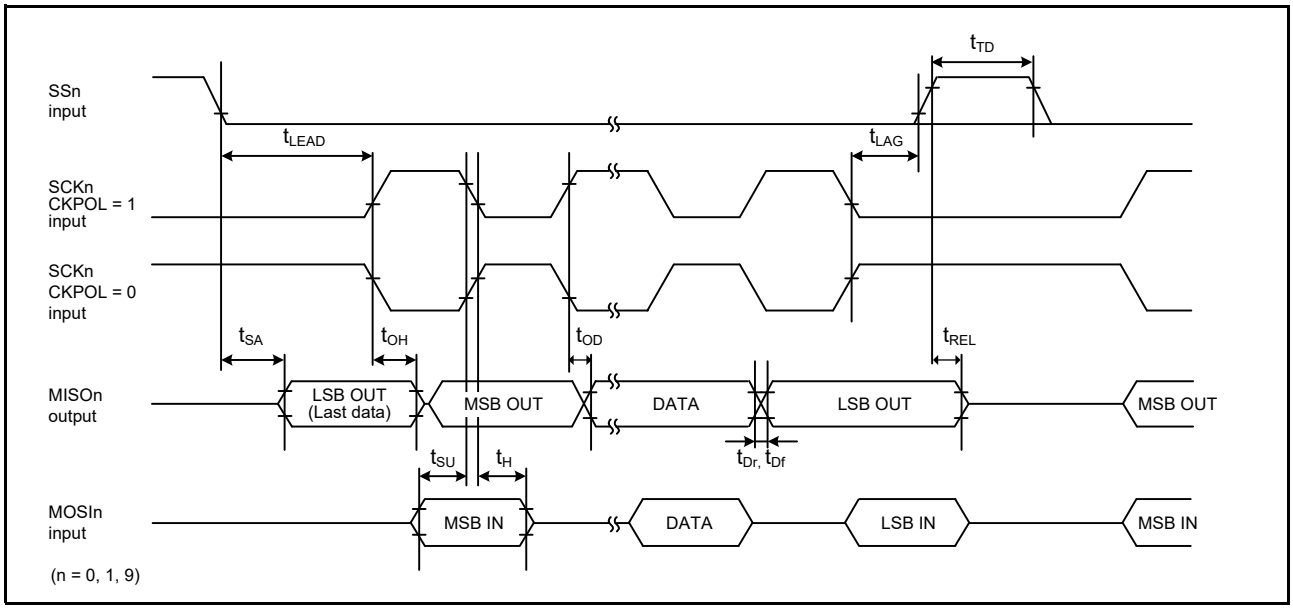


Figure 46.47 SCI simple SPI mode timing (slave, CKPH = 0)

Table 46.36 SCI timing (3)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V

Parameter		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	-	1000	ns	Figure 46.48
	SDA input fall time	t_{Sf}	-	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	250	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b*1	-	400	pF	
Simple IIC (Fast mode)	SDA input rise time	t_{Sr}	-	300	ns	Figure 46.48
	SDA input fall time	t_{Sf}	-	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	100	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b*1	-	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle.

Note 1. Cb indicates the total capacity of the bus line.

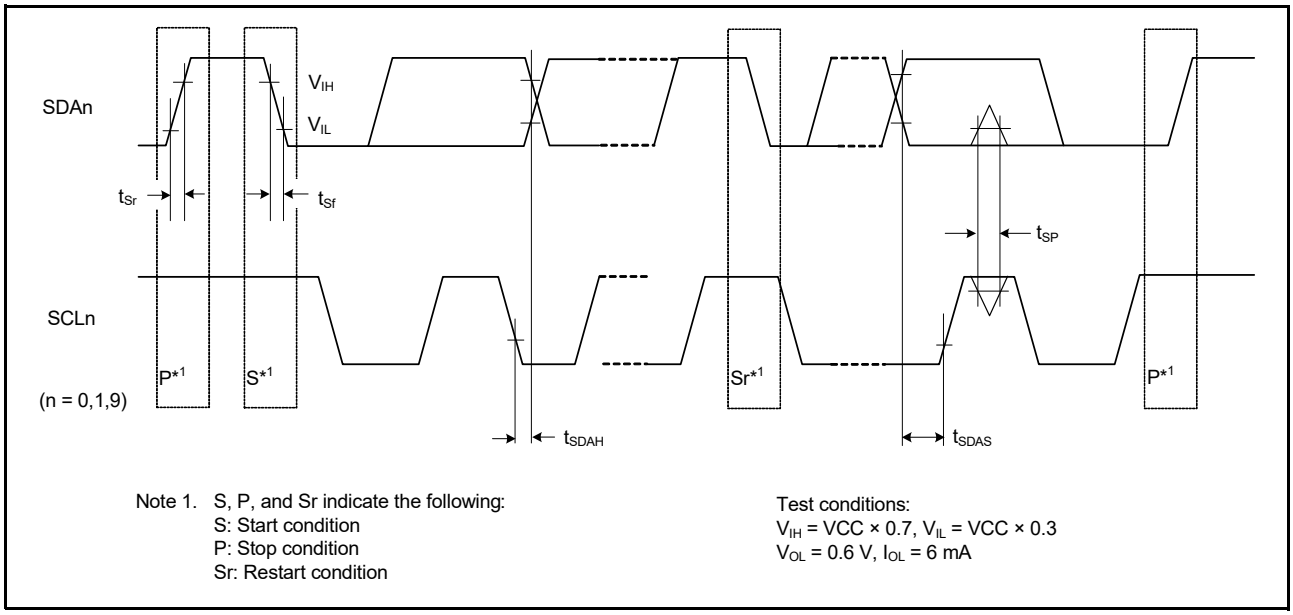


Figure 46.48 SCI simple IIC mode timing

46.3.10 SPI Timing

Table 46.37 SPI timing (1 of 2)

Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter				Symbol	Min	Max	Unit*1	Test conditions
SPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}	Figure 46.49 C = 30pF
		Slave			6	4096		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3	-	ns	
		Slave			3 × t_{Pcyc}	-		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3	-	ns	
		Slave			3 × t_{Pcyc}	-		
	RSPCK clock rise and fall time	Output	2.7V or above	t_{SPCKr}, t_{SPCKf}	-	10	ns	
			2.4V or above		-	15		
			1.8V or above		-	20		
			1.6V or above		-	30		
		Input			-	1	μs	

Table 46.37 SPI timing (2 of 2)

Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter				Symbol	Min	Max	Unit*1	Test conditions
SPI	Data input setup time	Master		t_{SU}	10	-	ns	Figure 46.50 to Figure 46.55 C = 30pF
		Slave	2.4V or above		10	-		
			1.8V or above		15	-		
			1.6V or above		20	-		
	Data input hold time	Master (RSPCK is PCLKB/2)		t_{HF}	0	-	ns	
		Master (RSPCK is not PCLKB/2)		t_{H}	t_{Pcyc}	-		
		Slave		t_{H}	20	-		
	SSL setup time	Master		t_{LEAD}	- 30 + N x t_{Spcyc}*2	-	ns	
		Slave			6 x t_{Pcyc}	-	ns	
	SSL hold time	Master		t_{LAG}	- 30 + N x t_{Spcyc}*3	-	ns	
		Slave			6 x t_{Pcyc}	-	ns	
	Data output delay	Master	2.7V or above	t_{OD}	-	14	ns	Figure 46.50 to Figure 46.55 C = 30pF
			2.4V or above		-	20		
			1.8V or above		-	25		
			1.6V or above		-	30		
		Slave	2.7V or above		-	50		
			2.4V or above		-	60		
			1.8V or above		-	85		
			1.6V or above		-	110		
	Data output hold time	Master		t_{OH}	0	-	ns	
		Slave			0	-		
	Successive transmission delay	Master		t_{TD}	t_{SPcyc} + 2 × t_{Pcyc}	8 × t_{SPcyc} + 2 × t_{Pcyc}	ns	
		Slave			6 × t_{Pcyc}	-		
	MOSI and MISO rise and fall time	Output	2.7V or above	t_{Dr}, t_{Df}	-	10	ns	
			2.4V or above		-	15		
			1.8V or above		-	20		
			1.6V or above		-	30		
		Input			-	1	μs	
	SSL rise and fall time	Output	2.7V or above	t_{SSLr}, t_{SSLf}	-	10	ns	
			2.4V or above		-	15		
			1.8V or above		-	20		
			1.6V or above		-	30		
		Input			-	1	μs	
	Slave access time		2.4V or above	t_{SA}	-	2 × t_{Pcyc} +100	ns	Figure 46.54 and Figure 46.55 C = 30pF
			1.8V or above		-	2 × t_{Pcyc} +140		
			1.6V or above		-	2 × t_{Pcyc} +180		
	Slave output release time		2.4V or above	t_{REL}	-	2 × t_{Pcyc} +100	ns	
			1.8V or above		-	2 × t_{Pcyc} +140		
			1.6V or above		-	2 × t_{Pcyc} +180		

Note 1. t_{Pcyc}: PCLKB cycle.
Note 2. N is set as an integer from 1 to 8 by the SPCKD register.
Note 3. N is set as an integer from 1 to 8 by the SSLND register.

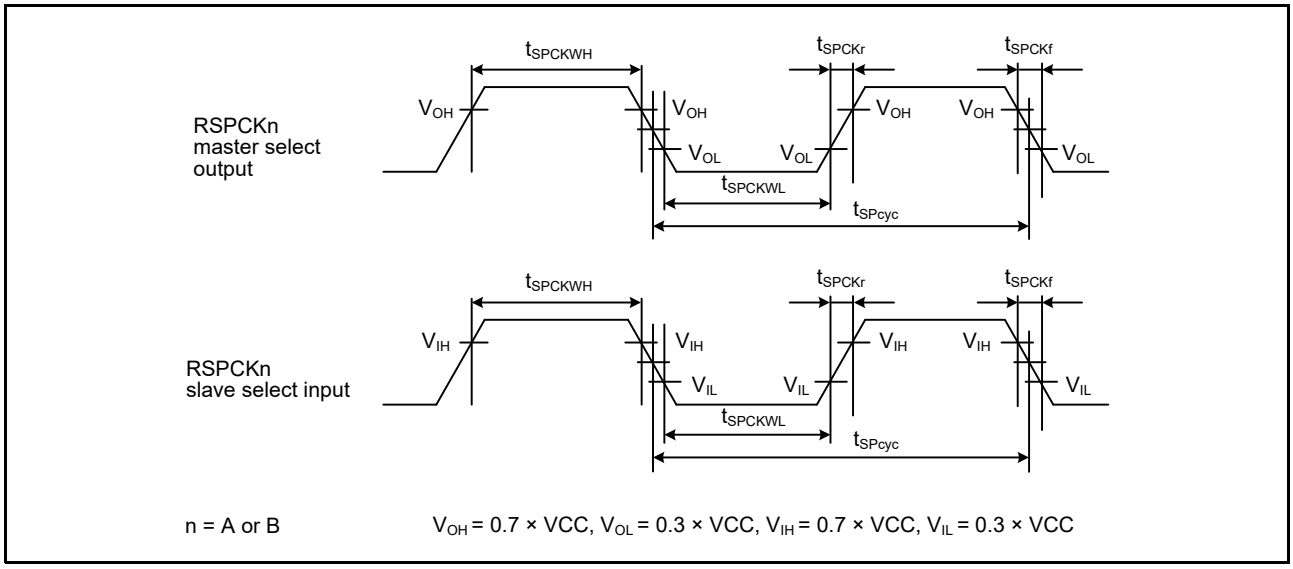


Figure 46.49 SPI clock timing

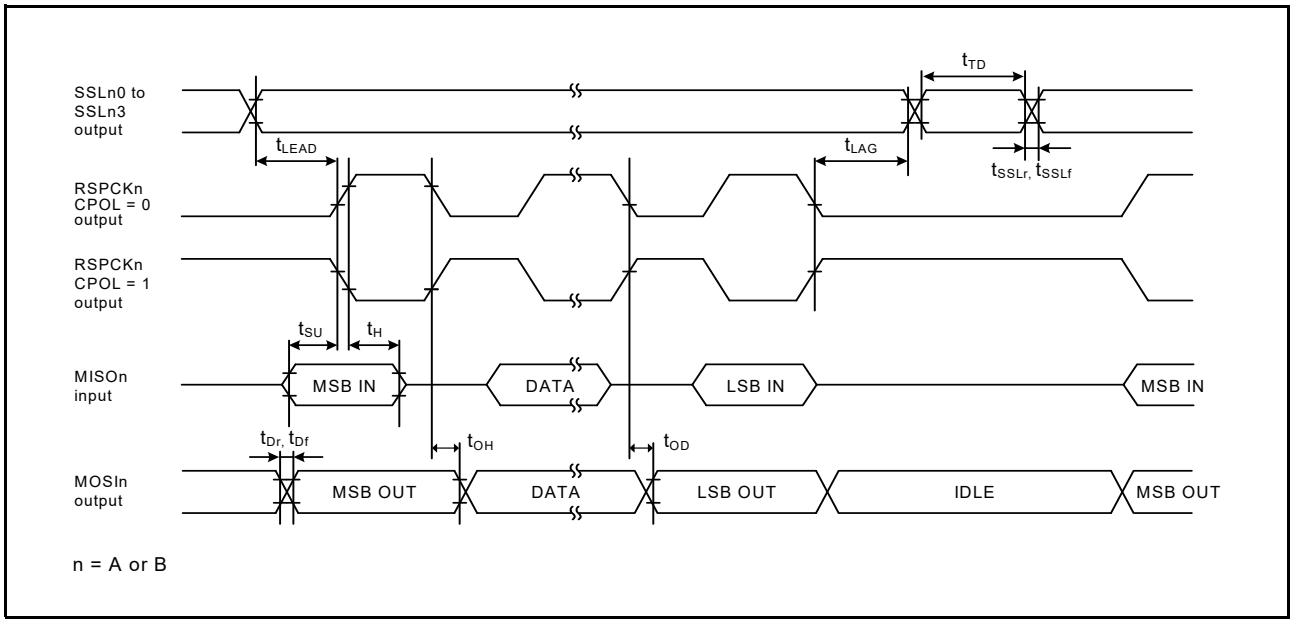


Figure 46.50 SPI timing (master, CPHA = 0) (bit rate: PCLKB division ratio is set to any value other than 1/2)

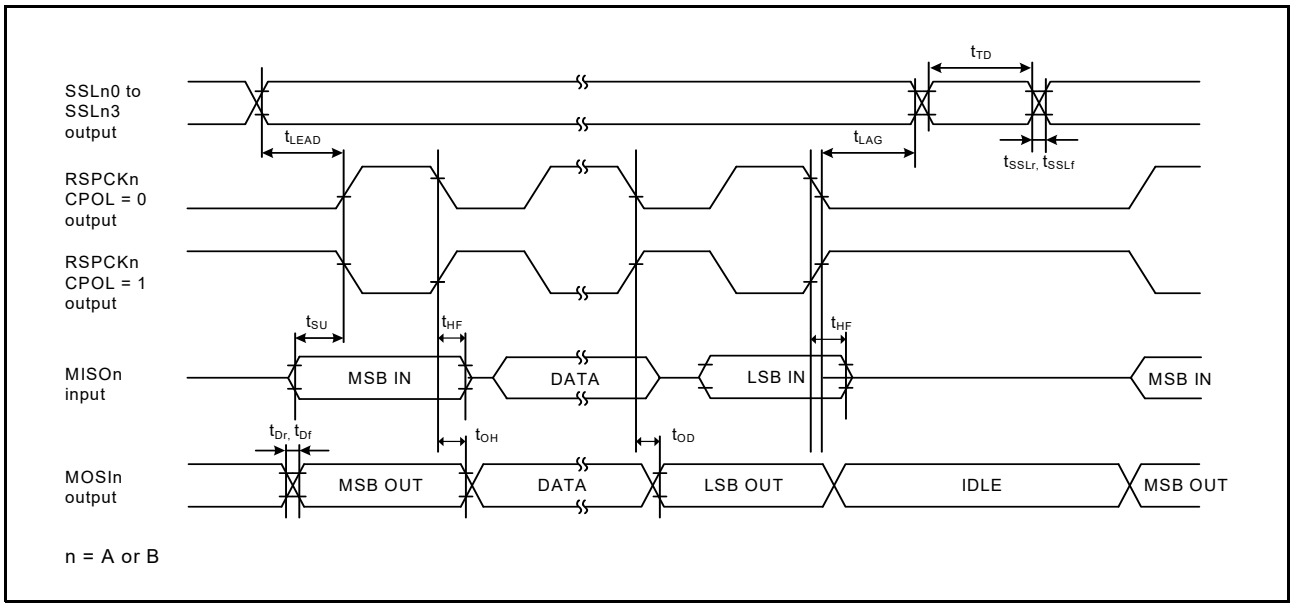


Figure 46.51 SPI timing (master, CPHA = 0) (bit rate: PCLKB division ratio is set to 1/2)

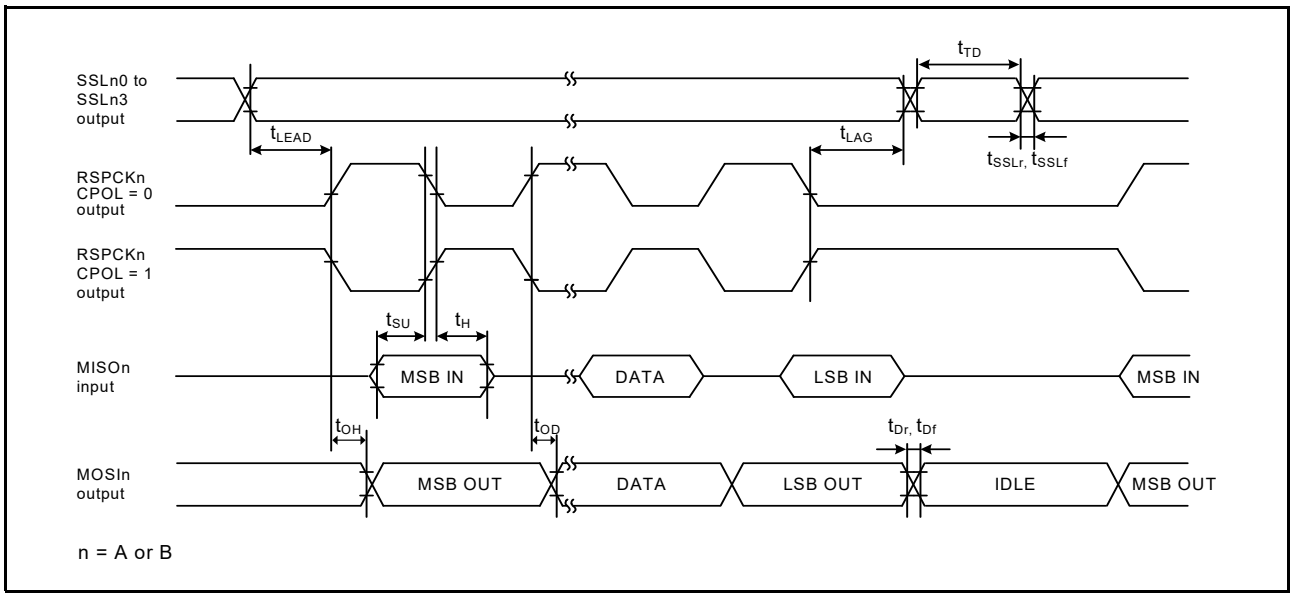


Figure 46.52 SPI timing (master, CPHA = 1) (bit rate: PCLKB division ratio is set to any value other than 1/2)

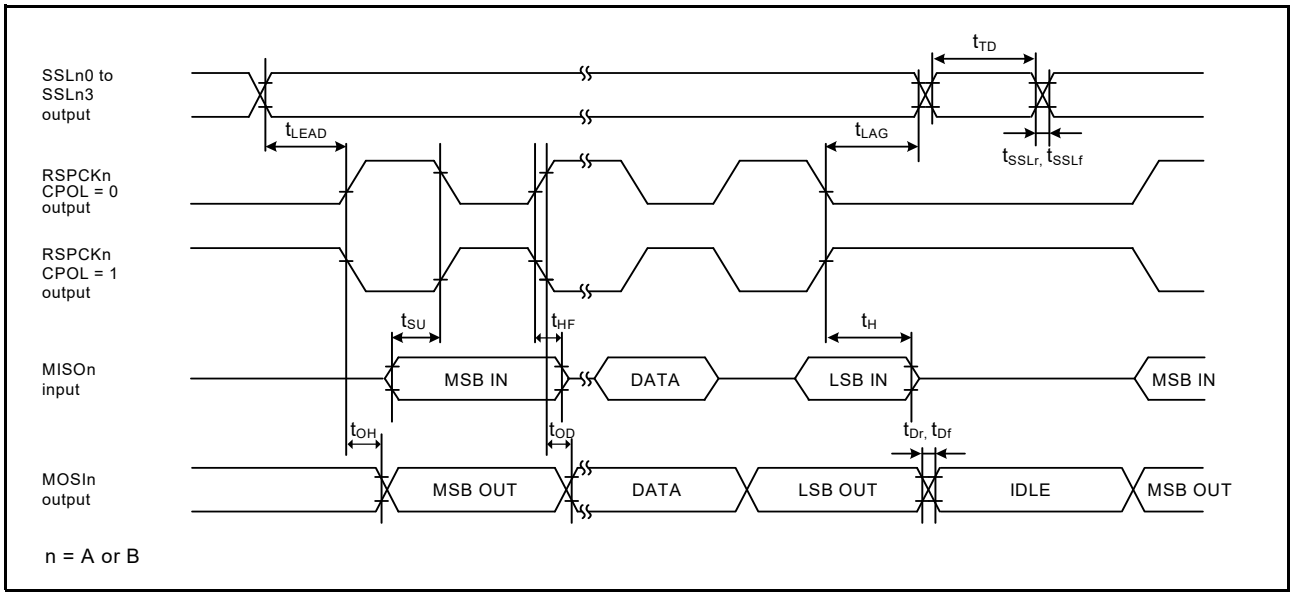


Figure 46.53 SPI timing (master, CPHA = 1) (bit rate: PCLKB division ratio is set to 1/2)

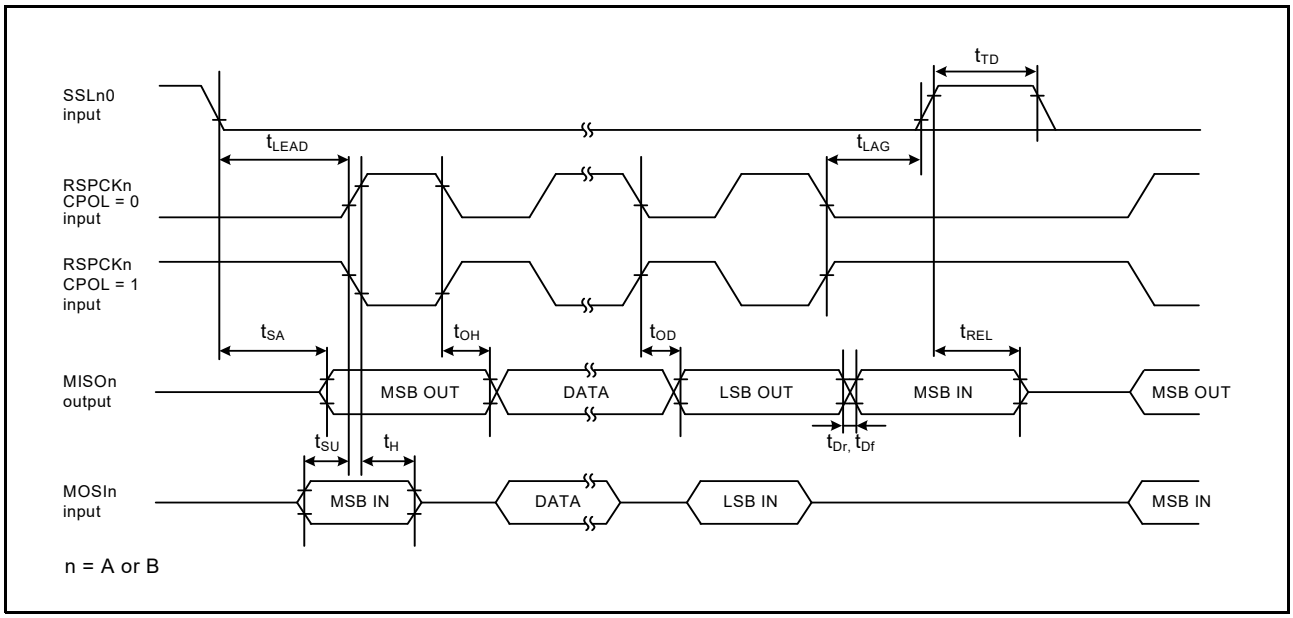


Figure 46.54 SPI timing (slave, CPHA = 0)

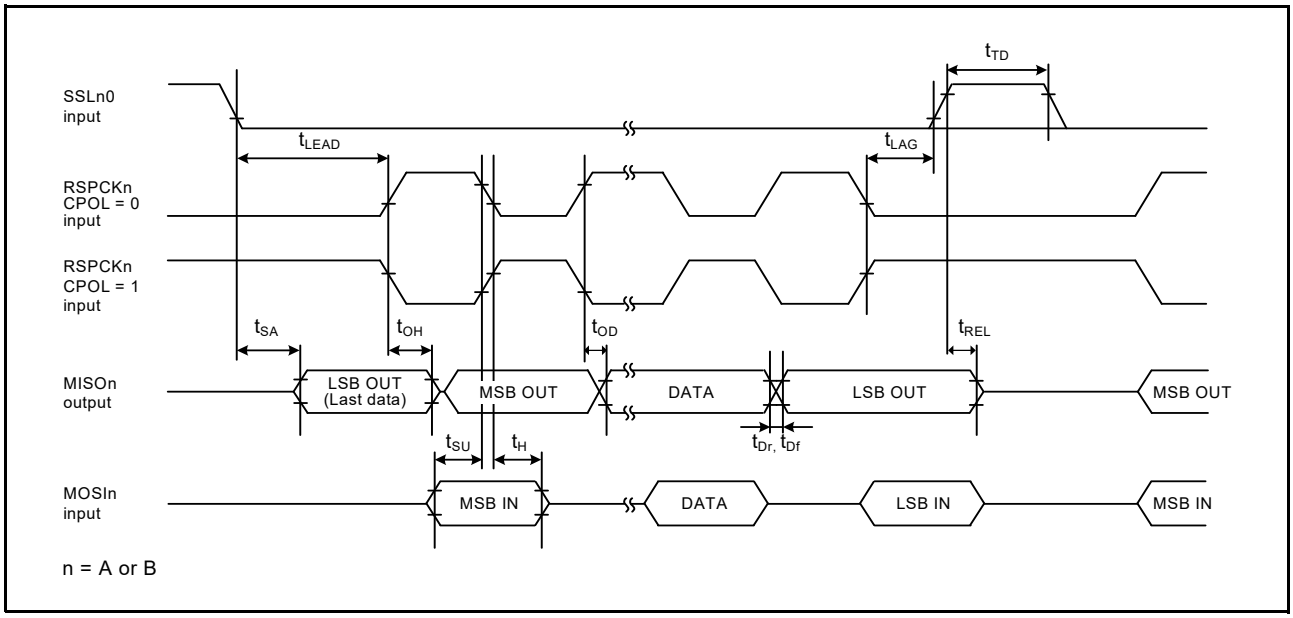


Figure 46.55 SPI timing (slave, CPHA = 1)

46.3.11 IIC Timing

Table 46.38 IIC timing
Conditions: VCC = AVCC0 = 2.7 to 5.5 V

Parameter		Symbol	Min*1	Max	Unit	Test conditions
IIC (standard mode, SMBus)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	-	ns	Figure 46.56
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL, SDA input rise time	t_{Sr}	-	1000	ns	
	SCL, SDA input fall time	t_{Sf}	-	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time (When wakeup function is disabled)	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	SDA input bus free time (When wakeup function is enabled)	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	START condition input hold time (When wakeup function is disabled)	t_{STAH}	t_{IICcyc} + 300	-	ns	
	START condition input hold time (When wakeup function is enabled)	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	Repeated START condition input setup time	t_{STAS}	1000	-	ns	
	STOP condition input setup time	t_{STOS}	1000	-	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	
IIC (Fast mode)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	-	ns	Figure 46.56
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL, SDA input rise time	t_{Sr}	-	300	ns	
	SCL, SDA input fall time	t_{Sf}	-	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time (When wakeup function is disabled)	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	SDA input bus free time (When wakeup function is enabled)	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	START condition input hold time (When wakeup function is disabled)	t_{STAH}	t_{IICcyc} + 300	-	ns	
	START condition input hold time (When wakeup function is enabled)	t_{STAH}	1(5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	Repeated START condition input setup time	t_{STAS}	300	-	ns	
	STOP condition input setup time	t_{STOS}	300	-	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKB cycle

Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.

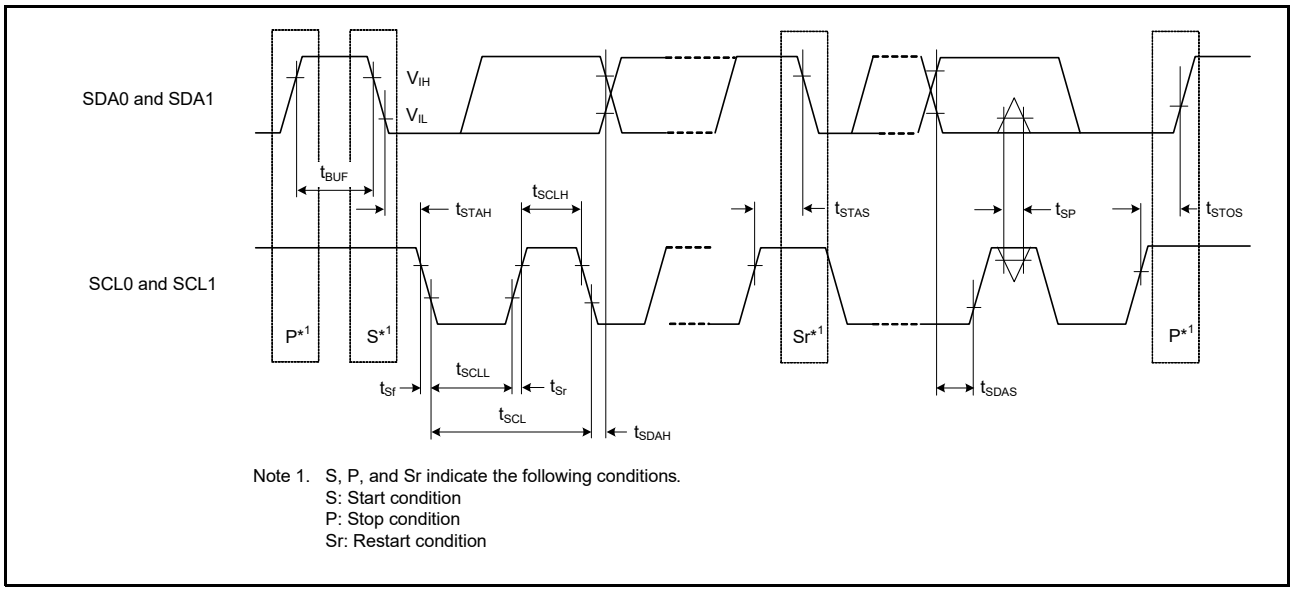


Figure 46.56 I²C bus interface input/output timing

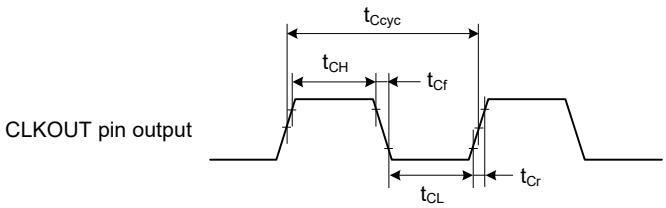
46.3.12 CLKOUT Timing

Table 46.39 CLKOUT timing

Parameter			Symbol	Min	Max	Unit	Test conditions
CLKOUT	CLKOUT pin output cycle*1	VCC = 2.7 V or above	t_{Ccyc}	62.5	-	ns	Figure 46.57
		VCC = 1.8 V or above		125	-		
		VCC = 1.6 V or above		250	-		
	CLKOUT pin high pulse width*2	VCC = 2.7 V or above	t_{CH}	15	-	ns	
		VCC = 1.8 V or above		30	-		
		VCC = 1.6 V or above		150	-		
	CLKOUT pin low pulse width*2	VCC = 2.7 V or above	t_{CL}	15	-	ns	
		VCC = 1.8 V or above		30	-		
		VCC = 1.6 V or above		150	-		
	CLKOUT pin output rise time	VCC = 2.7 V or above	t_{Cr}	-	12	ns	
		VCC = 1.8 V or above		-	25		
		VCC = 1.6 V or above		-	50		
	CLKOUT pin output fall time	VCC = 2.7 V or above	t_{Cf}	-	12	ns	
		VCC = 1.8 V or above		-	25		
		VCC = 1.6 V or above		-	50		

Note 1. When the EXTAL external clock input or an oscillator divided by 1 (the CKOCR.CKOSEL[2:0] bits are 011b and the CKOCR.CKODIV[2:0] bits are 000b) is used for output from CLKOUT, specifications in Table 46.39 should be satisfied with 45% to 55% of input duty cycle.

Note 2. When MOCO is selected as the clock output source (the CKOCR.CKOSEL[2:0] bits are 001b), set the clock output division ratio to 2 (the CKOCR.CKODIV[2:0] bits are 001b).



Test conditions: V_{OH} = VCC × 0.7, V_{OL} = VCC × 0.3, I_{OH} = -1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Figure 46.57 CLKOUT output timing

46.4 USB Characteristics

46.4.1 USBFS Timing

Table 46.40 USB characteristics

Conditions: VCC = AVCC0 = VCC_USB = 3.0 to 3.6 V, Ta = -20 to +85°C

Parameter			Symbol	Min	Max	Unit	Test conditions
Input characteristics	Input high level voltage		V_{IH}	2.0	-	V	-
	Input low level voltage		V_{IL}	-	0.8	V	-
	Differential input sensitivity		V_{DI}	0.2	-	V	| USB_DP - USB_DM |
	Differential common mode range		V_{CM}	0.8	2.5	V	-
Output characteristics	Output high level voltage		V_{OH}	2.8	VCC_USB	V	I_{OH} = -200 μA
	Output low level voltage		V_{OL}	0.0	0.3	V	I_{OL}= 2 mA
	Cross-over voltage		V_{CRS}	1.3	2.0	V	Figure 46.58, Figure 46.59, Figure 46.60
	Rise time	FS	t_r	4	20	ns	
		LS		75	300		
	Fall time	FS	t_f	4	20	ns	
		LS		75	300		
	Rise/fall time ratio	FS	t_r/t_f	90	111.11	%	
		LS		80	125		
	Output resistance		Z_{DRV}	28	44	Ω	(Adjusting the resistance of external elements is not necessary.)
VBUS characteristics	VBUS input voltage		V_{IH}	VCC × 0.8	-	V	-
			V_{IL}	-	VCC × 0.2	V	-
Pull-up, pull-down	Pull-down resistor		R_{PD}	14.25	24.80	kΩ	-
	Pull-up resistor		R_{PUI}	0.9	1.575	kΩ	During idle state
			R_{PUA}	1.425	3.09	kΩ	During reception
Battery Charging Specification Ver 1.2	D + sink current		I_{DP_SINK}	25	175	μA	-
	D - sink current		I_{DM_SINK}	25	175	μA	-
	DCD source current		I_{DP_SRC}	7	13	μA	-
	Data detection voltage		V_{DAT_REF}	0.25	0.4	V	-
	D + source voltage		V_{DP_SRC}	0.5	0.7	V	Output current = 250 μA
	D - source voltage		V_{DM_SRC}	0.5	0.7	V	Output current = 250 μA

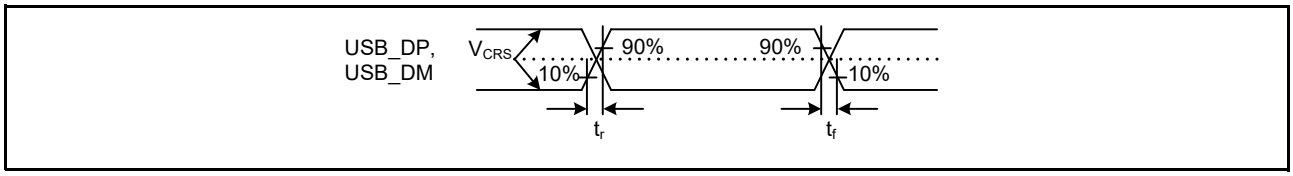


Figure 46.58 USB_DP and USB_DM output timing

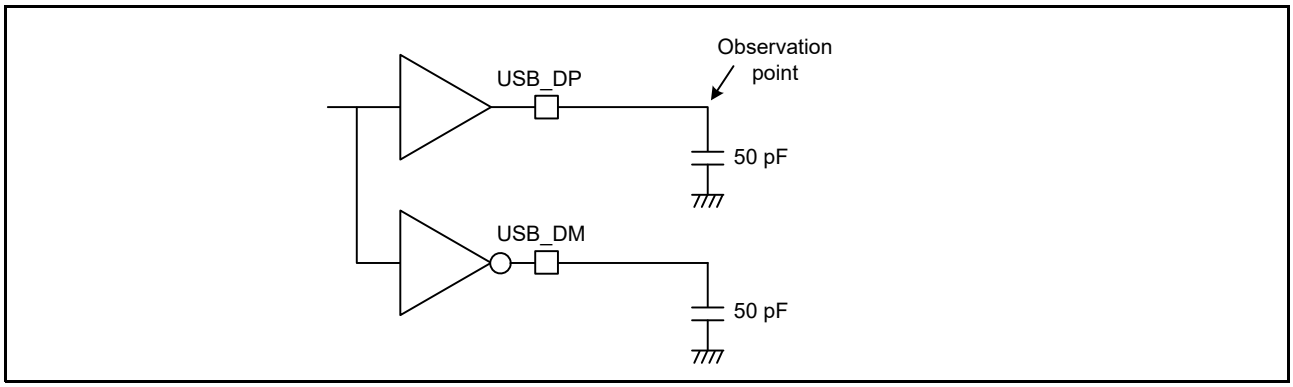


Figure 46.59 Test circuit for Full-Speed (FS) connection

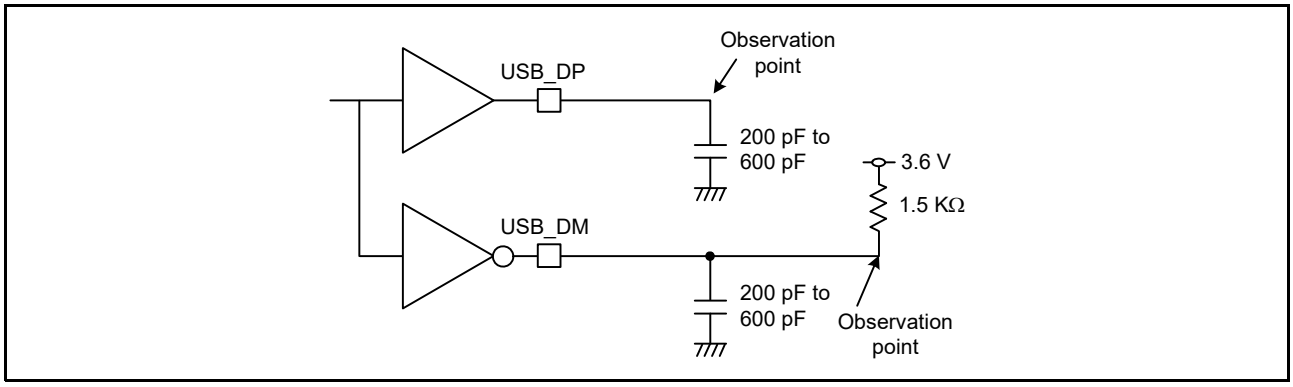


Figure 46.60 Test circuit for Low-Speed (LS) connection

46.4.2 USB External Supply

Table 46.41 USB regulator

Parameter		Min	Typ	Max	Unit	Test conditions
VCC_USB supply current	VCC_USB_LDO ≥ 3.8V	-	-	50	mA	-
	VCC_USB_LDO ≥ 4.5V	-	-	100	mA	-
VCC_USB supply voltage		3.0	-	3.6	V	-

46.5 ADC14 Characteristics

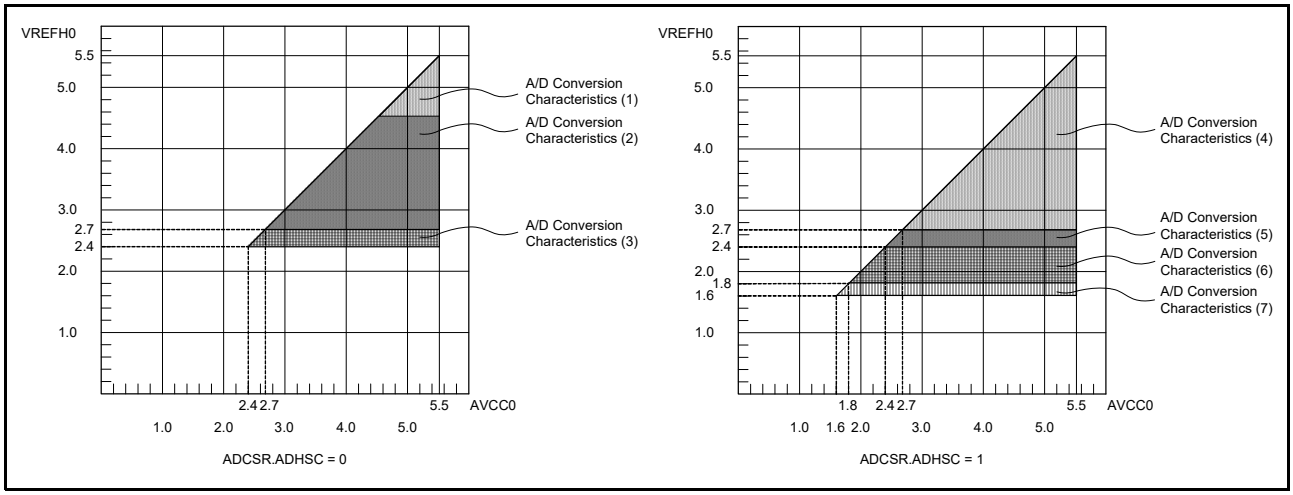


Figure 46.61 AVCC0 to VREFH0 voltage range

Table 46.42 A/D conversion characteristics (1) in high-speed A/D conversion mode (1 of 2)
Conditions: VCC = AVCC0 = 4.5 to 5.5 V, VREFH0 = 4.5 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
Frequency		1	-	64	MHz	-
Analog input capacitance*2	Cs	-	-	8 (reference data)	pF	High-precision channel
		-	-	9 (reference data)	pF	Normal-precision channel
Analog input resistance	Rs	-	-	2.5 (reference data)	kΩ	High-precision channel
		-	-	6.7 (reference data)	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKD = 64 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.70	-	-	μs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		1.13	-	-	μs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-

Table 46.42 A/D conversion characteristics (1) in high-speed A/D conversion mode (2 of 2)
Conditions: VCC = AVCC0 = 4.5 to 5.5 V, VREFH0 = 4.5 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
Conversion time*1 (Operation at PCLKD = 64 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.80	-	-	μs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		1.22	-	-	μs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±2.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Full-scale error		-	±3.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±5.0	±20	LSB	High-precision channel
				±32.0	LSB	Other than above
DNL differential nonlinearity error		-	±4.0	-	LSB	-
INL integral nonlinearity error		-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (Cin), see section section 46.2.4, I/O VOH, VOL, and Other Characteristics.

Table 46.43 A/D conversion characteristics (2) in high-speed A/D conversion mode (1 of 2)
Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
Frequency		1	-	48	MHz	-
Analog input capacitance*2	Cs	-	-	8 (reference data)	pF	High-precision channel
		-	-	9 (reference data)	pF	Normal-precision channel
Analog input resistance	Rs	-	-	2.5 (reference data)	kΩ	High-precision channel
		-	-	6.7 (reference data)	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKD = 48 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.94	-	-	μs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		1.50	-	-	μs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above

Table 46.43 A/D conversion characteristics (2) in high-speed A/D conversion mode (2 of 2)
Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-
Conversion time*1 (Operation at PCLKD = 48 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	1.06	-	-	μs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		1.63	-	-	μs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±2.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Full-scale error		-	±3.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±5.0	±20	LSB	High-precision channel
				±32.0	LSB	Other than above
DNL differential nonlinearity error		-	±4.0	-	LSB	-
INL integral nonlinearity error		-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (Cin), see section 46.2.4, I/O VOH, VOL, and Other Characteristics.

Table 46.44 A/D conversion characteristics (3) in high-speed A/D conversion mode (1 of 2)
Conditions: VCC = AVCC0 = 2.4 to 5.5 V, VREFH0 = 2.4 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
Frequency		1	-	32	MHz	-
Analog input capacitance*2	Cs	-	-	8 (reference data)	pF	High-precision channel
		-	-	9 (reference data)	pF	Normal-precision channel
Analog input resistance	Rs	-	-	2.5 (reference data)	kΩ	High-precision channel
		-	-	6.7 (reference data)	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-

Table 46.44 A/D conversion characteristics (3) in high-speed A/D conversion mode (2 of 2)
Conditions: VCC = AVCC0 = 2.4 to 5.5 V, VREFH0 = 2.4 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
Conversion time*1 (Operation at PCLKD = 32 MHz)	Permissible signal source impedance Max. = 1.3 kΩ	1.41	-	-	μs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		2.25	-	-	μs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-
Conversion time*1 (Operation at PCLKD = 32 MHz)	Permissible signal source impedance Max. = 1.3 kΩ	1.59	-	-	μs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		2.44	-	-	μs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±2.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Full-scale error		-	±3.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±5.0	±20	LSB	High-precision channel
				±32.0	LSB	Other than above
DNL differential nonlinearity error		-	±4.0	-	LSB	-
INL integral nonlinearity error		-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (Cin), see section 46.2.4, I/O VOH, VOL, and Other Characteristics.

Table 46.45 A/D conversion characteristics (4) in low-power A/D conversion mode (1 of 2)
Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
Frequency		1	-	24	MHz	-
Analog input capacitance*2	Cs	-	-	8 (reference data)	pF	High-precision channel
		-	-	9 (reference data)	pF	Normal-precision channel

Table 46.45 A/D conversion characteristics (4) in low-power A/D conversion mode (2 of 2)
Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
Analog input resistance	Rs	-	-	2.5 (reference data)	kΩ	High-precision channel
		-	-	6.7 (reference data)	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKD = 24 MHz)	Permissible signal source impedance Max. = 1.1 kΩ	2.25	-	-	μs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		3.38	-	-	μs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-
Conversion time*1 (Operation at PCLKD = 24 MHz)	Permissible signal source impedance Max. = 1.1 kΩ	2.50	-	-	μs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		3.63	-	-	μs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±2.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Full-scale error		-	±3.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±5.0	±20	LSB	High-precision channel
				±32.0	LSB	Other than above
DNL differential nonlinearity error		-	±4.0	-	LSB	-
INL integral nonlinearity error		-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (Cin), seesection 46.2.4, I/O VOH, VOL, and Other Characteristics.

Table 46.46 A/D conversion characteristics (5) in low-power A/D conversion mode
Conditions: VCC = AVCC0 = 2.4 to 5.5 V, VREFH0 = 2.4 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
Frequency		1	-	16	MHz	-
Analog input capacitance*2	Cs	-	-	8 (reference data)	pF	High-precision channel
		-	-	9 (reference data)	pF	Normal-precision channel
Analog input resistance	Rs	-	-	2.5 (reference data)	kΩ	High-precision channel
		-	-	6.7 (reference data)	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKD = 16 MHz)	Permissible signal source impedance Max. = 2.2 kΩ	3.38	-	-	μs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		5.06	-	-	μs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-
Conversion time*1 (Operation at PCLKD = 16 MHz)	Permissible signal source impedance Max. = 2.2 kΩ	3.75	-	-	μs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		5.44	-	-	μs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±2.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Full-scale error		-	±3.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±5.0	±20	LSB	High-precision channel
				±32.0	LSB	Other than above
DNL differential nonlinearity error		-	±4.0	-	LSB	-
INL integral nonlinearity error		-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute

accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (Cin), see section 46.2.4, I/O VOH, VOL, and Other Characteristics.

Table 46.47 A/D conversion characteristics (6) in low-power A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = 1.8 to 5.5 V (AVCC0 = VCC when VCC < 2.0 V), VREFH0 = 1.8 to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
Frequency		1	-	8	MHz	-
Analog input capacitance*2	Cs	-	-	8 (reference data)	pF	High-precision channel
		-	-	9 (reference data)	pF	Normal-precision channel
Analog input resistance	Rs	-	-	3.8 (reference data)	kΩ	High-precision channel
		-	-	8.2 (reference data)	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKD = 8 MHz)	Permissible signal source impedance Max. = 5 kΩ	6.75	-	-	μs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		10.13	-	-	μs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±1.0	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than above
Full-scale error		-	±1.5	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±3.0	±8.0	LSB	High-precision channel
				±12.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-
Conversion time*1 (Operation at PCLKD = 8 MHz)	Permissible signal source impedance Max. = 5 kΩ	7.50	-	-	μs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		10.88	-	-	μs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±4.0	±30.0	LSB	High-precision channel
				±40.0	LSB	Other than above
Full-scale error		-	±6.0	±30.0	LSB	High-precision channel
				±40.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-

Table 46.47 A/D conversion characteristics (6) in low-power A/D conversion mode (2 of 2)
Conditions: VCC = AVCC0 = 1.8 to 5.5 V (AVCC0 = VCC when VCC < 2.0 V), VREFH0 = 1.8 to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter	Min	Typ	Max	Unit	Test Conditions
Absolute accuracy	-	±12.0	±32.0	LSB	High-precision channel
			±48.0	LSB	Other than above
DNL differential nonlinearity error	-	±4.0	-	LSB	-
INL integral nonlinearity error	-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (Cin), see section 46.2.4, I/O VOH, VOL, and Other Characteristics.

Table 46.48 A/D conversion characteristics (7) in low-power A/D conversion mode (1 of 2)
Conditions: VCC = AVCC0 = 1.6 to 5.5 V (AVCC0 = VCC when VCC < 2.0 V), VREFH0 = 1.6 to 5.5 V, VSS = AVSS0 = VREFL0 = 0
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
Frequency		1	-	4	MHz	-
Analog input capacitance*2	Cs	-	-	8 (reference data)	pF	High-precision channel
		-	-	9 (reference data)	pF	Normal-precision channel
Analog input resistance	Rs	-	-	13.1 (reference data)	kΩ	High-precision channel
		-	-	14.3 (reference data)	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKD = 4 MHz)	Permissible signal source impedance Max. = 9.9 kΩ	13.5	-	-	μs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		20.25	-	-	μs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±1.0	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than above
Full-scale error		-	±1.5	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±3.0	±8.0	LSB	High-precision channel
				±12.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-

Table 46.48 A/D conversion characteristics (7) in low-power A/D conversion mode (2 of 2)
Conditions: VCC = AVCC0 = 1.6 to 5.5 V (AVCC0 = VCC when VCC < 2.0 V), VREFH0 = 1.6 to 5.5 V, VSS = AVSS0 = VREFL0 = 0
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
Conversion time*1 (Operation at PCLKD = 4 MHz)	Permissible signal source impedance Max. = 9.9 kΩ	15.0	-	-	μs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		21.75	-	-	μs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±4.0	±30.0	LSB	High-precision channel
				±40.0	LSB	Other than above
Full-scale error		-	±6.0	±30.0	LSB	High-precision channel
				±40.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±12.0	±32.0	LSB	High-precision channel
				±48.0	LSB	Other than above
DNL differential nonlinearity error		-	±4.0	-	LSB	-
INL integral nonlinearity error		-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (Cin), see section 46.2.4, I/O VOH, VOL, and Other Characteristics.

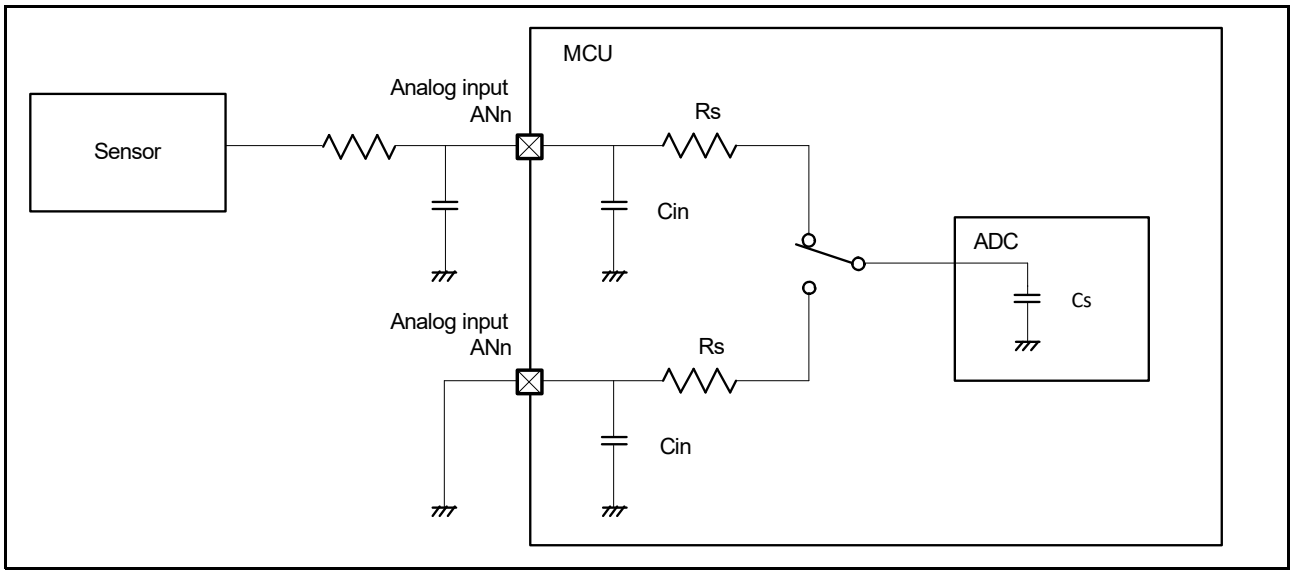


Figure 46.62 Equivalent circuit for analog input

Table 46.49 14-bit A/D converter channel classification (1 of 2)

Classification	Channel	Conditions	Remarks
High-precision channel	AN000 to AN013	AVCC0 = 1.6 to 5.5 V	Pins AN000 to AN013 cannot be used as general I/O, IRQ2 input, or for TS transmission when the A/D converter is in use.
Normal-precision channel	AN016 to AN022		-
Internal reference voltage input channel	Internal reference voltage	AVCC0 = 2.0 to 5.5 V	-

Table 46.49 14-bit A/D converter channel classification (2 of 2)

Classification	Channel	Conditions	Remarks
Temperature sensor input channel	Temperature sensor output	AVCC0 = 2.0 to 5.5 V	-

Table 46.50 A/D internal reference voltage characteristics

Conditions: VCC = AVCC0 = VREFH0 = 2.0 to 5.5 V*1

Parameter	Min	Typ	Max	Unit	Test conditions
Internal reference voltage input channel*2	1.36	1.43	1.50	V	-
Frequency*3	1	-	2	MHz	-
Sampling time*4	5.0	-	-	μs	-

Note 1. The internal reference voltage cannot be selected for input channels when AVCC0 < 2.0 V.

Note 2. The 14-bit A/D internal reference voltage indicates the voltage when the internal reference voltage is input to the 14-bit A/D converter.

Note 3. This is a parameter for ADC14 when the internal reference voltage is used as the high-potential reference voltage.

Note 4. This is a parameter for ADC14 when the internal reference voltage is selected for an analog input channel in ADC14.

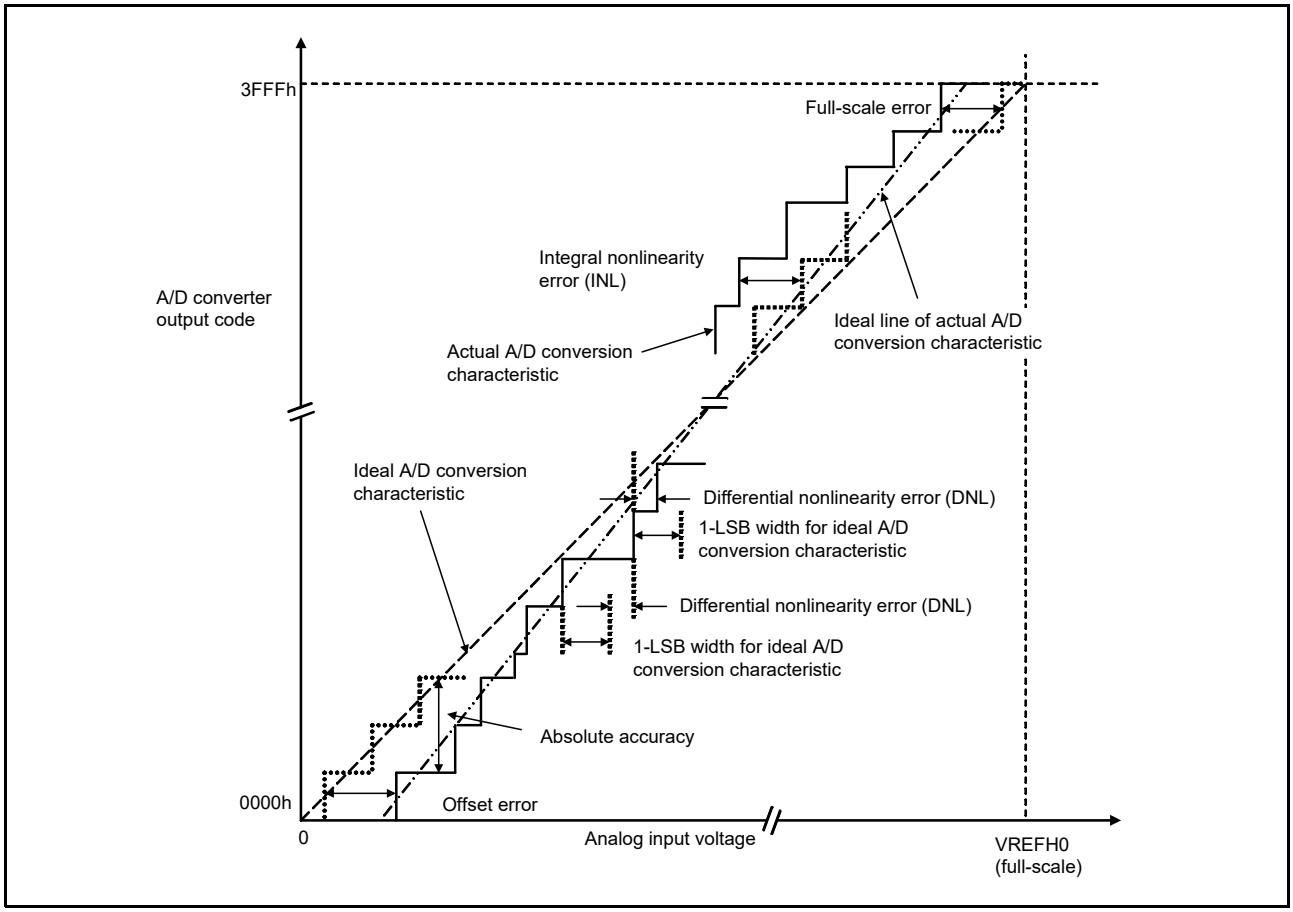


Figure 46.63 Illustration of 14-bit A/D converter characteristic terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of the analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as the analog input voltage. For example, if 12-bit resolution is used and the reference voltage VREFH0 = 3.072 V, then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If analog input voltage is 6 mV, an absolute accuracy of ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh, though an output code of 008h can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

46.6 DAC8 Characteristics

Table 46.51 D/A conversion characteristics
Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter		Min	Typ	Max	Unit	Test conditions
Resolution		-	-	8	bit	-
Charge pump stabilization time		-	-	100	μs	-
Conversion time	VCC = 2.7 to 5.5V	-	-	3.0	μs	35-pF capacitive load
	VCC = 1.8 to 2.7V	-	-	6.0	μs	
Absolute accuracy	VCC = 2.4 to 5.5V	-	-	±3.0	LSB	2-MΩ resistive load
	VCC = 1.8 to 2.4V	-	-	±3.5		
	VCC = 2.4 to 5.5V	-	-	±2.0	LSB	4-MΩ resistive load
	VCC = 1.8 to 2.4V	-	-	±2.5		
RO output resistance		-	7.4	-	kΩ	-

46.7 TSN Characteristics

Table 46.52 TSN characteristics
Conditions: VCC = AVCC0 = 2.0 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	-	-	±1.5	-	°C	2.4 V or above
		-	±2.0	-	°C	Below 2.4 V
Temperature slope	-	-	-3.65	-	mV/°C	-
Output voltage (at 25°C)	-	-	1.05	-	V	VCC = 3.3 V
Temperature sensor start time	t_{START}	-	-	5	μs	-
Sampling time	-	5	-	-	μs	

46.8 OSC Stop Detect Characteristics

Table 46.53 Oscillation stop detection circuit characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Detection time	t_{dr}	-	-	1	ms	Figure 46.64

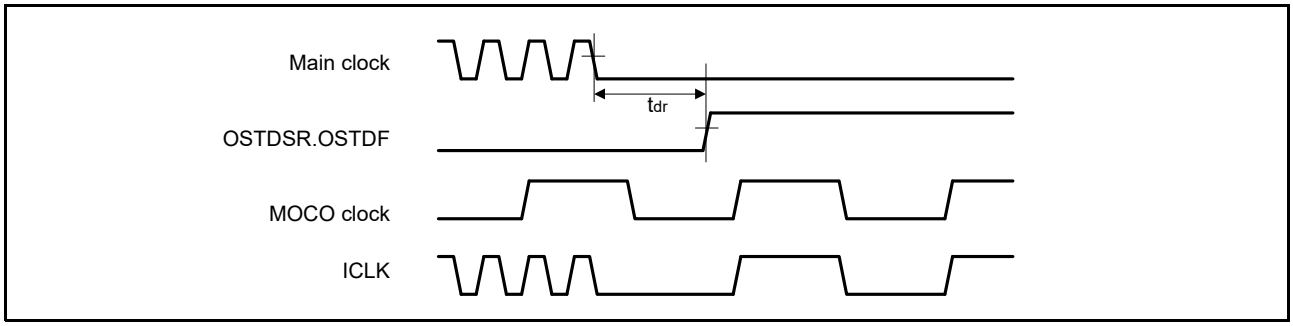


Figure 46.64 Oscillation stop detection timing

46.9 POR and LVD Characteristics

Table 46.54 Power-on reset circuit and voltage detection circuit characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Voltage detection level*1	Power-on reset (POR)	V_{POR}	1.27	1.42	1.57	V	Figure 46.65, Figure 46.66
	Voltage detection circuit (LVD0)*2	V_{det0_0}	3.68	3.85	4.00	V	Figure 46.67 At falling edge VCC
		V_{det0_1}	2.68	2.85	2.96		
		V_{det0_2}	2.38	2.53	2.64		
		V_{det0_3}	1.78	1.90	2.02		
		V_{det0_4}	1.60	1.69	1.82		
	Voltage detection circuit (LVD1)*3	V_{det1_0}	4.13	4.29	4.45	V	Figure 46.68 At falling edge VCC
		V_{det1_1}	3.98	4.16	4.30		
		V_{det1_2}	3.86	4.03	4.18		
		V_{det1_3}	3.68	3.86	4.00		
		V_{det1_4}	2.98	3.10	3.22		
		V_{det1_5}	2.89	3.00	3.11		
		V_{det1_6}	2.79	2.90	3.01		
		V_{det1_7}	2.68	2.79	2.90		
		V_{det1_8}	2.58	2.68	2.78		
		V_{det1_9}	2.48	2.58	2.68		
		V_{det1_A}	2.38	2.48	2.58		
		V_{det1_B}	2.10	2.20	2.30		
		V_{det1_C}	1.84	1.96	2.05		
		V_{det1_D}	1.74	1.86	1.95		
		V_{det1_E}	1.63	1.75	1.84		
		V_{det1_F}	1.60	1.65	1.73		
	Voltage detection circuit (LVD2)*4	V_{det2_0}	4.11	4.31	4.48	V	Figure 46.69 At falling edge VCC
		V_{det2_1}	3.97	4.17	4.34		
		V_{det2_2}	3.83	4.03	4.20		
		V_{det2_3}	3.64	3.84	4.01		

Note 1. These characteristics apply when noise is not superimposed on the power supply. When a setting causes this voltage detection level to overlap with that of the voltage detection circuit, it cannot be specified whether LVD1 or LVD2 is used for voltage detection.

Note 2. # in the symbol $V_{det0_\#}$ denotes the value of the OFS1.VDSEL1[2:0] bits.

Note 3. # in the symbol $V_{det1_\#}$ denotes the value of the LVDLVLR.LVD1LVL[4:0] bits.

Note 4. # in the symbol $V_{det2_\#}$ denotes the value of the LVDLVLR.LVD2LVL[2:0] bits.

Table 46.55 Power-on reset circuit and voltage detection circuit characteristics (2) (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Wait time after power-on reset cancellation	LVD0:enable	t_{POR}	-	1.7	-	ms	-
	LVD0:disable	t_{POR}	-	1.3	-	ms	-
Wait time after voltage monitor 0,1,2 reset cancellation	LVD0:enable*1	$t_{LVD0,1,2}$	-	0.6	-	ms	-
	LVD0:disable*2	$t_{LVD1,2}$	-	0.2	-	ms	-
Response delay*3		t_{det}	-	-	350	μs	Figure 46.65, Figure 46.66
Minimum VCC down time		t_{VOFF}	450	-	-	μs	Figure 46.65, VCC = 1.0 V or above

Table 46.55 Power-on reset circuit and voltage detection circuit characteristics (2) (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Power-on reset enable time	$t_{W\ (POR)}$	1	-	-	ms	Figure 46.66, VCC = below 1.0 V
LVD operation stabilization time (after LVD is enabled)	$T_{d\ (E-A)}$	-	-	300	μs	Figure 46.68, Figure 46.69
Hysteresis width (POR)	V_{PORH}	-	110	-	mV	-
Hysteresis width (LVD0, LVD1 and LVD2)	V_{LVH}	-	60	-	mV	LVD0 selected
		-	100	-		V_{det1_0} to V_{det1_2} selected.
		-	60	-		V_{det1_3} to V_{det1_9} selected.
		-	50	-		V_{det1_A} to V_{det1_B} selected.
		-	40	-		V_{det1_C} to V_{det1_F} selected.
		-	60	-		LVD2 selected

Note 1. When OFS1.LVDAS = 0
Note 2. When OFS1.LVDAS = 1
Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for the POR/LVD.

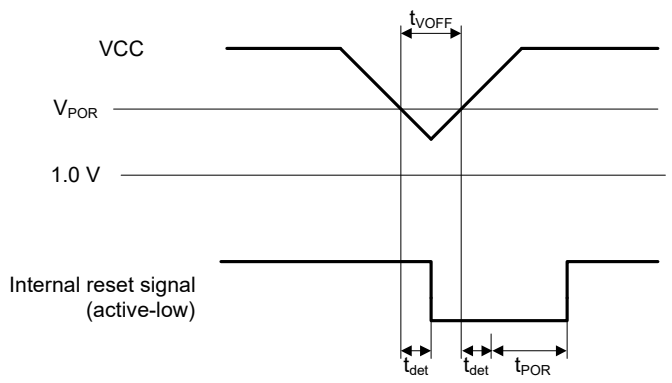
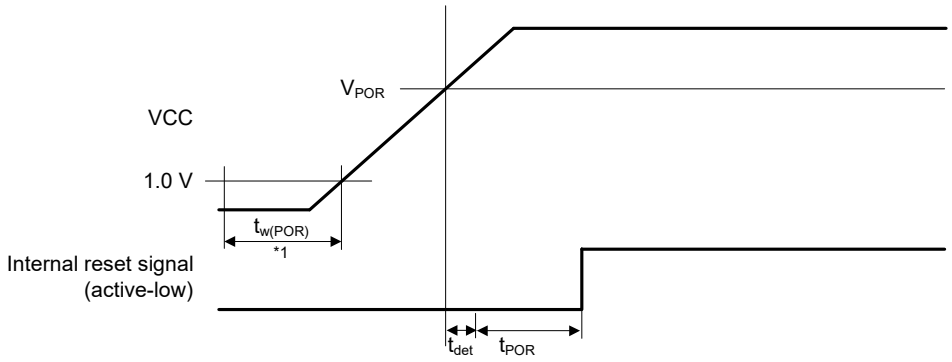


Figure 46.65 Voltage detection reset timing



Note: $t_{W(POR)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When VCC turns on, maintain $t_{W(POR)}$ for 1.0 ms or more.

Figure 46.66 Power-on reset timing

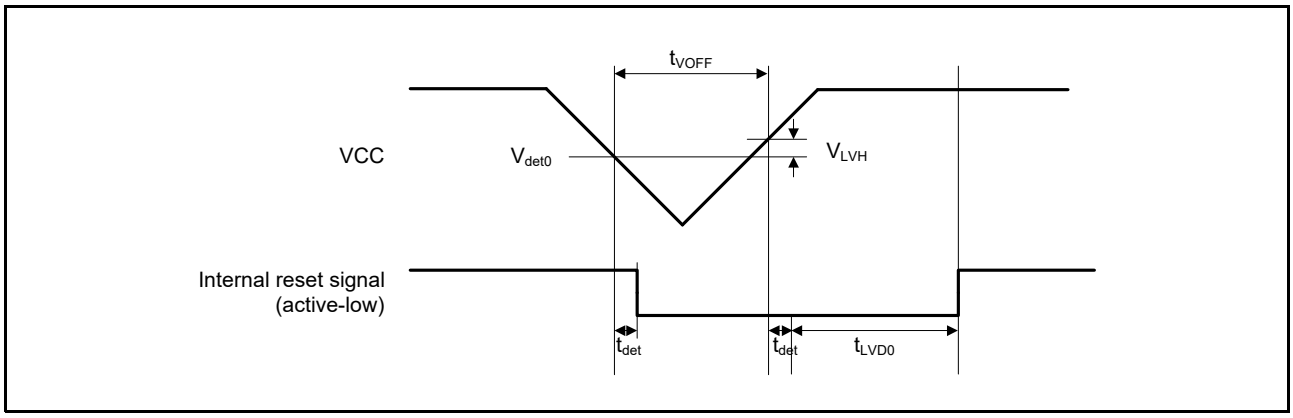


Figure 46.67 Voltage detection circuit timing (V_{det0})

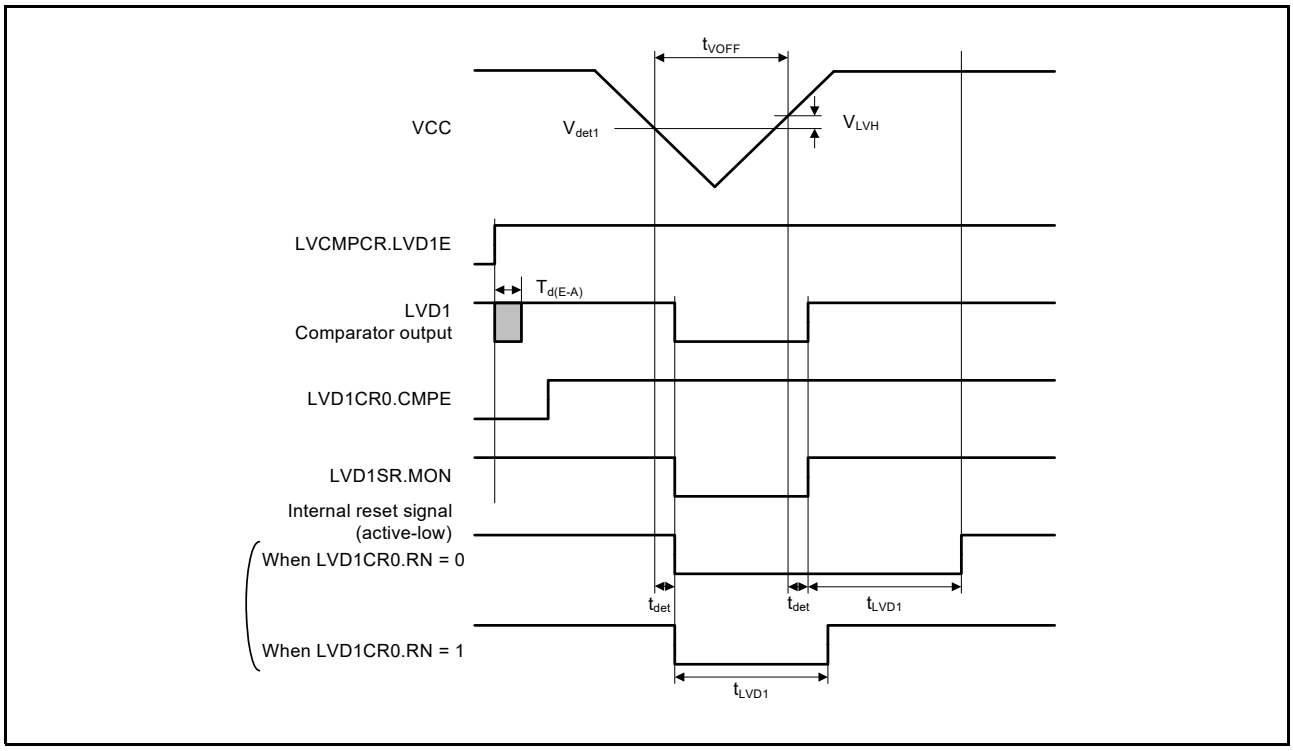


Figure 46.68 Voltage detection circuit timing (V_{det1})

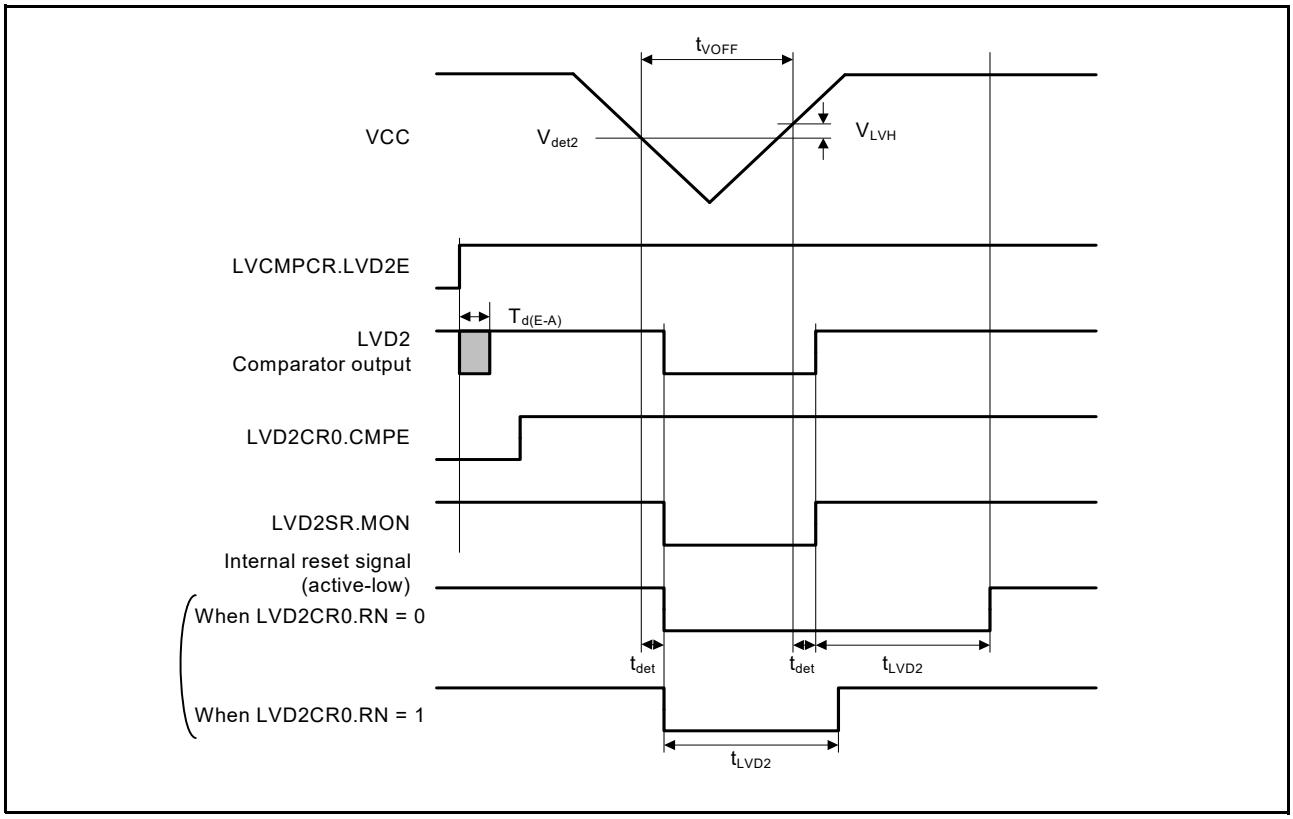


Figure 46.69 Voltage detection circuit timing (V_{det2})

46.10 CTSU Characteristics

Table 46.56 CTSU characteristics

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
External capacitance connected to TSCAP pin	C_{tscap}	9	10	11	nF	-
TS pin capacitive load	C_{base}	-	-	50	pF	-
Permissible output high current	ΣIoH	-	-	-24	mA	When the mutual capacitance method is applied

46.11 Comparator Characteristics

Table 46.57 ACMPHS characteristics
Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input offset voltage	V_{IOCMP}	-	±5	±40	mV	-
Input voltage range	V_{ICPM}	0	-	AVCC0	V	-
Output delay time	T_d	-	50	100	ns	Input amplitude ±100 mV
Stabilization wait time during input channel switching*1	T_{WAIT}	300	-	-	ns	Input amplitude ±100 mV
Operation stabilization wait time*2	T_{cmp}	1	-	-	μs	3.3 V ≤ AVCC0 ≤ 5.5 V
		3	-	-	μs	2.7 V ≤ AVCC0 < 3.3 V

Note 1. Period from when the comparator input channel is switched until the switched result reflects in its output.
Note 2. Period from when comparator operation is enabled (CPMCTL.HCMPON = 1) until the comparator satisfies the DC/AC characteristics.

Table 46.58 ACMPLP characteristics
Conditions: VCC = AVCC0 = 1.8 to 5.5 V, VSS = AVSS0 = 0 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input voltage range	IVREF0	V_{REF}	0	-	VCC - 1.4*1	V	-
	IVREF1 (Standard mode)		0	-	VCC - 1.4	V	
	IVREF1 (Window mode)		1.4*1	-	VCC	V	
	IVCMP0, IVCMP1	V_I	0	-	VCC	V	
Internal reference voltage		-	1.36	1.44	1.50	V	-
Output delay	Comparator high-speed mode (Standard mode)	T_d	-	-	1.2	μs	VCC = 3.0 Slew rate of input signal > 50 mV/μs
	Comparator high-speed mode (Window mode)				2.0	μs	
	Comparator low-speed mode (Standard mode)				5.0	μs	
Offset voltage	Comparator high-speed mode (Standard mode)	-	-	-	50	mV	-
	Comparator high-speed mode (Window mode)				60	mV	
	Comparator low-speed mode (Standard mode)				40	mV	
Operation stabilization wait time		T_{cmp}	100	-	-	μs	-

Note 1. In window mode, be sure to satisfy the following condition: IVREF1 - IVREF0 ≥ 0.2 V.

46.12 OPAMP Characteristics

Table 46.59 OPAMP characteristics (1 of 2)
Conditions: 1.8 V ≤ AVCC0 = VCC ≤ 5.5 V, VSS = AVSS0 = 0 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Common mode input range	V_{icm1}	Low-power mode	0.1	-	AVCC0 - 0.5	V
	V_{icm2}	High-speed mode	0.2	-	AVCC0 - 0.6	
Output voltage range	V_{o1}	Low-power mode	0.1	-	AVCC0 - 0.1	V
	V_{o2}	High-speed mode	0.1	-	AVCC0 - 0.1	
Input offset voltage	V_{ioff1}	Low-power mode	-7	-	7	mV
	V_{ioff2}	High-speed mode	-5	-	5	

Table 46.59 OPAMP characteristics (2 of 2)
Conditions: 1.8 V ≤ AVCC0 = VCC ≤ 5.5 V, VSS = AVSS0 = 0 V

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Open gain	A_V	-		80	120	-	dB
Gain-bandwidth (GB) product	GBW1	Low-power mode		-	0.012	-	MHz
	GBW2	High-speed mode		-	1.7	-	
Phase margin	PM	CL = 20 pF		50	-	-	deg
Gain margin	GM	CL = 20 pF		10	-	-	dB
Equivalent input noise	V_{noise1}	f = 10 Hz	Low-power mode	-	700	-	nV/√Hz
	V_{noise2}	f = 1 kHz		-	400	-	
	V_{noise3}	f = 1 kHz	High-speed mode	-	90	-	
	V_{noise4}	f = 100 kHz		-	50	-	
Power supply reduction ratio	PSRR	-		-	90	-	dB
Common mode signal reduction ratio	CMRR	-		-	90	-	dB
Stabilization wait time	T_{std1}	CL = 20 pF Only operational amplifier is activated.*1	Low-power mode VCC < 3.6V	1800	-	-	μs
			Low-power mode VCC < 5.5V	2500	-	-	
	T_{std2}		High-speed mode	13	-	-	
	T_{std3}	CL = 20 pF Operational amplifier and reference current circuit are activated simultaneously.	Low-power mode VCC < 3.6V	1800	-	-	
			Low-power mode VCC < 5.5V	2500	-	-	
	T_{std4}		High-speed mode	13	-	-	
Settling time	T_{set1}	CL = 20 pF	Low-power mode VCC < 3.6V	-	-	1400	μs
			Low-power mode VCC < 5.5V	-	-	2000	μs
	T_{set2}		High-speed mode	-	-	13	μs
Slew rate	T_{slew1}	CL = 20 pF	Low-power mode	-	0.005	-	V/μs
	T_{slew2}		High-speed mode	-	1.1	-	V/μs
Load current	I_{load1}	Low-power mode		-100	-	100	μA
	I_{load2}	High-speed mode		-100	-	100	
Load capacitance	CL	-		-	-	20	pF

Note 1. When the operational amplifier and the reference current circuit have already been activated.

46.13 Flash Memory Characteristics

46.13.1 Code Flash Memory Characteristics

Table 46.60 Code flash characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Conditions
Reprogramming/erasure cycle*1		N_{PEC}	1000	-	-	Times	-
Data hold time	After 1000 times N_{PEC}	t_{DRP}	20*2, *3	-	-	Year	T_a = +85°C

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 1,000), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 256 times for different addresses in 1-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled. (overwriting is prohibited.)

Note 2. Characteristic when using the flash memory programmer and the self-programming library provided by Renesas Electronics.

Note 3. This result is obtained from reliability testing.

Table 46.61 Code flash characteristics (2)

High-speed operating mode

Conditions: VCC = AVCC0 = 2.7 to 5.5 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 32 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	4 bytes	t_{P4}	-	116	998	-	54	506	μs
Erasure time	1 KB	t_{E1K}	-	9.03	287	-	5.67	222	ms
Blank check time	4 bytes	t_{BC4}	-	-	56.8	-	-	16.6	μs
	1 KB	t_{BC1K}	-	-	1899	-	-	140	μs
Erase suspended time		t_{SED}	-	-	22.5	-	-	10.7	μs
Startup area switching setting time		t_{SAS}	-	21.9	585	-	12.1	447	ms
Access window time		t_{AWS}	-	21.9	585	-	12.1	447	ms
OCD/serial programmer ID setting time		t_{OSIS}	-	21.9	585	-	12.1	447	ms
Flash memory mode transition wait time 1		t_{DIS}	2	-	-	2	-	-	μs
Flash memory mode transition wait time 2		t_{MS}	5	-	-	5	-	-	μs

Note 1. Does not include the time until each operation of the flash memory is started after instructions are executed by the software.

Note 2. The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 3. The frequency accuracy of ICLK must be ±3.5% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Table 46.62 Code flash characteristics (3)
Middle-speed operating mode
Conditions: VCC = AVCC0 = 1.8 to 5.5 V, Ta = -40 to +85°C

Parameter		Symbol	ICLK = 1 MHz			ICLK = 8 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	4 bytes	t_{P4}	-	157	1411	-	101	966	μs
Erasure time	1 KB	t_{E1K}	-	9.10	289	-	6.10	228	ms
Blank check time	2 bytes	t_{BC4}	-	-	87.7	-	-	52.5	μs
	1 KB	t_{BC1K}	-	-	1930	-	-	414	μs
Erase suspended time		t_{SED}	-	-	32.7	-	-	21.6	μs
Startup area switching setting time		t_{SAS}	-	22.8	592	-	14.2	465	ms
Access window time		t_{AWS}	-	22.8	592	-	14.2	465	ms
OCD/serial programmer ID setting time		t_{OSIS}	-	22.8	592	-	14.2	465	ms
Flash memory mode transition wait time 1		t_{DIS}	2	-	-	2	-	-	μs
Flash memory mode transition wait time 2		t_{MS}	720	-	-	720	-	-	ns

Note 1. Does not include the time until each operation of the flash memory is started after instructions are executed by the software.
Note 2. The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 3. The frequency accuracy of ICLK must be ±3.5% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

46.13.2 Data Flash Memory Characteristics

Table 46.63 Data flash characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Conditions
Reprogramming/erasure cycle*1		N_{DPEC}	100000	1000000	-	Times	-
Data hold time	After 10000 times of N_{DPEC}	t_{DDRP}	20*2, *3	-	-	Year	Ta = +85°C
	After 100000 times of N_{DPEC}		5*2, *3	-	-	Year	
	After 1000000 times of N_{DPEC}		-	1*2, *3	-	Year	Ta = +25°C

Note 1. The reprogram/erase cycle is the number of erasure for each block. When the reprogram/erase cycle is n times (n = 100,000), erasing can be performed n times for each block. For instance, when 1-byte programming is performed 1,000 times for different addresses in 1-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled. (overwriting is prohibited.)
Note 2. Characteristics when using the flash memory programmer and the self-programming library provided by Renesas Electronics.
Note 3. These results are obtained from reliability testing.

Table 46.64 Data flash characteristics (2)
High-speed operating mode
Conditions: VCC = AVCC0 = 2.7 to 5.5 V

Parameter		Symbol	ICLK = 4 MHz			ICLK = 32 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	1-byte	t_{DP1}	-	52.4	463	-	42.1	387	μs
Erasure time	1-KB	t_{DE1K}	-	8.98	286	-	6.42	237	ms
Blank check time	1-byte	t_{DBC1}	-	-	24.3	-	-	16.6	μs
	1-KB	t_{DBC1K}	-	-	1872	-	-	512	μs
Suspended time during erasing		t_{DSED}	-	-	13.0	-	-	10.7	μs
Data flash STOP recovery time		t_{DSTOP}	5	-	-	5	-	-	μs

Note 1. Does not include the time until each operation of the flash memory is started after instructions are executed by the software.
Note 2. The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 3. The frequency accuracy of ICLK must be ±3.5% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Table 46.65 Data flash characteristics (3)
Middle-speed operating mode
Conditions: VCC = AVCC0 = 1.8 to 5.5 V, Ta = -40 to +85°C

Parameter		Symbol	ICLK = 4 MHz			ICLK = 8 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	1-byte	t_{DP1}	-	94.7	886	-	89.3	849	μs
Erasure time	1-KB	t_{DE1K}	-	9.59	299	-	8.29	273	ms
Blank check time	1-byte	t_{DBC1}	-	-	56.2	-	-	52.5	μs
	1-KB	t_{DBC1K}	-	-	2.17	-	-	1.51	ms
Suspended time during erasing		t_{DSED}	-	-	23.0	-	-	21.7	μs
Data flash STOP recovery time		t_{DSTOP}	720	-	-	720	-	-	ns

Note 1. Does not include the time until each operation of the flash memory is started after instructions are executed by the software.
Note 2. The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 3. The frequency accuracy of ICLK must be ±3.5% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

46.13.3 Serial Wire Debug (SWD)

Table 46.66 SWD characteristics (1) (1 of 2)
Conditions: VCC = AVCC0 = 2.4 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	80	-	-	ns	Figure 46.70
SWCLK clock high pulse width	t_{SWCKH}	35	-	-	ns	
SWCLK clock low pulse width	t_{SWCKL}	35	-	-	ns	
SWCLK clock rise time	t_{SWCKr}	-	-	5	ns	
SWCLK clock fall time	t_{SWCKf}	-	-	5	ns	

Table 46.66 SWD characteristics (1) (2 of 2)
Conditions: VCC = AVCC0 = 2.4 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWDIO setup time	t_{SWDS}	16	-	-	ns	Figure 46.71
SWDIO hold time	t_{SWDH}	16	-	-	ns	
SWDIO data delay time	t_{SWDD}	2	-	70	ns	

Table 46.67 SWD characteristics (2)
Conditions: VCC = AVCC0 = 1.6 to 2.4 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	250	-	-	ns	Figure 46.70
SWCLK clock high pulse width	t_{SWCKH}	120	-	-	ns	
SWCLK clock low pulse width	t_{SWCKL}	120	-	-	ns	
SWCLK clock rise time	t_{SWCKr}	-	-	5	ns	
SWCLK clock fall time	t_{SWCKf}	-	-	5	ns	
SWDIO setup time	t_{SWDS}	50	-	-	ns	Figure 46.71
SWDIO hold time	t_{SWDH}	50	-	-	ns	
SWDIO data delay time	t_{SWDD}	2	-	150	ns	

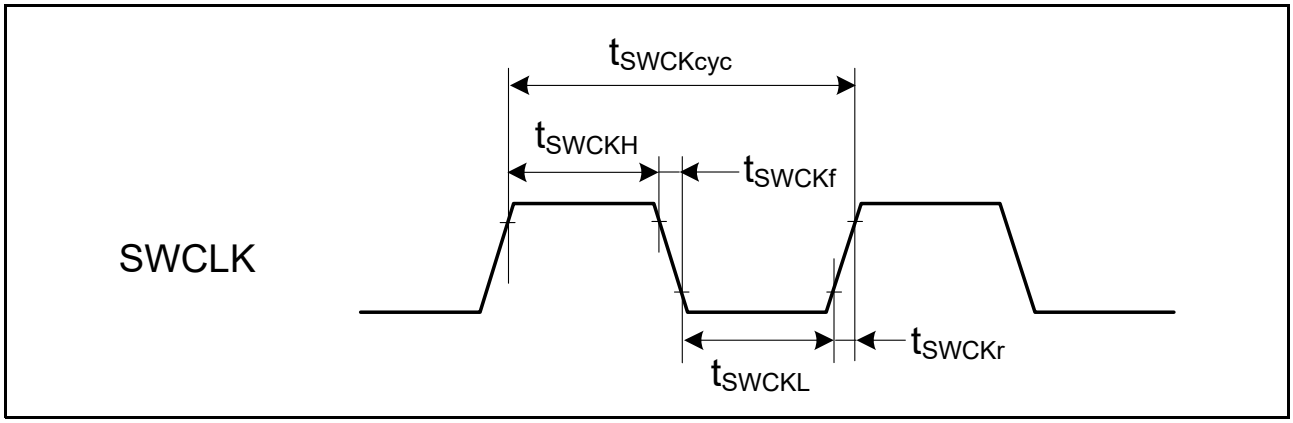


Figure 46.70 SWD SWCLK timing

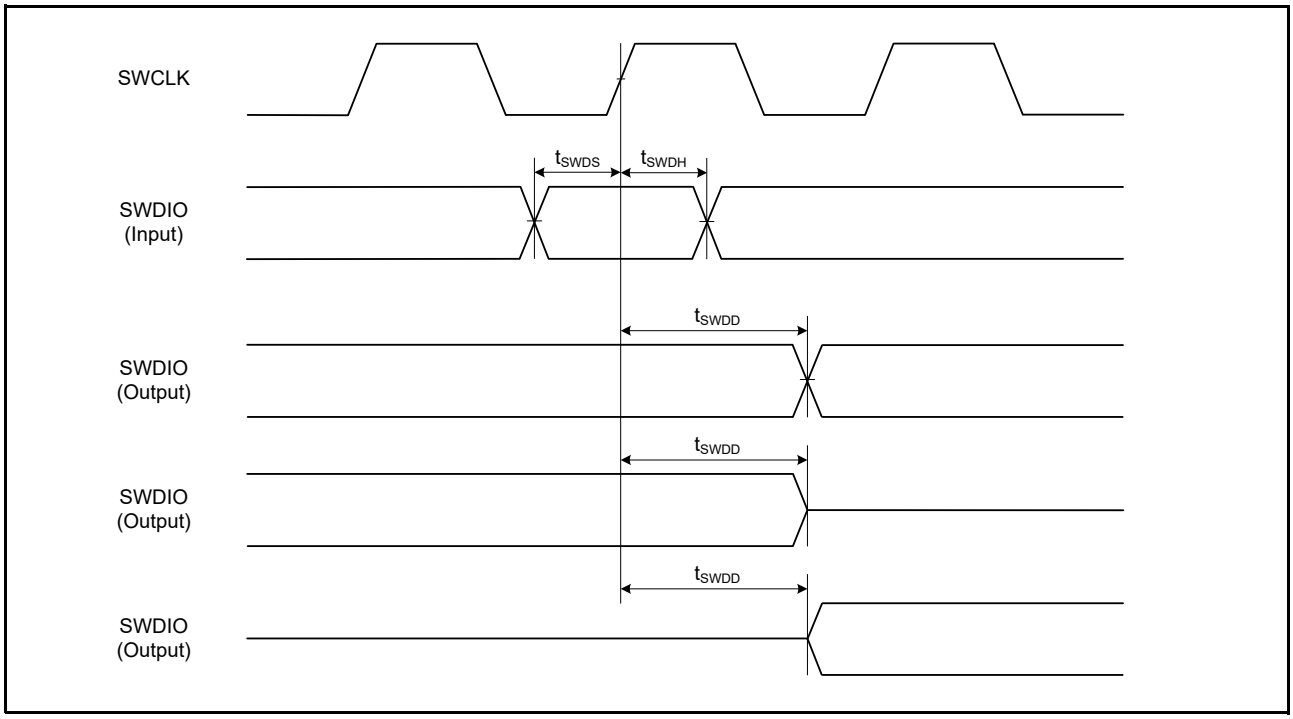


Figure 46.71 SWD input/output timing

Appendix 1. Port States in Each Processing Mode

Table 1.1 Port states in each processing state (1 of 2)

Port Name	Reset	Software Standby Mode
P000/IRQ6, P001/IRQ7, P002/IRQ2	Hi-Z	Keep-O*1
P003	Hi-Z	Keep-O
P004/DA2_B/IRQ3	Hi-Z	[DA2 output (DACE2=1)] DA output retained [Other than the above (DACE2=0)] Keep-O*1
P010	Hi-Z	Keep-O
P011/DA2_A	Hi-Z	[DA2 output (DACE2=1)] DA output retained [Other than the above (DACE2=0)] Keep-O
P012, P013	Hi-Z	Keep-O
P014/DA0	Hi-Z	[DA0 output (DACE0=1)] DA output retained [Other than the above (DACE0=0)] Keep-O
P015/DA1_A/IRQ7	Hi-Z	[DA1 output (DACE1=1)] DA output retained [Other than the above (DACE1=0)] Keep-O*1
P100/KR00/IRQ2/CMPIN0/ AGTIO0_A/RXD0_A/DRX0	Hi-Z	[AGTIO0_A output selected] AGTIO0_A output [Other than the above] Keep-O*1
P101/KR01/IRQ1/CMPREF0	Hi-Z	Keep-O*1
P102/KR02/AGTO0	Hi-Z	[AGTO0 selected] AGTO0 output [Other than the above] Keep-O*1
P103/KR03, P104/KR04/IRQ1/RXD0_C, P105/KR05/IRQ0, P106/KR06, P107/KR07	Hi-Z	Keep-O*1
P108/SWDIO	Pull-up	Keep-O
P109/CLKOUT_B	Hi-Z	[CLKOUT selected] CLKOUT output [Other than the above] Keep-O
P110/IRQ3/VCOUT	Hi-Z	[ACMPLP selected] VCOUT output [Other than the above] Keep-O*1
P111/IRQ4/AGTOA0	Hi-Z	[AGTOA0 selected] AGTOA0 output [Other than the above] Keep-O*1
P112/AGTOB0	Hi-Z	[AGTOB0 selected] AGTOB0 output [Other than the above] Keep-O
P113	Hi-Z	Keep-O
P200/NMI	Hi-Z	Hi-Z
P201	Pull-up	Keep-O
P204/AGTIO1_A/SCL0_B	Hi-Z	[AGTIO1_A output selected] AGTIO1_A output [Other than the above] Keep-O*1

Table 1.1 Port states in each processing state (2 of 2)

Port Name	Reset	Software Standby Mode
P205/IRQ1/CLKOUT_A/AGTO1	Hi-Z	[AGTO1 selected] AGTO1 output [CLKOUT selected] CLKOUT output [Other than the above] Keep-O*1
P206/IRQ0/RXD0_D, P212/IRQ3/EXTAL, P213/IRQ2/XTAL	Hi-Z	Keep-O*1
P214/XCOUT, P215/XCIN	Hi-Z	[Sub-clock Oscillator selected] Sub-clock Oscillator is operating [Other than the above] Hi-Z
P300/SWCLK	Pull-up	Keep-O
P301/IRQ6/AGTIO0_D	Hi-Z	[AGTIO0_D output selected] AGTIO0_D output [Other than the above] Keep-O*1
P302/IRQ5	Hi-Z	Keep-O*1
P303, P304	Hi-Z	Keep-O
P400/AGTIO1_D/SCL0_A/IRQ0	Hi-Z	[AGTIO1_D output selected] AGTIO1_D output [Other than the above] Keep-O*1
P401/SDA0_A/IRQ5, P402/IRQ4	Hi-Z	Keep-O*1
P403	Hi-Z	Keep-O
P407/SDA0_B/RTCOUT/ USB_VBUS/AGTIO0_C	Hi-Z	[AGTIO0_C output selected] AGTIO0_C output [RTCOUT selected] RTCOUT output [Other than the above] Keep-O*1
P408/SCL0_C/IRQ7, P409/IRQ6	Hi-Z	Keep-O*1
P410/IRQ5/AGTOB1/RXD0_B	Hi-Z	[AGTOB1 selected] AGTOB1 output [Other than the above] Keep-O*1
P411/IRQ4/AGTOA1	Hi-Z	[AGTOA1 selected] AGTOA1 output [Other than the above] Keep-O*1
P500/DA1_B	Hi-Z	[DA1 output (DACE1=1)] DA output retained [Other than the above (DACE1=0)] Keep-O
P501, P502	Hi-Z	Keep-O
P914/USB_DP	Hi-Z	Keep-O
P915/USB_DM	Hi-Z	Keep-O

Hi-Z: High-impedance

Keep-O: Output pins retain their previous values. Input pins become high-impedance.

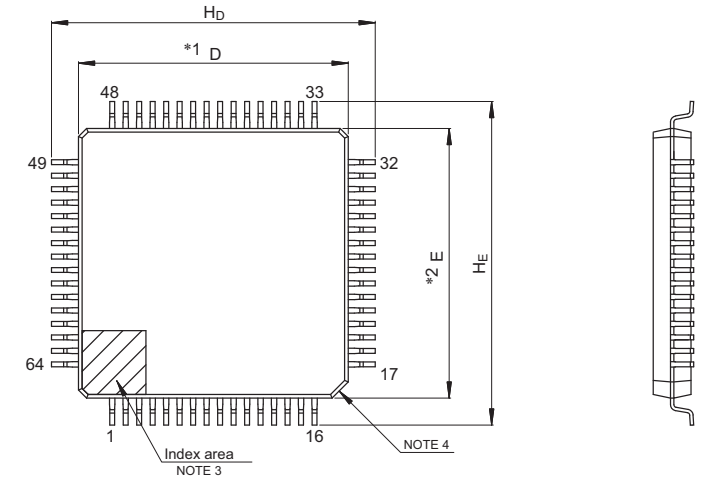
Note 1. Input is enabled if the pin is specified as the software standby canceling source while it is used as an external interrupt pin.

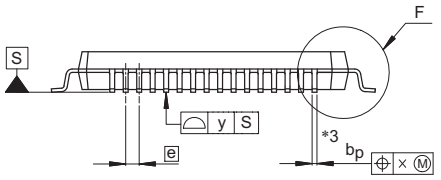
Appendix 2.Package Dimensions

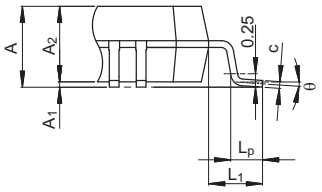
Information on the latest version of the package dimensions or mountings is displayed in "Packages" on the Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	—	0.3

Unit: mm







Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

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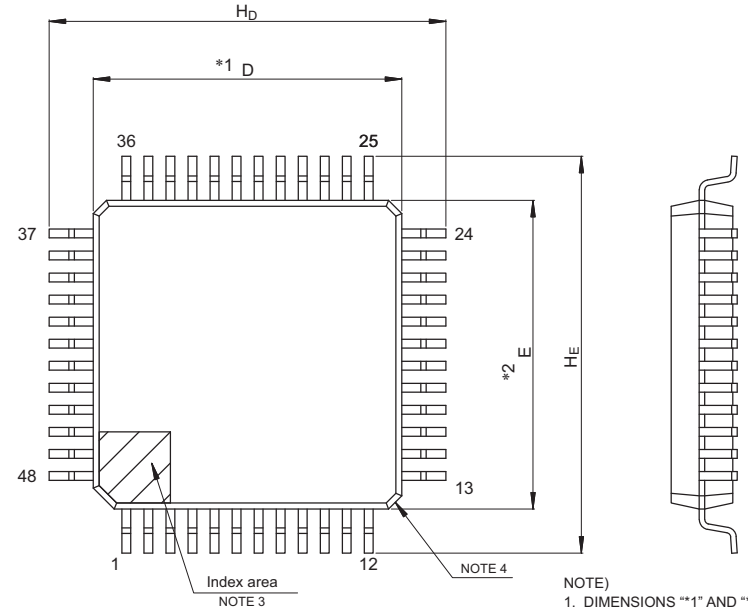
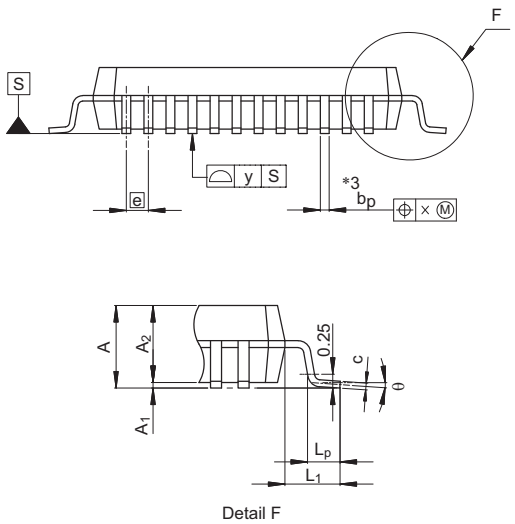
Figure 2.1 LQFP 64-pin

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP48-7x7-0.50	PLQP0048KB-B	—	0.2

Unit: mm



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.



Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

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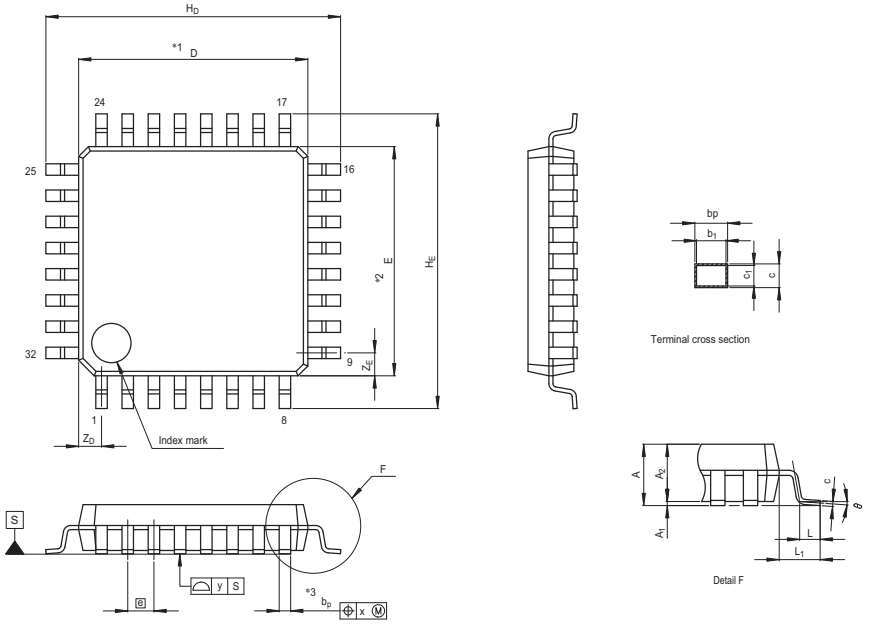
Figure 2.2 LQFP 48-pin

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP32-7x7-0.80	PLQP0032GB-A	32P6U-A	0.2g

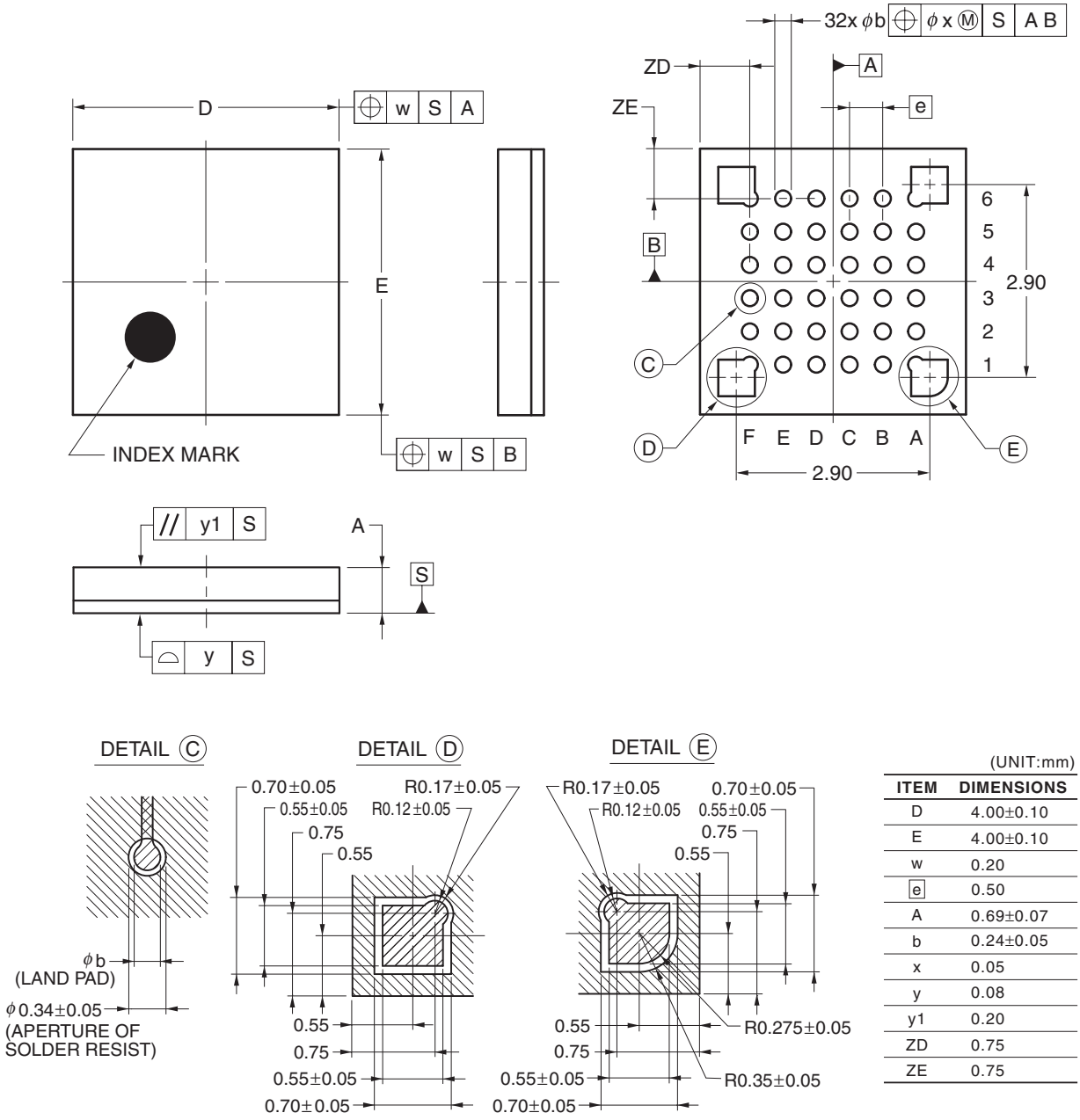


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	0.7	—
Z_E	—	0.7	—
L	0.3	0.5	0.7
L_1	—	1.0	—

Figure 2.3 LQFP 32-pin

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-WFLGA36-4x4-0.50	PWLG0036KA-A	P36FC-50-AA4-2	0.023



(UNIT:mm)

ITEM	DIMENSIONS
D	4.00±0.10
E	4.00±0.10
w	0.20
e	0.50
A	0.69±0.07
b	0.24±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.75
ZE	0.75

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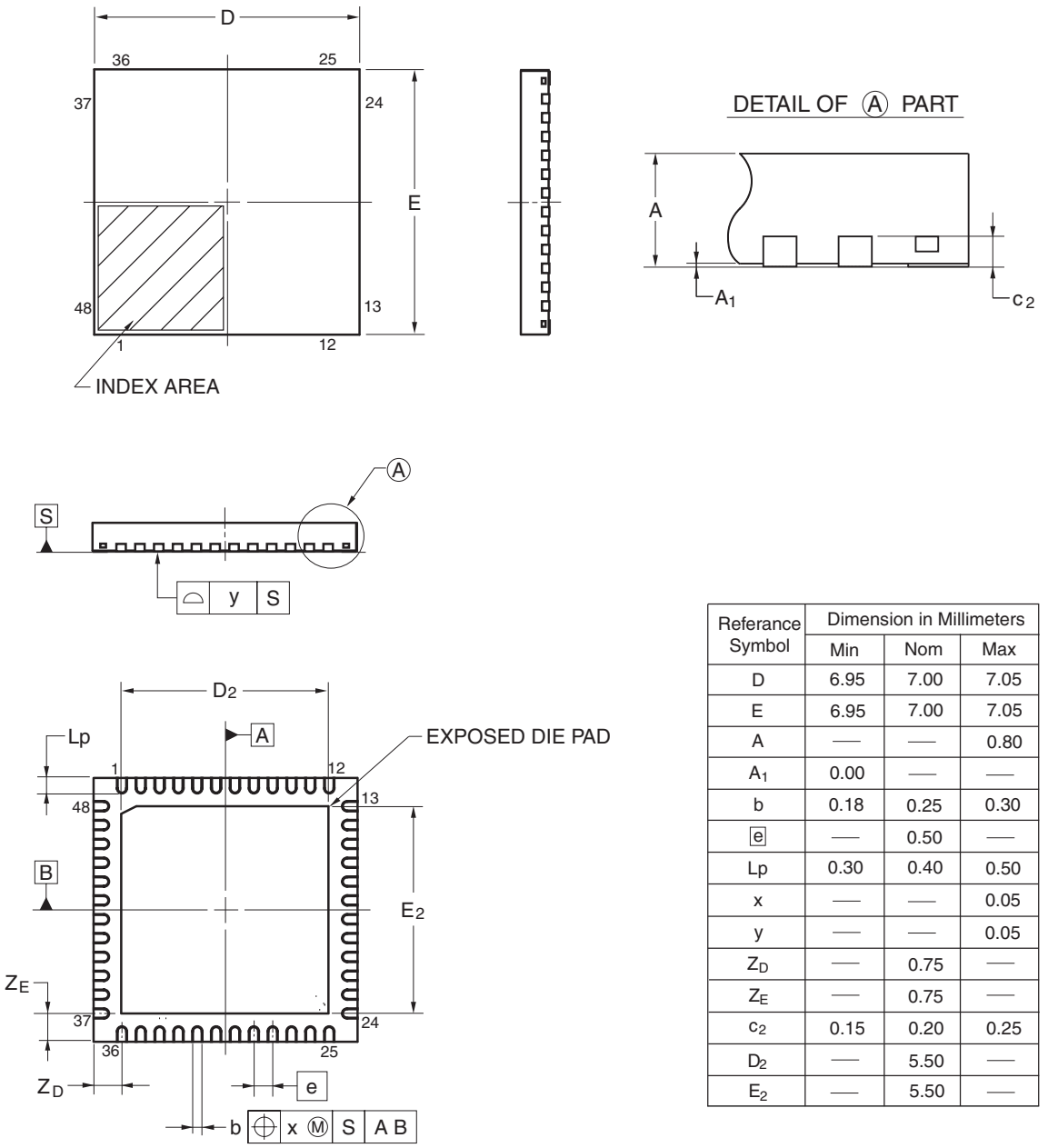
Figure 2.4 LGA 36-pin

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN48-7x7-0.50	PWQN0048KB-A	48PJN-A P48K8-50-5B4-6	0.13



Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.95	7.00	7.05
E	6.95	7.00	7.05
A	—	—	0.80
A_1	0.00	—	—
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	0.75	—
Z_E	—	0.75	—
c_2	0.15	0.20	0.25
D_2	—	5.50	—
E_2	—	5.50	—

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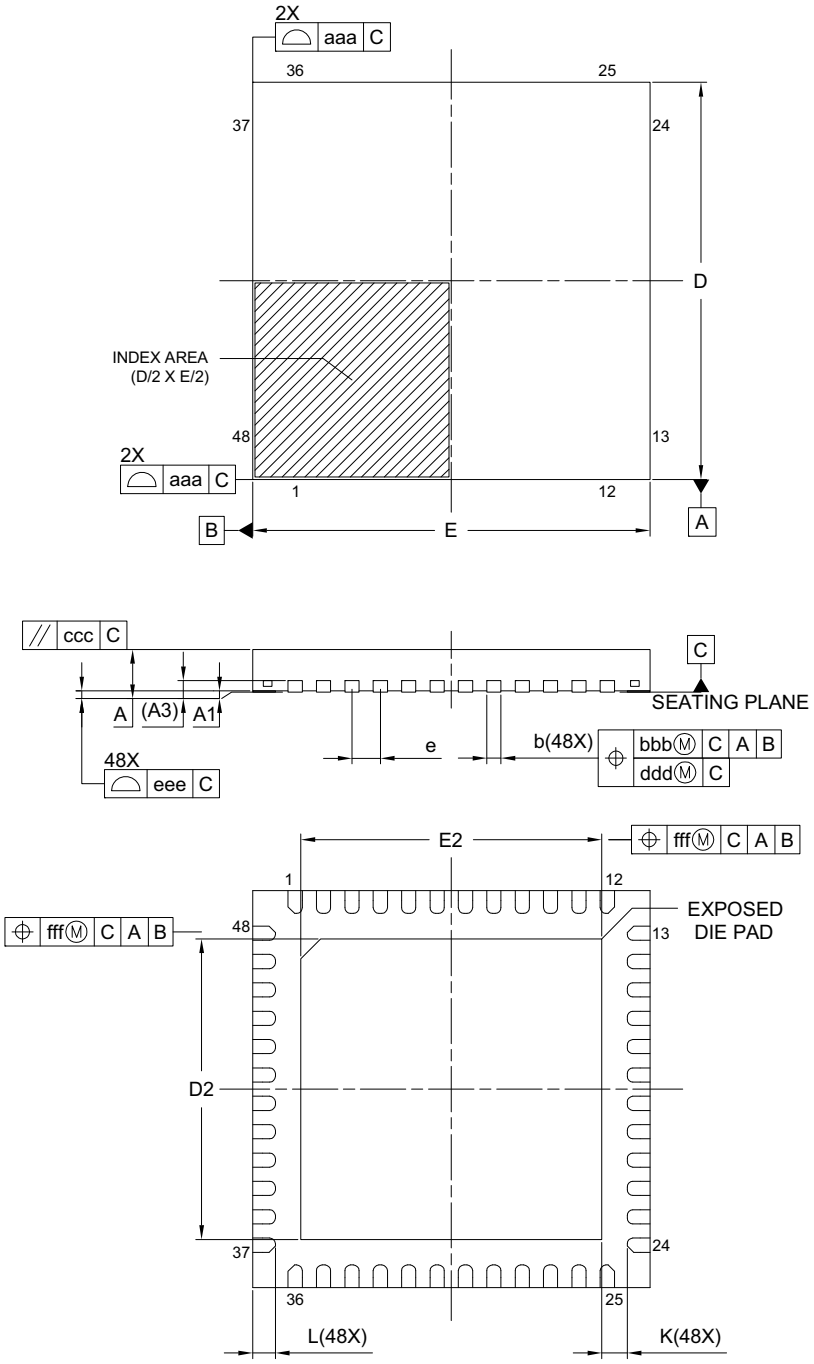
Figure 2.5 QFN 48-pin (1)

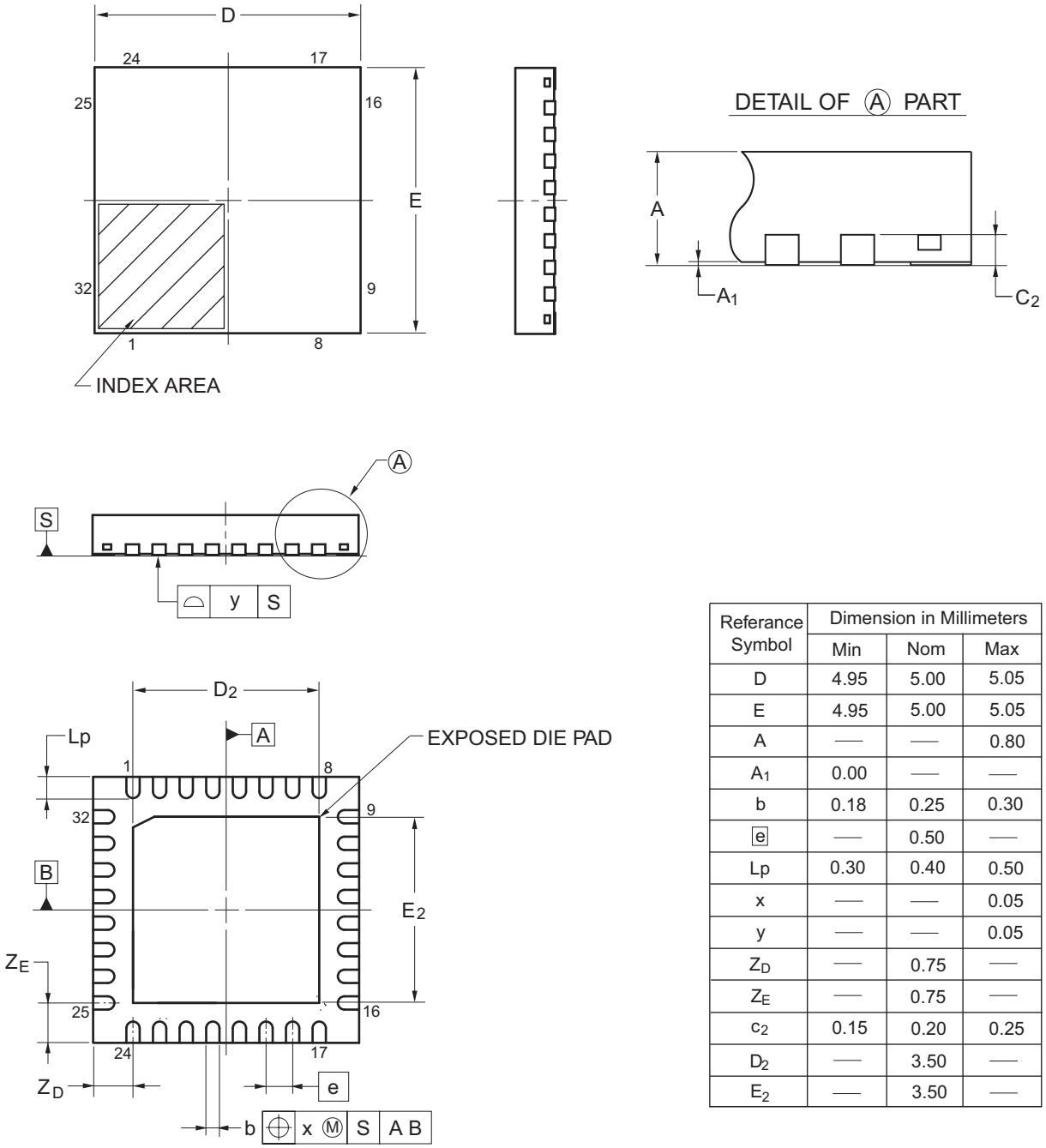
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN048-7x7-0.50	PWQN0048KC-A	0.13 g



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3	0.203 REF.		
b	0.20	0.25	0.30
D	7.00 BSC		
E	7.00 BSC		
e	0.50 BSC		
L	0.30	0.40	0.50
K	0.20	—	—
D_2	5.25	5.30	5.35
E_2	5.25	5.30	5.35
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Figure 2.6 QFN 48-pin (2)

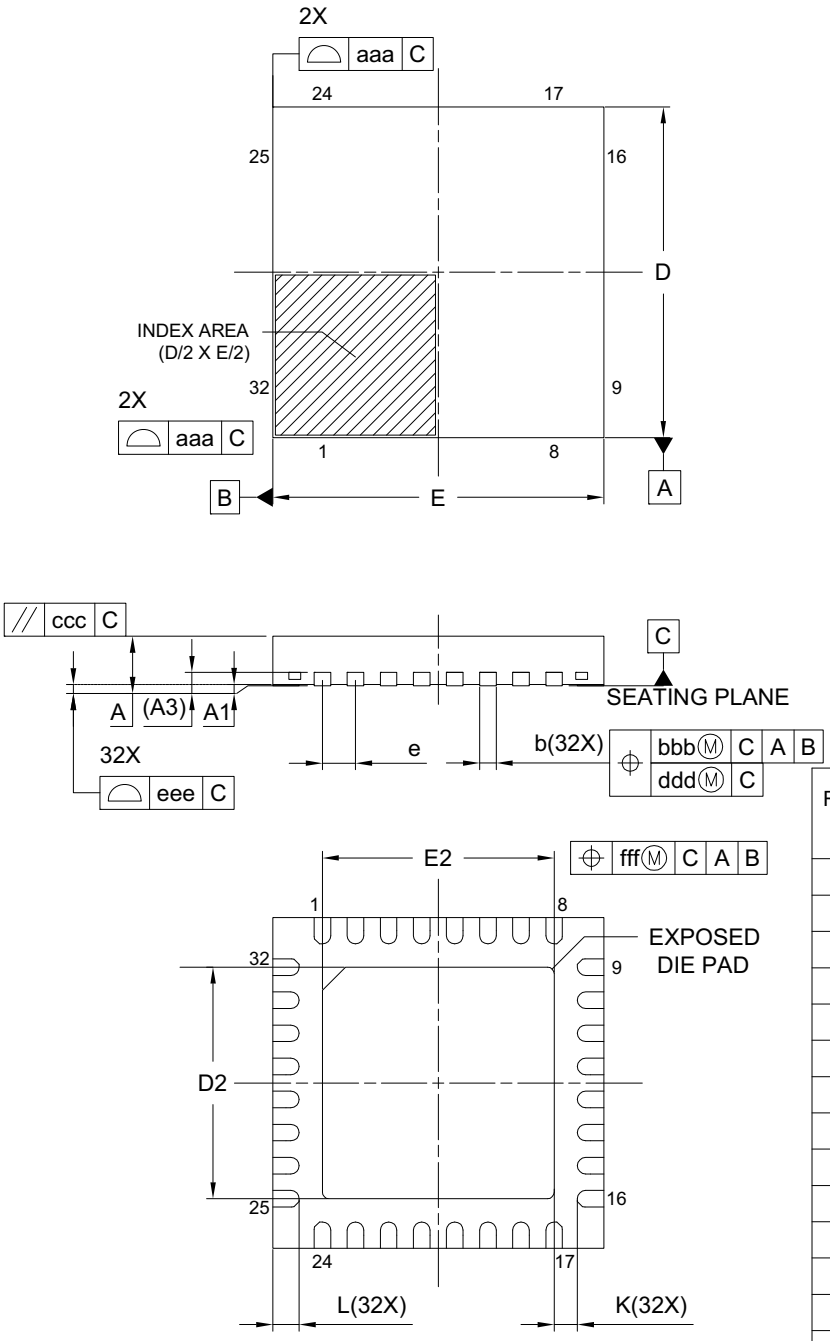
JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN32-5x5-0.50	PWQN0032KB-A	P32K8-50-3B4-5	0.06



Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.95	5.00	5.05
E	4.95	5.00	5.05
A	—	—	0.80
A_1	0.00	—	—
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	0.75	—
Z_E	—	0.75	—
c_2	0.15	0.20	0.25
D_2	—	3.50	—
E_2	—	3.50	—

Figure 2.7 QFN 32-pin (1)

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN032-5x5-0.50	PWQN0032KF-A	0.06



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3	0.203 REF.		
b	0.18	0.25	0.30
D	5.00 BSC		
E	5.00 BSC		
e	0.50 BSC		
L	0.35	0.40	0.45
K	0.20	—	—
D_2	3.45	3.50	3.55
E_2	3.45	3.50	3.55
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Figure 2.8 QFN 32-pin (2)

Appendix 3. I/O Registers

This appendix describes I/O register addresses, access cycles, and reset values by function.

3.1 Peripheral Base Addresses

This section provides the base addresses for peripherals described in this manual.

Table 3.1 shows the name of each peripheral, description, and its base address.

Table 3.1 Peripheral base address (1 of 2)

Name	Description	Base address
MMPU	Bus Master MPU	0x40000000
SMPU	Bus Slave MPU	0x40000C00
SPMON	CPU Stack Pointer Monitor	0x40000D00
SRAM	SRAM Control	0x40002000
BUS	BUS Control	0x40003000
DTC	Data Transfer Controller	0x40005400
ICU	Interrupt Controller	0x40006000
DBG	Debug Function	0x4001B000
SYSTEM	System Control	0x4001E000
PORT0	Port 0 Control Registers	0x40040000
PORT1	Port 1 Control Registers	0x40040020
PORT2	Port 2 Control Registers	0x40040040
PORT3	Port 3 Control Registers	0x40040060
PORT4	Port 4 Control Registers	0x40040080
PORT5	Port 5 Control Registers	0x400400A0
PORT9	Port 9 Control Registers	0x40040120
PFS	Pmn Pin Function Control Register	0x40040800
PMISC	Miscellaneous Port Control Register	0x40040D00
ELC	Event Link Controller	0x40041000
POEG	Port Output Enable Module for GPT	0x40042000
RTC	Realtime Clock	0x40044000
WDT	Watchdog Timer	0x40044200
IWDT	Independent Watchdog Timer	0x40044400
CAC	Clock Frequency Accuracy Measurement Circuit	0x40044600
MSTP	Module Stop Control B,C,D	0x40047000
CAN0	CAN0 Module	0x40050000
IIC0	Inter-Integrated Circuit 0	0x40053000
IIC1	Inter-Integrated Circuit 1	0x40053100
DOC	Data Operation Circuit	0x40054100
ADC140	14-bit A/D Converter	0x4005C000
SCI0	Serial Communication Interface 0	0x40070000
SCI1	Serial Communication Interface 1	0x40070020
SCI9	Serial Communication Interface 9	0x40070120
SPI0	Serial Peripheral Interface 0	0x40072000
SPI1	Serial Peripheral Interface 1	0x40072100
CRC	CRC Calculator	0x40074000
GPT320	General PWM Timer 0 (32-bit)	0x40078000
GPT161	General PWM Timer 1 (16-bit)	0x40078100

Table 3.1 Peripheral base address (2 of 2)

Name	Description	Base address
GPT162	General PWM Timer 2 (16-bit)	0x40078200
GPT163	General PWM Timer 3 (16-bit)	0x40078300
GPT164	General PWM Timer 4 (16-bit)	0x40078400
GPT165	General PWM Timer 5 (16-bit)	0x40078500
GPT166	General PWM Timer 6 (16-bit)	0x40078600
GPT_OPS	Output Phase Switching Controller	0x40078FF0
GPT_ODC	PWM Delay Generation Circuit	0x4007B000
KINT	Key Interrupt Function	0x40080000
CTSU	Capacitive Touch Sensing Unit	0x40081000
AGT0	Low Power Asynchronous General purpose Timer 0	0x40084000
AGT1	Low Power Asynchronous General purpose Timer 1	0x40084100
ACMPHS0	High-Speed Analog Comparator 0	0x40085000
ACMPHS1	High-Speed Analog Comparator 1	0x40085100
ACMPHS2	High-Speed Analog Comparator 2	0x40085200
ACMPLP	Low-Power Analog Comparator	0x40085E00
OPAMP	Operational Amplifier	0x40086000
DALI	Digital Addressable Lighting Interface	0x4008F000
USBFS	USB 2.0 Full-Speed Module	0x40090000
DAC8	8-bit D/A converter	0x4009E000
TSN	Temperature Sensor	0x407EC000

Name = Peripheral name
Description = Peripheral functionality
Base address = Lowest reserved address or address used by the peripheral

3.2 Access Cycles

This section provides access cycle information for the I/O registers described in this manual.

The following information applies to Table 3.2 and Table 3.3:

- Registers are grouped by associated module
- The number of access cycles indicates the number of cycles based on the specified reference clock
- In the internal I/O register area, reserved addresses that are not allocated to registers must not be accessed, otherwise operations cannot be guaranteed
- The number of I/O register access cycles depends on bus cycles of the internal peripheral bus and divided clock synchronization cycles. Divided clock synchronization cycles differ depending on the frequency ratio between ICLK and PCLK.
- When the frequency of ICLK is equal to that of PCLK, the number of divided clock synchronization cycles is always constant.
- When the frequency of ICLK is greater than that of PCLK, at least 1 PCLK cycle is added to the number of divided clock synchronization cycles.

Note: This applies to the number of cycles when access from the CPU does not conflict with the instruction fetching to the external memory or bus access from other bus master such as DTC.

Table 3.2 shows register access cycles for non-GPT modules.

Table 3.2 Access cycles for non-GPT modules

Peripheral	Address		Number of access cycles					
			ICLK = PCLK		ICLK > PCLK*1		Cycle unit	Related function
	From	To	Read	Write	Read	Write		
MMPU, SMPU, SPMON, SRAM, BUS, DTC, ICU, DBG	4000 0000h	4001 BFFFh	2				ICLK	Memory Protection Unit, SRAM, Buses, Data Transfer Controller, Interrupt Controller, CPU
SYSTEM	4001 E000h	4001 E3FFh	3				ICLK	Low Power Modes, Resets, Low Voltage Detection, Clock Generation Circuit, Register Write Protection
SYSTEM	4001 E400h	4001 E6FFh	7		5 to 7		PCLKB	Low Power Mode, Resets, Low Voltage Detect
PORTn, PFS, PMISC, ELC, POEG, RTC, WDT, IWDT, CAC, MSTP	4004 0000h	4004 7FFFh	3		2 to 3		PCLKB	I/O Ports, Event Link Controller, Port Output Enable for GPT, Realtime Clock, Watchdog Timer, Independent Watchdog Timer, Clock Frequency Accuracy Measurement Circuit, Module Stop Control
CAN0, IICn, DOC, ADC140	4005 0000h	4005 EFFFh	3		2 to 3		PCLKB	Controller Area Network, I²C Bus Interface, Data Operation Circuit, 14-Bit A/D Converter
SCIn	4007 0000h	4007 0EFFh	5*2		2 to 3*2		PCLKB	Serial Communications Interface
SPIn	4007 2000h	4007 2FFFh	5*3		2 to 3*3		PCLKB	Serial Peripheral Interface
CRC	4007 4000h	4007 4FFFh	3		2 to 3		PCLKB	CRC Calculator
GPT320, GPT16Hm, GPT16n, GPT_OPS, GPT_OCD	4007 8000h	4007 BFFFh	See Table 3.3*4				PCLKB	General PWM Timer, PWM Delay Generation Circuit
TSN	407E C000h	407E CFFFh	7		7		ICLK	Temperature Sensor
KINT, CTSU	4008 0000h	4008 1FFFh	2		1 to 2		PCLKB	Key Interrupt Function, Capacitive Touch Sensing Unit
AGTn	4008 4000h	4008 4FFFh	3		2 to 3		PCLKB	Low Power Asynchronous General Purpose Timer
ACMPHSn, ACMPLP, OPAMP	4008 5000h	4008 6FFFh	2		1 to 2		PCLKB	High-Speed Analog Comparator, Low-Power Analog Comparator, Operational Amplifier
USBFS	4009 0000h	4009 03FFh	4		3 to 4		PCLKB	USB 2.0 Full-Speed Module
USBFS	4009 0400h	4009 04FFh	3		2 to 3		PCLKB	USB 2.0 Full-Speed Module
DAC8	4009 E000h	4009 E00Fh	2		1 to 2		PCLKB	8-Bit D/A Converter

Note 1. If the number of PCLK cycles is non-integer (for example 1.5), the minimum value is without the decimal point, and the maximum value is rounded up to the decimal point. For example, 1.5 to 2.5 is 1 to 3.

Note 2. When accessing a 16-bit register (FTDRHL, FRDRHL, FCR, FDR, LSR, and CDR), access is 2 cycles more than the value shown in Table 3.2. When accessing an 8-bit register (FTDRH, FTDRL, FRDRH, and FRDRL), the access cycles are as shown in Table 3.2.

Note 3. When accessing a 32-bit register (SPDR), access is 2 cycles more than the value in Table 3.2. When accessing an 8-bit or a 16-bit register (SPDR_HA), the access cycles are as shown in Table 3.2.

Note 4. The access cycles differs depending on the frequency ratio between ICLK, PCLKB, and PCLKD, as shown in Table 3.3.

Table 3.3 shows register access cycles for GPT modules.

Table 3.3 Access cycles for GPT modules

	Number of access cycles		
Frequency ratio between ICLK and PCLK	**Read**	**Write**	**Cycle unit**
ICLK > PCLKD = PCLKB	5 to 6	3 to 4	PCLKB
ICLK > PCLKD > PCLKB	3 to 4	2 to 3	PCLKB
PCLKD = ICLK = PCLKB	6	4	PCLKB
PCLKD = ICLK > PCLKB	2 to 3	1 to 2	PCLKB
PCLKD > ICLK = PCLKB	4	3	PCLKB
PCLKD > ICLK > PCLKB	2 to 3	1 to 2	PCLKB

3.3 Register Descriptions

This section provides information associated with registers described in this manual.

Table 3.4 shows a list of the registers, including address offset and sizes, access rights, and reset values.

Table 3.4 Register description (1 of 28)

Peripheral name	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
MMPU	-	-	-	MMPUCTLA	Bus Master MPU Control Register	0x000	16	read/ write	0x0000	0xFFFF
				MMPUPTA	Group A Protection of Register	0x102	16	read/ write	0x0000	0xFFFF
	4	0x010	0-3	MMPUACA%s	Group A Region %s Access Control Register	0x200	16	read/ write	0x0000	0xFFFF
	4	0x010	0-3	MMPUSA%s	Group A Region %s Start Address Register	0x204	32	read/ write	0x0000 0000	0x0000 0003
	4	0x010	0-3	MMPUEA%s	Group A Region %s End Address Register	0x208	32	read/ write	0x0000 0003	0x0000 0003
SMPU	-	-	-	SMPUCTL	Slave MPU Control Register	0x00	16	read/ write	0x0000	0xFFFF
				SMPUMBIU	Access Control Register for MBIU	0x10	16	read/ write	0x2000	0xFFFF
				SMPUFBIU	Access Control Register for FBIU	0x14	16	read/ write	0x0000	0xFFFF
				SMPUSRAM0	Access Control Register for SRAM	0x18	16	read/ write	0x0000	0xFFFF
	3	0x4	0,2,6	SMPUP%sBIU	Access Control Register for P%sBIU	0x20	16	read/ write	0x0000	0xFFFF
SPMON	-	-	-	MSPMPUOAD	Stack Pointer Monitor Operation After Detection Register	0x00	16	read/ write	0x0000	0xFFFF
				MSPMPUCTL	Stack Pointer Monitor Access Control Register	0x04	16	read/ write	0x0000	0xFEFF
				MSPMPUPT	Stack Pointer Monitor Protection Register	0x06	16	read/ write	0x0000	0xFFFF
				MSPMPUSA	Main Stack Pointer Monitor Start Address Register	0x08	32	read/ write	0x0000 0000	0x0000 0003

Table 3.4 Register description (2 of 28)

Peripheral name	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
SPMON	-	-	-	MSPMPUEA	Main Stack Pointer Monitor End Address Register	0x0C	32	read/ write	0x0000 0003	0x0000 0003
				PSPMPUOAD	Stack Pointer Monitor Operation After Detection Register	0x10	16	read/ write	0x0000	0xFFFF
				PSPMPUCTL	Stack Pointer Monitor Access Control Register	0x14	16	read/ write	0x0000	0xFEFF
				PSPMPUPT	Stack Pointer Monitor Protection Register	0x16	16	read/ write	0x0000	0xFFFF
				PSPMPUSA	Process Stack Pointer Monitor Start Address Register	0x18	32	read/ write	0x0000 0000	0x0000 0003
				PSPMPUEA	Process Stack Pointer Monitor End Address Register	0x1C	32	read/ write	0x0000 0003	0x0000 0003
SRAM	-	-	-	PARIOAD	SRAM Parity Error Operation After Detection Register	0x00	8	read/ write	0x00	0xFF
				SRAMPRCR	SRAM Protection Register	0x04	8	read/ write	0x00	0xFF
				ECCMODE	ECC Operating Mode Control Register	0xC0	8	read/ write	0x00	0xFF
				ECC2STS	ECC 2-Bit Error Status Register	0xC1	8	read/ write	0x00	0xFF
				ECC1STSEN	ECC 1-Bit Error Information Update Enable Register	0xC2	8	read/ write	0x00	0xFF
				ECC1STS	ECC 1-Bit Error Status Register	0xC3	8	read/ write	0x00	0xFF
				ECCPRCR	ECC Protection Register	0xC4	8	read/ write	0x00	0xFF
				ECCPRCR2	ECC Protection Register 2	0xD0	8	read/ write	0x00	0xFF
				ECCETST	ECC Test Control Register	0xD4	8	read/ write	0x00	0xFF
				ECCOAD	SRAM ECC Error Operation After Detection Register	0xD8	8	read/ write	0x00	0xFF
BUS	-	-	-	BUSMCNTSYS	Master Bus Control Register SYS	0x1008	16	read/ write	0x0000	0xFFFF
				BUSMCNTDMA	Master Bus Control Register DMA	0x100C	16	read/ write	0x0000	0xFFFF
				BUSSCNTFLI	Slave Bus Control Register FLI	0x1100	16	read/ write	0x0000	0xFFFF
				BUSSCNTRAM0	Slave Bus Control Register RAM0	0x110C	16	read/ write	0x0000	0xFFFF
	2	0x4	P0B,P 2B	BUSSCNT%s	Slave Bus Control Register %s	0x1114	16	read/ write	0x0000	0xFFFF
	-	-	-	BUSSCNTP4B	Slave Bus Control Register P4B	0x1120	16	read/ write	0x0000	0xFFFF

Table 3.4 Register description (3 of 28)

Peripheral name	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
BUS	-	-	-	BUSSCNTP6B	Slave Bus Control Register P6B	0x1128	16	read/ write	0x0000	0xFFFF
				BUSSCNTFBU	Slave Bus Control Register FBU	0x1130	16	read/ write	0x0000	0xFFFF
	2	0x10	3,4	BUS%sERRADD	Bus Error Address Register %s	0x1820	32	read-only	0x0000 0000	0x0000 0000
	2	0x10	3,4	BUS%sERRSTAT	Bus Error Status Register %s	0x1824	8	read-only	0x00	0xFE
DTC	-	-	-	DTCCR	DTC Control Register	0x00	8	read/ write	0x08	0xFF
				DTCVBR	DTC Vector Base Register	0x04	32	read/ write	0x0000 0000	0xFFFF FFFF
				DTCST	DTC Module Start Register	0x0C	8	read/ write	0x00	0xFF
				DTCSTS	DTC Status Register	0x0E	16	read-only	0x0000	0xFFFF
ICU	8	0x1	0-7	IRQCR%s	IRQ Control Register %s	0x000	8	read/ write	0x00	0xFF
	-	-	-	NMICR	NMI Pin Interrupt Control Register	0x100	8	read/ write	0x00	0xFF
				NMIER	Non-Maskable Interrupt Enable Register	0x120	16	read/ write	0x0000	0xFFFF
				NMICLR	Non-Maskable Interrupt Status Clear Register	0x130	16	read/ write	0x0000	0xFFFF
				NMISR	Non-Maskable Interrupt Status Register	0x140	16	read-only	0x0000	0xFFFF
				WUPEN	Wake Up Interrupt Enable Register	0x1A0	32	read/ write	0x0000 0000	0xFFFF FFFF
				SELSR0	Snooze Event Link Setting Register	0x200	16	read/ write	0x0000	0xFFFF
	32	0x4	0-31	IELSR%s	ICU Event Link Setting Register %s	0x300	32	read/ write	0x0000 0000	0xFFFF FFFF
DBG	-	-	-	DBGSTR	Debug Status Register	0x00	32	read-only	0x0000 0000	0xFFFF FFFF
				DBGSTOPCR	Debug Stop Control Register	0x10	32	read/ write	0x0000 0003	0xFFFF FFFF
SYSTEM	-	-	-	SBYCR	Standby Control Register	0x00C	16	read/ write	0x0000	0xFFFF
				MSTPCRA	Module Stop Control Register A	0x01C	32	read/ write	0xFFB FFFFF	0xFFFF FFFF
				SCKDIVCR	System Clock Division Control Register	0x020	32	read/ write	0x0400 0404	0xFFFF FFFF
				SCKSCR	System Clock Source Control Register	0x026	8	read/ write	0x01	0xFF
				MOSCCR	Main Clock Oscillator Control Register	0x032	8	read/ write	0x01	0xFF

Table 3.4 Register description (4 of 28)

Peripheral name	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
SYSTEM	-	-	-	HOCOCR	High-Speed On-Chip Oscillator Control Register	0x036	8	read/ write	0x00	0xFE
				MOCOCR	Middle-Speed On-Chip Oscillator Control Register	0x038	8	read/ write	0x00	0xFF
				OSCSF	Oscillation Stabilization Flag Register	0x03C	8	read-only	0x00	0xFE
				CKOCR	Clock Out Control Register	0x03E	8	read/ write	0x00	0xFF
				OSTDCR	Oscillation Stop Detection Control Register	0x040	8	read/ write	0x00	0xFF
				OSTDSR	Oscillation Stop Detection Status Register	0x041	8	read/ write	0x00	0xFF
				MOCOUTCR	MOCO User Trimming Control Register	0x061	8	read/ write	0x00	0xFF
				HOCOUTCR	HOCO User Trimming Control Register	0x062	8	read/ write	0x00	0xFF
				SNZCR	Snooze Control Register	0x092	8	read/ write	0x00	0xFF
				SNZEDCR	Snooze End Control Register	0x094	8	read/ write	0x00	0xFF
				SNZREQCR	Snooze Request Control Register	0x098	32	read/ write	0x0000 0000	0xFFFF FFFF
				FLSTOP	Flash Operation Control Register	0x09E	8	read/ write	0x00	0xFF
				OPCCR	Operating Power Control Register	0x0A0	8	read/ write	0x02	0xFF
				MOSCWTCR	Main Clock Oscillator Wait Control Register	0x0A2	8	read/ write	0x05	0xFF
				HOCOWTCR	High-Speed On-Chip Oscillator Wait Control Register	0x0A5	8	read/ write	0x05	0xFF
				SOPCCR	Sub Operating Power Control Register	0x0AA	8	read/ write	0x00	0xFF
				RSTSR1	Reset Status Register 1	0x0C0	16	read/ write	0x0000	0xE0F8
				LVD1CR1	Voltage Monitor 1 Circuit Control Register 1	0x0E0	8	read/ write	0x01	0xFF
				LVD1SR	Voltage Monitor 1 Circuit Status Register	0x0E1	8	read/ write	0x02	0xFF
				LVD2CR1	Voltage Monitor 2 Circuit Control Register 1	0x0E2	8	read/ write	0x01	0xFF
				LVD2SR	Voltage Monitor 2 Circuit Status Register	0x0E3	8	read/ write	0x02	0xFF

Table 3.4 Register description (5 of 28)

Peripheral name	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
SYSTEM	-	-	-	PRCR	Protect Register	0xFE	16	read/ write	0x0000	0xFFFF
	-	-	-	SYOCDCR	System Control OCD Control Register	0x40E	8	read/ write	0x00	0xFF
				RSTSR0	Reset Status Register 0	0x410	8	read/ write	0x00	0xF0
				RSTSR2	Reset Status Register 2	0x411	8	read/ write	0x00	0xFE
				MOMCR	Main Clock Oscillator Mode Oscillation Control Register	0x413	8	read/ write	0x00	0xFF
				LVCMPCR	Voltage Monitor Circuit Control Register	0x417	8	read/ write	0x00	0xFF
				LVDLVLR	Voltage Detection Level Select Register	0x418	8	read/ write	0x07	0xFF
				LVD1CR0	Voltage Monitor 1 Circuit Control Register 0	0x41A	8	read/ write	0x80	0xFF
				LVD2CR0	Voltage Monitor 2 Circuit Control Register 0	0x41B	8	read/ write	0x80	0xFF
				SOSCCR	Sub-clock Oscillator Control Register	0x480	8	read/ write	0x01	0xFF
				SOMCR	Sub-clock Oscillator Mode Control Register	0x481	8	read/ write	0x00	0xFF
				LOCOCR	Low-Speed On-Chip Oscillator Control Register	0x490	8	read/ write	0x00	0xFF
				LOCOUTCR	LOCO User Trimming Control Register	0x492	8	read/ write	0x00	0xFF
PORT0,3-5,9	-	-	-	PCNTR1	Port Control Register 1	0x00	32	read/ write	0x0000 0000	0xFFFF FFFF
				PDR	Data Direction Register	0x00	16	read/ write	0x0000	0xFFFF
				PODR	Output Data Register	0x02	16	read/ write	0x0000	0xFFFF
				PCNTR2	Port Control Register 2	0x04	32	read-only	0x0000 0000	0xFFFF 0000
				PIDR	Input Data Register	0x06	16	read-only	0x0000	0xFFFF
				PCNTR3	Port Control Register 3	0x08	32	write-only	0x0000 0000	0xFFFF FFFF
				POSR	Output Set Register	0x08	16	write-only	0x0000	0xFFFF
				PORR	Output Reset Register	0x0A	16	write-only	0x0000	0xFFFF
PORT1,2	-	-	-	PCNTR1	Port Control Register 1	0x00	32	read/ write	0x0000 0000	0xFFFF FFFF

Table 3.4 Register description (6 of 28)

Peripheral name	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
PORT1,2	-	-	-	PDR	Data Direction Register	0x00	16	read/ write	0x0000	0xFFFF
				PODR	Output Data Register	0x02	16	read/ write	0x0000	0xFFFF
				PCNTR2	Port Control Register 2	0x04	32	read-only	0x0000 0000	0xFFFF 0000
				EIDR	Event Input Data Register	0x04	16	read-only	0x0000	0x0000
				PIDR	Input Data Register	0x06	16	read-only	0x0000	0xFFFF
				PCNTR3	Port Control Register 3	0x08	32	write-only	0x0000 0000	0xFFFF FFFF
				POSR	Output Set Register	0x08	16	write-only	0x0000	0xFFFF
				PORR	Output Reset Register	0x0A	16	write-only	0x0000	0xFFFF
				PCNTR4	Port Control Register 4	0x0C	32	read/ write	0x0000 0000	0xFFFF FFFF
				EOSR	Event Output Set register	0x0C	16	read/ write	0x0000	0xFFFF
				EORR	Event Output Reset Register	0x0E	16	read/ write	0x0000	0xFFFF
PFS	-	-	-	P000PFS	P000 Pin Function Control Register	0x000	32	read/ write	0x0000 0000	0xFFFF FFFF
				P000PFS_HA	P000 Pin Function Control Register	0x002	16	read/ write	0x0000	0xFFFF
				P000PFS_BY	P000 Pin Function Control Register	0x003	8	read/ write	0x00	0xFF
	4	0x4	1-4	P00%sPFS	P00%s Pin Function Control Register	0x004	32	read/ write	0x0000 0000	0xFFFF FFFF
	4	0x4	1-4	P00%sPFS_HA	P00%s Pin Function Control Register	0x006	16	read/ write	0x0000	0xFFFF
	4	0x4	1-4	P00%sPFS_BY	P00%s Pin Function Control Register	0x007	8	read/ write	0x00	0xFF
	6	0x4	10-15	P0%sPFS	P0%s Pin Function Control Register	0x028	32	read/ write	0x0000 0000	0xFFFF FFFF
	6	0x4	10-15	P0%sPFS_HA	P0%s Pin Function Control Register	0x02A	16	read/ write	0x0000	0xFFFF
	6	0x4	10-15	P0%sPFS_BY	P0%s Pin Function Control Register	0x02B	8	read/ write	0x00	0xFF
	-	-	-	P100PFS	P100 Pin Function Control Register	0x040	32	read/ write	0x0000 0000	0xFFFF FFFF
				P100PFS_HA	P100 Pin Function Control Register	0x042	16	read/ write	0x0000	0xFFFF
				P100PFS_BY	P100 Pin Function Control Register	0x043	8	read/ write	0x00	0xFF
	7	0x4	1-7	P10%sPFS	P10%s Pin Function Control Register	0x044	32	read/ write	0x0000 0000	0xFFFF FFFF
	7	0x4	1-7	P10%sPFS_HA	P10%s Pin Function Control Register	0x046	16	read/ write	0x0000	0xFFFF
	7	0x4	1-7	P10%sPFS_BY	P10%s Pin Function Control Register	0x047	8	read/ write	0x00	0xFF

Table 3.4 Register description (7 of 28)

Peripheral name	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
PFS	-	-	-	P108PFS	P108 Pin Function Control Register	0x060	32	read/ write	0x0001 0010	0xFFFF FFFF
				P108PFS_HA	P108 Pin Function Control Register	0x062	16	read/ write	0x0010	0xFFFF
				P108PFS_BY	P108 Pin Function Control Register	0x063	8	read/ write	0x10	0xFF
				P109PFS	P109 Pin Function Control Register	0x064	32	read/ write	0x0000 0000	0xFFFF FFFF
				P109PFS_HA	P109 Pin Function Control Register	0x066	16	read/ write	0x0000	0xFFFF
				P109PFS_BY	P109 Pin Function Control Register	0x067	8	read/ write	0x00	0xFF
	4	0x4	10-13	P1%sPFS	P1%s Pin Function Control Register	0x068	32	read/ write	0x0000 0000	0xFFFF FFFF
	4	0x4	10-13	P1%sPFS_HA	P1%s Pin Function Control Register	0x06A	16	read/ write	0x0000	0xFFFF
	4	0x4	10-13	P1%sPFS_BY	P1%s Pin Function Control Register	0x06B	8	read/ write	0x00	0xFF
	-	-	-	P200PFS	P200 Pin Function Control Register	0x080	32	read/ write	0x0000 0000	0xFFFF FFFF
				P200PFS_HA	P200 Pin Function Control Register	0x082	16	read/ write	0x0000	0xFFFF
				P200PFS_BY	P200 Pin Function Control Register	0x083	8	read/ write	0x00	0xFF
				P201PFS	P201 Pin Function Control Register	0x084	32	read/ write	0x0000 0010	0xFFFF FFFF
				P201PFS_HA	P201 Pin Function Control Register	0x086	16	read/ write	0x0010	0xFFFF
				P201PFS_BY	P201 Pin Function Control Register	0x087	8	read/ write	0x10	0xFF
	3	0x4	4-6	P20%sPFS	P20%s Pin Function Control Register	0x090	32	read/ write	0x0000 0000	0xFFFF FFFF
	3	0x4	4-6	P20%sPFS_HA	P20%s Pin Function Control Register	0x092	16	read/ write	0x0000	0xFFFF
	3	0x4	4-6	P20%sPFS_BY	P20%s Pin Function Control Register	0x093	8	read/ write	0x00	0xFF
	4	0x4	12-15	P2%sPFS	P2%s Pin Function Control Register	0x0B0	32	read/ write	0x0000 0000	0xFFFF FFFF
	4	0x4	12-15	P2%sPFS_HA	P2%s Pin Function Control Register	0x0B2	16	read/ write	0x0000	0xFFFF
	4	0x4	12-15	P2%sPFS_BY	P2%s Pin Function Control Register	0x0B3	8	read/ write	0x00	0xFF
	-	-	-	P300PFS	P300 Pin Function Control Register	0x0C0	32	read/ write	0x0001 0010	0xFFFF FFFF
				P300PFS_HA	P300 Pin Function Control Register	0x0C2	16	read/ write	0x0010	0xFFFF
				P300PFS_BY	P300 Pin Function Control Register	0x0C3	8	read/ write	0x10	0xFF
	4	0x4	1-4	P30%sPFS	P30%s Pin Function Control Register	0x0C4	32	read/ write	0x0000 0000	0xFFFF FFFF
	4	0x4	1-4	P30%sPFS_HA	P30%s Pin Function Control Register	0x0C6	16	read/ write	0x0000	0xFFFF

Table 3.4 Register description (8 of 28)

Peripheral name	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
PFS	4	0x4	1-4	P30%sPFS_BY	P30%s Pin Function Control Register	0x0C7	8	read/ write	0x00	0xFF
	4	0x4	0-3	P40%sPFS	P40%s Pin Function Control Register	0x100	32	read/ write	0x0000 0000	0xFFFF FFFF
	4	0x4	0-3	P40%sPFS_HA	P40%s Pin Function Control Register	0x102	16	read/ write	0x0000	0xFFFF
	4	0x4	0-3	P40%sPFS_BY	P40%s Pin Function Control Register	0x103	8	read/ write	0x00	0xFF
	3	0x4	7-9	P40%sPFS	P40%s Pin Function Control Register	0x11C	32	read/ write	0x0000 0000	0xFFFF FFFF
	3	0x4	7-9	P40%sPFS_HA	P40%s Pin Function Control Register	0x11E	16	read/ write	0x0000	0xFFFF
	3	0x4	7-9	P40%sPFS_BY	P40%s Pin Function Control Register	0x11F	8	read/ write	0x00	0xFF
	2	0x4	10,11	P4%sPFS	P4%s Pin Function Control Register	0x128	32	read/ write	0x0000 0000	0xFFFF FFFF
	2	0x4	10,11	P4%sPFS_HA	P4%s Pin Function Control Register	0x12A	16	read/ write	0x0000	0xFFFF
	2	0x4	10,11	P4%sPFS_BY	P4%s Pin Function Control Register	0x12B	8	read/ write	0x00	0xFF
	3	0x4	0-2	P50%sPFS	P50%s Pin Function Control Register	0x140	32	read/ write	0x0000 0000	0xFFFF FFFF
	3	0x4	0-2	P50%sPFS_HA	P50%s Pin Function Control Register	0x142	16	read/ write	0x0000	0xFFFF
	3	0x4	0-2	P50%sPFS_BY	P50%s Pin Function Control Register	0x143	8	read/ write	0x00	0xFF
	-	-	-	P914PFS	P914 Pin Function Control Register	0x278	32	read/ write	0x0001 0000	0xFFFF FFFF
				P914PFS_HA	P914 Pin Function Control Register	0x27A	16	read/ write	0x0000	0xFFFF
				P914PFS_BY	P914 Pin Function Control Register	0x27B	8	read/ write	0x00	0xFF
				P915PFS	P915 Pin Function Control Register	0x27C	32	read/ write	0x0001 0000	0xFFFF FFFF
				P915PFS_HA	P915 Pin Function Control Register	0x27E	16	read/ write	0x0000	0xFFFF
				P915PFS_BY	P915 Pin Function Control Register	0x27F	8	read/ write	0x00	0xFF
PMISC	-	-	-	PWPR	Write-Protect Register	0x03	8	read/ write	0x80	0xFF
ELC	-	-	-	ELCR	Event Link Controller Register	0x00	8	read/ write	0x00	0xFF
	2	0x2	0,1	ELSEGR%s	Event Link Software Event Generation Register %s	0x02	8	read/ write	0x80	0xFF
	4	0x4	0-3	ELSR%s	Event Link Setting Register %s	0x10	16	read/ write	0x0000	0xFFFF
	2	0x4	8,9	ELSR%s	Event Link Setting Register %s	0x30	16	read/ write	0x0000	0xFFFF
	2	0x4	14,15	ELSR%s	Event Link Setting Register %s	0x48	16	read/ write	0x0000	0xFFFF
	4	0x4	18-21	ELSR%s	Event Link Setting Register %s	0x58	16	read/ write	0x0000	0xFFFF

Table 3.4 Register description (9 of 28)

Peripheral name	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
POEG	2	0x100	A,B	POEGG%s	POEG Group %s Setting Register	0x00	32	read/ write	0x0000 0000	0xFFFF FFFF
RTC	-	-	-	R64CNT	64-Hz Counter	0x00	8	read-only	0x00	0x80
				RSECCNT	Second Counter	0x02	8	read/ write	0x00	0x00
				BCNT0	Binary Counter 0	0x02	8	read/ write	0x00	0x00
				RMINCNT	Minute Counter	0x04	8	read/ write	0x00	0x00
				BCNT1	Binary Counter 1	0x04	8	read/ write	0x00	0x00
				RHRCNT	Hour Counter	0x06	8	read/ write	0x00	0x00
				BCNT2	Binary Counter 2	0x06	8	read/ write	0x00	0x00
				RWKCNT	Day-of-Week Counter	0x08	8	read/ write	0x00	0x00
				BCNT3	Binary Counter 3	0x08	8	read/ write	0x00	0x00
				RDAYCNT	Day Counter	0x0A	8	read/ write	0x00	0xC0
				RMONCNT	Month Counter	0x0C	8	read/ write	0x00	0xE0
				RYRCNT	Year Counter	0x0E	16	read/ write	0x0000	0xFF00
				RSECAR	Second Alarm Register	0x10	8	read/ write	0x00	0x00
				BCNT0AR	Binary Counter 0 Alarm Register	0x10	8	read/ write	0x00	0x00
				RMINAR	Minute Alarm Register	0x12	8	read/ write	0x00	0x00
				BCNT1AR	Binary Counter 1 Alarm Register	0x12	8	read/ write	0x00	0x00
				RHRAR	Hour Alarm Register	0x14	8	read/ write	0x00	0x00
				BCNT2AR	Binary Counter 2 Alarm Register	0x14	8	read/ write	0x00	0x00
				RWKAR	Day-of-Week Alarm Register	0x16	8	read/ write	0x00	0x00
				BCNT3AR	Binary Counter 3 Alarm Register	0x16	8	read/ write	0x00	0x00
				RDAYAR	Date Alarm Register	0x18	8	read/ write	0x00	0x00
				BCNT0AER	Binary Counter 0 Alarm Enable Register	0x18	8	read/ write	0x00	0x00
				RMONAR	Month Alarm Register	0x1A	8	read/ write	0x00	0x00
				BCNT1AER	Binary Counter 1 Alarm Enable Register	0x1A	8	read/ write	0x00	0x00
				RYRAR	Year Alarm Register	0x1C	16	read/ write	0x0000	0xFF00

Table 3.4 Register description (10 of 28)

Peripheral name	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
RTC	-	-	-	BCNT2AER	Binary Counter 2 Alarm Enable Register	0x1C	16	read/ write	0x0000	0xFF00
				RYRAREN	Year Alarm Enable Register	0x1E	8	read/ write	0x00	0x00
				BCNT3AER	Binary Counter 3 Alarm Enable Register	0x1E	8	read/ write	0x00	0x00
				RCR1	RTC Control Register 1	0x22	8	read/ write	0x00	0x0A
				RCR2	RTC Control Register 2	0x24	8	read/ write	0x00	0x0E
				RCR4	RTC Control Register 4	0x28	8	read/ write	0x00	0xFE
				RFRH	Frequency Register H	0x2A	16	read/ write	0x0000	0xFFFE
				RFRL	Frequency Register L	0x2C	16	read/ write	0x0000	0x0000
				RADJ	Time Error Adjustment Register	0x2E	8	read/ write	0x00	0x00
WDT	-	-	-	WDTRR	WDT Refresh Register	0x00	8	read/ write	0xFF	0xFF
				WDTCR	WDT Control Register	0x02	16	read/ write	0x33F3	0xFFFF
				WDTSR	WDT Status Register	0x04	16	read/ write	0x0000	0xFFFF
				WDTRCR	WDT Reset Control Register	0x06	8	read/ write	0x80	0xFF
				WDTCSTPR	WDT Count Stop Control Register	0x08	8	read/ write	0x80	0xFF
IWDT	-	-	-	IWDTRR	IWDT Refresh Register	0x00	8	read/ write	0xFF	0xFF
				IWDTSR	IWDT Status Register	0x04	16	read/ write	0x0000	0xFFFF
CAC	-	-	-	CACR0	CAC Control Register 0	0x00	8	read/ write	0x00	0xFF
				CACR1	CAC Control Register 1	0x01	8	read/ write	0x00	0xFF
				CACR2	CAC Control Register 2	0x02	8	read/ write	0x00	0xFF
				CAICR	CAC Interrupt Control Register	0x03	8	read/ write	0x00	0xFF
				CASTR	CAC Status Register	0x04	8	read-only	0x00	0xFF
				CAULVR	CAC Upper-Limit Value Setting Register	0x06	16	read/ write	0x0000	0xFFFF
				CALLVR	CAC Lower-Limit Value Setting Register	0x08	16	read/ write	0x0000	0xFFFF
				CACNTBR	CAC Counter Buffer Register	0x0A	16	read-only	0x0000	0xFFFF
MSTP	-	-	-	MSTPCRB	Module Stop Control Register B	0x00	32	read/ write	0xFFFF FFFF	0xFFFF FFFF

Table 3.4 Register description (11 of 28)

Peripheral name	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
MSTP	-	-	-	MSTPCRC	Module Stop Control Register C	0x04	32	read/ write	0xFFFF FFFF	0xFFFF FFFF
				MSTPCRD	Module Stop Control Register D	0x08	32	read/ write	0xFFFF FFFF	0xFFFF FFFF
CAN0	32	0x10	0-31	MB%s_ID	Mailbox Register	0x200	32	read/ write	0x0000 0000	0x0000 0000
	32	0x10	0-31	MB%s_DL	Mailbox Register	0x204	16	read/ write	0x0000	0x0000
	32	0x10	0-31	MB%s_D0	Mailbox Register	0x206	8	read/ write	0x00	0x00
	32	0x10	0-31	MB%s_D1	Mailbox Register	0x207	8	read/ write	0x00	0x00
	32	0x10	0-31	MB%s_D2	Mailbox Register	0x208	8	read/ write	0x00	0x00
	32	0x10	0-31	MB%s_D3	Mailbox Register	0x209	8	read/ write	0x00	0x00
	32	0x10	0-31	MB%s_D4	Mailbox Register	0x20A	8	read/ write	0x00	0x00
	32	0x10	0-31	MB%s_D5	Mailbox Register	0x20B	8	read/ write	0x00	0x00
	32	0x10	0-31	MB%s_D6	Mailbox Register	0x20C	8	read/ write	0x00	0x00
	32	0x10	0-31	MB%s_D7	Mailbox Register	0x20D	8	read/ write	0x00	0x00
	32	0x10	0-31	MB%s_TS	Mailbox Register	0x20E	16	read/ write	0x0000	0x0000
	8	0x4	0-7	MKR[%s]	Mask Register	0x400	32	read/ write	0x0000 0000	0x0000 0000
	2	0x4	0,1	FIDCR%s	FIFO Received ID Compare Registers	0x420	32	read/ write	0x0000 0000	0x0000 0000
	-	-	-	MKIVLR	Mask Invalid Register	0x428	32	read/ write	0x0000 0000	0x0000 0000
				MIER	Mailbox Interrupt Enable Register (Normal mailbox mode)	0x42C	32	read/ write	0x0000 0000	0x0000 0000
				MIER_FIFO	Mailbox Interrupt Enable Register (FIFO mailbox mode)	0x42C	32	read/ write	0x0000 0000	0x0000 0000
	32	0x1	0-31	MCTL_TX[%s]	Message Control Register (Transmit mode (when the TRMREQ bit is 1 and the RECREQ bit is 0))	0x820	8	read/ write	0x00	0xFF
	32	0x1	0-31	MCTL_RX[%s]	Message Control Register (Receive mode (when the TRMREQ bit is 0 and the RECREQ bit is 1))	0x820	8	read/ write	0x00	0xFF
	-	-	-	CTLR	Control Register	0x840	16	read/ write	0x0500	0xFFFF

Table 3.4 Register description (12 of 28)

Peripheral name	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
CAN0	-	-	-	STR	Status Register	0x842	16	read-only	0x0500	0xFFFF
				BCR	Bit Configuration Register	0x844	32	read/write	0x0000 0000	0xFFFF FFFF
				RFCR	Receive FIFO Control Register	0x848	8	read/write	0x80	0xFF
				RFPCR	Receive FIFO Pointer Control Register	0x849	8	write-only	0x00	0x00
				TFCR	Transmit FIFO Control Register	0x84A	8	read/write	0x80	0xFF
				TFPCR	Transmit FIFO Pointer Control Register	0x84B	8	write-only	0x00	0x00
				EIER	Error Interrupt Enable Register	0x84C	8	read/write	0x00	0xFF
				EIFR	Error Interrupt Factor Judge Register	0x84D	8	read/write	0x00	0xFF
				RECR	Receive Error Count Register	0x84E	8	read-only	0x00	0xFF
				TECR	Transmit Error Count Register	0x84F	8	read-only	0x00	0xFF
				ECSR	Error Code Store Register	0x850	8	read/write	0x00	0xFF
				CSSR	Channel Search Support Register	0x851	8	read/write	0x00	0x00
				MSSR	Mailbox Search Status Register	0x852	8	read-only	0x80	0xFF
				MSMR	Mailbox Search Mode Register	0x853	8	read/write	0x00	0xFF
				TSR	Time Stamp Register	0x854	16	read-only	0x0000	0xFFFF
				AFSR	Acceptance Filter Support Register	0x856	16	read/write	0x0000	0x0000
				TCR	Test Control Register	0x858	8	read/write	0x00	0xFF
IIC0	-	-	-	ICCR1	I^2C Bus Control Register 1	0x00	8	read/write	0x1F	0xFF
				ICCR2	I^2C Bus Control Register 2	0x01	8	read/write	0x00	0xFF
				ICMR1	I^2C Bus Mode Register 1	0x02	8	read/write	0x08	0xFF
				ICMR2	I^2C Bus Mode Register 2	0x03	8	read/write	0x06	0xFF
				ICMR3	I^2C Bus Mode Register 3	0x04	8	read/write	0x00	0xFF
				ICFER	I^2C Bus Function Enable Register	0x05	8	read/write	0x72	0xFF
				ICSER	I^2C Bus Status Enable Register	0x06	8	read/write	0x09	0xFF
				ICIER	I^2C Bus Interrupt Enable Register	0x07	8	read/write	0x00	0xFF

Table 3.4 Register description (13 of 28)

Peripheral name	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
IIC0	-	-	-	ICSR1	I2C Bus Status Register 1	0x08	8	read/ write	0x00	0xFF
				ICSR2	I2C Bus Status Register 2	0x09	8	read/ write	0x00	0xFF
	3	0x2	0-2	SARL%s	Slave Address Register L%s	0x0A	8	read/ write	0x00	0xFF
	3	0x2	0-2	SARU%s	Slave Address Register U%s	0x0B	8	read/ write	0x00	0xFF
	-	-	-	ICBRL	I2C Bus Bit Rate Low-Level Register	0x10	8	read/ write	0xFF	0xFF
				ICBRH	I2C Bus Bit Rate High-Level Register	0x11	8	read/ write	0xFF	0xFF
				ICDRT	I2C Bus Transmit Data Register	0x12	8	read/ write	0xFF	0xFF
				ICDRR	I2C Bus Receive Data Register	0x13	8	read-only	0x00	0xFF
				ICWUR	I2C Bus Wake Up Unit Register	0x16	8	read/ write	0x10	0xFF
				ICWUR2	Reserved	0x17	8	read/ write	0xFD	0xFF
IIC1	-	-	-	ICCR1	I2C Bus Control Register 1	0x00	8	read/ write	0x1F	0xFF
				ICCR2	I2C Bus Control Register 2	0x01	8	read/ write	0x00	0xFF
				ICMR1	I2C Bus Mode Register 1	0x02	8	read/ write	0x08	0xFF
				ICMR2	I2C Bus Mode Register 2	0x03	8	read/ write	0x06	0xFF
				ICMR3	I2C Bus Mode Register 3	0x04	8	read/ write	0x00	0xFF
				ICFER	I2C Bus Function Enable Register	0x05	8	read/ write	0x72	0xFF
				ICSER	I2C Bus Status Enable Register	0x06	8	read/ write	0x09	0xFF
				ICIER	I2C Bus Interrupt Enable Register	0x07	8	read/ write	0x00	0xFF
				ICSR1	I2C Bus Status Register 1	0x08	8	read/ write	0x00	0xFF
				ICSR2	I2C Bus Status Register 2	0x09	8	read/ write	0x00	0xFF
	3	0x2	0-2	SARL%s	Slave Address Register L%s	0x0A	8	read/ write	0x00	0xFF
	3	0x2	0-2	SARU%s	Slave Address Register U%s	0x0B	8	read/ write	0x00	0xFF
	-	-	-	ICBRL	I2C Bus Bit Rate Low-Level Register	0x10	8	read/ write	0xFF	0xFF
				ICBRH	I2C Bus Bit Rate High-Level Register	0x11	8	read/ write	0xFF	0xFF
				ICDRT	I2C Bus Transmit Data Register	0x12	8	read/ write	0xFF	0xFF
				ICDRR	I2C Bus Receive Data Register	0x13	8	read-only	0x00	0xFF

Table 3.4 Register description (14 of 28)

Peripheral name	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
DOC	-	-	-	DOCR	DOC Control Register	0x00	8	read/ write	0x00	0xFF
				DODIR	DOC Data Input Register	0x02	16	read/ write	0x0000	0xFFFF
				DODSR	DOC Data Setting Register	0x04	16	read/ write	0x0000	0xFFFF
ADC140	-	-	-	ADCSR	A/D Control Register	0x000	16	read/ write	0x0000	0xFFFF
				ADANSA0	A/D Channel Select Register A0	0x004	16	read/ write	0x0000	0xFFFF
				ADANSA1	A/D Channel Select Register A1	0x006	16	read/ write	0x0000	0xFFFF
				ADADS0	A/D-Converted Value Addition/ Average Channel Select Register 0	0x008	16	read/ write	0x0000	0xFFFF
				ADADS1	A/D-Converted Value Addition/ Average Channel Select Register 1	0x00A	16	read/ write	0x0000	0xFFFF
				ADADC	A/D-Converted Value Addition/ Average Count Select Register	0x00C	8	read/ write	0x00	0xFF
				ADCER	A/D Control Extended Register	0x00E	16	read/ write	0x0000	0xFFFF
				ADSTRGR	A/D Conversion Start Trigger Select Register	0x010	16	read/ write	0x0000	0xFFFF
				ADEXICR	A/D Conversion Extended Input Control Register	0x012	16	read/ write	0x0000	0xFFFF
				ADANSB0	A/D Channel Select Register B0	0x014	16	read/ write	0x0000	0xFFFF
				ADANSB1	A/D Channel Select Register B1	0x016	16	read/ write	0x0000	0xFFFF
				ADDBLDR	A/D Data Duplication Register	0x018	16	read-only	0x0000	0xFFFF
				ADTSDR	A/D Temperature Sensor Data Register	0x01A	16	read-only	0x0000	0xFFFF
				ADOCDR	A/D Internal Reference Voltage Data Register	0x01C	16	read-only	0x0000	0xFFFF
				ADRD	A/D Self-Diagnosis Data Register	0x01E	16	read-only	0x0000	0xFFFF
	14	0x2	0-13	ADDR%s	A/D Data Register %s	0x020	16	read-only	0x0000	0xFFFF
	7	0x2	16-22	ADDR%s	A/D Data Register %s	0x040	16	read-only	0x0000	0xFFFF
	-	-	-	ADDISCR	A/D Disconnection Detection Control Register	0x07A	8	read/ write	0x00	0xFF

Table 3.4 Register description (15 of 28)

Peripheral name	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
ADC140	-	-	-	ADGSPCR	A/D Group Scan Priority Control Register	0x080	16	read/ write	0x0000	0xFFFF
				ADDBLDRA	A/D Data Duplication Register A	0x084	16	read-only	0x0000	0xFFFF
				ADDBLDRB	A/D Data Duplication Register B	0x086	16	read-only	0x0000	0xFFFF
				ADHVREFCNT	A/D High-Potential/ Low-Potential Reference Voltage Control Register	0x08A	8	read/ write	0x00	0xFF
				ADWINMON	A/D Compare Function Window A/ B Status Monitor Register	0x08C	8	read-only	0x00	0xFF
				ADCMPCR	A/D Compare Function Control Register	0x090	16	read/ write	0x0000	0xFFFF
				ADCMPANSER	A/D Compare Function Window A Extended Input Select Register	0x092	8	read/ write	0x00	0xFF
				ADCMPLER	A/D Compare Function Window A Extended Input Comparison Condition Setting Register	0x093	8	read/ write	0x00	0xFF
				ADCMPANSR0	A/D Compare Function Window A Channel Select Register 0	0x094	16	read/ write	0x0000	0xFFFF
				ADCMPANSR1	A/D Compare Function Window A Channel Select Register 1	0x096	16	read/ write	0x0000	0xFFFF
				ADCMPLR0	A/D Compare Function Window A Comparison Condition Setting Register 0	0x098	16	read/ write	0x0000	0xFFFF
				ADCMPLR1	A/D Compare Function Window A Comparison Condition Setting Register 1	0x09A	16	read/ write	0x0000	0xFFFF
				ADCMPDR0	A/D Compare Function Window A Lower-Side Level Setting Register	0x09C	16	read/ write	0x0000	0xFFFF
				ADCMPDR1	A/D Compare Function Window A Upper-Side Level Setting Register	0x09E	16	read/ write	0x0000	0xFFFF
				ADCMPSR0	A/D Compare Function Window A Channel Status Register 0	0x0A0	16	read/ write	0x0000	0xFFFF

Table 3.4 Register description (16 of 28)

Peripheral name	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
ADC140	-	-	-	ADCMPSR1	A/D Compare Function Window A Channel Status Register 1	0x0A2	16	read/ write	0x0000	0xFFFF
				ADCMPSER	A/D Compare Function Window A Extended Input Channel Status Register	0x0A4	8	read/ write	0x00	0xFF
				ADCMPBNSR	A/D Compare Function Window B Channel Selection Register	0x0A6	8	read/ write	0x00	0xFF
				ADWINLLB	A/D Compare Function Window B Lower-Side Level Setting Register	0x0A8	16	read/ write	0x0000	0xFFFF
				ADWINULB	A/D Compare Function Window B Upper-Side Level Setting Register	0x0AA	16	read/ write	0x0000	0xFFFF
				ADCMPBSR	A/D Compare Function Window B Status Register	0x0AC	8	read/ write	0x00	0xFF
				ADSSTRL	A/D Sampling State Register L	0x0DD	8	read/ write	0x0D	0xFF
				ADSSTRT	A/D Sampling State Register T	0x0DE	8	read/ write	0x0D	0xFF
				ADSSTRO	A/D Sampling State Register O	0x0DF	8	read/ write	0x0D	0xFF
	14	0x1	00-13	ADSSTR%s	A/D Sampling State Register %s	0x0E0	8	read/ write	0x0D	0xFF
SCI0	-	-	-	SMR	Serial Mode Register (SCMR.SMIF = 0)	0x00	8	read/ write	0x00	0xFF
				SMR_SMCI	Serial Mode Register (SCMR.SMIF = 1)	0x00	8	read/ write	0x00	0xFF
				BRR	Bit Rate Register	0x01	8	read/ write	0xFF	0xFF
				SCR	Serial Control Register (SCMR.SMIF = 0)	0x02	8	read/ write	0x00	0xFF
				SCR_SMCI	Serial Control Register (SCMR.SMIF =1)	0x02	8	read/ write	0x00	0xFF
				TDR	Transmit Data Register	0x03	8	read/ write	0xFF	0xFF
				SSR	Serial Status Register (SCMR.SMIF = 0 and FCR.FM=0)	0x04	8	read/ write	0x84	0xFF
				SSR_FIFO	Serial Status Register (SCMR.SMIF = 0 and FCR.FM=1)	0x04	8	read/ write	0x80	0xFD

Table 3.4 Register description (17 of 28)

Peripheral name	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
SCI0	-	-	-	SSR_SMCI	Serial Status Register (SCMR.SMIF = 1)	0x04	8	read/ write	0x84	0xFF
				RDR	Receive Data Register	0x05	8	read-only	0x00	0xFF
				SCMR	Smart Card Mode Register	0x06	8	read/ write	0xF2	0xFF
				SEMR	Serial Extended Mode Register	0x07	8	read/ write	0x00	0xFF
				SNFR	Noise Filter Setting Register	0x08	8	read/ write	0x00	0xFF
				SIMR1	I^2C Mode Register 1	0x09	8	read/ write	0x00	0xFF
				SIMR2	I^2C Mode Register 2	0x0A	8	read/ write	0x00	0xFF
				SIMR3	I^2C Mode Register 3	0x0B	8	read/ write	0x00	0xFF
				SISR	I^2C Status Register	0x0C	8	read-only	0x00	0xCB
				SPMR	SPI Mode Register	0x0D	8	read/ write	0x00	0xFF
				TDRHL	Transmit 9-bit Data Register	0x0E	16	read/ write	0xFFFF	0xFFFF
				FTDRHL	Transmit FIFO Data Register HL	0x0E	16	write-only	0xFFFF	0xFFFF
				FTDRH	Transmit FIFO Data Register H	0x0E	8	write-only	0xFF	0xFF
				FTDRL	Transmit FIFO Data Register L	0x0F	8	write-only	0xFF	0xFF
				RDRHL	Receive 9-bit Data Register	0x10	16	read-only	0x0000	0xFFFF
				FRDRHL	Receive FIFO Data Register HL	0x10	16	read-only	0x0000	0xFFFF
				FRDRH	Receive FIFO Data Register H	0x10	8	read-only	0x00	0xFF
				FRDRL	Receive FIFO Data Register L	0x11	8	read-only	0x00	0xFF
				MDDR	Modulation Duty Register	0x12	8	read/ write	0xFF	0xFF
				DCCR	Data Compare Match Control Register	0x13	8	read/ write	0x40	0xFF
				FCR	FIFO Control Register	0x14	16	read/ write	0xF800	0xFFFF
				FDR	FIFO Data Count Register	0x16	16	read-only	0x0000	0xFFFF
				LSR	Line Status Register	0x18	16	read-only	0x0000	0xFFFF
				CDR	Compare Match Data Register	0x1A	16	read/ write	0x0000	0xFFFF
				SPTR	Serial Port Register	0x1C	8	read/ write	0x03	0xFF

Table 3.4 Register description (18 of 28)

Peripheral name	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
SCI1,9	-	-	-	SMR	Serial Mode Register (SCMR.SMIF = 0)	0x00	8	read/ write	0x00	0xFF
				SMR_SMCI	Serial Mode Register (SCMR.SMIF = 1)	0x00	8	read/ write	0x00	0xFF
				BRR	Bit Rate Register	0x01	8	read/ write	0xFF	0xFF
				SCR	Serial Control Register (SCMR.SMIF = 0)	0x02	8	read/ write	0x00	0xFF
				SCR_SMCI	Serial Control Register (SCMR.SMIF =1)	0x02	8	read/ write	0x00	0xFF
				TDR	Transmit Data Register	0x03	8	read/ write	0xFF	0xFF
				SSR	Serial Status Register (SCMR.SMIF = 0 and FCR.FM=0)	0x04	8	read/ write	0x84	0xFF
				SSR_SMCI	Serial Status Register (SCMR.SMIF = 1)	0x04	8	read/ write	0x84	0xFF
				RDR	Receive Data Register	0x05	8	read-only	0x00	0xFF
				SCMR	Smart Card Mode Register	0x06	8	read/ write	0xF2	0xFF
				SEMR	Serial Extended Mode Register	0x07	8	read/ write	0x00	0xFF
				SNFR	Noise Filter Setting Register	0x08	8	read/ write	0x00	0xFF
				SIMR1	I^2C Mode Register 1	0x09	8	read/ write	0x00	0xFF
				SIMR2	I^2C Mode Register 2	0x0A	8	read/ write	0x00	0xFF
				SIMR3	I^2C Mode Register 3	0x0B	8	read/ write	0x00	0xFF
				SISR	I^2C Status Register	0x0C	8	read-only	0x00	0xCB
				SPMR	SPI Mode Register	0x0D	8	read/ write	0x00	0xFF
				TDRHL	Transmit 9-bit Data Register	0x0E	16	read/ write	0xFFFF	0xFFFF
				RDRHL	Receive 9-bit Data Register	0x10	16	read-only	0x0000	0xFFFF
				MDDR	Modulation Duty Register	0x12	8	read/ write	0xFF	0xFF
				DCCR	Data Compare Match Control Register	0x13	8	read/ write	0x40	0xFF
				CDR	Compare Match Data Register	0x1A	16	read/ write	0x0000	0xFFFF
				SPTR	Serial Port Register	0x1C	8	read/ write	0x03	0xFF

Table 3.4 Register description (19 of 28)

Peripheral name	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
SPI0,1	-	-	-	SPCR	SPI Control Register	0x00	8	read/ write	0x00	0xFF
				SSLP	SPI Slave Select Polarity Register	0x01	8	read/ write	0x00	0xFF
				SPPCR	SPI Pin Control Register	0x02	8	read/ write	0x00	0xFF
				SPSR	SPI Status Register	0x03	8	read/ write	0x20	0xFF
				SPDR	SPI Data Register	0x04	32	read/ write	0x0000 0000	0xFFFF FFFF
				SPDR_HA	SPI Data Register (halfword access)	0x04	16	read/ write	0x0000	0xFFFF
				SPBR	SPI Bit Rate Register	0x0A	8	read/ write	0xFF	0xFF
				SPDCR	SPI Data Control Register	0x0B	8	read/ write	0x00	0xFF
				SPCKD	SPI Clock Delay Register	0x0C	8	read/ write	0x00	0xFF
				SSLND	SPI Slave Select Negation Delay Register	0x0D	8	read/ write	0x00	0xFF
				SPND	SPI Next-Access Delay Register	0x0E	8	read/ write	0x00	0xFF
				SPCR2	SPI Control Register 2	0x0F	8	read/ write	0x00	0xFF
				SPCMD0	SPI Command Register 0	0x10	16	read/ write	0x070D	0xFFFF
CRC	-	-	-	CRCCR0	CRC Control Register 0	0x00	8	read/ write	0x00	0xFF
				CRCCR1	CRC Control Register 1	0x01	8	read/ write	0x00	0xFF
				CRCDIR	CRC Data Input Register	0x04	32	read/ write	0x0000 0000	0xFFFF FFFF
				CRCDIR_BY	CRC Data Input Register (byte access)	0x04	8	read/ write	0x00	0xFF
				CRCDOR	CRC Data Output Register	0x08	32	read/ write	0x0000 0000	0xFFFF FFFF
				CRCDOR_HA	CRC Data Output Register (halfword access)	0x08	16	read/ write	0x0000	0xFFFF
				CRCDOR_BY	CRC Data Output Register (byte access)	0x08	8	read/ write	0x00	0xFF
				CRCSAR	Snoop Address Register	0x0C	16	read/ write	0x0000	0xFFFF
GPT320	-	-	-	GTWP	General PWM Timer Write-Protection Register	0x00	32	read/ write	0x0000 0000	0xFFFF FFFF
				GTSTR	General PWM Timer Software Start Register	0x04	32	read/ write	0x0000 0000	0xFFFF FFFF

Table 3.4 Register description (20 of 28)

Peripheral name	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
GPT320	-	-	-	GTSTP	General PWM Timer Software Stop Register	0x08	32	read/ write	0xFFFF FFFF	0xFFFF FFFF
				GTCLR	General PWM Timer Software Clear Register	0x0C	32	write-only	0x0000 0000	0xFFFF FFFF
				GTSSR	General PWM Timer Start Source Select Register	0x10	32	read/ write	0x0000 0000	0xFFFF FFFF
				GTPSR	General PWM Timer Stop Source Select Register	0x14	32	read/ write	0x0000 0000	0xFFFF FFFF
				GTCSR	General PWM Timer Clear Source Select Register	0x18	32	read/ write	0x0000 0000	0xFFFF FFFF
				GTUPSR	General PWM Timer Up Count Source Select Register	0x1C	32	read/ write	0x0000 0000	0xFFFF FFFF
				GTDNSR	General PWM Timer Down Count Source Select Register	0x20	32	read/ write	0x0000 0000	0xFFFF FFFF
				GTICASR	General PWM Timer Input Capture Source Select Register A	0x24	32	read/ write	0x0000 0000	0xFFFF FFFF
				GTICBSR	General PWM Timer Input Capture Source Select Register B	0x28	32	read/ write	0x0000 0000	0xFFFF FFFF
				GTCR	General PWM Timer Control Register	0x2C	32	read/ write	0x0000 0000	0xFFFF FFFF
				GTUDDTYC	General PWM Timer Count Direction and Duty Setting Register	0x30	32	read/ write	0x0000 0001	0xFFFF FFFF
				GTIOR	General PWM Timer I/O Control Register	0x34	32	read/ write	0x0000 0000	0xFFFF FFFF
				GTINTAD	General PWM Timer Interrupt Output Setting Register	0x38	32	read/ write	0x0000 0000	0xFFFF FFFF
				GTST	General PWM Timer Status Register	0x3C	32	read/ write	0x0000 8000	0xFFFF FFFF
				GTBER	General PWM Timer Buffer Enable Register	0x40	32	read/ write	0x0000 0000	0xFFFF FFFF
				GTCNT	General PWM Timer Counter	0x48	32	read/ write	0x0000 0000	0xFFFF FFFF
				GTCCRA	General PWM Timer Compare Capture Register A	0x4C	32	read/ write	0xFFFF FFFF	0xFFFF FFFF
				GTCCRB	General PWM Timer Compare Capture Register B	0x50	32	read/ write	0xFFFF FFFF	0xFFFF FFFF
				GTCCRC	General PWM Timer Compare Capture Register C	0x54	32	read/ write	0xFFFF FFFF	0xFFFF FFFF

Table 3.4 Register description (21 of 28)

Peripheral name	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
GPT320	-	-	-	GTCCRE	General PWM Timer Compare Capture Register E	0x58	32	read/ write	0xFFFF FFFF	0xFFFF FFFF
				GTCCRD	General PWM Timer Compare Capture Register D	0x5C	32	read/ write	0xFFFF FFFF	0xFFFF FFFF
				GTCCRF	General PWM Timer Compare Capture Register F	0x60	32	read/ write	0xFFFF FFFF	0xFFFF FFFF
				GTPR	General PWM Timer Cycle Setting Register	0x64	32	read/ write	0xFFFF FFFF	0xFFFF FFFF
				GTPBR	General PWM Timer Cycle Setting Buffer Register	0x68	32	read/ write	0xFFFF FFFF	0xFFFF FFFF
				GTDTCR	General PWM Timer Dead Time Control Register	0x88	32	read/ write	0x0000 0000	0xFFFF FFFF
				GTDVU	General PWM Timer Dead Time Value Register U	0x8C	32	read/ write	0xFFFF FFFF	0xFFFF FFFF
GPT161-6	-	-	-	GTWP	General PWM Timer Write-Protection Register	0x00	32	read/ write	0x0000 0000	0xFFFF FFFF
				GTSTR	General PWM Timer Software Start Register	0x04	32	read/ write	0x0000 0000	0xFFFF FFFF
				GTSTP	General PWM Timer Software Stop Register	0x08	32	read/ write	0xFFFF FFFF	0xFFFF FFFF
				GTCLR	General PWM Timer Software Clear Register	0x0C	32	write-only	0x0000 0000	0xFFFF FFFF
				GTSSR	General PWM Timer Start Source Select Register	0x10	32	read/ write	0x0000 0000	0xFFFF FFFF
				GTPSR	General PWM Timer Stop Source Select Register	0x14	32	read/ write	0x0000 0000	0xFFFF FFFF
				GTCSR	General PWM Timer Clear Source Select Register	0x18	32	read/ write	0x0000 0000	0xFFFF FFFF
				GTUPSR	General PWM Timer Up Count Source Select Register	0x1C	32	read/ write	0x0000 0000	0xFFFF FFFF
				GTDNSR	General PWM Timer Down Count Source Select Register	0x20	32	read/ write	0x0000 0000	0xFFFF FFFF
				GTICASR	General PWM Timer Input Capture Source Select Register A	0x24	32	read/ write	0x0000 0000	0xFFFF FFFF
				GTICBSR	General PWM Timer Input Capture Source Select Register B	0x28	32	read/ write	0x0000 0000	0xFFFF FFFF

Table 3.4 Register description (22 of 28)

Peripheral name	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
GPT161-6	-	-	-	GTCR	General PWM Timer Control Register	0x2C	32	read/ write	0x0000 0000	0xFFFF FFFF
				GTUDDTYC	General PWM Timer Count Direction and Duty Setting Register	0x30	32	read/ write	0x0000 0001	0xFFFF FFFF
				GTIOR	General PWM Timer I/O Control Register	0x34	32	read/ write	0x0000 0000	0xFFFF FFFF
				GTINTAD	General PWM Timer Interrupt Output Setting Register	0x38	32	read/ write	0x0000 0000	0xFFFF FFFF
				GTST	General PWM Timer Status Register	0x3C	32	read/ write	0x0000 8000	0xFFFF FFFF
				GTBER	General PWM Timer Buffer Enable Register	0x40	32	read/ write	0x0000 0000	0xFFFF FFFF
				GTCNT	General PWM Timer Counter	0x48	32	read/ write	0x0000 0000	0xFFFF FFFF
				GTCCRA	General PWM Timer Compare Capture Register A	0x4C	32	read/ write	0x0000 FFFF	0xFFFF FFFF
				GTCCRB	General PWM Timer Compare Capture Register B	0x50	32	read- write	0x0000 FFFF	0xFFFF FFFF
				GTCCRC	General PWM Timer Compare Capture Register C	0x54	32	read/ write	0x0000 FFFF	0xFFFF FFFF
				GTCCRE	General PWM Timer Compare Capture Register E	0x58	32	read/ write	0x0000 FFFF	0xFFFF FFFF
				GTCCRD	General PWM Timer Compare Capture Register D	0x5C	32	read/ write	0x0000 FFFF	0xFFFF FFFF
				GTCCRF	General PWM Timer Compare Capture Register F	0x60	32	read/ write	0x0000 FFFF	0xFFFF FFFF
				GTPR	General PWM Timer Cycle Setting Register	0x64	32	read/ write	0x0000 FFFF	0xFFFF FFFF
				GTPBR	General PWM Timer Cycle Setting Buffer Register	0x68	32	read/ write	0x0000 FFFF	0xFFFF FFFF
				GTDTCR	General PWM Timer Dead Time Control Register	0x88	32	read/ write	0x0000 0000	0xFFFF FFFF
				GTDVU	General PWM Timer Dead Time Value Register U	0x8C	32	read/ write	0x0000 FFFF	0xFFFF FFFF
GPT_OPS	-	-	-	OPSCR	Output Phase Switching Control Register	0x0	32	read/ write	0x0000 0000	0xFFFF FFFF
GPT_ODC	-	-	-	GTDLYCR	PWM Output Delay Control Register	0x00	16	read/ write	0x0000	0xFFFF
				GTDLYCR2	PWM Output Delay Control Register 2	0x02	16	read/ write	0x0000	0xFFFF

Table 3.4 Register description (23 of 28)

Peripheral name	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
GPT_ODC	3	0x4	1-3	GTDLYR%sA	GTIOC%sA Rising Output Delay Register	0x1C	16	read/ write	0x0000	0xFFFF
	3	0x4	1-3	GTDLYR%sB	GTIOC%sB Rising Output Delay Register	0x1E	16	read/ write	0x0000	0xFFFF
	3	0x4	1-3	GTDLYF%sA	GTIOC%sA Falling Output Delay Register	0x2C	16	read/ write	0x0000	0xFFFF
	3	0x4	1-3	GTDLYF%sB	GTIOC%sB Falling Output Delay Register	0x2E	16	read/ write	0x0000	0xFFFF
KINT	-	-	-	KRCTL	KEY Return Control Register	0x00	8	read/ write	0x00	0xFF
				KRF	KEY Return Flag Register	0x04	8	read/ write	0x00	0xFF
				KRM	KEY Return Mode Register	0x08	8	read/ write	0x00	0xFF
CTSU	-	-	-	CTSUCR0	CTSU Control Register 0	0x00	8	read/ write	0x00	0xFF
				CTSUCR1	CTSU Control Register 1	0x01	8	read/ write	0x00	0xFF
				CTSUSDPRS	CTSU Synchronous Noise Reduction Setting Register	0x02	8	read/ write	0x00	0xFF
				CTSUSST	CTSU Sensor Stabilization Wait Control Register	0x03	8	read/ write	0x00	0xFF
				CTSUMCH0	CTSU Measurement Channel Register 0	0x04	8	read/ write	0x3F	0xFF
				CTSUMCH1	CTSU Measurement Channel Register 1	0x05	8	read/ write	0x3F	0xFF
				CTSUCHAC0	CTSU Channel Enable Control Register 0	0x06	8	read/ write	0x00	0xFF
				CTSUCHAC1	CTSU Channel Enable Control Register 1	0x07	8	read/ write	0x00	0xFF
				CTSUCHAC2	CTSU Channel Enable Control Register 2	0x08	8	read/ write	0x00	0xFF
				CTSUCHAC3	CTSU Channel Enable Control Register 3	0x09	8	read/ write	0x00	0xFF
				CTSUCHTRC0	CTSU Channel Transmit/Receive Control Register 0	0x0B	8	read/ write	0x00	0xFF
				CTSUCHTRC1	CTSU Channel Transmit/Receive Control Register 1	0x0C	8	read/ write	0x00	0xFF
				CTSUCHTRC2	CTSU Channel Transmit/Receive Control Register 2	0x0D	8	read/ write	0x00	0xFF
				CTSUCHTRC3	CTSU Channel Transmit/Receive Control Register 3	0x0E	8	read/ write	0x00	0xFF

Table 3.4 Register description (24 of 28)

Peripheral name	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
CTSU	-	-	-	CTSUDCLKC	CTSU High-Pass Noise Reduction Control Register	0x10	8	read/ write	0x00	0xFF
				CTSUST	CTSU Status Register	0x11	8	read/ write	0x00	0xFF
				CTSUSSC	CTSU High-Pass Noise Reduction Spectrum Diffusion Control Register	0x12	16	read/ write	0x0000	0xFFFF
				CTSUSO0	CTSU Sensor Offset Register 0	0x14	16	read/ write	0x0000	0xFFFF
				CTSUSO1	CTSU Sensor Offset Register 1	0x16	16	read/ write	0x0000	0xFFFF
				CTSUSC	CTSU Sensor Counter	0x18	16	read-only	0x0000	0xFFFF
				CTSURC	CTSU Reference Counter	0x1A	16	read-only	0x0000	0xFFFF
				CTSUERRS	CTSU Error Status Register	0x1C	16	read-only	0x0000	0xFFFF
AGT0,1	-	-	-	AGT	AGT Counter Register	0x00	16	read/ write	0xFFFF	0xFFFF
				AGTCMA	AGT Compare Match A Register	0x02	16	read/ write	0xFFFF	0xFFFF
				AGTCMB	AGT Compare Match B Register	0x04	16	read/ write	0xFFFF	0xFFFF
				AGTCR	AGT Control Register	0x08	8	read/ write	0x00	0xFF
				AGTMR1	AGT Mode Register 1	0x09	8	read/ write	0x00	0xFF
				AGTMR2	AGT Mode Register 2	0x0A	8	read/ write	0x00	0xFF
				AGTIOC	AGT I/O Control Register	0x0C	8	read/ write	0x00	0xFF
				AGTISR	AGT Event Pin Select Register	0x0D	8	read/ write	0x00	0xFF
				AGTCMSR	AGT Compare Match Function Select Register	0x0E	8	read/ write	0x00	0xFF
				AGTIOSEL	AGT Pin Select Register	0x0F	8	read/ write	0x00	0xFF
ACMPHS0-2	-	-	-	CMPCTL	Comparator Control Register	0x000	8	read/ write	0x00	0xFF
				CMPSEL0	Comparator Input Select Register	0x004	8	read/ write	0x00	0xFF
				CMPSEL1	Comparator Reference Voltage Select Register	0x008	8	read/ write	0x00	0xFF
				CMPMON	Comparator Output Monitor Register	0x00C	8	read-only	0x00	0xFF
				CPIOC	Comparator Output Control Register	0x010	8	read/ write	0x00	0xFF
ACMPLP	-	-	-	COMPMDR	ACMPLP Mode Setting Register	0x00	8	read/ write	0x00	0xFF

Table 3.4 Register description (25 of 28)

Peripheral name	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
ACMPLP	-	-	-	COMPFIR	ACMPLP Filter Control Register	0x01	8	read/ write	0x00	0xFF
				COMPOCR	ACMPLP Output Control Register	0x02	8	read/ write	0x00	0xFF
				COMPSEL0	Comparator Input Select Register	0x04	8	read/ write	0x11	0xFF
				COMPSEL1	Comparator Reference Voltage Select Register	0x05	8	read/ write	0x91	0xFF
OPAMP	-	-	-	AMPMC	Operational Amplifier Mode Control Register	0x08	8	read/ write	0x00	0xFF
				AMPTRM	Operational Amplifier Trigger Mode Control Register	0x09	8	read/ write	0x00	0xFF
				AMPTRS	Operational Amplifier Activation Trigger Select Register	0x0A	8	read/ write	0x00	0xFF
				AMPC	Operational Amplifier Control Register	0x0B	8	read/ write	0x00	0xFF
				AMPMON	Operational Amplifier Monitor Register	0x0C	8	read/ write	0x00	0xFF

Table 3.4 Register description (26 of 28)

Peripheral name	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
DALI	-	-	-	BTVTHR1	DALI Bit Timing Violation Threshold Register 1	0x000	16	read/ write	0x4F00	0xFFFF
				BTVTHR2	DALI Bit Timing Violation Threshold Register 2	0x002	16	read/ write	0x654F	0xFFFF
				BTVTHR3	DALI Bit Timing Violation Threshold Register 3	0x004	16	read/ write	0x009D	0xFFFF
				BTVTHR4	DALI Bit Timing Violation Threshold Register 4	0x006	16	read/ write	0x00D B	0xFFFF
				COLTHR1	DALI Collision Threshold Register 1	0x008	16	read/ write	0x380F	0xFFFF
				COLTHR2	DALI Collision Threshold Register 2	0x00A	16	read/ write	0x443C	0xFFFF
				COLTHR3	DALI Collision Threshold Register 3	0x00C	16	read/ write	0x7148	0xFFFF
				COLTHR4	DALI Collision Threshold Register 4	0x00E	16	read/ write	0x8879	0xFFFF
				COLTHR5	DALI Collision Threshold Register 5	0x010	16	read/ write	0x008E	0xFFFF
				CNFR1	DALI Configuration Register 1	0x012	16	read/ write	0x00FF	0xFFFF
				CNFR2	DALI Configuration Register 2	0x014	16	read/ write	0x0000	0xFFFF
				TXWR1	DALI DTX Width Register 1	0x016	16	read/ write	0x003F	0xFFFF
				TDR1H	DALI Transmit Data Register 1H	0x01E	16	read/ write	0x0000	0xFFFF
				TDR1L	DALI Transmit Data Register 1L	0x020	16	read/ write	0x0000	0xFFFF
				TRSTR1	DALI Transmit Control Register 1	0x022	16	write-only	0x0000	0xFFFF
				CTR1	DALI Control Register 1	0x026	16	read/ write	0x0000	0xFFFF
				TXDCTR1	DALI DTX Control Register 1	0x028	16	read/ write	0x0000	0xFFFF
				RDR1H	DALI Reception Data Register 1H	0x02E	16	read-only	0x0000	0xFFFF
				RDR1L	DALI Reception Data Register 1L	0x030	16	read-only	0x0000	0xFFFF
				STR1	DALI Status Register 1	0x032	16	read-only	0x0000	0xFFFF
				COLR1	DALI Collision Register 1	0x036	16	read-only	0x0800	0xFFFF
				FECR1	DALI Flag Error Clear Register 1	0x03A	16	write-only	0x0000	0xFFFF
				SWRR1	DALI Software Reset Register 1	0x03C	16	write-only	0x0000	0xFFFF

Table 3.4 Register description (27 of 28)

Peripheral name	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
USBFS	-	-	-	SYSCFG	System Configuration Control Register	0x000	16	read/ write	0x0000	0xFFFF
				SYSSTS0	System Configuration Status Register 0	0x004	16	read-only	0x0000	0xFFFF
				DVSTCTR0	Device State Control Register 0	0x008	16	read/ write	0x0000	0xFFFF
				CFIFO	CFIFO Port Register	0x014	16	read/ write	0x0000	0xFFFF
				CFIFOL	CFIFO Port Register L	0x014	8	read/ write	0x00	0xFF
				CFIFOSEL	CFIFO Port Select Register	0x020	16	read/ write	0x0000	0xFFFF
				CFIFOCTR	CFIFO Port Control Register	0x022	16	read/ write	0x0000	0xFFFF
				INTENB0	Interrupt Enable Register 0	0x030	16	read/ write	0x0000	0xFFFF
				BRDYENB	BRDY Interrupt Enable Register	0x036	16	read/ write	0x0000	0xFFFF
				NRDYENB	NRDY Interrupt Enable Register	0x038	16	read/ write	0x0000	0xFFFF
				BEMPENB	BEMP Interrupt Enable Register	0x03A	16	read/ write	0x0000	0xFFFF
				SOFCFG	SOF Output Configuration Register	0x03C	16	read/ write	0x0000	0xFFFF
				INTSTS0	Interrupt Status Register 0	0x040	16	read/ write	0x0000	0xEF6F
				BRDYSTS	BRDY Interrupt Status Register	0x046	16	read/ write	0x0000	0xFFFF
				NRDYSTS	NRDY Interrupt Status Register	0x048	16	read/ write	0x0000	0xFFFF
				BEMPSTS	BEMP Interrupt Status Register	0x04A	16	read/ write	0x0000	0xFFFF

Table 3.4 Register description (28 of 28)

Peripheral name	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
USBFS	-	-	-	FRMNUM	Frame Number Register	0x04C	16	read/ write	0x0000	0xFFFF
				USBREQ	USB Request Type Register	0x054	16	read-only	0x0000	0xFFFF
				USBVAL	USB Request Value Register	0x056	16	read-only	0x0000	0xFFFF
				USBINDX	USB Request Index Register	0x058	16	read-only	0x0000	0xFFFF
				USBLENG	USB Request Length Register	0x05A	16	read-only	0x0000	0xFFFF
				DCPCFG	DCP Configuration Register	0x05C	16	read/ write	0x0000	0xFFFF
				DCPMAXP	DCP Maximum Packet Size Register	0x05E	16	read/ write	0x0040	0xFFFF
				DCPCTR	DCP Control Register	0x060	16	read/ write	0x0040	0xFFFF
				PIPESEL	Pipe Window Select Register	0x064	16	read/ write	0x0000	0xFFFF
				PIPECFG	Pipe Configuration Register	0x068	16	read/ write	0x0000	0xFFFF
				PIPEMAXP	Pipe Maximum Packet Size Register	0x06C	16	read/ write	0x0000	0xFFBF
	2	0x002	4,5	PIPE%sCTR	Pipe %s Control Register	0x076	16	read/ write	0x0000	0xFFFF
	2	0x002	6,7	PIPE%sCTR	Pipe %s Control Register	0x07A	16	read/ write	0x0000	0xFFFF
	2	0x004	4,5	PIPE%sTRE	Pipe %s Transaction Counter Enable Register	0x09C	16	read/ write	0x0000	0xFFFF
	2	0x004	4,5	PIPE%sTRN	Pipe %s Transaction Counter Register	0x09E	16	read/ write	0x0000	0xFFFF
	-	-	-	USBBCCTRL0	BC Control Register 0	0x0B0	16	read/ write	0x0000	0xFFFF
				UCKSEL	USB Clock Selection Register	0x0C4	16	read/ write	0x0000	0xFFFF
				USBMC	USB Module Control Register	0x0CC	16	read/ write	0x0002	0xFFFF
DAC8	3	0x01	0-2	DACS%s	D/A Conversion Value Setting Register %s	0x00	8	read/ write	0x00	0xFF
	-	-	-	DAM	D/A Converter Mode Register	0x03	8	read/ write	0x00	0xFF
				DACPC	D/A SW Charge Pump Control Register	0x07	8	read/ write	0x00	0xFF
TSN	-	-	-	TSCDRH	Temperature Sensor Calibration Data Register H	0x229	8	read-only	0x00	0x00
				TSCDRL	Temperature Sensor Calibration Data Register L	0x228	8	read-only	0x00	0x00

Peripheral name = Name of peripheral
Dim = Number of elements in an array of registers
Dim inc = Address increment between two neighboring registers of a register array in the address map

Dim index = Substring that replaces the %s placeholder in the register name
Register name = Name of register
Description = Register description
Address offset = Address of the register relative to the base address defined by the peripheral of the register
Size = Bit width of the register
Access = Register access rights:

- Read-only: Read access is permitted. Write operations have undefined results.
- Write-only: Write access is permitted. Read operations have undefined results.
- Read/write: Both read and write accesses are permitted. Writes affect the state of the register and reads return a value related to the register.

Reset value = Default reset value of the register
Reset mask = Identifies which register bits have a defined reset value

Revision History	S128 Microcontroller Group User's Manual

Rev.	Date	Chapter	Description
1.00	Mar 10, 2017	—	First release
1.10	Nov 28, 2018	—	Second release
		section 1, Overview	Updated definition of CAC in Table 1.3
			Updated Figure 1.2 and Table 1.14
		section 2, CPU	Updated Table 2.1
			Updated section 2.5.1, Debug Mode Definition
			Updated section 2.8.3.4, Connecting sequence and SWD authentication
		section 5, Resets	Updated Table 5.3 and Note 1.
			Updated Table 5.4
		section 7, Low Voltage Detection (LVD)	Updated Figure 7.4
		section 8, Clock Generation Circuit	Updated Table 8.2
			Updated Figure 8.1
			Updated definition of MOSCSF Flag in section 8.2.8
		section 10, Low Power Modes	Added section 10.9.15, Module-Stop Function for an Unused Circuit
		section 12, Interrupt Controller Unit (ICU)	Added a Note: in section 12.2.6
		section 14, Memory Protection Unit (MPU)	Updated the clearing condition for the ERROR bit in section 14.2.3.6, Stack Pointer Monitor Access Control Register (MSPMPUCTL, PSPMPUCTL)
			Updated section 14.5.2.1
			Updated section 14.6.1.1
		section 15, Data Transfer Controller (DTC)	Updated Figure 15.2
			Updated section 15.6.3
		section 16, Event Link Controller (ELC)	Added section 16.4.4, ELC Delay Time
		section 17, I/O Ports	Updated section 17.2.2 and section 17.2.5
			Updated Table 17.3
			Updated section 17.5.4
		section 18, Key Interrupt Function (KINT)	Updated the column title in Table 18.1
			Updated Figure 18.1
			Updated section 18.2.1 through section 18.2.3
		section 19, Port Output Enable for GPT (POEG)	Updated section 19.3.2
		section 20, General PWM Timer (GPT)	Changed bit 20 to reserved bit in section 20.2.24
			Updated Figure 20.77 through Figure 20.80
			Removed section 20.3.11.4 Rotation direction control
			Updated Table 20.20
			Updated section 20.3.11.7
			Updated Figure 20.81
		section 22, Low Power Asynchronous General Purpose Timer (AGT)	Updated Figure 22.1, Figure 22.7, and Figure 22.8
		section 23, Realtime Clock (RTC)	Updated Figure 23.7
		section 24, Watchdog Timer (WDT)	Updated Figure 24.3 and Figure 24.4
		section 25, Independent Watchdog Timer (IWDT)	Updated Figure 25.1
		section 26, USB 2.0 Full-Speed Module (USBFS)	Changed "single-end" to "single-ended" throughout chapter
			Updated section 26.2.4 through section 26.2.6
			Updated Table 26.9, Table 26.14
			Updated section 26.3.5
			Updated section (1), FIFO Port Selection

Rev.	Date	Chapter	Description
1.10	Nov 28, 2018	section 27, Serial Communications Interface (SCI)	Updated section 27.2.11
			Updated section 27.2.13
			Updated section 27.2.15
			Updated Table 27.15, Table 27.17, and Table 27.18
			Updated section 27.2.19
			Updated description of the IICSDAS[1:0] and IICSCLS[1:0] bits in section 27.2.23
			Updated description of the DCME bit in section 27.2.30
			Changed the TXD pin name to TXDn throughout document
			Updated section 27.3.5
			Updated Figure 27.5, Figure 27.6
			Updated Note 1 in Figure 27.30
			Updated section 27.5.2
			Updated Figure 27.38
			Updated Figure 27.52 and Figure 27.53
			Updated Table 27.25 through Table 27.28
			Updated section 27.2.11
			Updated section 27.13
		section 28, Digital Addressable Lighting Interface (DALI)	Updated Note 2. in section 28.2.6
			Updated Note 2. in section 28, Digital Addressable Lighting Interface (DALI)
			Updated Figure 28.5, Figure 28.6, Figure 28.10, Figure 28.11, Figure 28.14, and Figure 28.15
			Updated Table 28.4
			Updated section 28.5.2
		section 29, I^{2}C Bus Interface (IIC)	Updated section 29.2.1
			Updated Table 29.3
			Updated section 29.2.2
			Updated section 29.2.10
			Updated Table 29.6 through Table 29.8
			Updated Figure 29.26, Figure 29.28, Figure 29.31, Figure 29.36, Figure 29.37, Figure 29.45, Figure 29.48, and Figure 29.50
			Updated section 29.15
		section 30, Controller Area Network (CAN) Module	Updated Figure 30.3 andFigure 30.9
			Updated Table 30.9
		section 31, Serial Peripheral Interface (SPI)	Removed Note 1. from b5 and b7 in section 31.2.4
			Updated Figure 31.29 and Figure 31.30, and Figure 31.40
		section 33, 14-Bit A/D Converter (ADC14)	Updated Table 33.1
			Updated section 33.2.3
			Updated section 33.3.2.4 and section 33.3.2.5
			Updated section 33.3.4.3
			Updated Figure 33.16 through Figure 33.20, and Figure 33.22
			Updated Table 33.10
			Updated Figure 33.24 and Figure 33.25
			Updated section 33.3.9
			Updated the formula for maximum error in absolute accuracy in section 33.8.7
		section 36, Operational Amplifier (OPAMP)	Updated section 36.2.1
			Updated section 36.7
		section 41, SRAM	Added section 41.4.2, Store Buffer of SRAM
		section 42, Flash Memory	Updated Table 42.1 and Table 42.5
			Updated Figure 42.9
			Updated Note 1. in section 42.12.5
		section 46, Electrical Characteristics	Updated Table 46.2 through Table 46.5, Table 46.7 through Table 46.9
			Updated Figure 46.21
			Updated Figure 46.22 and Figure 46.23
			Updated Table 46.22, Table 46.31, Table 46.37
			Updated Figure 46.49 through Figure 46.55
			Updated Table 46.42 through Table 46.48

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1.10	Nov 28, 2018	section 46, Electrical Characteristics	Added Figure 46.62
			Updated Table 46.50
			Updated Figure 46.63
			Updated Note 1. in Table 46.58
		section 3, I/O Registers	Updated Table 3.2 and Table 3.4
1.20	Oct 31, 2024	—	Third release
		Features	Updated for Timers
		section 1, Overview	Updated Table 1.6, Timers
			Added Table 1.12, I/O ports
			Updated Figure 1.2, Part numbering scheme
			Updated Table 1.13, Product list
			Updated Table 1.14, Function comparison
			Updated Figure 1.5, Pin assignment for QFN 48-pin
			Updated Figure 1.8, Pin assignment for QFN 32-pin
		section 2, CPU	Updated section 2.1.3, Operating Frequency
			Updated section 2.6.5.2, Debug Stop Control Register (DBGSTOPCR)
			Updated section 2.8.3.4, Connecting sequence and SWD authentication
		section 6, Option-Setting Memory	Updated section 6.2.1, Option Function Select Register 0 (OFS0)
			Updated Note. in section 6.2.2, Option Function Select Register 1 (OFS1)
			Updated Table 6.2, Specifications for ID code protection
		section 7, Low Voltage Detection (LVD)	Updated Note 1. in section 7.2.3, Voltage Monitor 2 Circuit Control Register 1 (LVD2CR1)
			Updated Table 7.4, Procedure for setting bits related to the voltage monitor 1 interrupt and voltage monitor 1 reset so that voltage monitoring occurs
			Updated Table 7.7, Procedure for setting bits related to voltage monitor 2 interrupt and voltage monitor 2 reset so that voltage monitor stops
		section 8, Clock Generation Circuit	UpdatedTable 8.1, Clock generation circuit specifications for the clock sources
			Updated Figure 8.1, Clock generation circuit block diagram
			Updated section 8.2.4, Sub-Clock Oscillator Control Register (SOSCCR)
			Updated section 8.2.5, Low-Speed On-Chip Oscillator Control Register (LOCOCR)
			Updated section 8.2.6, High-Speed On-Chip Oscillator Control Register (HOCOCR)
			Updated section 8.2.8, Oscillation Stabilization Flag Register (OSCSF)
			Updated Note. in section 8.2.13, Main Clock Oscillator Mode Oscillation Control Register (MOMCR)
			Updated section 8.6.10, SysTick Timer-Dedicated Clock (SYSTICCLK)
		section 10, Low Power Modes	Updated Table 10.2, Operating conditions of each low power mode
			Updated Note 12. in Table 10.2, Operating conditions of each low power mode
			Updated section 10.2.5, Module Stop Control Register D (MSTPCRD)
			Updated section 10.5.1, Setting Operating Power Control Mode
			Updated section 10.6.2, Canceling Sleep Mode
			Updated section 10.7.3, Example of Software Standby Mode Application
			Updated Figure 10.7, Example of Software Standby mode application
			Updated Figure 10.12, Setting example for using SCI0 or the DALI in Snooze mode entry
			Updated section 10.9.1, Register Access
		section 12, Interrupt Controller Unit (ICU)	Updated Figure 12.1, ICU block diagram
			Updated section 12.2.1, IRQ Control Register i (IRQCRi) (i = 0 to 7)
			Updated section 12.2.2, Non-Maskable Interrupt Status Register (NMISR)
			Updated section 12.2.3, Non-Maskable Interrupt Enable Register (NMIER)
			Updated section 12.2.5, NMI Pin Interrupt Control Register (NMICR)
			Updated section 12.2.7, SYS Event Link Setting Register (SELSR0)
			Updated section 12.4.1, Detecting Interrupts
			Updated section 12.4.2.1, CPU interrupt request
			Updated section 12.4.2.2, DTC activation
			Updated section 12.4.4, External Pin Interrupts

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1.20	Oct 31, 2024	section 17, I/O Ports	Updated Table 17.2, I/O port functions
			Updated section 17.2.1, Port Control Register 1 (PCNTR1/PODR/PDR)
			Updated section 17.2.2, Port Control Register 2 (PCNTR2/EIDR/PIDR)
			Updated section 17.2.3, Port Control Register 3 (PCNTR3/PORR/POSR)
			Updated section 17.2.4, Port Control Register 4 (PCNTR4/EORR/EOSR)
			Updated section 17.2.5, Port mn Pin Function Select Register (PmnPFS/PmnPFS_HA/PmnPFS_BY) (m = 0 to 5, 9; n = 00 to 15)
			Updated section 17.3.2, Port Function Select
			Updated Table 17.7, Register settings for I/O pin functions (PORT1) (2)
			Updated Table 17.8, Register settings for I/O pin functions (PORT2)
		section 18, Key Interrupt Function (KINT)	Updated section 18.3.2, When Using Key Interrupt Flag (KRMD = 1)
		section 19, Port Output Enable for GPT (POEG)	Updated section 19.3, Output-Disable Control Operation
			Updated section 19.4, Interrupt Source
			Updated Figure 19.4, External trigger output timing to GPT
		section 20, General PWM Timer (GPT)	Updated Note 1. in Table 20.2, GPT functions
			Updated section 20.2.12, General PWM Timer Control Register (GTCR)
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		section 46, Electrical Characteristics	Added section 46.2.11, Thermal Characteristics
		Appendix 2, Package Dimensions	Added Figure 2.6, QFN 48-pin (2)
			Added Figure 2.8, QFN 32-pin (2)
		Appendix 3, I/O Registers	Updated Table 3.1, Peripheral base address
			Updated Table 3.2, Access cycles for non-GPT modules

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