
**CMOS Single-Chip 8-Bit Microcontroller, Flash Memory 32 KB,
SRAM 1 KB, 12-Bit ADC**

DS Rev. 1.10

Features**Core and Memory**

- 8-bit CISC M8051 core (8051 Compatible, 2-clock per cycle)
- 32 KB On-Chip Flash (ISP)
- 256 bytes IRAM, 768 bytes XRAM

General Purpose I/O (GPIO)

- Normal I/O: 42 Ports
- LED display drive pins: 8 Ports

Timer/Counter

- Basic Interval Timer (BIT) 8-bit × 1-ch
- Watchdog Timer (WDT) 8-bit × 1-ch
- 8-bit × 1-ch (T0)
- 16-bit × 2-ch (T1/T2)
- 8-bit × 2-ch (T3/T4) or 16-bit × 1-ch (T3)

Programmable Pulse Generation

- Pulse generation (by T1/T2)
- 8-bit PWM (by T0)
- 6-ch 10-bit PWM for Motor (by T4)

Buzzer

- 8-bit × 1-ch

Watch Timer (WT)

- 3.91 ms/0.25 s/0.5 s/1 s/1 minute interval at 32.768 kHz

12-bit A/D Converter

- 16 Input channels

16-bit CRC/Checksum Generator

- Auto and User CRC/Checksum mode

8bit SPI x 1 Channel**8bit UART x 1 Channel****8bit USI (UART + SPI + I2C) x 2 Channel**

- 8-bit UART/SPI/I2C x 2 channel

128-Bit Unique ID**Power-On Reset (POR)**

- Reset release level (1.4 V)

Low Voltage Reset

- 14 level detect (1.60 V, 2.00 V,,, 4.40 V)

Low Voltage Indicator

- 13 level detect (2.00 V, 2.10 V,,, 4.40 V)

Interrupt Sources

- External Interrupts (EINT0~7/8/10/11/12) (12)
- Timer 0/1/2/3/4 (6), WDT (1), BIT (1), WT (1)
- USI0/1 (6), SPI 2 (1), UART 2 (2), ADC (1)

Internal High Frequency RC Oscillator

- 16 MHz ±1.0% (T_A=-20 to +70°C, User trim)

Power-Down Mode

- STOP, IDLE mode

Operating Voltage and Frequency

- 2.0 V to 5.5 V (@32 to 38 kHz with SX-tal)
- 2.2 V to 5.5 V (@0.4 to 4.2 MHz with X-tal)
- 2.4 V to 5.5 V (@0.4 to 8.5 MHz with X-tal)
- 1.8 V to 5.5 V (@0.5 to 16 MHz with IRC)
- Voltage dropout converter included for core

Operating Temperature

- -40°C to +105°C

Package Type

- 44-LQFP
- 32-LQFP
- 32-SOP
- 28-SOP
- 28-TSSOP
- 24-QFN
- Pb-free package

Product Selection Table

Table 1. Device Summary

Part Number	Flash	IRAM/XRAM	USI	UART	SPI	Timer	ADC	I/O	Package
MC96F6432PL	32KB	256/768B	2	1	1	5	16 ch	42	44-LQFP
MC96F6332PL	32KB	256/768B	2	1	0	5	12 ch	30	32-LQFP
MC96F6332PD	32KB	256/768B	2	1	0	5	12 ch	30	32-SOP
MC96F6332PM	32KB	256/768B	2	1	0	5	11 ch	26	28-SOP
MC96F6332PR	32KB	256/768B	2	1	0	5	11 ch	26	28-TSSOP
MC96F6232PU	32KB	256/768B	1	1	0	5	8 ch	22	24-QFN

Contents

Features	1
Product Selection Table	2
1. Introduction	8
2. Description	8
2.1 Product Category Definition	8
2.2 Device Overview	9
2.3 Block Diagram	12
2.4 Functional Overview	13
2.4.1 Port Structures	13
2.4.2 Memory Organization	15
2.4.3 Ports	28
2.4.4 Interrupt Controller	31
2.4.5 Clock Generator	37
2.4.6 Basic Interval Timer (BIT)	38
2.4.7 Watchdog Timer (WDT)	39
2.4.8 Watch Timer (WT)	40
2.4.9 TIMER 0	41
2.4.10 TIMER 1	43
2.4.11 TIMER 2	45
2.4.12 TIMER 3 and Timer 4	47
2.4.13 Buzzer	50
2.4.14 12-Bit A/D Converter	51
2.4.15 Serial Peripheral Interface (SPI) 2	53
2.4.16 UART + SPI + I2C (USI 0/1)	54
2.4.17 UART 2	58
2.4.18 Flash CRC and Checksum Generator	60
2.4.19 Power Down Operation	62
2.4.20 Reset	63
2.4.21 Flash Memory	64
2.5 Development Tools	66
2.5.1 Compiler	66
2.5.2 E-OCD II Interface and OCD Debugger	67
2.5.3 Programmer	68
2.5.4 On-Chip Debug System	71
3. Pinouts and Pin Descriptions	76
3.1 Pinouts	76
3.2 Pin Description	81
4. Electrical Characteristics	85
4.1 Absolute Maximum Ratings	85
4.2 Recommended Operating Conditions	85
4.3 ADC Characteristics	86
4.4 Power-On Reset	87
4.5 Low Voltage Reset and Low Voltage Indicator Characteristics	88
4.6 Internal RC Oscillator Characteristics	89
4.7 Internal Watchdog Timer RC Oscillator Characteristics	89
4.8 DC Characteristics	90
4.9 Supply Current Characteristics	91
4.10 AC Characteristics	92

4.11	SPI Characteristics	93
4.12	UART Timing Characteristics	94
4.13	I2C Characteristics	95
4.14	Data Retention Voltage in STOP Mode	96
4.15	Internal Flash Characteristics	97
4.16	Input/output Capacitance Characteristics	97
4.17	Main Oscillator Characteristics	98
4.18	Sub Oscillator Characteristics	99
4.19	Main oscillator Stabilization Characteristics	100
4.20	Sub oscillator Stabilization Characteristics	100
4.21	Operating Voltage Range	101
4.22	Typical Characteristics	102
4.23	Recommended Circuit and Layout	105
4.24	Recommended Circuit and Layout with SMPS Power	106
5.	Package Information	107
5.1	44-LQFP Package Information	108
5.2	32-LQFP Package Information	109
5.3	32-SOP Package Information	110
5.4	28-SOP Package Information	111
5.5	28-TSSOP Package Information	112
5.6	24-QFN Package Information	113
6.	Ordering Information	114
Appendix		115
A.	Configure Option	115
	Register Description: Configure Option Control	115
B.	Instruction Table	116
C.	Flash Protection for Invalid Erase/Write	122
	How to Protect the Flash	122
	Protection Flow Description	123
	Other Protection by the Configure Options	125
Revision History		126

List of Tables

Table 1. Device Summary	2
Table 2. MC96F6432P Series Memory Density	8
Table 3. MC96F6432P Device Features and Peripheral Counts	9
Table 4. Summary of MC96F6432P Peripherals.....	11
Table 5. SFR Map Summary	20
Table 6. XSFR Map Summary	21
Table 7. SFR Map	22
Table 8. XSFR Map	26
Table 9. Interrupt Vector Address Table	36
Table 10. TIMER 0 Operating Modes.....	41
Table 11. TIMER 1 Operating Modes	43
Table 12. TIMER 2 Operating Modes.....	45
Table 13. TIMER 3/4 Operating Modes.....	47
Table 14. Buzzer Frequency at 8 MHz.....	50
Table 15. Peripheral Operation During Power-Down Mode.....	62
Table 16. Reset Value and the Relevant On-Chip Hardware.....	63
Table 17. Specification of E-Gang4 and E-Gang6	69
Table 18. Pins for MTP Programming	69
Table 19. Features of OCD	71
Table 20. Pin Description	81
Table 21. Absolute Maximum Ratings	85
Table 22. Recommended Operating Conditions	85
Table 23. ADC Characteristics	86
Table 24. Power-On Reset Characteristics	87
Table 25. LVR and LVI Characteristics.....	88
Table 26. Internal RC Oscillator Characteristics	89
Table 27. Internal WDTRC Oscillator Characteristics	89
Table 28. DC Characteristics.....	90
Table 29. Supply Current Characteristics.....	91
Table 30. AC Characteristics	92
Table 31. SPI Characteristics	93
Table 32. UART Timing Characteristics	94
Table 33. I2C Characteristics	95
Table 34. Data Retention Voltage in STOP Mode	96
Table 35. Internal Flash Characteristics	97
Table 36. I/O Capacitance Characteristics	97
Table 37. Main Oscillator Characteristics	98
Table 38. Sub Oscillator Characteristics	99
Table 39. Main Oscillator Stabilization Characteristics	100
Table 40. Sub Oscillator Stabilization Characteristics.....	100
Table 41. Instruction Table: Arithmetic.....	116
Table 42. Instruction Table: Logical	117
Table 43. Instruction Table: Data Transfer	118
Table 44. Instruction Table: Boolean	119
Table 45. Instruction Table: Branching	120
Table 46. Instruction Table: Miscellaneous	120
Table 47. Instruction Table: Additional Instructions	120

List of Figures

Figure 1. MC96F6432P Block Diagram	12
Figure 2. General-Purpose I/O Port Structure	13
Figure 3. External Interrupt I/O Port Structure	14
Figure 4. Program Memory	16
Figure 5. Internal Data Memory Map	17
Figure 6. Lower 128 Bytes Internal RAM	18
Figure 7. Extended SFR (XSFR) Area	19
Figure 8. Interrupt Group Priority Level.....	32
Figure 9. External Interrupt Description	33
Figure 10. Interrupt Controller Block Diagram	34
Figure 11. Clock Generator in Block Diagram.....	37
Figure 12. Basic Interval Timer in Block Diagram	38
Figure 13. Watchdog Timer in Block Diagram	39
Figure 14. WT Block Diagram	40
Figure 15. 8-Bit Timer 0 in Block Diagram	42
Figure 16. 16-Bit Timer 1 in Block Diagram	44
Figure 17. 16-Bit Timer 2 in Block Diagram	46
Figure 18. 8-Bit Timer 3/4 in Block Diagram (Two 8-Bit Mode).....	48
Figure 19. 16-Bit Timer 3 in Block Diagram (16-Bit Mode)	49
Figure 20. Buzzer Driver Block Diagram.....	50
Figure 21. 12-Bit ADC Block Diagram.....	52
Figure 22. AD Analog Input Pin with Capacitor	52
Figure 23. AD Power (AVREF) Pin with Capacitor.....	52
Figure 24. SPI 2 Block Diagram.....	53
Figure 25. UART Block Diagram (Where n = 0 and 1)	55
Figure 26. SPI Block Diagram (Where n = 0 and 1)	56
Figure 27. I2C Block Diagram (Where n = 0 and 1).....	57
Figure 28. UART 2 Block Diagram (where n = 2)	59
Figure 29. CRC-16 Polynomial Structure.....	60
Figure 30. Flash CRC/Checksum Generator Block Diagram	61
Figure 31. Reset Block Diagram	63
Figure 32. Flash Program ROM Structure	65
Figure 33. E-OCD II and OCD Pin Descriptions	67
Figure 34. E-PGM+ (Single Writer) and Pin Descriptions	68
Figure 35. E-Gang4 and E-Gang6 (for Mass Production)	69
Figure 36. PCB Design Guide for On-Board Programming	70
Figure 37. On-Chip Debugging System in Block Diagram.....	71
Figure 38. 10-Bit Transmission Packet	72
Figure 39. Data Transfer on Twin Bus	73
Figure 40. Bit Transfer on Serial Bus	73
Figure 41. Start and Stop Condition.....	73
Figure 42. Acknowledge on Serial Bus	74
Figure 43. Clock Synchronization During Wait Procedure.....	74
Figure 44. Connection of Transmission	75
Figure 45. MC96F6432PL 44-LQFP Pinouts	76
Figure 46. MC96F6332PL 32-LQFP Pinouts	77
Figure 47. MC96F6332PD 32-SOP Pinouts	78

Figure 48. MC96F6332PM 28-SOP Pinouts	79
Figure 49. MC96F6332PR 28-TSSOP Pinouts	79
Figure 50. MC96F6232PU 24-QFN Pinouts	80
Figure 51. Power-On Reset Timing	87
Figure 52. AC Timing	92
Figure 53. SPI Timing	93
Figure 54. UART Timing Characteristics	94
Figure 55. Timing Waveform of UART Module	94
Figure 56. I2C Timing	95
Figure 57. STOP Mode Release Timing When Initiated by Interrupts	96
Figure 58. STOP Mode Release Timing When Initiated by RESETB	96
Figure 59. Crystal/Ceramic Oscillator	98
Figure 60. External Clock	98
Figure 61. Crystal Oscillator	99
Figure 62. External Clock	99
Figure 63. Clock Timing Measurement at XIN	100
Figure 64. Clock Timing Measurement at SXIN	100
Figure 65. Operating Voltage Range	101
Figure 66. Operating Voltage Range (Sub OSC)	101
Figure 67. MAIN RUN (IDD1) Current	102
Figure 68. MAIN IDLE (IDD2) Current	103
Figure 69. SUB RUN (IDD3) Current	103
Figure 70. SUB IDLE (IDD4) Current	104
Figure 71. STOP (IDD5) Current	104
Figure 72. Recommended Circuit and Layout	105
Figure 73. Recommended Circuit and Layout with SMPS Power	106
Figure 74. 44-LQFP Package Outline	108
Figure 75. 32-LQFP Package Outline	109
Figure 76. 32-SOP Package Outline	110
Figure 77. 28-SOP Package Outline	111
Figure 78. 28-TSSOP Package Outline	112
Figure 79. 24-QFN Package Outline	113
Figure 80. MC96F6x32P Device Numbering Nomenclature	114
Figure 81. Flash Protection Against Abnormal Operations	122
Figure 82. Flowchart of Flash Protection	124

1. Introduction

This document provides an overview of the features supported by the device, including high-level information and brief explanations for each feature.

Refer to Table 3 for the list of features supported by the device.

2. Description

The MC96F6432P is an advanced CMOS 8-bit microcontroller with 32 KB of Flash. This is a powerful microcontroller which provides a highly flexible and cost-effective solution to many embedded control applications.

The MC96F6432P provides the following features : 32 KB of Flash, 256 bytes of IROM, 768 bytes of XRAM, general purpose I/O, Basic Interval Timer, Watchdog Timer, 8/16-bit timer/counter, 16-bit PPG output, 8-bit PWM output, 10-bit PWM output, Watch Timer, buzzer driving port, SPI, UART, USI, 16-bit CRC/Checksum generator, 12-bit A/D Converter, on-chip POR, LVR, LVI, on-chip oscillator and clock circuitry. The MC96F6432P also supports power saving modes to reduce power consumption.

The following sections describe the features and peripheral counts of the MC96F6432P in Table 2, Table 3, and Table 4.

2.1 Product Category Definition

Table 2 provides an overview of the memory capacity for the MC96F6432P.

See Table 3 in the next section for a list of features supported by the MC96F6432P.

Table 2. MC96F6432P Series Memory Density

Memory Density		Category
Flash	RAM	
32 KB	1024 Bytes	MC96F6432P

2.2 Device Overview

Table 3. MC96F6432P Device Features and Peripheral Counts

Peripheral		MC96F6432P
CPU		8-bit CISC core (M8051, 2 clocks per cycle)
Flash		• 32 KB with self r/w capability • On-chip debug and ISP • Endurance: 10,000 (Sector 0~507) - 100,000 times (Sector 508~511)
IRAM		256 bytes
XRAM		768 bytes
GPIO		• Normal I/O • 42 ports: P0[7:0], P1[7:0], P2[7:0], P3[7:0], P4[3:0], P5[5:0] • LED display drive pins: P1[1:0], P2[1:0], P3[3:0]
Timer/ counter		• BIT 8-bit x 1-ch • WDT 8-bit x 1-ch: 5 kHz internal RC oscillator for WDT • 8-bit x 1-ch (T0) • 16-bit x 2-ch (T1/T2) • 8-bit x 2-ch (T3/T4) or 16-bit x 1-ch (T3) • Watch Timer (WT)
BUZZER		8-bit x 1-ch
Programmable pulse generation		• Pulse generation (by T1/T2) • 8-Bit PWM (by T0) • 6-ch 10-Bit PWM for Motor (by T4)
ADC		12-bit ADC, 16 input channels
CRC and checksum generator		• 16-bit • Auto and user CRC/ checksum modes
Reset	Power on reset	Reset release level (1.4 V)
	Low voltage reset	14 Level detect (1.60 V, 2.00 V, ..., 4.4 V)
Low voltage indicator		13 Level detect (2.00 V, 2.10 V, ..., 4.4 V)
Seral interface		1 UART, 1 SPI, 2 USI (UART + SPI + I2C)
Power consumption		Stop and Idle modes
Internal RC oscillator		16MHz $\pm$ 1.0% (T_A = -20°C to +70°C, User trim)
Operating voltage and frequency		• 2.0 to 5.5 V @ 32 to 38 kHz with SX-tal • 2.2 to 5.5 V @ 0.4 to 4.2 MHz with X-tal • 2.4 to 5.5 V @ 0.4 to 8.5 MHz with X-tal • 1.8 to 5.5 V @ 0.5 to 16 MHz with IRC • Voltage dropout converter included for core

Table 3. MC96F6432P Device Features and Peripheral Counts (continued)

Peripheral	MC96F6432P
Minimum instruction execution time	• 0.125 μs @ 16 MHz IRC • 0.235 μs @ 8.5 MHz main clock • 61 μs @ 32.768 kHz sub clock
Operating temperature	-40 to +105°C
Package type	• 44-LQFP • 32-LQFP • 32-SOP • 28-SOP • 28-TSSOP • 24-QFN 04x04 • Pb-free package

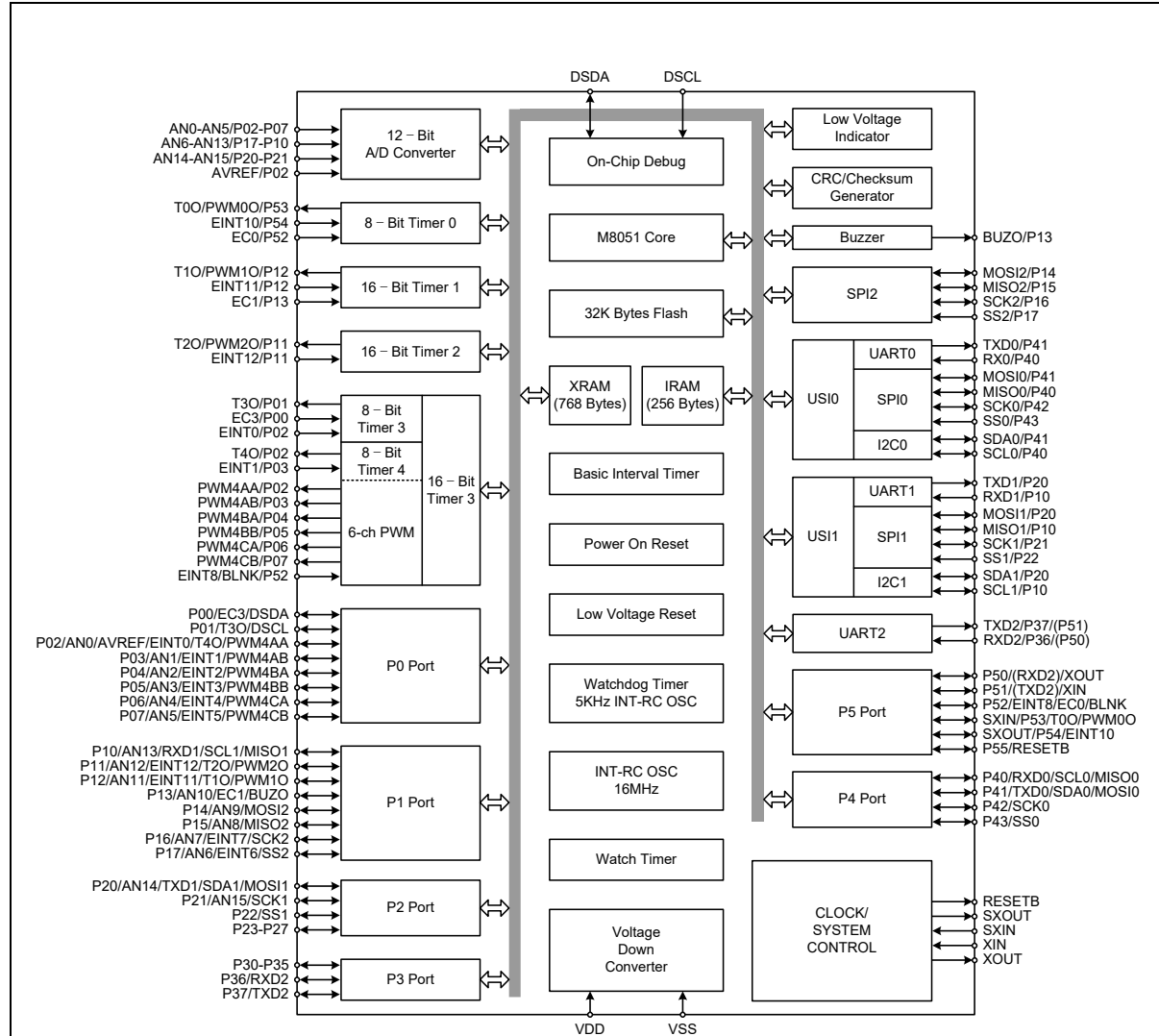
Table 4. Summary of MC96F6432P Peripherals

Peripheral		MC96F6432PL	MC96F6332PL MC96F6332PD	MC96F6332PM MC96F6332PR	MC96F6232PU
Code Flash memory		32 KB	32 KB	32 KB	32 KB
IRAM/XRAM		256/768 bytes	256/768 bytes	256/768 bytes	256/768 bytes
Timers	General purpose	2 (16-bit), 1 (8-bit), 1 (16-bit) or 2 (8-bit)			
	WDT	1			
	BIT	1			
Communication interfaces	SPI	1	0	0	0
	UART	1	1	1	1
	USI	2	2	2	1
WT		1			
BUZZER		1			
GPIO		42	30	26	22
ADCs Number of channels		50 ksp/s	50 ksp/s	50 ksp/s	50 ksp/s
		16	12	11	8
Max. CPU frequency		16 MHz			
128-bit Unique ID		1			
CRC/Checksum		1 (16-bit)			
Operating voltage		1.8 V to 5.5 V			
Operating temperature		Ambient operating temperature: -40°C to 105°C			
Packages		44-LQFP	32-LQFP 32-SOP	28-SOP 28-TSSOP	24-QFN

2.3 Block Diagram

Figure 1 describes MC96F6432P in a block diagram.

Figure 1. MC96F6432P Block Diagram



NOTES:

1. The P14-P17, P23-P25, P34-P37, and P43 are not in the 32-Pin package.
2. The P13-P17, P22-P27, P34-P37, and P43 are not in the 28-Pin package.
3. The P05-P07, P14-P17, P20, P22-P27, P34-P37, and P42-P43 are not in the 24-Pin package.

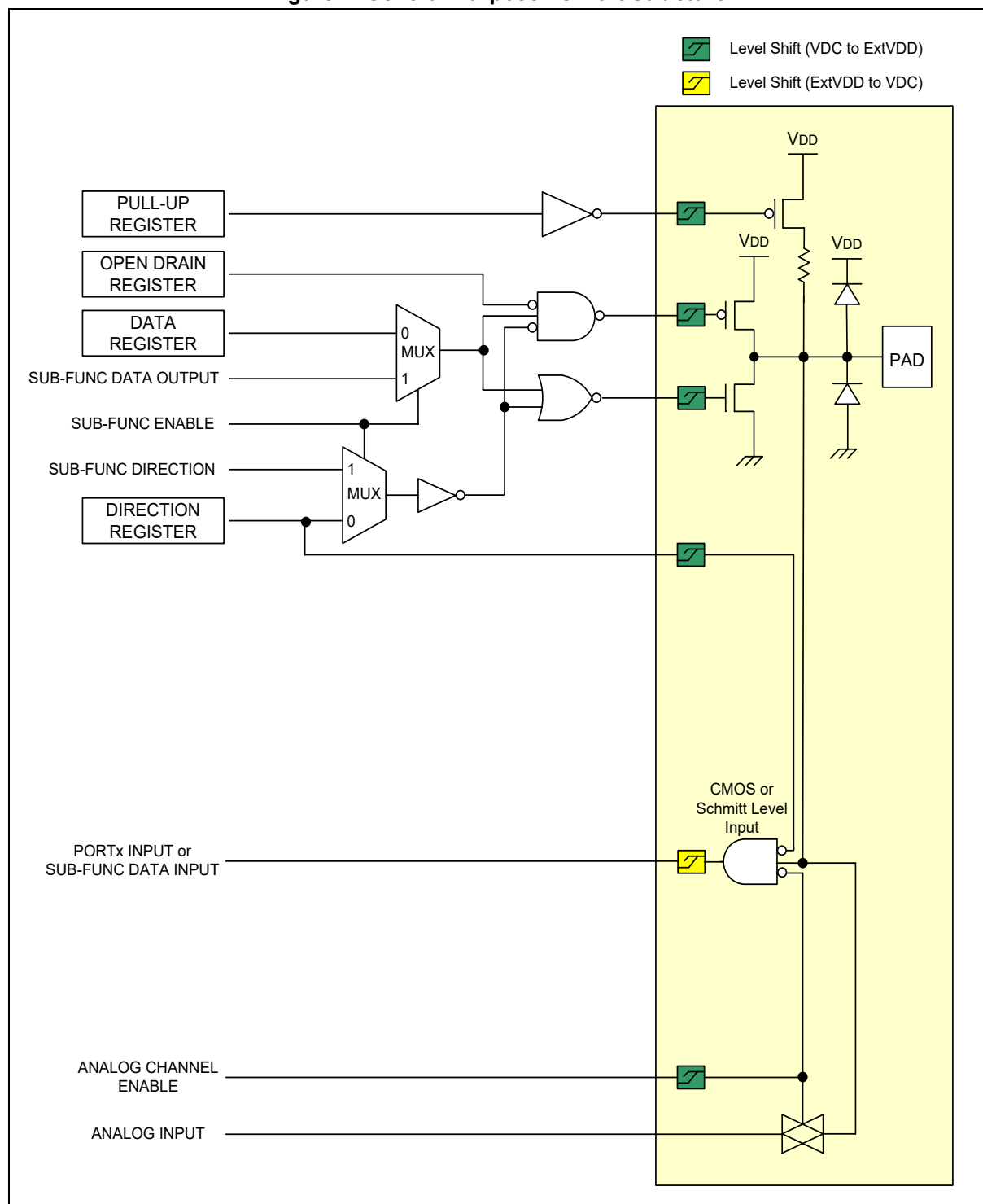
2.4 Functional Overview

The following sections provide an overview of the features of the MC96F6432P microcontroller.

2.4.1 Port Structures

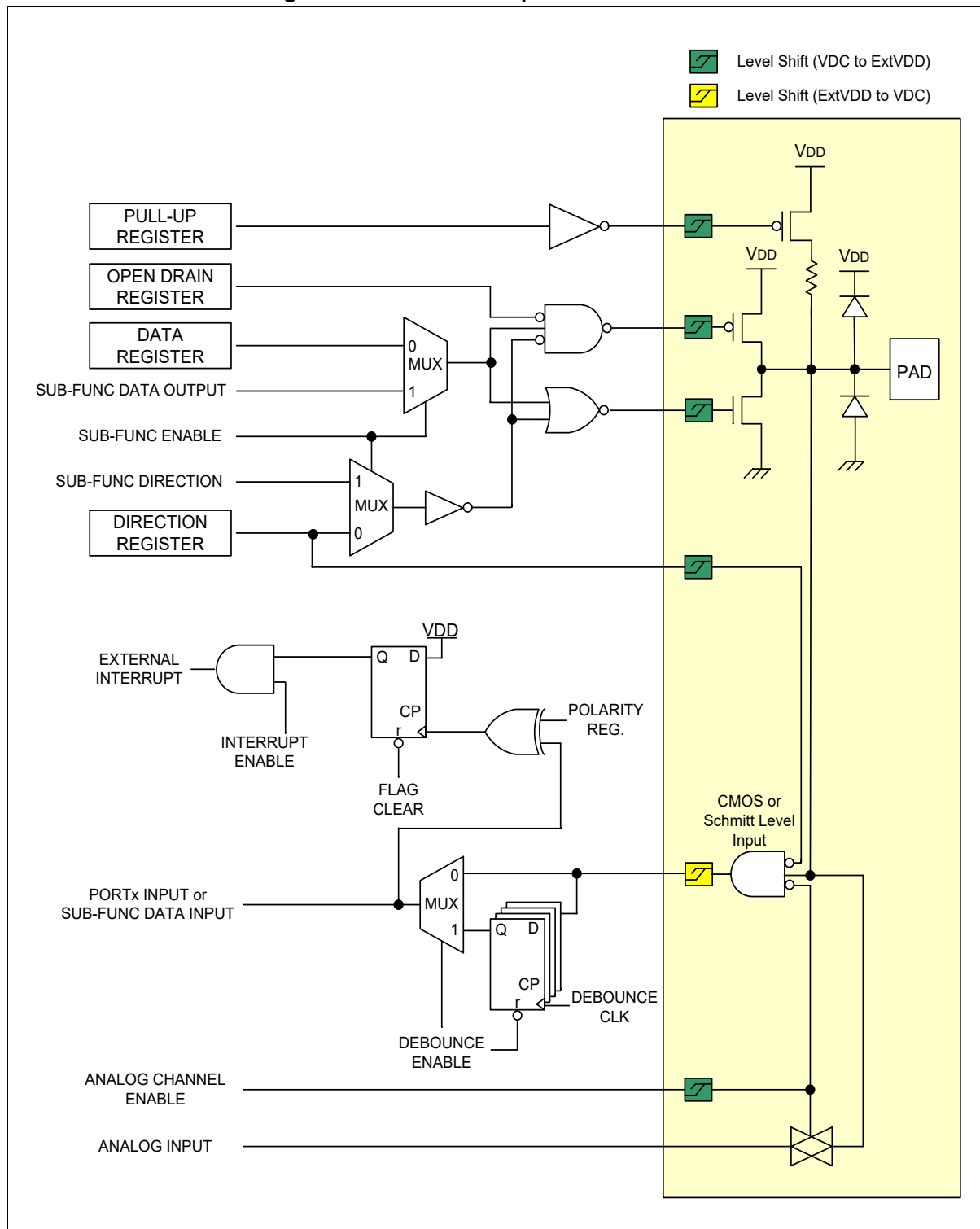
2.4.1.1 GPIO Port Structure

Figure 2. General-Purpose I/O Port Structure



2.4.1.2 External Interrupt I/O Port Structure

Figure 3. External Interrupt I/O Port Structure



2.4.2 Memory Organization

MC96F6432P addresses four separate memory spaces:

- Program memory
- Flash user memory
- Data memory
- XRAM memory

By means of this logical separation of the memory, 8-bit CPU address can access the data memory more rapidly. 16-bit data memory address is generated through the DPTR register.

MC96F6432P provides on-chip 32 KB of the ISP type Flash program memory, which is readable and writable. Internal data memory (IRAM) is 256 bytes, and it includes the stack area. External data memory (XRAM) is 768 bytes.

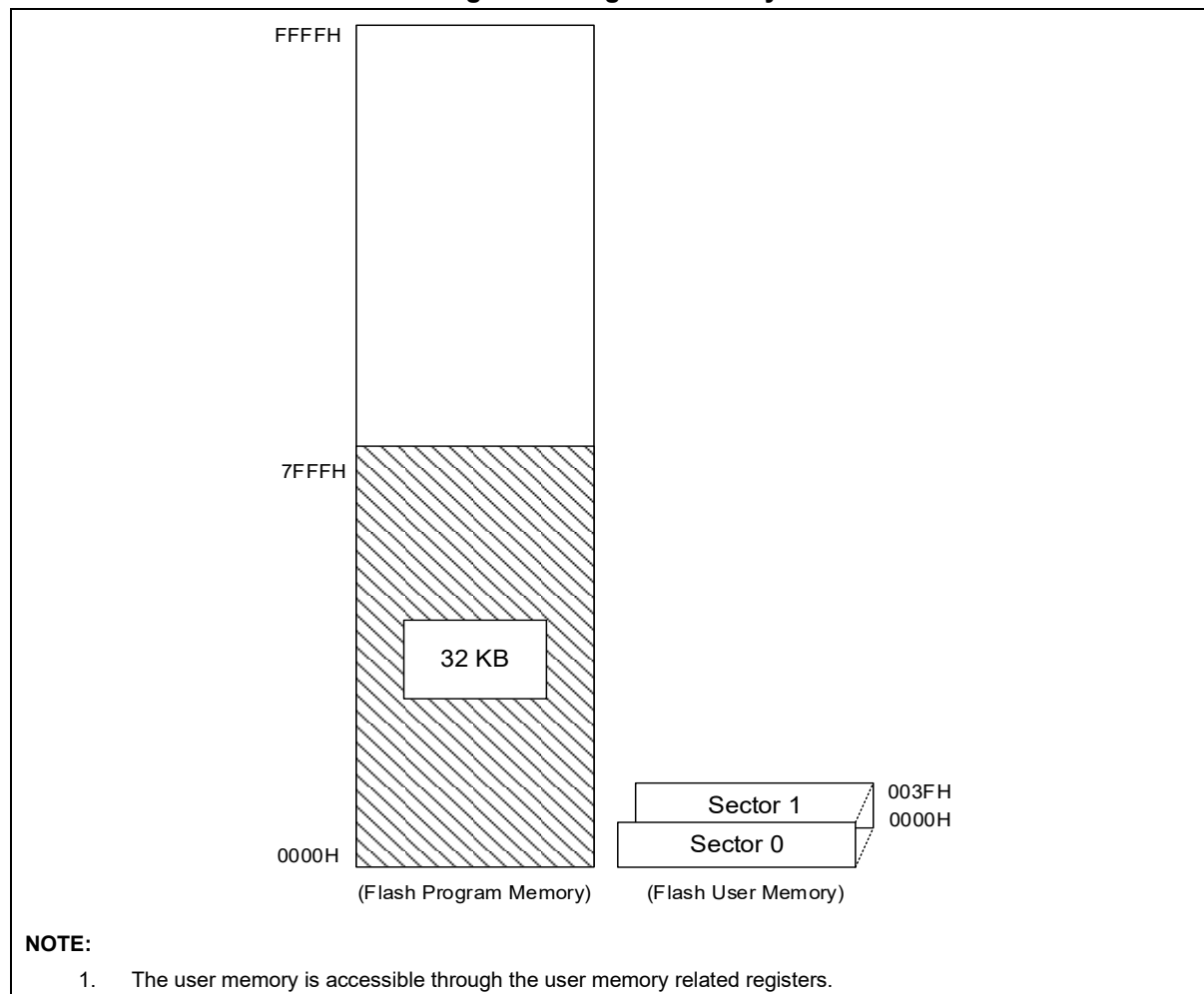
2.4.2.1 Program Memory

A 16-bit program counter is capable of addressing up to 64 KB, but MC96F6432P has only 32 KB program memory space. After reset, CPU begins execution from location 0000H. Each interrupt is assigned to a fixed location of the program memory. The interrupt causes the CPU to jump to that location, where it commences an execution of a service routine.

For example, an external interrupt 11 is assigned to location 000BH. If the external interrupt 11 is going to be used, its service routine must begin at location 000BH. If the interrupt is not going to be used, its service location is available as general purpose program memory. If an interrupt service routine is short enough (frequent cases with a control application), the service routine can reside entirely within an 8-byte interval.

A longer service routine can use a jump instruction to skip over subsequent interrupt locations, if other interrupts are in use. Figure 4 shows a map of the lower part of the program memory.

Figure 4. Program Memory



A more detailed description of program memory is described in Chapter 2.4.21. Flash Memory.

2.4.2.2 Flash User Memory

Flash user memory has 128 bytes memory space. This memory is accessible through the user memory related registers.

2.4.2.3 Internal Data Memory

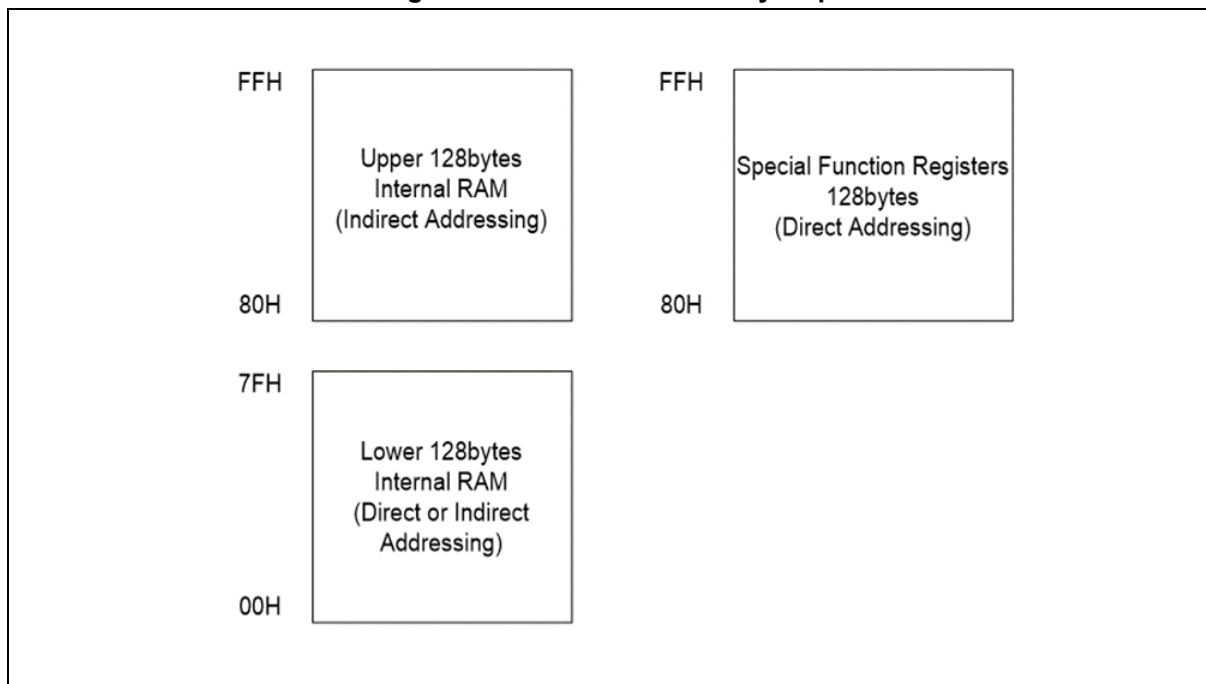
Internal data memory is divided into three spaces as shown in Figure 5. Those three spaces are generally called as,

- Lower 128 bytes
- Upper 128 bytes
- Special Function Registers (SFR space)

Internal data memory addresses are always one byte wide, which implies an address space of 256 bytes.

In fact, the addressing modes of the internal data memory can accommodate up to 384 bytes by using a simple trick. Direct addresses higher than 7FH access one memory space and indirect addresses higher than 7FH access a different memory space. By means of this method, the upper 128 bytes and SFR space can occupy the same block of addresses, 80H through FFH, although they are physically separate entities as shown in Figure 5.

Figure 5. Internal Data Memory Map

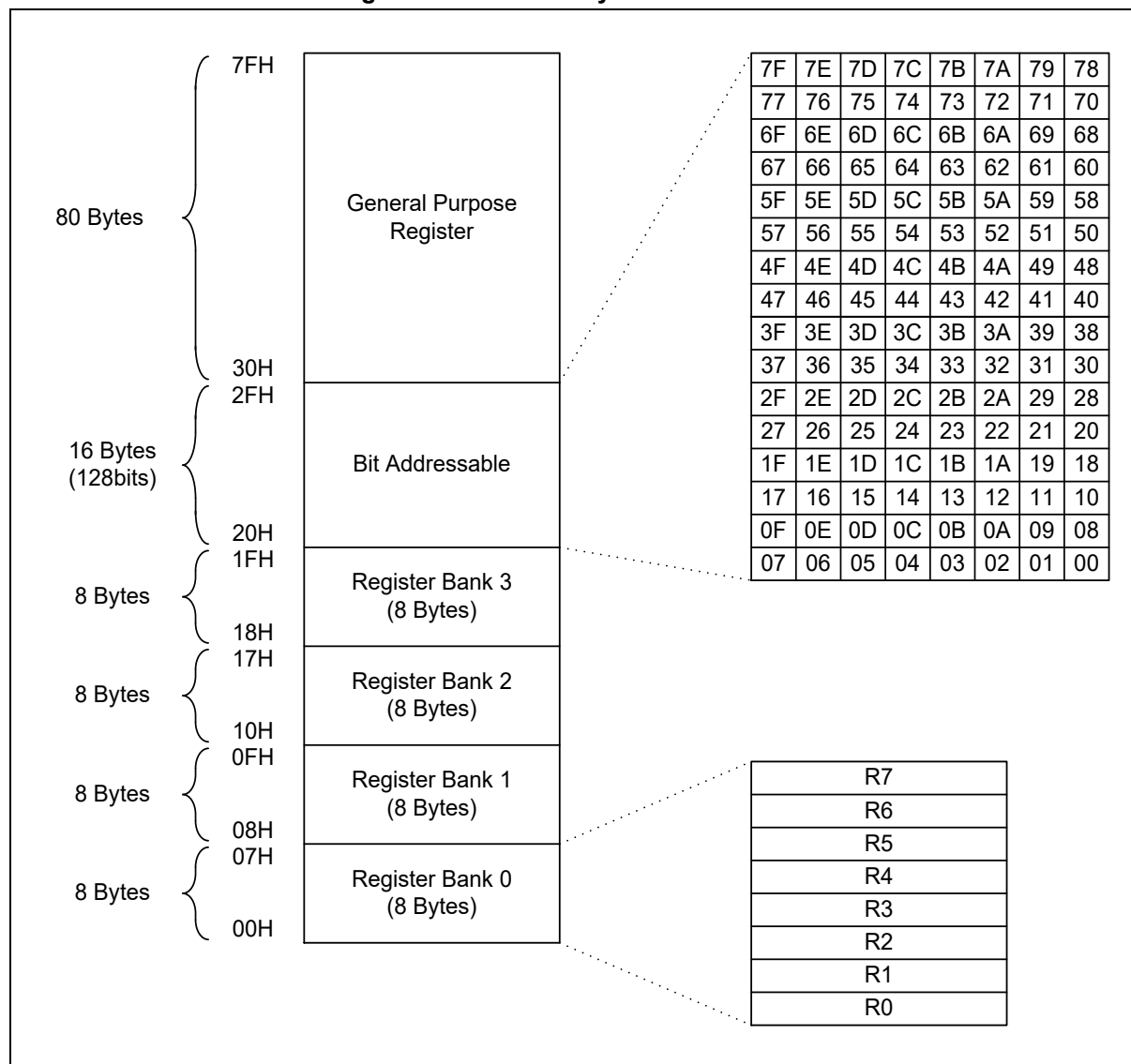


The lower 128 bytes of RAM are present in all 8051 devices as mapped in Figure 6. The lowest 32 bytes are grouped into 4 banks of 8 registers. Program instructions call out these registers as R0 through R7. Two bits in the Program Status Word select which register bank is in use. This allows more efficient use of code space, since register instructions are shorter than instructions that use direct addressing.

The next 16 bytes above the register banks form a block of bit-addressable memory space. The 8051-instruction set includes a wide selection of single-bit instructions, and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00H through 7FH.

Entire bytes in the lower 128 bytes can be accessed by either direct or indirect addressing, while the upper 128 bytes RAM can only be accessed by indirect addressing. These spaces are used for data RAM and stack.

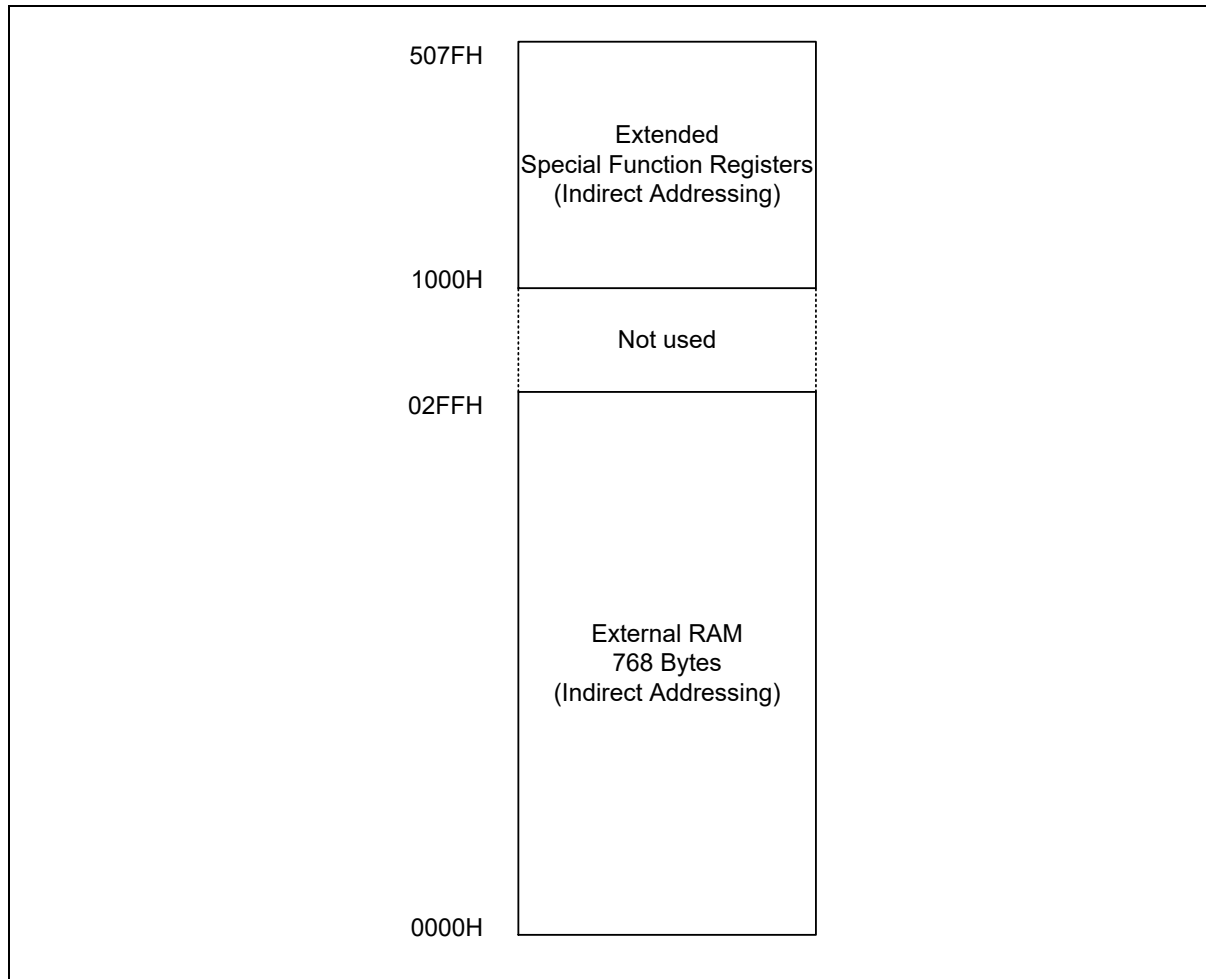
Figure 6. Lower 128 Bytes Internal RAM



2.4.2.4 Extended SFR and Data Memory Area

MC96F6432P has 768 bytes XRAM and XSFR registers. Extended SFR area has no relation to RAM or Flash. This area can be read or written to by using SFR in 8-bit unit.

Figure 7. Extended SFR (XSFR) Area



2.4.2.5 SFR Map

In this section, information of SFR map and map summaries are described through Table 5, Table 6, Table 7, and Table 8.

SFR Map Summary

Table 5. SFR Map Summary

	00H/08H ^{NOTE}	01H/09H	02H/0AH	03H/0BH	04H/0CH	05H/0DH	06H/0EH	07H/0FH
0F8H	IP1	–	FSADRH	FSADRM	FSADRL	FIDR	FMCR	P5FSR
0F0H	B	USI1ST1	USI1ST2	USI1BD	USI1SDHR	USI1DR	USI1SCLR	USI1SCHR
0E8H	RSTFR	USI1CR1	USI1CR2	USI1CR3	USI1CR4	USI1SAR	P3FSR	P4FSR
0E0H	ACC	USI0ST1	USI0ST2	USI0BD	USI0SDHR	USI0DR	USI0SCLR	USI0SCHR
0D8H	LVRCR	USI0CR1	USI0CR2	USI0CR3	USI0CR4	USI0SAR	P0DB	P15DB
0D0H	PSW	P5IO	P0FSRL	P0FSRH	P1FSRL	P1FSRH	P2FSRL	–
0C8H	OSCCR	P4IO	UART2CR1	UART2CR2	UART2CR3	UART2ST	UART2BD	UART2DR
0C0H	EIFLAG0	P3IO	T2CRL	T2CRH	T2ADRL	T2ADRH	T2BDRL	T2BDRH
0B8H	IP	P2IO	T1CRL	T1CRH	T1ADRL	T1ADRH	T1BDRL	T1BDRH
0B0H	P5	P1IO	T0CR	T0CNT	T0DR/ T0CDR	SPICR	SPIDR	SPISR
0A8H	IE	IE1	IE2	IE3	P0PU	P1PU	P2PU	P3PU
0A0H	P4	P0IO	EO	P4PU	EIPOL0L	EIPOL0H	EIFLAG1	EIPOL1
98H	P3	FCDIN	–	–	ADCCRL	ADCCRH	ADCDRL	ADCDRH
90H	P2	P0OD	P1OD	P2OD	P4OD	P5PU	WTCR	BUZCR
88H	P1	WTDR/ WTCNT	SCCR	BITCR	BITCNT	WDTCR	WDTR/ WDCNT	BUZDR
80H	P0	SP	DPL	DPH	DPL1	DPH1	LVICR	PCON

– Reserved

■ M8051 compatible

NOTE:

1. Registers 00H/08H are bit-addressable except OSCCR.

Extended SFR Map Summary**Table 6. XSFR Map Summary**

	00H/8H	01H/9H	02H/0AH	03H/0BH	04H/0CH	05H/0DH	06H/0EH	07H/0FH
5060H	–	–	–	–	–	–	–	–
5058H	FCDRL	–	–	–	–	–	–	–
5050H	FCSARH	FCEARH	FCSARM	FCEARM	FCSARL	FCEARL	FCCR	FCDRH
.....	–	–	–	–	–	–	–	–
5040H	USERMCR	USERMSSR	USERMIDR	–	–	–	–	–
.....	–	–	–	–	–	–	–	–
1068H	UNIQUEID8	UNIQUEID9	UNIQUEID10	UNIQUEID11	UNIQUEID12	UNIQUEID13	UNIQUEID14	UNIQUEID15
1060H	UNIQUEID0	UNIQUEID1	UNIQUEID2	UNIQUEID3	UNIQUEID4	UNIQUEID5	UNIQUEID6	UNIQUEID7
.....	–	–	–	–	–	–	–	–
1038H	XTFLSR	LDDRVSR	–	–	–	–	–	–
1030H	–	–	–	–	–	–	–	–
1028H	–	–	–	–	–	–	–	–
1020H	–	–	–	–	–	–	T2CAPL	T2CAPH
1018H	–	–	–	–	–	–	T1CAPL	T1CAPH
1010H	T4DLYA	T4DLYB	T4DLYC	T4DR	T4CAPR	T4CNT	–	–
1008H	T4PPRL	T4PPRH	T4ADRL	T4ADRH	T4BDRL	T4BDRH	T4CDRL	T4CDRH
1000H	T3CR	T3CNT/ T3DR/ T3CAPR	T4CR	T4PCR1	T4PCR2	T4PCR3	T4ISR	T4IMSK

 Reserved

SFR Map**Table 7. SFR Map**

Address	Function	Symbol	R/W	@ Reset							
				7	6	5	4	3	2	1	0
80H	P0 Data Register	P0	R/W	0	0	0	0	0	0	0	0
81H	Stack Pointer	SP	R/W	0	0	0	0	0	1	1	1
82H	Data Pointer Register Low	DPL	R/W	0	0	0	0	0	0	0	0
83H	Data Pointer Register High	DPH	R/W	0	0	0	0	0	0	0	0
84H	Data Pointer Register Low 1	DPL1	R/W	0	0	0	0	0	0	0	0
85H	Data Pointer Register High 1	DPH1	R/W	0	0	0	0	0	0	0	0
86H	Low Voltage Indicator Control Register	LVICR	R/W	–	–	0	0	0	0	0	0
87H	Power Control Register	PCON	R/W	–	–	–	–	–	–	0	0
88H	P1 Data Register	P1	R/W	0	0	0	0	0	0	0	0
89H	Watch Timer Data Register	WTDR	W	0	1	1	1	1	1	1	1
89H	Watch Timer Counter Register	WTCNT	R	–	0	0	0	0	0	0	0
8AH	System and Clock Control Register	SCCR	R/W	–	–	–	–	–	–	0	0
8BH	BIT Control Register	BITCR	R/W	0	0	0	–	0	0	0	1
8CH	Basic Interval Timer Counter Register	BITCNT	R	0	0	0	0	0	0	0	0
8DH	Watchdog Timer Control Register	WDTCR	R/W	0	0	0	–	–	–	0	0
8EH	Watchdog Timer Data Register	WTDTR	W	1	1	1	1	1	1	1	1
8EH	Watchdog Timer Counter Register	WDTCNT	R	0	0	0	0	0	0	0	0
8FH	BUZZER Data Register	BUZDR	R/W	1	1	1	1	1	1	1	1
90H	P2 Data Register	P2	R/W	0	0	0	0	0	0	0	0
91H	P0 Open-drain Selection Register	P0OD	R/W	0	0	0	0	0	0	0	0
92H	P1 Open-drain Selection Register	P1OD	R/W	0	0	0	0	0	0	0	0
93H	P2 Open-drain Selection Register	P2OD	R/W	0	0	0	0	0	0	0	0
94H	P4 Open-drain Selection Register	P4OD	R/W	–	–	–	–	0	0	0	0
95H	P5 Pull-up Resistor Selection Register	P5PU	R/W	–	–	0	0	0	0	0	0
96H	Watch Timer Control Register	WTCR	R/W	0	–	–	0	0	0	0	0
97H	BUZZER Control Register	BUZCR	R/W	–	–	–	–	–	0	0	0
98H	P3 Data Register	P3	R/W	0	0	0	0	0	0	0	0
99H	Flash CRC Data In Register	FCDIN	R/W	0	0	0	0	0	0	0	0
9AH	Reserved	–	–	–	–	–	–	–	–	–	–
9BH	Reserved	–	–	–	–	–	–	–	–	–	–
9CH	A/D Converter Control Low Register	ADCCRL	R/W	0	0	0	0	0	0	0	0
9DH	A/D Converter Control High Register	ADCCRH	R/W	0	–	0	0	0	0	0	0
9EH	A/D Converter Data Low Register	ADCDRL	R	x	x	x	x	x	x	x	x
9FH	A/D Converter Data High Register	ADCDRH	R	x	x	x	x	x	x	x	x

Table 7. SFR Map (continued)

Address	Function	Symbol	R/W	@ Reset							
				7	6	5	4	3	2	1	0
A0H	P4 Data Register	P4	R/W	–	–	–	–	0	0	0	0
A1H	P0 Direction Register	P0IO	R/W	0	0	0	0	0	0	0	0
A2H	Extended Operation Register	EO	R/W	–	–	–	0	–	0	0	0
A3H	P4 Pull-up Resistor Selection Register	P4PU	R/W	–	–	–	–	0	0	0	0
A4H	External Interrupt Polarity 0 Low Register	EIPOL0L	R/W	0	0	0	0	0	0	0	0
A5H	External Interrupt Polarity 0 High Register	EIPOL0H	R/W	0	0	0	0	0	0	0	0
A6H	External Interrupt Flag 1 Register	EIFLAG1	R/W	0	0	0	0	0	0	0	0
A7H	External Interrupt Polarity 1 Register	EIPOL1	R/W	0	0	0	0	0	0	0	0
A8H	Interrupt Enable Register	IE	R/W	0	–	0	0	0	0	0	0
A9H	Interrupt Enable Register 1	IE1	R/W	–	–	0	0	0	0	0	0
AAH	Interrupt Enable Register 2	IE2	R/W	–	–	0	0	0	0	0	0
ABH	Interrupt Enable Register 3	IE3	R/W	–	–	0	0	0	0	0	0
ACH	P0 Pull-up Resistor Selection Register	P0PU	R/W	0	0	0	0	0	0	0	0
ADH	P1 Pull-up Resistor Selection Register	P1PU	R/W	0	0	0	0	0	0	0	0
AEH	P2 Pull-up Resistor Selection Register	P2PU	R/W	0	0	0	0	0	0	0	0
AFH	P3 Pull-up Resistor Selection Register	P3PU	R/W	0	0	0	0	0	0	0	0
B0H	P5 Data Register	P5	R/W	–	–	0	0	0	0	0	0
B1H	P1 Direction Register	P1IO	R/W	0	0	0	0	0	0	0	0
B2H	Timer 0 Control Register	T0CR	R/W	0	–	0	0	0	0	0	0
B3H	Timer 0 Counter Register	T0CNT	R	0	0	0	0	0	0	0	0
B4H	Timer 0 Data Register	T0DR	R/W	1	1	1	1	1	1	1	1
B4H	Timer 0 Capture Data Register	T0CDR	R	0	0	0	0	0	0	0	0
B5H	SPI 2 Control Register	SPICR	R/W	0	0	0	0	0	0	0	0
B6H	SPI 2 Data Register	SPIDR	R/W	0	0	0	0	0	0	0	0
B7H	SPI 2 Status Register	SPISR	R/W	0	0	0	–	0	0	–	–
B8H	Interrupt Priority Register	IP	R/W	–	–	0	0	0	0	0	0
B9H	P2 Direction Register	P2IO	R/W	0	0	0	0	0	0	0	0
BAH	Timer 1 Control Low Register	T1CRL	R/W	0	0	0	0	–	0	0	0
BBH	Timer 1 Control High Register	T1CRH	R/W	0	–	0	0	–	–	–	0
BCH	Timer 1 A Data Low Register	T1ADRL	R/W	1	1	1	1	1	1	1	1
BDH	Timer 1 A Data High Register	T1ADRH	R/W	1	1	1	1	1	1	1	1
BEH	Timer 1 B Data Low Register	T1BDRL	R/W	1	1	1	1	1	1	1	1
BFH	Timer 1 B Data High Register	T1BDRH	R/W	1	1	1	1	1	1	1	1

Table 7. SFR Map (continued)

Address	Function	Symbol	R/W	@ Reset							
				7	6	5	4	3	2	1	0
C0H	External Interrupt Flag 0 Register	EIFLAG0	R/W	0	0	0	0	0	0	0	0
C1H	P3 Direction Register	P3IO	R/W	0	0	0	0	0	0	0	0
C2H	Timer 2 Control Low Register	T2CRL	R/W	0	0	0	0	–	0	–	0
C3H	Timer 2 Control High Register	T2CRH	R/W	0	–	0	0	–	–	–	0
C4H	Timer 2 A Data Low Register	T2ADRL	R/W	1	1	1	1	1	1	1	1
C5H	Timer 2 A Data High Register	T2ADRH	R/W	1	1	1	1	1	1	1	1
C6H	Timer 2 B Data Low Register	T2BDRL	R/W	1	1	1	1	1	1	1	1
C7H	Timer 2 B Data High Register	T2BDRH	R/W	1	1	1	1	1	1	1	1
C8H	Oscillator Control Register	OSCCR	R/W	–	–	0	0	1	0	0	0
C9H	P4 Direction Register	P4IO	R/W	–	–	–	–	0	0	0	0
CAH	UART2 Control Register 1	UART2CR1	R/W	–	–	0	0	0	0	0	–
CBH	UART2 Control Register 2	UART2CR2	R/W	0	0	0	0	0	0	0	0
CCH	UART2 Control Register 3	UART2CR3	R/W	–	0	–	–	–	0	0	0
CDH	UART2 Status Register	UART2ST	R/W	1	0	0	0	0	0	0	0
CEH	UART2 Baud Rate Generation Register	UART2BD	R/W	1	1	1	1	1	1	1	1
CFH	UART2 Data Register	UART2DR	R/W	0	0	0	0	0	0	0	0
D0H	Program Status Word Register	PSW	R/W	0	0	0	0	0	0	0	0
D1H	P5 Direction Register	P5IO	R/W	–	–	0	0	0	0	0	0
D2H	P0 Function Selection Low Register	P0FSRL	R/W	–	0	0	0	0	0	0	0
D3H	P0 Function Selection High Register	P0FSRH	R/W	–	–	0	0	0	0	0	0
D4H	P1 Function Selection Low Register	P1FSRL	R/W	0	0	0	0	0	0	0	0
D5H	P1 Function Selection High Register	P1FSRH	R/W	0	0	0	0	0	0	0	0
D6H	P2 Function Selection Low Register	P2FSRL	R/W	–	–	–	–	0	0	0	0
D7H	Reserved	–	–	–	–	–	–	–	–	–	–
D8H	Low Voltage Reset Control Register	LVRCCR	R/W	0	–	–	0	0	0	0	0
D9H	USI0 Control Register 1	USI0CR1	R/W	0	0	0	0	0	0	0	0
DAH	USI0 Control Register 2	USI0CR2	R/W	0	0	0	0	0	0	0	0
DBH	USI0 Control Register 3	USI0CR3	R/W	0	0	0	0	0	0	0	0
DCH	USI0 Control Register 4	USI0CR4	R/W	0	–	–	0	0	–	0	0
DDH	USI0 Slave Address Register	USI0SAR	R/W	0	0	0	0	0	0	0	0
DEH	P0 Debounce Enable Register	P0DB	R/W	0	0	0	0	0	0	0	0
DFH	P1/P5 Debounce Enable Register	P15DB	R/W	–	–	0	0	0	0	0	0

Table 7. SFR Map (continued)

Address	Function	Symbol	R/W	@ Reset							
				7	6	5	4	3	2	1	0
E0H	Accumulator Register	ACC	R/W	0	0	0	0	0	0	0	0
E1H	USI0 Status Register 1	USI0ST1	R/W	1	0	0	0	–	0	0	0
E2H	USI0 Status Register 2	USI0ST2	R	0	0	0	0	0	0	0	0
E3H	USI0 Baud Rate Generation Register	USI0BD	R/W	1	1	1	1	1	1	1	1
E4H	USI0 SDA Hold Time Register	USI0SDHR	R/W	0	0	0	0	0	0	0	1
E5H	USI0 Data Register	USI0DR	R/W	0	0	0	0	0	0	0	0
E6H	USI0 SCL Low Period Register	USI0SCLR	R/W	0	0	1	1	1	1	1	1
E7H	USI0 SCL High Period Register	USI0SCHR	R/W	0	0	1	1	1	1	1	1
E8H	Reset Flag Register	RSTFR	R/W	1	x	0	0	x	–	–	–
E9H	USI1 Control Register 1	USI1CR1	R/W	0	0	0	0	0	0	0	0
EAH	USI1 Control Register 2	USI1CR2	R/W	0	0	0	0	0	0	0	0
EBH	USI1 Control Register 3	USI1CR3	R/W	0	0	0	0	0	0	0	0
ECH	USI1 Control Register 4	USI1CR4	R/W	0	–	–	0	0	–	0	0
EDH	USI1 Slave Address Register	USI1SAR	R/W	0	0	0	0	0	0	0	0
EEH	P3 Function Selection Register	P3FSR	R/W	0	0	–	–	–	–	–	–
EFH	P4 Function Selection Register	P4FSR	R/W	–	–	–	0	–	0	–	0
F0H	B Register	B	R/W	0	0	0	0	0	0	0	0
F1H	USI1 Status Register 1	USI1ST1	R/W	1	0	0	0	–	0	0	0
F2H	USI1 Status Register 2	USI1ST2	R	0	0	0	0	0	0	0	0
F3H	USI1 Baud Rate Generation Register	USI1BD	R/W	1	1	1	1	1	1	1	1
F4H	USI1 SDA Hold Time Register	USI1SDHR	R/W	0	0	0	0	0	0	0	1
F5H	USI1 Data Register	USI1DR	R/W	0	0	0	0	0	0	0	0
F6H	USI1 SCL Low Period Register	USI1SCLR	R/W	0	0	1	1	1	1	1	1
F7H	USI1 SCL High Period Register	USI1SCHR	R/W	0	0	1	1	1	1	1	1
F8H	Interrupt Priority Register 1	IP1	R/W	–	–	0	0	0	0	0	0
F9H	Reserved	–	–	–	–	–	–	–	–	–	–
FAH	Flash Sector Address High Register	FSADRH	R/W	–	–	–	–	0	0	0	0
FBH	Flash Sector Address Middle Register	FSADRM	R/W	0	0	0	0	0	0	0	0
FCH	Flash Sector Address Low Register	FSADRL	R/W	0	0	0	0	0	0	0	0
FDH	Flash Identification Register	FIDR	R/W	0	0	0	0	0	0	0	0
FEH	Flash Mode Control Register	FMCR	R/W	0	–	–	–	–	0	0	0
FFH	P5 Function Selection Register	P5FSR	R/W	–	0	0	0	0	0	0	0

Extended SFR Map**Table 8. XSFR Map**

Address	Function	Symbol	R/W	@ Reset							
				7	6	5	4	3	2	1	0
1000H	Timer 3 Control Register	T3CR	R/W	0	–	0	0	0	0	0	0
1001H	Timer 3 Counter Register	T3CNT	R	0	0	0	0	0	0	0	0
1001H	Timer 3 Data Register	T3DR	W	1	1	1	1	1	1	1	1
1001H	Timer 3 Capture Data Register	T3CAPR	R	0	0	0	0	0	0	0	0
1002H	Timer 4 Control Register	T4CR	R/W	0	0	0	0	0	0	0	0
1003H	Timer 4 PWM Control Register 1	T4PCR1	R/W	0	0	0	0	0	0	0	0
1004H	Timer 4 PWM Control Register 2	T4PCR2	R/W	0	0	0	0	0	0	0	0
1005H	Timer 4 PWM Control Register 3	T4PCR3	R/W	–	0	0	0	–	–	–	–
1006H	Timer 4 Interrupt Status Register	T4ISR	R/W	0	0	0	0	0	–	–	–
1007H	Timer 4 Interrupt Mask Register	T4MSK	R/W	0	0	0	0	0	–	–	–
1008H	Timer 4 PWM Period Low Register	T4PPRL	R/W	1	1	1	1	1	1	1	1
1009H	Timer 4 PWM Period High Register	T4PPRH	R/W	–	–	–	–	–	–	0	0
100AH	Timer 4 PWM A Duty Low Register	T4ADRL	R/W	0	1	1	1	1	1	1	1
100BH	Timer 4 PWM A Duty High Register	T4ADRH	R/W	–	–	–	–	–	–	0	0
100CH	Timer 4 PWM B Duty Low Register	T4BDRL	R/W	0	1	1	1	1	1	1	1
100DH	Timer 4 PWM B Duty High Register	T4BDRH	R/W	–	–	–	–	–	–	0	0
100EH	Timer 4 PWM C Duty Low Register	T4CDRL	R/W	0	1	1	1	1	1	1	1
100FH	Timer 4 PWM C Duty High Register	T4CDRH	R/W	–	–	–	–	–	–	0	0
1010H	Timer 4 PWM A Delay Register	T4DLYA	R/W	0	0	0	0	0	0	0	0
1011H	Timer 4 PWM B Delay Register	T4DLYB	R/W	0	0	0	0	0	0	0	0
1012H	Timer 4 PWM C Delay Register	T4DLYC	R/W	0	0	0	0	0	0	0	0
1013H	Timer 4 Data Register	T4DR	R/W	1	1	1	1	1	1	1	1
1014H	Timer 4 Capture Data Register	T4CAPR	R	0	0	0	0	0	0	0	0
1015H	Timer 4 Counter Register	T4CNT	R	0	0	0	0	0	0	0	0

101EH	Timer 1 Capture Data Low Register	T1CAPL	R	0	0	0	0	0	0	0	0
101FH	Timer 1 Capture Data High Register	T1CAPH	R	0	0	0	0	0	0	0	0

1026H	Timer 2 Capture Data Low Register	T2CAPL	R	0	0	0	0	0	0	0	0
1027H	Timer 2 Capture Data High Register	T2CAPH	R	0	0	0	0	0	0	0	0

1038H	X-tal Filter Selection Register	XTFLSR	R/W	0	0	0	0	0	–	–	0
1039H	LED Display Drive Selection Register	LDDRVSR	R/W	0	0	0	0	0	0	0	0

Table 8. XSFR Map (continued)

Address	Function	Symbol	R/W	@ Reset							
				7	6	5	4	3	2	1	0

1060H	Unique ID Register 0	UNIQUEID0	R	x	x	x	x	x	x	x	x
1061H	Unique ID Register 1	UNIQUEID1	R	x	x	x	x	x	x	x	x
1062H	Unique ID Register 2	UNIQUEID2	R	x	x	x	x	x	x	x	x
1063H	Unique ID Register 3	UNIQUEID3	R	x	x	x	x	x	x	x	x
1064H	Unique ID Register 4	UNIQUEID4	R	x	x	x	x	x	x	x	x
1065H	Unique ID Register 5	UNIQUEID5	R	x	x	x	x	x	x	x	x
1066H	Unique ID Register 6	UNIQUEID6	R	x	x	x	x	x	x	x	x
1067H	Unique ID Register 7	UNIQUEID7	R	x	x	x	x	x	x	x	x
1068H	Unique ID Register 8	UNIQUEID8	R	x	x	x	x	x	x	x	x
1069H	Unique ID Register 9	UNIQUEID9	R	x	x	x	x	x	x	x	x
106AH	Unique ID Register 10	UNIQUEID10	R	x	x	x	x	x	x	x	x
106BH	Unique ID Register 11	UNIQUEID11	R	x	x	x	x	x	x	x	x
106CH	Unique ID Register 12	UNIQUEID12	R	x	x	x	x	x	x	x	x
106DH	Unique ID Register 13	UNIQUEID13	R	x	x	x	x	x	x	x	x
106EH	Unique ID Register 14	UNIQUEID14	R	x	x	x	x	x	x	x	x
106FH	Unique ID Register 15	UNIQUEID15	R	x	x	x	x	x	x	x	x

5040H	User Memory Control Register	USERMCR	0	0	0	0	0	0	0	0	0
5041H	User Memory Sector Selection Register	USERMSSR	0	0	0	0	0	0	0	0	0
5042H	User Memory Identification Register	USERMIDR	0	0	0	0	0	0	0	0	0

5050H	Flash CRC Start Address High Register	FCSARH	R/W	–	–	–	–	–	–	–	0
5051H	Flash CRC End Address High Register	FCEARH	R/W	–	–	–	–	–	–	–	0
5052H	Flash CRC Start Address Middle Register	FCSARM	R/W	0	0	0	0	0	0	0	0
5053H	Flash CRC End Address Middle Register	FCEARM	R/W	0	0	0	0	0	0	0	0
5054H	Flash CRC Start Address Low Register	FCSARL	R/W	0	0	0	0	–	–	–	–
5055H	Flash CRC End Address Low Register	FCEARL	R/W	0	0	0	0	–	–	–	–
5056H	Flash CRC Control Register	FCCR	R/W	0	0	0	–	0	0	0	0
5057H	Flash CRC Data High Register	FCDRH	R/W	1	1	1	1	1	1	1	1
5058H	Flash CRC Data Low Register	FCDRL	R/W	1	1	1	1	1	1	1	1

2.4.3 Ports

2.4.3.1 I/O Ports

MC96F6432P has six groups of I/O ports: P0, P1, P2, P3, P4 and P5. Each port can be easily configured as an input pin, an output, or an internal pull up and open-drain pin by software.

The port configuration pursues to meet various system configurations and design requirements.

2.4.3.2 Port Description of P0

As an 8-bit I/O port, P0 controls the following registers:

- P0 data register (P0)
- P0 direction register (P0IO)
- P0 debounce enable register (P0DB)
- P0 pull-up resistor selection register (P0PU)
- P0 open-drain selection register (P0OD)
- P0 Function selection registers (P0FSRH/P0FSRL)

2.4.3.3 Port Description of P1

As an 8-bit I/O port, P1 controls the following registers:

- P1 data register (P1)
- P1 direction register (P1IO)
- P1/P5 debounce enable register (P15DB)
- P1 pull-up resistor selection register (P1PU)
- P1 open-drain selection register (P1OD)
- P1 Function selection registers (P1FSRH/P1FSRL)

2.4.3.4 Port Description of P2

As an 8-bit I/O port, P2 controls the following registers:

- P2 data register (P2)
- P2 direction register (P2IO)
- P2 pull-up resistor selection register (P2PU)
- P2 open-drain selection register (P2OD)
- P2 Function selection register (P2FSRL)

2.4.3.5 Port Description of P3

As an 8-bit I/O port, P3 controls the following registers:

- P3 data register (P3)
- P3 direction register (P3IO)
- P3 pull-up resistor selection register (P3PU)
- P3 Function selection register (P3FSR)

2.4.3.6 Port Description of P4

As a 4-bit I/O port, P4 controls the following registers:

- P4 data register (P4)
- P4 direction register (P4IO)
- P4 pull-up resistor selection register (P4PU)
- P4 open-drain selection register (P4OD)
- P4 Function selection register (P4FSR)

2.4.3.7 Port Description of P5

As a 6-bit I/O port, P5 controls the following registers:

- P5 data register (P5)
- P5 direction register (P5IO)
- P5 pull-up resistor selection register (P5PU)
- P5 Function selection registers (P5FSR)

2.4.3.8 LED Display Drive Selection

As an 8-bit I/O port for LED display drive pins (P1[1:0], P2[1:0], P3[3:0])

2.4.4 Interrupt Controller

Up to 22 interrupt sources are available in the MC96F6432P. Allowing software control, each interrupt source can be enabled by defining separate enable register bit associated with it. It can also have four levels of priority assigned. The non-maskable interrupt source is always enabled with a higher priority than any other interrupt sources and is not controllable by software.

The interrupt controller features the following:

- Receives requests from 22 interrupt sources
- 6 group priority
- 4 priority levels
- Multi interrupt possibility
- If requests of different priority levels are received simultaneously, a request with higher priority level is served first.
- Each interrupt source can be controlled by an EA bit and an IEx bit
- Interrupt latency varies from 3 to 9 machine cycles in a single interrupt system.

Non-maskable interrupt is always enabled, while maskable interrupts can be enabled through four pairs of interrupt enable registers (IE, IE1, IE2, and IE3). Each bit of the four registers can individually enable or disable a particular interrupt source. Especially bit 7 (EA) in the register IE provides overall control.

It must be set to '1' to enable interrupts as described in the followings:

- When EA is set to '0' → all interrupts are disabled.
- When EA is set to '1' → a particular interrupt can be individually enabled or disabled by the associate bit of the interrupt enable registers.

EA is always cleared to '0' jumping to an interrupt service vector and set to '1' executing the [RETI] instruction. MC96F6432P supports a four-level priority scheme. Each maskable interrupt is individually assigned to one of the four levels according to IP and IP1.

Figure 8. Interrupt Group Priority Level

Interrupt Group	Highest Lowest →				
0 (Bit0)	Interrupt 0	Interrupt 6	Interrupt 12	Interrupt 18	Highest Lowest ↓
1 (Bit1)	Interrupt 1	Interrupt 7	Interrupt 13	Interrupt 19	
2 (Bit2)	Interrupt 2	Interrupt 8	Interrupt 14	Interrupt 20	
3 (Bit3)	Interrupt 3	Interrupt 9	Interrupt 15	Interrupt 21	
4 (Bit4)	Interrupt 4	Interrupt 10	Interrupt 16	Interrupt 22	
5 (Bit5)	Interrupt 5	Interrupt 11	Interrupt 17	Interrupt 23	

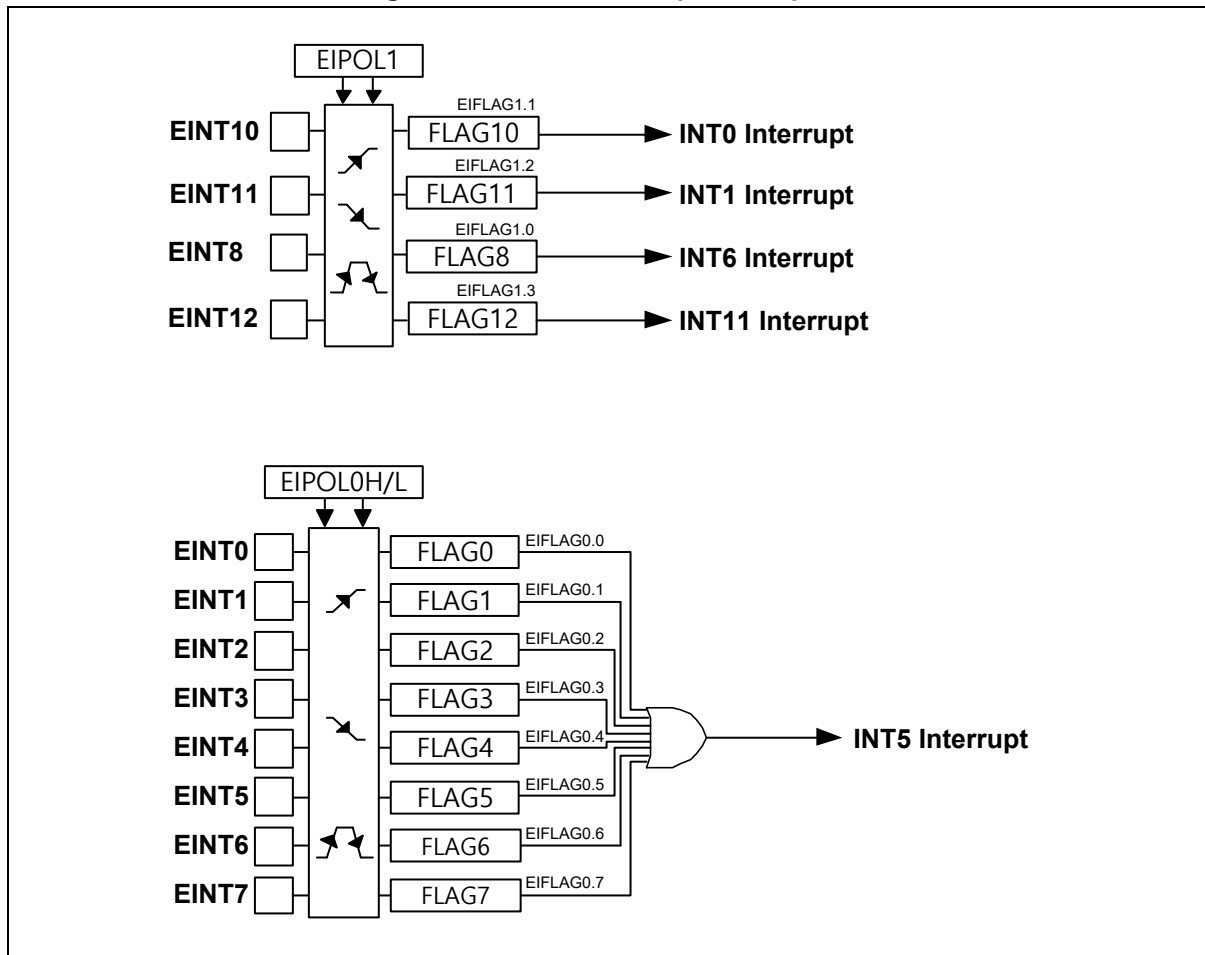
Figure 8 describes interrupt groups and their priority levels that is available for sharing interrupt priority. Priority of a group is set by 2 bits of Interrupt Priority (IP) registers: 1 bit from IP and another 1 bit from IP1.

Interrupt Service Routine serves an interrupt having higher priority first. If two requests of different priority levels are received simultaneously, the request with a higher priority level is served prior to the lower one.

2.4.4.1 External Interrupt

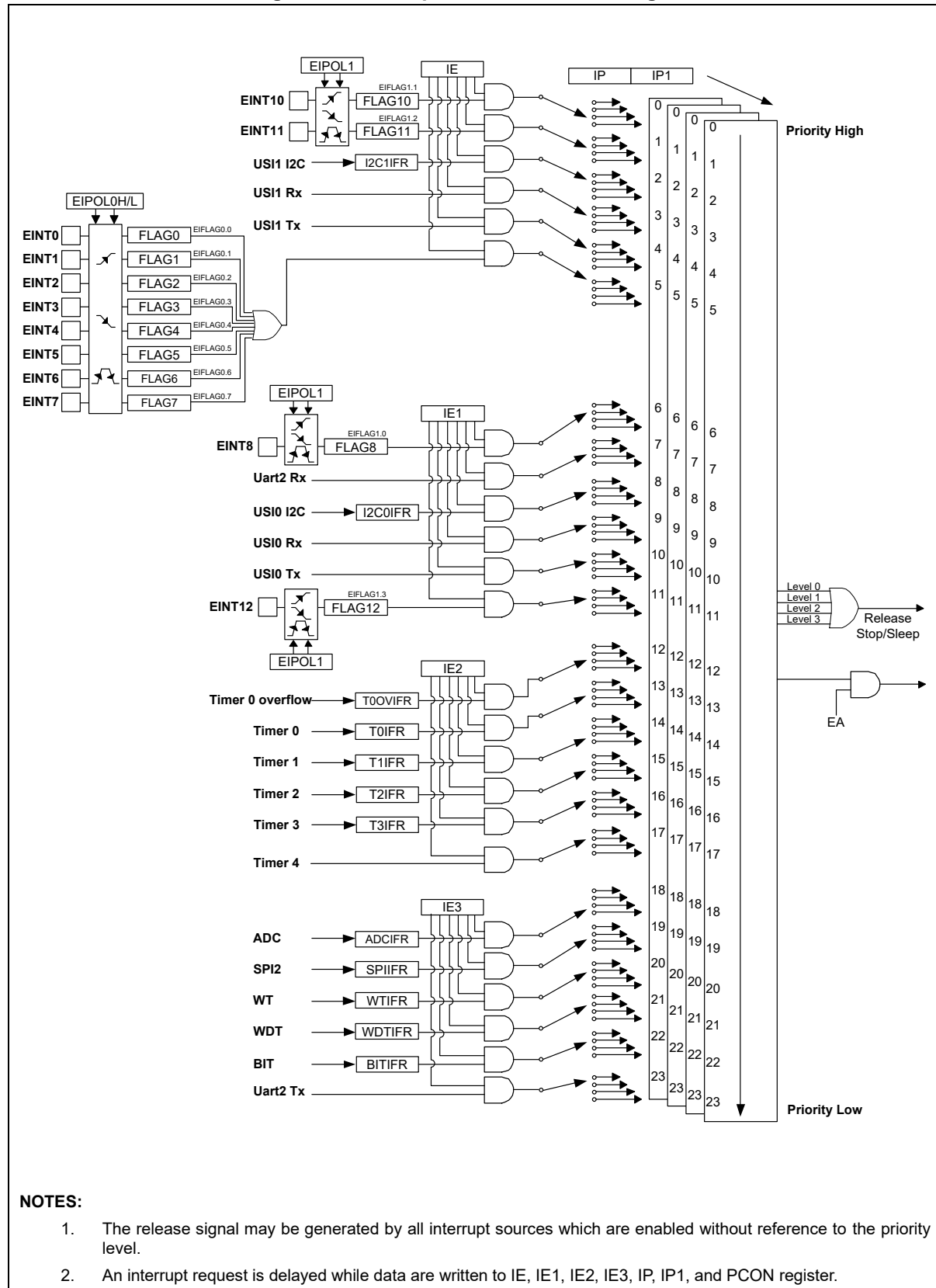
External interrupts on pins of INT0 to INT1, INT5 to INT6, INT11 receive various interrupt requests in accordance with the external interrupt polarity 0 registers (EIPOL0H/L), external interrupt polarity 1 register (EIPOL1), as shown in Figure 9. Each external interrupt source has enable/disable bits. An external interrupt flag register (EIFLAG) provides status of the external interrupts.

Figure 9. External Interrupt Description



2.4.4.2 Interrupt Controller Block Diagram

Figure 10. Interrupt Controller Block Diagram



In Figure 10, release signal for STOP and IDLE mode can be generated by all interrupt sources which are enabled without reference to priority level. An interrupt request will be delayed while data is written to one of the registers IE, IE1, IE2, IE3, IP, IP1, and PCON.

2.4.4.3 Interrupt Vector Table

When a certain interrupt occurs, a LCALL (Long Call) instruction pushes the contents of the PC (Program Counter) onto the stack and loads the appropriate vector address. CPU pauses from its current task for some time and processes the interrupt at the vector address. The Interrupt controller supports 24 interrupt sources and each interrupt source has a determined priority order as shown in Table 9.

Table 9. Interrupt Vector Address Table

Interrupt Source	Symbol	Interrupt Enable Bit	Priority	Mask	Vector Address
Hardware RESET	RESETB	–	0	Non-Maskable	0000H
External Interrupt 10	INT0	IE.0	1	Maskable	0003H
External Interrupt 11	INT1	IE.1	2	Maskable	000BH
USI1 I2C Interrupt	INT2	IE.2	3	Maskable	0013H
USI1 Rx Interrupt	INT3	IE.3	4	Maskable	001BH
USI1 Tx Interrupt	INT4	IE.4	5	Maskable	0023H
External Interrupt 0 – 7	INT5	IE.5	6	Maskable	002BH
External Interrupt 8	INT6	IE1.0	7	Maskable	0033H
UART2 Rx Interrupt	INT7	IE1.1	8	Maskable	003BH
USI0 I2C Interrupt	INT8	IE1.2	9	Maskable	0043H
USI0 Rx Interrupt	INT9	IE1.3	10	Maskable	004BH
USI0 Tx Interrupt	INT10	IE1.4	11	Maskable	0053H
External Interrupt 12	INT11	IE1.5	12	Maskable	005BH
T0 Overflow Interrupt	INT12	IE2.0	13	Maskable	0063H
T0 Match Interrupt	INT13	IE2.1	14	Maskable	006BH
T1 Match Interrupt	INT14	IE2.2	15	Maskable	0073H
T2 Match Interrupt	INT15	IE2.3	16	Maskable	007BH
T3 Match Interrupt	INT16	IE2.4	17	Maskable	0083H
T4 Interrupt	INT17	IE2.5	18	Maskable	008BH
ADC Interrupt	INT18	IE3.0	19	Maskable	0093H
SPI 2 Interrupt	INT19	IE3.1	20	Maskable	009BH
WT Interrupt	INT20	IE3.2	21	Maskable	00A3H
WDT Interrupt	INT21	IE3.3	22	Maskable	00ABH
BIT Interrupt	INT22	IE3.4	23	Maskable	00B3H
UART2 Tx Interrupt	INT23	IE3.5	24	Maskable	00BBH

To execute the maskable interrupts, both EA bit and a corresponding bit of IEx associated with a specific interrupt source must be set to '1'. When an interrupt request is received, a particular interrupt request flag is set to '1' and maintains its status until CPU accepts the interrupt. After the interrupt acceptance, the interrupt request flag will be cleared automatically.

2.4.5 Clock Generator

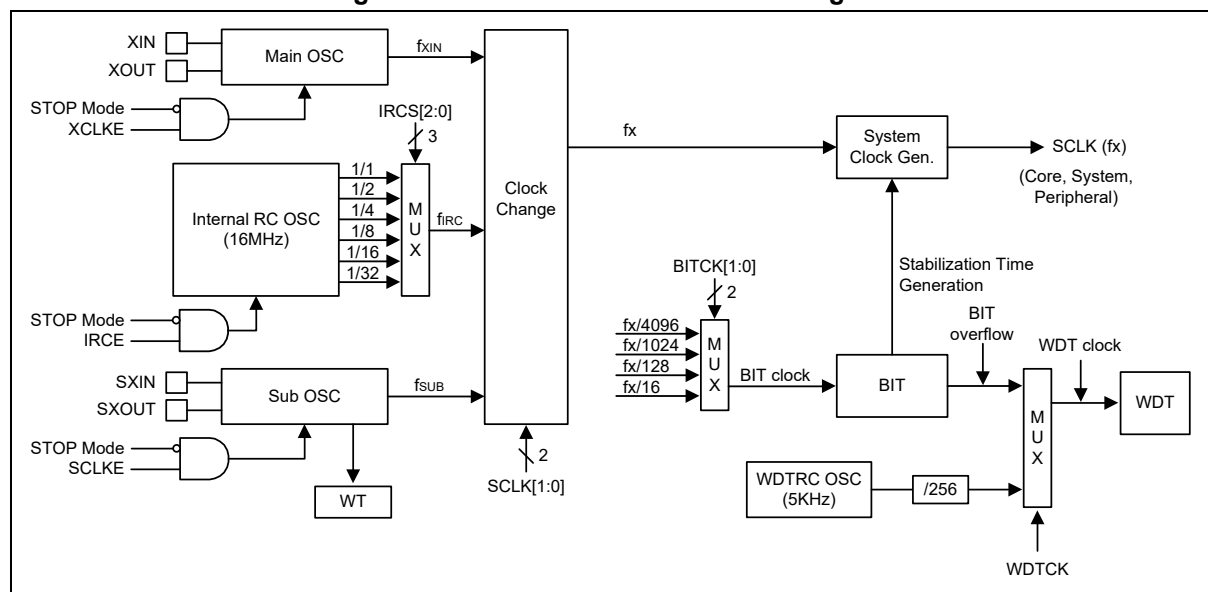
As shown in Figure 11, a clock generator produces basic clock pulses which provide a CPU and peripherals with a system clock. It contains main/sub-frequency clock oscillator. The main/sub clock operation can be easily obtained by attaching a crystal between the XIN/SXIN and XOUT/SXOUT pin, respectively. The main/sub clock can be also obtained from the external oscillator. In this case, it is necessary to put the external clock signal into the XIN/SXIN pin and open the XOUT/SXOUT pin. A default system clock is a 1 MHz INT-RC oscillator, and a default division rate is sixteen. To stabilize the system internally, it is used 1 MHz INT-RC oscillator on POR.

MC96F6432P incorporates four types of oscillators:

- Calibrated Internal RC Oscillator (16 MHz)
 - INT-RC OSC/32 (0.5 MHz)
 - INT-RC OSC/16 (1 MHz, default system clock)
 - INT-RC OSC/8 (2 MHz)
 - INT-RC OSC/4 (4 MHz)
 - INT-RC OSC/2 (8 MHz)
 - INT-RC OSC/1 (16 MHz)
- Main Crystal Oscillator (0.4~8.5 MHz)
- Sub Crystal Oscillator (32.768 kHz)
- Internal WDTRC Oscillator (5 kHz)

2.4.5.1 Block Diagram

Figure 11. Clock Generator in Block Diagram



2.4.6 Basic Interval Timer (BIT)

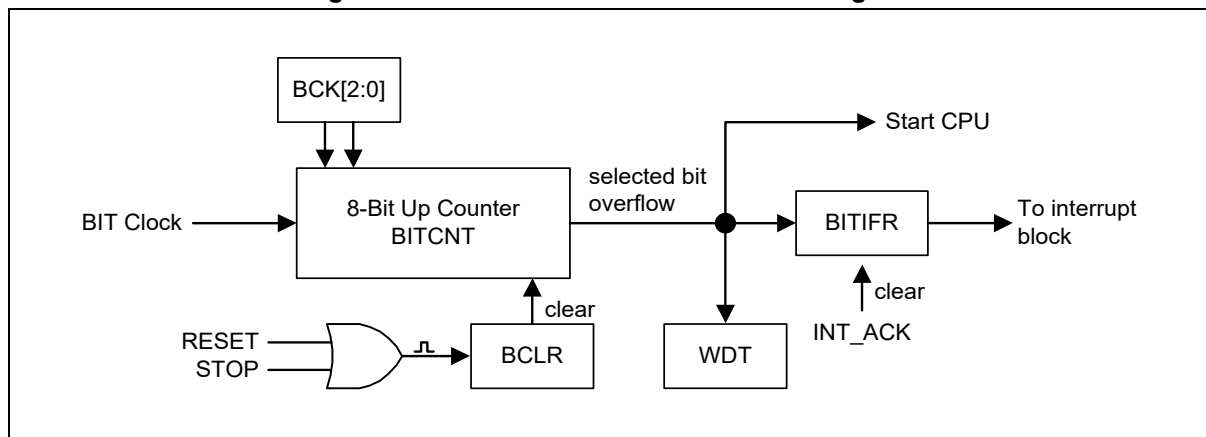
MC96F6432P has a free-running 8-bit Basic Interval Timer (BIT). BIT generates the time base for watchdog timer counting and provides a basic interval timer interrupt (BITIFR).

BIT of MC96F6432P features the following:

- During Power-On, BIT gives a stable clock generation time
- On exiting Stop mode, BIT gives a stable clock generation time
- As a timer, BIT generates a timer interrupt.

2.4.6.1 Block Diagram

Figure 12. Basic Interval Timer in Block Diagram



2.4.7 Watchdog Timer (WDT)

Watchdog Timer (WDT) is used to rapidly detect CPU malfunctions such as endless looping caused by noise. In addition, it is used to resume the CPU in a normal state. Watchdog timer signal for malfunction detection can be used as either a CPU reset or an interrupt request. When the WDT is not being used for the detection of the CPU malfunctions, it can be used as a timer generating an interrupt at fixed intervals.

The WDT can be used in a free running 8-bit timer mode or in a watchdog timer mode by setting WDTRSON bit, which is WDTCR[6]. If '1' is written to WDTCR[5], WDT counter value is cleared and counts up. After 1 machine cycle, this bit is cleared to '0' automatically.

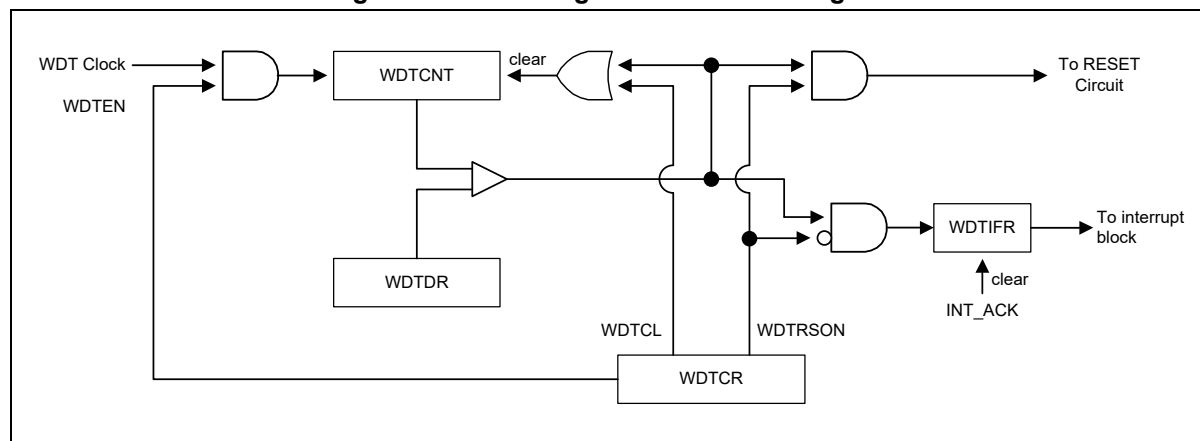
The WDT consists of an 8-bit binary counter and a watchdog timer data register. When the value of an 8-bit binary counter is equal to the 8 bits of WDCNT, an interrupt request flag is generated. This can be used as a watchdog timer interrupt or a reset of CPU in accordance with a bit WDTRSON.

The input clock source of watchdog timer is BIT overflow and WDTRC. Interval of watchdog timer interrupt is decided by the BIT overflow period and WDTDR set value. Equation of the WDT interrupt interval is described in the following:

- WDT Interrupt Interval = (BIT Interrupt Interval) X (WDTDR Value+1)
- WDT Interrupt Interval = $256/f_{WDTRC} \times (WDTDR \text{ Value} + 1)$ when WDTRC

2.4.7.1 Block Diagram

Figure 13. Watchdog Timer in Block Diagram



2.4.8 Watch Timer (WT)

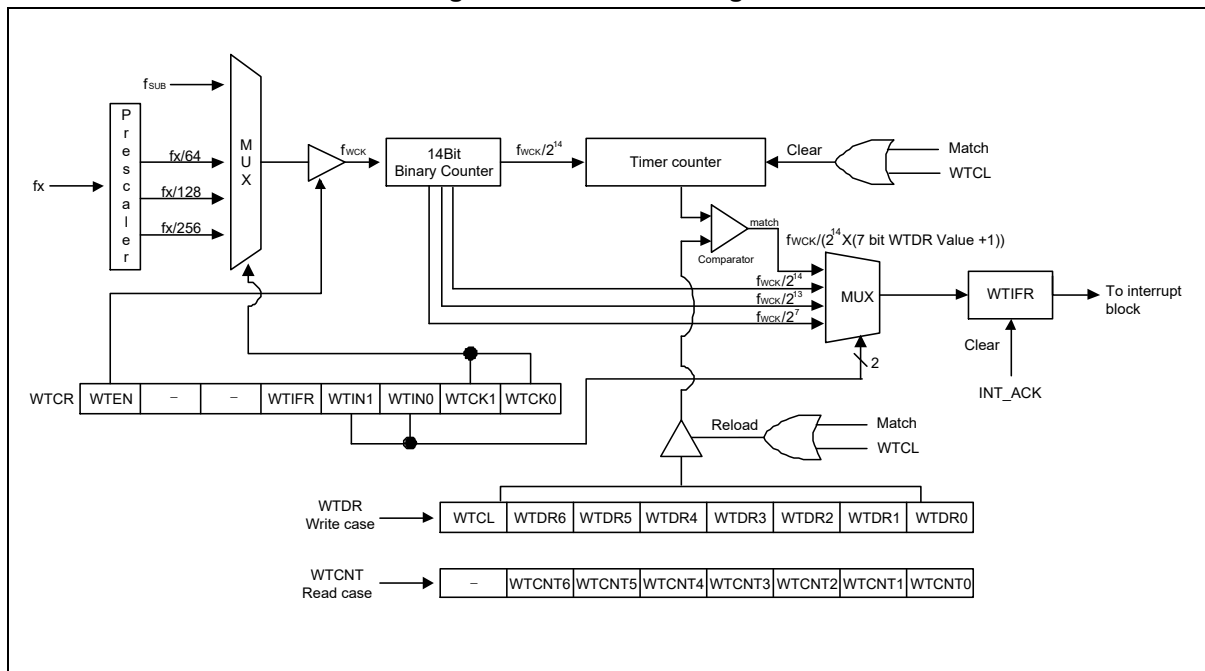
The watch timer has the function for RTC (Real Time Clock) operation. It is generally used for RTC design. The internal structure of the watch timer consists of the clock source select circuit, timer counter circuit, output select circuit and watch timer control register.

To operate the watch timer, determine the input clock source, output interval and set WTEN to '1' in watch timer control register (WTCR). It can be executed simultaneously or individually.

To stop or reset WT, clear the WTEN bit in WTCR register. Even if CPU is STOP mode, sub clock can be so alive that WT can continue the operation.

The watch timer counter circuits may be composed of 21-bit counter which contains low 14-bit with binary counter and high 7-bit counter to raise resolution. In WTDR, it can control WT clear and set interval value at write time and it can read 7-bit WT counter value at read time.

Figure 14. WT Block Diagram



2.4.9 TIMER 0

The 8-bit timer 0 consists of multiplexer, timer 0 counter register, timer 0 data register, timer 0 capture data register and timer 0 control register (T0CNT, T0DR, T0CDR, T0CR).

TIMER 0 operates in one of three operating modes:

- 8-bit capture mode
- 8-bit timer/counter mode
- 8-bit PWM output mode

Specifically in capture mode, data is captured into input capture data register (T0CDR) by EINT10. Timer 0 outputs the comparison result between counter and data register through T0O port in timer/counter mode. Timer 0 outputs PWM wave form through PWM0O port in the PPG mode).

A timer/counter 0 uses an internal clock or an external clock (EC0) as an input clock source. The clock sources are described below, and one is selected by clock selection logic which is controlled by clock selection bits (T0CK[2:0]).

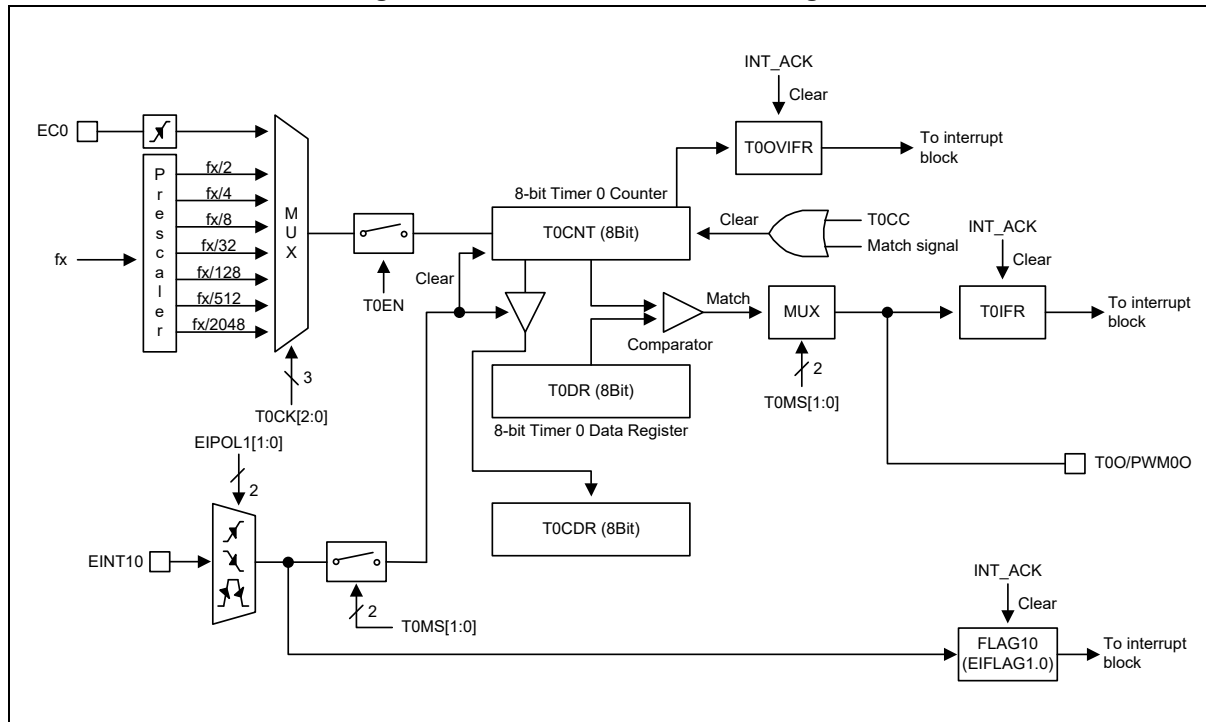
- Timer 0 clock sources: $f_x/2$, 4, 8, 32, 128, 512, 2048 and EC0

Table 10. TIMER 0 Operating Modes

T0EN	P5FSRL[5:4]	T0MS[1:0]	T0CK[2:0]	Timer 0
1	10	00	XXX	8 Bit Timer/Counter Mode
1	00	1X	XXX	8 Bit Capture Mode
1	10	01	XXX	8 Bit PWM Mode

2.4.9.1 Block Diagram

Figure 15. 8-Bit Timer 0 in Block Diagram



2.4.10 TIMER 1

A 16-bit timer 1 incorporates a multiplexer and eight registers such as timer 1 A data register high/low, timer 1 B data register high/low, timer 1 capture data register high/low, and timer 1 control register high/low (T1ADRH, T1ADRL, T1BDRH, T1BDRL, T1CAPH, T1CAPL, T1CRH, T1CRL).

TIMER 1 operates in one of four operating modes:

- 16-bit capture mode
- 16-bit timer/ counter mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

Specifically in capture mode, data is captured into capture data register (T1CAPH/T1CAPL) by EINT11. Timer 1 outputs the comparison result between counter and data register through T1O port in timer/counter mode. Timer 1 outputs PWM wave form through PWM1O port in the PPG mode).

A timer/counter 1 uses an internal clock or an external clock (EC1) as an input clock source. The clock sources are described below, and one is selected by clock selection logic which is controlled by clock selection bits (T1CK[2:0]).

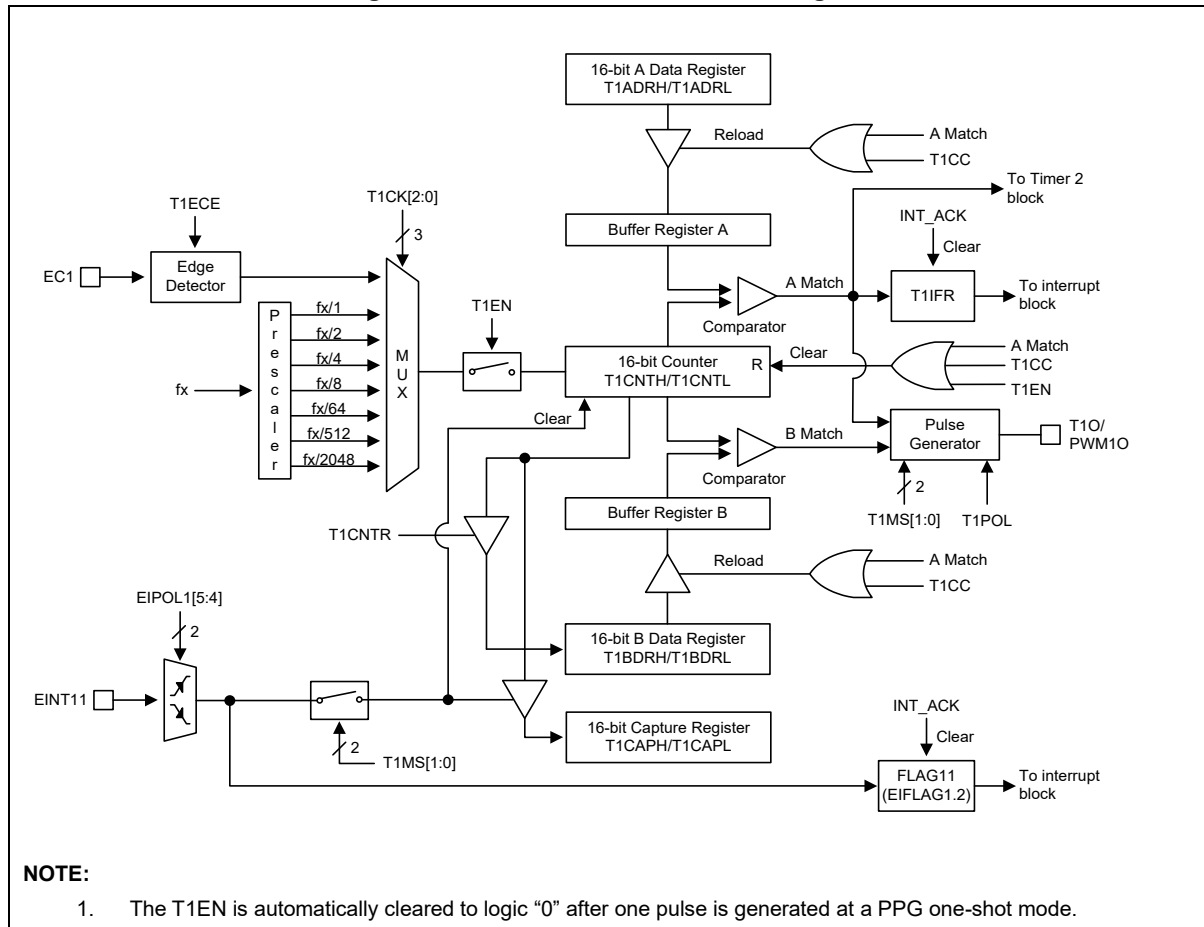
- Timer 1 clock sources: $f_x/1, 2, 4, 8, 64, 512, 2048$ and EC1

Table 11. TIMER 1 Operating Modes

T1EN	P1FSRL[5:4]	T1MS[1:0]	T1CK[2:0]	Timer 1
1	11	00	XXX	16 Bit Timer/Counter Mode
1	00	01	XXX	16 Bit Capture Mode
1	11	10	XXX	16 Bit PPG Mode (one-shot mode)
1	11	11	XXX	16 Bit PPG Mode (repeat mode)

2.4.10.1 Block Diagram

Figure 16. 16-Bit Timer 1 in Block Diagram



2.4.11 TIMER 2

A 16-bit timer 2 incorporates a multiplexer and eight registers such as timer 2 A data register high/low, timer 2 B data register high/low, timer 2 capture data register high/low, and timer 2 control register high/low (T2ADRH, T2ADRL, T2BDRH, T2BDRL, T2CAPH, T2CAPL, T2CRH, T2CRL).

TIMER 2 operates in one of four operating modes:

- 16-bit capture mode
- 16-bit timer/ counter mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

Specifically in capture mode, data is captured into capture data register (T2CAPH/T2CAPL) by EINT12. Timer 2 outputs the comparison result between counter and data register through T2O port in timer/counter mode. Timer 2 outputs PWM wave form through PWM2O port in the PPG mode).

A timer/counter 2 uses an internal clock or an external clock (T1 A Match) as an input clock source. The clock sources are described below, and one is selected by clock selection logic which is controlled by clock selection bits (T2CK[2:0]).

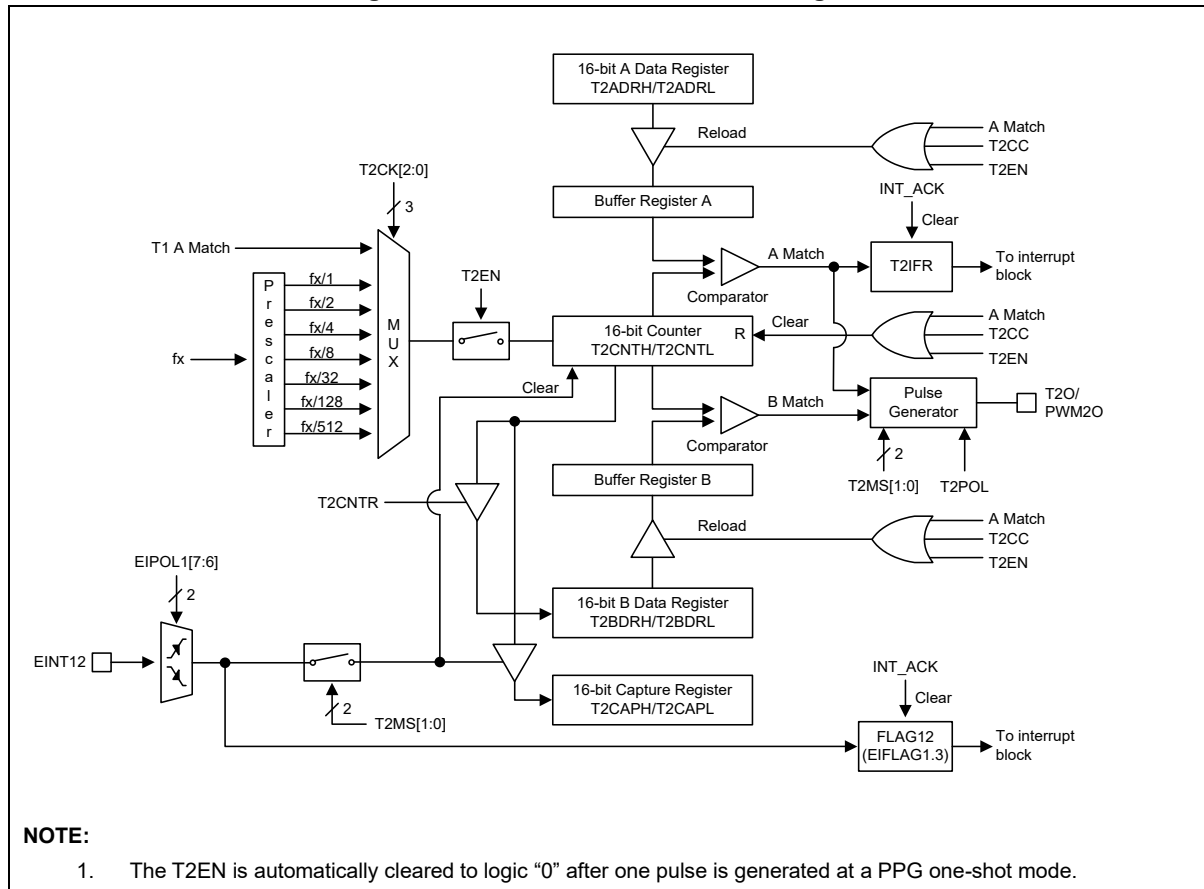
- Timer 2 clock sources: fX/1, 2, 4, 8, 32, 128, 512 and T1 A Match

Table 12. TIMER 2 Operating Modes

T2EN	P1FSRL[3:2]	T2MS[1:0]	T2CK[2:0]	Timer 2
1	11	00	XXX	16 Bit Timer/Counter Mode
1	00	01	XXX	16 Bit Capture Mode
1	11	10	XXX	16 Bit PPG Mode (one-shot mode)
1	11	11	XXX	16 Bit PPG Mode (repeat mode)

2.4.11.1 Block Diagram

Figure 17. 16-Bit Timer 2 in Block Diagram



2.4.12 TIMER 3 and Timer 4

Timer 3 and timer 4 can be used as either two 8-bit timer/counter or one 16-bit timer/counter with combine them. Each 8-bit timer/event counter module has multiplexer, comparator, 8-bit timer data register, 8-bit counter register, control register and capture data register (T3CNT, T3DR, T3CAPR, T3CR, T4CNT, T4DR, T4CAPR and T4CR). For PWM, it has PWM register (T4PPRL, T4PPRH, T4ADRL, T4ADRH, T4BDRL, T4BDRH, T4CDRL, T4CDRH, T4DLYA, T4DLYB, T4DLYC).

TIMER 3/4 operates in one of five operating modes:

- 8-bit timer/counter mode
- 8-bit capture mode
- 16-bit timer/counter mode
- 16-bit capture mode
- 10-bit PWM mode

The timer/counter 3 and 4 can be clocked by an internal or an external clock source (EC3). The clock source is selected by clock selection logic which is controlled by the clock selection bits (T3CK[2:0], T4CK[3:0]). Also, the timer/counter 4 can use more clock sources than timer/counter 3.

- TIMER 3 clock source: $fX/(2, 4, 8, 32, 128, 512, 2048)$, EC3
- TIMER 4 clock source: $fX/(1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024, 2048, 4096, 8192, 16384)$, T3 clock

In the capture mode, by EINT0/EINT1, the data is captured into input capture data register (T3CAPR, T4CAPR). In 8-bit timer/counter 3/4 mode, whenever counter value is equal to T3DR/T4DR, T3O/T4O port toggles. Also, In 16-bit timer/counter 3 mode. The timer 3 outputs the comparison result between counter and data register through T3O port. The PWM waveforms to PWMAA, PWMAB, PWMBA, PWMBB, PWMCA, PWMCB Port(6-channel) in the PWM mode

Table 13. TIMER 3/4 Operating Modes

16 Bit	T3MS	T4MS	PWM4E	T3CK[2:0]	T4CK[3:0]	Timer 3	Timer 4
0	0	0	0	XXX	XXXX	8-bit Timer/Counter Mode	8-bit Timer/Counter Mode
0	1	1	0	XXX	XXXX	8-bit Capture Mode	8-bit Capture Mode
1	0	0	0	XXX	XXXX	16-bit Timer/Counter Mode	
1	1	1	0	XXX	XXXX	16-bit Capture Mode	
0	X	X	1	XXX	XXXX	10-bit PWM Mode	

2.4.12.1 Block Diagram

Figure 18. 8-Bit Timer 3/4 in Block Diagram (Two 8-Bit Mode)

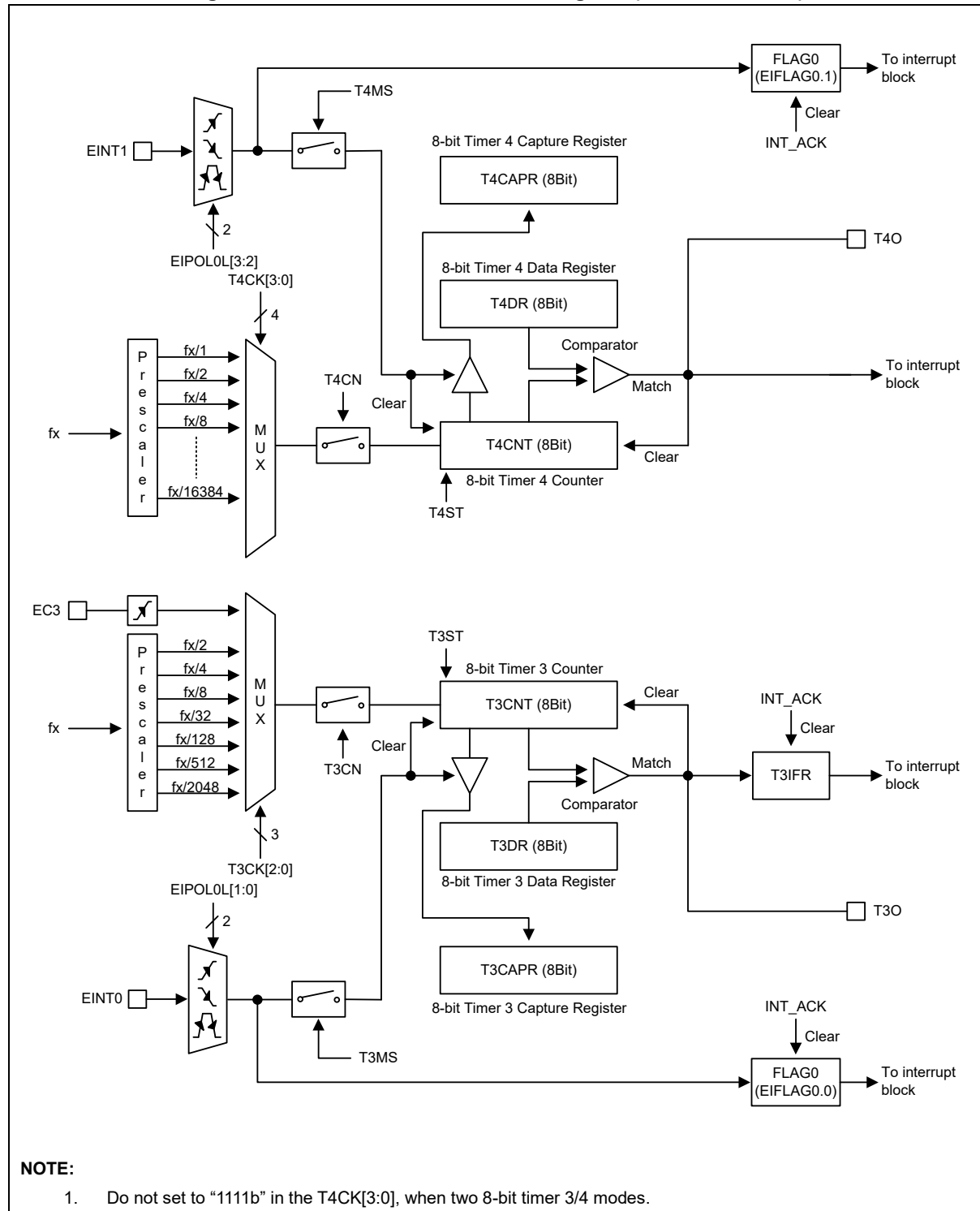
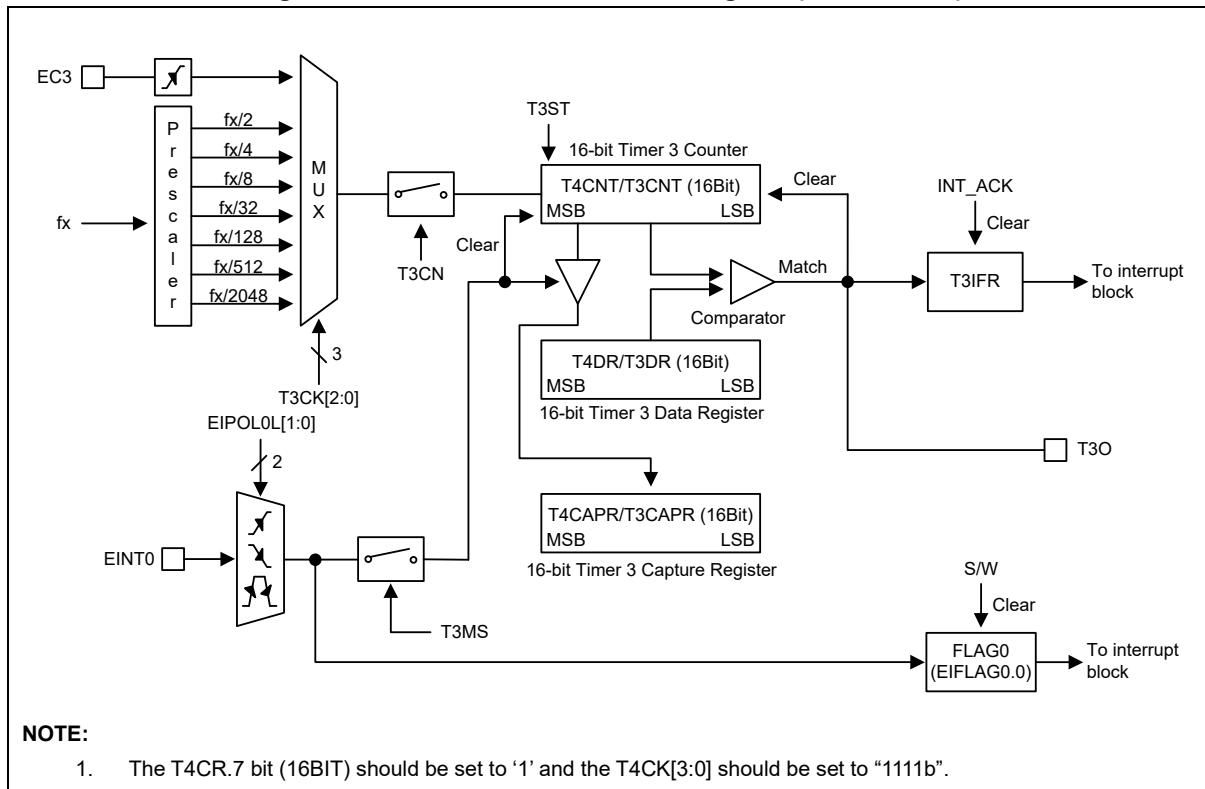


Figure 19. 16-Bit Timer 3 in Block Diagram (16-Bit Mode)

2.4.13 Buzzer

The Buzzer consists of an 8-bit counter, buzzer data register (BUZDR) and buzzer control register (BUZCR). The Square Wave (61.035Hz~125.0 kHz @ 8 MHz) is outputted through P11/BUZO pin. The buzzer data register (BUZDR) controls the buzzer frequency (look at the following expression). In buzzer control register (BUZCR), BUCK[2:0] selects source clock divided by prescaler.

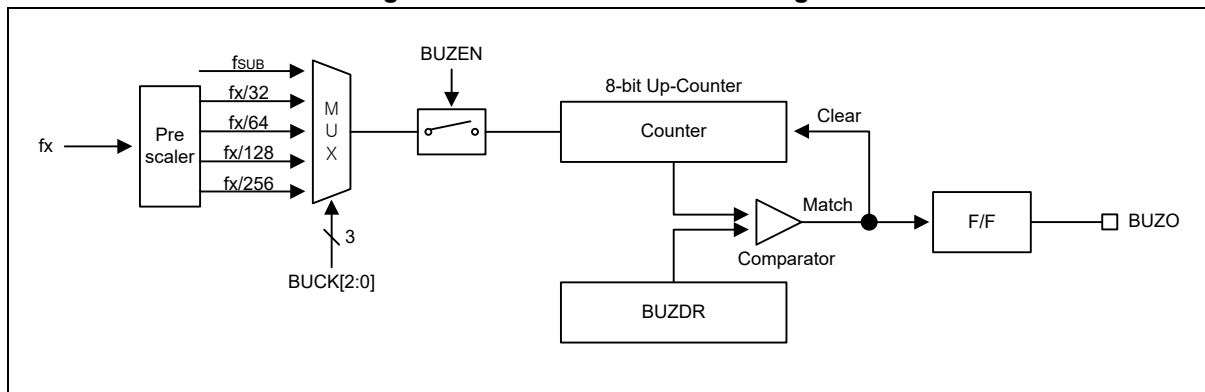
$$f_{\text{BUZ}}(\text{Hz}) = \frac{\text{Oscillator Frequency}}{2 \times \text{Prescaler Ratio} \times (\text{BUZDR} + 1)}$$

Table 14. Buzzer Frequency at 8 MHz

BUZDR[7:0]	Buzzer Frequency (kHz)			
	BUZCR[3:1]=000	BUZCR[3:1]=001	BUZCR[3:1]=010	BUZCR[3:1]=011
0000_0000	125 kHz	62.5 kHz	31.25 kHz	15.625 kHz
0000_0001	62.5 kHz	31.25 kHz	15.625 kHz	7.812 kHz
...	...	...	...	...
1111_1101	492.126 Hz	246.063 Hz	123.031 Hz	61.515 Hz
1111_1110	490.196 Hz	245.098 Hz	122.549 Hz	61.274 Hz
1111_1111	488.281 Hz	244.141 Hz	122.07 Hz	61.035 Hz

2.4.13.1 Block Diagram

Figure 20. Buzzer Driver Block Diagram



2.4.14 12-Bit A/D Converter

Analog-to-Digital (A/D) converter allows conversion of an analog input signal to a corresponding 12-bit digital output. The A/D module has 16 analog inputs, and the output of the multiplexer becomes the input into the converter, which generates a result via successive approximation.

The A/D module incorporates four registers as listed in the following. Each register can be selected for the corresponding channel by setting ADSEL[3:0]. When conversion is completed, two registers ADCDRH and ADCDRL contain the results of the conversion, the conversion status bit AFLAG is set to '1', and A/D interrupt is set. During the A/D conversion, AFLAG bit is read as '0'.

- A/D converter control high register (ADCCRH)
- A/D converter control low register (ADCCRL)
- A/D converter data high register (ADCDRH)
- A/D converter data low register (ADCDRL)

2.4.14.1 Block Diagram

Figure 21. 12-Bit ADC Block Diagram

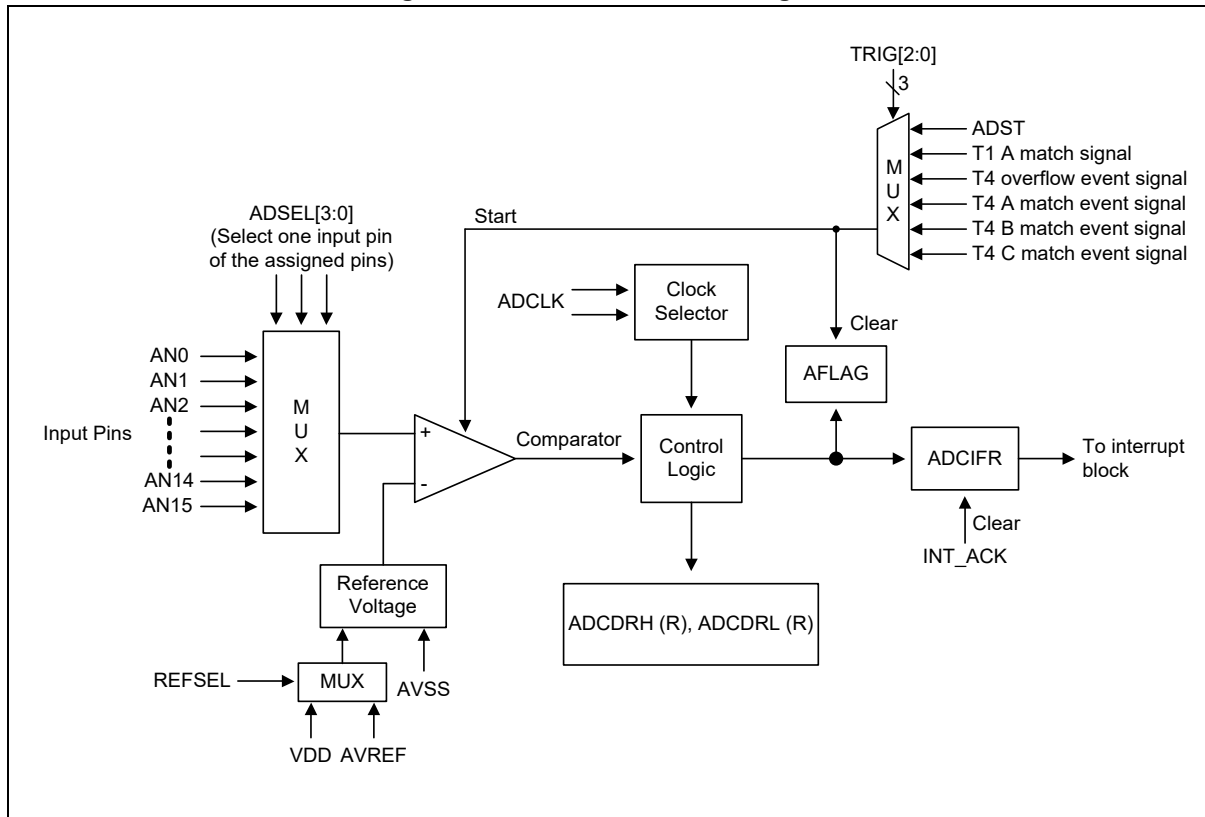


Figure 22. AD Analog Input Pin with Capacitor

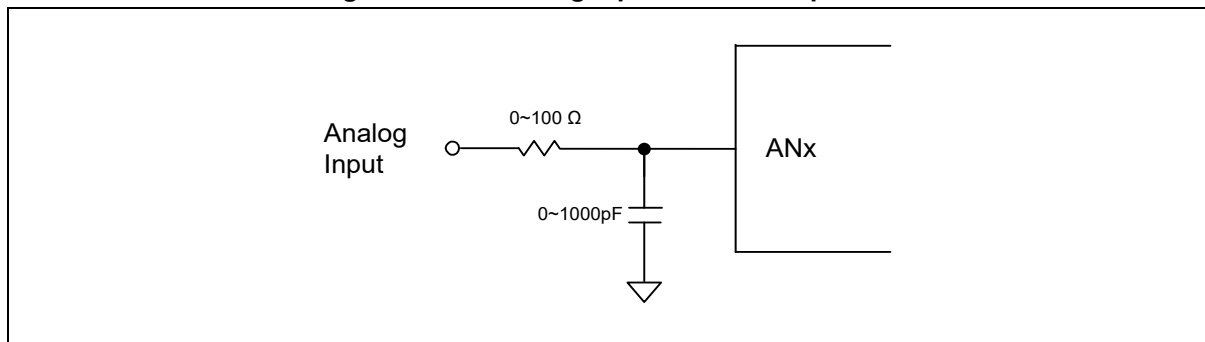
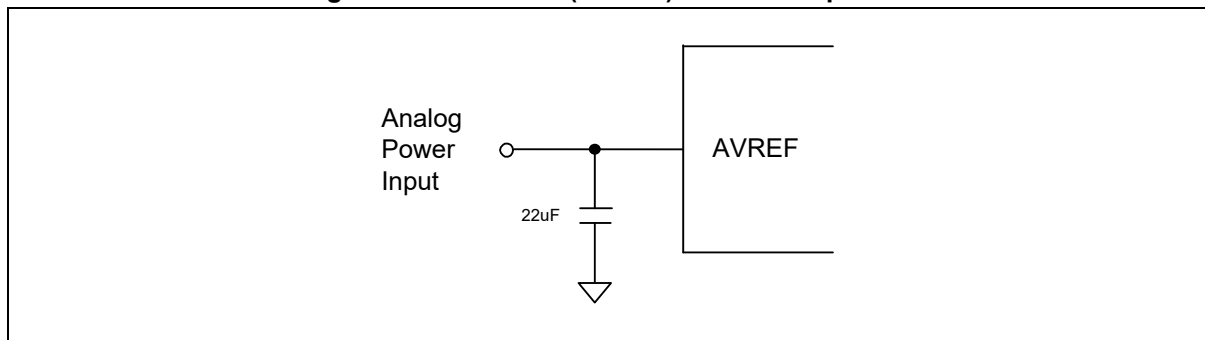


Figure 23. AD Power (AVREF) Pin with Capacitor

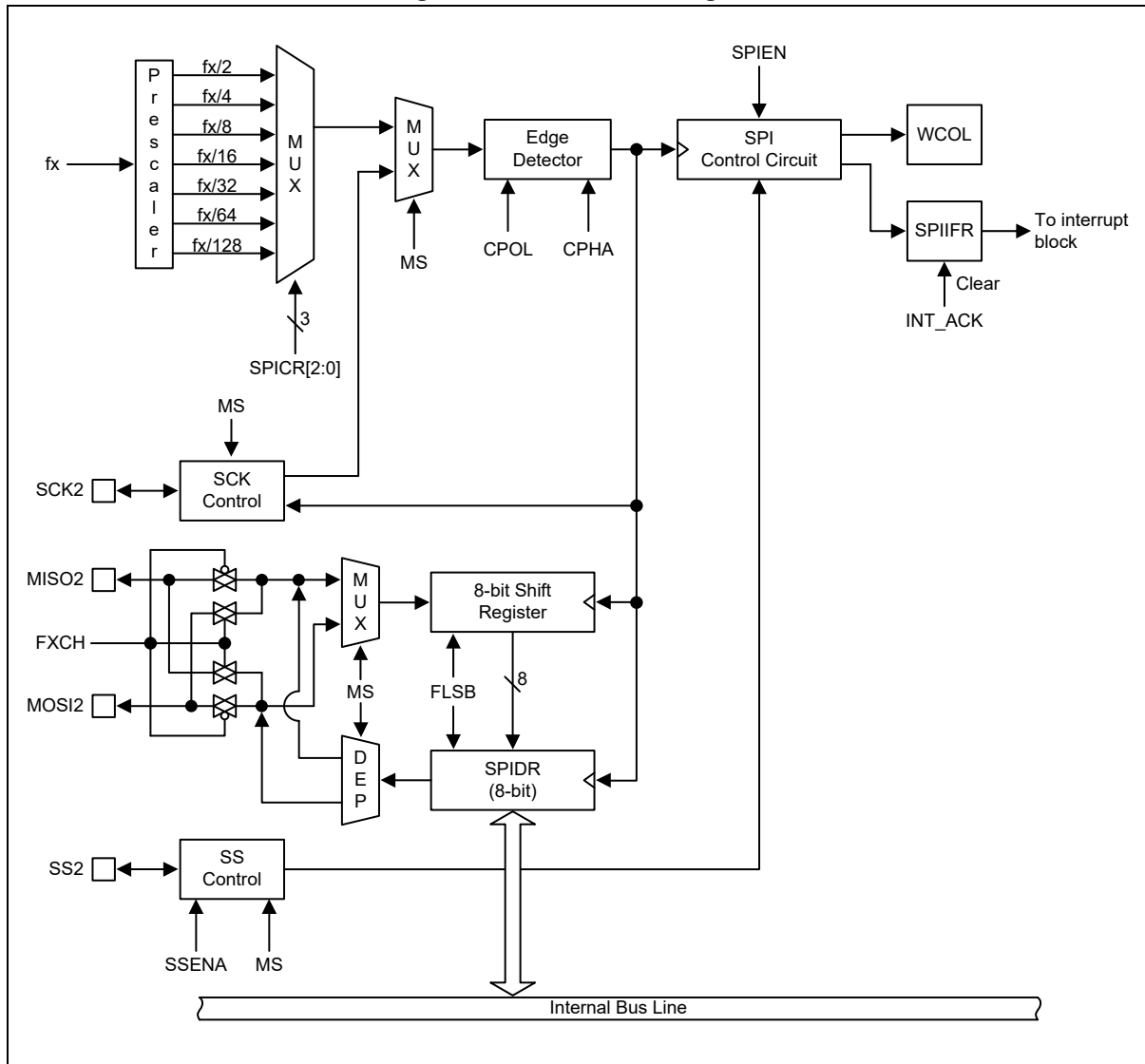


2.4.15 Serial Peripheral Interface (SPI) 2

There is a Serial Peripheral Interface (SPI) channel in MC96F6432P. The SPI allows synchronous serial data transfer between the external serial devices. It can do Full-duplex communication by 4-wire (MOSI, MISO, SCK, SS) and support master/slave mode. In addition, it can select serial clock (SCK) polarity, phase, and whether to transfer the LSB first data or the MSB first data.

2.4.15.1 Block Diagram

Figure 24. SPI 2 Block Diagram



2.4.16 UART + SPI + I2C (USI 0/1)

The USI is an acronym of USART, SPI and I2C. The MC96F6432A has two USI function blocks, USI0 and USI1 that are of the same functionality. Each USI consists of USI control register 1/2/3/4, USI status register 1/2, USI baud-rate generation register, USI data register, USI SDA hold time register, USI SCL high period register, USI SCL low period register and USI slave address register (USInCR1, USInCR2, USInCR3, USInCR4, USInST1, USInST2, USInBD, USInDR, USInSDHR, USInSCHR, USInSCLR, USInSAR) n is 0 or 1.

The operation mode is selected by the operation mode of USIn selection bits (USInMS[1:0]).

USI 0/1 operates in one of four operating modes:

- Asynchronous mode (UART)
- Synchronous mode (USART)
- SPI mode
- I2C mode

2.4.16.1 Block Diagram

Figure 25. UART Block Diagram (Where n = 0 and 1)

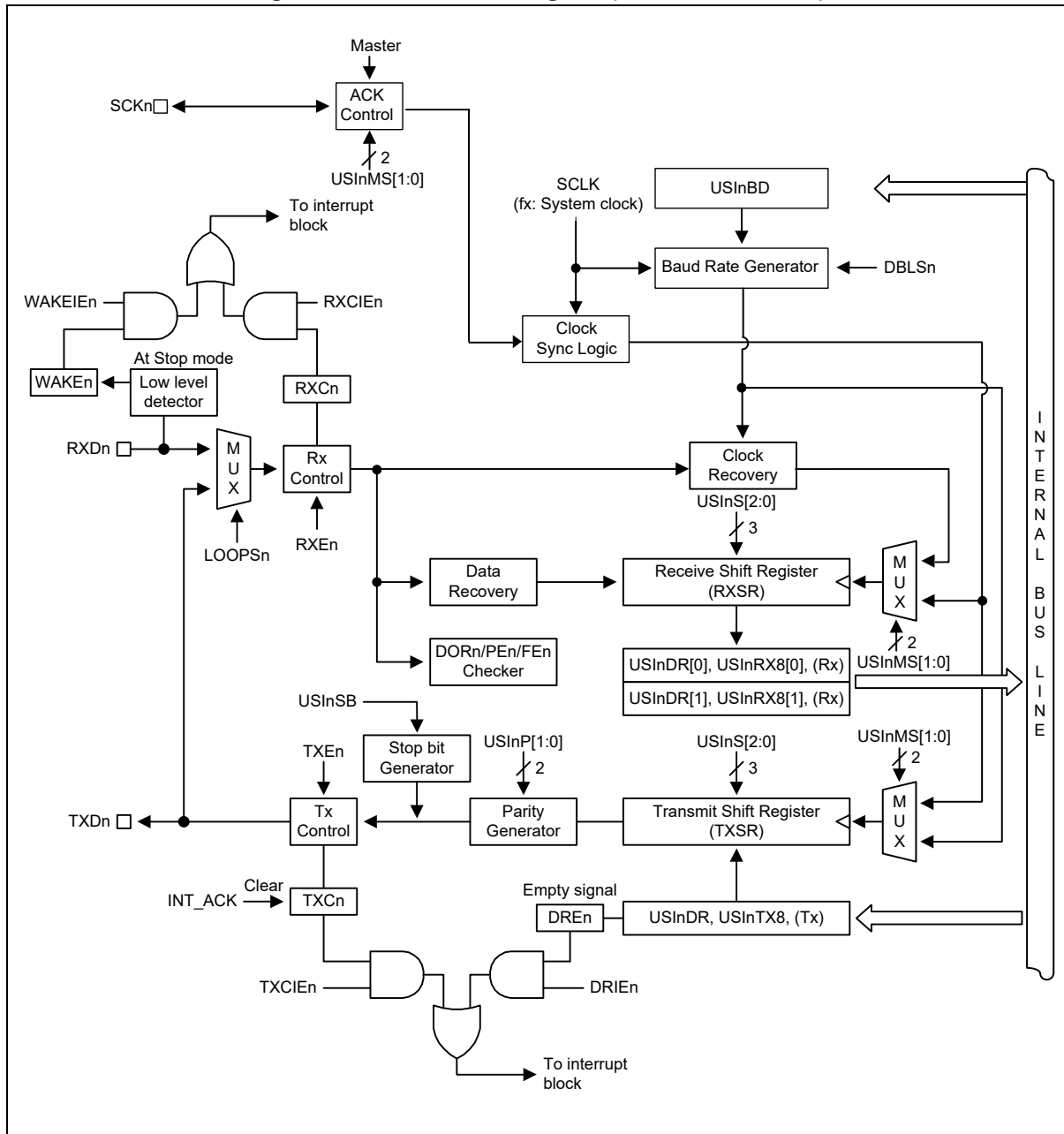


Figure 26. SPI Block Diagram (Where n = 0 and 1)

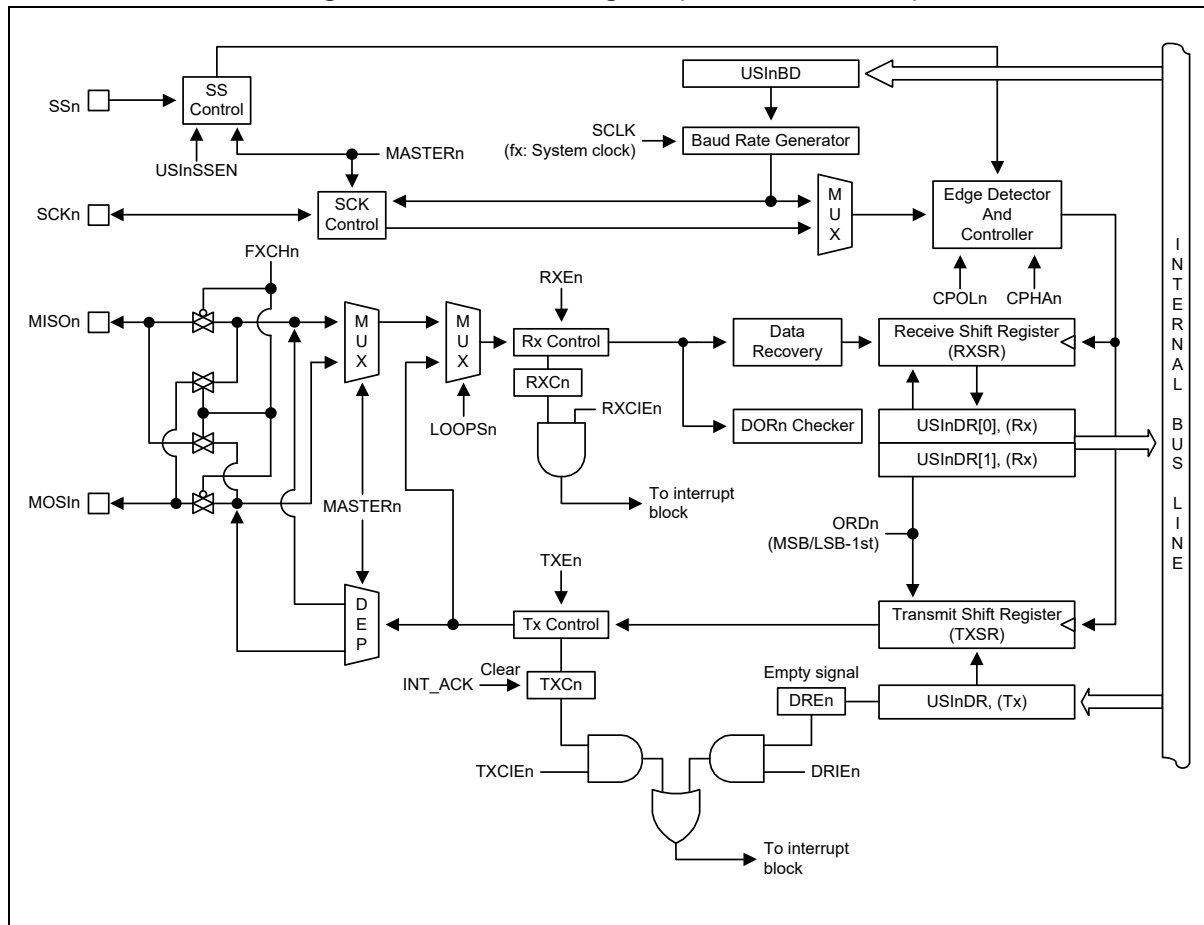
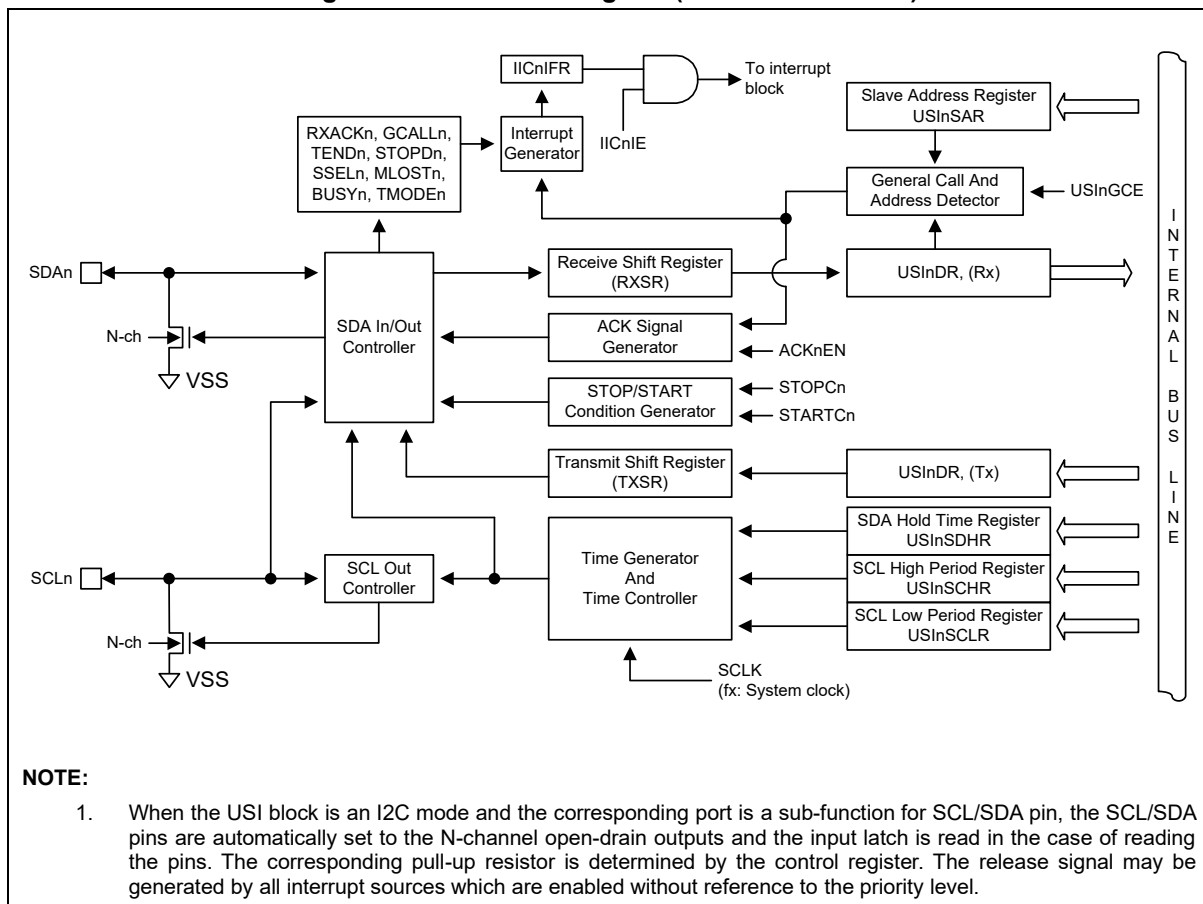


Figure 27. I2C Block Diagram (Where n = 0 and 1)



2.4.17 UART 2

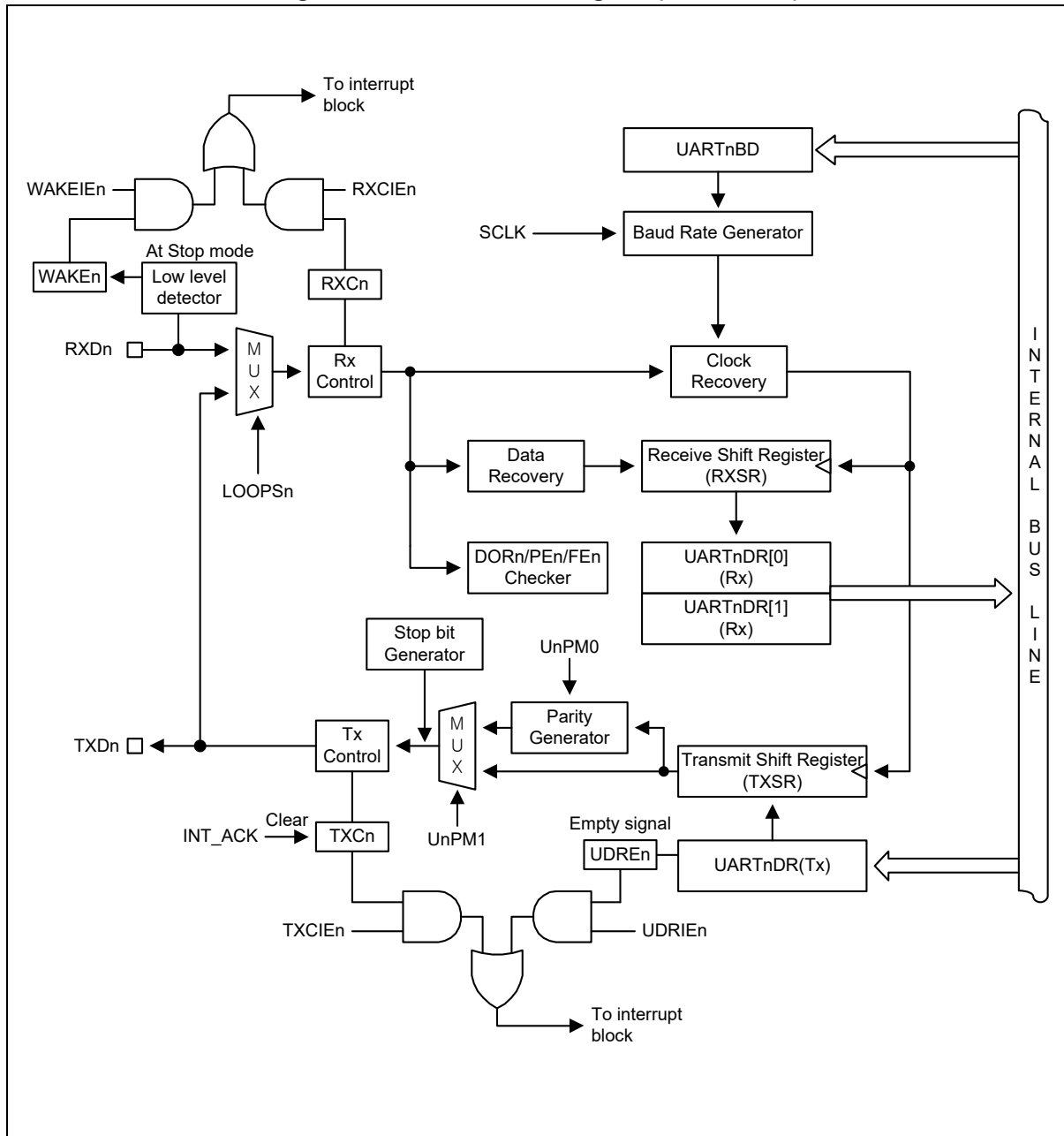
The MC96F6432P has built-in 1-channel of UART module (Universal Asynchronous Receiver/Transmitter).

The UART 2 of the MC96F6432P features the following:

- Full-duplex and half-duplex operations
- Baud rate generator
- Supports serial frames with 5,6,7, or 8 Data bits and 1 or 2 Stop bits
- Odd or even parity generation, and parity check supported by hardware
- Data OverRun Detection
- Framing Error Detection
- Double speed Asynchronous communication mode

2.4.17.1 Block Diagram

Figure 28. UART 2 Block Diagram (where n = 2)



2.4.18 Flash CRC and Checksum Generator

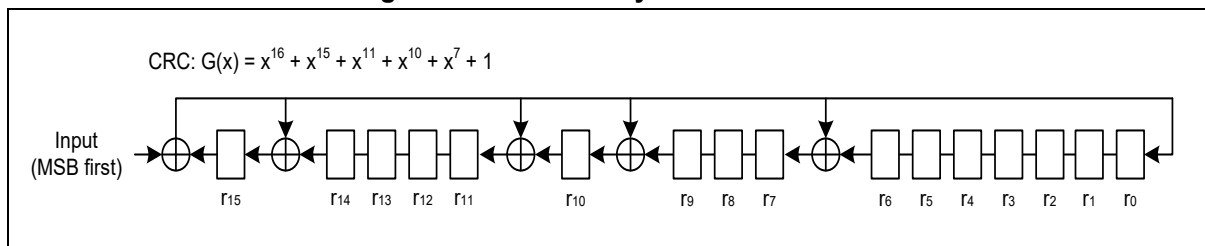
Flash CRC (Cyclic Redundancy Check) generator of MC96F6432P generates 16-bit CRC code bits from Flash and a polynomial generator. The CRC code for each input data frame is appended to the frame.

Specifically, CRC-based technique is used to verify data transmission or storage integrity. In the scope of the functional safety standards, this technique offers a means of verifying the Flash memory integrity. The Flash CRC generator helps compute a signature of software during runtime, to be compared with a reference signature.

The CRC generator has the following features:

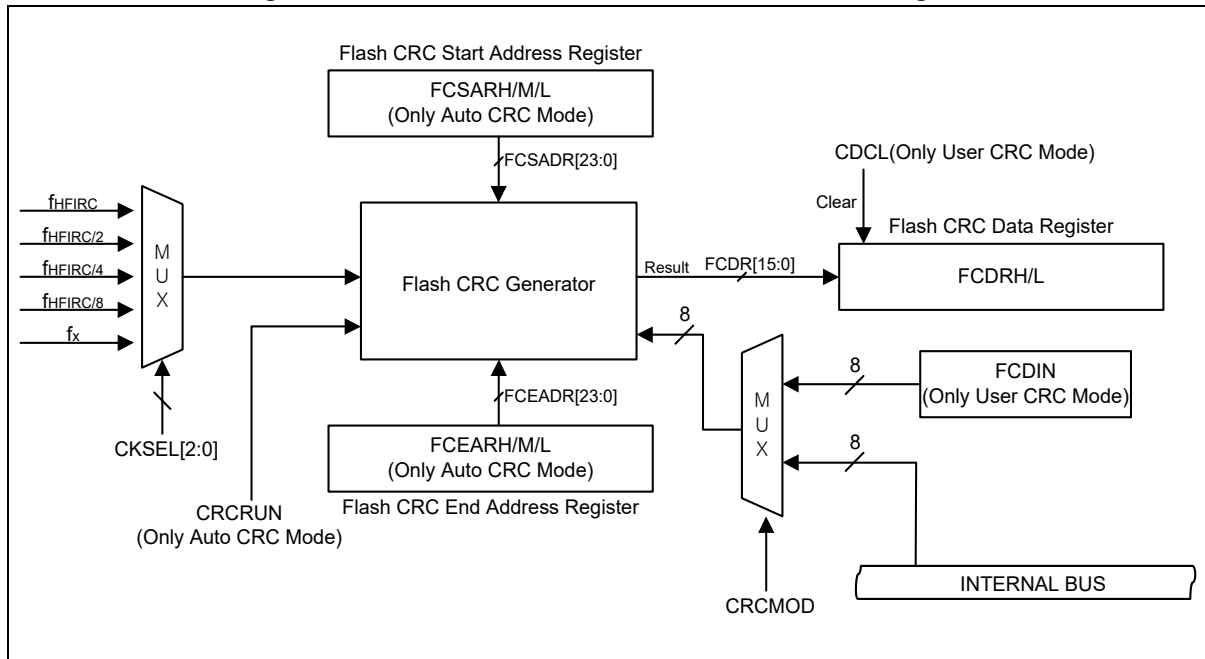
- Auto CRC and User CRC Mode
- CRC Clock: f_{IRC} , $f_{IRC}/2$, $f_{IRC}/4$, $f_{IRC}/8$ and f_x (System clock)
- CRC-16 polynomial: 0x8C81 ($X^{16} + X^{15} + X^{11} + X^{10} + X^7 + 1$)

Figure 29. CRC-16 Polynomial Structure



2.4.18.1 Block Diagram

Figure 30. Flash CRC/Checksum Generator Block Diagram



2.4.19 Power Down Operation

MC96F6432P offers two power-down modes to minimize power consumption of itself. Programs under the two power saving modes IDLE and STOP, are stopped and power consumption is reduced considerably.

2.4.19.1 Peripheral Operation in IDLE/STOP Mode

Peripheral's operations during IDLE mode and STOP mode are described in Table 15.

Table 15. Peripheral Operation During Power-Down Mode

Peripheral	IDLE mode	STOP mode
CPU	ALL CPU Operation are Disable	ALL CPU Operation are Disable
RAM	Retain	Retain
Basic Interval Timer	Operates Continuously	Stop
Watchdog Timer	Operates Continuously	Stop (Can be operated with WDTRC OSC)
Watch Timer	Operates Continuously	Stop (Can be operated with sub clock)
Timer0~4	Operates Continuously	Halted (Only when the Event Counter Mode is Enabled, Timer operates Normally)
ADC	Operates Continuously	Stop
BUZ	Operates Continuously	Stop
SPI	Operates Continuously	Only operate with external clock
USI0/1	Operates Continuously	Only operate with external clock
UART	Operates Continuously	Stop
Internal OSC (16MHz)	Oscillation	Stop when the system clock (fx) is fIRC
WDTRC OSC (5kHz)	Can be operated with setting value	Can be operated with setting value
Main OSC (0.4~8.5MHz)	Oscillation	Stop when $fx = f_{XIN}$
Sub OSC (32.768kHz)	Oscillation	Stop when $fx = f_{SUB}$
I/O Port	Retain	Retain
Control Register	Retain	Retain
Address Data Bus	Retain	Retain
Release Method	By RESET, all Interrupts	By RESET, Timer Interrupt (EC0, EC1, EC3), SPI (External clock), External Interrupt, UART by RX, WT (sub clock), WDT

2.4.20 Reset

When a reset event occurs, an internal register is selected to be initialized in accordance with a reset value. Each reset value described in Table 16 indicates a corresponding On-Chip Hardware that is to be initialized.

Table 16. Reset Value and the Relevant On-Chip Hardware

On-Chip Hardware	Reset Value
Program Counter (PC)	0000H
Accumulator	00H
Stack Pointer (SP)	07H
Peripheral clock	On
Control register	Refer to peripheral registers.

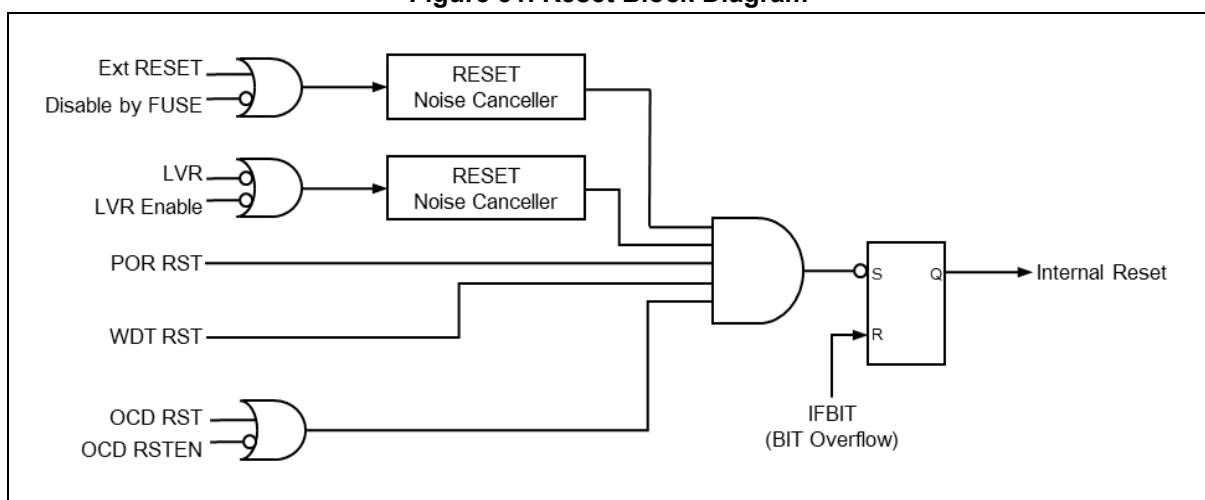
MC96F6432P has 5 types of reset sources as listed in the following:

- External RESETB
- Power On RESET (POR)
- WDT overflow reset (in a case of WDTEN='1')
- Low voltage reset (in a case of LVREN='0')
- OCD RESET

2.4.20.1 Block Diagram

Figure 31 shows a reset block of MC96F6432P.

Figure 31. Reset Block Diagram



2.4.21 Flash Memory

MC96F6432P incorporates Flash memory inside. Program can be written, erased, and overwritten on the Flash memory while it is mounted on a board. The Flash memory can be read by 'MOVC' instruction and programmed in OCD, serial ISP mode or user program mode.

The following are the main features of Flash memory:

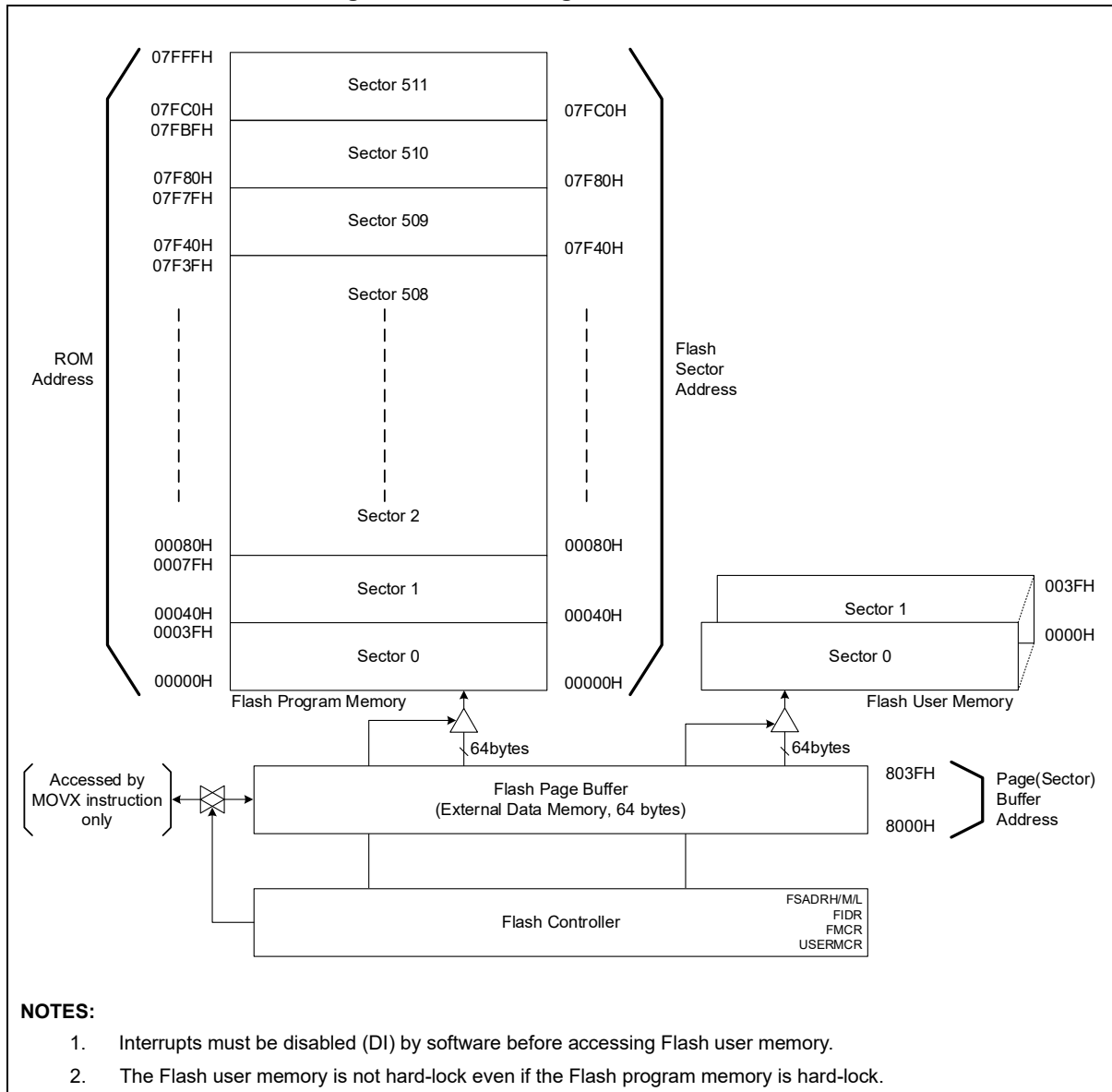
- Flash Size: 32 KB
- Single power supply program and erase
- Command interface for fast program and erase operation
- Minimum 10,000 (Sector 0~507)/100,000 (508~511) program/erase cycles at typical voltage and temperature for Flash memory

NOTE:

1. Interrupts must be disabled (DI) by software before accessing Flash user memory.

2.4.21.1 Flash Program ROM Structure

Figure 32. Flash Program ROM Structure



2.5 Development Tools

This chapter describes wide range of development tools for MC96F6432P. ABOV offers software tools, debuggers, and programmers to help a user in generating right results to match target applications. ABOV supports the entire development ecosystem of the customers.

2.5.1 Compiler

ABOV semiconductor does not provide any compiler for MC96F6432P. However, since MC96F6432P has M8051 as its CPU core, users can use all kinds of third party's standard 8051 compilers such as Keil C Compiler. These compilers' output debug information can be integrated with our OCD emulator and debugger. Refer to our website www.abovsemi.com for more information regarding the OCD emulator and debugger.

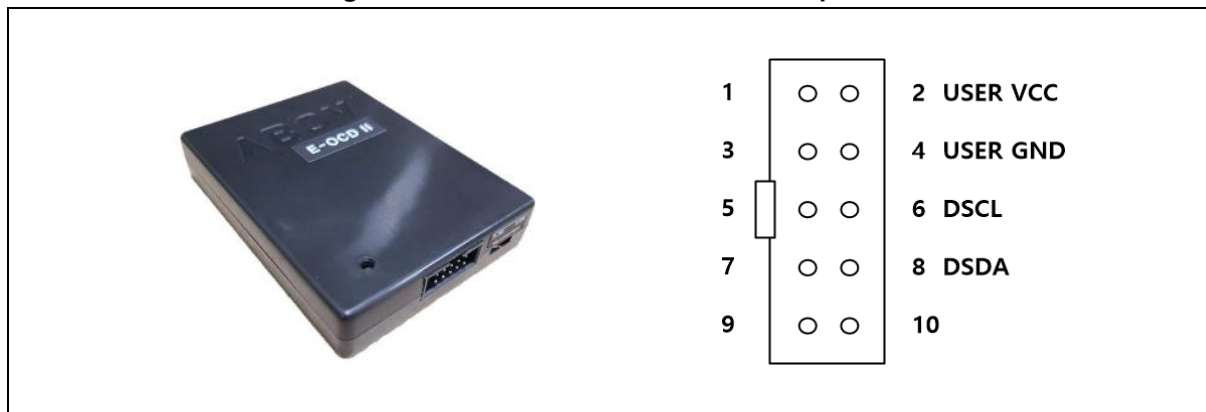
2.5.2 E-OCD II Interface and OCD Debugger

The E-OCD II interface supports ABOV Semiconductor's 8051 series microcontroller emulation. It uses two wires to interface between the host computer and the microcontroller, which is attached to the target system. The E-OCD II can read or change the value of the microcontroller's internal memory and I/O peripherals. In addition, it controls the microcontroller's internal debugging logic. This means E-OCD II controls emulation, step run, monitoring, and many more functions regarding debugging.

The OCD debugger program runs underneath MS operating systems such as MS Windows NT/ 2000/ XP/Vista/7/8/8.1/10/11 (32-bit, 64-bit).

Programming information using the E-OCD II is provided in the section 2.5.4 On-Chip Debug System. For more detailed information about the E-OCD II, refer to our website www.abovsemi.com and download the debugger software and documents.

Figure 33. E-OCD II and OCD Pin Descriptions



The following are the OCD mode connections:

- DSCL (MC96F6432P P01 port)
- DSDA (MC96F6432P P00 port)

2.5.3 Programmer

2.5.3.1 E-PGM+ and E-PGM Serial

The E-PGM+ and E-PGM Serial are standalone programmers, which allows users to program on the device directly.

- Supports for all ABOV microcontroller devices
- A dedicated tool for mass production
- 40-pin Textool DIP socket for single-chip programming (E-PGM+ only)
- 10-pin connector for ISP mode
- USB host interface
- HEX downloads and controls

Figure 34. E-PGM+ (Single Writer) and Pin Descriptions



2.5.3.2 Gang Programmer

E-Gang4 and E-Gang6 allows a user to program on multiple devices at a time. They run not only in host-controlled mode but also in standalone mode without host control. USB interface is available, and it is easy to connect to the handler.

Table 17. Specification of E-Gang4 and E-Gang6

Gang Programmer	E-Gang4	E-Gang6
Dimension (x, y, h)	33.5 x 22.5 x 35 mm	148.2 x 22.5 x 35 mm
Weight	2.0 kg	2.8 kg
Input voltage	DC Adaptor 15 V/2 A	DC Adaptor 15 V/2 A
Operating temperature	-10°C to 40°C	-10°C to 40°C
Storage temperature	-30°C to 80°C	-30°C to 80°C
Waterproof	No	No

Figure 35. E-Gang4 and E-Gang6 (for Mass Production)



2.5.3.3 MTP Programming

Program memory of MC96F6432P is an MTP Type. This Flash is accessed through four pins such as DSCL, DSDA, VDD, and VSS in serial data format.

Table 18 describes each pin and corresponding I/O status.

Table 18. Pins for MTP Programming

Pin Name	Main Chip Pin Name	During Programming	
		I/O	Description
DSCL	P01	I	Serial clock pin. Input only pin.
DSDA	P00	I/O	Serial data pin. Output port when reading and input port when programming. Can be assigned as input/push-pull output port.
VDD, VSS	VDD, VSS	-	Logic power supply pin.

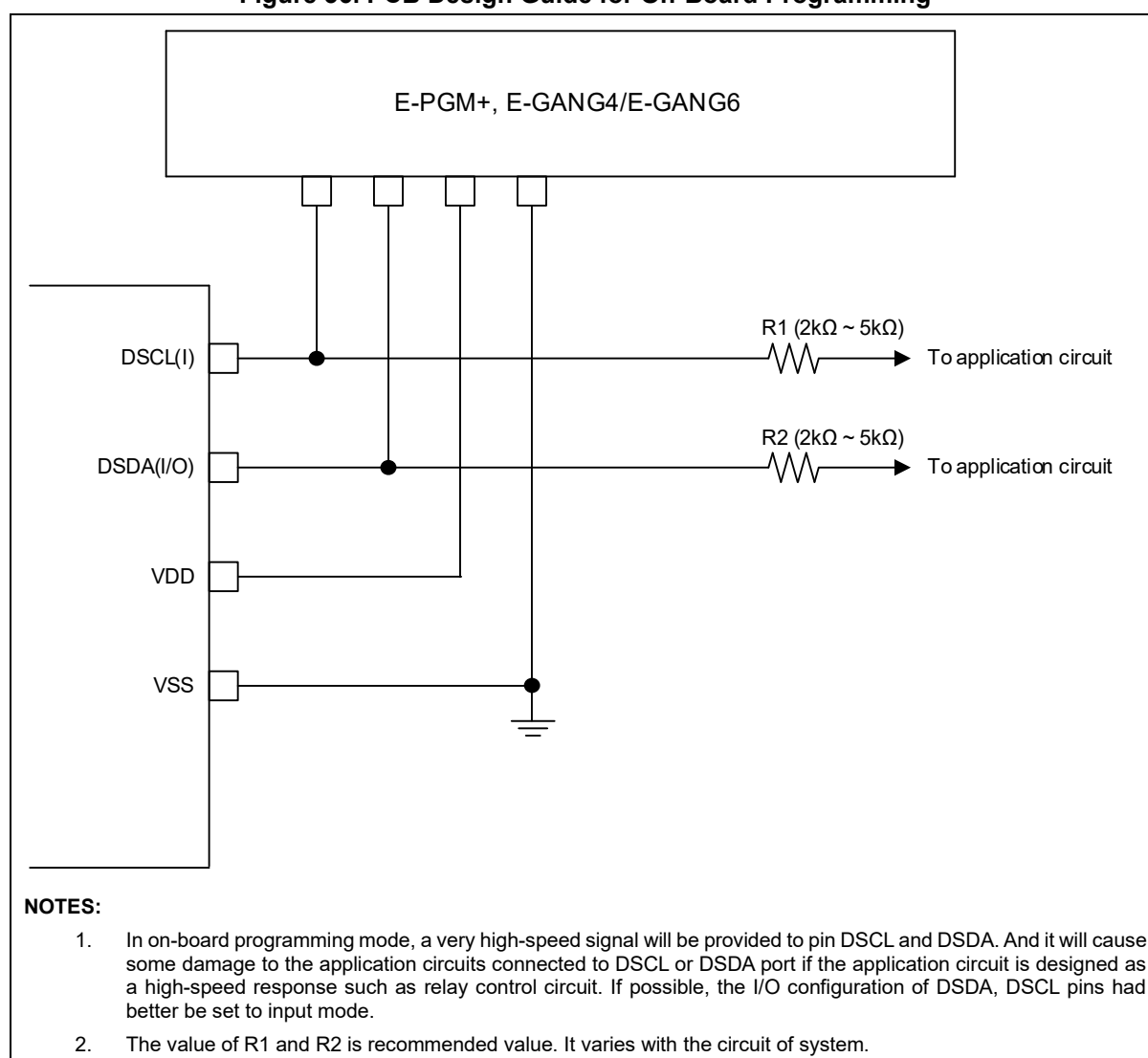
2.5.3.4 On-Board Programming

The MC96F6432P needs only four signal lines including VDD and VSS pins for programming Flash with serial protocol. Therefore, the on-board programming is possible if the programming signal lines are considered when the PCB of application board is designed.

2.5.3.5 Circuit Design Guide

When programming Flash memory, the programming tool needs four signal lines, DSCL, DSDA, VDD, and VSS. When you design a PCB circuit, you should consider the usage of these four signal lines for the on-board programming.

Figure 36. PCB Design Guide for On-Board Programming



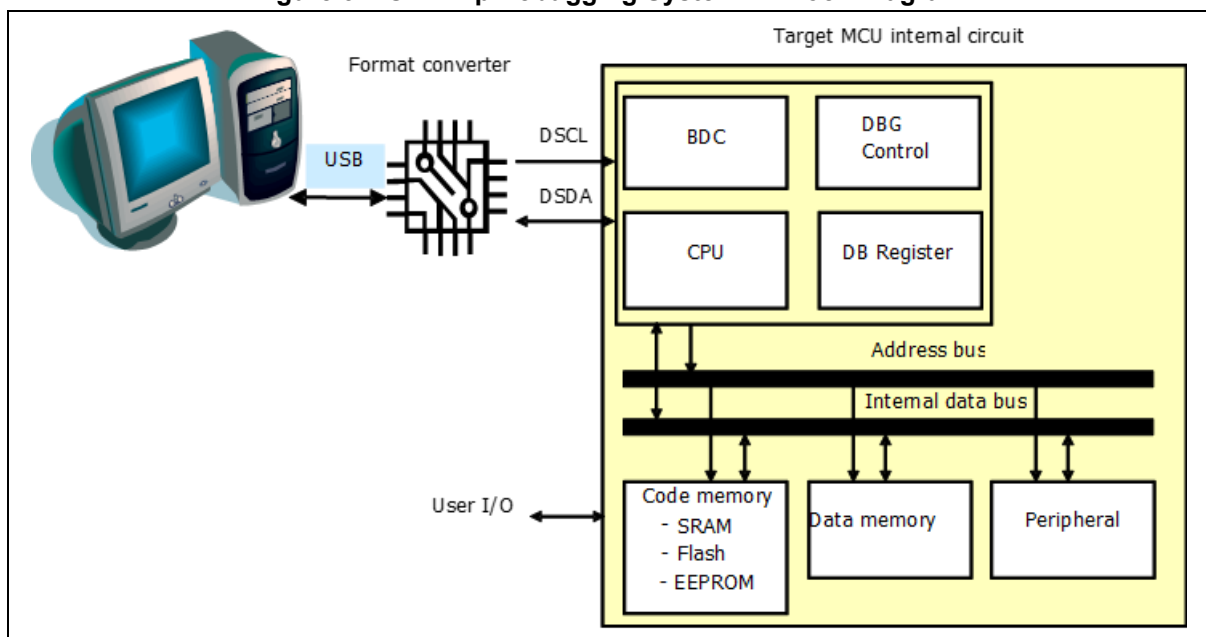
2.5.4 On-Chip Debug System

Detail descriptions for programming via the OCD interface can be found in the following figures. Table 19 describes features of OCD and Figure 37 shows a block diagram of the OCD interface and the On-chip Debug system.

Table 19. Features of OCD

Two wire external interface	• One for serial clock input • One for bi-directional serial data bus
Debugger accesses	• All internal peripherals • Internal data RAM • Program Counter • Flash memory and EEPROM memory
Extensive On-Chip Debugging Supports for Break Conditions	• Break instruction • Single step break • Program memory break points on single address • Programming of Flash, Data Flash, Fuses, and Lock bits through the two-wire interface • On-Chip Debugging supported by E-OCD-II.
Operating frequency	The maximum frequency of a target microcontroller

Figure 37. On-Chip Debugging System in Block Diagram

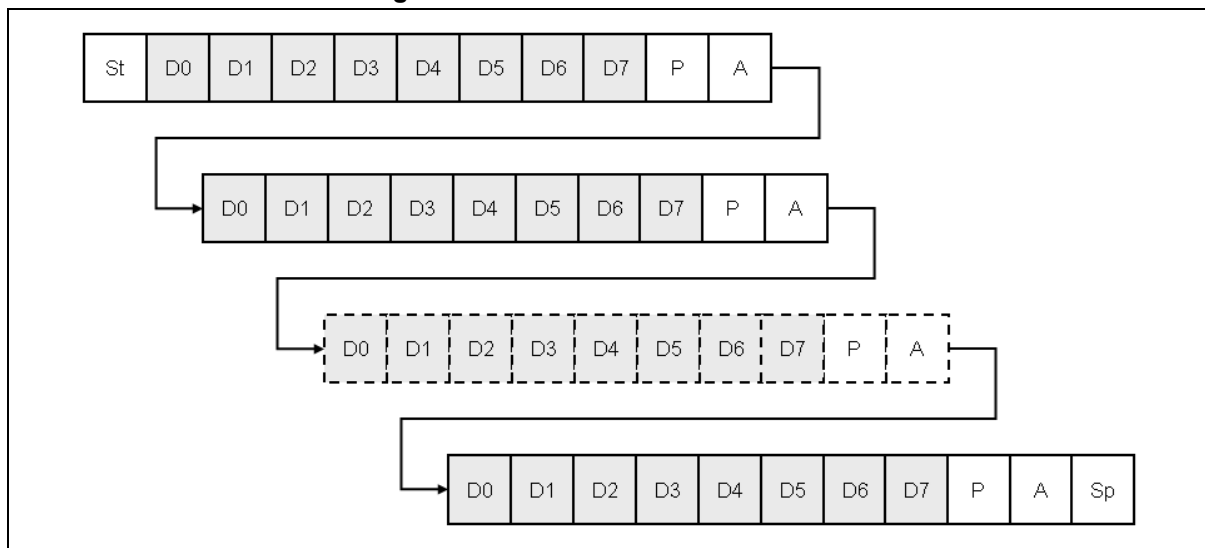


2.5.4.1 Two-Pin External Interface

Basic Transmission Packet

- 10-bit packet transmission using a two-pin interface.
- 1-packet consists of 8-bit data, 1-bit parity and 1-bit acknowledge.
- Parity is even of '1' for 8-bit data in transmitter.
- Receiver generates acknowledge bit as '0' when transmission for 8-bit data and its parity has no error.
- When transmitter has no acknowledge (Acknowledge bit is '1' at tenth clock), error process is executed in transmitter.
- When acknowledge error is generated, the host computer makes stop condition and transmits command which has error again.
- Background debugger command is composed of a bundle of packets.
- Start condition and stop condition notify the start and the stop of background debugger command respectively.

Figure 38. 10-Bit Transmission Packet



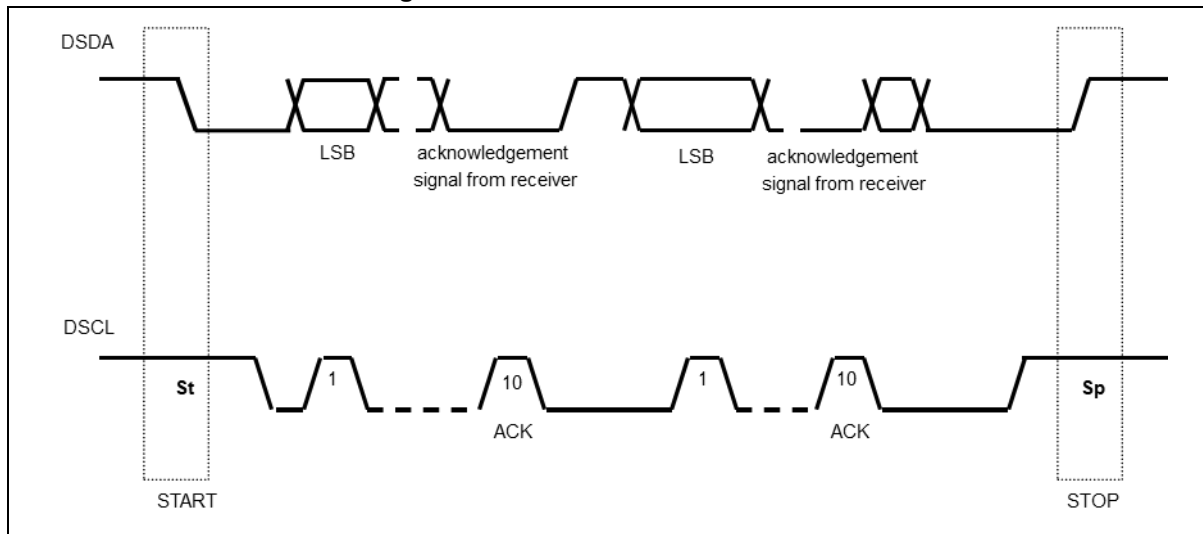
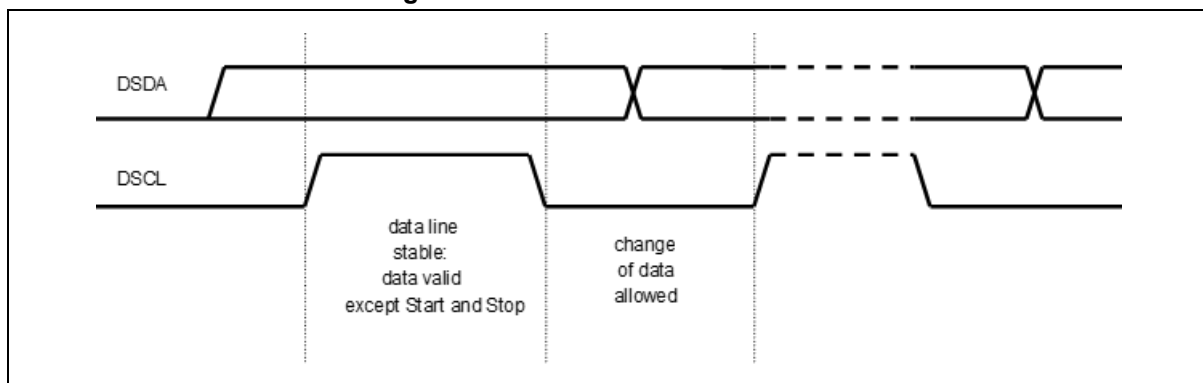
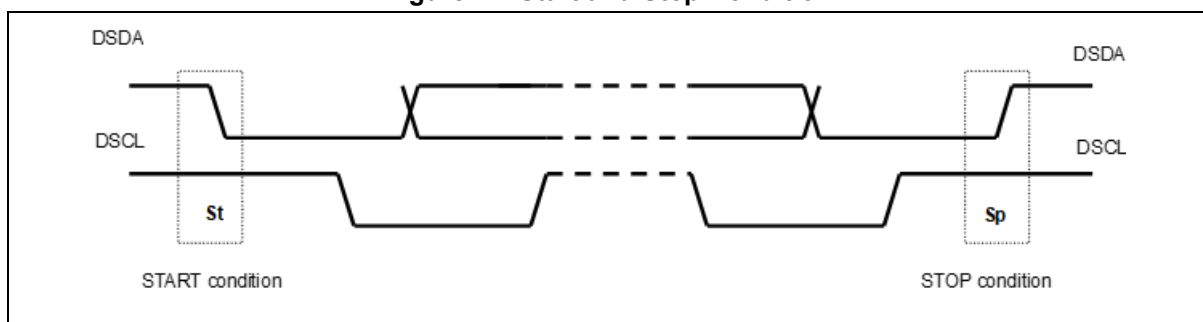
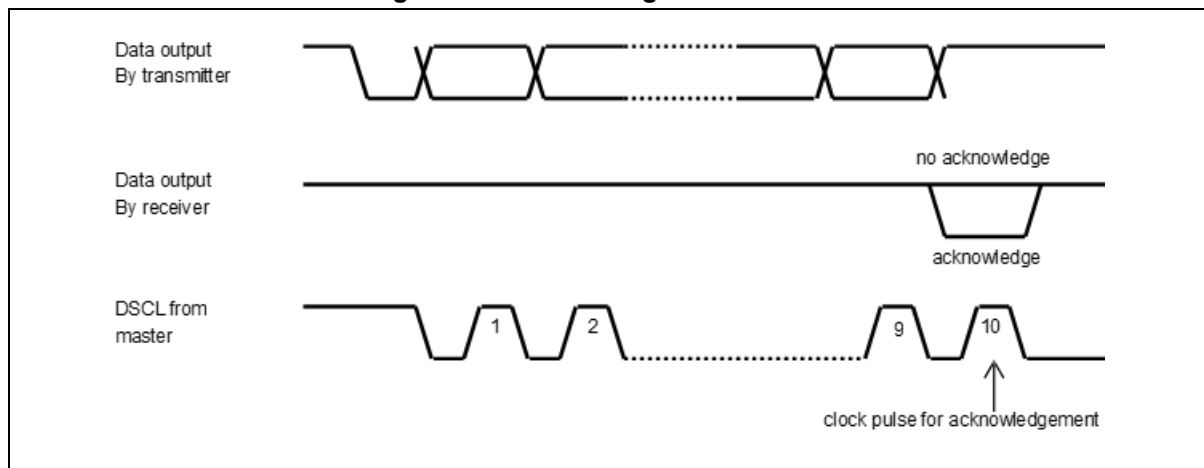
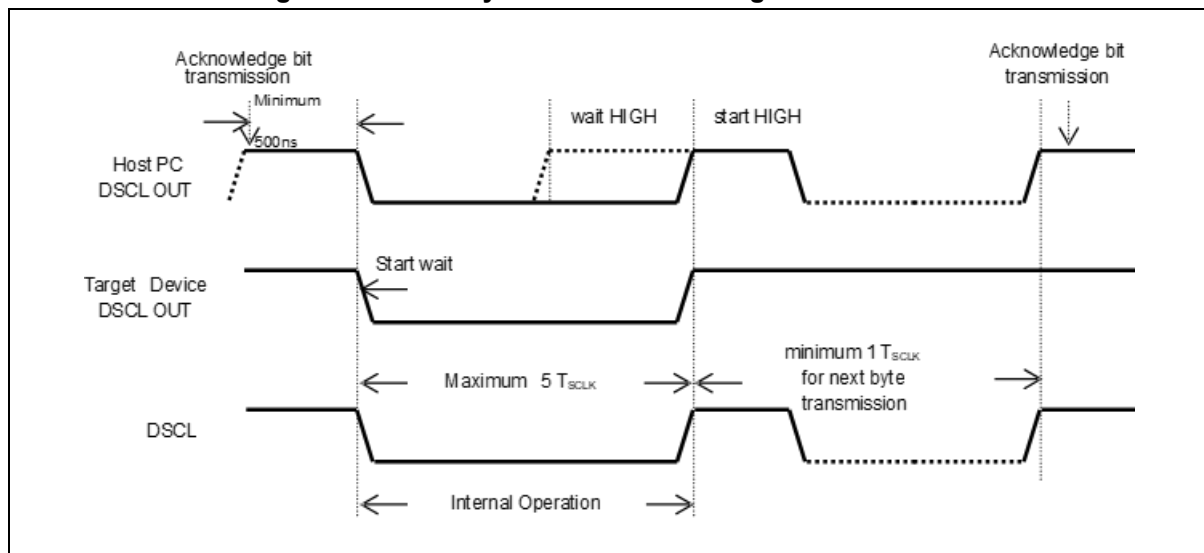
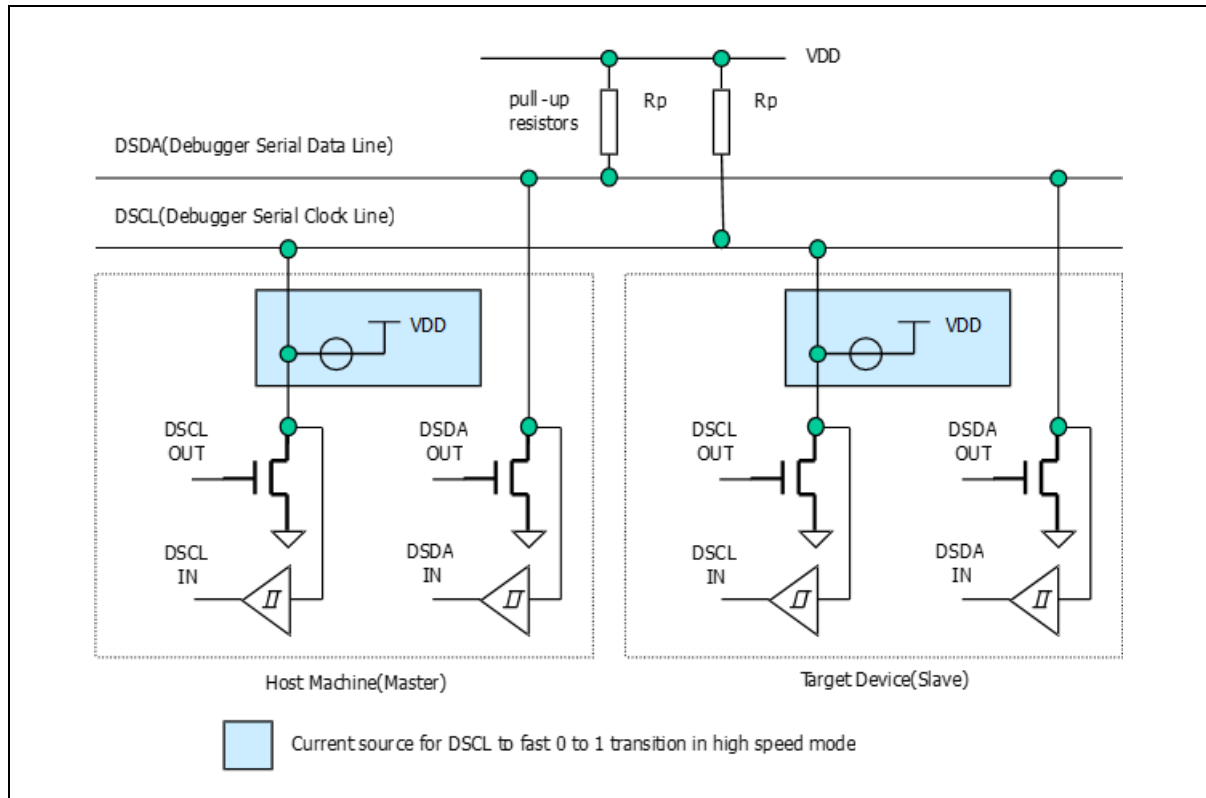
Packet Transmission Timing**Figure 39. Data Transfer on Twin Bus****Figure 40. Bit Transfer on Serial Bus****Figure 41. Start and Stop Condition**

Figure 42. Acknowledge on Serial Bus**Figure 43. Clock Synchronization During Wait Procedure**

2.5.4.2 Connection of Transmission

Two-pin interface connection uses open-drain (wire-AND bidirectional I/O).

Figure 44. Connection of Transmission



3. Pinouts and Pin Descriptions

In this chapter, MC96F6432P pinouts and pin descriptions are described.

3.1 Pinouts

Figure 45. MC96F6432PL 44-LQFP Pinouts

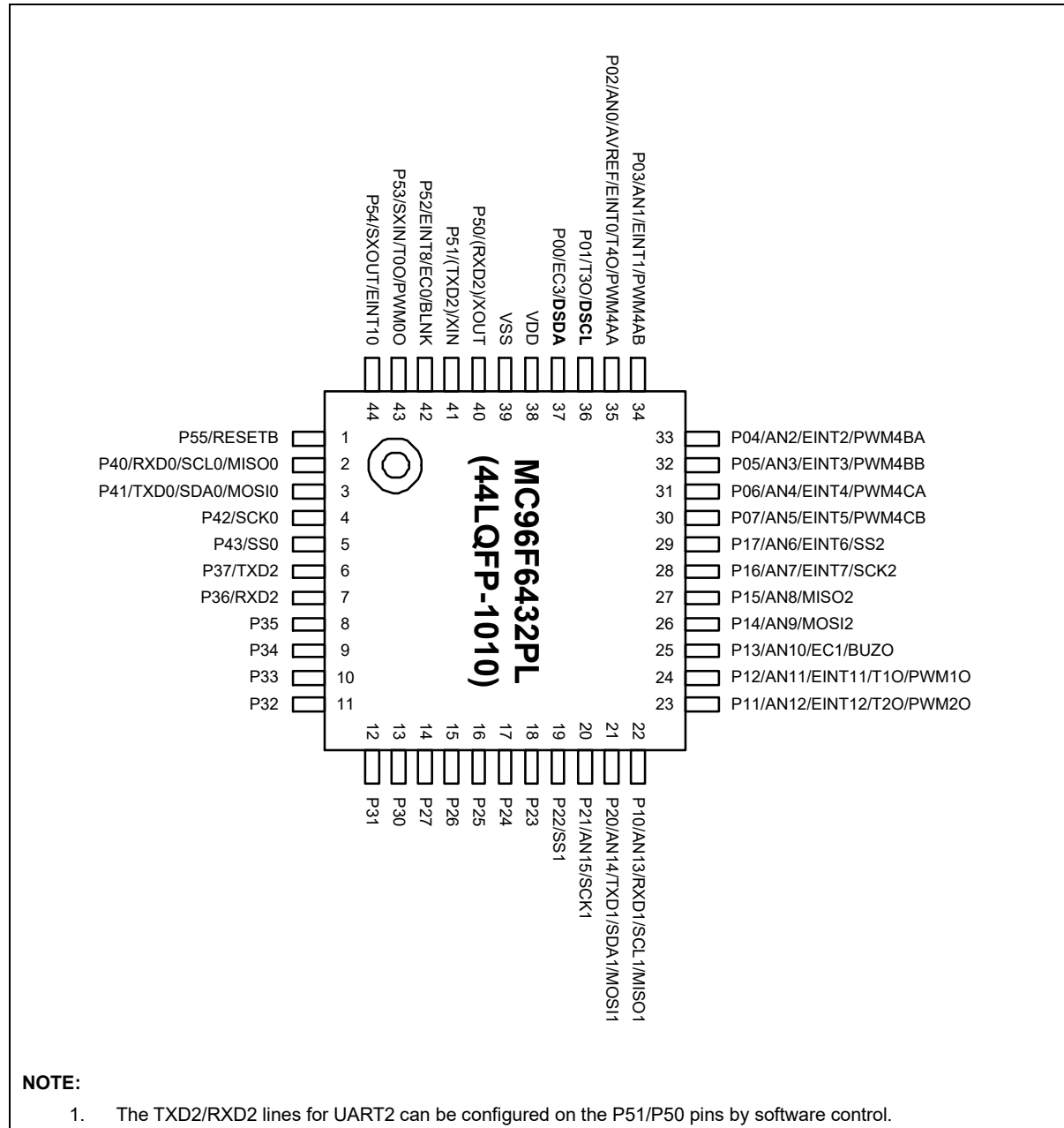
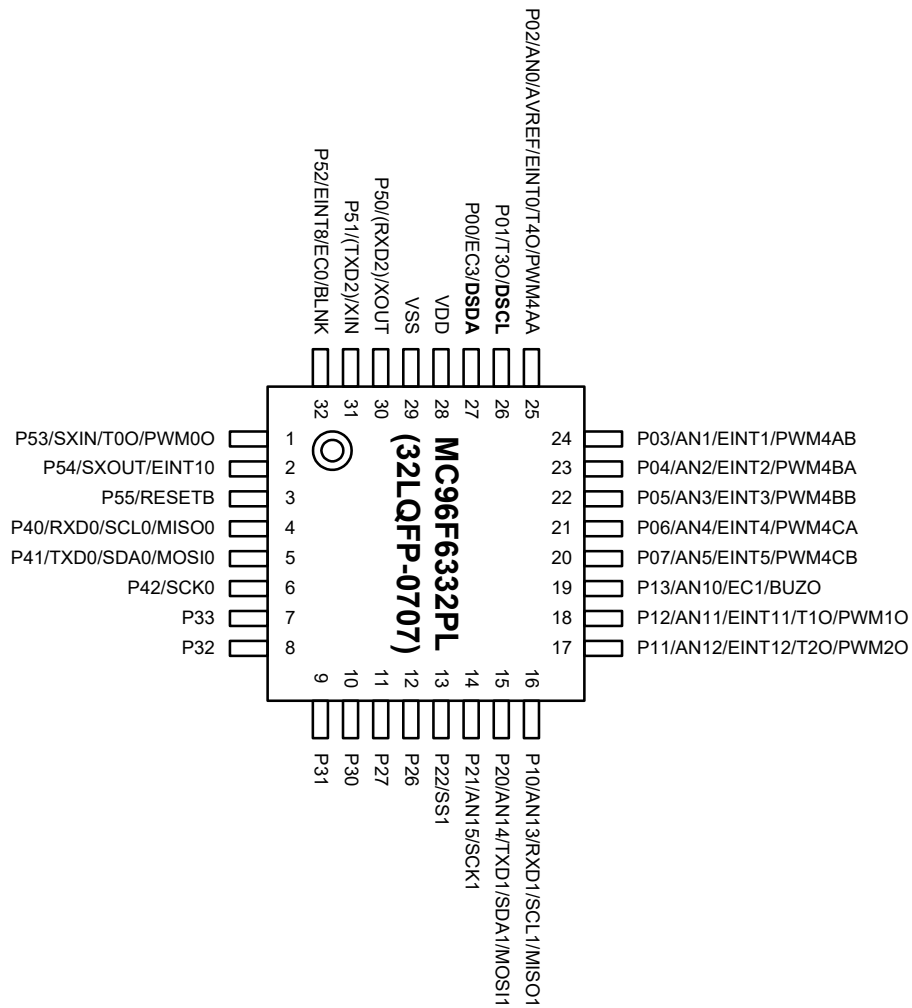


Figure 46. MC96F6332PL 32-LQFP Pinouts

**NOTES:**

1. The P14-P17, P23-P25, P34-P37, and P43 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 32-pin package is used.
2. The TXD2/RXD2 lines for UART2 can be configured on the P51/P50 pins by software control.

Figure 47. MC96F6332PD 32-SOP Pinouts

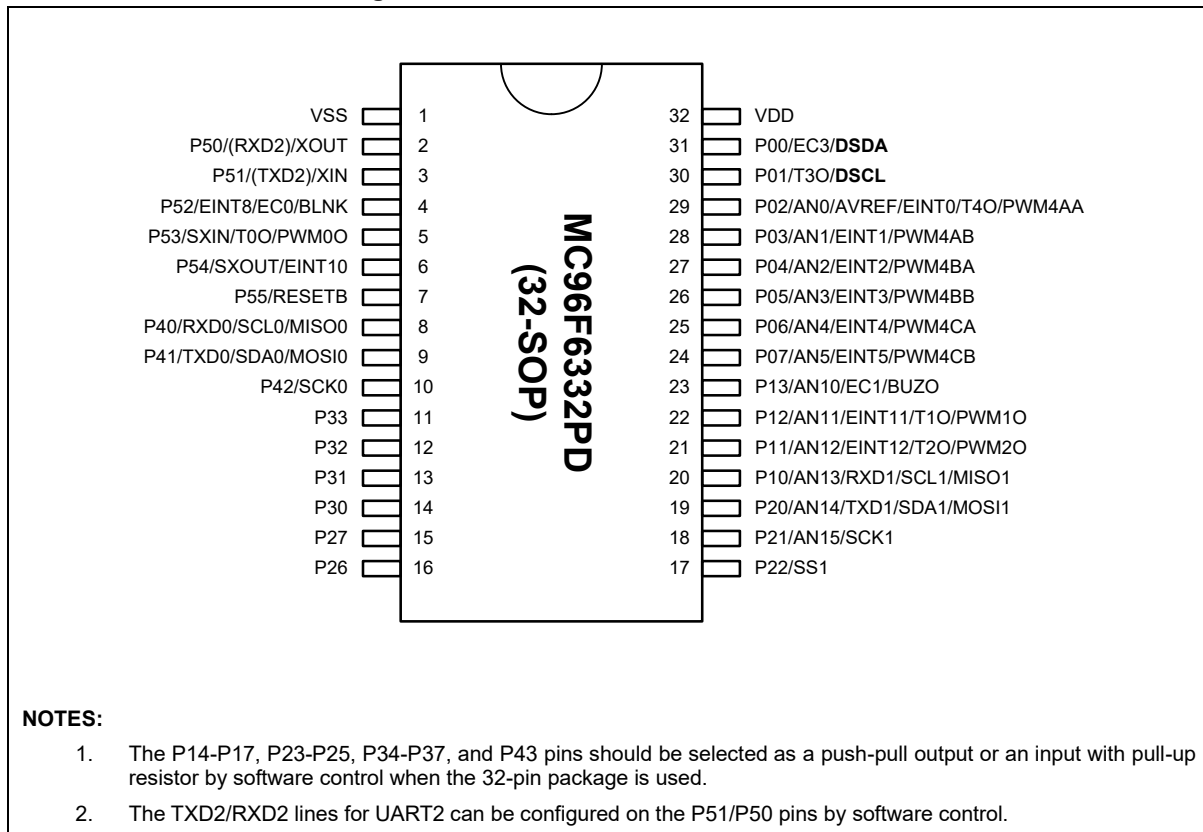


Figure 48. MC96F6332PM 28-SOP Pinouts

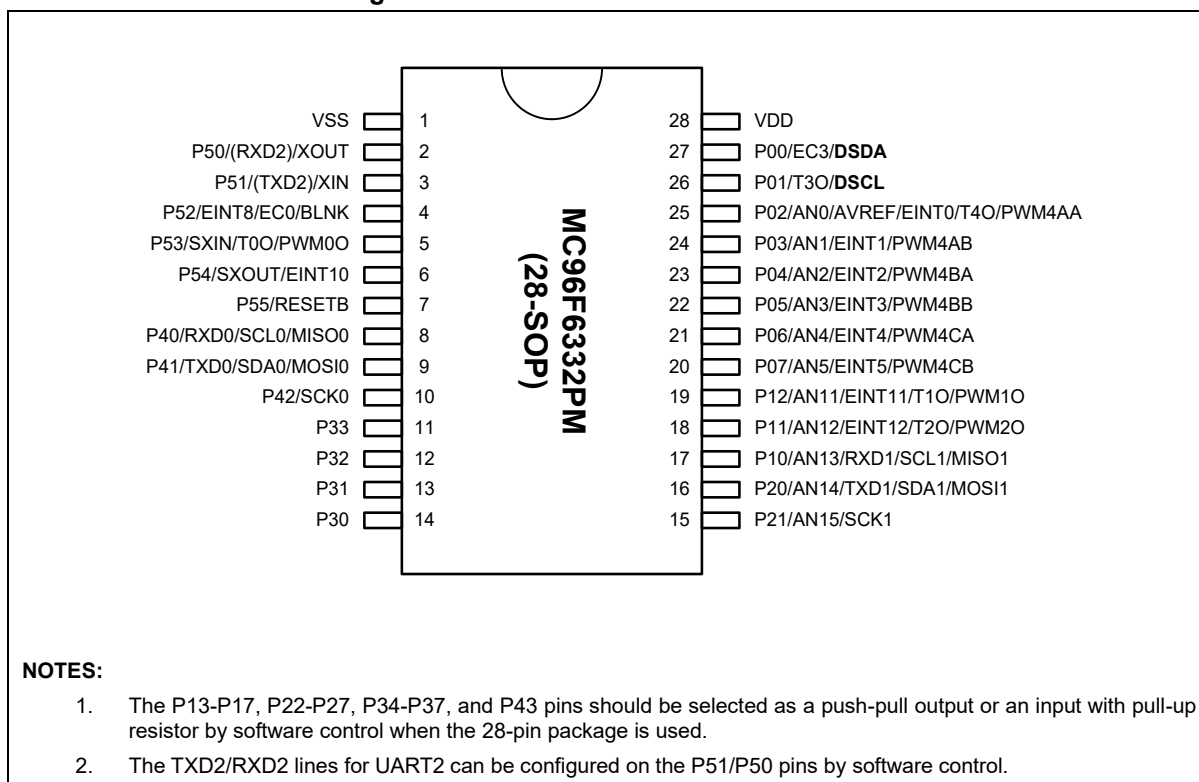


Figure 49. MC96F6332PR 28-TSSOP Pinouts

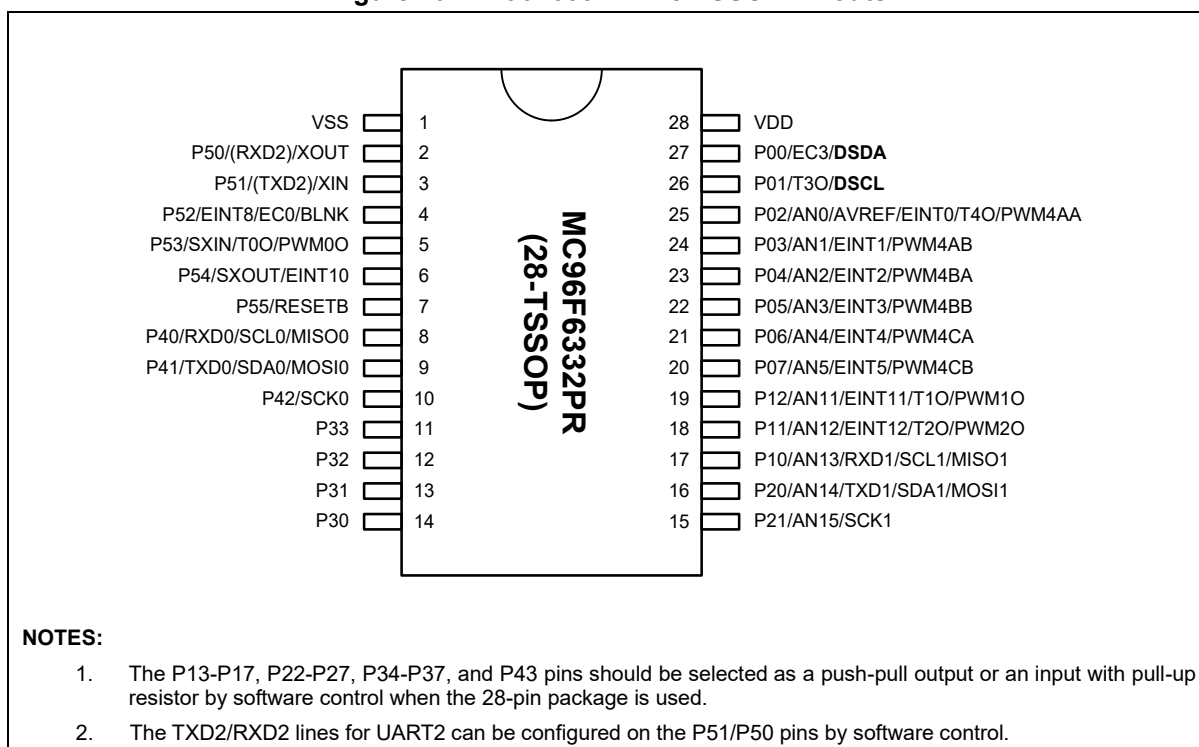
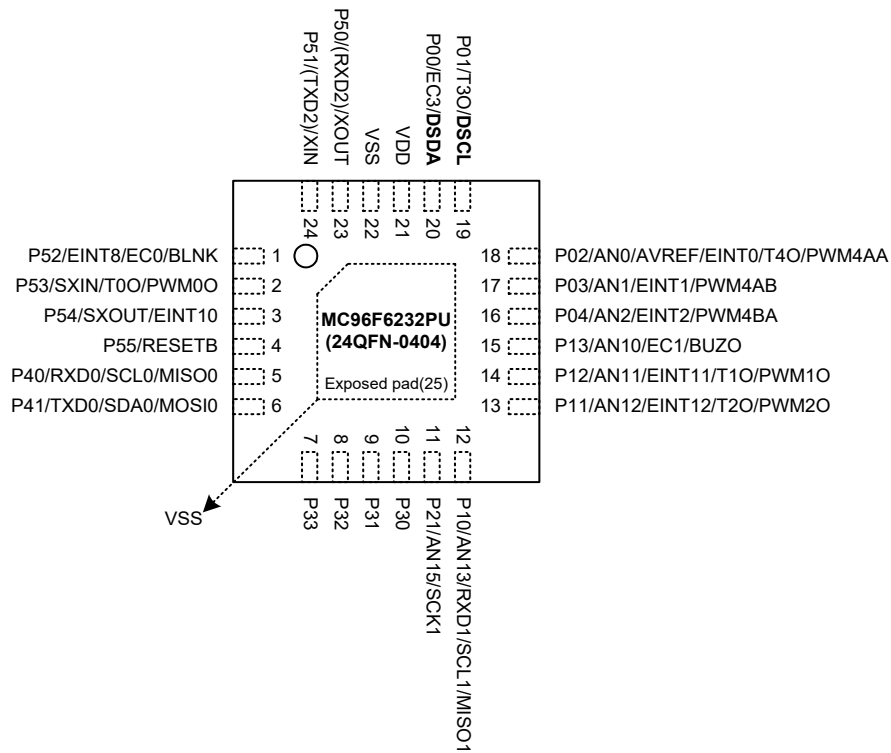


Figure 50. MC96F6232PU 24-QFN Pinouts**NOTES:**

1. The P05-P07, P14-P17, P20, P22-P27, P34-P37, and P42-P43 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 24-pin package is used.
2. The TXD2/RXD2 lines for UART2 can be configured on the P51/P50 pins by software control.

3.2 Pin Description

Table 20. Pin Description

Pin Name	I/O	Function	@Reset	Shared With
P00	I/O	Port 0 is a bit-programmable I/O port which can be configured as a Schmitt trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P05-P07 are not in the 24-Pin package.	Input	EC3/DSDA
P01				T3O/DSCL
P02				AN0/AVREF/EINT0/T4O/PWM4AA
P03				AN1/EINT1/PWM4AB
P04				AN2/EINT2/PWM4BA
P05				AN3/EINT3/PWM4BB
P06				AN4/EINT4/PWM4CA
P07				AN5/EINT5/PWM4CB
P10	I/O	Port 1 is a bit-programmable I/O port which can be configured as a Schmitt trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P14-P17 are not in the 32-Pin package. The P13-P17 are not in the 28-Pin package. The P14-P17 are not in the 24-Pin package.	Input	AN13/RXD1/SCL1/MISO1
P11				AN12/EINT12/T2O/PWM2O
P12				AN11/EINT11/T1O/PWM1O
P13				AN10/EC1/BUZO
P14				AN9/MOSI2
P15				AN8/MISO2
P16				AN7/EINT7/SCK2
P17				AN6/EINT6/SS2
P20	I/O	Port 2 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P23-P25 are not in the 32-Pin package. The P22-P27 are not in the 28-Pin package. The P20, P22-P27 are not in the 24-Pin package.	Input	AN14/TXD1/SDA1/MOSI1
P21				AN15/SCK1
P22				SS1
P23-P27				—
P30-P35	I/O	Port 3 is a bit-programmable I/O port which can be configured as an input or a push-pull output. A pull-up resistor can be specified in 1-bit unit. The P34-P37 are only in the 44-Pin package.	Input	—
P36				RXD2
P37				TXD2
P40	I/O	Port 4 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P43 is not in the 32/28-Pin package. The P42-P43 are not in the 24-Pin package.	Input	RXD0/SCL0/MISO0
P41				TXD0/SDA0/MOSI0
P42				SCK0
P43				SS0
P50	I/O	Port 5 is a bit-programmable I/O port which can be configured as a Schmitt trigger input or a push-pull output. A pull-up resistor can be specified in 1-bit unit.	Input	XOUT/(RXD2)
P51				XIN/(TXD2)
P52				EINT8/EC0/BLNK
P53				SXIN/T0O/PWM0O
P54				SXOUT/EINT10
P55				RESETB

Table 20. Pin Description (continued)

Pin Name	I/O	Function	@Reset	Shared With
EINT0	I/O	External interrupt and Timer 3 capture input	Input	P02/AN0/AVREF/T4O/PWM4AA
EINT1	I/O	External interrupt and Timer 4 capture input	Input	P03/AN1/PWM4AB
EINT2	I/O	External interrupt inputs	Input	P04/AN2/PWM4BA
EINT3				P05/AN3/PWM4BB
EINT4				P06/AN4/PWM4CA
EINT5				P07/AN5/PWM4CB
EINT6				P17/AN6/SS2
EINT7				P16/AN7/SCK2
EINT8				P52/EC0/BLNK
EINT10	I/O	External interrupt and Timer 0 capture input	Input	P54/SXOUT
EINT11	I/O	External interrupt and Timer 1 capture input	Input	P12/AN11/T1O/PWM1O
EINT12	I/O	External interrupt and Timer 2 capture input	Input	P11/AN12/T2O/PWM2O
T0O	I/O	Timer 0 interval output	Input	P53/SXIN/PWM0O
T1O	I/O	Timer 1 interval output	Input	P12/AN11/EINT11/PWM1O
T2O	I/O	Timer 2 interval output	Input	P11/AN12/EINT12/PWM2O
T3O	I/O	Timer 3 interval output	Input	P01/DSCL
T4O	I/O	Timer 4 interval output	Input	P02/AN0/AVREF/EINT0/PWM4AA
PWM0O	I/O	Timer 0 PWM output	Input	P53/SXIN/T0O
PWM1O	I/O	Timer 1 pulse output	Input	P12/AN11/EINT11/T1O
PWM2O	I/O	Timer 2 pulse output	Input	P11/AN12/EINT12/T2O
PWM4AA	I/O	Timer 4 PWM outputs	Input	P02/AN0/AVREF/EINT0/T4O
PWM4AB				P03/AN1/EINT1
PWM4BA				P04/AN2/EINT2
PWM4BB				P05/AN3/EINT3
PWM4CA				P06/AN4/EINT4
PWM4CB				P07/AN5/EINT5
BLNK	I/O	External Sync Signal Input for 6-ch PWMs	Input	P52/EINT8/EC0
EC0	I/O	Timer 0 event count input	Input	P52/EINT8/BLNK
EC1	I/O	Timer 1 event count input	Input	P13/AN10
EC3	I/O	Timer 3 event count input	Input	P00/DSDA
BUZO	I/O	Buzzer signal output	Input	P13/AN10/EC1

Table 20. Pin Description (continued)

Pin Name	I/O	Function	@Reset	Shared With
SCK0	I/O	Serial 0 clock input/output	Input	P42
SCK1	I/O	Serial 1 clock input/output	Input	P21/AN15
SCK2	I/O	Serial 2 clock input/output	Input	P16/AN7/EINT7
MOSI0	I/O	SPI 0 master output, slave input	Input	P41/TXD0/SDA0
MOSI1	I/O	SPI 1 master output, slave input	Input	P20/AN14/TXD1/SDA1
MOSI2	I/O	SPI 2 master output, slave input	Input	P14/AN9
MISO0	I/O	SPI 0 master input, slave output	Input	P40/RXD0/SCL0
MISO1	I/O	SPI 1 master input, slave output	Input	P10/AN13/RXD1/SCL1
MISO2	I/O	SPI 2 master input, slave output	Input	P15/AN8
SS0	I/O	SPI 0 slave select input	Input	P43
SS1	I/O	SPI 1 slave select input	Input	P22
SS2	I/O	SPI 2 slave select input	Input	P17/AN6/EINT6
TXD0	I/O	UART 0 data output	Input	P41/SDA0/MOSI0
TXD1	I/O	UART 1 data output	Input	P20/AN14/SDA1/MOSI1
RXD0	I/O	UART 0 data input	Input	P40/SCL0/MISO0
RXD1	I/O	UART 1 data input	Input	P10/AN13/SCL1/MISO1
SCL0	I/O	I2C 0 clock input/output	Input	P40/RXD0/MISO0
SCL1	I/O	I2C 1 clock input/output	Input	P10/AN13/RXD1/MISO1
SDA0	I/O	I2C 0 data input/output	Input	P41/TXD0/MOSI0
SDA1	I/O	I2C 1 data input/output	Input	P20/AN14/TXD1/MOSI1
AVREF	I/O	A/D converter reference voltage	Input	P02/AN0/EINT0/T4O/PWM4A A
AN0	I/O	A/D converter analog input channels	Input	P02/AVREF/EINT0/T4O/PWM 4AA
AN1				P03/EINT1/PWM4AB
AN2				P04/EINT2/PWM4BA
AN3				P05/EINT3/PWM4BB
AN4				P06/EINT4/PWM4CA
AN5				P07/EINT5/PWM4CB
AN6				P17/EINT6/SS2
AN7				P16/EINT7/SCK2
AN8				P15/MISO2
AN9				P14/MOSI2
AN10				P13/EC1
AN11				P12/EINT11/T1O/PWM1O
AN12				P11/EINT12/T2O/PWM2O

Table 20. Pin Description (continued)

Pin Name	I/O	Function	@Reset	Shared With
AN13		A/D converter analog input channels		P10/RXD1/SCL1/MISO1
AN14				P20/TXD1/SDA1/MOSI1
AN15				P21/SCK1
RESETB	I/O	System reset pin with a pull-up resistor when it is selected as the RESETB by CONFIGURE OPTION	Input	P55
DSDA	I/O	On-chip debugger data input/output ⁽⁵⁾ , ⁽⁶⁾	Input	P00/EC3
DSCL	I/O	On-chip debugger clock input ⁽⁵⁾ , ⁽⁶⁾	Input	P01/T3O
XIN	I/O	Main oscillator pins	Input	P51/(TXD2)
XOUT				P50/(RXD2)
SXIN	I/O	Sub oscillator pins	Input	P53/T0O/PWM0O
SXOUT				P54/EINT10
VDD, VSS	–	Power input pins	–	–

NOTES:

1. The P14-P17, P23-P25, P34-P37, and P43 are not in the 32-Pin package.
2. The P13-P17, P22-P27, P34-P37, and P43 are not in the 28-Pin package.
3. The P05-P07, P14-P17, P20, P22-P27, P34-P37, and P42-P43 are not in the 24-Pin package.
4. The P55/RESETB pin is configured as one of the P55 and the RESETB pin by the "CONFIGURE OPTION".
5. If the P00/EC3/DSDA and P01/T3O/DSCL pins are connected to an emulator during reset or power-on reset, the pins are automatically configured as the debugger pins.
6. The P00/EC3/DSDA and P01/T3O/DSCL pins are configured as inputs with internal pull-up resistor only during the reset or power-on reset.
7. The P50/(RXD2)/XOUT, P51/(TXD2)/XIN, P53/SXIN/T0O/PWM0O, and P54/SXOUT/EINT10 pins are configured as a function pin by software control.

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 21. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Remark
Supply voltage	VIN	-0.3 ~ +6.5	V	—
Normal voltage Pin	VI	-0.3 ~ VDD+0.3		Voltage on any pin with respect to VSS
	VO	-0.3 ~ VDD+0.3		
	IOH	-25	mA	Maximum current output sourced by (IOH per I/O pin)
	ΣIOH	-200		Maximum current (ΣIOH)
	IOL	180		Maximum current sunk by (IOL per I/O pin)
	ΣIOL	200		Maximum current (ΣIOL)
Total power dissipation	PT	600	mW	—
Operating temperature	TOP	-40 ~ +105	°C	—
Storage temperature	TSTG	-65 ~ +150		—

CAUTION:

- Stresses beyond those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

4.2 Recommended Operating Conditions

Table 22. Recommended Operating Conditions

(TA = -40°C to +105°C)

Parameter	Symbol	Conditions		Typ.	Max.	Unit
Operating voltage	VDD	fx = 32 to 38 kHz	SX-tal	2.0	5.5	V
		fx = 0.4 to 4.2 MHz	X-tal	2.2	5.5	
		fx = 0.4 to 8.5 MHz		2.4	5.5	
		fx = 0.5 to 16 MHz	Internal RC	1.8	5.5	
Operating temperature	T _{OPR}	VDD = 1.8 to 5.5 V		-40	105	°C

4.3 ADC Characteristics

Table 23. ADC Characteristics

(T_A=-40°C to +105°C, VDD=1.8V to 5.5V, VSS=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	—	—	—	12	—	bit
Integral Non-linear	INL	VDD = 2.7 to 5.5 V, f _x =8 MHz	—	—	±6	LSB
Differential Non-linearity	DNL		—	—	±1	
Top offset error	TOE		—	—	±5	
Zero offset error	ZOE		—	—	±5	
Conversion time	t _{CON}	VDD = 2.7 to 5.5 V, f _x =8 MHz	20	—	—	μs
Analog input voltage	V _{AN}	—	VSS	—	AVREF	V
Analog reference voltage	AVREF	— ⁽³⁾	1.8	—	VDD	
A/DC input leakage current	I _{AN}	VDD = 5.12 V	—	—	2	μA
A/DC current	I _{ADC}	Enable	—	1	2	mA
		Disable	—	—	0.1	μA

NOTES:

1. Zero offset error is the difference between 0000000000 and the converted output for zero input voltage (VSS).
2. The top offset error is the difference between 1111111111 and the converted output for top input voltage (VDD).
3. If AVREF is less than 2.7 V, the resolution degrades by 1-bit whenever AVREF drops 0.1 V.. (@ADCLK = 0.5 MHz, under 2.7 V resolution has no test)

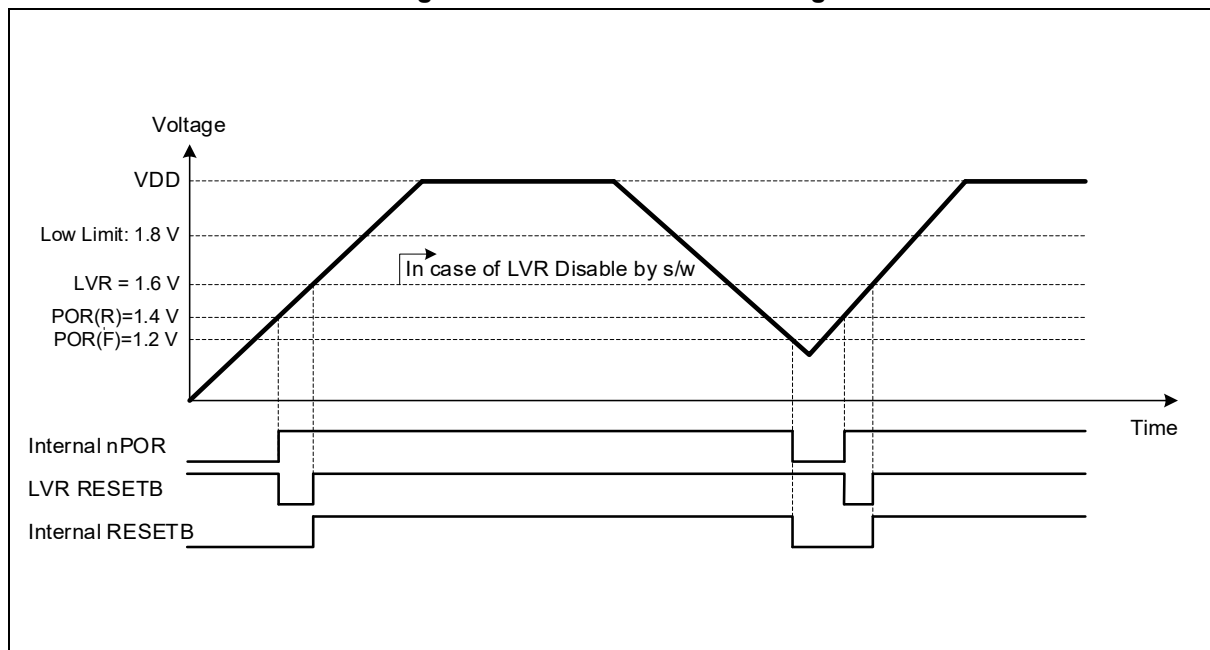
4.4 Power-On Reset

Table 24. Power-On Reset Characteristics

($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{DD} = 1.8\text{ V}$ to 5.5 V , $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
RESET release level	V _{POR}	–	–	1.4	–	V
VDD Voltage Rising Time	t _R	0.5 to 2 V	0.05	–	100	ms/V
POR current	I _{POR}	–	–	0.2	–	μA

Figure 51. Power-On Reset Timing



4.5 Low Voltage Reset and Low Voltage Indicator Characteristics

Table 25. LVR and LVI Characteristics

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{DD} = 1.8\text{ V}$ to 5.5 V , $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Detection level	VLVR VLVI	LVR: All levels LVI: other levels except 1.60V 1.60V level: Rising edge voltage Other levels: Falling edge voltage		–	1.60	1.79	V
				1.84	2.00	2.16	
				1.93	2.10	2.27	
				2.02	2.20	2.38	
				2.13	2.32	2.51	
				2.24	2.44	2.64	
				2.38	2.59	2.80	
				2.53	2.75	2.97	
				2.70	2.93	3.16	
				2.89	3.14	3.39	
				3.11	3.38	3.65	
				3.37	3.67	3.97	
				3.68	4.00	4.32	
				4.06	4.40	4.74	
LVR/LVI Hysteresis	ΔV	–		–	100	180	mV
Minimum pulse width	t_{LW}	–		100	–	–	μs
LVR and LVI current	I_{BL}	Enable	$V_{DD} = 3\text{ V}$	–	10.0	18.0	μA
		Disable		–	–	0.1	

4.6 Internal RC Oscillator Characteristics

Table 26. Internal RC Oscillator Characteristics

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{DD} = 1.8\text{ V}$ to 5.5 V , $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Frequency	f_{IRC}	$V_{DD} = 1.8\text{ to }5.5\text{ V}$	–	16	–	MHz
Tolerance	–	$T_A = -20^\circ\text{C}$ to $+70^\circ\text{C}$ (user trim, using only E-PGM+)	–	–	± 1.0	%
		$T_A = -20^\circ\text{C}$ to $+70^\circ\text{C}$			± 1.5	
		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			± 2.0	
		$T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$			± 3.0	
Clock duty ratio	T_{OD}	–	40	50	60	%
Stabilization time	t_{HFS}	–	–	–	100	μs
Internal RC	I_{IRC}	Enable	–	0.6	–	mA
		Disable	–	–	0.1	μA

NOTES:

1. User Trimming means the calibration of HFIRC frequency using E-PGM+ and E-PGM Serial.
2. To ensure $\pm 1.0\%$ tolerance of HFIRC frequency, it is necessary to do User Trimming.
3. Guaranteed by design but might be On-Board programming after SMT process. (HFIRC Calibration with high temperature can cause the shift of the frequency, be sure to calibrate enough to cool to near room temperature after SMT process)

4.7 Internal Watchdog Timer RC Oscillator Characteristics

Table 27. Internal WDTRC Oscillator Characteristics

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{DD} = 1.8\text{ V}$ to 5.5 V , $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Frequency	f_{WDTRC}	–	2	5	10	kHz
Stabilization time	t_{WDTS}	–	–	–	1	ms
WDTRC current	I_{WDTRC}	Enable	–	1	–	μA
		Disable	–	–	0.1	

4.8 DC Characteristics

Table 28. DC Characteristics

 (T_A=-40°C to +105°C, VDD=1.8 V to 5.5 V, VSS=0 V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input high voltage	V _{IH1}	P0, P1, P5, RESETB		0.8VDD	–	VDD	V
	V _{IH2}	All input pins except V _{IH1}		0.7VDD	–	VDD	
Input low voltage	V _{IL1}	P0, P1, P5, RESETB		–	–	0.2VDD	V
	V _{IL2}	All input pins except V _{IL1}		–	–	0.3VDD	
Output high voltage	V _{OH}	VDD = 4.5 V, I _{OH} = -15 mA; T _A = 25°C, All output ports		VDD-1.0	–	–	V
Output low voltage	V _{OL1}	VDD = 4.5 V, I _{OL} = 15 mA; T _A = 25°C, All output ports except V _{OL2}		–	–	1.0	V
	V _{OL2}	VDD=4.5 V; P1[1:0], P2[1:0], and P3[3:0] LDDRvx = 1 (x = 0 to 7)	I _{OL} =160 mA; Up to 85°C	–	1.5	3.0	
			I _{OL} =120 mA; Up to 105°C				
			VDD=4.5 V, I _{OL} =15 mA; T _A =25°C LDDRvx = 0 (x = 0 to 7)		–	–	1.0
Input high leakage current	I _{IH}	All Input ports		–	–	1	μA
Input low leakage current	I _{IL}	All Input ports		-1	–	–	μA
Pull-up resistor	R _{PU1}	V _I =0 V, T _A =25°C, All Input ports	VDD=5 V	25	50	100	kΩ
			VDD=3 V	50	100	200	
	R _{PU2}	V _I =0 V, T _A =25°C, RESETB	VDD=5 V	150	250	400	
			VDD=3 V	300	500	700	
OSC feedback resistor	R _{X1}	XIN=VDD, XOUT=VSS, T _A =25°C, VDD=5 V		600	1200	2000	kΩ
	R _{X2}	SXIN=VDD, SXOUT=VSS, T _A =25°C, VDD=5 V		2500	5000	10000	kΩ

4.9 Supply Current Characteristics

Table 29. Supply Current Characteristics

($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{DD} = 1.8\text{ V}$ to 5.5 V , $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply current	I_{DD1} (RUN)	$f_{XIN} = 8\text{ MHz}$, $V_{DD} = 5\text{ V} \pm 10\%$	—	2.2	4.4	mA
		$f_{XIN} = 4\text{ MHz}$, $V_{DD} = 3\text{ V} \pm 10\%$	—	1.0	2.0	
		$f_{IRC} = 16\text{ MHz}$, $V_{DD} = 5\text{ V} \pm 10\%$	—	2.0	4.0	
	I_{DD2} (IDLE)	$f_{XIN} = 8\text{ MHz}$, $V_{DD} = 5\text{ V} \pm 10\%$	—	1.5	3.0	mA
		$f_{XIN} = 4\text{ MHz}$, $V_{DD} = 3\text{ V} \pm 10\%$	—	0.6	1.2	
		$f_{IRC} = 16\text{ MHz}$, $V_{DD} = 5\text{ V} \pm 10\%$	—	1.0	2.0	
	I_{DD3} (RUN)	$f_{SUB} = 32.768\text{ kHz}$, $V_{DD} = 3\text{ V} \pm 10\%$, $T_A = 25^{\circ}\text{C}$	—	170	270	μA
	I_{DD4} (IDLE)	$f_{SUB} = 32.768\text{ kHz}$, $V_{DD} = 3\text{ V} \pm 10\%$, $T_A = 25^{\circ}\text{C}$	—	6.0	12.0	μA
	I_{DD5} (STOP)	$V_{DD} = 5\text{ V} \pm 10\%$, $T_A = 25^{\circ}\text{C}$	—	1.5	5.0	μA

NOTES:

1. Where the f_{XIN} is an external main oscillator, the f_{SUB} is an external sub oscillator. The IRC is an internal RC oscillator, and the f_X is the selected system clock.
2. All supply current items don't include the current of an internal Watch-dog timer RC (WDTRC) oscillator and a peripheral block.
3. All supply current items include the current of the power-on reset (POR) block.

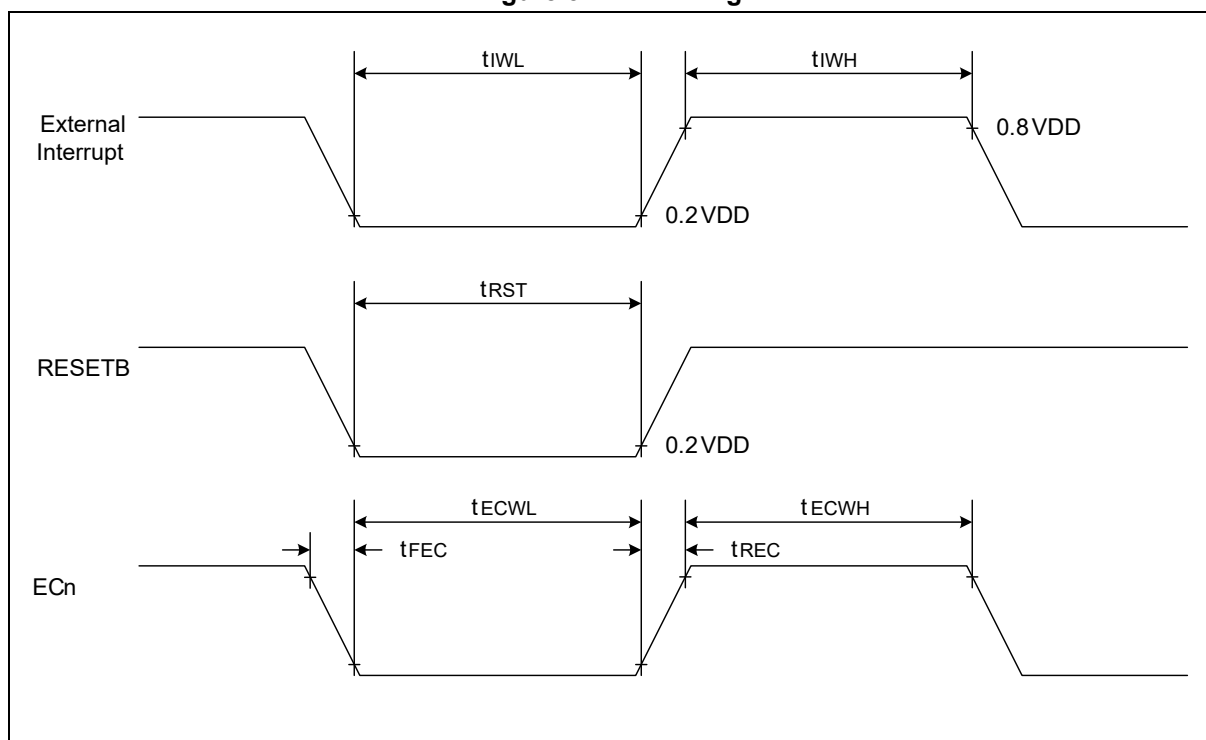
4.10 AC Characteristics

Table 30. AC Characteristics

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{DD} = 1.8\text{ V}$ to 5.5 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
RESETB input low width	t_{RST}	$V_{DD} = 5\text{ V}$	10	—	—	μs
Interrupt input high, low width	t_{IWH} , t_{IWL}	All interrupt, $V_{DD} = 5\text{ V}$	200	—	—	ns
External counter input high, low pulse width	t_{ECWH} , t_{ECWL}	EC_n , $V_{DD} = 5\text{ V}$ ($n=0, 1, 3$)	200	—	—	
External counter transition time	t_{REC} , t_{FEC}	EC_n , $V_{DD} = 5\text{ V}$ ($n=0, 1, 3$)	20	—	—	

Figure 52. AC Timing



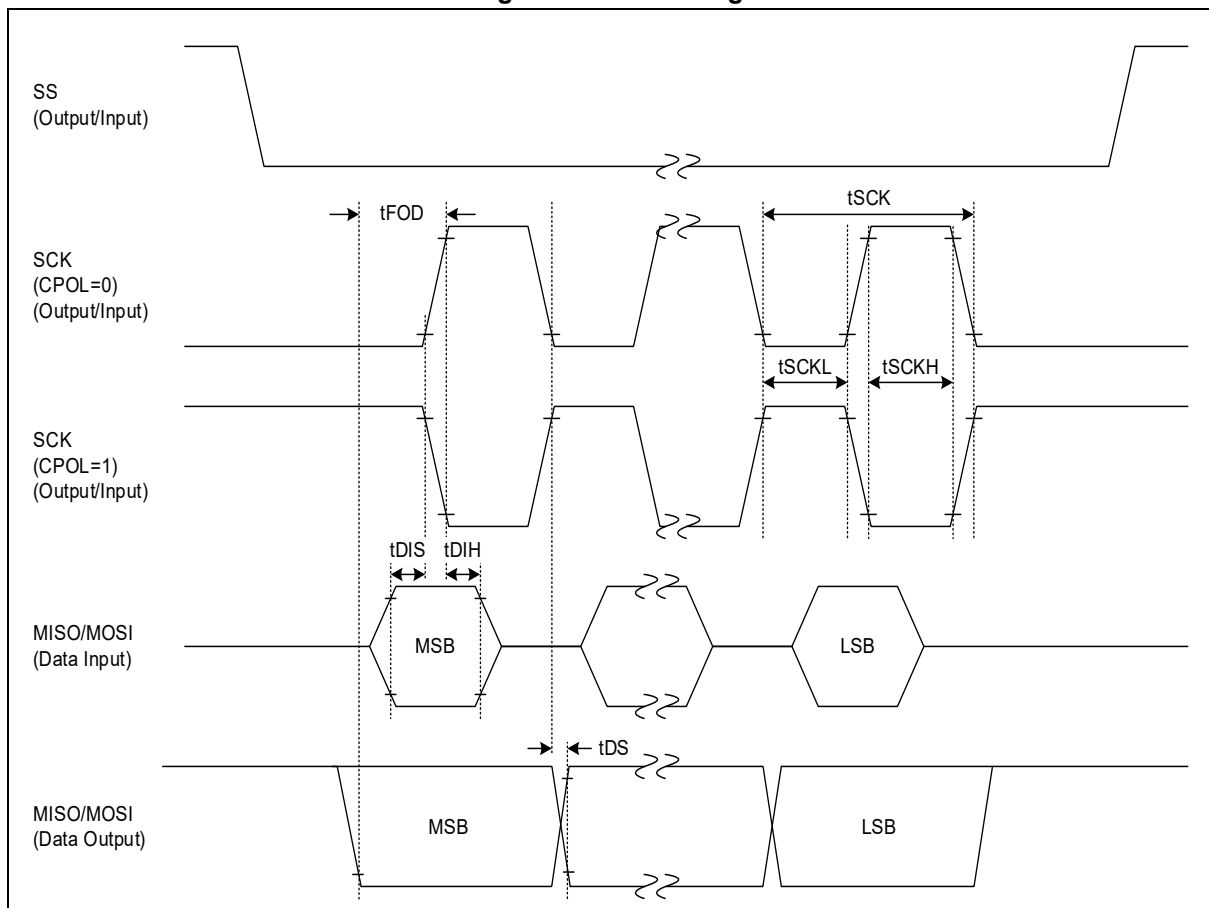
4.11 SPI Characteristics

Table 31. SPI Characteristics

($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{DD} = 1.8\text{ V}$ to 5.5 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output clock pulse period	t_{SCK}	Internal SCK source	1000	—	—	ns
Input clock pulse period		External SCK source	1000	—	—	
Output clock high, low pulse width	t_{SCKH} t_{SCKL}	Internal SCK source	350	—	—	
Input clock high, low pulse width		External SCK source	350	—	—	
First output clock delay time	t_{FOD}	Internal/external SCK source	500	—	—	
Output clock delay time	t_{DS}	—	—	—	250	
Input setup time	t_{DIS}	—	500	—	—	
Input hold time	t_{DIH}	—	750	—	—	

Figure 53. SPI Timing



4.12 UART Timing Characteristics

Table 32. UART Timing Characteristics

($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{DD} = 2.2\text{ V}$ to 5.5 V , $f_x = 8.0\text{ MHz}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Serial port clock cycle time	t_{SCK}	1,800	$t_{CPU} \times 16$	2,200	ns
Output data setup to clock rising edge	t_{S1}	810	$t_{CPU} \times 13$	—	
Clock rising edge to input data valid	t_{S2}	—	—	590	
Output data hold after clock rising edge	t_{H1}	$t_{CPU} - 50$	t_{CPU}	—	
Input data hold after clock rising edge	t_{H2}	0	—	—	
Serial port clock High, Low level width	t_{HIGH}, t_{LOW}	720	$t_{CPU} \times 8$	1,280	

Figure 54. UART Timing Characteristics

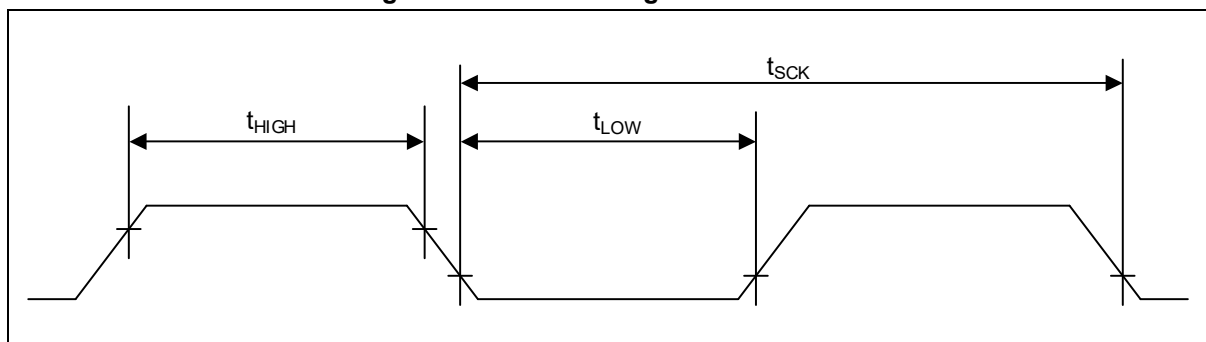
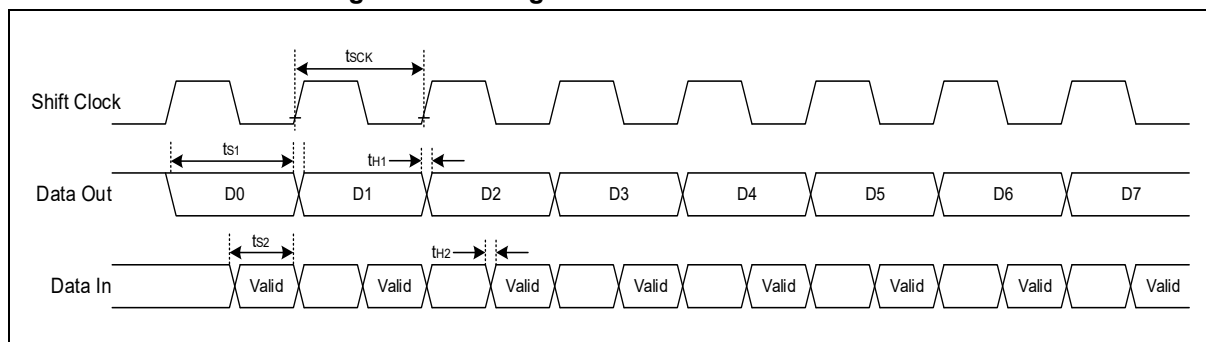


Figure 55. Timing Waveform of UART Module



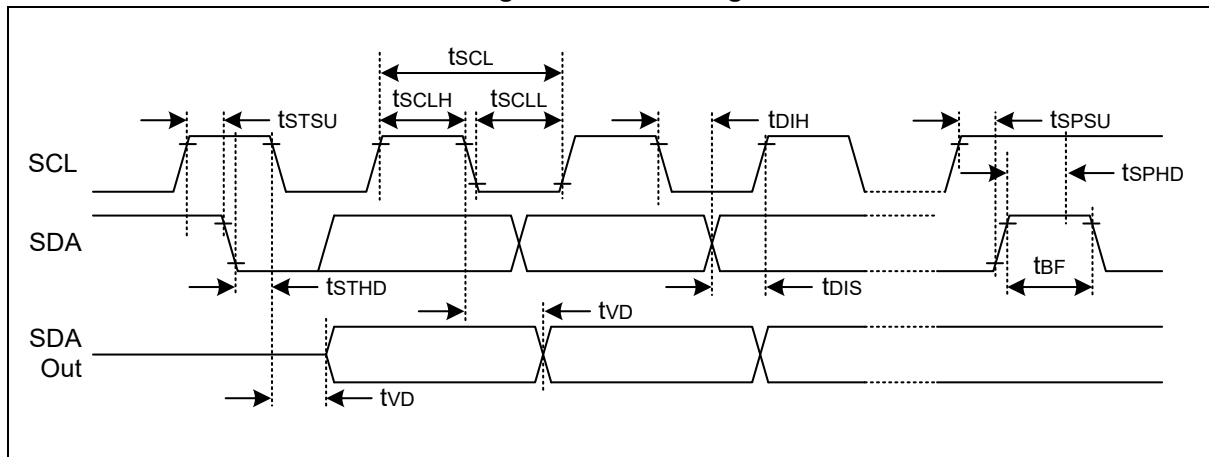
4.13 I2C Characteristics

Table 33. I2C Characteristics

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{DD} = 1.8\text{ V}$ to 5.5 V)

Parameter	Symbol	Standard Mode		High-Speed Mode		Unit
		Min.	Max.	Min.	Max.	
Clock frequency	tSCL	0	100	0	400	kHz
Clock High Pulse Width	tSCLH	4.0	–	0.6	–	μs
Clock Low Pulse Width	tSCLL	4.7	–	1.3	–	
Bus Free Time	tBF	4.7	–	1.3	–	
Start Condition Setup Time	tSTSU	4.7	–	0.6	–	
Start Condition Hold Time	tSTHD	4.0	–	0.6	–	
Stop Condition Setup Time	tSPSU	4.0	–	0.6	–	
Stop Condition Hold Time	tSPHD	4.0	–	0.6	–	
Output Valid from Clock	tVD	0	–	0	–	
Data Input Hold Time	tDIH	0	–	0	1.0	ns
Data Input Setup Time	tDIS	250	–	100	–	

Figure 56. I2C Timing



4.14 Data Retention Voltage in STOP Mode

Table 34. Data Retention Voltage in STOP Mode

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{DD} = 1.8\text{ V}$ to 5.5 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data retention supply voltage	V_{DDDR}	—	1.8	—	5.5	V
Data retention supply current	I_{DDDR}	$V_{DDDR} = 1.8\text{ V}$ ($T_A = 25^\circ\text{C}$), STOP mode	—	—	1	μA

Figure 57. STOP Mode Release Timing When Initiated by Interrupts

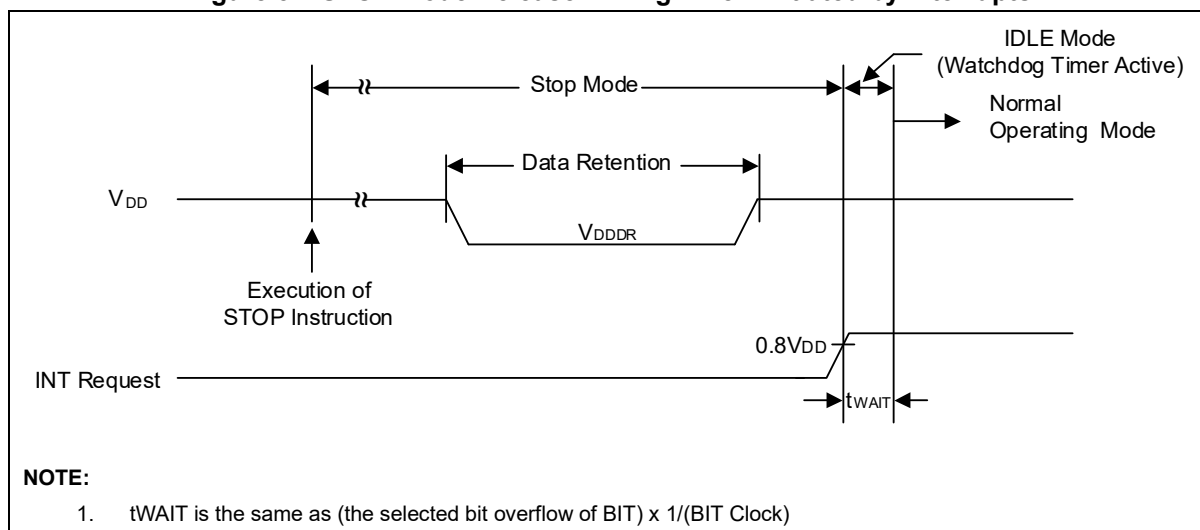
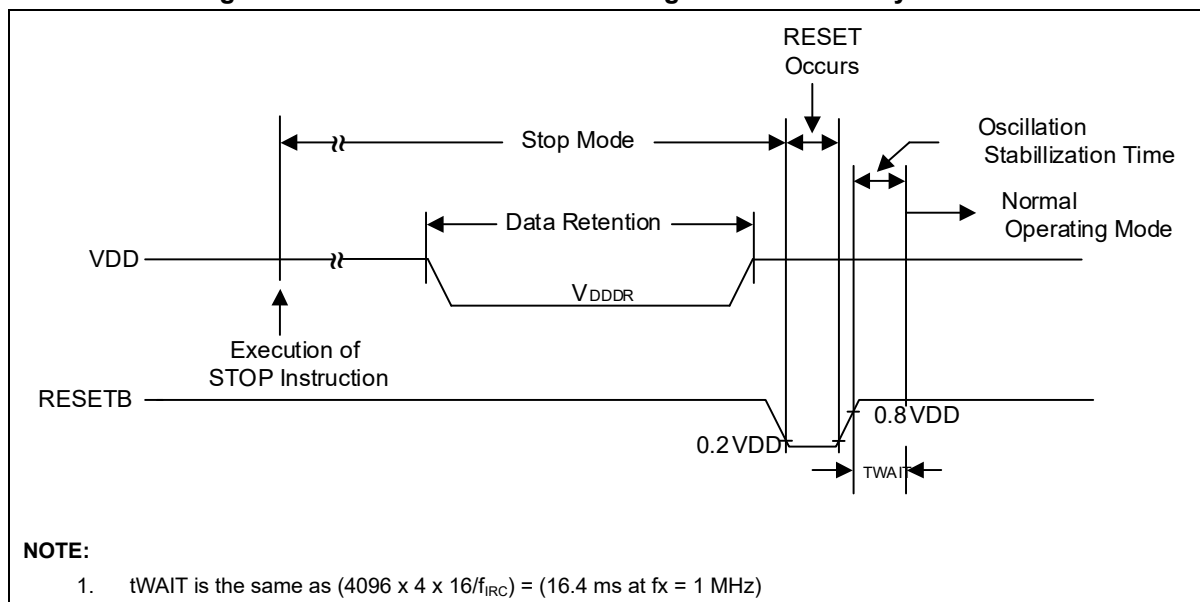


Figure 58. STOP Mode Release Timing When Initiated by RESETB



4.15 Internal Flash Characteristics

Table 35. Internal Flash Characteristics

(T_A=-40°C to +105°C, VDD=1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Sector write time	t _{FSW}	—	—	3.0	3.5	ms
Sector erase time	t _{FSE}	—	—	3.0	3.5	
Code write protection time	t _{FHL}	—	—	3.0	3.5	
Page buffer reset time	t _{FBR}	—	—	—	5	μs
System clock frequency	f _{SCLK}	—	0.4	—	—	MHz
Endurance of write/erase (Sector 0~507)	N _{FWE}	—	10,000	—	—	times
Endurance of write/erase (Sector 508~511)			100,000			
Flash Retention Time	t _{FRT}	—	10	—	—	years

4.16 Input/output Capacitance Characteristics

Table 36. I/O Capacitance Characteristics

(T_A=-40°C to +105°C, VDD=0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	f _x =1 MHz Unmeasured pins are connected to VSS.	—	—	10	pF
Output capacitance	C _{OUT}					
I/O capacitance	C _{IO}					

4.17 Main Oscillator Characteristics

Table 37. Main Oscillator Characteristics

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{DD} = 2.2\text{ V}$ to 5.5 V)

Oscillator	Parameter	Conditions	Min.	Typ.	Max.	Unit
Crystal/ Ceramic Oscillator	Main oscillation frequency	2.2 V – 5.5 V	0.4	–	4.2	MHz
		2.4 V – 5.5 V	0.4	–	8.5	
External Clock	XIN input frequency	2.2 V – 5.5 V	0.4	–	4.2	
		2.4 V – 5.5 V	0.4	–	8.5	

Figure 59. Crystal/Ceramic Oscillator

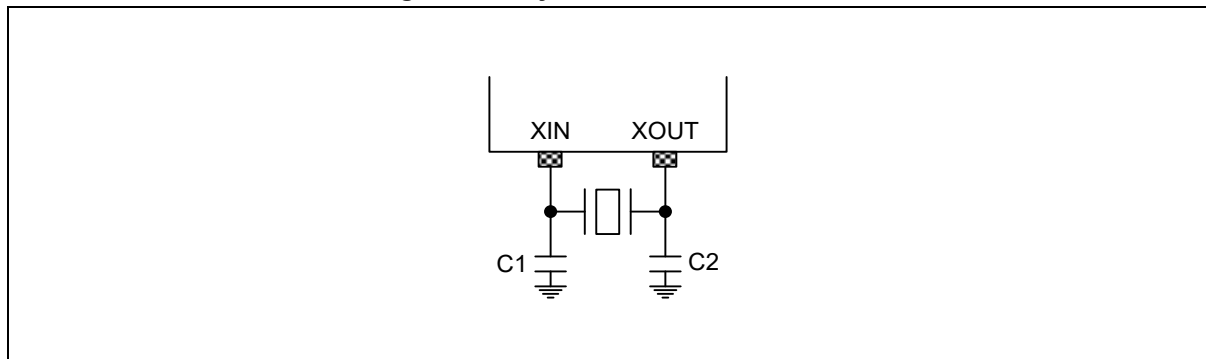
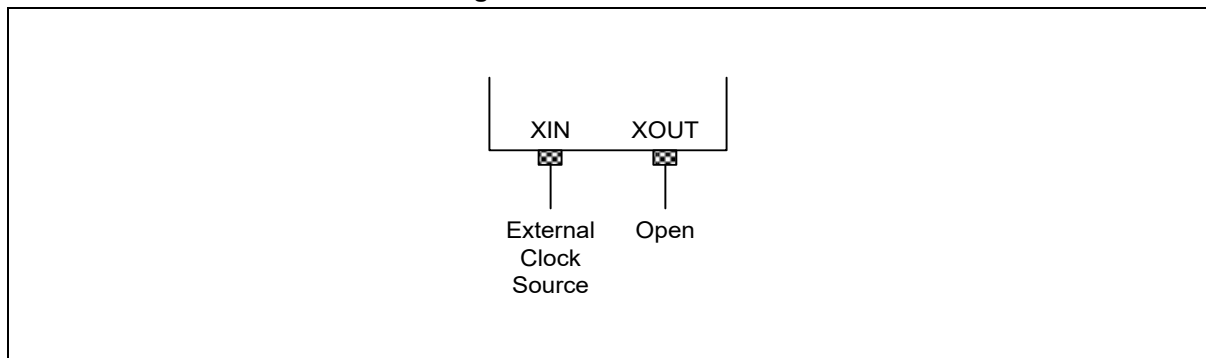


Figure 60. External Clock



4.18 Sub Oscillator Characteristics

Table 38. Sub Oscillator Characteristics

($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{DD} = 2.0\text{ V}$ to 5.5 V)

Oscillator	Parameter	Conditions	Min.	Typ.	Max.	Unit
Crystal	Sub oscillation frequency	2.0 V – 5.5 V	32	32.768	38	kHz
External clock	SXIN input frequency		32	–	100	

Figure 61. Crystal Oscillator

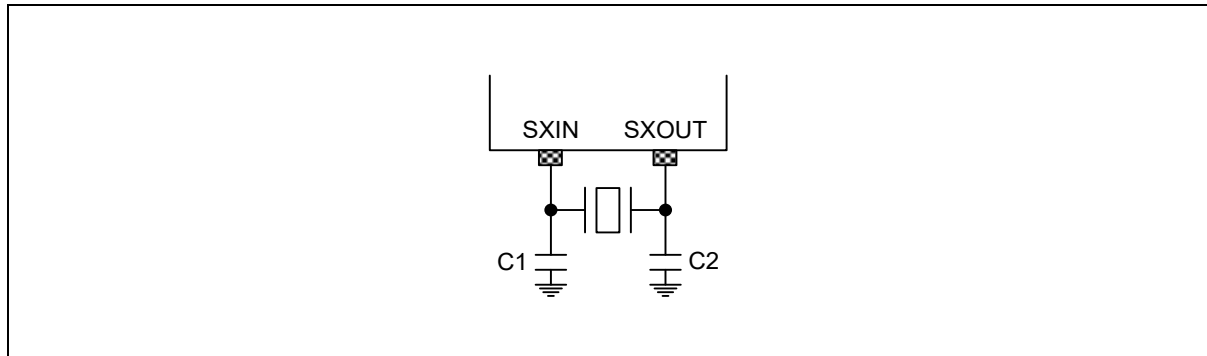
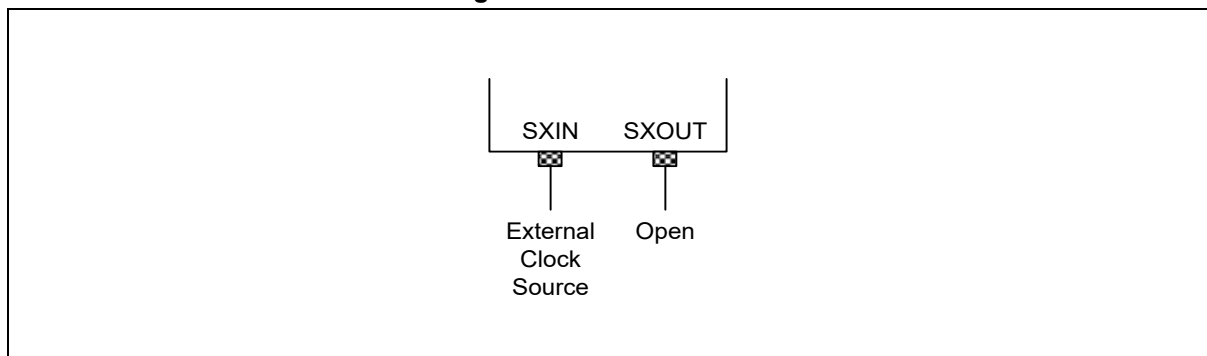


Figure 62. External Clock



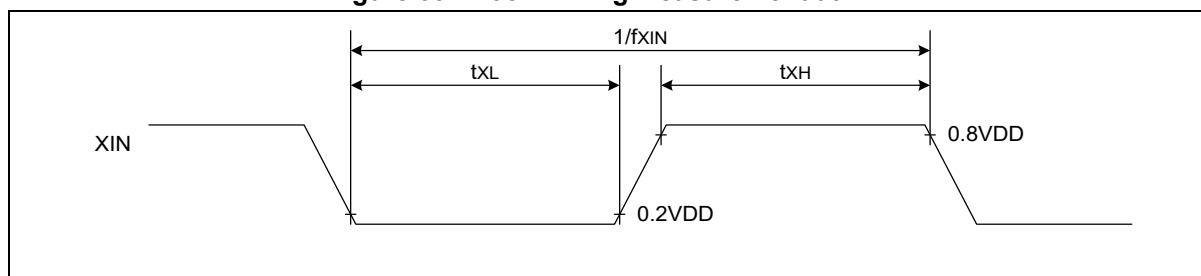
4.19 Main oscillator Stabilization Characteristics

Table 39. Main Oscillator Stabilization Characteristics

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{DD} = 2.2\text{ V}$ to 5.5 V)

Oscillator	Conditions	Min.	Typ.	Max.	Unit
Crystal	$f_{XIN} \geq 1\text{ MHz}$ Oscillation stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	—	—	60	ms
Ceramic		—	—	10	
External Clock	$f_{XIN} = 0.4\text{ to }8.5\text{ MHz}$ XIN input high and low width (t_{XL} , t_{XH})	58	—	1250	ns

Figure 63. Clock Timing Measurement at XIN



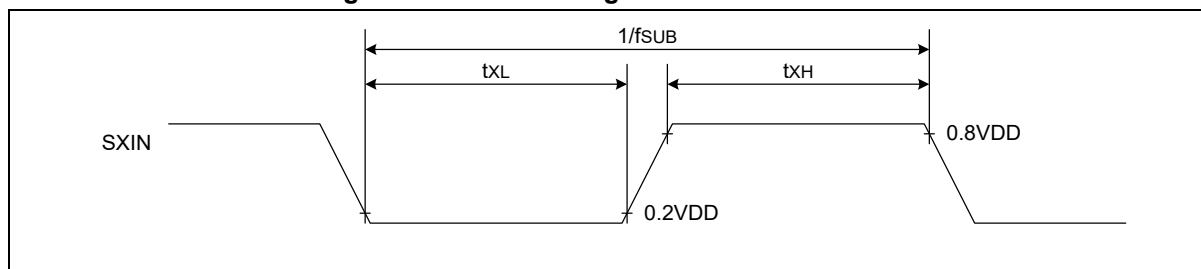
4.20 Sub oscillator Stabilization Characteristics

Table 40. Sub Oscillator Stabilization Characteristics

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{DD} = 2.0\text{ V}$ to 5.5 V)

Oscillator	Conditions	Min.	Typ.	Max.	Unit
Crystal	—	—	—	10	sec
	$V_{DD} = 3\text{ V}$, $T_A = 25^\circ\text{C}$	—	0.7	1.5	
External Clock	$SXIN$ input high and low width (t_{XL} , t_{XH})	5	—	15	μs

Figure 64. Clock Timing Measurement at SXIN



4.21 Operating Voltage Range

Figure 65. Operating Voltage Range

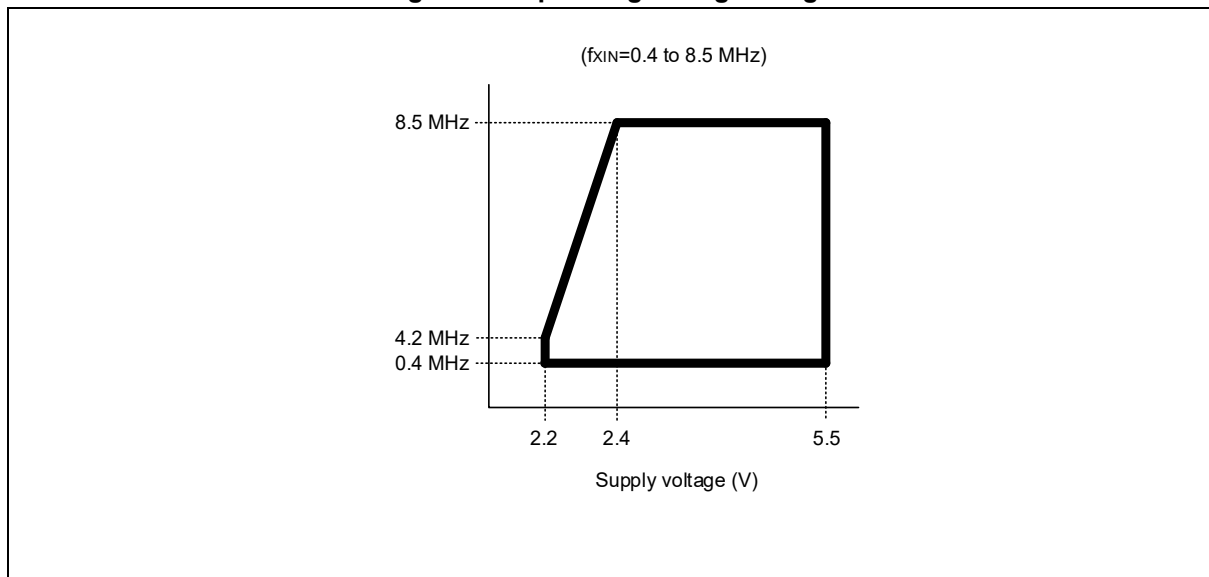
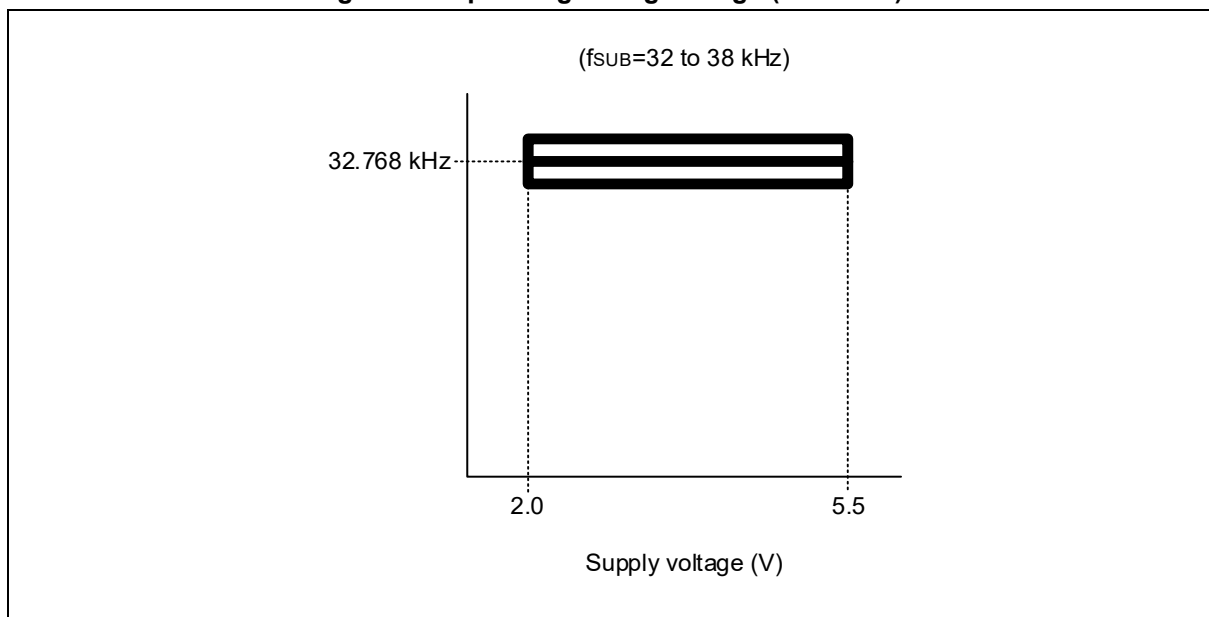


Figure 66. Operating Voltage Range (Sub OSC)



4.22 Typical Characteristics

Figures and tables described in this chapter can be used only for design guidance and are not tested or guaranteed. In graphs or tables some data may exceed the specified operating range and can be only for information. The device is guaranteed to operate properly only within the specified range.

The data presented in this chapter is a statistical summary of data collected on units from different lots over a period. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

Figure 67. MAIN RUN (IDD1) Current

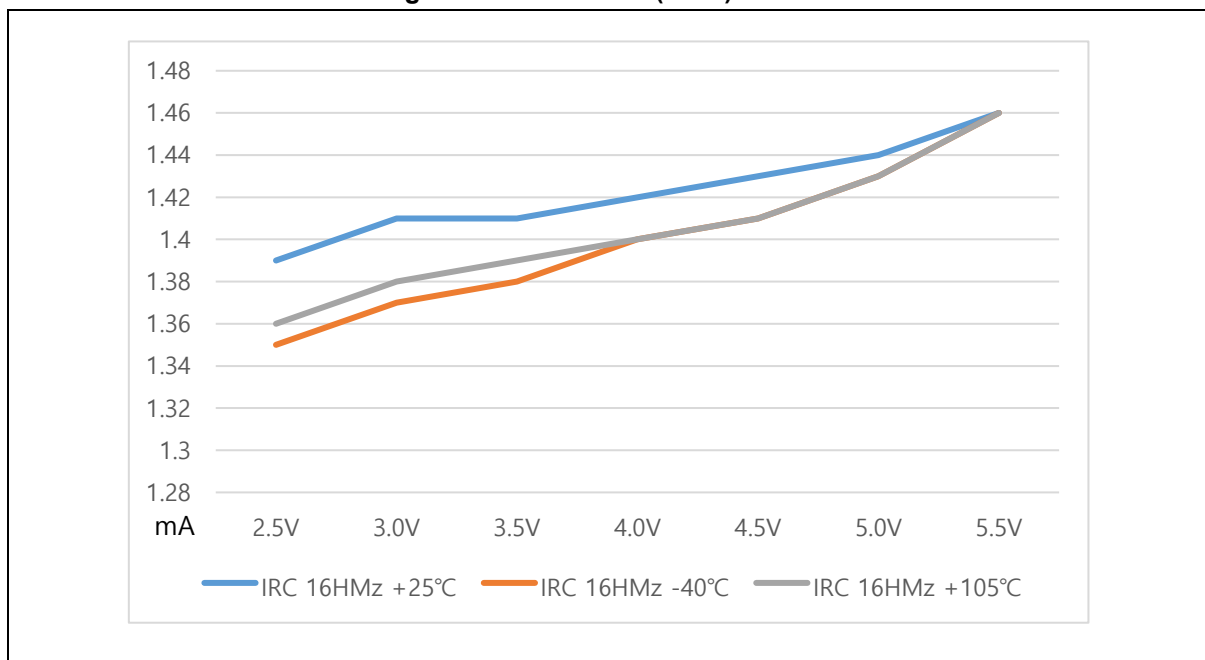


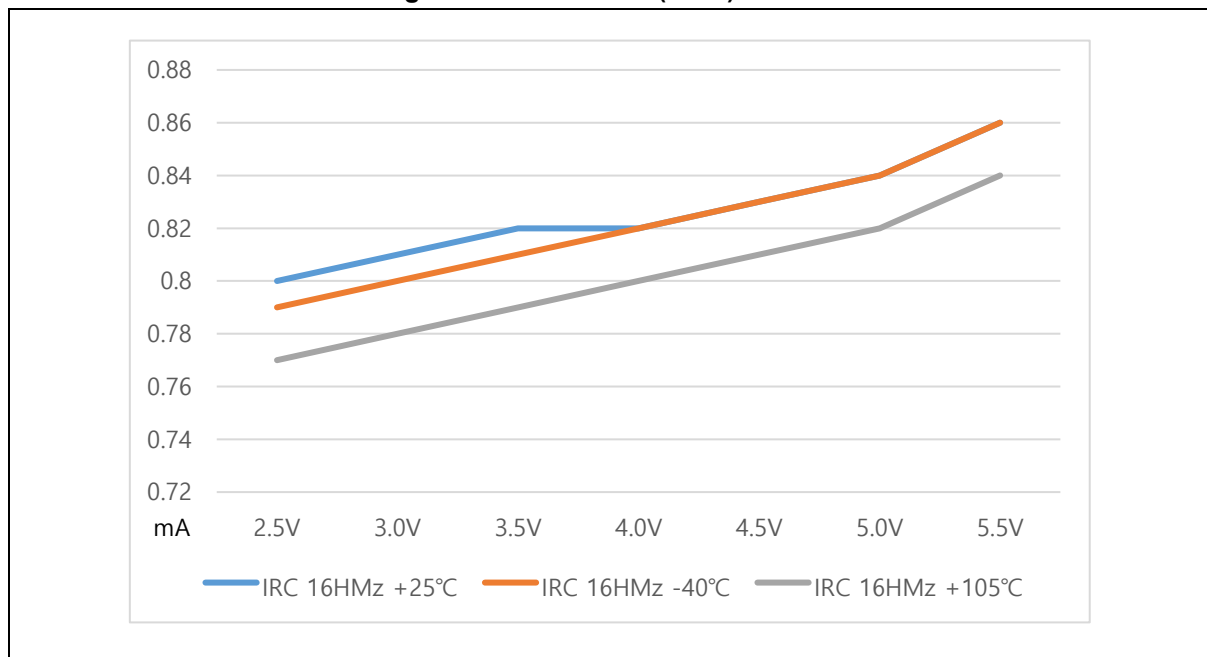
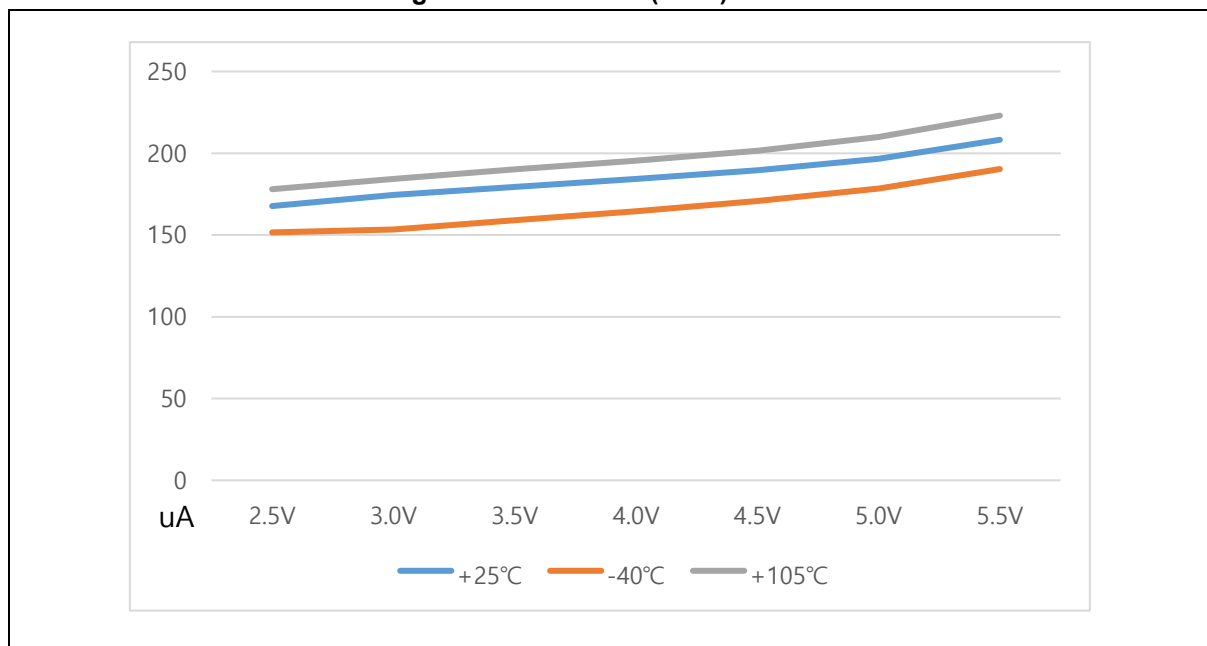
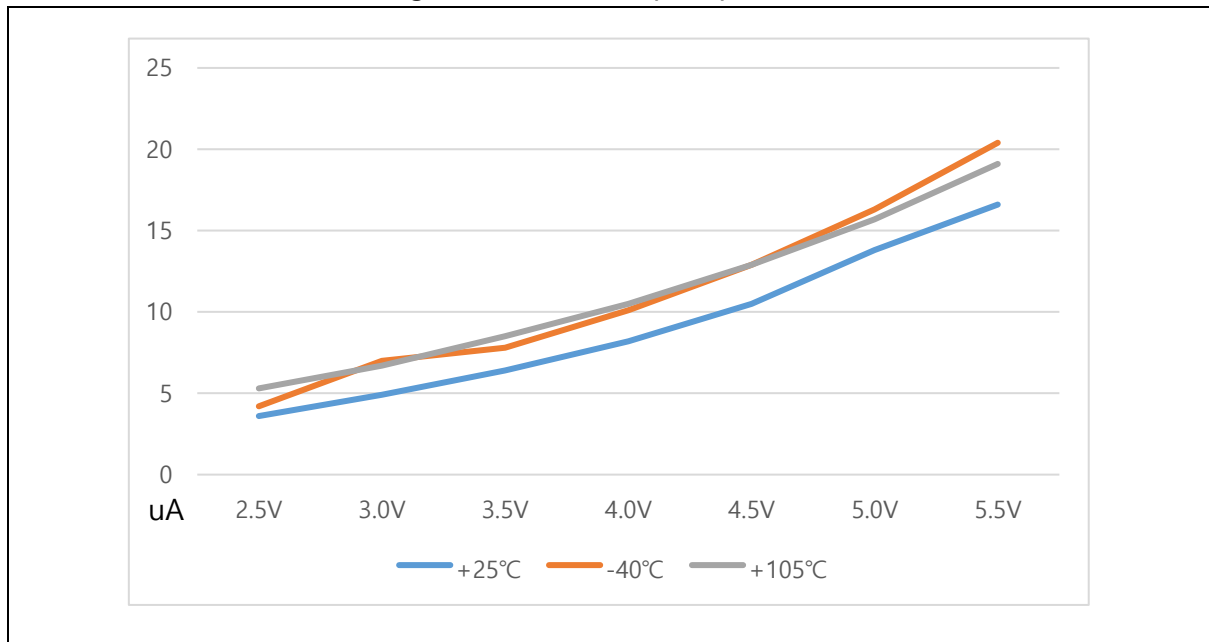
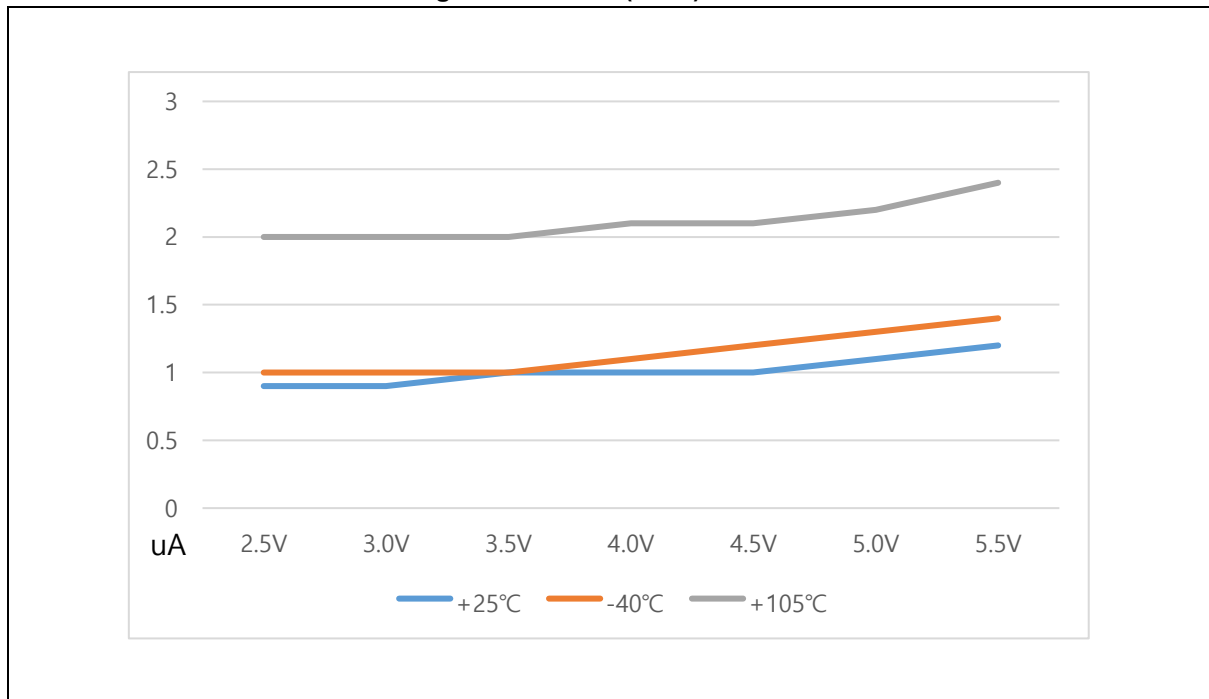
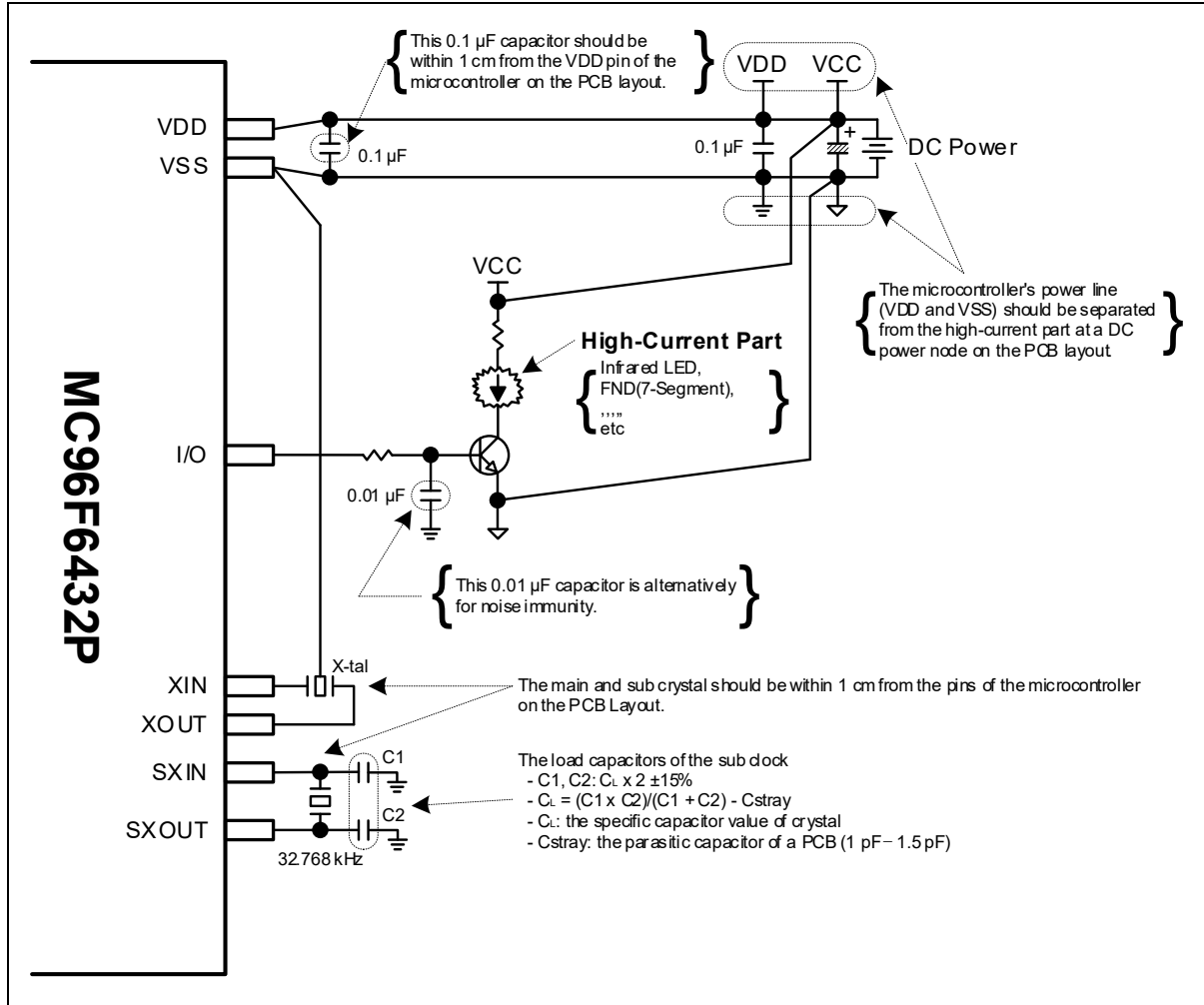
Figure 68. MAIN IDLE (IDD2) Current**Figure 69. SUB RUN (IDD3) Current**

Figure 70. SUB IDLE (IDD4) Current**Figure 71. STOP (IDD5) Current**

4.23 Recommended Circuit and Layout

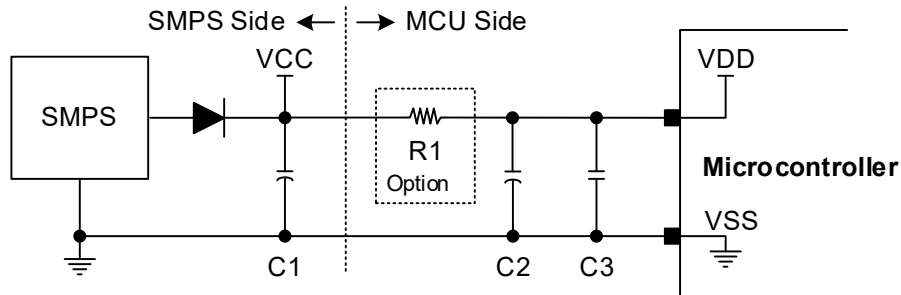
The Figure 72 is a recommended circuit and layout for MC96F6432P.

Figure 72. Recommended Circuit and Layout



4.24 Recommended Circuit and Layout with SMPS Power

Figure 73. Recommended Circuit and Layout with SMPS Power



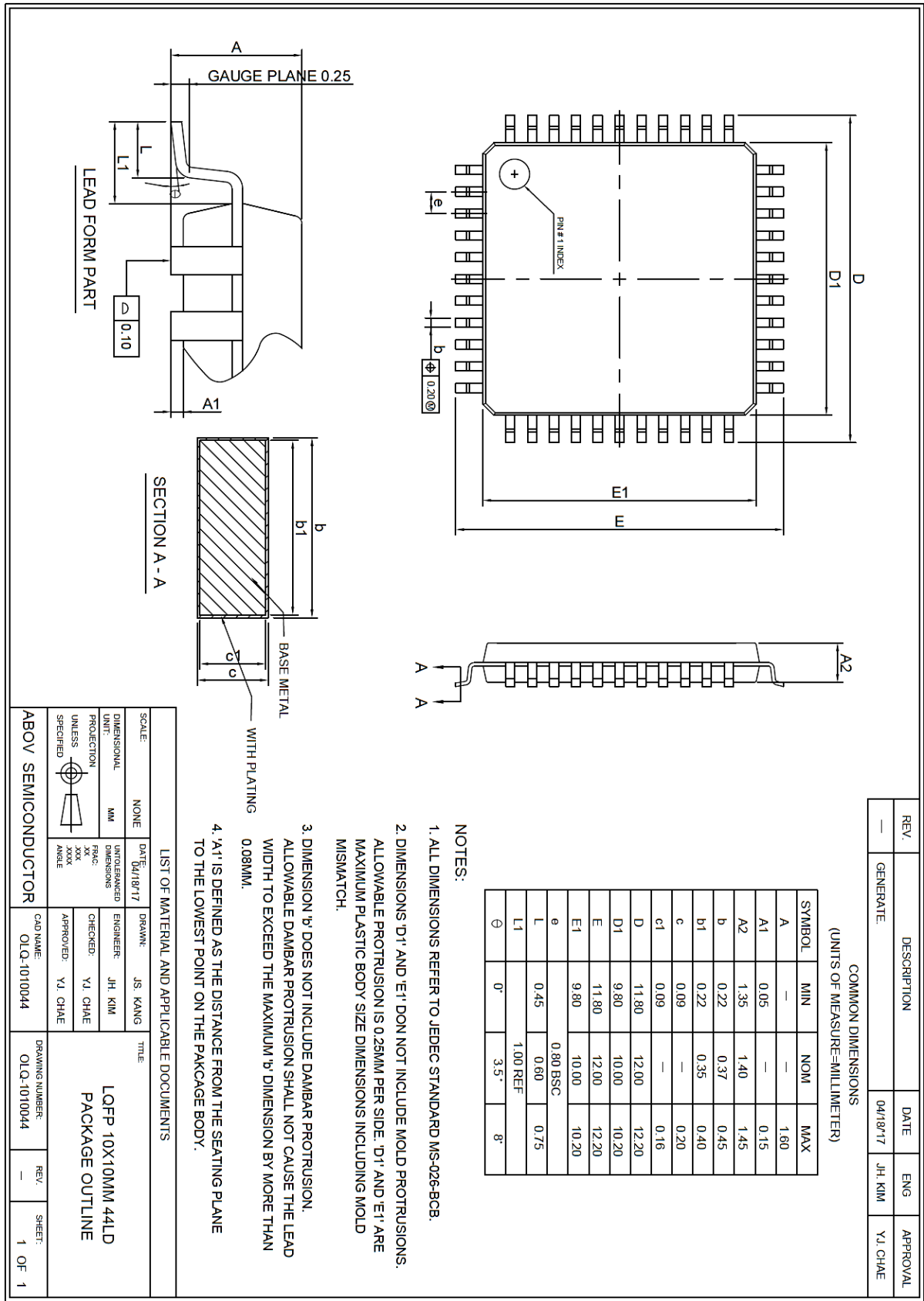
NOTES:

1. The C1 capacitor is to flatten out the voltage of the SMPS power, VCC.
 - Recommended C1: 470 μ F/25 V more
2. The R1 and C2 are RC filters for VDD and suppress the ripple of VCC.
 - Recommended R1: 10 Ω - 20 Ω
 - Recommended C2: 47 μ F/25 V more
 - The R1 and C2 should be as close to the C3 as possible.
 - The R1 is optional so it may not apply.
3. The C3 capacitor is used for temperature compensation because an electrolytic capacitor becomes worse characteristics at low temperature.
 - Recommended C3: ceramic capacitor 2.2 μ F more
 - The C3 should be within 1 cm from VDD pin of the microcontroller on the PCB layout.
4. The above circuit is recommended to improve noise immunity (EFT, Surge, ESD, etc.) when the SMPS supplies the VDD of the microcontroller.

5. Package Information

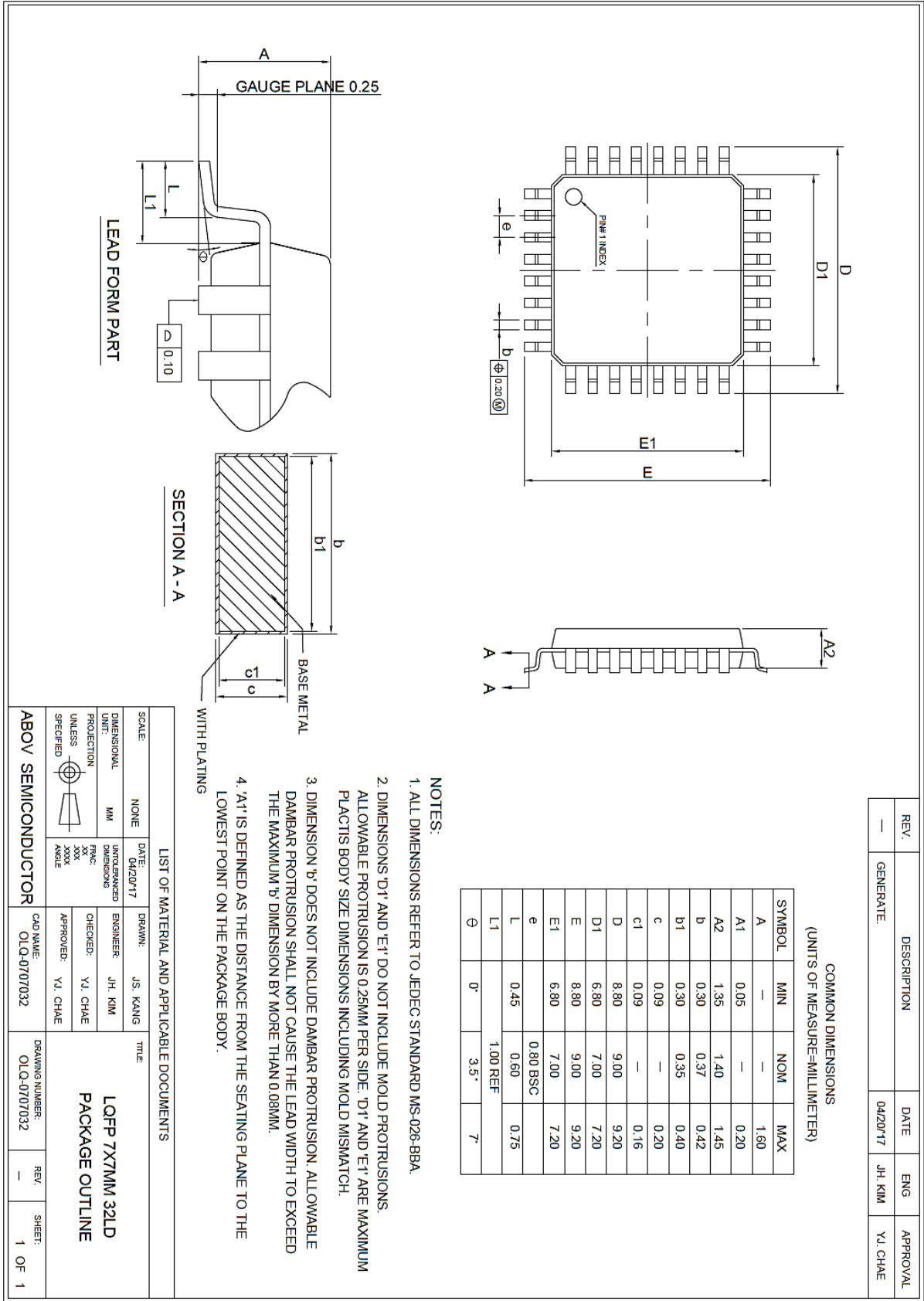
5.1 44-LQFP Package Information

Figure 74. 44-LQFP Package Outline



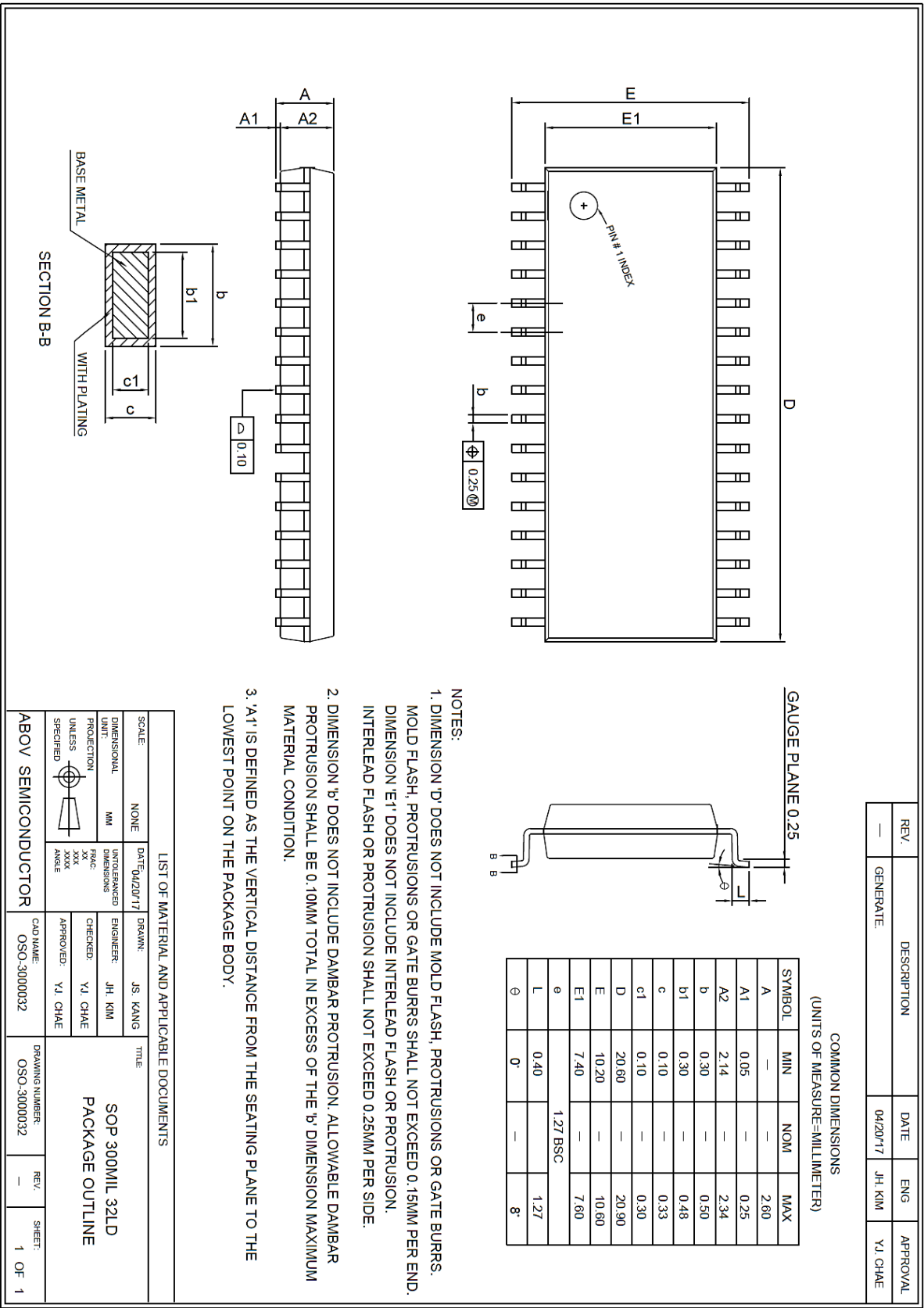
5.2 32-LQFP Package Information

Figure 75. 32-LQFP Package Outline



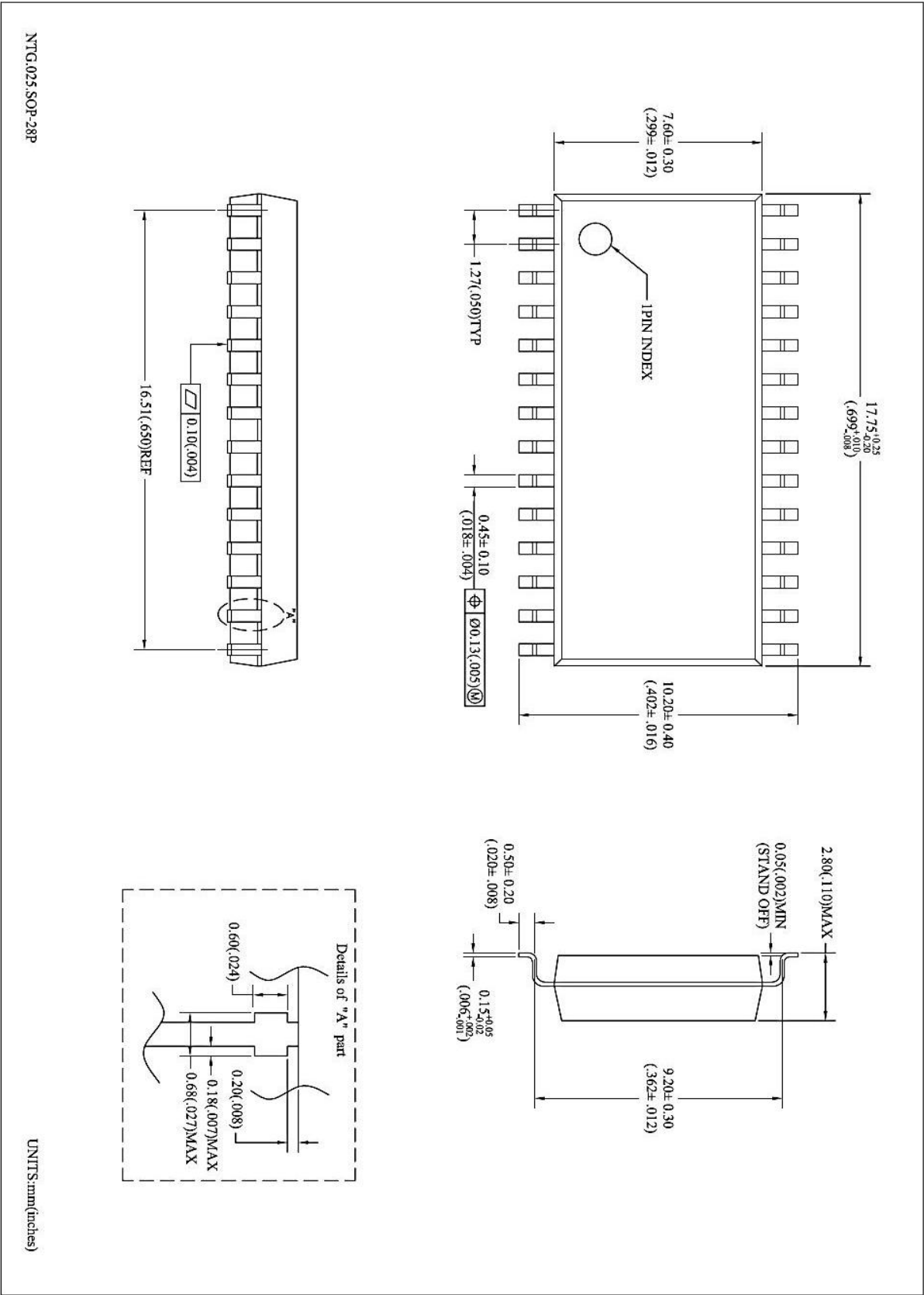
5.3 32-SOP Package Information

Figure 76. 32-SOP Package Outline



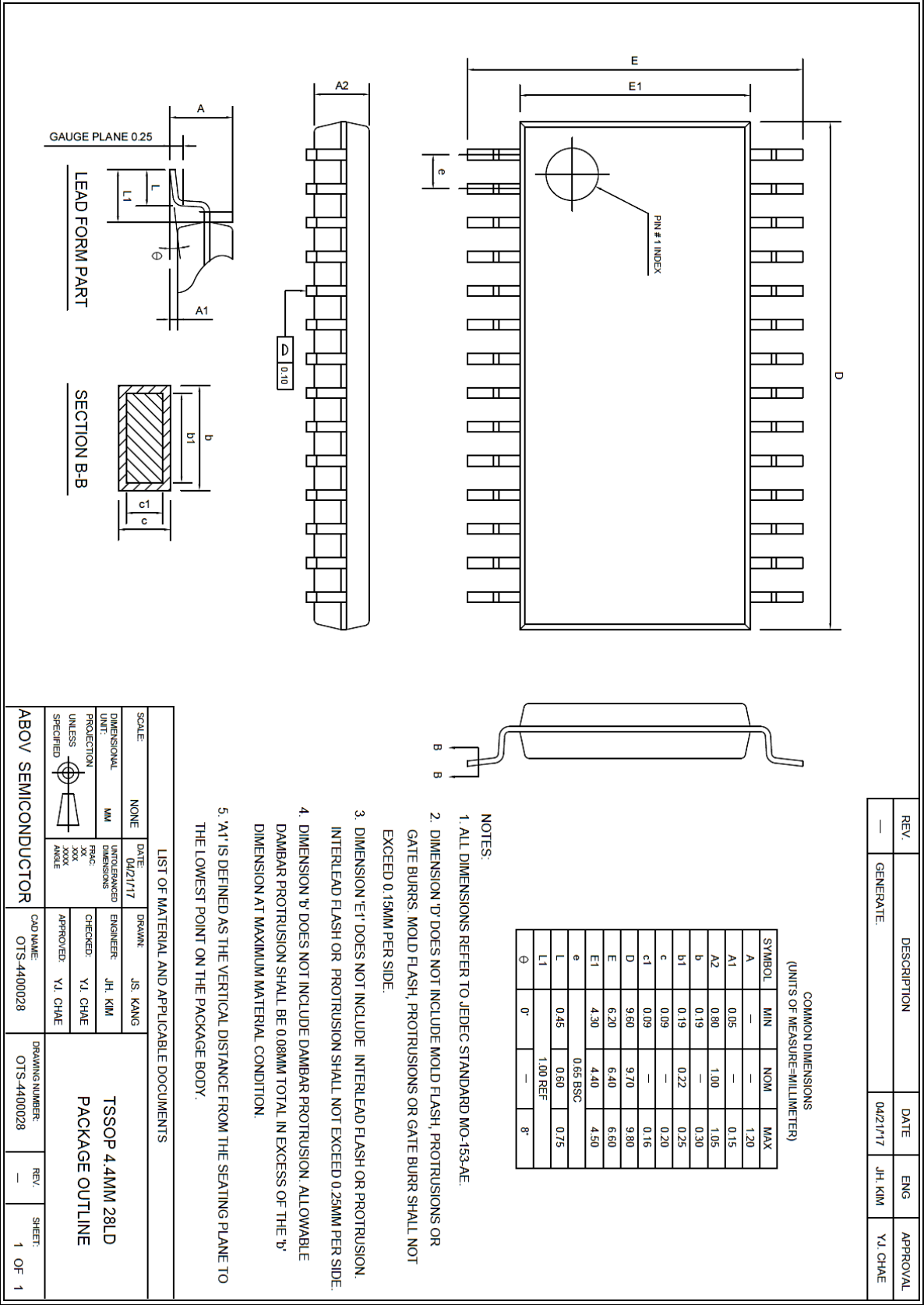
5.4 28-SOP Package Information

Figure 77. 28-SOP Package Outline



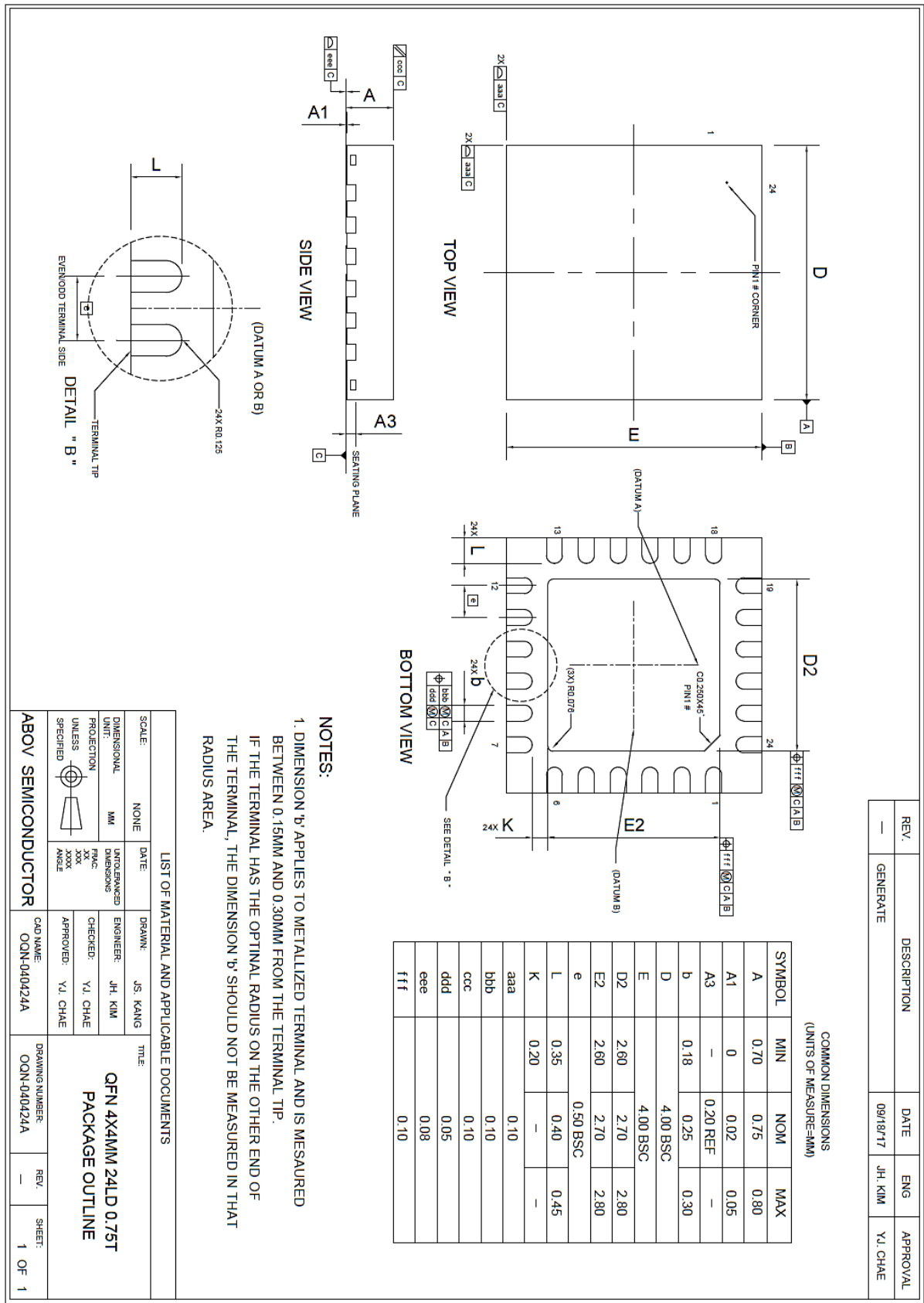
5.5 28-TSSOP Package Information

Figure 78. 28-TSSOP Package Outline



5.6 24-QFN Package Information

Figure 79. 24-QFN Package Outline



6. Ordering Information

Figure 80. MC96F6x32P Device Numbering Nomenclature

MC96F6x32P L		B	2	N
MC96F6x32P Family Name				
x=4	44 Pin			
x=3	32 or 28 Pin			
x=2	24 Pin			
Package type				
L	LQFP			
D	SOP(32 Pin)			
M	SOP(28 Pin)			
R	TSSOP			
U	QFN			
Br (Bromine) free				
B	yes			
None	No			
Temperature				
none	-40°C ~ 85°C (Commercial grade)			
2	-40°C ~ 105°C (Industrial grade)			
Material of Bonding wire				
None	Au			
N	Cu			

NOTE:

1. For more information on any aspect of this device, please contact your nearest distributor or [ABOV sales office](#).

Appendix

A. Configure Option

Register Description: Configure Option Control

CONFIGURE OPTION 2: ROM Address 003FH

7	6	5	4	3	2	1	0
R_P	HL	–	VAPEN	–	–	–	RSTS

Initial value: 00H

R_P	Code Read Protection
0	Disable
1	Enable
HL	Code Write Protection
0	Disable
1	Enable
VAPEN	Vector Area (00H – FFH) Write Protection
0	Disable Protection (Erasable by instruction)
1	Enable Protection (Not erasable by instruction)
RSTS	Select RESETB pin
0	Disable RESETB pin (P55)
1	Enable RESETB pin

CONFIGURE OPTION 1: ROM Address 003EH

7	6	5	4	3	2	1	0
–	–	–	–	PAEN	PASS2	PASS1	PASS0

Initial value: 00H

PAEN	Enable Specific Area Write Protection		
0	Disable (Erasable by instruction)		
1	Enable (Not erasable by instruction)		
PASS [2:0]	Select Specific Area for Write Protection		
NOTE:			
1. When PAEN = '1', it is applied.			
PASS2	PASS1	PASS0	
0	0	0	0.7 KB (Address 0100H – 03FFH)
0	0	1	1.7 KB (Address 0100H – 07FFH)
0	1	0	2.7 KB (Address 0100H – 0BFFH)
0	1	1	3.7 KB (Address 0100H – 0FFFH)
1	0	0	29.7 KB (Address 0100h – 77FFH)
1	0	1	30.7 KB (Address 0100h – 7BFFH)
1	1	0	31.2 KB (Address 0100h – 7DFFH)
1	1	1	31.5 KB (Address 0100h – 7EFFH)

B. Instruction Table

- Instructions are either 1, 2 or 3 bytes long as listed in the 'Bytes' column in tables shown below.
- Each instruction takes either 1, 2 or 4 machine cycles to execute as listed in the following tables in this section.
- 1 machine cycle comprises 2 system clock cycles.

Table 41. Instruction Table: Arithmetic

Arithmetic				
Mnemonic	Description	Bytes	Cycles	Hex code
ADD A,Rn	Add register to A	1	1	28-2F
ADD A,dir	Add direct byte to A	2	1	25
ADD A,@Ri	Add indirect memory to A	1	1	26-27
ADD A,#data	Add immediate to A	2	1	24
ADDC A,Rn	Add register to A with carry	1	1	38-3F
ADDC A,dir	Add direct byte to A with carry	2	1	35
ADDC A,@Ri	Add indirect memory to A with carry	1	1	36-37
ADDC A,#data	Add immediate to A with carry	2	1	34
SUBB A,Rn	Subtract register from A with borrow	1	1	98-9F
SUBB A,dir	Subtract direct byte from A with borrow	2	1	95
SUBB A,@Ri	Subtract indirect memory from A with borrow	1	1	96-97
SUBB A,#data	Subtract immediate from A with borrow	2	1	94
INC A	Increment A	1	1	04
INC Rn	Increment register	1	1	08-0F
INC dir	Increment direct byte	2	1	05
INC @Ri	Increment indirect memory	1	1	06-07
DEC A	Decrement A	1	1	14
DEC Rn	Decrement register	1	1	18-1F
DEC dir	Decrement direct byte	2	1	15
DEC @Ri	Decrement indirect memory	1	1	16-17
INC DPTR	Increment data pointer	1	2	A3
MUL AB	Multiply A by B	1	4	A4
DIV AB	Divide A by B	1	4	84
DAA	Decimal Adjust A	1	1	D4

Table 42. Instruction Table: Logical

Logical				
Mnemonic	Description	Bytes	Cycles	Hex code
ANL A,Rn	AND register to A	1	1	58-5F
ANL A,dir	AND direct byte to A	2	1	55
ANL A,@Ri	AND indirect memory to A	1	1	56-57
ANL A,#data	AND immediate to A	2	1	54
ANL dir,A	AND A to direct byte	2	1	52
ANL dir,#data	AND immediate to direct byte	3	2	53
ORL A,Rn	OR register to A	1	1	48-4F
ORL A,dir	OR direct byte to A	2	1	45
ORL A,@Ri	OR indirect memory to A	1	1	46-47
ORL A,#data	OR immediate to A	2	1	44
ORL dir,A	OR A to direct byte	2	1	42
ORL dir,#data	OR immediate to direct byte	3	2	43
XRL A,Rn	Exclusive-OR register to A	1	1	68-6F
XRL A,dir	Exclusive-OR direct byte to A	2	1	65
XRL A, @Ri	Exclusive-OR indirect memory to A	1	1	66-67
XRL A,#data	Exclusive-OR immediate to A	2	1	64
XRL dir,A	Exclusive-OR A to direct byte	2	1	62
XRL dir,#data	Exclusive-OR immediate to direct byte	3	2	63
CLR A	Clear A	1	1	E4
CPL A	Complement A	1	1	F4
SWAP A	Swap Nibbles of A	1	1	C4
RL A	Rotate A left	1	1	23
RLC A	Rotate A left through carry	1	1	33
RR A	Rotate A right	1	1	03
RRC A	Rotate A right through carry	1	1	13

Table 43. Instruction Table: Data Transfer

Data transfer				
Mnemonic	Description	Bytes	Cycles	Hex code
MOV A,Rn	Move register to A	1	1	E8-EF
MOV A,dir	Move direct byte to A	2	1	E5
MOV A,@Ri	Move indirect memory to A	1	1	E6-E7
MOV A,#data	Move immediate to A	2	1	74
MOV Rn,A	Move A to register	1	1	F8-FF
MOV Rn,dir	Move direct byte to register	2	2	A8-AF
MOV Rn,#data	Move immediate to register	2	1	78-7F
MOV dir,A	Move A to direct byte	2	1	F5
MOV dir,Rn	Move register to direct byte	2	2	88-8F
MOV dir,dir	Move direct byte to direct byte	3	2	85
MOV dir,@Ri	Move indirect memory to direct byte	2	2	86-87
MOV dir,#data	Move immediate to direct byte	3	2	75
MOV @Ri,A	Move A to indirect memory	1	1	F6-F7
MOV @Ri,dir	Move direct byte to indirect memory	2	2	A6-A7
MOV @Ri,#data	Move immediate to indirect memory	2	1	76-77
MOV DPTR,#data	Move immediate to data pointer	3	2	90
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	2	93
MOVC A,@A+PC	Move code byte relative PC to A	1	2	83
MOVX A,@Ri	Move external data(A8) to A	1	2	E2-E3
MOVX A,@DPTR	Move external data(A16) to A	1	2	E0
MOVX @Ri,A	Move A to external data(A8)	1	2	F2-F3
MOVX @DPTR,A	Move A to external data(A16)	1	2	F0
PUSH dir	Push direct byte onto stack	2	2	C0
POP dir	Pop direct byte from stack	2	2	D0
XCH A,Rn	Exchange A and register	1	1	C8-CF
XCH A,dir	Exchange A and direct byte	2	1	C5
XCH A,@Ri	Exchange A and indirect memory	1	1	C6-C7
XCHD A,@Ri	Exchange A and indirect memory nibble	1	1	D6-D7

Table 44. Instruction Table: Boolean

Boolean				
Mnemonic	Description	Bytes	Cycles	Hex code
CLR C	Clear carry	1	1	C3
CLR bit	Clear direct bit	2	1	C2
SETB C	Set carry	1	1	D3
SETB bit	Set direct bit	2	1	D2
CPL C	Complement carry	1	1	B3
CPL bit	Complement direct bit	2	1	B2
ANL C,bit	AND direct bit to carry	2	2	82
ANL C,/bit	AND direct bit inverse to carry	2	2	B0
ORL C,bit	OR direct bit to carry	2	2	72
ORL C,/bit	OR direct bit inverse to carry	2	2	A0
MOV C,bit	Move direct bit to carry	2	1	A2
MOV bit,C	Move carry to direct bit	2	2	92

Table 45. Instruction Table: Branching

Branching				
Mnemonic	Description	Bytes	Cycles	Hex code
ACALL addr 11	Absolute jump to subroutine	2	2	11→F1
LCALL addr 16	Long jump to subroutine	3	2	12
RET	Return from subroutine	1	2	22
RETI	Return from interrupt	1	2	32
AJMP addr 11	Absolute jump unconditional	2	2	01→E1
LJMP addr 16	Long jump unconditional	3	2	02
SJMP rel	Short jump (relative address)	2	2	80
JC rel	Jump on carry = 1	2	2	40
JNC rel	Jump on carry = 0	2	2	50
JB bit,rel	Jump on direct bit = 1	3	2	20
JNB bit,rel	Jump on direct bit = 0	3	2	30
JBC bit,rel	Jump on direct bit = 1 and clear	3	2	10
JMP @A+DPTR	Jump indirect relative DPTR	1	2	73
JZ rel	Jump on accumulator = 0	2	2	60
JNZ rel	Jump on accumulator ≠0	2	2	70
CJNE A,dir,rel	Compare A,direct jne relative	3	2	B5
CJNE A,#d,rel	Compare A,immediate jne relative	3	2	B4
CJNE Rn,#d,rel	Compare register, immediate jne relative	3	2	B8-BF
CJNE @Ri,#d,rel	Compare indirect, immediate jne relative	3	2	B6-B7
DJNZ Rn,rel	Decrement register, jnz relative	2	2	D8-DF
DJNZ dir,rel	Decrement direct byte, jnz relative	3	2	D5

Table 46. Instruction Table: Miscellaneous

Miscellaneous				
Mnemonic	Description	Bytes	Cycles	Hex code
NOP	No operation	1	1	00

Table 47. Instruction Table: Additional Instructions

Additional instructions (selected through EO[7:4])				
Mnemonic	Description	Bytes	Cycles	Hex code
MOVC @DPTR++,A	M8051W/M8051EW-specific instruction supporting software download into program memory	1	2	A5
TRAP	Software break command	1	1	A5

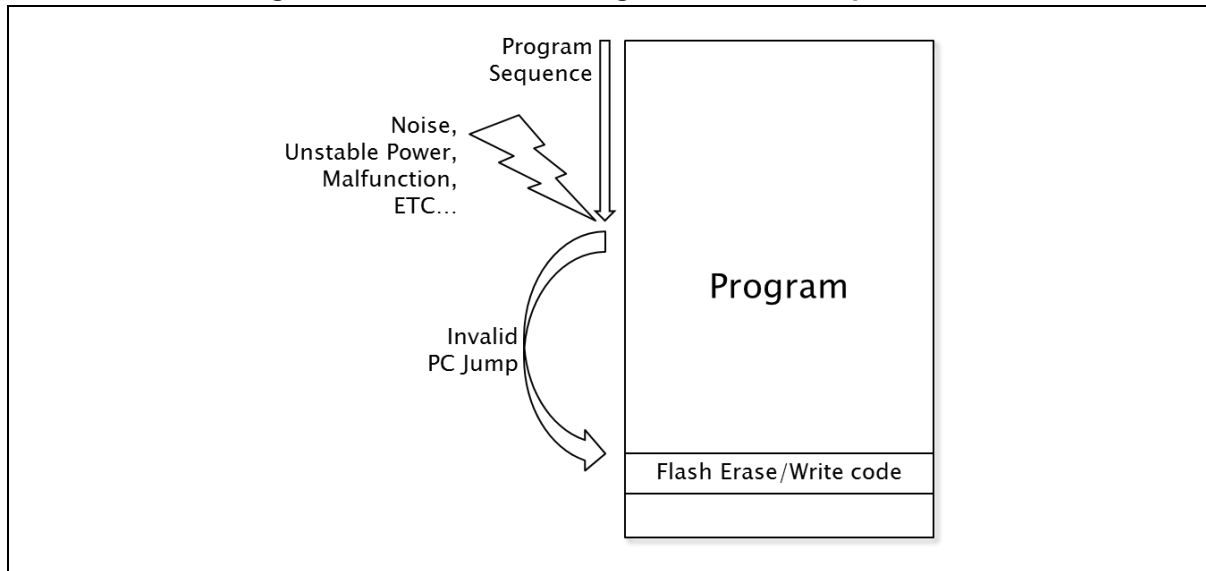
In the above table, an entry such as E8-EF indicates a continuous block of hex opcodes used for 8 different registers, and the register numbers of which are defined by the lowest three bits of the corresponding code. Non-continuous blocks of codes, shown as 11→F1 (for example), are used for absolute jumps and calls, with the top 3 bits of the code being used to store the top three bits of the destination address.

The CJNE instructions use the abbreviation #d for immediate data; other instructions use #data.

C. Flash Protection for Invalid Erase/Write

Appendix C shows example code to prevent code or data from being changed by abnormal operations such as noise, unstable power, and malfunction.

Figure 81. Flash Protection Against Abnormal Operations



How to Protect the Flash

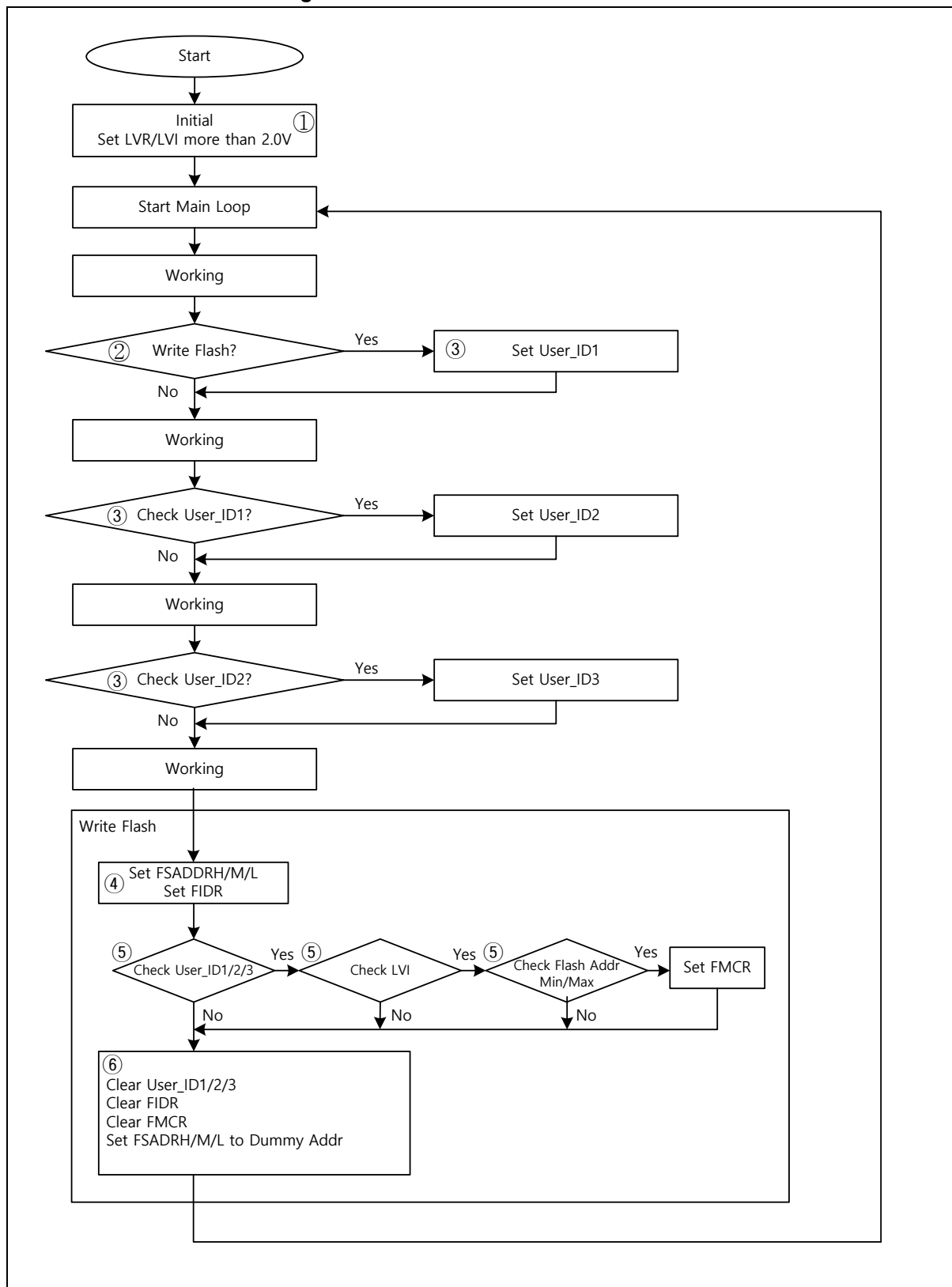
- Divide into decision and execution to Erase/Write in Flash.
 - Check the program sequence from decision to execution in order of precedence about Erase/Write.
 - Setting the flags in program and checking the flags in main loop at the end
 - When the Flash Erase/Write is executed, check the flags. If not matched, do not execute.
- Check the range of Flash Sector Address
 - If the Flash sector address is outside of specific area, do not execute.
- Use the Dummy Address
 - Set the Flash sector address to dummy address in usually run time.
 - Change the Flash sector address to real area range shortly before Erase/Write.
 - Even if invalid Erase/Write occurs, it will be Erase/Write in dummy address in Flash.
- Use the LVR/LVI
 - Unstable or low power gives an adverse effect on the microcontroller. So, use the LVR/LVI.

Protection Flow Description

The Flash protection procedure is described in flowchart in Figure 82, and each step in this figure is described in the following lists:

1. Initialization
 - A. Set the LVR/LVI. Check the power by LVR/LVI and do not execute under unstable or low power.
 - B. Initialize User_ID1/2/3
 - C. Set Flash Sector Address High/Middle/Low to Dummy address. Dummy address is set to unused area range in Flash.
2. Decide to Write
 - A. When the Erase/Write are determined, set flag. Do not directly Erase/Write in Flash.
 - B. Make the user data.
3. Check and Set User_ID1/2/3
 - A. In the middle of source, insert code which can check and set the flags.
 - B. By setting the User_ID 1/2/3 sequentially and identifying the flow of the program.
4. Set Flash Sector Address
 - A. Set address to real area range shortly before Erase/Write in Flash.
 - B. Set to Dummy address after Erase/Write. Even if invalid work occurs, it will be Erase/Write in Dummy address in Flash.
5. Check Flags
 - A. If every flag (User_ID1/2/3, LVI, Flash Address Min/Max) was set, then do Erase/Write.
 - B. If the Flash Sector Address is outside of Min/Max, do not execute
 - C. Address Min/Max is set to unused area.
6. Initialize Flags
 - A. Initialize User_ID1/2/3
 - B. Set Flash Sector Address to Dummy Address
- Sample Source
 - Refer to the ABOV website (www.abovsemi.com).
 - It is created based on the MC97F2664.
 - Each product should be modified according to the Page Buffer Size and Flash Size

Figure 82. Flowchart of Flash Protection



Other Protection by the Configure Options

- Protection by Configure option
 - Set Flash protection by the microcontroller's Write Tool (OCD, PGM+, etc.)
 - Vector Area:
00H~FFH
 - Specific Area (MC96F6432P):
0.7 KB (Address 0100H – 03FFH)
1.7 KB (Address 0100H – 07FFH)
2.7 KB (Address 0100H – 0BFFH)
3.8 KB (Address 0100H – 0FFFH)
29.7 KB (Address 0100h – 77FFH)
30.7 KB (Address 0100h – 7BFFH)
31.2 KB (Address 0100h – 7DFFH)
31.5 KB (Address 0100h – 7EFFH)
 - The range of protection may be different for each product.

Revision History

Revision	Date	Note
1.00	Feb. 17, 2025	Initial release
1.10	Jul. 9, 2025	• Added 32-SOP package. • Corrected typos.

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