

PSoC™ 4 MCU: PSoC™ 4200L Automotive

Based on Arm® Cortex®-M0

General description

PSoC™ 4 is a scalable and reconfigurable platform architecture for a family of programmable embedded system controllers with an Arm® Cortex®-M0 CPU. It combines programmable and reconfigurable analog and digital blocks with flexible automatic routing. The PSoC™ 4200L product family, based on this platform, is a combination of a microcontroller with digital programmable logic, programmable analog, programmable interconnect, secure expansion of memory off-chip, high-performance analog-to-digital conversion, opamps with Comparator mode, and standard communication and timing peripherals. The PSoC™ 4200L products will be fully compatible with members of the PSoC™ 4 platform for new applications and design needs. The programmable analog and digital subsystems allow flexibility and in-field tuning of the design.

Features

- 32-bit MCU subsystem
 - 48 MHz Arm® Cortex®-M0 CPU with single-cycle multiply
 - Up to 256 kB of flash with read accelerator
 - Up to 32 kB of SRAM
 - DMA engine with 32 channels
- Programmable analog
 - Four opamps that operate in Deep Sleep mode at very low current levels
 - All opamps have reconfigurable high current pin-drive, high-bandwidth internal drive, ADC input buffering, and Comparator modes with flexible connectivity allowing input connections to any pin
 - Four current DACs (IDACs) for general-purpose or capacitive sensing applications on any pin
 - Two low-power comparators that operate in Deep Sleep mode
- Programmable digital
 - Eight programmable logic blocks, each with 8 Macrocells and an 8-bit data path (called universal digital blocks or UDBs)
 - Infineon-provided peripheral component library, user-defined state machines, and Verilog input
- Low-power 1.71 V to 5.5 V operation
 - 20-nA Stop Mode with GPIO pin wakeup
 - Hibernate and Deep Sleep modes allow wakeup-time versus power trade-offs
- Capacitive sensing
 - Two capacitive sigma-delta blocks provide best-in-class SNR (>5:1) and water tolerance
 - Infineon-supplied software component makes capacitive sensing design easy
 - Automatic hardware tuning (SmartSense)
- Segment LCD drive
 - LCD drive supported on any pin with up to a maximum of 64 outputs (common or segment)
 - Operates in Deep Sleep mode with 4 bits per pin memory
- Serial communication
 - Four independent run-time reconfigurable Serial Communication Blocks (SCBs) with reconfigurable I²C, SPI, or UART functionality
 - USB Full-Speed device interface 12 Mbits/sec with Battery Charger Detect capability
 - Two independent CAN blocks for industrial and automotive networking
- Timing and pulse-width modulation
 - Eight 16-bit timer/counter pulse-width modulator (TCPWM) blocks
 - Center-aligned, Edge, and Pseudo-random modes
 - Comparator-based triggering of Kill signals for motor drive and other high-reliability digital logic applications

Features

- Up to 98 programmable GPIOs
 - 124-ball VFBGA package
 - Any of up to 94 GPIO pins can be CAPSENSE™, analog, or digital
 - Drive modes, strengths, and slew rates are programmable
- PSoC™ Creator design environment
 - Integrated development environment (IDE) provides schematic design entry and build (with analog and digital automatic routing)
 - Applications programming interface (API) component for all fixed-function and programmable peripherals
- Industry-standard tool compatibility
 - After schematic entry, development can be done with Arm®-based industry-standard development tools

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More information

1 More information

Infineon provides a wealth of data at www.infineon.com to help you to select the right PSoC™ device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article [KBA86521, How to Design with PSoC™ 3, PSoC™ 4, and PSoC™ 5LP](#). Following is an abbreviated list for PSoC™ 4:

- Overview: [PSoC™ Portfolio, PSoC™ Roadmap](#)
- Product Selectors: [PSoC™ 1, PSoC™ 3, PSoC™ 4, PSoC™ 5LP](#)
In addition, PSoC™ Creator includes a device selection tool.
- Application notes: Infineon offers a large number of PSoC™ application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC™ 4 are:
 - [AN79953](#): Getting started with PSoC™ 4
 - [AN88619](#): PSoC™ 4 hardware design considerations
 - [AN86439](#): Using PSoC™ 4 GPIO pins
 - [AN57821](#): Mixed signal circuit board layout
 - [AN81623](#): Digital design best practices
 - [AN73854](#): Introduction to bootloaders
 - [AN89610](#): Arm® Cortex® code optimization
 - [AN85951](#): PSoC™ 4 and PSoC™ 6 MCU CAPSENSE™ design guide
- Technical reference manual (TRM) is in two documents:
 - [Architecture TRM](#) details each PSoC™ 4 functional block.
 - [Registers TRM](#) describes each of the PSoC™ 4 registers.
- Development kits:
 - [CY8CKIT-042](#), PSoC™ 4 pioneer kit, is an easy-to-use and inexpensive development platform. This kit includes connectors for Arduino™ compatible shields and Digilent® Pmod™ daughter cards.
 - [CY8CKIT-046](#), PSoC™ 4 L-Series pioneer kit, is an easy-to-use and inexpensive development platform. This kit includes connectors for Arduino™ compatible shields.
 - [CY8CKIT-049](#) is a very low-cost prototyping platform. It is a low-cost alternative to sampling PSoC™ 4 devices.
 - [CY8CKIT-001](#) is a common development platform for any one of the PSoC™ 1, PSoC™ 3, PSoC™ 4, or PSoC™ 5LP families of devices.

The [MiniProg3](#) device provides an interface for flash programming and debug.

2 PSoC™ Creator

PSoC™ Creator is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC™ 3, PSoC™ 4, and PSoC™ 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC™ Components; see the [list of component datasheets](#). With PSoC™ Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC™ hardware, using the PSoC™ Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

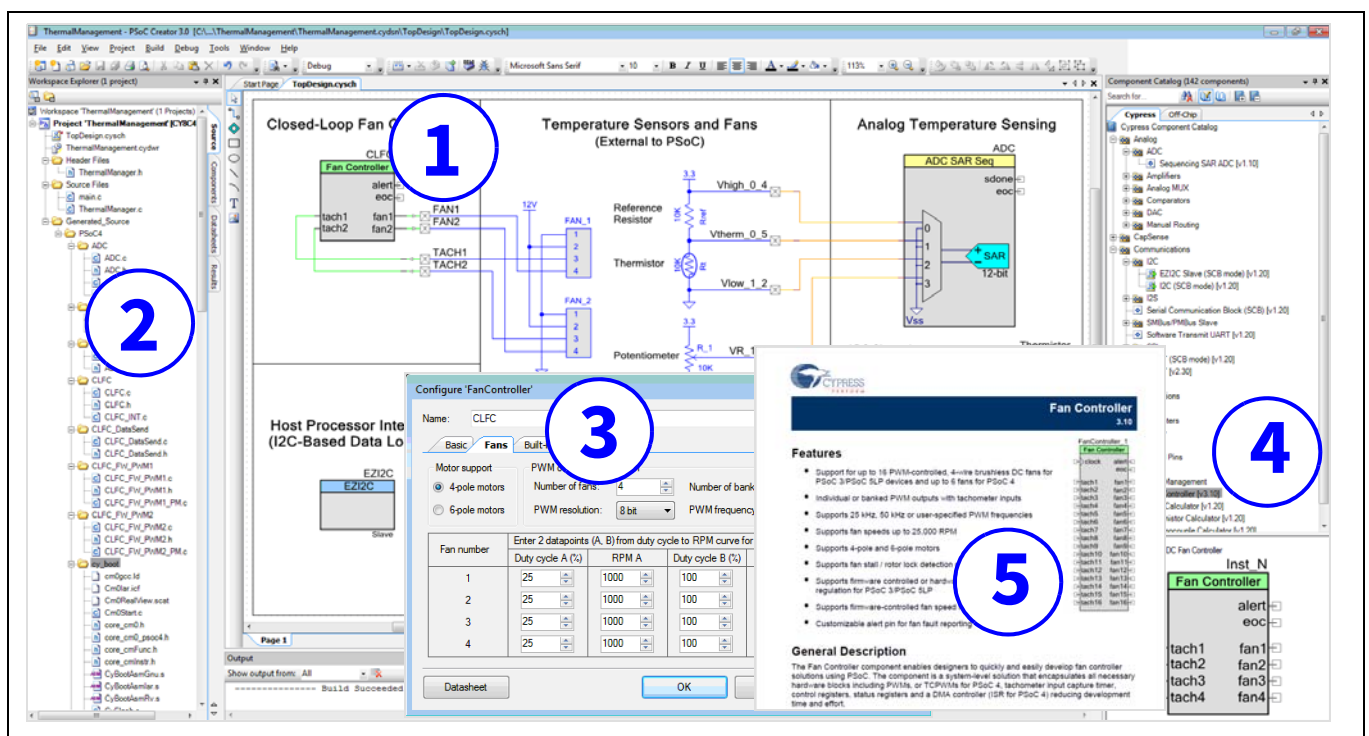


Figure 1 Multiple-sensor example project in PSoC™ Creator contents

3 PSoC™ 4200L block diagram

The PSoC™ 4200L devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The Arm® serial wire debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC™ Creator IDE provides fully integrated programming and debug support for PSoC™ 4200L devices. The SWD interface is fully compatible with industry-standard third-party tools. The PSoC™ 4200L family provides a level of security not possible with multi-chip application solutions or with microcontrollers. This is due to its ability to disable debug features, robust flash protection, and because it allows customer-proprietary functionality to be implemented in on-chip programmable blocks.

The debug circuits are enabled by default and can only be disabled in firmware. If not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. Because all programming, debug, and test interfaces are disabled when maximum device security is enabled, PSoC™ 4200L with device security enabled may not be returned for failure analysis. This is a trade-off the PSoC™ 4200L allows the customer to make.

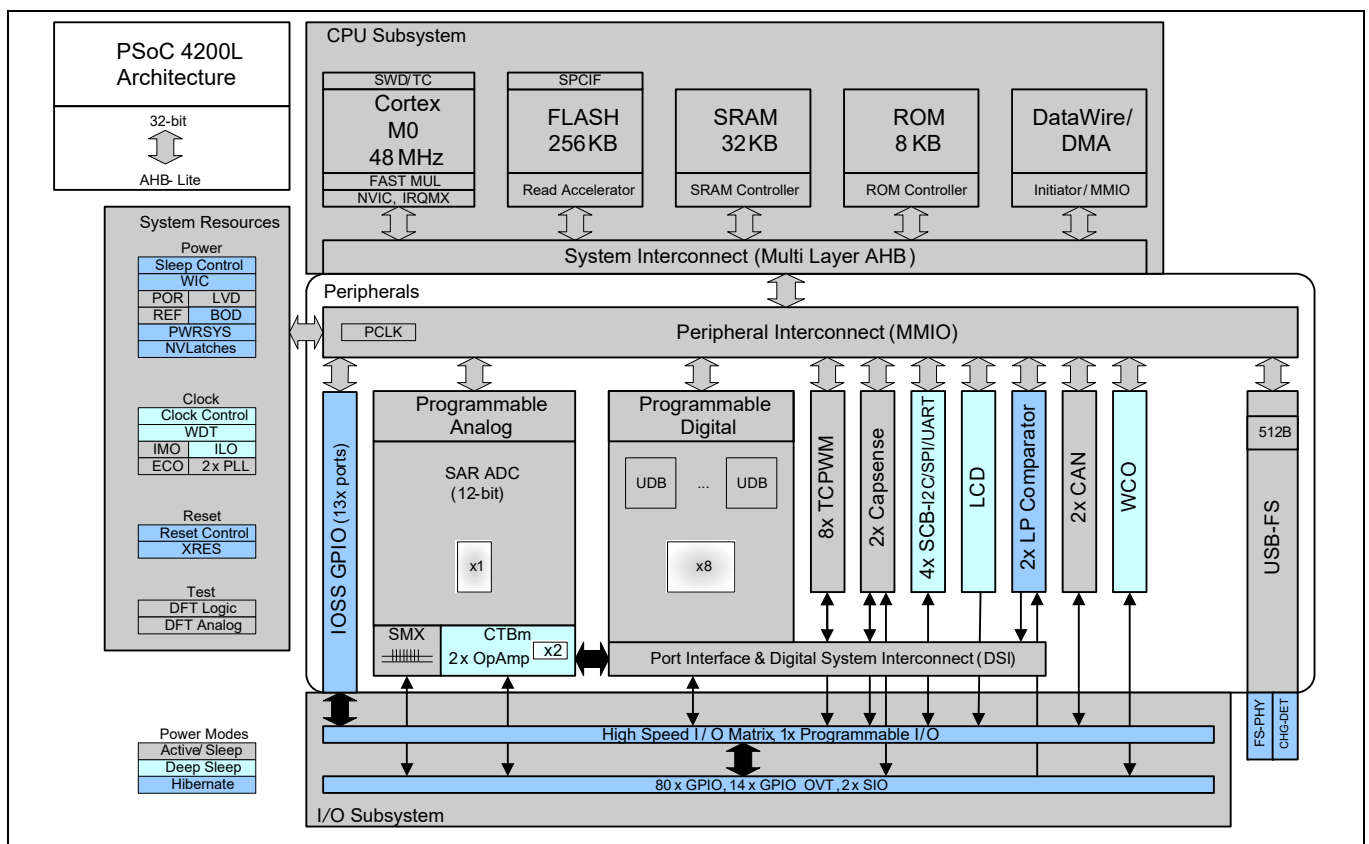


Figure 2 Block diagram

4 Functional definition

4.1 CPU and memory subsystem

4.1.1 CPU

The Cortex®-M0 CPU in the PSoC™ 4200L is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and execute a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex®-M3 and M4, thus enabling upward compatibility. The Infineon implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC), which can wake the processor up from the Deep Sleep mode allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex®-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a 2-wire form of JTAG; the debug configuration used for PSoC™ 4200L has four break-point (address) comparators and two watchpoint (data) comparators.

4.1.2 Flash

The PSoC™ 4200L has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 2 wait-state (WS) access time at 48 MHz and with 1-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

4.1.3 SRAM

SRAM memory is retained during Hibernate.

4.1.4 SROM

A supervisory ROM that contains boot and configuration routines is provided.

4.1.5 DMA

A DMA engine is provided that can do 32-bit transfers and has chainable ping-pong descriptors.

4.2 System resources

4.2.1 Power system

The power system is described in detail in the section **“Power”** on page 20. It provides assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (brown-out detect (BOD)) or interrupts (low voltage detect (LVD)). The PSoC™ 4200L operates with a single external supply over the range of 1.71 to 5.5 V and has five different power modes, transitions between which are managed by the power system. The PSoC™ 4200L provides Sleep, Deep Sleep, Hibernate, and Stop low-power modes.

4.2.2 Clock system

The PSoC™ 4200L clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no meta-stable conditions occur.

The clock system for the PSoC™ 4200L consists of a crystal oscillator (4 to 33 MHz), a watch crystal oscillator (32 kHz), a phase-locked loop (PLL), the IMO and the ILO internal oscillators, and provision for an external clock.

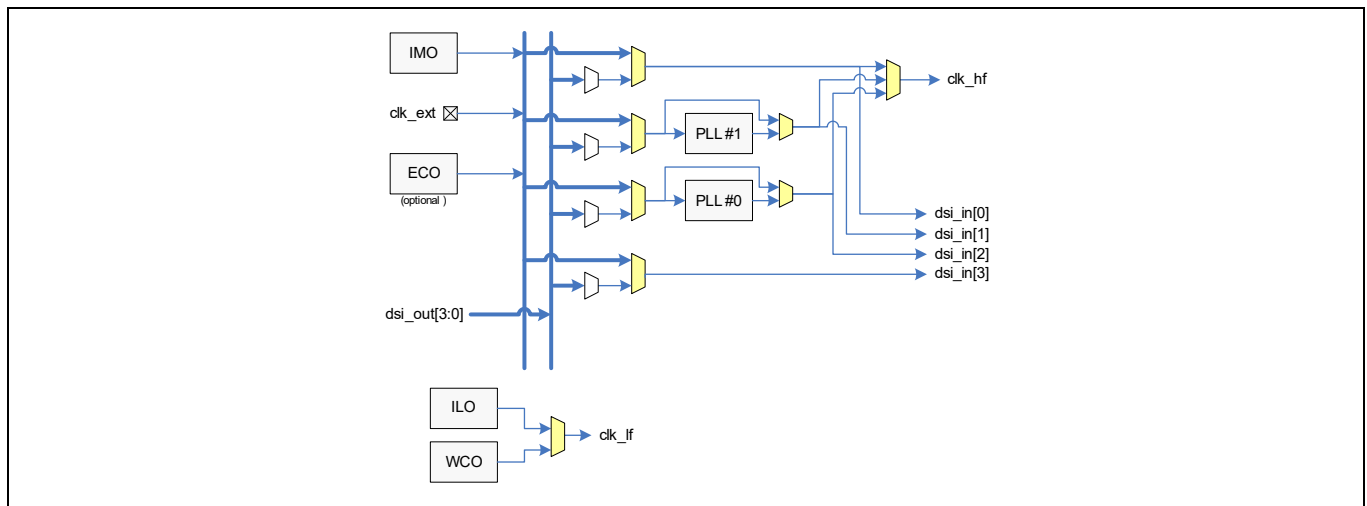


Figure 3 PSoC™ 4200L MCU clocking architecture

The clk_hf signal can be divided down to generate synchronous clocks for the UDBs, and the analog and digital peripherals. There are a total of 16 clock dividers for the PSoC™ 4200L, each with 16-bit divide capability; this allows 12 to be used for the fixed-function blocks and four for the UDBs. The analog clock leads the digital clocks to allow analog events to occur before digital clock-related noise is generated. The 16-bit capability allows a lot of flexibility in generating fine-grained frequency values and is fully supported in PSoC™ Creator.

4.2.3 IMO clock source

The IMO is the primary source of internal clocking in the PSoC™ 4200L. It is trimmed during testing to achieve the specified accuracy. Trim values are stored in nonvolatile latches (NVL). Additional trim settings from flash can be used to compensate for changes. The IMO default frequency is 24 MHz and it can be adjusted between 3 to 48 MHz in steps of 1 MHz. IMO tolerance with Infineon-provided calibration settings is $\pm 2\%$.

4.2.4 ILO clock source

The ILO is a very low power oscillator, nominally 32 kHz, which is primarily used to generate clocks for peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Infineon provides a software component, which does the calibration.

4.2.5 Crystal oscillators and PLL

The PSoC™ 4200L clock subsystem also implements two oscillators: high-frequency (4 to 33 MHz) and low-frequency (32-kHz watch crystal) that can be used for precision timing applications. The PLL can generate a 48-MHz output from the high-frequency oscillator.

4.2.6 Watchdog timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the timeout occurs. The watchdog reset is recorded in the Reset Cause register.

4.2.7 Reset

The PSoC™ 4200L can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset to avoid complications with configuration and multiple pin functions during power-on or reconfiguration.

4.2.8 Voltage reference

The PSoC™ 4200L reference system generates all internally required references. A 1% voltage reference spec is provided for the 12-bit ADC. To allow better signal-to-noise ratios (SNR) and better absolute accuracy, it is possible to add an external bypass capacitor to the internal reference using a GPIO pin or to use an external reference for the SAR.

4.3 Analog blocks

4.3.1 12-bit SAR ADC

The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The block functionality is augmented for the user by adding a reference buffer to it (trimmable to $\pm 1\%$) and by providing the choice (for the PSoC™ 4200L case) of three internal voltage references: V_{DD} , $V_{DD}/2$, and V_{REF} (nominally 1.024 V) as well as an external reference through a GPIO pin. The Sample-and-Hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. The system performance will be 65 dB for true 12-bit precision if appropriate references are used and system noise levels permit. To improve performance in noisy conditions, it is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer (expandable to 16 inputs). The sequencer cycles through selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, the aggregate sampling bandwidth is equal to 1 Msps, whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware-driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. In addition, the signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is able to digitize the output of the on-board temperature sensor for calibration and other temperature-dependent functions. The SAR is not available in Deep Sleep and Hibernate modes as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 to 5.5 V.

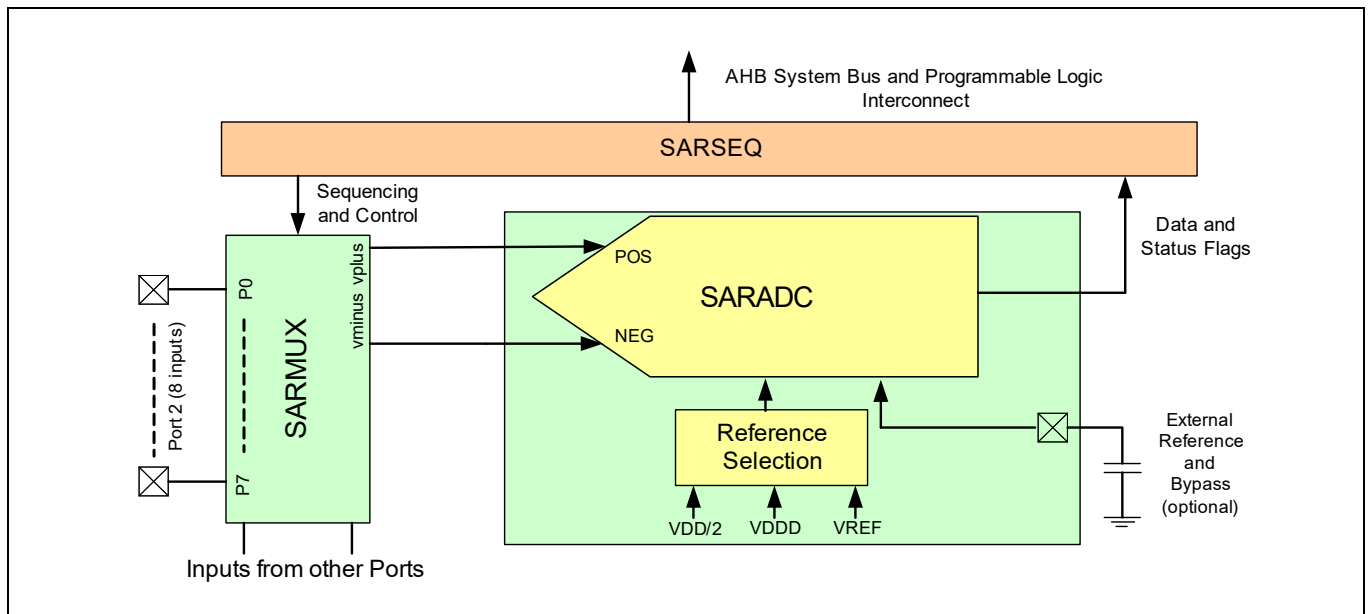


Figure 4 SAR ADC system diagram

4.3.2 Analog multiplex bus

The PSoC™ 4200L has two concentric analog buses (Analog Mux Bus A and Analog Mux Bus B) that circumnavigate the periphery of the chip. These buses can transport analog signals from any pin to various analog blocks (including the opamps) and to the CAPSENSE™ blocks allowing, for instance, the ADC to monitor any pin on the chip. These buses are independent and can also be split into three independent sections. This allows one section to be used for CAPSENSE™ purposes, one for general analog signal processing, and the third for general-purpose digital peripherals and GPIO.

4.3.3 Four opamps (CTBm Blocks)

The PSoC™ 4200L has four opamps with Comparator modes, which allow most common analog functions to be performed on-chip eliminating external components; PGAs, voltage buffers, filters, trans-impedance amplifiers, and other functions can be realized with external passives saving power, cost, and space. The on-chip opamps are designed with enough bandwidth to drive the Sample-and-Hold circuit of the ADC without requiring external buffering. The opamps can operate in the Deep Sleep mode at very low power levels. The following diagram shows one of two identical opamp pairs of the opamp subsystem.

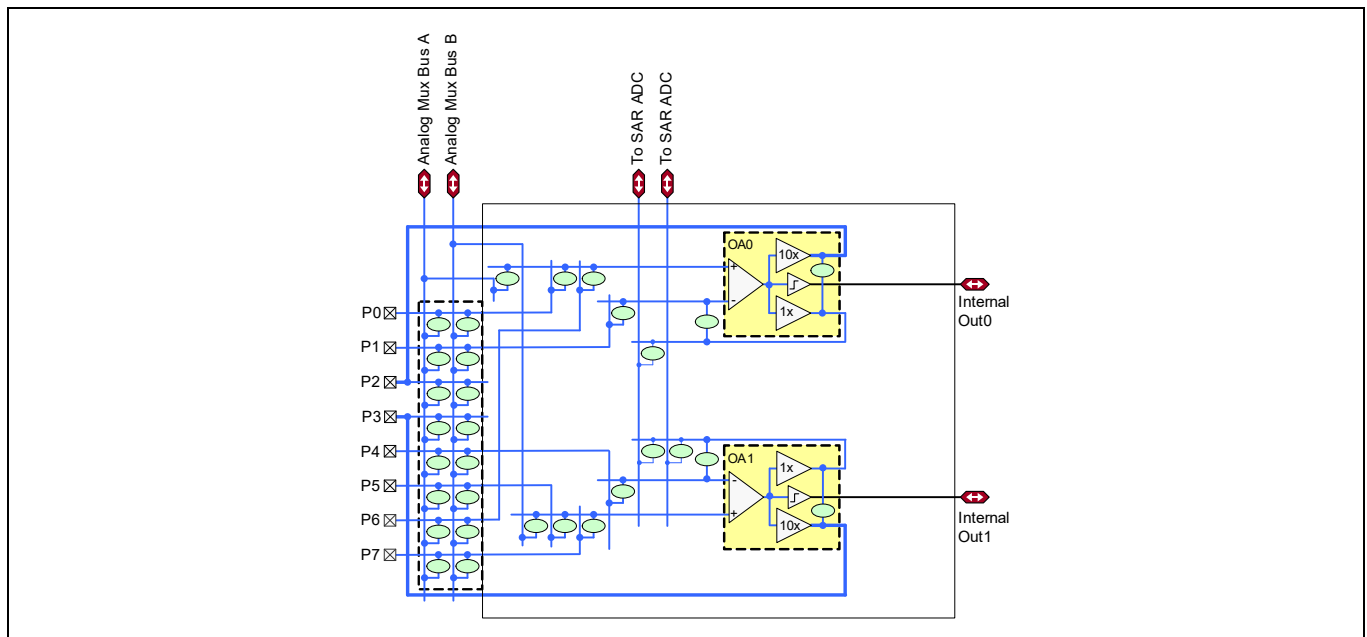


Figure 5 Identical opamp pairs in opamp subsystem

The ovals in [Figure 5](#) represent analog switches, which may be controlled via user firmware, the SAR sequencer, or user-defined programmable logic. The opamps (OA0 and OA1) are configurable via these switches to perform all standard opamp functions with appropriate feedback components.

The opamps (OA0 and OA1) are programmable and reconfigurable to provide standard opamp functionality via switchable feedback components, unity gain functionality for driving pins directly, or for internal use (such as buffering SAR ADC inputs as indicated in the diagram), or as true comparators.

The opamp inputs provide highly flexible connectivity and can connect directly to dedicated pins or, via the analog mux buses, to any pin on the chip. Analog switch connectivity is controllable by user firmware as well as user-defined programmable digital state machines (implemented via UDBs).

The opamps operate in Deep Sleep mode at very low currents allowing analog circuits to remain operational during Deep Sleep.

4.3.4 Temperature sensor

The PSoC™ 4200L has one on-chip temperature sensor. This consists of a diode, which is biased by a current source that can be disabled to save power. The temperature sensor is connected to the ADC, which digitizes the reading and produces a temperature value using Infineon-supplied software that includes calibration and linearization.

4.3.5 Low-power comparators

The PSoC™ 4200L has a pair of low-power comparators, which can also operate in the Deep Sleep and Hibernate modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid meta-stability unless operating in an asynchronous power mode (Hibernate) where the system wake-up circuit is activated by a comparator switch event.

4.4 Programmable digital

4.4.1 Universal digital blocks (UDBs) and port interfaces

The PSoC™ 4200L has eight UDBs; the UDB array also provides a switched Digital System Interconnect (DSI) fabric that allows signals from peripherals and ports to be routed to and through the UDBs for communication and control. The UDB array is shown in the following figure.

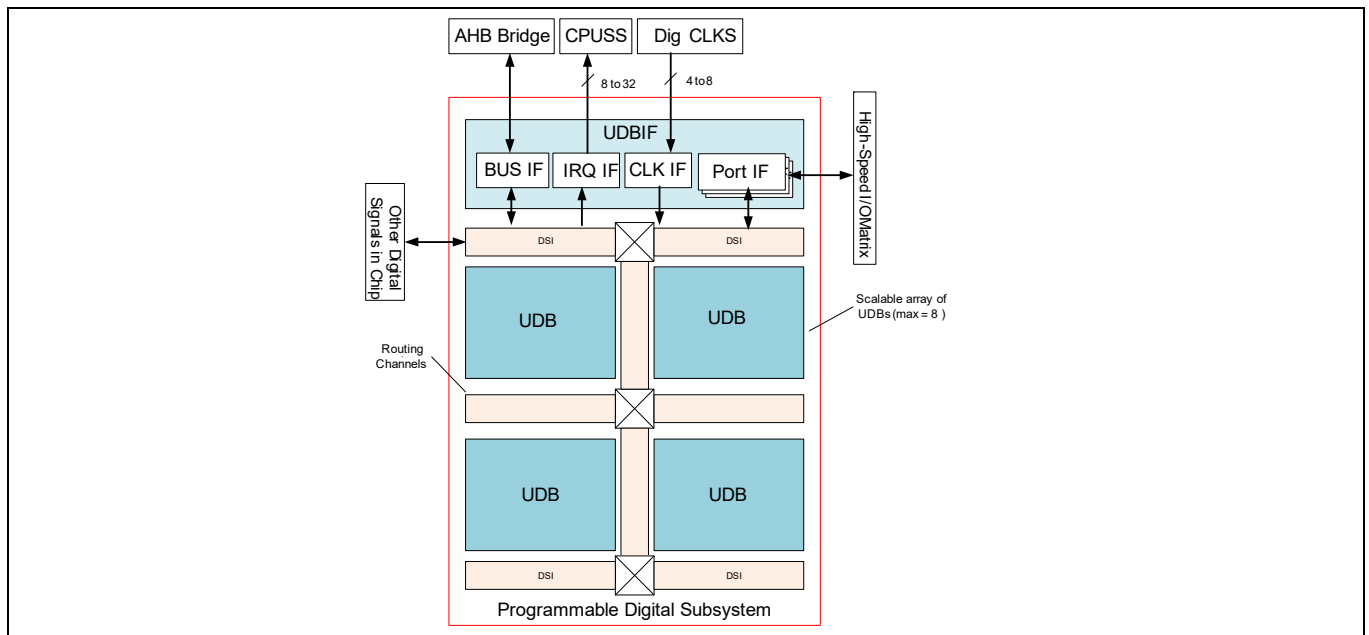


Figure 6 UDB array

UDBs can be clocked from a clock divider block, from a port interface (required for peripherals such as SPI), and from the DSI network directly or after synchronization.

A port interface is defined, which acts as a register that can be clocked with the same source as the PLDs inside the UDB array. This allows faster operation because the inputs and outputs can be registered at the port interface close to the I/O pins and at the edge of the array. The port interface registers can be clocked by one of the I/Os from the same port. This allows interfaces such as SPI to operate at higher clock speeds by eliminating the delay for the port input to be routed over DSI and used to register other inputs. The port interface is shown in **Figure 7**.

The UDBs can generate interrupts (one UDB at a time) to the interrupt controller. The UDBs retain the ability to connect to most of the pins on the chip through the DSI, with the exception of the pins from Port 7, 8, and 9.

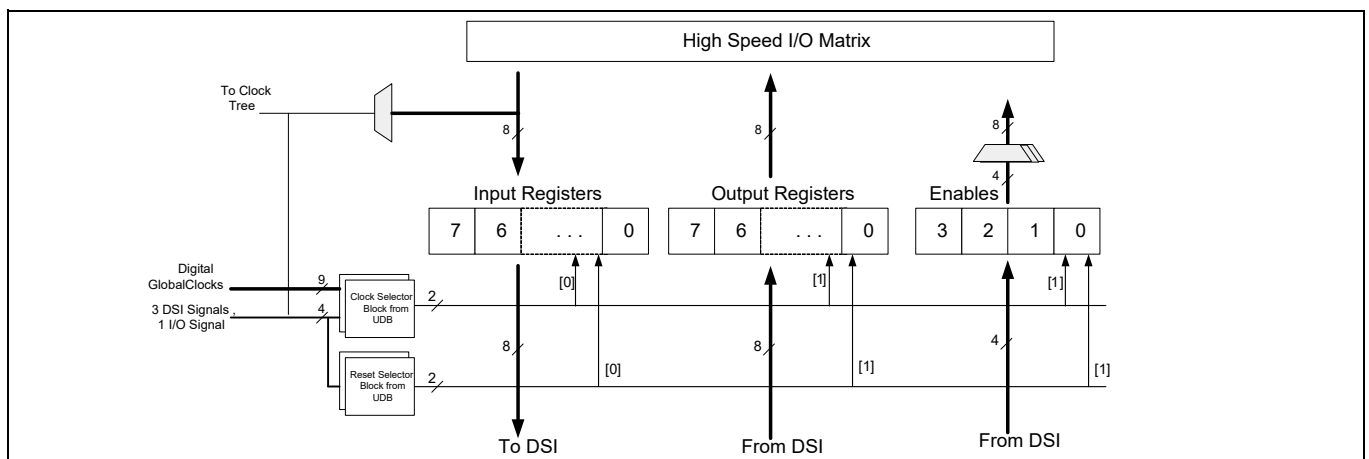


Figure 7 Port interface

4.5 Fixed function digital

4.5.1 Timer/Counter/PWM (TCPWM) block

The TCPWM block consists of one 16-bit counter with user-programmable period length. There is a Capture register to record the count value at the time of an event (which may be an I/O event), a period register which is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals, which are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as deadband programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an overcurrent state is indicated and the PWMs driving the FETs need to be shut off immediately with no time for software intervention. The PSoC™ 4200L has eight TCPWM blocks.

4.5.2 Serial Communication Blocks (SCB)

The PSoC™ 4200L has four SCBs, which can each implement an I²C, UART, or SPI interface.

I²C Mode: The hardware I²C block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EzI2C that creates a mailbox address range in the memory of the PSoC™ 4200L and effectively reduces I²C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time. The FIFO mode is available in all channels and is very useful in the absence of DMA.

The I²C peripheral is compatible with the I²C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I²C-bus specification and user manual (UM10204). The I²C bus I/O is implemented with GPIO in open-drain modes.

UART Mode: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

SPI Mode: The SPI mode supports full Motorola SPI, TI SSP (essentially adds a start pulse used to synchronize SPI Coders), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO.

4.5.3 USB device

A Full-speed USB 2.0 device interface is provided. It has a Control endpoint and eight other endpoints. The interface has a USB transceiver and can be operated from the IMO obviating the need for a crystal oscillator.

4.5.4 CAN blocks

There are two independent CAN 2.0B blocks, which are certified CAN conformant.

4.6 GPIO

The PSoC™ 4200L has 96 GPIOs. The GPIO block implements the following:

- Eight drive strength modes including strong push-pull, resistive pull-up and pull-down, weak (resistive) pull-up and pull-down, open drain and open source, input only, and disabled
- Input threshold select (CMOS or LVTTTL)
- Individual control of input and output disables
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode and Hibernate modes)
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals are also fixed to reduce internal multiplexing complexity (these signals do not go through the DSI network). DSI signals are not affected by this and any pin may be routed to any UDB through the DSI network, with the exception of pins from Port 7, 8, and 9.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (13 for PSoC™ 4200L).

There are 14 GPIO pins that are overvoltage tolerant (V_{IN} can exceed V_{DD}). The overvoltage cells will not sink more than 10 μ A when their inputs exceed V_{DDIO} in compliance with I²C specifications. Meeting the I²C minimum fall time requirement for FM and FM+ may require the slower slew rate setting depending on bus loading (also applies to all GPIO and SIO pins).

4.7 SIO

The Special I/O (SIO) pins have the following features in addition to the GPIO features:

- Overvoltage protection and hot swap capability
- Programmable switching thresholds
- Programmable output pull-up voltage capability

They allow interfacing to buses, such as I²C with full I²C compatibility and interfacing to devices operating at different voltage levels. There are two SIO pins on the PSoC™ 4200L.

4.8 Special function peripherals

4.8.1 LCD segment Drive

The PSoC™ 4200L has an LCD controller, which can drive up to eight commons and up to 56 segments. Any pin can be either a common or a segment pin. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as digital correlation and PWM.

Digital correlation pertains to modulating the frequency and levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays.

PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays.

4.8.2 CAPSENSE™

CAPSENSE™ is supported on all pins in the PSoC™ 4200L through two CAPSENSE™ Sigma-Delta (CSD) blocks that can be connected to any pin through an analog mux bus that any GPIO pin can be connected to via an Analog switch. CAPSENSE™ function can thus be provided on any pin or group of pins in a system under software control. A component is provided for the CAPSENSE™ block to make it easy for the user.

Shield voltage can be driven on another Mux Bus to provide water tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input.

Each CAPSENSE™ block has two IDACs which can be used for general purposes if CAPSENSE™ is not being used. (both IDACs are available in that case) or if CAPSENSE™ is used without water tolerance (one IDAC is available). The two CAPSENSE™ blocks can be used independently.

5 Pinouts

The following is the pin list for the PSoC™ 4200L.

Table 1 Pinout

| 124-BGA | | 124-BGA | |
|---------|------|---------|-------|
| Pin | Name | Pin | Name |
| H13 | P0.0 | C3 | VSSA |
| H12 | P0.1 | C5 | P1.0 |
| G13 | P0.2 | B5 | P1.1 |
| G12 | P0.3 | A5 | P1.2 |
| K10 | VSSD | A4 | P1.3 |
| G11 | P0.4 | B4 | P1.4 |
| F13 | P0.5 | C4 | P1.5 |
| F12 | P0.6 | A3 | P1.6 |
| F11 | P0.7 | B3 | P1.7 |
| E13 | P8.0 | B1 | VREF |
| E12 | P8.1 | C3 | VSSA |
| E11 | P8.2 | D4 | VSSA |
| D13 | P8.3 | B2 | VDDA |
| D12 | P8.4 | C1 | P2.0 |
| C13 | P8.5 | C2 | P2.1 |
| C12 | P8.6 | D1 | P2.2 |
| B12 | P8.7 | D2 | P2.3 |
| C11 | XRES | D3 | P2.4 |
| A12 | VCCD | E1 | P2.5 |
| D10 | VSSD | E2 | P2.6 |
| B13 | VDDD | E3 | P2.7 |
| A13 | VDDD | K4 | VSSD |
| A11 | P9.0 | A1 | VDDA |
| B11 | P9.1 | F1 | P10.0 |
| A10 | P9.2 | F2 | P10.1 |
| B10 | P9.3 | F3 | P10.2 |
| C10 | P9.4 | G1 | P10.3 |
| A9 | P9.5 | G2 | P10.4 |
| B9 | P9.6 | G3 | P10.5 |
| C9 | P9.7 | H1 | P10.6 |
| | | H2 | P10.7 |
| C8 | P5.0 | K4 | VSSD |
| B8 | P5.1 | J1 | P6.0 |
| A8 | P5.2 | J2 | P6.1 |
| A7 | P5.3 | J3 | P6.2 |
| B7 | P5.4 | K1 | P6.3 |

Pinouts

Table 1 Pinout

| 124-BGA | | 124-BGA | |
|---------|-------|---------|------------|
| Pin | Name | Pin | Name |
| C7 | P5.5 | K2 | P6.4 |
| A6 | P5.6 | L1 | P12.0 |
| B6 | P5.7 | L2 | P12.1 |
| A2 | VDDA | K3 | P6.5 |
| B2 | VDDA | L3 | VSSD |
| N2 | P3.0 | L8 | P4.0 |
| M2 | P3.1 | N9 | P4.1 |
| N3 | P3.2 | M9 | P4.2 |
| M3 | P3.3 | N10 | P4.3 |
| N4 | P3.4 | M10 | P4.4 |
| M4 | P3.5 | N11 | P4.5 |
| N5 | P3.6 | M11 | P4.6 |
| M5 | P3.7 | M12 | P4.7 |
| M1 | VDDIO | L11 | VSSD |
| N1 | VDDIO | L12 | D+/P13.0 |
| N6 | P11.0 | L13 | D-/P13.1 |
| M6 | P11.1 | M13 | VBUS/P13.2 |
| L6 | P11.2 | L9 | P7.0 |
| N7 | P11.3 | L10 | P7.1 |
| M7 | P11.4 | K13 | P7.2 |
| L7 | P11.5 | K12 | P7.3 |
| N8 | P11.6 | K11 | P7.4 |
| M8 | P11.7 | J13 | P7.5 |
| N12 | VDDIO | J12 | P7.6 |
| N13 | VDDIO | J11 | P7.7 |

Port 12 (Port pins 12.0 and 12.1) are SIO pins.

Port 13 (Port pins 13.0 and 13.1) require VBUS (P13.2) to be powered.

Ports 6 (Port pins P6.0..6.5) and 9 (Port pins 9.0..9.7) are overvoltage tolerant (GPIO_OVT)

Balls C6, D11, H11, H3, L4, and L5 are No Connects (NC) on the 124-BGA package.

Pinouts

Each of the pins shown in the previous table can have multiple programmable functions as shown in the following table.

| Port/pin | Analog | USB | Alt. function 1 | Alt. function 2 | Alt. function 3 | Alt. function 4 | Alt. function 5 |
|----------|----------------------------------|-----|----------------------|-------------------|----------------------------|------------------|----------------------|
| P0.0 | lpcomp.in_p[0] | | | | can[1].can_rx:0 | usb.vbus_valid | scb[0].spi_select1:3 |
| P0.1 | lpcomp.in_n[0] | | | | can[1].can_tx:0 | | scb[0].spi_select2:3 |
| P0.2 | lpcomp.in_p[1] | | | | | | scb[0].spi_select3:3 |
| P0.3 | lpcomp.in_n[1] | | | | | | |
| P0.4 | wco_in | | | scb[1].uart_rx:0 | | scb[1].i2c_scl:0 | scb[1].spi_mosi:0 |
| P0.5 | wco_out | | | scb[1].uart_tx:0 | | scb[1].i2c_sda:0 | scb[1].spi_miso:0 |
| P0.6 | | | srss.ext_clk:0 | scb[1].uart_cts:0 | | | scb[1].spi_clk:0 |
| P0.7 | | | | scb[1].uart_rts:0 | can[1].can_tx- _enb_n:0 | srss.wakeup | scb[1].spi_select0:0 |
| P8.0 | | | | scb[3].uart_rx:0 | | scb[3].i2c_scl:0 | scb[3].spi_mosi:0 |
| P8.1 | | | | scb[3].uart_tx:0 | | scb[3].i2c_sda:0 | scb[3].spi_miso:0 |
| P8.2 | | | | scb[3].uart_cts:0 | | lpcomp.comp[0]:0 | scb[3].spi_clk:0 |
| P8.3 | | | | scb[3].uart_rts:0 | | lpcomp.comp[1]:0 | scb[3].spi_select0:0 |
| P8.4 | | | | | | | scb[3].spi_select1:0 |
| P8.5 | | | | | | | scb[3].spi_select2:0 |
| P8.6 | | | | | | | scb[3].spi_select3:0 |
| P8.7 | | | | | | | |
| P9.0 | | | tcpwm.line[0]:2 | scb[0].uart_rx:0 | | scb[0].i2c_scl:0 | scb[0].spi_mosi:0 |
| P9.1 | | | tcpwm.line_comp[0]:2 | scb[0].uart_tx:0 | | scb[0].i2c_sda:0 | scb[0].spi_miso:0 |
| P9.2 | | | tcpwm.line[1]:2 | scb[0].uart_cts:0 | | | scb[0].spi_clk:0 |
| P9.3 | | | tcpwm.line_comp[1]:2 | scb[0].uart_rts:0 | | | scb[0].spi_select0:0 |
| P9.4 | | | tcpwm.line[2]:2 | | | | scb[0].spi_select1:0 |
| P9.5 | | | tcpwm.line_comp[2]:2 | | | | scb[0].spi_select2:0 |
| P9.6 | | | tcpwm.line[3]:2 | | | scb[3].i2c_scl:3 | scb[0].spi_select3:0 |
| P9.7 | | | tcpwm.line_comp[3]:2 | | | scb[3].i2c_sda:3 | |
| P5.0 | ctb1_pads[0] csd[1].c_mod | | tcpwm.line[4]:2 | scb[2].uart_rx:0 | | scb[2].i2c_scl:0 | scb[2].spi_mosi:0 |
| P5.1 | ctb1_pads[1] csd[1].c_sh_tank | | tcpwm.line_comp[4]:2 | scb[2].uart_tx:0 | | scb[2].i2c_sda:0 | scb[2].spi_miso:0 |
| P5.2 | ctb1_pads[2] ctb1_oa0_out_10x | | tcpwm.line[5]:2 | scb[2].uart_cts:0 | | lpcomp.comp[0]:1 | scb[2].spi_clk:0 |
| P5.3 | ctb1_pads[3] ctb1_oa1_out_10x | | tcpwm.line_comp[5]:2 | scb[2].uart_rts:0 | | lpcomp.comp[1]:1 | scb[2].spi_select0:0 |
| P5.4 | ctb1_pads[4] | | tcpwm.line[6]:2 | | | | scb[2].spi_select1:0 |
| P5.5 | ctb1_pads[5] | | tcpwm.line_comp[6]:2 | | | | scb[2].spi_select2:0 |
| P5.6 | ctb1_pads[6] | | tcpwm.line[7]:2 | | | | scb[2].spi_select3:0 |
| P5.7 | ctb1_pads[7] | | tcpwm.line_comp[7]:2 | | | | |
| P1.0 | ctb0_pads[0] | | tcpwm.line[2]:1 | scb[0].uart_rx:1 | | scb[0].i2c_scl:1 | scb[0].spi_mosi:1 |
| P1.1 | ctb0_pads[1] | | tcpwm.line_comp[2]:1 | scb[0].uart_tx:1 | | scb[0].i2c_sda:1 | scb[0].spi_miso:1 |
| P1.2 | ctb0_pads[2] ctb0_oa0_out_10x | | tcpwm.line[3]:1 | scb[0].uart_cts:1 | | | scb[0].spi_clk:1 |
| P1.3 | ctb0_pads[3] ctb0_oa1_out_10x | | tcpwm.line_comp[3]:1 | scb[0].uart_rts:1 | | | scb[0].spi_select0:1 |
| P1.4 | ctb0_pads[4] | | tcpwm.line[6]:1 | | | | scb[0].spi_select1:1 |
| P1.5 | ctb0_pads[5] | | tcpwm.line_comp[6]:1 | | | | scb[0].spi_select2:1 |
| P1.6 | ctb0_pads[6] | | tcpwm.line[7]:1 | | | | scb[0].spi_select3:1 |
| P1.7 | ctb0_pads[7], sar_ext_vref | | tcpwm.line_comp[7]:1 | | | | |

Pinouts

| Port/pin | Analog | USB | Alt. function 1 | Alt. function 2 | Alt. function 3 | Alt. function 4 | Alt. function 5 |
|----------|------------------|--------|-----------------------|-------------------|-----------------------|------------------|----------------------|
| P2.0 | sarmux_pads[0] | | tcpwm.line[4]:1 | scb[1].uart_rx:1 | | scb[1].i2c_scl:1 | scb[1].spi_mosi:1 |
| P2.1 | sarmux_pads[1] | | tcpwm.line_compl[4]:1 | scb[1].uart_tx:1 | | scb[1].i2c_sda:1 | scb[1].spi_miso:1 |
| P2.2 | sarmux_pads[2] | | tcpwm.line[5]:1 | scb[1].uart_cts:1 | | | scb[1].spi_clk:1 |
| P2.3 | sarmux_pads[3] | | tcpwm.line_compl[5]:1 | scb[1].uart_rts:1 | | | scb[1].spi_select0:1 |
| P2.4 | sarmux_pads[4] | | tcpwm.line[0]:1 | | | | scb[1].spi_select1:0 |
| P2.5 | sarmux_pads[5] | | tcpwm.line_compl[0]:1 | | | | scb[1].spi_select2:0 |
| P2.6 | sarmux_pads[6] | | tcpwm.line[1]:1 | | | | scb[1].spi_select3:0 |
| P2.7 | sarmux_pads[7] | | tcpwm.line_compl[1]:1 | | | | |
| P10.0 | | | | scb[2].uart_rx:1 | | scb[2].i2c_scl:1 | scb[2].spi_mosi:1 |
| P10.1 | | | | scb[2].uart_tx:1 | | scb[2].i2c_sda:1 | scb[2].spi_miso:1 |
| P10.2 | | | | scb[2].uart_cts:1 | | | scb[2].spi_clk:1 |
| P10.3 | | | | scb[2].uart_rts:1 | | | scb[2].spi_select0:1 |
| P10.4 | | | | | | | scb[2].spi_select1:1 |
| P10.5 | | | | | | | scb[2].spi_select2:1 |
| P10.6 | | | | | | | scb[2].spi_select3:1 |
| P10.7 | | | | | | | |
| P6.0 | | | tcpwm.line[4]:0 | scb[3].uart_rx:1 | can[0].can_tx_enu_n:0 | scb[3].i2c_scl:1 | scb[3].spi_mosi:1 |
| P6.1 | | | tcpwm.line_compl[4]:0 | scb[3].uart_tx:1 | can[0].can_rx:0 | scb[3].i2c_sda:1 | scb[3].spi_miso:1 |
| P6.2 | | | tcpwm.line[5]:0 | scb[3].uart_cts:1 | can[0].can_tx:0 | scb[2].i2c_scl:3 | scb[3].spi_clk:1 |
| P6.3 | | | tcpwm.line_compl[5]:0 | scb[3].uart_rts:1 | | scb[2].i2c_sda:3 | scb[3].spi_select0:1 |
| P6.4 | | | tcpwm.line[6]:0 | | | scb[0].i2c_scl:3 | scb[3].spi_select1:1 |
| P12.0 | | | tcpwm.line[7]:0 | | | scb[1].i2c_scl:3 | scb[3].spi_select3:1 |
| P12.1 | | | tcpwm.line_compl[7]:0 | | | scb[1].i2c_sda:3 | |
| P6.5 | | | tcpwm.line_compl[6]:0 | | | scb[0].i2c_sda:3 | scb[3].spi_select2:1 |
| P3.0 | | | tcpwm.line[0]:0 | scb[1].uart_rx:2 | | scb[1].i2c_scl:2 | scb[1].spi_mosi:2 |
| P3.1 | | | tcpwm.line_compl[0]:0 | scb[1].uart_tx:2 | | scb[1].i2c_sda:2 | scb[1].spi_miso:2 |
| P3.2 | | | tcpwm.line[1]:0 | scb[1].uart_cts:2 | | cpuss.swd_data:0 | scb[1].spi_clk:2 |
| P3.3 | | | tcpwm.line_compl[1]:0 | scb[1].uart_rts:2 | | cpuss.swd_clk:0 | scb[1].spi_select0:2 |
| P3.4 | | | tcpwm.line[2]:0 | | | | scb[1].spi_select1:1 |
| P3.5 | | | tcpwm.line_compl[2]:0 | | | | scb[1].spi_select2:1 |
| P3.6 | | | tcpwm.line[3]:0 | | | | scb[1].spi_select3:1 |
| P3.7 | | | tcpwm.line_compl[3]:0 | | | | |
| P11.0 | | | tcpwm.line[4]:3 | scb[2].uart_rx:2 | | scb[2].i2c_scl:2 | scb[2].spi_mosi:2 |
| P11.1 | | | tcpwm.line_compl[4]:3 | scb[2].uart_tx:2 | | scb[2].i2c_sda:2 | scb[2].spi_miso:2 |
| P11.2 | | | tcpwm.line[5]:3 | scb[2].uart_cts:2 | | cpuss.swd_data:1 | scb[2].spi_clk:2 |
| P11.3 | | | tcpwm.line_compl[5]:3 | scb[2].uart_rts:2 | | cpuss.swd_clk:1 | scb[2].spi_select0:2 |
| P11.4 | | | tcpwm.line[6]:3 | | | | scb[2].spi_select1:2 |
| P11.5 | | | tcpwm.line_compl[6]:3 | | | | scb[2].spi_select2:2 |
| P11.6 | | | tcpwm.line[7]:3 | | | | scb[2].spi_select3:2 |
| P11.7 | | | tcpwm.line_compl[7]:3 | | | | |
| P4.0 | | | | scb[0].uart_rx:2 | can[0].can_rx:1 | scb[0].i2c_scl:2 | scb[0].spi_mosi:2 |
| P4.1 | | | | scb[0].uart_tx:2 | can[0].can_tx:1 | scb[0].i2c_sda:2 | scb[0].spi_miso:2 |
| P4.2 | csd[0].c_mod | | | scb[0].uart_cts:2 | can[0].can_tx_enu_n:1 | lpcomp.comp[0]:2 | scb[0].spi_clk:2 |
| P4.3 | csd[0].c_sh_tank | | | scb[0].uart_rts:2 | | lpcomp.comp[1]:2 | scb[0].spi_select0:2 |
| P4.4 | | | | | can[1].can_tx_enu_n:1 | | scb[0].spi_select1:2 |
| P4.5 | | | | | can[1].can_rx:1 | | scb[0].spi_select2:2 |
| P4.6 | | | | | can[1].can_tx:1 | | scb[0].spi_select3:2 |
| P4.7 | | | | | | | |
| P13.0 | | USB DP | | | | | |
| P13.1 | | USB DM | | | | | |

Pinouts

| Port/pin | Analog | USB | Alt. function 1 | Alt. function 2 | Alt. function 3 | Alt. function 4 | Alt. function 5 |
|----------|--------------|------|-----------------------|-------------------|-----------------|------------------|----------------------|
| P13.2 | | VBUS | | | | | |
| P7.0 | srss.eco_in | | tcpwm.line[0]:3 | scb[3].uart_rx:2 | | scb[3].i2c_scl:2 | scb[3].spi_mosi:2 |
| P7.1 | srss.eco_out | | tcpwm.line_compl[0]:3 | scb[3].uart_tx:2 | | scb[3].i2c_sda:2 | scb[3].spi_miso:2 |
| P7.2 | | | tcpwm.line[1]:3 | scb[3].uart_cts:2 | | | scb[3].spi_clk:2 |
| P7.3 | | | tcpwm.line_compl[1]:3 | scb[3].uart_rts:2 | | | scb[3].spi_select0:2 |
| P7.4 | | | tcpwm.line[2]:3 | | | | scb[3].spi_select1:2 |
| P7.5 | | | tcpwm.line_compl[2]:3 | | | | scb[3].spi_select2:2 |
| P7.6 | | | tcpwm.line[3]:3 | | | | scb[3].spi_select3:2 |
| P7.7 | | | tcpwm.line_compl[3]:3 | | | | |

Descriptions of the power pin functions are as follows:

VDDD: Power supply for both analog and digital sections (where there is no V_{DDA} pin)

VDDA: Analog V_{DD} pin where package pins allow; should be present before or concurrently with VDDD and the value of VDDA should be equal to or higher than VDDD and VDDIO

VDDIO: I/O pin power domain. It should not be present without VDDD.

VSSA: Analog ground pin where package pins allow; shorted to VSS otherwise

VSS: Ground pin

VCCD: Regulated digital supply (1.8 V \pm 5%)

VBUS: USB voltage. There is no constraint on VBUS with respect to VDDD. However, since it comes from USB, it is typically assumed to and ideally be 5 V (4.35 to 5.5 V is the range).

GPIO and GPIO_OVT pins can be used as CSD sense and shield pins (a total of 96). Up to 64 of the pins can be used for LCD drive.

The following package is supported: 124-ball BGA.

6 Power

The supply voltage range is 1.71 V to 5.5 V with all functions and circuits operating over that range.

The PSoC™ 4200L family allows two distinct modes of power supply operation: Unregulated external supply and regulated external supply modes.

6.1 Unregulated external supply

In this mode, the PSoC™ 4200L is powered by an external power supply that can be anywhere in the range of 1.8 V to 5.5 V. This range is also designed for battery-powered operation, for instance, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of the PSoC™ 4200L supplies the internal logic and the VCCD output of the PSoC™ 4200L must be bypassed to ground via an external Capacitor (in the range of 1 to 1.6 μ F; X5R ceramic or better).

VDDA and VDDD must be shorted together on the PC board; the grounds, VSSA and VSS must also be shorted together. Bypass capacitors must be used from VDDD and VDDA to ground, typical practice for systems in this frequency range is to use a capacitor in the 1 μ F range in parallel with a smaller capacitor (0.1 μ F, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

| Power supply | Bypass capacitors |
|-------------------------|---|
| VDDD–VSS and VDDIO–VSS | 0.1 μ F ceramic at each pin plus bulk capacitor 1 to 10 μ F. |
| VDDA–VSSA | 0.1 μ F ceramic at pin. Additional 1 μ F to 10 μ F bulk capacitor |
| VCCD–VSS | 1 μ F ceramic capacitor at the VCCD pin |
| VREF–VSSA (optional) | The internal bandgap may be bypassed with a 1 μ F to 10 μ F capacitor for better ADC performance. |

6.2 Regulated external supply

In this mode, the PSoC™ 4200L is powered by an external power supply that must be within the range of 1.71 V to 1.89 V ($1.8 \pm 5\%$); note that this range needs to include power supply ripple. In this mode, the VCCD and VDDD pins are shorted together and bypassed. The internal regulator is disabled in firmware.

7 Electrical specifications

7.1 Absolute maximum ratings

Table 2 Absolute maximum ratings^[1]

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/conditions |
|----------|------------------------------|---|------|-----|-----------------------|-------|--------------------|
| SID1 | V _{DD_ABS} | Analog or digital supply relative to V _{SS} (V _{SSD} = V _{SSA}) | -0.5 | - | 6 | V | Absolute maximum |
| SID2 | V _{CCD_ABS} | Direct digital core voltage input relative to V _{SSD} | -0.5 | - | 1.95 | V | Absolute maximum |
| SID3 | V _{GPIO_ABS} | GPIO voltage; V _{DDD} or V _{DDA} | -0.5 | - | V _{DD} + 0.5 | V | Absolute maximum |
| SID4 | I _{GPIO_ABS} | Current per GPIO | -25 | - | 25 | mA | Absolute maximum |
| SID5 | I _{G-PIO_injection} | GPIO injection current per pin | -0.5 | - | 0.5 | mA | Absolute maximum |
| BID44 | ESD_HBM | Electrostatic discharge human body model | 2200 | - | - | V | |
| BID45 | ESD_CDM | Electrostatic discharge charged device model | 500 | - | - | V | |
| BID46 | LU | Pin current for latch-up | -140 | - | 140 | mA | |

7.2 Device level specifications

All specifications are valid for $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ and $T_J \leq 125^{\circ}\text{C}$, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 3 DC specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/conditions |
|----------|------------------|---|------|-----|------|-------|-------------------------------|
| SID53 | V _{DDD} | Power supply input voltage (V _{DDA} = V _{DDD} = V _{DD}) | 1.8 | - | 5.5 | V | With regulator enabled |
| SID255 | V _{DDD} | Power supply input voltage unregulated | 1.71 | 1.8 | 1.89 | V | Internally unregulated supply |
| SID54 | V _{CCD} | Output voltage (for core logic) | - | 1.8 | - | V | |
| SID55 | C _{EFC} | External regulator voltage (V _{CCD}) bypass | 1 | 1.3 | 1.6 | μF | X5R ceramic or better |
| SID56 | C _{EXC} | Power supply decoupling capacitor | - | 1 | - | μF | X5R ceramic or better |

Active mode

| | | | | | | | |
|------|------------------|-----------------------------------|---|------|------|----|--|
| SID6 | I _{DD1} | Execute from flash; CPU at 6 MHz | - | 2.2 | 3.1 | mA | |
| SID7 | I _{DD2} | Execute from flash; CPU at 12 MHz | - | 3.7 | 4.8 | mA | |
| SID8 | I _{DD3} | Execute from flash; CPU at 24 MHz | - | 6.7 | 8.0 | mA | |
| SID9 | I _{DD4} | Execute from flash; CPU at 48 MHz | - | 12.8 | 14.5 | mA | |

Note

- Usage above the absolute maximum conditions listed in [Table 2](#) may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150°C in compliance with JEDEC Standard JESD22-A103, high temperature storage life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

Electrical specifications

Table 3 DC specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ conditions |
|--|--------------------|--|-----|-----|--------|-------|--|
| Sleep Mode | | | | | | | |
| SID21 | I _{DD16} | I ² C wakeup, WDT, and Comparators on. Regulator Off. | – | – | 2.9 | mA | V _{DD} = 1.71 to 1.89, 6 MHz |
| SID22 | I _{DD17} | I ² C wakeup, WDT, and Comparators on. | – | 1.7 | 2.1 | mA | V _{DD} = 1.8 to 5.5, 6 MHz |
| SID23 | I _{DD18} | I ² C wakeup, WDT, and Comparators on. Regulator Off. | – | 2.4 | 2.9 | mA | V _{DD} = 1.71 to 1.89, 12 MHz |
| SID24 | I _{DD19} | I ² C wakeup, WDT, and Comparators on. | – | 2.3 | 2.8 | mA | V _{DD} = 1.8 to 5.5, 12 MHz |
| Deep Sleep Mode, –40°C to +60°C | | | | | | | |
| SID30 | I _{DD25} | I ² C wakeup and WDT on. Regulator Off. | – | – | 13.5 | μA | V _{DD} = 1.71 to 1.89 |
| SID31 | I _{DD26} | I ² C wakeup and WDT on. | – | 1.3 | 20.0 | μA | V _{DD} = 1.8 to 3.6 |
| SID32 | I _{DD27} | I ² C wakeup and WDT on. | – | – | 20.0 | μA | V _{DD} = 3.6 to 5.5 |
| Deep Sleep Mode, +85°C | | | | | | | |
| SID33 | I _{DD28} | I ² C wakeup and WDT on. Regulator Off. | – | – | 45.0 | μA | V _{DD} = 1.71 to 1.89 |
| SID34 | I _{DD29} | I ² C wakeup and WDT on. | – | 15 | 60.0 | μA | V _{DD} = 1.8 to 3.6 |
| SID35 | I _{DD30} | I ² C wakeup and WDT on. | – | – | 45.0 | μA | V _{DD} = 3.6 to 5.5 |
| Hibernate Mode, –40°C to +60°C | | | | | | | |
| SID39 | I _{DD34} | Regulator Off. | – | – | 1123 | nA | V _{DD} = 1.71 to 1.89 |
| SID40 | I _{DD35} | | – | 150 | 1600 | nA | V _{DD} = 1.8 to 3.6 |
| SID41 | I _{DD36} | | – | – | 1600 | nA | V _{DD} = 3.6 to 5.5 |
| Hibernate Mode, +85°C | | | | | | | |
| SID42 | I _{DD37} | Regulator Off. | – | – | 4142 | nA | V _{DD} = 1.71 to 1.89 |
| SID43 | I _{DD38} | | – | – | 9700 | nA | V _{DD} = 1.8 to 3.6 |
| SID44 | I _{DD39} | | – | – | 10,400 | nA | V _{DD} = 3.6 to 5.5 |
| Stop Mode | | | | | | | |
| SID304 | I _{DD43A} | Stop Mode current; V _{DD} = 3.6 V | – | 20 | 659 | nA | T = –40°C to +60°C |
| SID304A | I _{DD43B} | Stop Mode current; V _{DD} = 3.6 V | – | – | 1810 | nA | T = +85°C |
| XRES current | | | | | | | |
| SID307 | I _{DD_XR} | Supply current while XRES (Active Low) asserted | – | 2 | 5 | mA | |

Table 4 AC specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ conditions |
|-----------------|-------------------------|-----------------------------|------------|------------|------------|--------------|--|
| SID48 | F _{CPU} | CPU frequency | DC | – | 48 | MHz | 1.71 ≤ V _{DD} ≤ 5.5 |
| SID49 | T _{SLEEP} | Wakeup from sleep mode | – | 0 | – | μs | Guaranteed by characterization |
| SID50 | T _{DEEPSLEEP} | Wakeup from Deep Sleep mode | – | – | 25 | μs | 24-MHz IMO. Guaranteed by characterization |
| SID51 | T _{HIBERNATE} | Wakeup from Hibernate mode | – | – | 0.7 | ms | Guaranteed by characterization |
| SID51A | T _{STOP} | Wakeup from Stop mode | – | – | 1.9 | ms | Guaranteed by characterization |
| SID52 | T _{RESETWIDTH} | External reset pulse width | 1 | – | – | μs | Guaranteed by characterization |

Electrical specifications

7.2.1 GPIO

Table 5 GPIO DC specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ conditions |
|----------|-----------------|--|--------------------------|-----|----------------------|------------|--|
| SID57 | $V_{IH}^{[2]}$ | Input voltage high threshold | $0.7 \times V_{DD}$ D | - | - | V | CMOS Input |
| SID57A | I_{IHS} | Input current when Pad > V_{DDIO} for OVT inputs | - | - | 10 | μ A | Per I ² C Spec |
| SID58 | V_{IL} | Input voltage low threshold | - | - | $0.3 \times V_{DDD}$ | V | CMOS Input |
| SID241 | $V_{IH}^{[2]}$ | LVTTL input, $V_{DDD} < 2.7$ V | $0.7 \times V_{DD}$ D | - | - | V | |
| SID242 | V_{IL} | LVTTL input, $V_{DDD} < 2.7$ V | - | - | $0.3 \times V_{DDD}$ | V | |
| SID243 | $V_{IH}^{[2]}$ | LVTTL input, $V_{DDD} \geq 2.7$ V | - | - | 2.0 | V | |
| SID244 | V_{IL} | LVTTL input, $V_{DDD} \geq 2.7$ V | 0.8 | - | - | V | |
| SID59 | V_{OH} | Output voltage high level | $V_{DDD} - 0.6$ | - | - | V | $I_{OH} = 4$ mA, $V_{DDD} \geq 3$ V |
| SID60 | V_{OH} | Output voltage high level | $V_{DDD} - 0.5$ | - | - | V | $I_{OH} = 1$ mA at 1.8 V V_{DDD} |
| SID61 | V_{OL} | Output voltage low level | - | - | 0.6 | V | $I_{OL} = 4$ mA at 1.8 V V_{DDD} |
| SID62 | V_{OL} | Output voltage low level | - | - | 0.6 | V | $I_{OL} = 8$ mA, $V_{DDD} \geq 3$ V |
| SID62A | V_{OL} | Output voltage low level | - | - | 0.4 | V | $I_{OL} = 3$ mA, $V_{DDD} \geq 3$ V |
| SID63 | R_{PULLUP} | Pull-up resistor | 3.5 | 5.6 | 8.5 | k Ω | |
| SID64 | $R_{PULLDOWN}$ | Pull-down resistor | 3.5 | 5.6 | 8.5 | k Ω | |
| SID65 | I_{IL} | Input leakage current (absolute value) | - | - | 2 | nA | 25°C, $V_{DDD} = 3.0$ V |
| SID65A | I_{IL_CTBM} | Input leakage current (absolute value) for CTBM pins | - | - | 4 | nA | |
| SID66 | C_{IN} | Input capacitance | - | - | 7 | pF | Not applicable for P6.4, P6.5, P12.0, P12.1, and for USB pins. |
| SID67 | V_{HYSTTL} | Input hysteresis LVTTL | 25 | 40 | - | mV | $V_{DDD} \geq 2.7$ V |
| SID68 | $V_{HYSCMOS}$ | Input hysteresis CMOS | $0.05 \times V_{DDD}$ | - | - | mV | |
| SID69 | I_{DIODE} | Current through protection diode to V_{DD}/V_{SS} | - | - | 100 | μ A | Guaranteed by characterization |
| SID69A | I_{TOT_GPIO} | Maximum Total Source or Sink Chip Current | - | - | 200 | mA | Guaranteed by characterization |

Note

2. V_{IH} must not exceed $V_{DDD} + 0.2$ V.

Table 6 GPIO AC specifications
 (Guaranteed by characterization)^[3]

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ conditions |
|----------|-----------------------|---|-----|-----|------|-------|--|
| SID70 | T _{RISEF} | Rise time in fast strong mode | 2 | – | 12 | ns | 3.3 V V _{DDD} , Load = 25 pF |
| SID71 | T _{FALLF} | Fall time in fast strong mode | 2 | – | 12 | ns | 3.3 V V _{DDD} , Load = 25 pF |
| SID72 | T _{RISES} | Rise time in slow strong mode | 10 | – | 60 | ns | 3.3 V V _{DDD} , Load = 25 pF |
| SID73 | T _{FALLS} | Fall time in slow strong mode | 10 | – | 60 | ns | 3.3 V V _{DDD} , Load = 25 pF |
| SID74 | F _{GPIOOUT1} | GPIO Fout; 3.3 V ≤ V _{DDD} ≤ 5.5 V. Fast strong mode. | – | – | 33 | MHz | 90/10%, 25 pF load, 60/40 duty cycle |
| SID75 | F _{GPIOOUT2} | GPIO Fout; 1.7 V ≤ V _{DDD} ≤ 3.3 V. Fast strong mode. | – | – | 16.7 | MHz | 90/10%, 25 pF load, 60/40 duty cycle |
| SID76 | F _{GPIOOUT3} | GPIO Fout; 3.3 V ≤ V _{DDD} ≤ 5.5 V. Slow strong mode. | – | – | 7 | MHz | 90/10%, 25 pF load, 60/40 duty cycle |
| SID245 | F _{GPIOOUT4} | GPIO Fout; 1.7 V ≤ V _{DDD} ≤ 3.3 V. Slow strong mode. | – | – | 3.5 | MHz | 90/10%, 25 pF load, 60/40 duty cycle |
| SID246 | F _{GPIOIN} | GPIO input operating frequency; 1.71 V ≤ V _{DDD} ≤ 5.5 V | – | – | 48 | MHz | 90/10% V _{IO} |

Note

3. Simultaneous switching transitions on many fully-loaded GPIO pins may cause ground perturbations depending on several factors including PCB and decoupling capacitor design. For applications that are very sensitive to ground perturbations, the slower GPIO slew rate setting may be used.

Electrical specifications

7.2.2 XRES

Table 7 XRES DC specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ conditions |
|----------|----------------------|--|-----------------------|-----|-----------------------|-------|--------------------------------|
| SID77 | V _{IH} | Input voltage high threshold | 0.7 × V _{DD} | – | – | V | CMOS Input |
| SID78 | V _{IL} | Input voltage low threshold | – | – | 0.3 × V _{DD} | V | CMOS Input |
| SID79 | R _{PULLUP} | Pull-up resistor | 3.5 | 5.6 | 8.5 | kΩ | |
| SID80 | C _{IN} | Input capacitance | – | 3 | – | pF | |
| SID81 | V _{HYSXRES} | Input voltage hysteresis | – | 100 | – | mV | Guaranteed by characterization |
| SID82 | I _{DIODE} | Current through protection diode to V _{DD} /V _{SS} | – | – | 100 | μA | Guaranteed by characterization |

Table 8 XRES AC specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ conditions |
|----------|-------------------------|-------------------|-----|-----|-----|-------|--------------------------------|
| SID83 | T _{RESETWIDTH} | Reset pulse width | 1 | – | – | μs | Guaranteed by characterization |

Electrical specifications

7.3 Analog peripherals

7.3.1 Opamp

Table 9 Opamp specifications

(Guaranteed by characterization)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/conditions |
|----------|---------------------|---|-------|------|-----------------|-------|--------------------------------------|
| | I_{DD} | Opamp block current. No load. | - | - | - | - | |
| SID269 | I_{DD_HI} | Power = high | - | 1100 | 1850 | μA | |
| SID270 | I_{DD_MED} | Power = medium | - | 550 | 950 | μA | |
| SID271 | I_{DD_LOW} | Power = low | - | 150 | 350 | μA | |
| | GBW | Load = 20 pF, 0.1 mA. $V_{DDA} = 2.7$ V | - | - | - | - | |
| SID272 | GBW_HI | Power = high | 6 | - | - | MHz | |
| SID273 | GBW_MED | Power = medium | 4 | - | - | MHz | |
| SID274 | GBW_LO | Power = low | - | 1 | - | MHz | |
| | I_{OUT_MAX} | $V_{DDA} \geq 2.7$ V, 500 mV from rail | - | - | - | - | |
| SID275 | $I_{OUT_MAX_HI}$ | Power = high | 10 | - | - | mA | |
| SID276 | $I_{OUT_MAX_MID}$ | Power = medium | 10 | - | - | mA | |
| SID277 | $I_{OUT_MAX_LO}$ | Power = low | - | 5 | - | mA | |
| | I_{OUT} | $V_{DDA} = 1.71$ V, 500 mV from rail | - | - | - | - | |
| SID278 | $I_{OUT_MAX_HI}$ | Power = high | 4 | - | - | mA | |
| SID279 | $I_{OUT_MAX_MID}$ | Power = medium | 4 | - | - | mA | |
| SID280 | $I_{OUT_MAX_LO}$ | Power = low | - | 2 | - | mA | |
| SID281 | V_{IN} | Input voltage range | -0.05 | - | $V_{DDA} - 0.2$ | V | Charge-pump on, $V_{DDA} \geq 2.7$ V |
| SID282 | V_{CM} | Input common mode voltage | -0.05 | - | $V_{DDA} - 0.2$ | V | Charge-pump on, $V_{DDA} \geq 2.7$ V |
| | V_{OUT} | $V_{DDA} \geq 2.7$ V | - | - | - | - | |
| SID283 | V_{OUT_1} | Power = high, $I_{load} = 10$ mA | 0.5 | - | $V_{DDA} - 0.5$ | V | |
| SID284 | V_{OUT_2} | Power = high, $I_{load} = 1$ mA | 0.2 | - | $V_{DDA} - 0.2$ | V | |
| SID285 | V_{OUT_3} | Power = medium, $I_{load} = 1$ mA | 0.2 | - | $V_{DDA} - 0.2$ | V | |
| SID286 | V_{OUT_4} | Power = low, $I_{load} = 0.1$ mA | 0.2 | - | $V_{DDA} - 0.2$ | V | |
| SID288 | V_{OS_TR} | Offset voltage, trimmed | 1 | ±0.5 | 1 | mV | High mode |
| SID288A | V_{OS_TR} | Offset voltage, trimmed | - | ±1 | - | mV | Medium mode |
| SID288B | V_{OS_TR} | Offset voltage, trimmed | - | ±2 | - | mV | Low mode |
| SID290 | $V_{OS_DR_TR}$ | Offset voltage drift, trimmed | -10 | ±3 | 10 | μV/°C | High mode |
| SID290A | $V_{OS_DR_TR}$ | Offset voltage drift, trimmed | - | ±10 | - | μV/°C | Medium mode |
| SID290B | $V_{OS_DR_TR}$ | Offset voltage drift, trimmed | - | ±10 | - | μV/°C | Low mode |
| SID291 | CMRR | DC | 60 | 70 | - | dB | $V_{DDD} = 3.6$ V |
| SID292 | PSRR | At 1 kHz, 100 mV ripple | 70 | 85 | - | dB | $V_{DDD} = 3.6$ V |

Electrical specifications

Table 9 Opamp specifications

(Guaranteed by characterization) (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/conditions |
|------------------------|----------------------|---|-----|------|-----|---------|---|
| | Noise | | - | - | - | - | |
| SID293 | V _{N1} | Input referred, 1 Hz - 1GHz, power = high | - | 94 | - | μVrms | |
| SID294 | V _{N2} | Input referred, 1 kHz, power = high | - | 72 | - | nV/rtHz | |
| SID295 | V _{N3} | Input referred, 10kHz, power = high | - | 28 | - | nV/rtHz | |
| SID296 | V _{N4} | Input referred, 100kHz, power = high | - | 15 | - | nV/rtHz | |
| SID297 | Cload | Stable up to maximum load. Performance specs at 50 pF. | - | - | 125 | pF | |
| SID298 | Slew_rate | Load = 50 pF, Power = High, V _{DDA} ≥ 2.7 V | 6 | - | - | V/μs | |
| SID299 | T _{op_wake} | From disable to enable, no external RC dominating | - | 25 | - | μs | |
| SID299A | OL_GAIN | Open Loop Gain | - | 90 | - | dB | |
| | Comp_mode | Comparator mode; 50 mV drive, T _{rise} = T _{fall} (approx.) | - | - | - | | |
| SID300 | T _{PD1} | Response time; power = high | - | 150 | - | ns | |
| SID301 | T _{PD2} | Response time; power = medium | - | 400 | - | ns | |
| SID302 | T _{PD3} | Response time; power = low | - | 2000 | - | ns | |
| SID303 | V _{hyst_op} | Hysteresis | - | 10 | - | mV | |
| Deep Sleep Mode | | Mode 2 is lowest current range. Mode 1 has higher GBW. | | | | | Deep Sleep mode V _{DDA} ≥ 2.7 V. |
| SID_DS_1 | IDD_HI_M1 | Mode 1, High current | - | 1400 | - | μA | 25°C |
| SID_DS_2 | IDD_MED_M1 | Mode 1, Medium current | - | 700 | - | μA | 25°C |
| SID_DS_3 | IDD_LOW_M1 | Mode 1, Low current | - | 200 | - | μA | 25°C |
| SID_DS_4 | IDD_HI_M2 | Mode 2, High current | - | 120 | - | μA | 25°C |
| SID_DS_5 | IDD_MED_M2 | Mode 2, Medium current | - | 60 | - | μA | 25°C |
| SID_DS_6 | IDD_LOW_M2 | Mode 2, Low current | - | 15 | - | μA | 25°C |
| SID_DS_7 | GBW_HI_M1 | Mode 1, High current | - | 4 | - | MHz | 20-pF load, no DC load 0.2 V to V _{DDA} - 1.5 V |
| SID_DS_8 | GBW_MED_M1 | Mode 1, Medium current | - | 2 | - | MHz | 20-pF load, no DC load 0.2 V to V _{DDA} - 1.5 V |
| SID_DS_9 | GBW_LOW_M1 | Mode 1, Low current | - | 0.5 | - | MHz | 20-pF load, no DC load 0.2 V to V _{DDA} - 1.5 V |
| SID_DS_10 | GBW_HI_M2 | Mode 2, High current | - | 0.5 | - | MHz | 20-pF load, no DC load 0.2 V to V _{DDA} - 1.5 V |

Electrical specifications

Table 9 Opamp specifications

(Guaranteed by characterization) (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/conditions |
|-----------|-------------|------------------------|-----|-----|-----|-------|---|
| SID_DS_11 | GBW_MED_M2 | Mode 2, Medium current | - | 0.2 | - | MHz | 20-pF load, no DC load 0.2 V to $V_{DDA} - 1.5$ V |
| SID_DS_12 | GBW_LOW_M2 | Mode 2, Low current | - | 0.1 | - | MHz | 20-pF load, no DC load 0.2 V to $V_{DDA} - 1.5$ V |
| SID_DS_13 | VOS_HI_M1 | Mode 1, High current | - | 5 | - | mV | With trim 25°C, 0.2 V to $V_{DDA} - 1.5$ V |
| SID_DS_14 | VOS_MED_M1 | Mode 1, Medium current | - | 5 | - | mV | With trim 25°C, 0.2 V to $V_{DDA} - 1.5$ V |
| SID_DS_15 | VOS_LOW_M1 | Mode 1, Low current | - | 5 | - | mV | With trim 25°C, 0.2 V to $V_{DDA} - 1.5$ V |
| SID_DS_16 | VOS_HI_M2 | Mode 2, High current | - | 5 | - | mV | With trim 25°C, 0.2 V to $V_{DDA} - 1.5$ V |
| SID_DS_17 | VOS_MED_M2 | Mode 2, Medium current | - | 5 | - | mV | With trim 25°C, 0.2 V to $V_{DDA} - 1.5$ V |
| SID_DS_18 | VOS_LOW_M2 | Mode 2, Low current | - | 5 | - | mV | With trim 25°C, 0.2 V to $V_{DDA} - 1.5$ V |
| SID_DS_19 | IOUT_HI_M1 | Mode 1, High current | - | 10 | - | mA | Output is 0.5 V to $V_{DDA} - 0.5$ V |
| SID_DS_20 | IOUT_MED_M1 | Mode 1, Medium current | - | 10 | - | mA | Output is 0.5 V to $V_{DDA} - 0.5$ V |
| SID_DS_21 | IOUT_LOW_M1 | Mode 1, Low current | - | 4 | - | mA | Output is 0.5 V to $V_{DDA} - 0.5$ V |
| SID_DS_22 | IOUT_HI_M2 | Mode 2, High current | - | 1 | - | mA | Output is 0.5 V to $V_{DDA} - 0.5$ V |
| SID_DS_23 | IOUT_MED_M2 | Mode 2, Medium current | - | 1 | - | mA | Output is 0.5 V to $V_{DDA} - 0.5$ V |
| SID_DS_24 | IOUT_LOW_M2 | Mode 2, Low current | - | 0.5 | - | mA | Output is 0.5 V to $V_{DDA} - 0.5$ V |

Electrical specifications

7.3.2 Comparator

Table 10 Comparator DC specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/conditions |
|----------|----------------------|--|-----|-----|-------------------------|-------|--|
| SID85 | V _{OFFSET2} | Input offset voltage. Custom trim. Common mode voltage range from 0 to V _{DD} -1. | - | - | ±4 | mV | |
| SID85A | V _{OFFSET3} | Input offset voltage. Ultra low-power mode. | - | ±12 | - | mV | V _{DDD} ≥ 2.2 V for Temp < 0°C, V _{DDD} ≥ 1.8 V for Temp > 0°C |
| SID86 | V _{HYST} | Hysteresis when enabled. Common mode voltage range from 0 to V _{DD} -1. | - | 10 | 35 | mV | Guaranteed by characterization |
| SID87 | V _{ICM1} | Input common mode voltage in normal mode | 0 | - | V _{DDD} - 0.2 | V | Modes 1 and 2. |
| SID247 | V _{ICM2} | Input common mode voltage in low power mode | 0 | - | V _{DDD} | V | |
| SID247A | V _{ICM2} | Input common mode voltage in ultra low power mode | 0 | - | V _{DDD} - 1.15 | V | V _{DDD} ≥ 2.2 V for Temp < 0°C, V _{DDD} ≥ 1.8 V for Temp > 0°C |
| SID88 | CMRR | Common mode rejection ratio | 50 | - | - | dB | V _{DDD} ≥ 2.7 V. Guaranteed by characterization |
| SID88A | CMRR | Common mode rejection ratio | 42 | - | - | dB | V _{DDD} < 2.7 V. Guaranteed by characterization |
| SID89 | I _{CMP1} | Block current, normal mode | - | 280 | 400 | µA | Guaranteed by characterization |
| SID248 | I _{CMP2} | Block current, low power mode | - | 50 | 100 | µA | Guaranteed by characterization |
| SID259 | I _{CMP3} | Block current, ultra low power mode | - | 6 | 28 | µA | Guaranteed by characterization, V _{DDD} ≥ 2.2 V for Temp < 0°C, V _{DDD} ≥ 1.8 V for Temp > 0°C |
| SID90 | Z _{CMP} | DC input impedance of comparator | 35 | - | - | MΩ | Guaranteed by characterization |

Table 11 Comparator AC specifications

(Guaranteed by characterization)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/conditions |
|----------|--------------------|-------------------------------------|-----|-----|-----|-------|--|
| SID91 | T _{RESP1} | Response time, normal mode | - | 38 | 110 | ns | 50-mV overdrive |
| SID258 | T _{RESP2} | Response time, low power mode | - | 70 | 200 | ns | 50-mV overdrive |
| SID92 | T _{RESP3} | Response time, ultra low power mode | - | 2.3 | 15 | µs | 200-mV overdrive. V _{DDD} ≥ 2.2 V for Temp < 0°C, V _{DDD} ≥ 1.8 V for Temp > 0°C |

Electrical specifications

7.3.3 Temperature sensor

Table 12 Temperature sensor specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ conditions |
|----------|----------------------|-----------------------------|-----|-----|-----|-------|------------------------|
| SID93 | T _{SENSACC} | Temperature sensor accuracy | -5 | ±1 | +5 | °C | -40 to +85°C |

7.3.4 SAR ADC

Table 13 SAR ADC DC specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ conditions |
|----------|-----------|------------------------------------|-----------------|-----|------------------|-------|--------------------------------------|
| SID94 | A_RES | Resolution | - | - | 12 | bits | |
| SID95 | A_CHNIS_S | Number of channels - single ended | - | - | 16 | | |
| SID96 | A-CHNKS_D | Number of channels - differential | - | - | 8 | | Diff inputs use neighboring I/O |
| SID97 | A-MONO | Monotonicity | - | - | - | | Yes. Based on characterization |
| SID98 | A_GAINERR | Gain error | - | - | ±0.1 | % | With external reference. |
| SID99 | A_OFFSET | Input offset voltage | - | - | 2 | mV | Measured with 1-V V _{REF} . |
| SID100 | A_ISAR | Current consumption | - | - | 1 | mA | |
| SID101 | A_VINS | Input voltage range - single ended | V _{SS} | - | V _{DDA} | V | Based on device characterization |
| SID102 | A_VIND | Input voltage range - differential | V _{SS} | - | V _{DDA} | V | Based on device characterization |
| SID103 | A_INRES | Input resistance | - | - | 2.2 | kΩ | Based on device characterization |
| SID104 | A_INCAP | Input capacitance | - | - | 10 | pF | Based on device characterization |

Table 14 SAR ADC AC specifications

(Guaranteed by characterization)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ conditions |
|----------|-----------|---|-----|-----|-----|-------|--------------------------|
| SID106 | A_PSRR | Power supply rejection ratio | 70 | - | - | dB | |
| SID107 | A_CMRR | Common mode rejection ratio | 66 | - | - | dB | Measured at 1 V |
| SID108 | A_SAMP_1 | Sample rate with external reference bypass cap | - | - | 1 | Msp/s | |
| SID108A | A_SAMP_2 | Sample rate with no bypass cap. Reference = V _{DD} | - | - | 500 | ksps | |
| SID108B | A_SAMP_3 | Sample rate with no bypass cap. Internal reference | - | - | 100 | ksps | |
| SID109 | A_SNDR | Signal-to-noise and distortion ratio (SINAD) | 65 | - | - | dB | F _{IN} = 10 kHz |

Electrical specifications

Table 14 SAR ADC AC specifications

(Guaranteed by characterization) (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ conditions |
|----------|-----------|----------------------------|------|-----|------|-------|--|
| SID111 | A_INL | Integral non linearity | -1.7 | - | +2 | LSB | $V_{DD} = 1.71$ to 5.5, 1 Msps, $V_{REF} = 1$ to 5.5. |
| SID111A | A_INL | Integral non linearity | -1.5 | - | +1.7 | LSB | $V_{DDD} = 1.71$ to 3.6, 1 Msps, $V_{REF} = 1.71$ to V_{DDD} . |
| SID111B | A_INL | Integral non linearity | -1.5 | - | +1.7 | LSB | $V_{DDD} = 1.71$ to 5.5, 500 ksps, $V_{REF} = 1$ to 5.5. |
| SID112 | A_DNL | Differential non linearity | -1 | - | +2.2 | LSB | $V_{DDD} = 1.71$ to 5.5, 1 Msps, $V_{REF} = 1$ to 5.5. |
| SID112A | A_DNL | Differential non linearity | -1 | - | +2 | LSB | $V_{DDD} = 1.71$ to 3.6, 1 Msps, $V_{REF} = 1.71$ to V_{DDD} . |
| SID112B | A_DNL | Differential non linearity | -1 | - | +2.2 | LSB | $V_{DDD} = 1.71$ to 5.5, 500 ksps, $V_{REF} = 1$ to 5.5. |
| SID113 | A_THD | Total harmonic distortion | - | - | -65 | dB | $F_{IN} = 10$ kHz. |

7.3.5 CSD

Table 15 CSD block specification

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ conditions |
|-------------------|------------|--|------|-------|-----|-------|---|
| CSD specification | | | | | | | |
| SID308 | VCSD | Voltage range of operation | 1.71 | - | 5.5 | V | |
| SID309 | IDAC1 | DNL for 8-bit resolution | -1 | - | 1 | LSB | |
| SID310 | IDAC1 | INL for 8-bit resolution | -3 | - | 3 | LSB | |
| SID311 | IDAC2 | DNL for 7-bit resolution | -1 | - | 1 | LSB | |
| SID312 | IDAC2 | INL for 7-bit resolution | -3 | - | 3 | LSB | |
| SID313 | SNR | Ratio of counts of finger to noise. Guaranteed by characterization | 5 | - | - | Ratio | Capacitance range of 9 to 35 pF, 0.1 pF sensitivity |
| SID314 | IDAC1_CRT1 | Output current of Idac1 (8-bits) in high range | - | 612 | - | μA | |
| SID314A | IDAC1_CRT2 | Output current of Idac1(8-bits) in low range | - | 306 | - | μA | |
| SID315 | IDAC2_CRT1 | Output current of Idac2 (7-bits) in high range | - | 304.8 | - | μA | |
| SID315A | IDAC2_CRT2 | Output current of Idac2 (7-bits) in low range | - | 152.4 | - | μA | |

7.4 Digital peripherals

The following specifications apply to the Timer/Counter/PWM peripheral in timer mode.

7.4.1 Timer/counter/PWM

Table 16 TCPWM specifications

(Guaranteed by characterization)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ conditions |
|--------------|-----------|--|------|-----|-----|-------|--|
| SID.TCPWM.1 | ITCPWM1 | Block current consumption at 3 MHz | - | - | 45 | μA | All modes (Timer/Counter/PWM) |
| SID.TCPWM.2 | ITCPWM2 | Block current consumption at 12 MHz | - | - | 155 | μA | All modes (Timer/Counter/PWM) |
| SID.TCPWM.2A | ITCPWM3 | Block current consumption at 48 MHz | - | - | 650 | μA | All modes (Timer/Counter/PWM) |
| SID.TCPWM.3 | TCPWMFREQ | Operating frequency | - | - | Fc | MHz | Fc max = Fcpu. Maximum = 48 MHz |
| SID.TCPWM.4 | TPWMENEXT | Input Trigger Pulse Width for all Trigger Events | 2/Fc | - | - | ns | Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected. |
| SID.TCPWM.5 | TPWMEXT | Output Trigger Pulse widths | 2/Fc | - | - | ns | Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs |
| SID.TCPWM.5A | TCRES | Resolution of Counter | 1/Fc | - | - | ns | Minimum time between successive counts |
| SID.TCPWM.5B | PWMRES | PWM Resolution | 1/Fc | - | - | ns | Minimum pulse width of PWM Output |
| SID.TCPWM.5C | QRES | Quadrature inputs resolution | 1/Fc | - | - | ns | Minimum pulse width between Quadrature phase inputs. |

Electrical specifications

7.4.2 I²C

Table 17 Fixed I²C DC specifications

(Guaranteed by characterization)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/conditions |
|----------|-------------------|---|-----|------|-----|-------|--------------------|
| SID149 | I _{I2C1} | Block current consumption at 100 kHz | – | 10.5 | 55 | μA | |
| SID150 | I _{I2C2} | Block current consumption at 400 kHz | – | – | 135 | μA | |
| SID151 | I _{I2C3} | Block current consumption at 1 Mbps | – | – | 310 | μA | |
| SID152 | I _{I2C4} | I ² C enabled in Deep Sleep mode | – | – | 1.4 | μA | |

Table 18 Fixed I²C AC specifications

(Guaranteed by characterization)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/conditions |
|----------|-------------------|-------------|-----|-----|-----|-------|--------------------|
| SID153 | F _{I2C1} | Bit rate | – | – | 1 | Mbps | |

Electrical specifications

7.4.3 LCD direct drive

Table 19 LCD direct drive DC specifications

(Guaranteed by characterization)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/conditions |
|----------|-----------------------|---|-----|-----|------|-------|-------------------------------------|
| SID154 | I _{LCDLOW} | Operating current in low power mode | – | 5 | – | μA | 16 × 4 small segment disp. at 50 Hz |
| SID155 | C _{LCDCAP} | LCD capacitance per segment/common driver | – | 500 | 5000 | pF | Guaranteed by Design |
| SID156 | LCD _{OFFSET} | Long-term segment offset | – | 20 | – | mV | |
| SID157 | I _{LCDOP1} | PWM Mode current. 5-V bias. 24-MHz IMO | – | 0.6 | – | mA | 32 × 4 segments. 50 Hz, 25°C |
| SID158 | I _{LCDOP2} | PWM Mode current. 3.3-V bias. 24-MHz IMO. | – | 0.5 | – | mA | 32 × 4 segments. 50 Hz, 25°C |

Table 20 LCD direct drive AC specifications

(Guaranteed by characterization)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/conditions |
|----------|------------------|----------------|-----|-----|-----|-------|--------------------|
| SID159 | F _{LCD} | LCD frame rate | 10 | 50 | 150 | Hz | |

Table 21 Fixed UART DC specifications

(Guaranteed by characterization)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/conditions |
|----------|--------------------|---|-----|-----|-----|-------|--------------------|
| SID160 | I _{UART1} | Block current consumption at 100 Kbits/sec | – | 9 | 55 | μA | |
| SID161 | I _{UART2} | Block current consumption at 1000 Kbits/sec | – | – | 312 | μA | |

Table 22 Fixed UART AC specifications

(Guaranteed by characterization)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/conditions |
|----------|-------------------|-------------|-----|-----|-----|-------|--------------------|
| SID162 | F _{UART} | Bit rate | – | – | 1 | Mbps | |

Electrical specifications

7.4.4 SPI specifications

Table 23 Fixed SPI DC specifications

(Guaranteed by characterization)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units |
|----------|-------------------|--|-----|-----|-----|-------|
| SID163 | I _{SPI1} | Block current consumption at 1 Mbits/sec | – | – | 360 | μA |
| SID164 | I _{SPI2} | Block current consumption at 4 Mbits/sec | – | – | 560 | μA |
| SID165 | I _{SPI3} | Block current consumption at 8 Mbits/sec | – | – | 600 | μA |

Table 24 Fixed SPI AC specifications

(Guaranteed by characterization)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units |
|----------|------------------|---|-----|-----|-----|-------|
| SID166 | F _{SPI} | SPI operating frequency (master; 6X oversampling) | – | – | 8 | MHz |

Table 25 Fixed SPI master mode AC specifications

(Guaranteed by characterization)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units |
|----------|------------------|--|-----|-----|-----|-------|
| SID167 | T _{DMO} | MOSI valid after Sclock driving edge | – | – | 15 | ns |
| SID168 | T _{DSI} | MISO valid before Sclock capturing edge. Full clock, late MISO Sampling used | 20 | – | – | ns |
| SID169 | T _{HMO} | Previous MOSI data hold time with respect to capturing edge at Slave | 0 | – | – | ns |

Table 26 Fixed SPI slave mode AC specifications

(Guaranteed by characterization)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units |
|----------|----------------------|---|-----|-----|---------------------------|-------|
| SID170 | T _{DMI} | MOSI valid before Sclock capturing edge | 40 | – | – | ns |
| SID171 | T _{DSO} | MISO valid after Sclock driving edge | – | – | 42 + 3 × T _{SCB} | ns |
| SID171A | T _{DSO_ext} | MISO valid after Sclock driving edge in Ext. Clock mode | – | – | 48 | ns |
| SID172 | T _{HSO} | Previous MISO data hold time | 0 | – | – | ns |
| SID172A | T _{SSELSCK} | SSEL Valid to first SCK Valid edge | 100 | – | – | ns |

Electrical specifications

7.5 Memory

Table 27 Flash DC specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/conditions |
|----------|-----------------|---------------------------|------|-----|-----|-------|--------------------|
| SID173 | V _{PE} | Erase and program voltage | 1.71 | – | 5.5 | V | |

Table 28 Flash AC specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/conditions |
|----------|-------------------------|--|-------|-----|-----|---------|---------------------------------|
| SID174 | T _{ROWWRITE} | Row (block) write time (erase and program) | – | – | 20 | ms | Row (block) = 256 bytes |
| SID175 | T _{ROWERASE} | Row erase time | – | – | 13 | ms | |
| SID176 | T _{ROWPROGRAM} | Row program time after erase | – | – | 7 | ms | |
| SID178 | T _{BULKERASE} | Bulk erase time (128 KB) | – | – | 35 | ms | |
| SID180 | T _{DEVPROG} | Total device program time | – | – | 15 | seconds | Guaranteed by characterization |
| SID181 | F _{END} | Flash endurance | 100 k | – | – | cycles | Guaranteed by characterization |
| SID182 | F _{RET} | Flash retention. T _A ≤ 55°C, 100 k P/E cycles | 20 | – | – | years | Guaranteed by characterization |
| SID182A | | Flash retention. T _A ≤ 85°C, 10 k P/E cycles | 10 | – | – | years | Guaranteed by characterization |
| SID182B | F _{RETQ} | Flash retention. T _A ≤ 105°C, 10 k P/E cycles, ≤ three years at T _A ≥ 85°C | 10 | 20 | – | years | Guaranteed by characterization. |

Electrical specifications

7.6 System resources

7.6.1 Power-on reset (POR) with brown out

Table 29 Imprecise power-on reset (PRES)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/conditions |
|----------|-----------------------|----------------------|------|-----|------|-------|--------------------------------|
| SID185 | V _{RISEIPOR} | Rising trip voltage | 0.80 | – | 1.45 | V | Guaranteed by characterization |
| SID186 | V _{FALLIPOR} | Falling trip voltage | 0.75 | – | 1.4 | V | Guaranteed by characterization |
| SID187 | V _{IPOHYST} | Hysteresis | 15 | – | 200 | mV | Guaranteed by characterization |

Table 30 Precise power-on reset (POR)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/conditions |
|----------|------------------------|--|------|-----|-----|-------|--------------------------------|
| SID190 | V _{FALLPPOR} | BOD trip voltage in active and sleep modes | 1.64 | – | – | V | Guaranteed by characterization |
| SID192 | V _{FALLDPSLP} | BOD trip voltage in Deep Sleep | 1.4 | – | – | V | Guaranteed by characterization |

7.6.2 Voltage monitors

Table 31 Voltage monitors DC specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/conditions |
|----------|--------------------|--------------------------|------|------|------|-------|--------------------------------|
| SID195 | V _{LVI1} | LVI_A/D_SEL[3:0] = 0000b | 1.71 | 1.75 | 1.79 | V | |
| SID196 | V _{LVI2} | LVI_A/D_SEL[3:0] = 0001b | 1.76 | 1.80 | 1.85 | V | |
| SID197 | V _{LVI3} | LVI_A/D_SEL[3:0] = 0010b | 1.85 | 1.90 | 1.95 | V | |
| SID198 | V _{LVI4} | LVI_A/D_SEL[3:0] = 0011b | 1.95 | 2.00 | 2.05 | V | |
| SID199 | V _{LVI5} | LVI_A/D_SEL[3:0] = 0100b | 2.05 | 2.10 | 2.15 | V | |
| SID200 | V _{LVI6} | LVI_A/D_SEL[3:0] = 0101b | 2.15 | 2.20 | 2.26 | V | |
| SID201 | V _{LVI7} | LVI_A/D_SEL[3:0] = 0110b | 2.24 | 2.30 | 2.36 | V | |
| SID202 | V _{LVI8} | LVI_A/D_SEL[3:0] = 0111b | 2.34 | 2.40 | 2.46 | V | |
| SID203 | V _{LVI9} | LVI_A/D_SEL[3:0] = 1000b | 2.44 | 2.50 | 2.56 | V | |
| SID204 | V _{LVI10} | LVI_A/D_SEL[3:0] = 1001b | 2.54 | 2.60 | 2.67 | V | |
| SID205 | V _{LVI11} | LVI_A/D_SEL[3:0] = 1010b | 2.63 | 2.70 | 2.77 | V | |
| SID206 | V _{LVI12} | LVI_A/D_SEL[3:0] = 1011b | 2.73 | 2.80 | 2.87 | V | |
| SID207 | V _{LVI13} | LVI_A/D_SEL[3:0] = 1100b | 2.83 | 2.90 | 2.97 | V | |
| SID208 | V _{LVI14} | LVI_A/D_SEL[3:0] = 1101b | 2.93 | 3.00 | 3.08 | V | |
| SID209 | V _{LVI15} | LVI_A/D_SEL[3:0] = 1110b | 3.12 | 3.20 | 3.28 | V | |
| SID210 | V _{LVI16} | LVI_A/D_SEL[3:0] = 1111b | 4.39 | 4.50 | 4.61 | V | |
| SID211 | LVI_IDD | Block current | – | – | 100 | µA | Guaranteed by characterization |

Table 32 Voltage monitors AC specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/conditions |
|----------|----------------------|---------------------------|-----|-----|-----|-------|--------------------------------|
| SID212 | T _{MONTRIP} | Voltage monitor trip time | – | – | 1 | µs | Guaranteed by characterization |

Electrical specifications

7.6.3 SWD interface

Table 33 SWD interface specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/conditions |
|----------|--------------|---|------------|-----|-----------|-------|---------------------------------------|
| SID213 | F_SWDCLK1 | $3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | - | - | 14 | MHz | SWDCLK \leq 1/3 CPU clock frequency |
| SID214 | F_SWDCLK2 | $1.71\text{ V} \leq V_{DD} \leq 3.3\text{ V}$ | - | - | 7 | MHz | SWDCLK \leq 1/3 CPU clock frequency |
| SID215 | T_SWDI_SETUP | $T = 1/f\text{ SWDCLK}$ | $0.25 * T$ | - | - | ns | Guaranteed by characterization |
| SID216 | T_SWDI_HOLD | $T = 1/f\text{ SWDCLK}$ | $0.25 * T$ | - | - | ns | Guaranteed by characterization |
| SID217 | T_SWDO_VALID | $T = 1/f\text{ SWDCLK}$ | - | - | $0.5 * T$ | ns | Guaranteed by characterization |
| SID217A | T_SWDO_HOLD | $T = 1/f\text{ SWDCLK}$ | 1 | - | - | ns | Guaranteed by characterization |

7.6.4 Internal main oscillator

Table 34 IMO DC specifications

(Guaranteed by design)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/conditions |
|----------|-------------------|---------------------------------|-----|-----|------|-------|--------------------|
| SID218 | I _{IMO1} | IMO operating current at 48 MHz | - | - | 1000 | μA | |
| SID219 | I _{IMO2} | IMO operating current at 24 MHz | - | - | 325 | μA | |
| SID220 | I _{IMO3} | IMO operating current at 12 MHz | - | - | 225 | μA | |
| SID221 | I _{IMO4} | IMO operating current at 6 MHz | - | - | 180 | μA | |
| SID222 | I _{IMO5} | IMO operating current at 3 MHz | - | - | 150 | μA | |

Table 35 IMO AC specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/conditions |
|----------|-------------------------|--------------------------------------|-----|-----|-----|-------|--------------------|
| SID223 | F _{IMOTOL1} | Frequency variation from 3 to 48 MHz | - | - | ±2 | % | |
| SID226 | T _{STARTIMO} | IMO startup time | - | - | 12 | μs | |
| SID227 | T _{JITRMSIMO1} | RMS Jitter at 3 MHz | - | 156 | - | ps | |
| SID228 | T _{JITRMSIMO2} | RMS Jitter at 24 MHz | - | 145 | - | ps | |
| SID229 | T _{JITRMSIMO3} | RMS Jitter at 48 MHz | - | 139 | - | ps | |

Electrical specifications

7.6.5 Internal low-speed oscillator

Table 36 ILO DC specifications

(Guaranteed by design)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/conditions |
|----------|----------------------|---------------------------------|-----|-----|------|-------|--------------------------------|
| SID231 | I _{ILO1} | ILO operating current at 32 kHz | – | 0.3 | 1.05 | μA | Guaranteed by characterization |
| SID233 | I _{ILOLEAK} | ILO leakage current | – | 2 | 15 | nA | Guaranteed by design |

Table 37 ILO AC specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/conditions |
|----------|------------------------|--------------------------|-----|-----|-----|-------|--------------------------------|
| SID234 | T _{STARTILO1} | ILO startup time | – | – | 2 | ms | Guaranteed by characterization |
| SID236 | T _{ILODUTY} | ILO duty cycle | 40 | 50 | 60 | % | Guaranteed by characterization |
| SID237 | F _{ILOTIM1} | 32 kHz trimmed frequency | 15 | 32 | 50 | kHz | ±60% with trim. |

Table 38 PLL DC specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/conditions |
|----------|------------|--------------------------|-----|-----|-----|-------|--------------------|
| SID410 | IDD_PLL_48 | In = 3 MHz, Out = 48 MHz | – | 530 | 610 | μA | |
| SID411 | IDD_PLL_24 | In = 3 MHz, Out = 24 MHz | – | 300 | 405 | μA | |

Table 39 PLL AC specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/conditions |
|----------|---------------------|--|------|-----|-----|-------|----------------------|
| SID412 | F _{PLLIN} | PLL input frequency | 1 | – | 48 | MHz | |
| SID413 | F _{PLLINT} | PLL intermediate frequency; prescaler out | 1 | – | 3 | MHz | |
| SID414 | F _{PLLVCO} | VCO output frequency before post-divide | 22.5 | – | 104 | MHz | |
| SID415 | D _{IVVCO} | VCO Output post-divider range; PLL output frequency is F _{PPLVCO} /D _{IVVCO} | 1 | – | 8 | – | |
| SID416 | PLLlocktime | Lock time at startup | – | – | 250 | us | |
| SID417 | Jperiod_1 | Period jitter for VCO ≥ 67 MHz | – | – | 150 | ps | Guaranteed By design |
| SID416A | Jperiod_2 | Period jitter for VCO ≤ 67 MHz | – | – | 200 | ps | Guaranteed By design |

Electrical specifications

Table 40 External clock specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/conditions |
|----------|------------|------------------------------------|-----|-----|-----|-------|--------------------------------|
| SID305 | ExtClkFreq | External clock input frequency | 0 | – | 48 | MHz | Guaranteed by characterization |
| SID306 | ExtClkDuty | Duty cycle; Measured at $V_{DD}/2$ | 45 | – | 55 | % | Guaranteed by characterization |

Table 41 Watch crystal oscillator (WCO) specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/conditions |
|----------|-----------|-------------|-----|-----|-----|-------|--------------------|
|----------|-----------|-------------|-----|-----|-----|-------|--------------------|

IMO WCO-PLL calibrated mode

| | | | | | | | |
|--------|---------|--|------|---|-----|---|--------------------------------|
| SID330 | IMOWCO1 | Frequency variation with IMO set to 3 MHz | –0.6 | – | 0.6 | % | Does not include WCO tolerance |
| SID331 | IMOWCO2 | Frequency variation with IMO set to 5 MHz | –0.4 | – | 0.4 | % | Does not include WCO tolerance |
| SID332 | IMOWCO3 | Frequency variation with IMO set to 7 or 9 MHz | –0.3 | – | 0.3 | % | Does not include WCO tolerance |
| SID333 | IMOWCO4 | All other IMO frequency settings | –0.2 | – | 0.2 | % | Does not include WCO tolerance |

WCO specifications

| | | | | | | | |
|--------|--------|-------------------------------------|---|--------|------|-----|----------------------|
| SID398 | FWCO | Crystal frequency | – | 32.768 | – | kHz | |
| SID399 | FTOL | Frequency tolerance | – | 50 | 250 | ppm | With 20-ppm crystal. |
| SID400 | ESR | Equivalent series resistance | – | 50 | – | kΩ | |
| SID401 | PD | Drive Level | – | – | 1 | μW | |
| SID402 | TSTART | Startup time | – | – | 500 | ms | |
| SID403 | CL | Crystal load capacitance | 6 | – | 12.5 | pF | |
| SID404 | C0 | Crystal shunt capacitance | – | 1.35 | – | pF | |
| SID405 | IWCO1 | Operating current (high power mode) | – | – | 8 | uA | |

Table 42 External crystal oscillator (ECO) specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/conditions |
|----------|-----------|-------------------------|-----|-----|-----|-------|--------------------|
| SID316 | IECO1 | Block operating current | – | – | 1.5 | mA | |
| SID317 | FECO | Crystal frequency range | 4 | – | 33 | MHz | |

Electrical specifications

Table 43 UDB AC specifications

(Guaranteed by characterization)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ conditions |
|------------------------------------|---------------------------|--|-----|-----|-----|-------|------------------------|
| Datapath performance | | | | | | | |
| SID249 | F _{MAX-TIMER} | Max frequency of 16-bit timer in a UDB pair | – | – | 48 | MHz | |
| SID250 | F _{MAX-ADDER} | Max frequency of 16-bit adder in a UDB pair | – | – | 48 | MHz | |
| SID251 | F _{MAX_CRC} | Max frequency of 16-bit CRC/PRS in a UDB pair | – | – | 48 | MHz | |
| PLD performance in UDB | | | | | | | |
| SID252 | F _{MAX_PLD} | Max frequency of 2-pass PLD function in a UDB pair | – | – | 48 | MHz | |
| Clock to output performance | | | | | | | |
| SID253 | T _{CLK_OUT_UBD1} | Prop. delay for clock in to data out at 25°C, Typ. | – | 15 | – | ns | |
| SID254 | T _{CLK_OUT_UBD2} | Prop. delay for clock in to data out, Worst case. | – | 25 | – | ns | |

Table 44 Block specs

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ conditions |
|----------|------------------------|---|-----|-----|-----|---------|---|
| SID256 | T _{WS48} | Number of wait states at 48 MHz | 2 | – | – | | CPU execution from Flash. Guaranteed by characterization |
| SID257 | T _{WS24} | Number of wait states at 24 MHz | 1 | – | – | | CPU execution from Flash. Guaranteed by characterization |
| SID260 | V _{REFSAR} | Trimmed internal reference to SAR | –1 | – | +1 | % | Percentage of V _{bg} (1.024 V). Guaranteed by characterization |
| SID261 | F _{SARINTREF} | SAR operating speed without external reference bypass | – | 500 | – | ksps | 12-bit resolution. Guaranteed by characterization |
| SID262 | T _{CLKSWITCH} | Clock switching from clk1 to clk2 in clk1 periods | 3 | – | 4 | Periods | Guaranteed by design |

* T_{ws48} and T_{ws24} are guaranteed by design

Electrical specifications

Table 45 UDB port adaptor specifications

(Based on LPC Component Specs; all specs except TLCLKDO are guaranteed by design -10-pF load, 3-V V_{DDIO} and V_{DDD})

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ conditions |
|----------|------------------|---------------------------------------|-----|-----|-----|-------|------------------------|
| SID263 | T_{LCLKDO} | LCLK to output delay | - | - | 18 | ns | |
| SID264 | $T_{DINLCLK}$ | Input setup time to LCLK rising edge | - | - | 7 | ns | |
| SID265 | $T_{DINLCLKHLD}$ | Input hold time from LCLK rising edge | 0 | - | - | ns | |
| SID266 | $T_{LCLKHIZ}$ | LCLK to output tristated | - | - | 28 | ns | |
| SID267 | T_{FLCLK} | LCLK frequency | - | - | 33 | MHz | |
| SID268 | $T_{LCLKDUTY}$ | LCLK duty cycle (percentage high) | 40 | - | 60 | % | |

Table 46 USB device block specifications (USB only)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / conditions |
|----------|--------------|---|------|-----|-----|-------|--|
| SID321 | Vusb_5 | Device supply for USB operation | 4.5 | - | 5.5 | V | USB Configured, USB Reg. enabled |
| SID322 | Vusb_3.3 | Device supply for USB operation | 3.15 | - | 3.6 | V | USB Configured, USB Reg. bypassed |
| SID323 | Vusb_3 | Device supply for USB operation (Functional operation only) | 2.85 | - | 3.6 | V | USB Configured, USB Reg. bypassed |
| SID324 | Iusb_config | Device supply current in Active mode, IMO = 24 MHz | - | 10 | - | mA | $V_{DDD} = 5\text{ V}$ |
| SID325 | Iusb_config | Device supply current in Active mode, IMO = 24 MHz | - | 8 | - | mA | $V_{DDD} = 3.3\text{ V}$ |
| SID326 | Isub_suspend | Device supply current in Sleep mode | - | 0.5 | - | mA | $V_{DDD} = 5\text{ V}$, PICU wakeup |
| SID327 | Isub_suspend | Device supply current in Sleep mode | - | 0.3 | - | mA | $V_{DDD} = 5\text{ V}$, Device disconnected |
| SID328 | Isub_suspend | Device supply current in Sleep mode | - | 0.5 | - | mA | $V_{DDD} = 3.3\text{ V}$, PICU wakeup |
| SID329 | Isub_suspend | Device supply current in Sleep mode | - | 0.3 | - | mA | $V_{DDD} = 3.3\text{ V}$, Device disconnected |

Electrical specifications

Table 47 SIO specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / conditions |
|---|--------------------------|--|-------------------------|-----|--------------------------|-------|--|
| SIO DC specifications | | | | | | | |
| SID330 | V _{IH} | Input voltage high threshold | 0.7 * V _{DD} | - | - | V | CMOS input; with respect to V _{DDIO} |
| SID331 | V _{IL} | Input voltage low threshold | - | - | 0.3*V _{DD} | V | CMOS input; with respect to V _{DDIO} |
| SID332 | V _{IH} | Differential input mode high voltage; hysteresis disabled | V _r + 0.2 | - | - | V | V _r is the SIO reference voltage |
| SID333 | V _{IL} | Differential input mode low voltage, hysteresis disabled | - | - | V _r -0.2 | V | V _r is the SIO reference voltage |
| SID334 | V _{OH} | Output high voltage in unregulated mode | V _{DDIO} - 0.4 | - | - | V | I _{OH} = 4 mA, V _{DD} = 3.3 V |
| SID335 | V _{OH} | Output high voltage in regulated mode | V _r - 0.65 | - | V _r + 0.2 | V | I _{OH} = 1 mA |
| SID336 | V _{OH} | Output high voltage in regulated mode | V _r - 0.3 | - | V _r + 0.2 | V | I _{OH} = 0.1 mA |
| SID337 | V _{OL} | Output low voltage | - | - | 0.8 | V | V _{DDIO} = 3.3 V, I _{OL} = 25 mA |
| SID338 | V _{OL} | Output low voltage | - | - | 0.4 | V | V _{DDIO} = 1.8 V, I _{OL} = 4 mA |
| SID339 | V _{inref} | Input voltage reference | 0.48 | - | 0.52 * V _{DDIO} | V | |
| SID340 | V _{outref} | Output voltage reference (regulated mode) | 1 | - | V _{DDIO} - 1 | V | V _{DDIO} > 3.3 |
| SID341 | V _{outref} | Output voltage reference (regulated mode) | 1 | - | V _{DDIO} - 0.5 | V | V _{DDIO} < 3.3 |
| SID342 | R _{PULLUP} | Pull-up resistor | 3.5 | 5.6 | 8.5 | kΩ | |
| SID343 | R _{PULLDOWN} | Pull-down resistor | 3.5 | 5.6 | 8.5 | kΩ | |
| SID344 | I _{IL} | Input leakage current (absolute value) | - | - | 14 | nA | V _{IH} ≤ V _{DDIO} ; 25°C |
| SID345 | I _{IL} | Input leakage current (absolute value) | - | - | 10 | nA | V _{IH} > V _{DDIO} ; 25°C |
| SID346 | C _{IN} | Input capacitance | - | - | 7 | pF | |
| SID347 | V _{HYST-Single} | Hysteresis in single-ended mode | - | 40 | - | mV | |
| SID348 | V _{HYST-Diff} | Hysteresis in differential mode | - | 35 | - | mV | |
| SID349 | I _{DIODE} | Current through protection diode to V _{DD} /V _{SS} | - | - | 100 | μA | |
| SIO AC specifications (Guaranteed by design) | | | | | | | |
| SID350 | T _{RISEF} | Rise time in Fast Strong mode | - | - | 12 | ns | 3.3-V V _{DD} , Load = 25 pF |
| SID351 | T _{FALLF} | Fall time in Fast Strong mode | - | - | 12 | ns | 3.3-V V _{DD} , Load = 25 pF |

Electrical specifications

Table 47 SIO specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / conditions |
|----------|---------------------|--|-----|-----|-----|-------|---|
| SID352 | T _{RISES} | Rise time in Slow Strong mode | - | - | 75 | ns | 3.3-V V _{DD} , Cload = 25 pF |
| SID353 | T _{FALLS} | Fall time in Slow Strong mode | - | - | 70 | ns | 3.3-V V _{DD} , Cload = 25 pF |
| SID354 | F _{SIOUT1} | SIO Fout; Unregulated, Fast Strong mode | - | - | 33 | MHz | 3.3-V ≤ V _{DD} ≤ 5.5 V, 25 pF. Guaranteed by design. |
| SID355 | F _{SIOUT2} | SIO Fout; Unregulated, Fast Strong mode | - | - | 16 | MHz | 1.71-V ≤ V _{DD} ≤ 3.3 V, 25 pF |
| SID356 | F _{SIOUT3} | SIO Fout; Regulated, Fast Strong mode | - | - | 20 | MHz | 3.3-V ≤ V _{DD} ≤ 5.5 V, 25 pF |
| SID357 | F _{SIOUT4} | SIO Fout; Regulated, Fast Strong mode | - | - | 10 | MHz | 1.71 V ≤ V _{DD} ≤ 3.3 V, 25 pF |
| SID358 | F _{SIOUT3} | SIO Fout; Unregulated, Slow Strong mode. | - | - | 5 | MHz | 3.3 V ≤ V _{DD} ≤ 5.5 V, 25 pF |
| SID359 | F _{SIOUT4} | SIO Fout, Unregulated, Slow Strong mode. | - | - | 3.5 | MHz | 1.71 V ≤ V _{DD} ≤ 3.3 V, 25 pF |
| SID360 | F _{SIOUT5} | SIO Fout, Regulated, Slow Strong mode. | - | - | 2.5 | MHz | 1.7 V ≤ V _{DD} ≤ 5.5 V, 25 pF |
| SID361 | F _{GPIOIN} | GPIO input operating frequency; 1.71 V ≤ V _{DD} ≤ 5.5 V | - | - | 48 | MHz | 1.71 V ≤ V _{DD} ≤ 5.5 V |

Table 48 CAN specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / conditions |
|----------|-----------|--------------------------------|-----|-----|-----|-------|----------------------|
| SID420 | IDD_CAN | Block current consumption | - | - | 200 | uA | |
| SID421 | CAN_bits | CAN Bit rate (Min 8-MHz clock) | - | - | 1 | Mbps | |

8 Ordering information

The PSoC™ 4200L family part numbers and features are listed in the following table.

Table 49 PSoC™ 4200L ordering information

| Category | MPN | Features | | | | | | | | | | | | | | Package |
|----------|------------------|---------------------|------------|-----------|-----|---------------|-----|------------------|----------------|----------------|--------------|------------|----------------|-----|------|-----------|
| | | Max CPU Speed (MHz) | Flash (KB) | SRAM (KB) | UDB | Op-amp (CTBm) | CSD | Direct LCD Drive | 12-bit SAR ADC | LP Comparators | TCPWM Blocks | SCB Blocks | USB Full Speed | CAN | GPIO | 124-VFBGA |
| 4248 | CY8C4248BZA-L489 | 48 | 256 | 32 | 8 | 4 | 1 | Yes | 1000 ksps | 2 | 8 | 4 | Yes | Yes | 98 | Yes |
| | CY8C4248BZS-L489 | 48 | 256 | 32 | 8 | 4 | 1 | Yes | 1000 ksps | 2 | 8 | 4 | Yes | Yes | 98 | Yes |

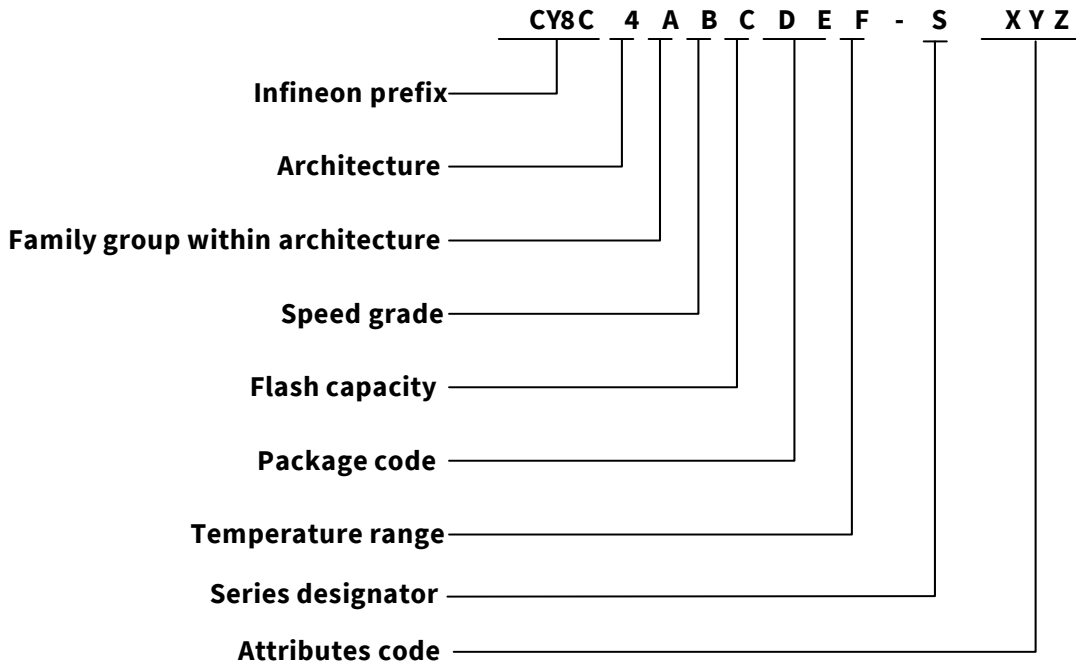
The nomenclature used in [Table 49](#) is based on the following part numbering convention:

Table 50 MPN nomenclature

| Field | Description | Values | Meaning |
|-------|-------------------|---------|--|
| CY8C | Infineon prefix | | |
| 4 | Architecture | 4 | PSoC™ 4 |
| A | Family | 2 | 4200 family |
| B | CPU speed | 4 | 48 MHz |
| C | Flash capacity | 6 | 64 KB |
| | | 7 | 128 KB |
| | | 8 | 256 KB |
| DE | Package code | AX, AZ | TQFP |
| | | LT | QFN |
| | | BZ | BGA |
| | | FD | CSP |
| F | Temperature range | A | Auto A (-40 to +85°C) |
| | | S | AUTO S (-40 to +105°C) |
| S | Series designator | S | PSoC™ 4 S-Series |
| | | L | PSoC™ 4 L-Series |
| | | M | PSoC™ 4 M-Series |
| XYZ | Attributes code | 000-999 | Code of feature set in the specific family |

8.1 Part numbering conventions

The part number fields are defined as follows.



Packaging

9 Packaging

Table 51 Package dimensions

| SPEC ID# | Package | Description | Package DWG # |
|----------|----------------|---|---------------|
| PKG_1 | 124-ball VFBGA | 124-ball, 9 mm x 9 mm x 1.0 mm height with 0.65 mm ball pitch | 001-97718 |

Table 52 Package characteristics

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|-----------------|---|------------|-----|-----|-----|---------|
| T _A | Operating ambient temperature (CY8C4248BZS - L489) | | -40 | 25 | 105 | °C |
| | Operating ambient temperature (CY8C4248BZA-L489) | | -40 | 25 | 85 | °C |
| T _J | Operating junction temperature | | -40 | - | 125 | °C |
| T _{JA} | Package θ _{JA} (124-ball VFBGA) | | - | 85 | - | °C/Watt |
| T _{JC} | Package θ _{JC} (124-ball VFBGA) | | - | 6 | - | °C/Watt |

Table 53 Solder reflow peak temperature

| Package | Maximum peak temperature | Maximum time at peak temperature |
|----------------|--------------------------|----------------------------------|
| 124-ball VFBGA | 260°C | 30 seconds |

Table 54 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2

| Package | MSL |
|----------------|-------|
| 124-ball VFBGA | MSL 3 |

Packaging

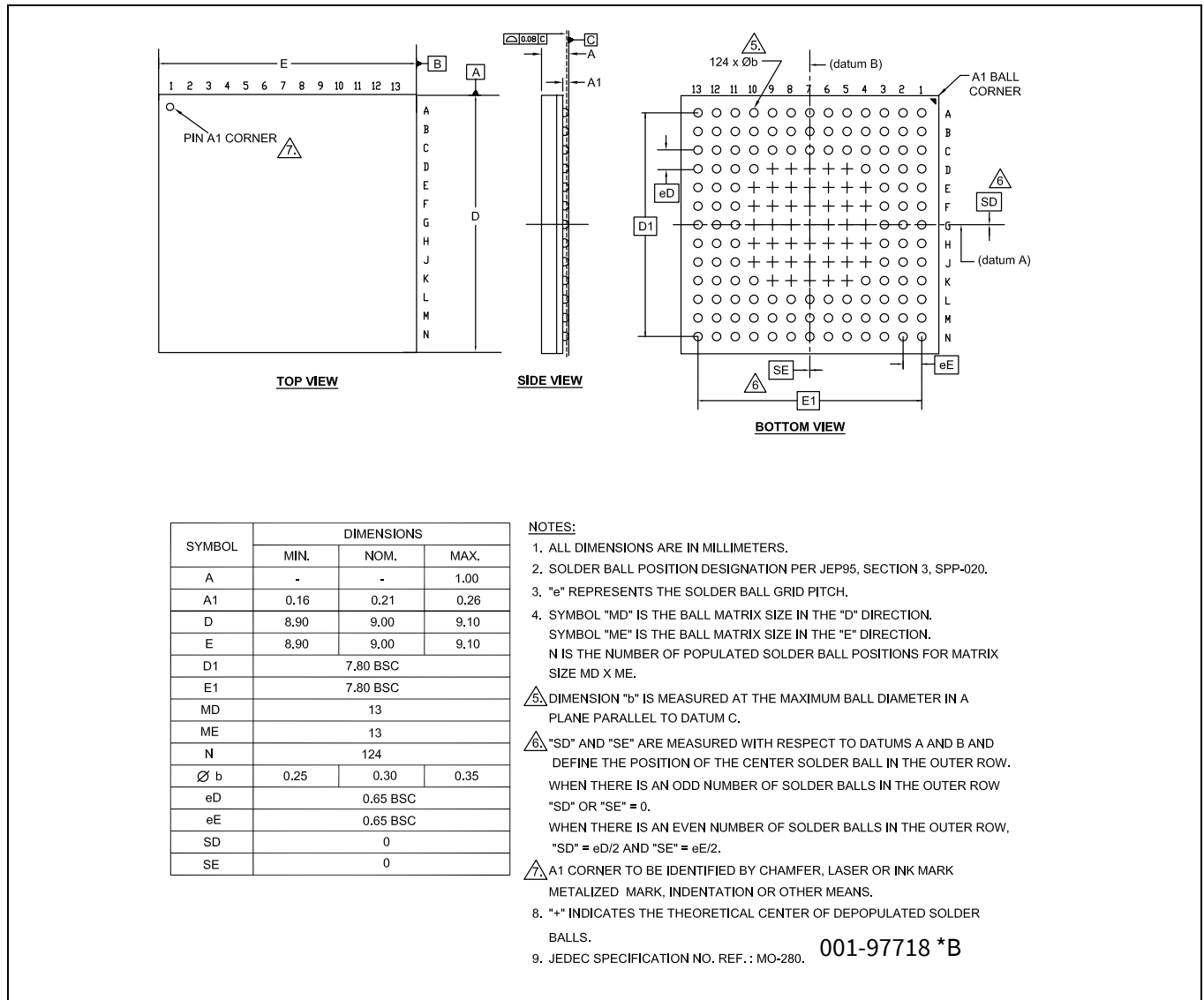


Figure 8 124-ball VFBGA package outline

10 Acronyms

Table 55 Acronyms used in this document

| Acronym | Description |
|---------|--|
| abus | analog local bus |
| ADC | analog-to-digital converter |
| AG | analog global |
| AHB | AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm® data transfer bus |
| ALU | arithmetic logic unit |
| AMUXBUS | analog multiplexer bus |
| API | application programming interface |
| APSR | application program status register |
| Arm® | advanced RISC machine, a CPU architecture |
| ATM | automatic thump mode |
| BW | bandwidth |
| CAN | Controller Area Network, a communications protocol |
| CMRR | common-mode rejection ratio |
| CPU | central processing unit |
| CRC | cyclic redundancy check, an error-checking protocol |
| DAC | digital-to-analog converter, see also IDAC, VDAC |
| DFB | digital filter block |
| DIO | digital input/output, GPIO with only digital capabilities, no analog. See GPIO. |
| DMIPS | Dhrystone million instructions per second |
| DMA | direct memory access, see also TD |
| DNL | differential nonlinearity, see also INL |
| DNU | do not use |
| DR | port write data registers |
| DSI | digital system interconnect |
| DWT | data watchpoint and trace |
| ECC | error correcting code |
| ECO | external crystal oscillator |
| EEPROM | electrically erasable programmable read-only memory |
| EMI | electromagnetic interference |
| EMIF | external memory interface |
| EOC | end of conversion |
| EOF | end of frame |
| EPSR | execution program status register |
| ESD | electrostatic discharge |
| ETM | embedded trace macrocell |

Acronyms

Table 55 Acronyms used in this document *(continued)*

| Acronym | Description |
|--------------------------|--|
| FIR | finite impulse response, see also IIR |
| FPB | flash patch and breakpoint |
| FS | full-speed |
| GPIO | general-purpose input/output, applies to a PSoC™ pin |
| HVI | high-voltage interrupt, see also LVI, LVD |
| IC | integrated circuit |
| IDAC | current DAC, see also DAC, VDAC |
| IDE | integrated development environment |
| I ² C, or IIC | Inter-Integrated Circuit, a communications protocol |
| IIR | infinite impulse response, see also FIR |
| ILO | internal low-speed oscillator, see also IMO |
| IMO | internal main oscillator, see also ILO |
| INL | integral nonlinearity, see also DNL |
| I/O | input/output, see also GPIO, DIO, SIO, USBIO |
| IPOR | initial power-on reset |
| IPSR | interrupt program status register |
| IRQ | interrupt request |
| ITM | instrumentation trace macrocell |
| LCD | liquid crystal display |
| LIN | Local Interconnect Network, a communications protocol. |
| LR | link register |
| LUT | lookup table |
| LVD | low-voltage detect, see also LVI |
| LVI | low-voltage interrupt, see also HVI |
| LVTTL | low-voltage transistor-transistor logic |
| MAC | multiply-accumulate |
| MCU | microcontroller unit |
| MISO | master-in slave-out |
| NC | no connect |
| NMI | nonmaskable interrupt |
| NRZ | non-return-to-zero |
| NVIC | nested vectored interrupt controller |
| NVL | nonvolatile latch, see also WOL |
| opamp | operational amplifier |
| PAL | programmable array logic, see also PLD |
| PC | program counter |
| PCB | printed circuit board |
| PGA | programmable gain amplifier |

Table 55 Acronyms used in this document *(continued)*

| Acronym | Description |
|---------|--|
| PHUB | peripheral hub |
| PHY | physical layer |
| PICU | port interrupt control unit |
| PLA | programmable logic array |
| PLD | programmable logic device, see also PAL |
| PLL | phase-locked loop |
| PMDD | package material declaration data sheet |
| POR | power-on reset |
| PRES | precise power-on reset |
| PRS | pseudo random sequence |
| PS | port read data register |
| PSoC™ | Programmable System-on-Chip™ |
| PSRR | power supply rejection ratio |
| PWM | pulse-width modulator |
| RAM | random-access memory |
| RISC | reduced-instruction-set computing |
| RMS | root-mean-square |
| RTC | real-time clock |
| RTL | register transfer language |
| RTR | remote transmission request |
| RX | receive |
| SAR | successive approximation register |
| SC/CT | switched capacitor/continuous time |
| SCL | I ² C serial clock |
| SDA | I ² C serial data |
| S/H | sample and hold |
| SINAD | signal to noise and distortion ratio |
| SIO | special input/output, GPIO with advanced features. See GPIO. |
| SOC | start of conversion |
| SOF | start of frame |
| SPI | Serial Peripheral Interface, a communications protocol |
| SR | slew rate |
| SRAM | static random access memory |
| SRES | software reset |
| SWD | serial wire debug, a test protocol |
| SWV | single-wire viewer |
| TD | transaction descriptor, see also DMA |
| THD | total harmonic distortion |

Acronyms

Table 55 Acronyms used in this document *(continued)*

| Acronym | Description |
|----------------|--|
| TIA | transimpedance amplifier |
| TRM | technical reference manual |
| TTL | transistor-transistor logic |
| TX | transmit |
| UART | Universal Asynchronous Transmitter Receiver, a communications protocol |
| UDB | universal digital block |
| USB | Universal Serial Bus |
| USBIO | USB input/output, PSoC™ pins used to connect to a USB port |
| VDAC | voltage DAC, see also DAC, IDAC |
| WDT | watchdog timer |
| WOL | write once latch, see also NVL |
| WRES | watchdog timer reset |
| XRES | external reset I/O pin |
| XTAL | crystal |

11 Document conventions

11.1 Units of measure

Table 56 Units of measure

| Symbol | Unit of measure |
|--------|------------------------|
| °C | degrees Celsius |
| dB | decibel |
| fF | femto farad |
| Hz | hertz |
| KB | 1024 bytes |
| kbps | kilobits per second |
| Khr | kilohour |
| kHz | kilohertz |
| kΩ | kilo ohm |
| ksps | kilosamples per second |
| LSB | least significant bit |
| Mbps | megabits per second |
| MHz | megahertz |
| MΩ | mega-ohm |
| Msps | megasamples per second |
| μA | microampere |
| μF | microfarad |
| μH | microhenry |
| μs | microsecond |
| μV | microvolt |
| μW | microwatt |
| mA | milliampere |
| ms | millisecond |
| mV | millivolt |
| nA | nanoampere |
| ns | nanosecond |
| nV | nanovolt |
| Ω | ohm |
| pF | picofarad |
| ppm | parts per million |
| ps | picosecond |
| s | second |
| sps | samples per second |
| sqrtHz | square root of hertz |
| V | volt |

Revision history

Revision history

| Document version | Date of release | Description of changes |
|------------------|-----------------|------------------------|
| ** | 2022-06-16 | New datasheet. |

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