
**8-bit Microcontroller for Touch Sensing and
Smart Proximity Sensing**

DS Rev. 1.06

Features**CPU**

- 8-bit M8051 core
- 8051-compatible, 2-clock per cycle

On-Chip Flash

- 64 KB code Flash memory
- Endurance: 10,000 times

SRAM

- 4 KB SRAM

GPIO

- Normal I/O: Max. 46 ports
- High sink current port: 8 ports

Timers

- Basic Interval Timer (BIT)
- Watchdog Timer (WDT)
- 8-bit Timer × 1-ch (T0)
- 16-bit Timer × 5-ch (T1/T2/T3/T4/T5)

Interfaces

- USI (USART/SPI/I2C) × 1
- USART (USART/SPI) × 2

12-bit ADC

- 16 external input channels
- Internal Reference Voltage

Self-Capacitive Touch Sensor

- 32 channels
- 10 V Conducted Susceptibility (CS) Immunity

Water Shield

- 4-channel – mesh

Power-On Reset, Low-Voltage Reset

- Reset release level (1.48 V)
- 4 levels (1.6 V/2.7 V/3.7 V/4.2 V)

Low-Voltage Indicator

- 4 levels (2.2 V/3 V/4 V/4.5 V)

On-Chip RC Oscillator

- HSIRC 16 MHz
 - ±1.5% (TA= 0°C to +60°C)
 - ±2.5% (TA= -40°C to +85°C)
 - ±3.5% (TA= -40°C to +105°C)
- LSIRC 32 kHz ±50% (TA= -40°C to +85°C)

On-Chip WDT Oscillator

- 32 kHz (±50% @ -40°C to 85°C)

Power-Down Mode

- STOP/IDLE mode

Operating Voltages

- 2.0 V to 5.5 V @ 16 MHz
- 2.7 V to 5.5 V (1.5% IRC, CS 10 V touch)

Operating Frequency

- 2,4,8,16 MHz (Fsys)

Operating Temperature

- -40°C to +85°C
- -40°C to +105°C

Packages

- 24-QFN (4 x 4 mm)
- 28-SOP (300 mil, 2.05 mm, 1.27 mm)
- 28-TSSOP (170 mil, 1 mm, 0.65 mm)
- 28-TSSOP-105 (170 mil, 1 mm, 0.65 mm)
- 32-LQFP (7 x 7 mm)
- 44-LQFP (10 x 10 mm)
- 48-LQFP (7 x 7 mm)
- 48-LQFP-105 (7 x 7 mm)

Product Selection Table

Table 1. Device Summary

Part Number	Flash [KB]	XRAM [KB]	SPI [ch]	USART [ch]	I2C [ch]	Timer	Touch [ch]	PWM [ch]	ADC [ch]	IO [pin]	Temp. [°C]	Package
A96T430LUN	64	4	2	2	1	6	19	6	8	24	-40 to 85	24-QFN
A96T430GDN	64	4	2	2	1	6	23	6	8	26	-40 to 85	28-SOP
A96T430GRN	64	4	2	2	1	6	23	6	8	26	-40 to 85	28-TSSOP
A96T430GR2N	64	4	2	2	1	6	23	6	8	26	-40 to 105	28-TSSOP
A96T430KNN	64	4	2	2	1	6	27	6	8	30	-40 to 85	32-LQFP
A96T430SNN	64	4	3	3	1	6	32	6	16	42	-40 to 85	44-LQFP
A96T430CLN	64	4	3	3	1	6	32	6	16	46	-40 to 85	48-LQFP
A96T430CL2N	64	4	3	3	1	6	32	6	16	46	-40 to 105	48-LQFP

* For available options or further information on the devices with “**” marks, please contact [ABOV sales offices](#).

Contents

Features	1
Product Selection Table	2
1. Introduction	10
2. Description	11
2.1 Product Category Definition	11
2.2 Device Overview	12
2.3 Block Diagram	15
2.4 Functional Overview	16
2.4.1 Port Structure	16
2.4.2 Memory Organization	17
2.4.2.1 Program Memory	18
2.4.2.2 Data Memory	19
2.4.2.3 External Data Memory	21
2.4.2.4 SFR Map	22
2.4.3 I/O Ports	33
2.4.3.1 P0 Port	33
2.4.3.2 P1 Port	33
2.4.3.3 P2 Port	33
2.4.3.4 P3 Port	33
2.4.3.5 P4 Port	33
2.4.3.6 P5 Port	33
2.4.4 Interrupt Controller	34
2.4.4.1 External Interrupt	36
2.4.4.2 Block Diagram	37
2.4.4.3 Interrupt Vector Table	38
2.4.5 Clock Generator	39
2.4.5.1 Block Diagram	39
2.4.6 BIT	40
2.4.6.1 Block Diagram	40
2.4.7 WDT	41
2.4.7.1 WDT Interrupt Timing Waveform	41
2.4.7.2 Block Diagram	42
2.4.8 WT	43
2.4.8.1 Block Diagram	43
2.4.9 Timer 0/1/2/3/4/5	44
2.4.9.1 Timer 0	44
2.4.9.2 Timer 1	52
2.4.9.3 Timer 2	59
2.4.9.4 Timer 3	67
2.4.9.5 Timer 4	75
2.4.9.6 Timer 5	83
2.4.10 Buzzer Driver	91
2.4.10.1 Block Diagram	91
2.4.11 USI	92
2.4.11.1 USI UART Mode	93
2.4.11.2 USI SPI Mode	94
2.4.11.3 USI I2C Mode	94

2.4.12	USART	95
2.4.12.1	Block Diagram	96
2.4.13	Self-Capacitive Touch Sensor	97
2.4.13.1	Features	97
2.4.13.2	Block Diagram	98
2.4.13.3	CAPN Port	99
2.4.14	12-bit ADC	100
2.4.14.1	Conversion Timing	100
2.4.14.2	Block Diagram	101
2.4.15	Power-Down Operation	102
2.4.15.1	Peripheral Operation in IDLE/STOP Mode	102
2.4.16	RESET	103
2.4.16.1	Reset Source	103
2.4.16.2	Reset Block Diagram	103
2.4.17	Memory Programming	104
2.4.17.1	Flash Control and Status Register	104
2.4.17.2	Memory Map	105
2.5	Debug Interface	106
2.5.1	Core	107
2.5.1.1	Debug Interface	109
2.5.1.2	Interrupt Priority	110
2.5.1.3	Extended Stack Pointer	111
2.5.2	OCD (On-Chip Debugger) Emulator and Debugger	112
2.5.2.1	On-Chip Debug System	114
2.5.2.2	Entering Debug Mode	115
2.5.2.3	Two-Wire Communication Protocol	116
2.5.3	Circuit Design Guide	121
2.5.3.1	Connection of Transmission	122
3.	Pinouts and Pin Description	123
3.1	Pinouts	123
3.1.1	A96T430LUN (24-QFN)	123
3.1.2	A96T430GDN (28-SOP)	124
3.1.3	A96T430GRN/A96T420GR2N (28-TSSOP)	125
3.1.4	A96T430KNN (32-LQFP)	126
3.1.5	A96T430SNN (44-LQFP)	127
3.1.6	A96T430CLN/A96T430CL2N (48-LQFP)	128
3.2	Pin Description	129
4.	Electrical Characteristics	136
4.1	Absolute Maximum Ratings	136
4.2	Recommended Operating Conditions	136
4.3	Touch Sensing Characteristics	137
4.4	ADC Characteristics	138
4.5	Power-On Reset Characteristics	138
4.6	Low-Voltage Reset and Low-Voltage Indicator Characteristics	139
4.7	High-Speed Internal RC Oscillator Characteristics	140
4.8	Low-Speed Internal RC Oscillator Characteristics	140
4.9	DC Characteristics	141
4.10	AC Characteristics	142
4.11	USART Characteristics	143
4.12	SPI Characteristics	148

4.13	UART Characteristics	149
4.14	I2C Characteristics	150
4.15	Data Retention Voltage in STOP Mode.....	151
4.16	Internal Flash ROM Characteristics	152
4.17	Input/Output Capacitance	152
4.18	Recommended Circuit and Layout.....	153
4.19	Typical Characteristics	154
5.	Package Information	156
5.1	24-QFN Package Information	156
5.2	28-SOP Package Information	157
5.3	28-TSSOP Package Information.....	158
5.4	32-LQFP Package Information.....	159
5.5	44-LQFP Package Information.....	160
5.6	48-LQFP Package Information.....	161
6.	Ordering Information	162
	Revision History	163

List of Tables

Table 1. Device Summary	2
Table 2. A96T430 Series Memory Density	11
Table 3. A96T430 Device Features and Peripherals	12
Table 4. Summary of A96T430 Peripherals	14
Table 5. SFR Map Summary	22
Table 6. XSFR Map Summary	23
Table 7. SFR Map	26
Table 8. XSFR Map	30
Table 9. Interrupt Vector Address Table	38
Table 10. Timer 0 Operating Modes	44
Table 11. Timer 1 Operating Modes	52
Table 12. Timer 2 Operating Modes	59
Table 13. Timer 3 Operating Modes	67
Table 14. TIMER 4 Operating Modes	75
Table 15. TIMER 5 Operating Modes	83
Table 16. Buzzer Frequency at 8 MHz	91
Table 17. Peripheral Operation During Power-Down Mode	102
Table 18. Reset State	103
Table 19. Core and Debug Information	106
Table 20. Core and Debug Interface by Series	107
Table 21. Feature Comparison Chart by Series and Cores	108
Table 22. OCD Type of Each Series	109
Table 23. Comparison of OCD 1 and OCD 2	109
Table 24. Interrupt Priorities in Groups and Levels	110
Table 25. Debug Feature by Series	112
Table 26. OCD 1 and OCD 2 Pin Description	113
Table 27. Features of OCD	114
Table 28. Pin Description	129
Table 29. Absolute Maximum Ratings	136
Table 30. Recommended Operating Conditions	136
Table 31. Touch Switch Characteristics	137
Table 32. ADC Characteristics	138
Table 33. Power-On Reset Characteristics	138
Table 34. LVR and LVI Characteristics	139
Table 35. High-Speed Internal RC Oscillator Characteristics	140
Table 36. Internal WDTRC Oscillator Characteristics	140
Table 37. DC Characteristics	141
Table 38. AC Characteristics	142
Table 39. USART Timing Characteristics in SPI or Synchronous Mode Operations	143
Table 40. SPI Characteristics	148
Table 41. UART Characteristics	149
Table 42. I2C Characteristics	150
Table 43. Data Retention Voltage in STOP Mode	151
Table 44. Internal Flash ROM Characteristics	152
Table 45. Input/Output Capacitance	152

List of Figures

Figure 1. Block Diagram of A96T430	15
Figure 2. General-Purpose I/O Port Structure	16
Figure 3. Program Memory	18
Figure 4. Data Memory Map	19
Figure 5. Lower 128-byte RAM	20
Figure 6. XDATA Memory Area	21
Figure 7. Interrupt Group Priority Level	35
Figure 8. External Interrupt Description	36
Figure 9. Block Diagram of Interrupt	37
Figure 10. Clock Generator Block Diagram	39
Figure 11. Basic Interval Timer Block Diagram	40
Figure 12. Watchdog Timer Interrupt Timing Waveform	41
Figure 13. Watchdog Timer Block Diagram	42
Figure 14. Watch Timer Block Diagram	43
Figure 15. 8-bit Timer/Counter Mode for Timer 0	45
Figure 16. 8-bit Timer/Counter 0 Example	46
Figure 17. 8-bit-PWM Mode for Timer 0	47
Figure 18. PWM Output Waveforms in PWM Mode for Timer 0	48
Figure 19. 8-bit Capture Mode for Timer 0	49
Figure 20. Input Capture Mode Operation for Timer 0	50
Figure 21. Express Timer Overflow in Capture Mode	50
Figure 22. 8-bit Timer 0 Block Diagram	51
Figure 23. 16-bit Timer/Counter Mode for Timer 1	53
Figure 24. 16-bit Timer/Counter 1 Example	54
Figure 25. 16-bit Capture Mode for Timer 1	55
Figure 26. Input Capture Mode Operation for Timer 1	56
Figure 27. Express Timer Overflow in Capture Mode	56
Figure 28. 16-bit PPG Mode for Timer 1	57
Figure 29. 16-bit Timer 1 Block Diagram	58
Figure 30. 16-bit Timer/Counter Mode for Timer 2	60
Figure 31. 16-bit Timer/Counter 2 Example	61
Figure 32. 16-bit Capture Mode for Timer 2	62
Figure 33. Input Capture Mode Operation for Timer 2	63
Figure 34. Express Timer Overflow in Capture Mode	63
Figure 35. 16-bit PPG Mode for Timer 2	64
Figure 36. 16-bit PPG Mode Timming Chart for Timer 2	65
Figure 37. 16-bit Timer 2 Block Diagram	66
Figure 38. 16-bit Timer/Counter Mode for Timer 3	68
Figure 39. 16-bit Timer/Counter 3 Example	69
Figure 40. 16-bit Capture Mode for Timer 3	70
Figure 41. Input Capture Mode Operation for Timer 3	71
Figure 42. Express Timer Overflow in Capture Mode	71
Figure 43. 16-bit PPG Mode for Timer 3	72
Figure 44. 16-bit PPG Mode Timming Chart for Timer 3	73
Figure 45. 16-bit Timer 3 Block Diagram	74
Figure 46. 16-bit Timer/Counter Mode for Timer 4	76
Figure 47. 16-bit Timer/Counter 4 Example	77

Figure 48. 16-bit Capture Mode for Timer 4	78
Figure 49. Input Capture Mode Operation for Timer 4	79
Figure 50. Express Timer Overflow in Capture Mode	79
Figure 51. 16-bit PPG Mode for Timer 4	80
Figure 52. 16-bit PPG Mode Timming Chart for Timer 4	81
Figure 53. 16-bit Timer 4 Block Diagram	82
Figure 54. 16-bit Timer/Counter Mode for Timer 5	84
Figure 55. 16-bit Timer/Counter 5 Example	85
Figure 56. 16-bit Capture Mode for Timer 5	86
Figure 57. Input Capture Mode Operation for Timer 5	87
Figure 58. Express Timer Overflow in Capture Mode	87
Figure 59. 16-bit PPG Mode for Timer 5	88
Figure 60. 16-bit PPG Mode Timming Chart for Timer 5	89
Figure 61. 16-bit Timer 5 Block Diagram	90
Figure 62. Buzzer Driver Block Diagram	91
Figure 63. USART1 Block Diagram	96
Figure 64. 16-bit Touch Block Diagram	98
Figure 65. CAPN Pin with Cs Capacitor (VDD)	99
Figure 66. CAPN Pin with Cs Capacitor (GND)	99
Figure 67. 12-bit ADC Block Diagram	101
Figure 68. ADC Input Pin with Capacitor	101
Figure 69. Reset Block Diagram	103
Figure 70. Flash Memory Map	105
Figure 71. Address Configuration of Flash Memory	105
Figure 72. Configuration of Extended Stack Pointer	111
Figure 73. OCD 1 and OCD 2 Connector Pin Diagram	113
Figure 74. Block Diagram of OCD Interface and System	114
Figure 75. Timing Diagram of Debug Mode Entry	115
Figure 76. 10-bit Transmission Packet	116
Figure 77. General Data Transfer Timing in OCD	117
Figure 78. Bit Transfer on OCD Bus	118
Figure 79. Start and Stop Condition	118
Figure 80. Acknowledge on Serial Bus	119
Figure 81. Clock Synchronization During Wait Procedure	120
Figure 82. PCB Design Guide for OCD Interface	121
Figure 83. Connection of Transmission	122
Figure 84. A96T430 24-QFN Pin Assignment	123
Figure 85. A96T430 28-SOP Pin Assignment	124
Figure 86. A96T430 28-TSSOP Pin Assignment	125
Figure 88. A96T430 32-LQFP Pin Assignment	126
Figure 89. A96T430 44-LQFP Pin Assignment	127
Figure 90. A96T430 48-LQFP Pin Assignment	128
Figure 92. AC Timing	142
Figure 93. SPI Master Mode Timing (UCPHA = 0, MSB First)	144
Figure 94. SPI/Synchronous Master Mode Timing (UCPHA = 1, MSB First)	145
Figure 95. SPI Slave Mode Timing (UCPHA = 0, MSB First)	146
Figure 96. SPI/Synchronous Slave Mode Timing (UCPHA = 1, MSB First)	147
Figure 97. SPI Timing	148
Figure 98. Waveform for UART Timing Characteristics	149
Figure 99. Timing Waveform for UART Module	149

Figure 100. I2C Timing	150
Figure 101. STOP Mode Release Timing when Initiated by Interrupts	151
Figure 102. STOP Mode Release Timing when Initiated by RESETB	151
Figure 103. Recommended Voltage Range	153
Figure 104. IDD1 (RUN) Current	154
Figure 105. IDD2 (IDLE) Current	154
Figure 106. IDD3 (STOP1) Current	155
Figure 107. IDD4 (STOP2) Current	155
Figure 108. Package Dimension (24-QFN)	156
Figure 109. Package Dimension (28-SOP)	157
Figure 110. Package Dimension (28-TSSOP)	158
Figure 111. Package Dimension (32-LQFP)	159
Figure 112. Package Dimension (44-LQFP)	160
Figure 113. Package Dimension (48-LQFP)	161
Figure 114. A96T430 Device Numbering Nomenclature	162

1. Introduction

This document provides an overview of the features supported by each device, including high-level information and brief explanations for each feature.

2. Description

The A96T430 is an advanced CMOS 8-bit microcontroller with 64 Kbytes of flash memory. This is a powerful microcontroller which provides a highly flexible and cost-effective solution to many embedded control applications. Refer to Table 2 for the list of features supported by the device.

2.1 Product Category Definition

Table 2 provides an overview of the memory capacity for available devices in the A96T430 series.

Refer to Table 3 for the list of features supported by each product category.

Table 2. A96T430 Series Memory Density

Memory Density		Category
Flash	RAM	
64 KB	4 KB	A96T430

2.2 Device Overview

Table 3 summarizes and lists product-specific features available in the A96T430 series, considering the largest package.

Table 3. A96T430 Device Features and Peripherals

Peripherals		Description
Core	CPU	8-bit M8051 core (2-clock per cycle)
	Interrupt	Up to 24 peripheral interrupts are supported. • EINT0 to 5, EINT8, EINT10, EINT11, EINT12 (5) • Timer 0/1/2/3/4/5 (6) • WDT (1) • BIT (1) • WT (1) • USART Rx/Tx (4) • USI 1-ch. *Rx/Tx/I2C (3) • Touch (1) • ADC (1) • LVI (1)
Memory	ROM (Flash) capacity	• 64 Kbytes Flash with self-read and write capability • In-system programming (ISP) • Endurance: 10,000 times
	IRAM	256 bytes
	XRAM	3,840 bytes
Programmable pulse generation		• Pulse generation (by T1/T2/T3/T4/T5) • 8-bit PWM (by T0) • 16-bit PPG (by T1/T2/T3/T4/T5)
Buzzer		8-bit × 1-ch
Minimum instruction execution time		125 ns (@ 16 MHz, NOP Instruction)
Power down mode		• STOP1 mode • STOP2 mode • IDLE mode
General Purpose I/O (GPIO)		• Normal I/O: 46 ports • High sink current port: 8 ports

Table 3. A96T430 Device Features and Peripherals (continued)

Peripherals		Description
Reset	Power-on reset	Power-on reset: 1.28 V
	Low-voltage reset	4-level (1.6 V/2.7 V/3.7 V/4.2 V)
Low-voltage indicator		4-level (2.2 V/3 V/4 V/4.5 V)
WT (Watch Timer)		14-bit x 1-ch
Timer		• BIT (Basic Interval Timer) 8-bit x 1-ch. • WDT (Watchdog Timer) 8-bit x 1-ch. • 8-bit x 1-ch (Timer 0) • 16-bit x 5-ch (Timer 1/2/3/4/5)
Communication function	USI	• One USI (USART + SPI + I2C) • 8-bit USART or 8-bit SPI or I2C × 1-ch
	USART	• Two USART (USART + SPI) • 8-bit USART or 8-bit SPI × 2-ch • Receiver timer out (RTO) • 0% error baud rate
12-bit ADC		16 Input channels
Self-Capacitive Touch Switch		• 32 channels • Fast Initial Self-Calibration • Key detection mode: Single/Multi-mode • CS Immunity: 10 V • 16-bit Sensing Resolutions • Support Touch Key Int. Wakeup at Power down
Internal RC oscillator		• HSIRC 16 MHz ±1.5% (TA=0°C to +60°C) • HSIRC 16 MHz ±2.5% (TA=-40°C to +85°C) • HSIRC 16 MHz ±3.5% (TA=-40°C to +105°C) • Selectable from 2, 4, 8, and 16 MHz
Operating voltage and frequency		• 2.0 V to 5.5 V @ 16 MHz • 2.7 V to 5.5 V (Touch, ADC)
Operating temperature		• -40°C to +85°C • -40°C to +105°C
Package		• 24-QFN • 28-SOP • 28-TSSOP • 32-LQFP • 44-LQFP • 48-LQFP • Pb-free packages

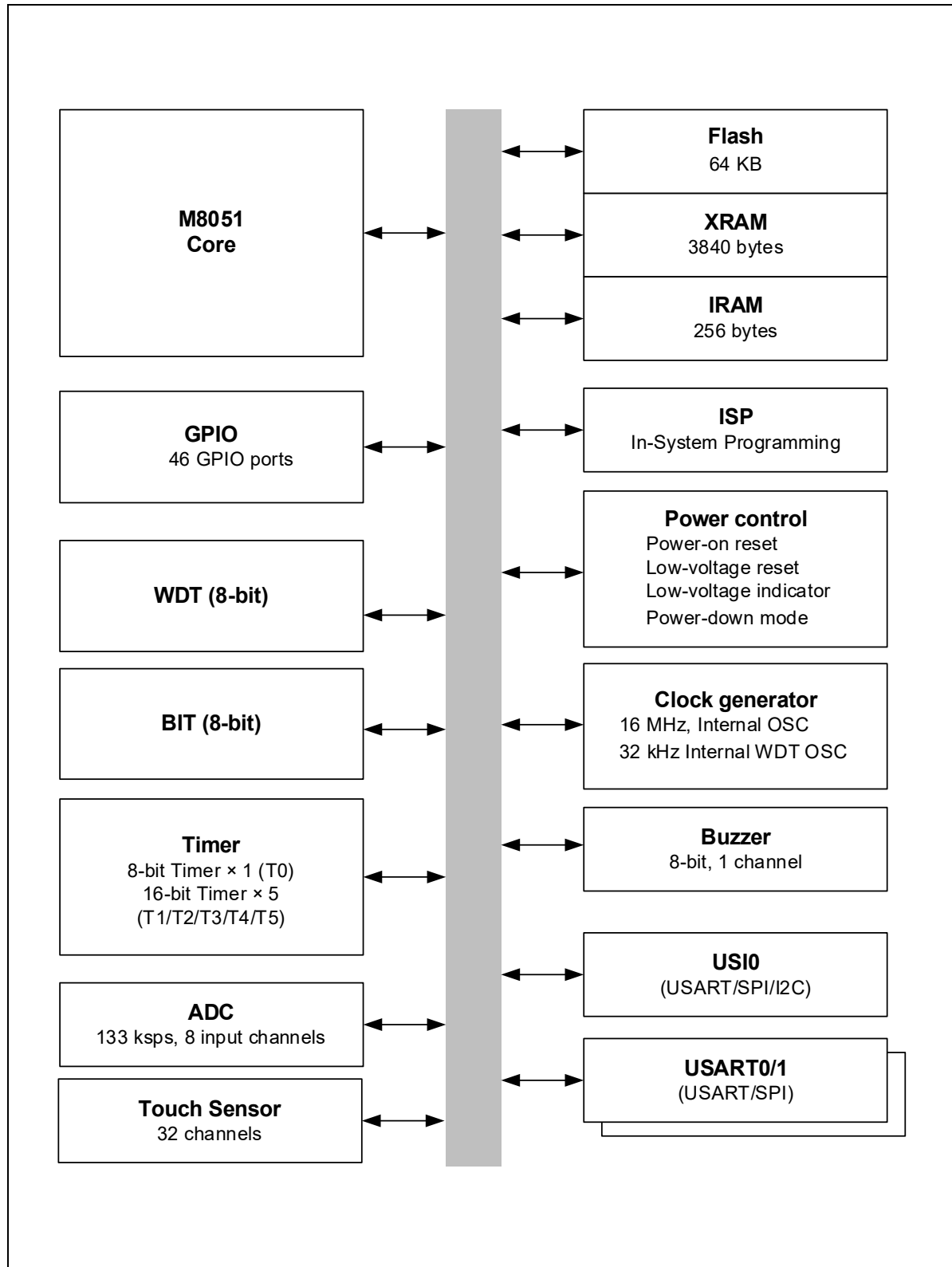
Table 4. Summary of A96T430 Peripherals

Peripheral		A96T430					
Code Flash Memory		64 KB					
SRAM		4 KB					
Timer	General-Purpose	8-bit Timer x 1 (T0) 16-bit Timer x 5 (T1/T2/T3/T4/T5)					
	Basic Interval Timer	1					
	Watchdog Timer	1					
	Watch Timer	1					
Communication Interfaces	USI	1 (USART/SPI/I2C)					
	USART	2 (USART/SPI)					
GPIO		46					
12-bit ADC	Sampling rate	380 ksp/s					
	Input channel	16					
Operating Frequency		16 MHz					
Operating Voltage		2.0 V to 5.5 V					
Operating Temperature		-40°C to +85°C, -40°C to +105°C					
Package		24-QFN	28-SOP	28-TSSOP	32-LQFP	44-LFQP	48-LQFP

2.3 Block Diagram

Figure 1 shows a block diagram of the A96T430 series.

Figure 1. Block Diagram of A96T430

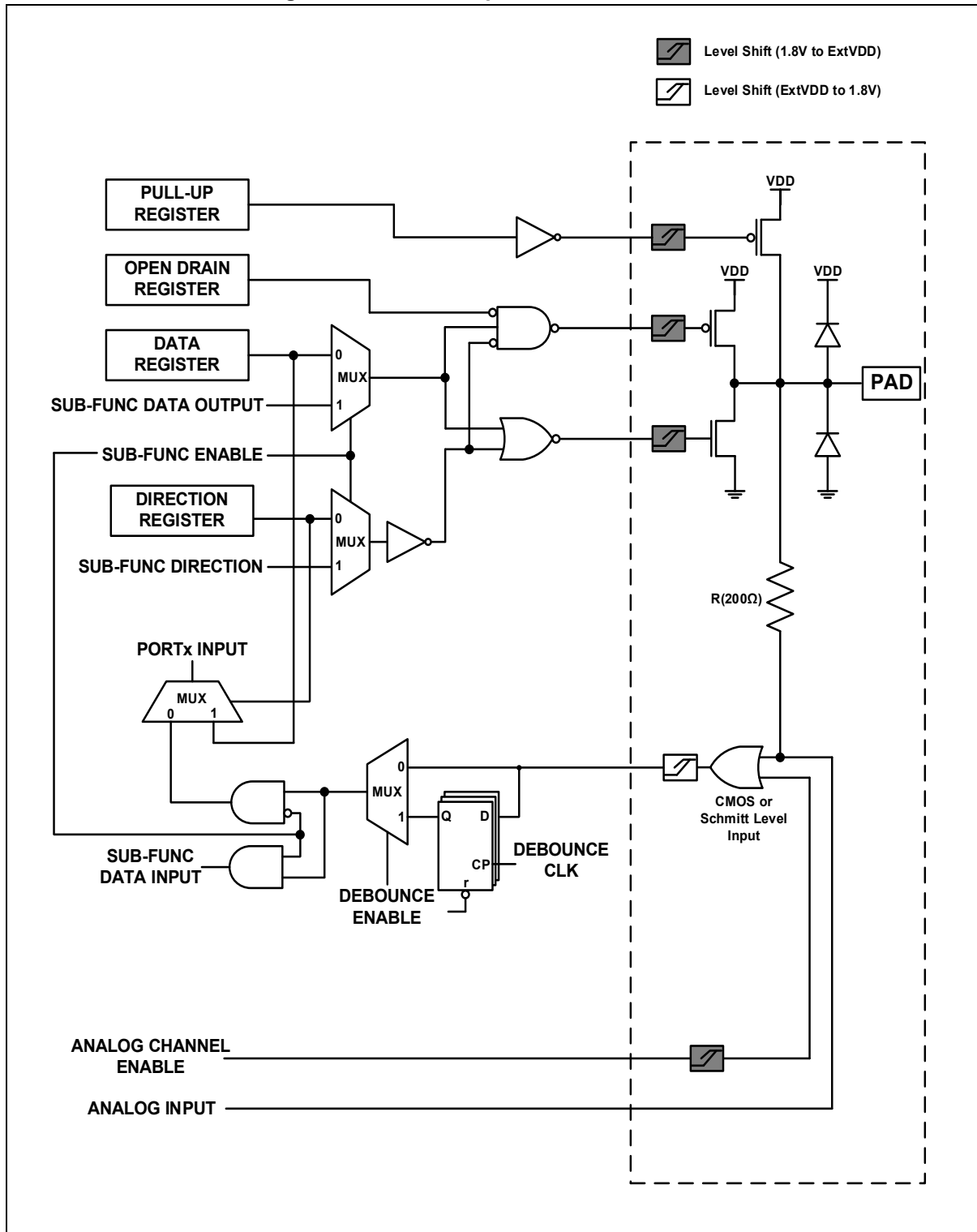


2.4 Functional Overview

The following sections provide overviews of the features of the A96T430 microcontroller.

2.4.1 Port Structure

Figure 2. General-Purpose I/O Port Structure



2.4.2 Memory Organization

The A96T430 addresses two separate address memory stores: Program memory and Data memory. The logical separation of Program and Data memory allows Data memory to be accessed by 8-bit addresses, which makes the 8-bit CPU access the data memory more rapidly. Nevertheless, 16-bit Data memory addresses can also be generated through the DPTR register.

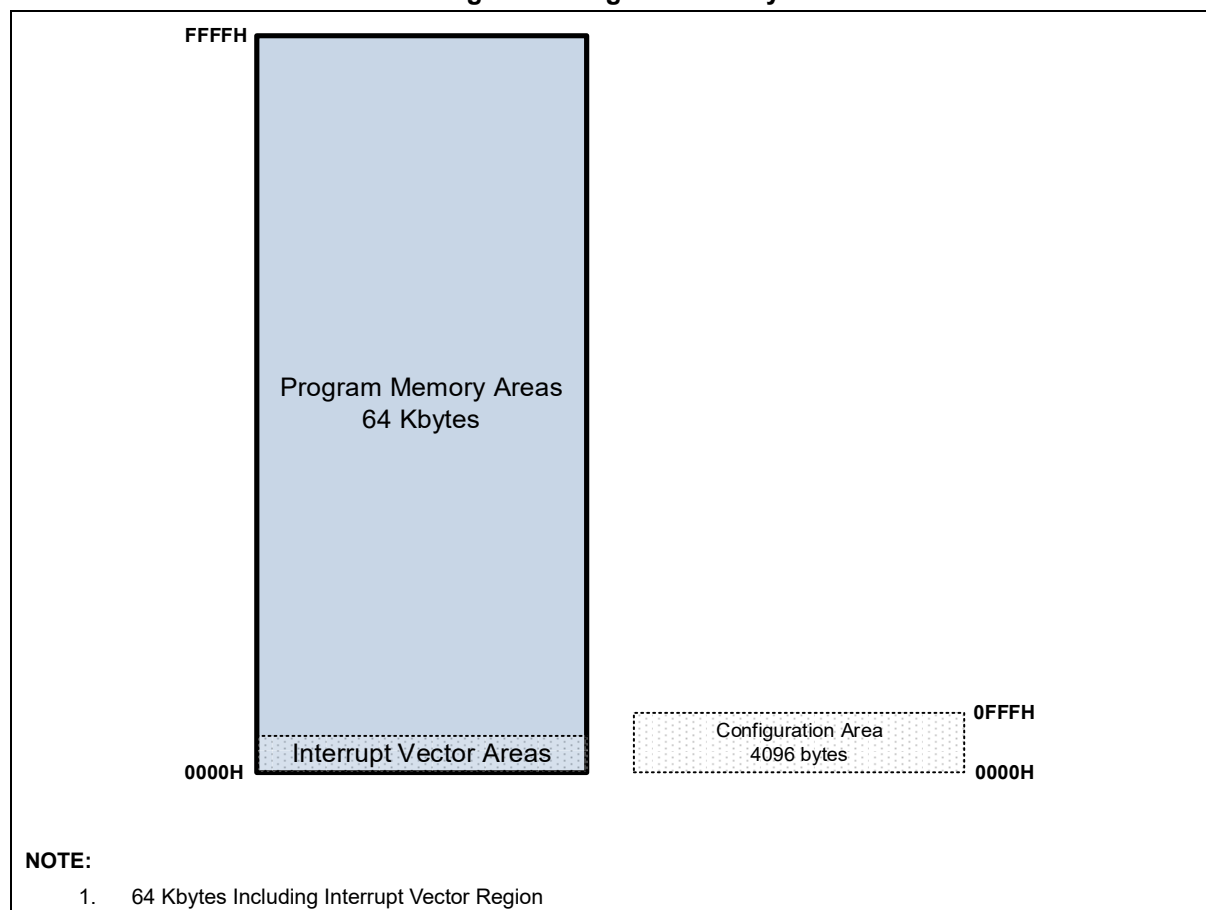
The A96T430 provides on-chip 64 Kbytes of the ISP type Flash program memory, which can be read and written to. Internal data memory (IRAM) is 256 bytes, and it includes the stack area. External data memory (XRAM) is 3840 bytes.

2.4.2.1 Program Memory

A 16-bit program counter can address up to 64 Kbytes, and this device has just 64 Kbytes program memory space.

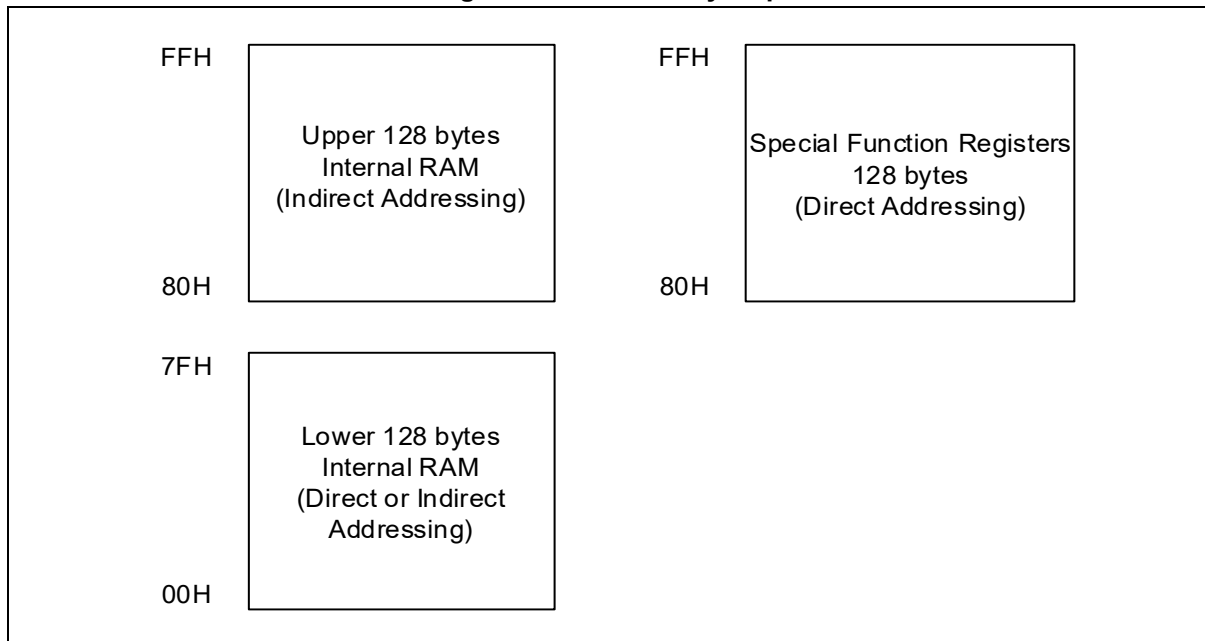
Figure 3 shows the map of the lower part of the program memory. After reset, the CPU begins execution from location 0000H. Each interrupt is assigned to a fixed location in program memory. The interruption causes the CPU to jump to that location, where it commences execution of the service routine. External interrupt 3, for example, is assigned to location 001BH. If external interrupt 3 is going to be used, its service routine must begin at location 001BH. If the interruption is not going to be used, its service location is available as general-purpose program memory. If an interrupt service routine is short enough (as is often the case in control applications), it can reside entirely within that 8 bytes interval. Longer service routines can use a jump instruction to skip over subsequent interrupt locations, if other interrupts are in use.

Figure 3. Program Memory



2.4.2.2 Data Memory

Figure 4. Data Memory Map



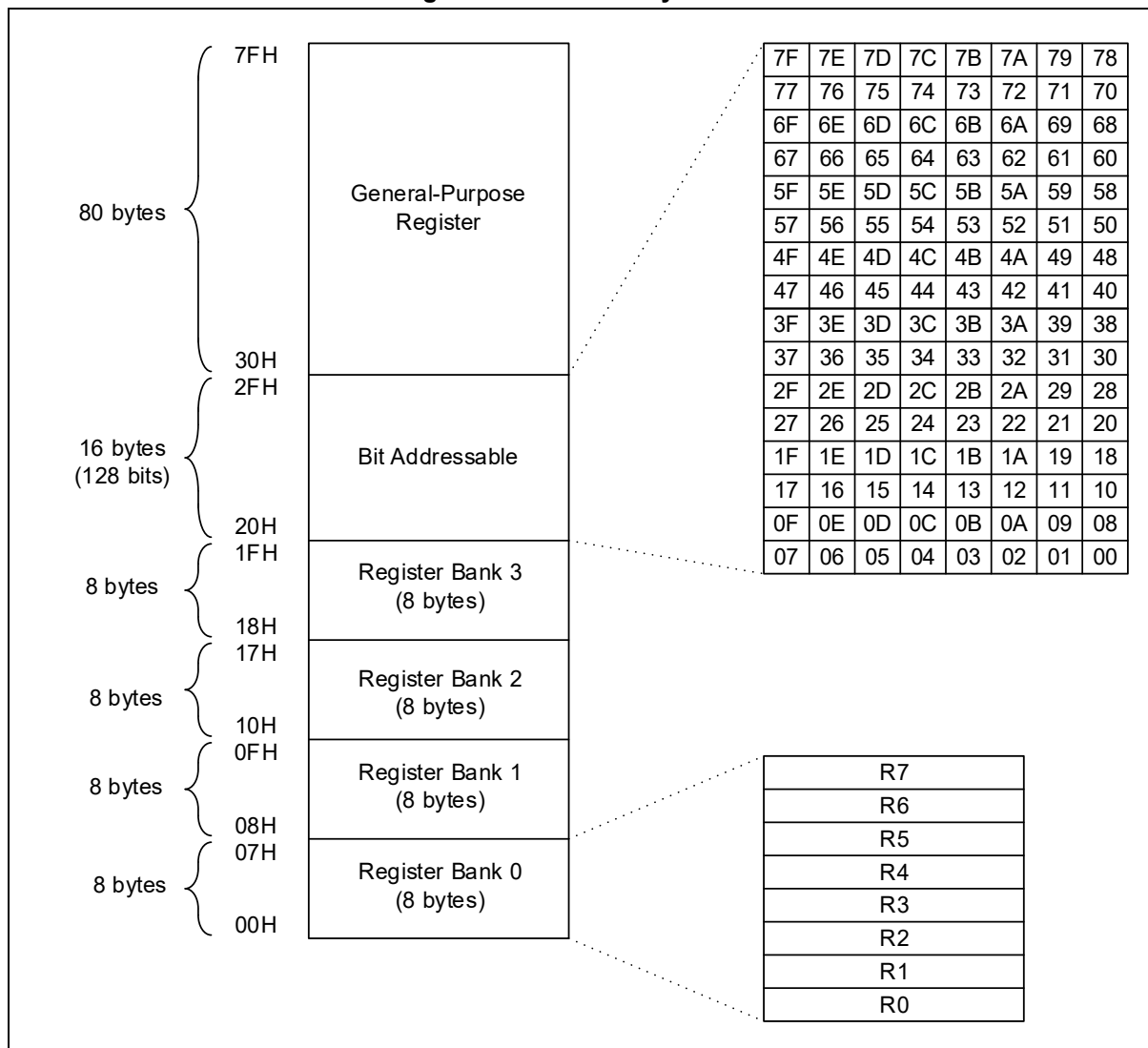
The internal data memory space is divided into three blocks, which are generally referred to as the lower 128 bytes, upper 128 bytes, and SFR space.

Internal data memory addresses are always one byte wide, which implies an address space of only 256 bytes. However, in fact, the addressing modes for internal RAM can accommodate up to 3840 bytes by using a simple trick. Direct addresses higher than 7FH access one memory space and indirect addresses higher than 7FH access a different memory space. Thus Figure 4 shows the upper 128 bytes and SFR space occupying the same block of addresses, 80H through FFH, although they are physically separate entities.

The lower 128 bytes of RAM are present in all 8051 devices as mapped in Figure 4. The lowest 32 bytes are grouped into 4 banks of 8 registers. Program instructions call out these registers as R0 through R7. Two bits in the Program Status Word select which register bank is in use. This allows more efficient use of code space, since register instructions are shorter than instructions that use direct addressing.

The next 16 bytes above the register banks form a block of bit-addressable memory space. The 8051-instruction set includes a wide selection of single-bit instructions, and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00H through 7FH.

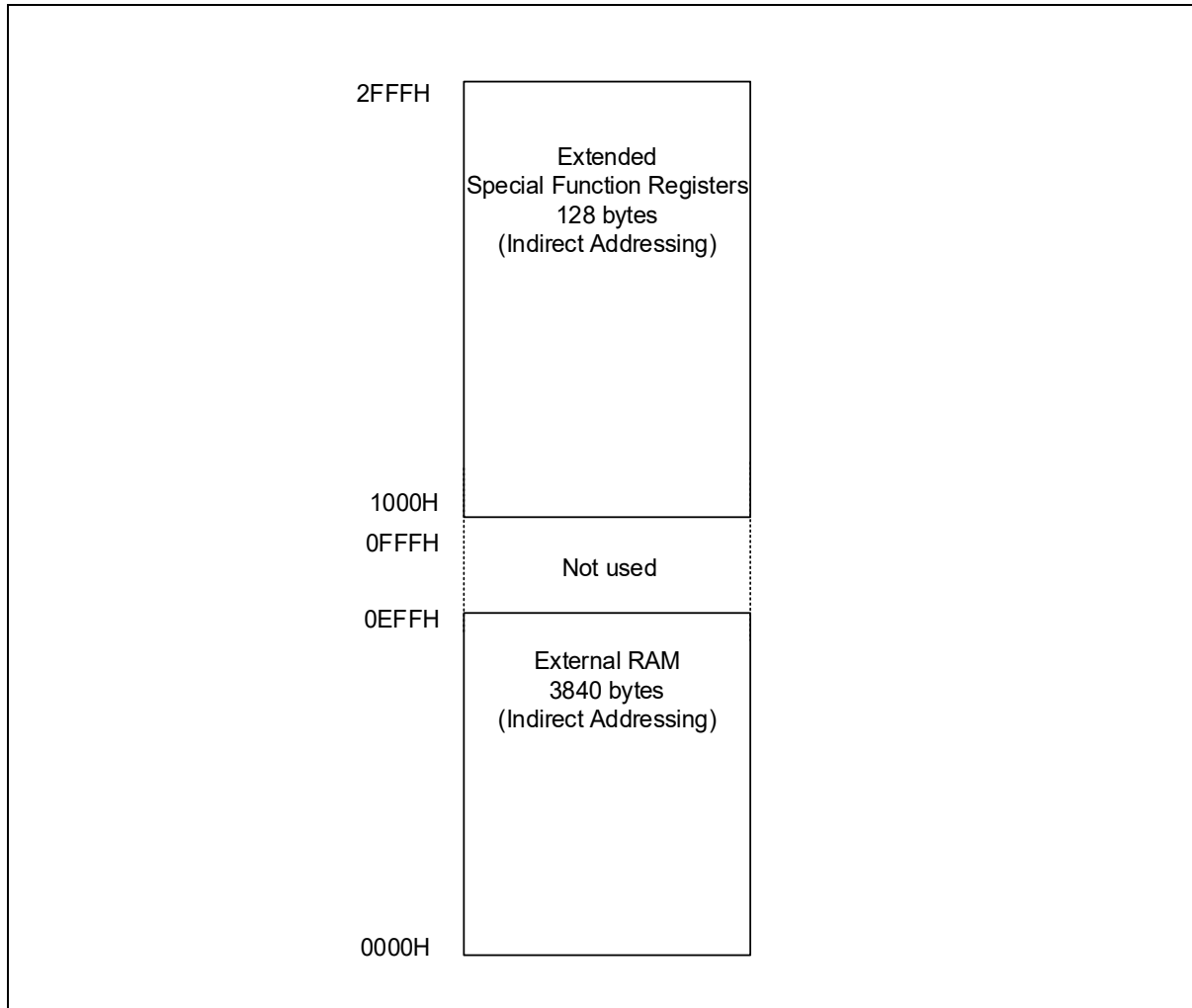
All the bytes in the lower 128 bytes can be accessed by either direct or indirect addressing. The upper 128 bytes RAM can only be accessed by indirect addressing. These spaces are used for data RAM and stack.

Figure 5. Lower 128-byte RAM

2.4.2.3 External Data Memory

The A96T430 has 3840 bytes XRAM and XSFR. This area has no relation with RAM/Flash. It can be read and written through SFR with 8-bit units.

Figure 6. XDATA Memory Area



2.4.2.4 SFR Map

Table 5. SFR Map Summary

Address	00H/8H ⁽¹⁾	01H/9H	02H/0AH	03H/0BH	04H/0CH	05H/0DH	06H/0EH	07H/0FH
0F8H	IP1	TS_CON	–	–	UBAUD	UDATA	–	–
0F0H	B	–	–	–	–	–	–	–
0E8H	RSTFR	–	–	–	–	–	–	–
0E0H	ACC	USI0ST1	USI0ST2	USI0BD	USI0SDHR	USI0DR	USI0SCLR	USI0SCHR
0D8H	LVR CR	USI0CR1	USI0CR2	USI0CR3	USI0CR4	USI0SAR	–	–
0D0H	PSW	P5IO	UCTRL21	UCTRL22	UCTRL23	UBAUD2	UDATA2	USTAT2
0C8H	OSCCR	P4IO	–	UCTRL1	UCTRL2	UCTRL3	–	USTAT
0C0H	EIFLAG0	P3IO	T2CRL	T2CRH	T2ADRL	T2ADRH	T2BDRL	T2BDRH
0B8H	IP	P2IO	T1CRL	T1CRH	T1ADRL	T1ADRH	T1BDRL	T1BDRH
0B0H	P5	P1IO	T0CR	T0CNT	T0DR/ T0CDR	P4PU	P5PU	WKCON
0A8H	IE	IE1	IE2	IE3	P0PU	P1PU	P2PU	P3PU
0A0H	P4	P0IO	EO	P5OD	EIPOL0L	EIPOL0H	EIFLAG1	EIPOL1
98H	P3	–	–	–	ADCCR1	ADCCRH	ADC1DR	ADC1RH
90H	P2	P0OD	P1OD	P2OD	P3OD	P4OD	WTCR	BUZCR
88H	P1	WTD1/ WTCNT	SCCR	BITCR	BITCNT	WDCR	WTD1/ WDCNT	BUZDR
80H	P0	SP	DPL	DPH	DPL1	DPH1	LVICR	PCON

NOTE:

1. 00H/8H, These registers are bit-addressable.

Table 6. XSFR Map Summary

Address	00H/8H ⁽¹⁾	01H/9H	02H/0AH	03H/0BH	04H/0CH	05H/0DH	06H/0EH	07H/0FH
1078H	–	–	–	–	–	–	–	–
1070H	–	–	–	–	–	–	–	–
1068H	–	–	–	–	–	–	–	–
1060H	–	–	–	–	–	–	–	–
1058H	–	–	–	–	–	–	–	–
1050H	P2_LEDD LY	–	–	–	–	–	–	–
1048H	P4FSRL	P4FSRH	P5FSRL	P5FSRH	DBCONT0	DBCONT1	DBCONT2	DBCONT3
1040H	P0FSRL	P0FSRH	P1FSRL	P1FSRH	P2FSRL	P2FSRH	P3FSRL	P3FSRH
1038H	–	–	–	–	–	–	–	–
1030H	UCTRL24	FPCR2	RTOCH2	RTOCL2	–	–	–	FETR
1028H	–	FEARM	FEARL	FEDR0	FEDR1	FEDR2	FEDR3	FECR
1020H	FEMR	–	FESR	–	–	–	–	–
1018H	UCTRL4	FPCR	RTOCH	RTOCL	CHECKS UM0	CHECKS UM1	CHECKS UM2	–
1010H	T5CRH	T5CRL	T5ADRH	T5ADRL	T5BDRH	T5BDRL	–	–
1008H	T4CRH	T4CRL	T4ADRH	T4ADRL	T4BDRH	T4BDRL	–	–
1000H	T3CRH	T3CRL	T3ADRH	T3ADRL	T3BDRH	T3BDRL	–	–

Table 6. XSFR Map Summary (continued)

Address	00H/8H ⁽¹⁾	01H/9H	02H/0AH	03H/0BH	04H/0CH	05H/0DH	06H/0EH	07H/0FH
2ED8H	–	TS_DIFF_CH_SEL	VDAC_ST ART_H	VDAC_ST ART_L	VDAC_ST OP_H	VDAC_ST OP_L	VDAC_C OMP_H	VDAC_C OMP_L
2ED0H	–	–	TS_CLK_CFG2	PS_SEQ_SEL	PRS_SEE D	SHLD_CO N	TS_LDO_CON	–
2EC8H	TS_TRIM	TS_CLK_CFG	TRIM_OS C	DELTA_O SC	TLED	–	–	TS_SLP_CON
2EC0H	–	TS_MOD E	TS_SUM_CNT	TS_CH_S EL3	TS_CH_S EL2	TS_CH_S EL1	TS_CH_S EL0	TS_S1_W IDH
2EB8H	SCO28_H	SCO28_L	SCO29_H	SCO29_L	SCO30_H	SCO30_L	SCO31_H	SCO31_L
2EB0H	SCO24_H	SCO24_L	SCO25_H	SCO25_L	SCO26_H	SCO26_L	SCO27_H	SCO27_L
2EA8H	SCO20_H	SCO20_L	SCO21_H	SCO21_L	SCO22_H	SCO22_L	SCO23_H	SCO23_L
2EA0H	SCO16_H	SCO16_L	SCO17_H	SCO17_L	SCO18_H	SCO18_L	SCO19_H	SCO19_L
2E98H	SCO12_H	SCO12_L	SCO13_H	SCO13_L	SCO14_H	SCO14_L	SCO15_H	SCO15_L
2E90H	SCO8_H	SCO8_L	SCO9_H	SCO9_L	SCO10_H	SCO10_L	SCO11_H	SCO11_L
2E88H	SCO4_H	SCO4_L	SCO5_H	SCO5_L	SCO6_H	SCO6_L	SCO7_H	SCO7_L
2E80H	SCO0_H	SCO0_L	SCO1_H	SCO1_L	SCO2_H	SCO2_L	SCO3_H	SCO3_L
2E78H	SUM_CH3_0_F0_H	SUM_CH3_0_F0_L	SUM_CH3_0_F1_H	SUM_CH3_0_F1_L	SUM_CH3_1_F0_H	SUM_CH3_1_F0_L	SUM_CH3_1_F1_H	SUM_CH3_1_F1_L
2E70H	SUM_CH2_8_F0_H	SUM_CH2_8_F0_L	SUM_CH2_8_F1_H	SUM_CH2_8_F1_L	SUM_CH2_9_F0_H	SUM_CH2_9_F0_L	SUM_CH2_9_F1_H	SUM_CH2_9_F1_L
2E68H	SUM_CH2_6_F0_H	SUM_CH2_6_F0_L	SUM_CH2_6_F1_H	SUM_CH2_6_F1_L	SUM_CH2_7_F0_H	SUM_CH2_7_F0_L	SUM_CH2_7_F1_H	SUM_CH2_7_F1_L
2E60H	SUM_CH2_4_F0_H	SUM_CH2_4_F0_L	SUM_CH2_4_F1_H	SUM_CH2_4_F1_L	SUM_CH2_5_F0_H	SUM_CH2_5_F0_L	SUM_CH2_5_F1_H	SUM_CH2_5_F1_L
2E58H	SUM_CH2_2_F0_H	SUM_CH2_2_F0_L	SUM_CH2_2_F1_H	SUM_CH2_2_F1_L	SUM_CH2_3_F0_H	SUM_CH2_3_F0_L	SUM_CH2_3_F1_H	SUM_CH2_3_F1_L
2E50H	SUM_CH2_0_F0_H	SUM_CH2_0_F0_L	SUM_CH2_0_F1_H	SUM_CH2_0_F1_L	SUM_CH2_1_F0_H	SUM_CH2_1_F0_L	SUM_CH2_1_F1_H	SUM_CH2_1_F1_L
2E48H	SUM_CH1_8_F0_H	SUM_CH1_8_F0_L	SUM_CH1_8_F1_H	SUM_CH1_8_F1_L	SUM_CH1_9_F0_H	SUM_CH1_9_F0_L	SUM_CH1_9_F1_H	SUM_CH1_9_F1_L
2E40H	SUM_CH1_6_F0_H	SUM_CH1_6_F0_L	SUM_CH1_6_F1_H	SUM_CH1_6_F1_L	SUM_CH1_7_F0_H	SUM_CH1_7_F0_L	SUM_CH1_7_F1_H	SUM_CH1_7_F1_L
2E38H	SUM_CH1_4_F0_H	SUM_CH1_4_F0_L	SUM_CH1_4_F1_H	SUM_CH1_4_F1_L	SUM_CH1_5_F0_H	SUM_CH1_5_F0_L	SUM_CH1_5_F1_H	SUM_CH1_5_F1_L
2E30H	SUM_CH1_2_F0_H	SUM_CH1_2_F0_L	SUM_CH1_2_F1_H	SUM_CH1_2_F1_L	SUM_CH1_3_F0_H	SUM_CH1_3_F0_L	SUM_CH1_3_F1_H	SUM_CH1_3_F1_L
2E28H	SUM_CH1_0_F0_H	SUM_CH1_0_F0_L	SUM_CH1_0_F1_H	SUM_CH1_0_F1_L	SUM_CH1_1_F0_H	SUM_CH1_1_F0_L	SUM_CH1_1_F1_H	SUM_CH1_1_F1_L
2E20H	SUM_CH8_F0_H	SUM_CH8_F0_L	SUM_CH8_F1_H	SUM_CH8_F1_L	SUM_CH9_F0_H	SUM_CH9_F0_L	SUM_CH9_F1_H	SUM_CH9_F1_L
2E18H	SUM_CH6_F0_H	SUM_CH6_F0_L	SUM_CH6_F1_H	SUM_CH6_F1_L	SUM_CH7_F0_H	SUM_CH7_F0_L	SUM_CH7_F1_H	SUM_CH7_F1_L
2E10H	SUM_CH4_F0_H	SUM_CH4_F0_L	SUM_CH4_F1_H	SUM_CH4_F1_L	SUM_CH5_F0_H	SUM_CH5_F0_L	SUM_CH5_F1_H	SUM_CH5_F1_L
2E08H	SUM_CH2_F0_H	SUM_CH2_F0_L	SUM_CH2_F1_H	SUM_CH2_F1_L	SUM_CH3_F0_H	SUM_CH3_F0_L	SUM_CH3_F1_H	SUM_CH3_F1_L
2E00H	SUM_CH0_F0_H	SUM_CH0_F0_L	SUM_CH0_F1_H	SUM_CH0_F1_L	SUM_CH1_F0_H	SUM_CH1_F0_L	SUM_CH1_F1_H	SUM_CH1_F1_L

Table 6. XSFR Map Summary (continued)

Address	00H/8H(1)	01H/9H	02H/0AH	03H/0BH	04H/0CH	05H/0DH	06H/0EH	07H/0FH
2FD8H	—	—	—	—	—	—	—	—
2FD0H	—	—	—	—	—	—	—	—
2FC8H	—	—	—	—	—	—	—	—
2FC0H	—	—	—	—	—	—	—	—
2FB8H	—	—	—	—	—	—	—	—
2FB0H	—	—	—	—	—	—	—	—
2FA8H	—	—	—	—	—	—	—	—
2FA0H	—	—	—	—	—	—	—	—
2F98H	—	—	—	—	—	—	—	—
2F90H	—	—	—	—	—	—	—	—
2F88H	—	—	—	—	—	—	—	—
2F80H	—	—	—	—	—	—	—	—
2F78H	—	—	—	—	—	—	—	—
2F70H	—	—	—	—	—	—	—	—
2F68H	—	—	—	—	—	—	—	—
2F60H	—	—	—	—	—	—	—	—
2F58H	—	—	—	—	—	—	—	—
2F50H	—	—	—	—	—	—	—	—
2F48H	—	—	—	—	—	—	—	—
2F40H	—	—	—	—	—	—	—	—
2F38H	—	—	—	—	—	—	—	—
2F30H	—	—	—	—	—	—	—	—
2F28H	—	—	—	—	—	—	—	—
2F20H	—	—	—	—	—	—	—	—
2F18H	—	—	—	—	—	—	—	—
2F10H	—	—	—	—	—	—	—	—
2F08H	—	—	—	—	—	—	—	—
2F00H	—	—	—	—	—	—	—	—

Table 7. SFR Map

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
80H	P0 Data Register	P0	R/W	0	0	0	0	0	0	0	0
81H	Stack Pointer	SP	R/W	0	0	0	0	0	1	1	1
82H	Data Pointer Register Low	DPL	R/W	0	0	0	0	0	0	0	0
83H	Data Pointer Register High	DPH	R/W	0	0	0	0	0	0	0	0
84H	Data Pointer Register Low 1	DPL1	R/W	0	0	0	0	0	0	0	0
85H	Data Pointer Register High 1	DPH1	R/W	0	0	0	0	0	0	0	0
86H	Low Voltage Indicator Control Register	LVICR	R/W	–	–	0	0	0	0	0	0
87H	Power Control Register	PCON	R/W	0	–	–	–	0	0	0	0
88H	P1 Data Register	P1	R/W	0	0	0	0	0	0	0	0
89H	Watch Timer Data Register	WTDR	W	0	1	1	1	1	1	1	1
	Watch Timer Counter Register	WTCNT	R	–	0	0	0	0	0	0	0
8AH	System and Clock Control Register	SCCR	R/W	–	–	–	–	–	–	0	0
8BH	Basic Interval Timer Control Register	BITCR	R/W	0	1	0	0	0	1	0	1
8CH	Basic Interval Timer Counter Register	BITCNT	R	0	0	0	0	0	0	0	0
8DH	Watchdog Timer Control Register	WDTCR	R/W	0	0	0	–	–	–	0	0
8EH	Watchdog Timer Data Register	WDTDR	W	1	1	1	1	1	1	1	1
	Watchdog Timer Counter Register	WDCNT	R	0	0	0	0	0	0	0	0
8FH	BUZZER Data Register	BUZDR	R/W	1	1	1	1	1	1	1	1
90H	P2 Data Register	P2	R/W	0	0	0	0	0	0	0	0
91H	P0 Open-drain Selection Register	P0OD	R/W	0	0	0	0	0	0	0	0
92H	P1 Open-drain Selection Register	P1OD	R/W	0	0	0	0	0	0	0	0
93H	P2 Open-drain Selection Register	P2OD	R/W	0	0	0	0	0	0	0	0
94H	P3 Open-drain Selection Register	P3OD	R/W	0	0	0	0	0	0	0	0
95H	P4 Open-drain Selection Register	P4OD	R/W	0	0	0	0	0	0	0	0
96H	Watch Timer Control Register	WTCR	R/W	0	–	–	0	0	0	0	0
97H	BUZZER Control Register	BUZCR	R/W	–	–	–	–	–	0	0	0
98H	P3 Data Register	P3	R/W	–	–	0	0	0	0	0	0
99H	Reserved	–	–	–	–	–	–	–	–	–	–
9AH	Reserved	–	–	–	–	–	–	–	–	–	–
9BH	Reserved	–	–	–	–	–	–	–	–	–	–
9CH	A/D Converter Control Low Register	ADCCRL	R/W	0	0	0	0	–	0	0	0
9DH	A/D Converter Control High Register	ADCCRH	R/W	0	0	0	0	0	0	0	1
9EH	A/D Converter Data Low Register	ADCDRL	R	0	0	0	0	0	0	0	0
9FH	A/D Converter Data High Register	ADCDRH	R	0	0	0	0	0	0	0	0

Table 7. SFR Map (continued)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
A0H	P4 Data Register	P4	R/W	0	0	0	0	0	0	0	0
A1H	P0 Direction Register	P0IO	R/W	0	0	0	0	0	0	0	0
A2H	Extended Operation Register	EO	R/W	–	–	–	0	–	0	0	0
A3H	P5 Open-drain Selection Register	P5OD	R/W	0	0	0	0	0	0	0	0
A4H	External Interrupt Polarity 0 Low Register	EIPOL0L	R/W	0	0	0	0	0	0	0	0
A5H	External Interrupt Polarity 0 High Register	EIPOL0H	R/W	–	–	–	–	0	0	0	0
A6H	External Interrupt Flag 1 Register	EIFLAG1	R/W	0	0	–	–	0	0	0	0
A7H	External Interrupt Polarity 1 Register	EIPOL1	R/W	0	0	0	0	0	0	0	0
A8H	Interrupt Enable Register	IE	R/W	0	–	0	0	0	0	0	0
A9H	Interrupt Enable Register 1	IE1	R/W	–	–	0	0	0	0	–	0
AAH	Interrupt Enable Register 2	IE2	R/W	–	–	0	0	0	0	0	0
ABH	Interrupt Enable Register 3	IE3	R/W	–	–	0	0	0	0	0	0
ACH	P0 Pull-up Resistor Selection Register	P0PU	R/W	0	0	0	0	0	0	0	0
ADH	P1 Pull-up Resistor Selection Register	P1PU	R/W	0	0	0	0	0	0	0	0
AEH	P2 Pull-up Resistor Selection Register	P2PU	R/W	0	0	0	0	0	0	0	0
AFH	P3 Pull-up Resistor Selection Register	P3PU	R/W	–	–	–	–	–	–	0	0
B0H	P5 Data Register	P5	R/W	0	0	0	0	0	0	0	0
B1H	P1 Direction Register	P1IO	R/W	0	0	0	0	0	0	0	0
B2H	Timer 0 Control Register	T0CR	R/W	0	–	0	0	0	0	0	0
B3H	Timer 0 Counter Register	T0CNT	R	0	0	0	0	0	0	0	0
B4H	Timer 0 Data Register	T0DR	R/W	1	1	1	1	1	1	1	1
	Timer 0 Capture Data Register	T0CDR	R	0	0	0	0	0	0	0	0
B5H	P4 Pull-up Resistor Selection Register	P4PU	R/W	0	0	0	0	0	0	0	0
B6H	P5 Pull-up Resistor Selection Register	P5PU	R/W	0	0	0	0	0	0	0	0
B7H	Wake up Control Register	WKCON	RW	0	1	1	1	0	0	0	0
B8H	Interrupt Priority Register	IP	R/W	–	–	0	0	0	0	0	0
B9H	P2 Direction Register	P2IO	R/W	0	0	0	0	0	0	0	0
BAH	Timer 1 Control Low Register	T1CRL	R/W	0	0	0	0	–	0	0	0
BBH	Timer 1 Counter High Register	T1CRH	R/W	0	–	0	0	–	–	–	0
BCH	Timer 1 A Data Low Register	T1ADRL	R/W	1	1	1	1	1	1	1	1
BDH	Timer 1 A Data High Register	T1ADRH	R/W	1	1	1	1	1	1	1	1
BEH	Timer 1 B Data Low Register	T1BDRL	R/W	1	1	1	1	1	1	1	1
BFH	Timer 1 B Data High Register	T1BDRH	R/W	1	1	1	1	1	1	1	1

Table 7. SFR Map (continued)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
C0H	External Interrupt Flag 0 Register	EIFLAG0	R/W	–	–	0	0	0	0	0	0
C1H	P3 Direction Register	P3IO	R/W	–	–	–	–	–	–	0	0
C2H	Timer 2 Control Low Register	T2CRL	R/W	0	0	0	0	–	0	–	0
C3H	Timer 2 Control High Register	T2CRH	R/W	0	–	0	0	–	–	–	0
C4H	Timer 2 A Data Low Register	T2ADRL	R/W	1	1	1	1	1	1	1	1
C5H	Timer 2 A Data High Register	T2ADRH	R/W	1	1	1	1	1	1	1	1
C6H	Timer 2 B Data Low Register	T2BDRL	R/W	1	1	1	1	1	1	1	1
C7H	Timer 2 B Data High Register	T2BDRH	R/W	1	1	1	1	1	1	1	1
C8H	Oscillator Control Register	OSCCR	R/W	0	0	1	0	1	0	–	0
C9H	P4 Direction Register	P4IO	R/W	0	0	0	0	0	0	0	0
CAH	Reserved	–	–	–	–	–	–	–	–	–	–
CBH	USART Control Register 1	UCTRL1	R/W	0	0	0	0	0	0	0	0
CCH	USART Control Register 2	UCTRL2	R/W	0	0	0	0	0	0	0	0
CDH	USART Control Register 3	UCTRL3	R/W	0	0	0	0	–	0	0	0
CEH	Reserved	–	–	–	–	–	–	–	–	–	–
CFH	USART Status Register	USTAT	R/W	1	0	0	0	0	0	0	0
D0H	Program Status Word Register	PSW	R/W	0	0	0	0	0	0	0	0
D1H	P5 Direction Register	P5IO	R/W	0	0	0	0	0	0	0	0
D2H	USART2 Control Register 1	UCTRL21	R/W	0	0	0	0	0	0	0	0
D3H	USART2 Control Register 2	UCTRL22	R/W	0	0	0	0	0	0	0	0
D4H	USART2 Control Register 3	UCTRL23	R/W	0	0	0	0	–	0	0	0
D5H	USART2 Baud Rate Generation Register	UBAUD2	R/W	1	1	1	1	1	1	1	1
D6H	USART2 Data Register	UDATA2	R/W	0	0	0	0	0	0	0	0
D7H	USART2 Status Register	USTAT2	R/W	1	0	0	0	0	0	0	0
D8H	Low Voltage Reset Control Register	LVRCR	R/W	–	–	–	0	0	0	0	0
D9H	USI0 Control Register 1	USI0CR1	R/W	0	0	0	0	0	0	0	0
DAH	USI0 Control Register 2	USI0CR2	R/W	0	0	0	0	0	0	0	0
DBH	USI0 Control Register 3	USI0CR3	R/W	0	0	0	0	0	0	0	0
DCH	USI0 Control Register 4	USI0CR4	R/W	0	–	0	0	0	0	0	0
DDH	USI0 Slave Address Register	USI0SAR	R/W	0	0	0	0	0	0	0	0
DEH	Reserved	–	–	–	–	–	–	–	–	–	–
DFH	Reserved	–	–	–	–	–	–	–	–	–	–

Table 7. SFR Map (continued)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
E0H	Accumulator Register	ACC	R/W	0	0	0	0	0	0	0	0
E1H	USI0 Status Register 1	USI0ST1	R/W	1	0	0	0	0	0	0	0
E2H	USI0 Status Register 2	USI0ST2	R	0	0	0	0	0	0	0	0
E3H	USI0 Baud Rate Generation Register	USI0BD	R/W	1	1	1	1	1	1	1	1
E4H	USI0 SDA Hold Time Register	USI0SHDR	R/W	0	0	0	0	0	0	0	1
E5H	USI0 Data Register	USI0DR	R/W	0	0	0	0	0	0	0	0
E6H	USI0 SCL Low Period Register	USI0SCLR	R/W	0	0	1	1	1	1	1	1
E7H	USI0 SCL High Period Register	USI0SCHR	R/W	0	0	1	1	1	1	1	1
E8H	Reset Flag Register	RSTFR	R/W	1	x	0	0	x	–	–	–
E9H	Reserved	–	–	–	–	–	–	–	–	–	–
EAH	Reserved	–	–	–	–	–	–	–	–	–	–
EBH	Reserved	–	–	–	–	–	–	–	–	–	–
ECH	Reserved	–	–	–	–	–	–	–	–	–	–
EDH	Reserved	–	–	–	–	–	–	–	–	–	–
EEH	Reserved	–	–	–	–	–	–	–	–	–	–
EFH	Reserved	–	–	–	–	–	–	–	–	–	–
F0H	B Register	B	R/W	0	0	0	0	0	0	0	0
F1H	Reserved	–	–	–	–	–	–	–	–	–	–
F2H	Reserved	–	–	–	–	–	–	–	–	–	–
F3H	Reserved	–	–	–	–	–	–	–	–	–	–
F4H	Reserved	–	–	–	–	–	–	–	–	–	–
F5H	Reserved	–	–	–	–	–	–	–	–	–	–
F6H	Reserved	–	–	–	–	–	–	–	–	–	–
F7H	Reserved	–	–	–	–	–	–	–	–	–	–
F8H	Interrupt Priority Register 1	IP1	R/W	–	–	0	0	0	0	0	0
F9H	Touch Sensor Control Register	TS_CON	R/W	0	0	0	0	0	0	0	0
FAH	Reserved	–	–	–	–	–	–	–	–	–	–
FBH	Reserved	–	–	–	–	–	–	–	–	–	–
FCH	USART Baud Rate Generation Register	UBAUD	R/W	1	1	1	1	1	1	1	1
FDH	USART Data Register	UDATA	R/W	0	0	0	0	0	0	0	0
FEH	Reserved	–	–	–	–	–	–	–	–	–	–
FFH	Reserved	–	–	–	–	–	–	–	–	–	–

Table 8. XSFR Map

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
1000H	Timer 3 Control High Register	T3CRH	R/W	0	–	0	0	–	–	–	0
1001H	Timer 3 Control Low Register	T3CRL	R/W	0	0	0	0	–	0	0	0
1002H	Timer 3 A Data High Register	T3ADRH	R/W	1	1	1	1	1	1	1	1
1003H	Timer 3 A Data Low Register	T3ADRL	R/W	1	1	1	1	1	1	1	1
1004H	Timer 3 B Data High Register	T3BDRH	R/W	1	1	1	1	1	1	1	1
1005H	Timer 3 B Data Low Register	T3BDRL	R/W	1	1	1	1	1	1	1	1
1006H	Reserved	–	–	–	–	–	–	–	–	–	–
1007H	Reserved	–	–	–	–	–	–	–	–	–	–
1008H	Timer 4 Control High Register	T4CRH	R/W	0	–	0	0	–	–	–	0
1009H	Timer 4 Control Low Register	T4CRL	R/W	0	0	0	0	–	0	–	0
100AH	Timer 4 A Data High Register	T4ADRH	R/W	1	1	1	1	1	1	1	1
100BH	Timer 4 A Data Low Register	T4ADRL	R/W	1	1	1	1	1	1	1	1
100CH	Timer 4 B Data High Register	T4BDRH	R/W	1	1	1	1	1	1	1	1
100DH	Timer 4 B Data Low Register	T4BDRL	R/W	1	1	1	1	1	1	1	1
100EH	Reserved	–	–	–	–	–	–	–	–	–	–
100FH	Reserved	–	–	–	–	–	–	–	–	–	–
1010H	Timer 5 Control High Register	T5CRH	R/W	0	–	0	0	–	–	–	0
1011H	Timer 5 Control Low Register	T5CRL	R/W	0	0	0	0	–	0	–	0
1012H	Timer 5 A Data High Register	T5ADRH	R/W	1	1	1	1	1	1	1	1
1013H	Timer 5 A Data Low Register	T5ADRL	R/W	1	1	1	1	1	1	1	1
1014H	Timer 5 B Data High Register	T5BDRH	R/W	1	1	1	1	1	1	1	1
1015H	Timer 5 B Data Low Register	T5BDRL	R/W	1	1	1	1	1	1	1	1
1016H	Reserved	–	–	–	–	–	–	–	–	–	–
1017H	Reserved	–	–	–	–	–	–	–	–	–	–
1018H	USART Control Register 4	UCTRL4	R/W	–	–	–	0	0	0	0	0
1019H	USART Floating Point Counter	FPCR	R/W	0	0	0	0	0	0	0	0
101AH	Receiver Time Out Counter High Register	RTOCH	R	0	0	0	0	0	0	0	0
101BH	Receiver Time Out Counter Low Register	RTOCL	R	0	0	0	0	0	0	0	0
101CH	Checksum Register0	CHECKSUM0	R	0	0	0	0	0	0	0	0
101DH	Checksum Register1	CHECKSUM1	R	0	0	0	0	0	0	0	0
101EH	Checksum Register2	CHECKSUM2	R	0	0	0	0	0	0	0	0
101FH	Reserved	–	–	–	–	–	–	–	–	–	–

Table 8. XSFR Map (continued)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
1020H	Flash Mode Register	FEMR	R/W	0	–	0	0	0	0	0	0
1021H	Reserved	–	–	–	–	–	–	–	–	–	–
1022H	Flash Status Register	FESR	R/W	1	–	–	–	0	0	0	0
1023H	Reserved	–	–	–	–	–	–	–	–	–	–
1024H	Reserved	–	–	–	–	–	–	–	–	–	–
1025H	Reserved	–	–	–	–	–	–	–	–	–	–
1026H	Reserved	–	–	–	–	–	–	–	–	–	–
1027H	Reserved	–	–	–	–	–	–	–	–	–	–
1028H	Reserved	–	–	–	–	–	–	–	–	–	–
1029H	Flash Address Middle Register	FEARM	R/W	0	0	0	0	0	0	0	0
102AH	Flash Address Low Register	FEARL	R/W	0	0	0	0	0	0	0	0
102BH	Flash Data Register0	FEDR0	R/W	0	0	0	0	0	0	0	0
102CH	Flash Data Register1	FEDR1	R/W	0	0	0	0	0	0	0	0
102DH	Flash Data Register2	FEDR2	R/W	0	0	0	0	0	0	0	0
102EH	Flash Data Register3	FEDR3	R/W	0	0	0	0	0	0	0	0
102FH	Flash Control Register	FECR	R/W	0	0	0	0	0	0	1	1
1030H	USART2 Control Register 4	UCTR24	R/W	0	0	0	0	0	0	0	0
1031H	USART Floating Point Counter2	FPCR2	R/W	0	0	0	0	0	0	0	0
1032H	Receiver Time Out Counter High Register2	RTOCH2	R	0	0	0	0	0	0	0	0
1033H	Receiver Time Out Counter Low Register2	RTOCL2	R	0	0	0	0	0	0	0	0
1034H	Reserved	–	–	–	–	–	–	–	–	–	–
1035H	Reserved	–	–	–	–	–	–	–	–	–	–
1036H	Reserved	–	–	–	–	–	–	–	–	–	–
1037H	Flash Test Register	FETR	R/W	0	0	0	0	0	0	0	0
1038H	Reserved	–	–	–	–	–	–	–	–	–	–
1039H	Reserved	–	–	–	–	–	–	–	–	–	–
103AH	Reserved	–	–	–	–	–	–	–	–	–	–
103BH	Reserved	–	–	–	–	–	–	–	–	–	–
103CH	Reserved	–	–	–	–	–	–	–	–	–	–
103DH	Reserved	–	–	–	–	–	–	–	–	–	–
103EH	Reserved	–	–	–	–	–	–	–	–	–	–
103FH	Reserved	–	–	–	–	–	–	–	–	–	–

Table 8. XSFR Map (continued)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
1040H	P0 Function Selection Low Register	P0FSRL	R/W	0	0	0	0	0	0	0	0
1041H	P0 Function Selection High Register	P0FSRH	R/W	0	0	0	0	0	0	0	0
1042H	P1 Function Selection Low Register	P1FSRL	R/W	0	0	0	0	0	0	0	0
1043H	P1 Function Selection High Register	P1FSRH	R/W	0	0	0	0	0	0	0	0
1044H	P2 Function Selection Low Register	P2FSRL	R/W	0	0	0	0	0	0	0	0
1045H	P2 Function Selection High Register	P2FSRH	R/W	0	0	0	0	0	0	0	0
1046H	P3 Function Selection Low Register	P3FSRL	R/W	0	0	0	0	0	0	0	0
1047H	P3 Function Selection High Register	P3FSRH	R/W	0	0	0	0	0	0	0	0
1048H	P4 Function Selection Low Register	P4FSRL	R/W	0	0	0	0	0	0	0	0
1049H	P4 Function Selection High Register	P4FSRH	R/W	0	0	0	0	0	0	0	0
104AH	P5 Function Selection Low Register	P5FSRL	R/W	0	0	0	0	0	0	0	0
104BH	P5 Function Selection High Register	P5FSRH	R/W	0	0	0	0	0	0	0	0
104CH	Port Debounce Control Register 0	DBCNT0	R/W	0	0	0	0	0	0	0	0
104DH	Port Debounce Control Register 1	DBCNT1	R/W	0	0	0	0	0	0	0	0
104EH	Port Debounce Control Register 2	DBCNT2	R/W	0	0	0	0	0	0	0	0
104FH	Port Debounce Control Register 3	DBCNT3	R/W	0	0	0	0	0	0	0	0
1050H	P2 Led delay enable register	P2LEDDLY	R/W	1	1	1	1	1	1	1	1
1051H	Reserved	—	—	—	—	—	—	—	—	—	—
1052H	Reserved	—	—	—	—	—	—	—	—	—	—
1053H	Reserved	—	—	—	—	—	—	—	—	—	—
1054H	Reserved	—	—	—	—	—	—	—	—	—	—
1055H	Reserved	—	—	—	—	—	—	—	—	—	—
1056H	Reserved	—	—	—	—	—	—	—	—	—	—
1057H	Reserved	—	—	—	—	—	—	—	—	—	—
1058H	Reserved	—	—	—	—	—	—	—	—	—	—
1059H	Reserved	—	—	—	—	—	—	—	—	—	—
105AH	Reserved	—	—	—	—	—	—	—	—	—	—
105BH	Reserved	—	—	—	—	—	—	—	—	—	—
105CH	Reserved	—	—	—	—	—	—	—	—	—	—
105DH	Reserved	—	—	—	—	—	—	—	—	—	—
105EH	Reserved	—	—	—	—	—	—	—	—	—	—
105FH	Reserved	—	—	—	—	—	—	—	—	—	—

2.4.3 I/O Ports

2.4.3.1 P0 Port

P0 is 8-bit I/O port. P0 control registers consist of P0 data register (P0), P0 direction register (P0IO), debounce enable register (P0DB), P0 pull-up resistor selection register (P0PU), and P0 open-drain selection register (P0OD). Refer to the port function selection registers for the P0 function selection.

2.4.3.2 P1 Port

P1 is an 8-bit I/O port. P1 control registers consist of P1 data register (P1), P1 direction register (P1IO), debounce enable register (P123DB), P1 pull-up resistor selection register (P1PU), and P1 open-drain selection register (P1OD). Refer to the port function selection registers for the P1 function selection.

2.4.3.3 P2 Port

P2 is an 8-bit I/O port. P2 control registers consist of P2 data register (P2), P2 direction register (P2IO), P2 pull-up resistor selection register (P2PU) and P2 open-drain selection register (P2OD). Refer to the port function selection registers for the P2 function selection.

2.4.3.4 P3 Port

P3 is an 8-bit I/O port. P3 control registers consist of P3 data register (P3), P3 direction register (P3IO) and P3 pull-up resistor selection register (P3PU). Refer to the port function selection registers for the P3 function selection.

2.4.3.5 P4 Port

P4 is an 8-bit I/O port. P4 control registers consist of P4 data register (P4), P4 direction register (P4IO) and P4 pull-up resistor selection register (P4PU). Refer to the port function selection registers for the P4 function selection.

2.4.3.6 P5 Port

P5 is a 2-bit I/O port. P5 control registers consist of P5 data register (P5), P5 direction register (P5IO) and P5 pull-up resistor selection register (P5PU). Refer to the port function selection registers for the P5 function selection.

2.4.4 Interrupt Controller

The A96T430 supports up to 24 interrupt sources. The interrupts have separate enable register bits associated with them, allowing software control. They can also have four levels of priority assigned to them. The non-maskable interrupt source is always enabled with a higher priority than any other interrupt source and is not controllable by software. The interrupt controller has the following features:

- Receive the request from 24 interrupt sources.
- 6 group priorities
- 4 priority levels
- Multi Interrupt possibility
- If the requests of different priority levels are received simultaneously, the request of higher priority level is served first.
- Each interrupt source can be controlled by EA bit and each IEx bit.
- Interrupt latency: 3 to 9 machine cycles in single interrupt system.

The non-maskable interrupt is always enabled. The maskable interrupts are enabled through four pairs of interrupts enable registers (IE, IE1, IE2, and IE3). Each bit of IE, IE1, IE2, IE3 register individually enables/disables the corresponding interrupt source. Overall control is provided by bit 7 of IE (EA). When EA is set to '0', all interrupts are disabled: when EA is set to '1', interrupts are individually enabled or disabled through the other bits of the interrupt enable registers. The EA bit is always cleared to '0' jumping to an interrupt service vector and set to '1' executing the [RETI] instruction. The A96T430 supports a four-level priority scheme. Each maskable interrupt is individually assigned to one of four priority levels according to IP and IP1.

Default interrupt mode is level-trigger mode basically, but if needed, it is possible to change to edge-trigger mode.

Figure 7 shows the Interrupt Group Priority Level that is available for sharing interrupt priority. Priority of a group is set by two bits of interrupt priority registers (one bit from IP, another one from IP1). Interrupt service routine serves higher priority interrupt first. If two requests of different priority levels are received simultaneously, the request of higher priority level is served prior to the lower one.

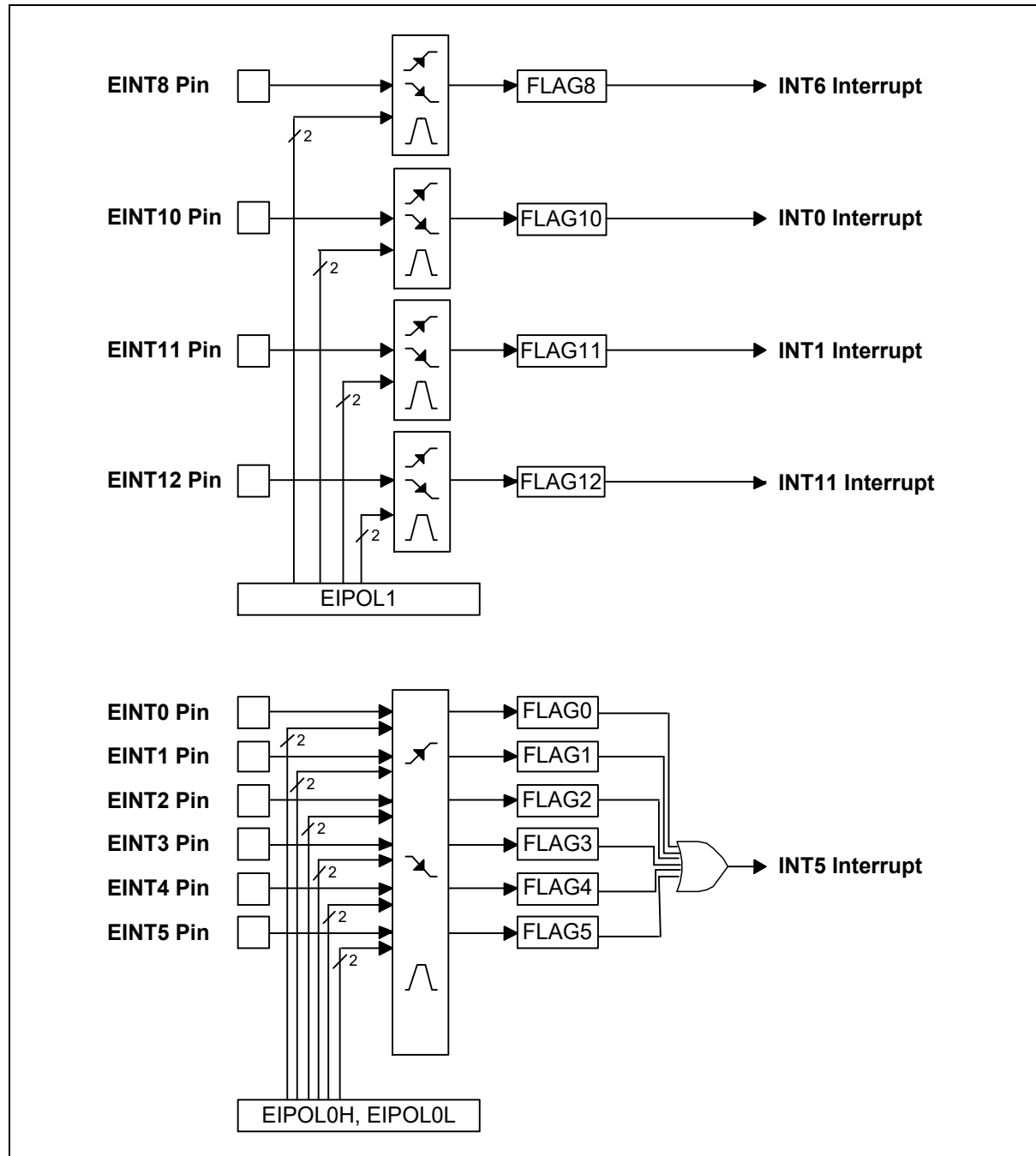
Figure 7. Interrupt Group Priority Level

Interrupt Group	Highest Lowest				
	→				
0 (bit-0)	Interrupt 0	Interrupt 6	Interrupt 12	Interrupt 18	Highest ↓ Lowest
1 (bit-1)	Interrupt 1	Interrupt 7	Interrupt 13	Interrupt 19	
2 (bit-2)	Interrupt 2	Interrupt 8	Interrupt 14	Interrupt 20	
3 (bit-3)	Interrupt 3	Interrupt 9	Interrupt 15	Interrupt 21	
4 (bit-4)	Interrupt 4	Interrupt 10	Interrupt 16	Interrupt 22	
5 (bit-5)	Interrupt 5	Interrupt 11	Interrupt 17	Interrupt 23	

2.4.4.1 External Interrupt

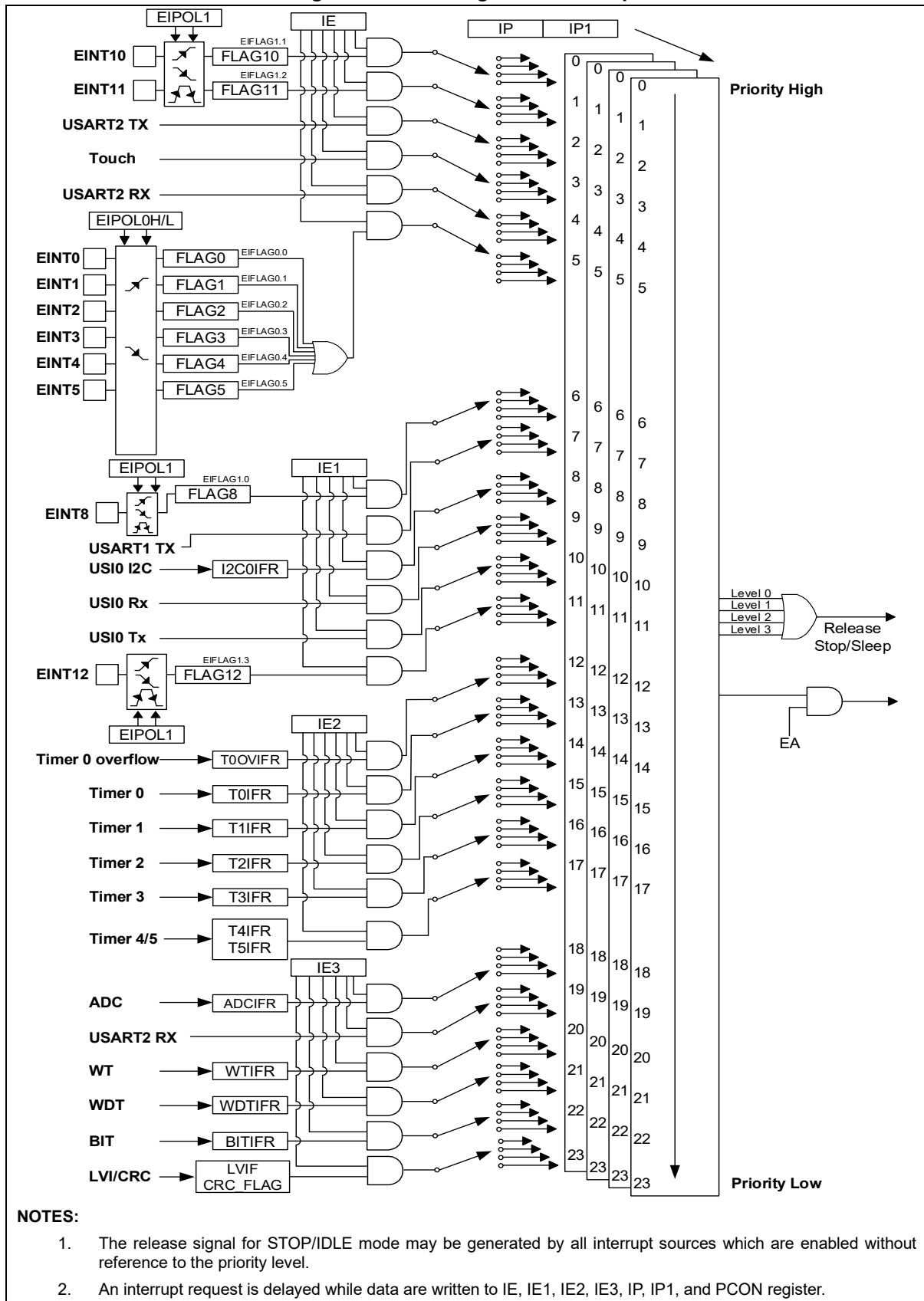
External interrupt on INT0, INT1, INT5, INT6 and INT11 receive various interrupt requests depending on the external interrupt polarity 0 high/low register (EIPOL0H/L) and external interrupt polarity 1 register (EIPOL1) as shown in Figure 8. Also, each external interrupt source has enable/disable bits. The external interrupt flag 0 register (EIFLAG0) and external interrupt flag 1 register 1 (EIFLAG1) provides the status of external interrupts.

Figure 8. External Interrupt Description



2.4.4.2 Block Diagram

Figure 9. Block Diagram of Interrupt



2.4.4.3 Interrupt Vector Table

The interrupt controller supports 23 interrupt sources as shown in Table 9.

When the interrupt is served, Long Call instruction (LCALL) is executed and program counter jumps to the vector address. All interrupt requests have their own priority order.

Table 9. Interrupt Vector Address Table

Interrupt Source	Symbol	Interrupt Enable Bit	Polarity	Mask	Vector Address
Hardware Reset	RESETB	-	0	Non-Maskable	0000H
External Interrupt 10	INT0	IE.0	1	Maskable	0003H
External Interrupt 11	INT1	IE.1	2	Maskable	000BH
USART2 TX Interrupt	INT2	IE.2	3	Maskable	0013H
Touch Interrupt	INT3	IE.3	4	Maskable	001BH
USART2 RX Interrupt	INT4	IE.4	5	Maskable	0023H
External Interrupt 0 – 5	INT5	IE.5	6	Maskable	002BH
External Interrupt 8	INT6	IE1.0	7	Maskable	0033H
USART1 TX Interrupt	INT7	IE1.1	8	Maskable	003BH
USI0 I2C Interrupt	INT8	IE1.2	9	Maskable	0043H
USI0 RX Interrupt	INT9	IE1.3	10	Maskable	004BH
USI0 TX Interrupt	INT10	IE1.4	11	Maskable	0053H
External Interrupt 12	INT11	IE1.5	12	Maskable	005BH
T0 Overflow Interrupt	INT12	IE2.0	13	Maskable	0063H
T0 Match Interrupt	INT13	IE2.1	14	Maskable	006BH
T1 Match Interrupt	INT14	IE2.2	15	Maskable	0073H
T2 Match Interrupt	INT15	IE2.3	16	Maskable	007BH
T3 Match Interrupt	INT16	IE2.4	17	Maskable	0083H
T4/T5 Match Interrupt	INT17	IE2.5	18	Maskable	008BH
ADC Interrupt	INT18	IE3.0	19	Maskable	0093H
USART1 RX Interrupt	INT19	IE3.1	20	Maskable	009BH
WT Interrupt	INT20	IE3.2	21	Maskable	00A3H
WDT Interrupt	INT21	IE3.3	22	Maskable	00ABH
BIT Interrupt	INT22	IE3.4	23	Maskable	00B3H
LVI Interrupt	INT23	IE3.5	24	Maskable	00BBH

For maskable interrupt execution, EA bit must set '1' and specific interrupt must be enabled by writing '1' to associated bit in the IEx. If an interrupt request is received, the specific interrupt request flag is set to '1'. And it remains '1' until CPU accepts interrupt. If the interrupt is served, the interrupt request flag will be cleared automatically.

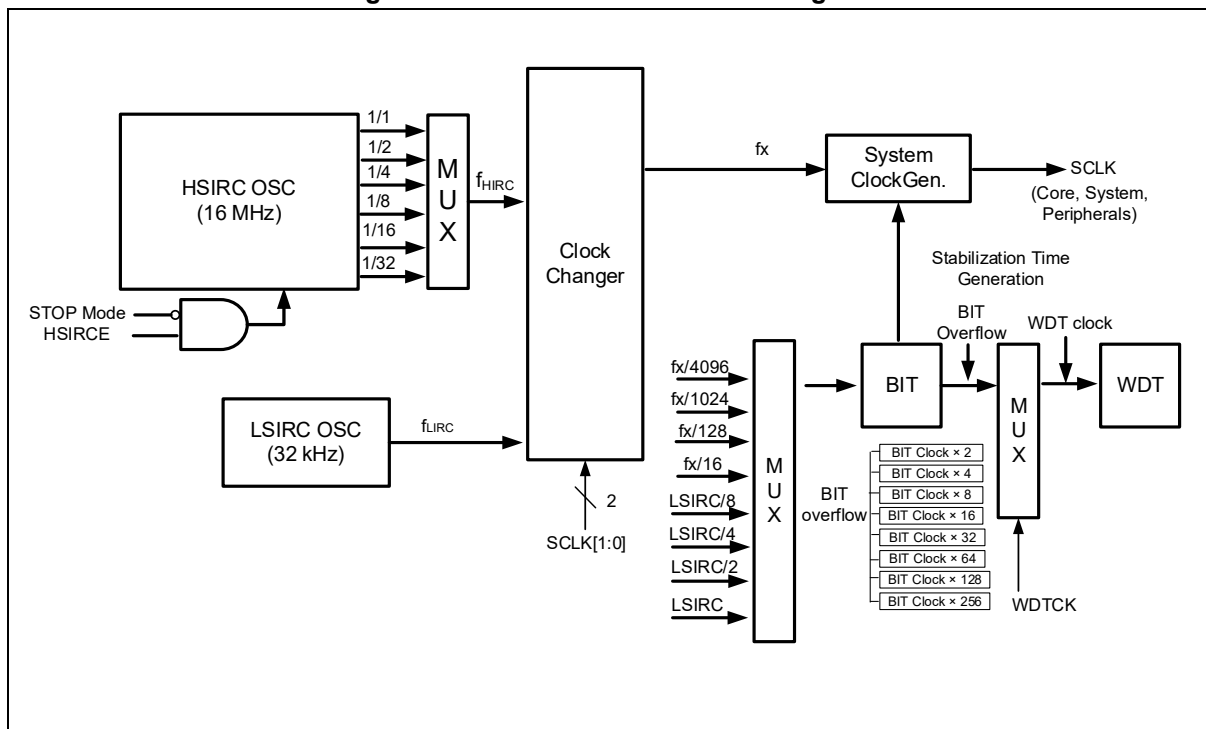
2.4.5 Clock Generator

As shown in Figure 10, the clock generator produces basic clock pulses which provide the system clock to be supplied to the CPU and the peripheral hardware. To stabilize the system internally, it is used with a 32 kHz Low-Internal-RC oscillator on POR.

- Calibrated High Internal RC Oscillator ($f_{\text{HSIRC}} = 16 \text{ MHz}$)
 - HSIRC OSC (16 MHz, Default system clock)
 - HSIRC OSC/2 (8 MHz)
 - HSIRC OSC/4 (4 MHz)
 - HSIRC OSC/8 (2 MHz)
 - HSIRC OSC/16 (1 MHz)
 - HSIRC OSC/32 (0.5 MHz)
- Internal LSIRC Oscillator (32 kHz)

2.4.5.1 Block Diagram

Figure 10. Clock Generator Block Diagram



2.4.6 BIT

The A96T430 has one 8-bit BIT (Basic Interval Timer) that is free-run and never stops. In addition, the basic interval timer generates the time base for Watchdog Timer counting. It also provides a basic interval timer interrupt (BITIFR).

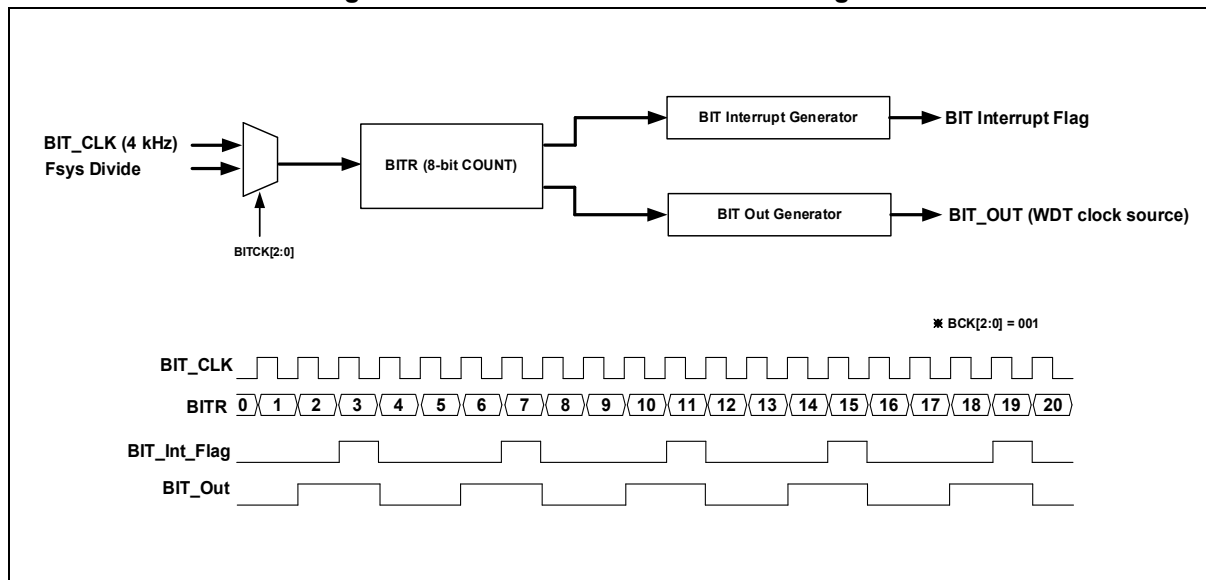
Figure 11 shows a block diagram of the BIT.

The A96T430's BIT provides the following functions:

- During Power-On, BIT gives a stable clock generation time.
- On exiting STOP mode, BIT gives a stable clock generation time.
- As timer function, timer interrupt occurrences.

2.4.6.1 Block Diagram

Figure 11. Basic Interval Timer Block Diagram



2.4.7 WDT

WDT (Watchdog Timer) rapidly detects the CPU malfunction such as endless looping caused by noise or something like that and resumes the CPU to the normal state. Watchdog Timer signal for malfunction detection can be used as either a CPU reset or an interrupt request.

When the WDT is not being used for malfunction detection, it can be used as a timer to generate an interrupt at fixed intervals. It is possible to use free running 8-bit timer mode (WDTRSON=0) or watchdog timer mode (WDTRSON=1) by setting WDTCSR[6] bit. If WDTCSR[5] is set to '1', the WDT counter value is cleared and counts up. After 1 machine cycle, this bit is cleared to '0' automatically.

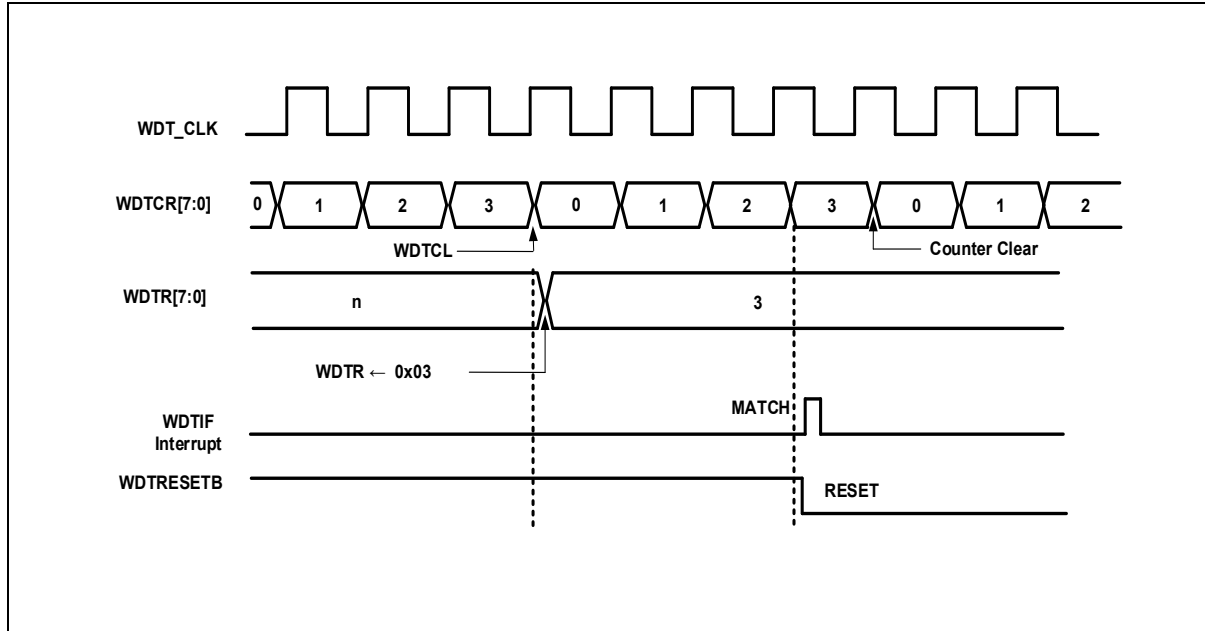
The WDT consists of an 8-bit binary counter and a Watchdog Timer data register. When the value of the 8-bit binary counter is equal to the 8 bits of WDTCNT, an interrupt request flag is generated. This can be used as a Watchdog Timer interrupt or a reset signal of CPU in accordance with a bit WDTRSON.

The input clock source of the WDT is BIT overflow. An interval between Watchdog Timer interrupts is decided by BIT overflow period and WDTDR set value. The equation can be described as the following:

$$\text{WDT Interrupt Interval} = (\text{BIT Interrupt Interval}) \times (\text{WDTDR Value} + 1)$$

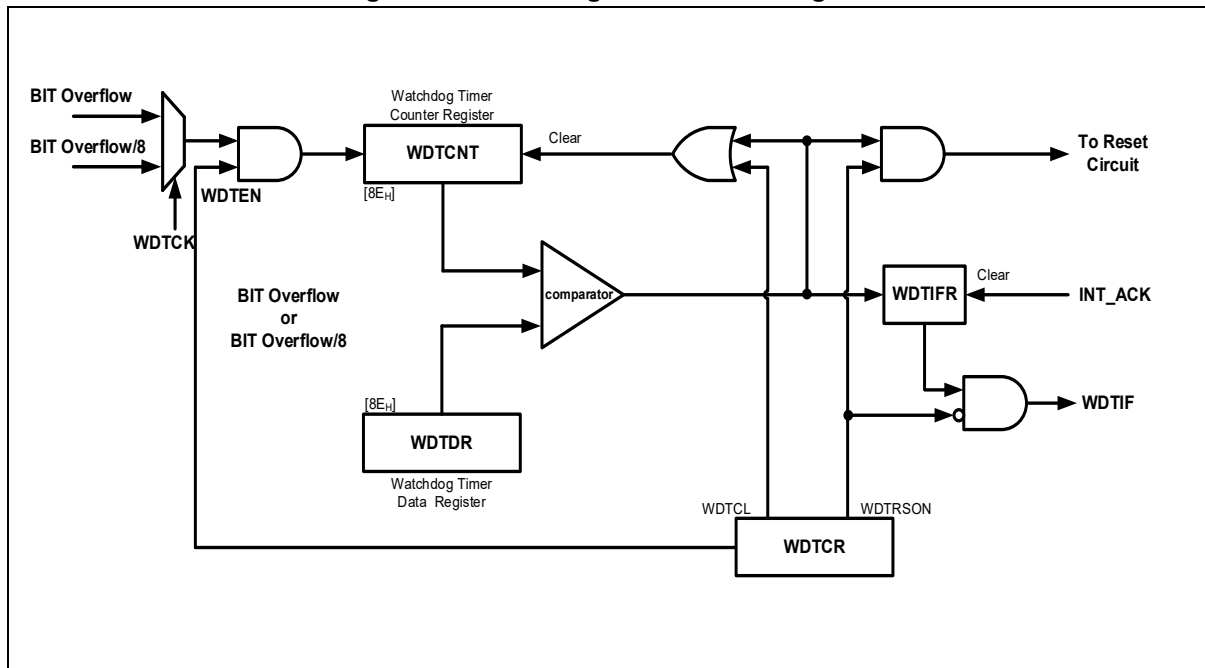
2.4.7.1 WDT Interrupt Timing Waveform

Figure 12. Watchdog Timer Interrupt Timing Waveform



2.4.7.2 Block Diagram

Figure 13. Watchdog Timer Block Diagram



2.4.8 WT

WT (Watch Timer) has the function for Real Time Clock (RTC) operation. It is generally used for RTC design.

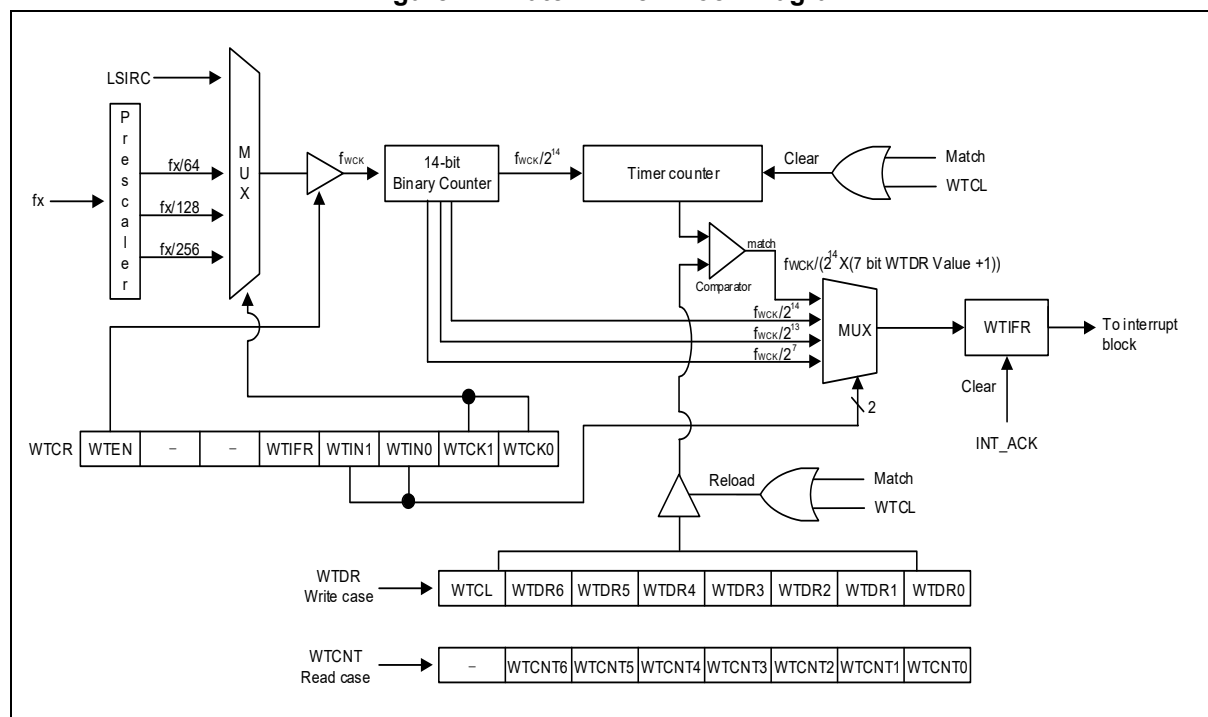
The internal structure of the Watch Timer consists of the clock source select circuit, timer counter circuit, output select circuit and Watch Timer control register. To operate the Watch Timer, determine the input clock source, output interval, and set WTEN to '1' in Watch Timer control register (WTCR). It is able to be executed simultaneously or individually.

To stop or reset the Watch Timer, clear the WTEN bit in WTCR register. Even if CPU is STOP mode, LSI clock can be so alive that the Watch Timer can continue the operation.

The Watch Timer circuits may be composed of 21-bit counters which contain low 14-bit with binary counter and high 7-bit counter to raise resolution. In WTDR, it can control the Watch Timer clear and set interval value at write time, and it can read 7-bit the Watch Timer counter value at read time.

2.4.8.1 Block Diagram

Figure 14. Watch Timer Block Diagram



2.4.9 Timer 0/1/2/3/4/5

2.4.9.1 Timer 0

The 8-bit timer 0 consists of a multiplexer, a timer 0 counter register, a timer 0 data register, a timer 0 capture data register and a timer 0 control register (T0CNT, T0DR, T0CDR, T0CR).

Timer 0 operates in one of three modes described in the following:

- 8-bit timer/counter mode
- 8-bit PWM output mode
- 8-bit capture mode

Timer/counter 0 can be clocked by an internal or an external clock source (EC0). The clock source is selected by clock selection logic which is controlled by clock selection bits T0CK[2:0].

- TIMER0 clock source: $f_x/2$, 4, 8, 32, 128, 512, 2048 and EC0

In capture mode, data is captured into input capture data register (T0CDR) by EINT1. In timer/counter mode, whenever counter value is equal to T0DR, T0O port toggles. In addition, timer 0 outputs PWM waveform through PWM0O port in the PWM mode.

Table 10. Timer 0 Operating Modes

T0EN	T0MS[1:0]	T0CK[2:0]	Timer 0
1	00	XXX	8-bit Timer/Counter Mode
1	01	XXX	8-bit PWM Mode
1	1X	XXX	8-bit Capture Mode

8-bit Timer/Counter Mode

As shown in Figure 15, 8-bit timer/counter mode is selected by control register.

8-bit timer has counter and data registers. The counter register is increased by internal or external clock input. Timer 0 can use the input clock with one of 2, 4, 8, 32, 128, 512 and 2048 prescale division rates (T0CK[2:0]). When both values of T0CNT and T0DR are identical to each other in timer 0, a match signal is generated, and the interrupt of Timer 0 occurs. T0CNT value is automatically cleared by the match signal and can be cleared by software (T0CC) too.

Figure 15. 8-bit Timer/Counter Mode for Timer 0

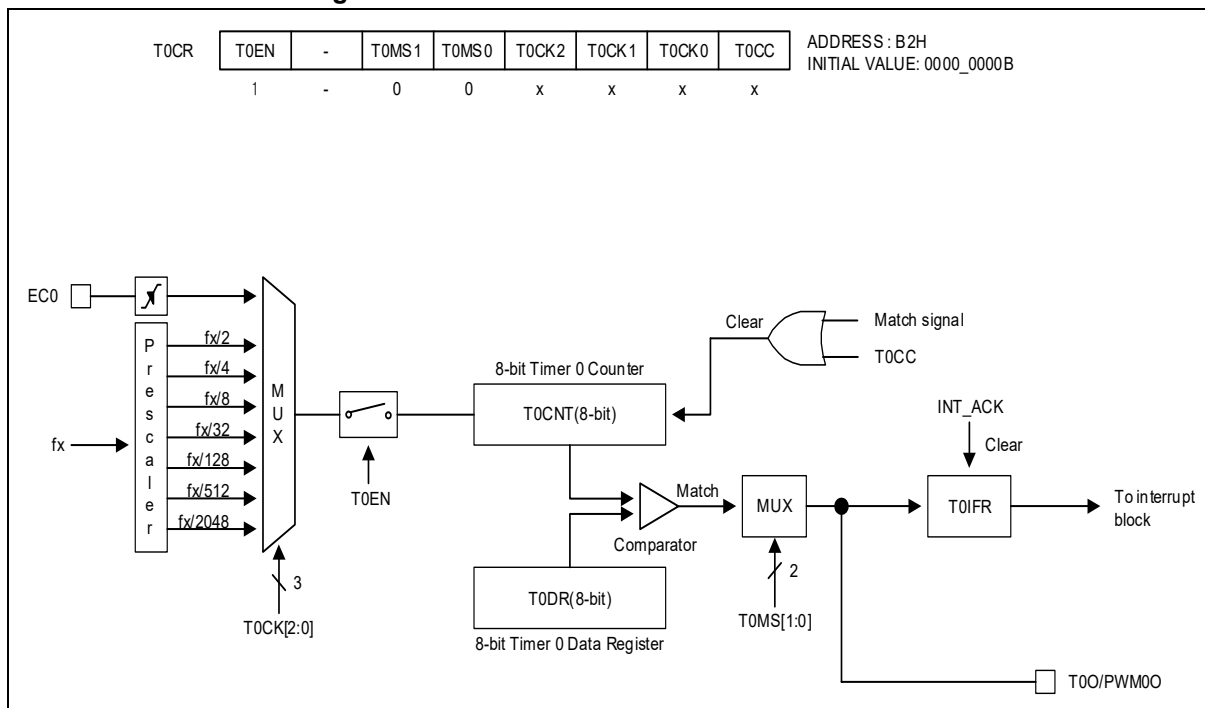
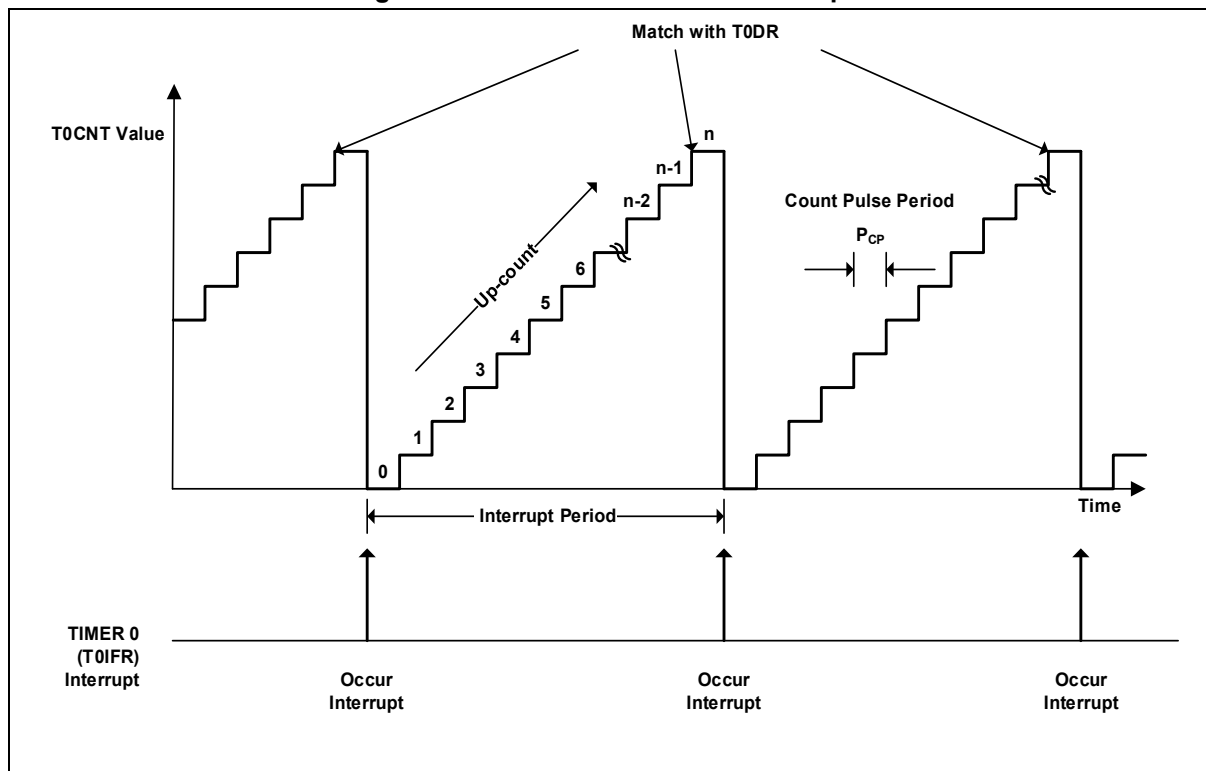


Figure 16. 8-bit Timer/Counter 0 Example



8-bit PWM Mode

Timer 0 has a high-speed PWM (Pulse Width Modulation) function. In PWM mode, T0O/PWM0O pin outputs up to 8-bit resolution PWM output. This pin should be configured as a PWM output by setting the T0O/PWM0O function by P0FSRL[7:6] bits.

In 8-bit timer/counter mode, a match signal is generated when the counter value is identical to the value of T0DR. When values of T0CNT and T0DR are identical to each other in timer 0, a match signal is generated and the interrupt of timer 0 occurs.

In PWM mode, the match signal does not clear the counter. Instead, it runs continuously, overflowing at “FFH”. Then the counter continues incrementing from “00H”. The timer 0 overflow interrupt is generated whenever a counter overflow occurs. T0CNT value is cleared by software (T0CC) bit.

Figure 17. 8-bit-PWM Mode for Timer 0

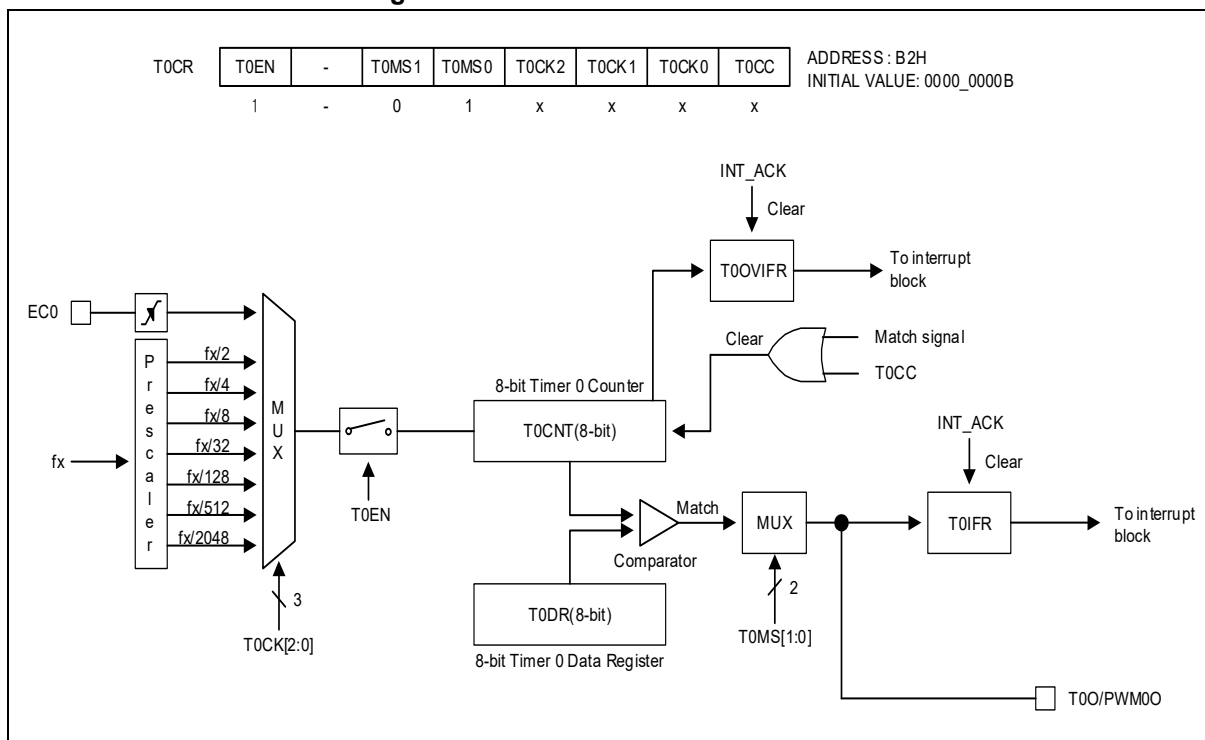
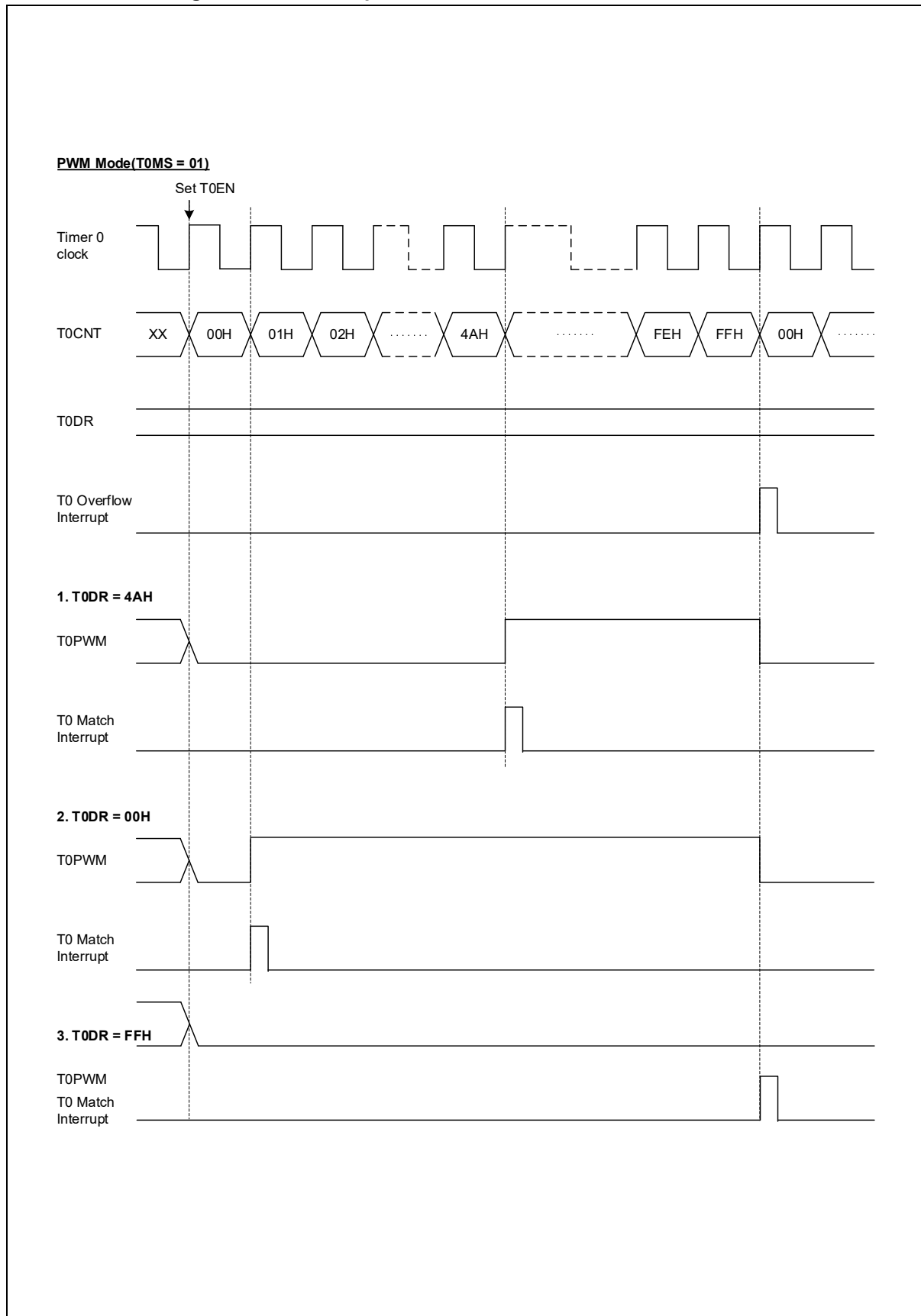


Figure 18. PWM Output Waveforms in PWM Mode for Timer 0



8-bit Capture Mode

Timer 0 capture mode is set by configuring T0MS[1:0] as '1x'. Clock source can use the internal/external clock. Basically, it has the same function as the 8-bit timer/counter mode has, and the interrupt occurs when T0CNT equals to T0DR. T0CNT value is automatically cleared by match signal, and it can be also cleared by software (T0CC).

This timer interrupt in capture mode is very useful when the pulse width of captured signal is wider than the maximum period of timer.

The capture result is loaded into T0CDR. In the timer 0 capture mode, timer 0 output (T0O) waveform is not available.

According to EIPOL1 registers setting, the external interrupt EINT1 function is chosen. Of course, the EINT1 pin must be set to an input port.

T0CDR and T0DR are at the same address. In the capture mode, reading operation reads T0CDR, not T0DR and writing operation will update T0DR.

Figure 19. 8-bit Capture Mode for Timer 0

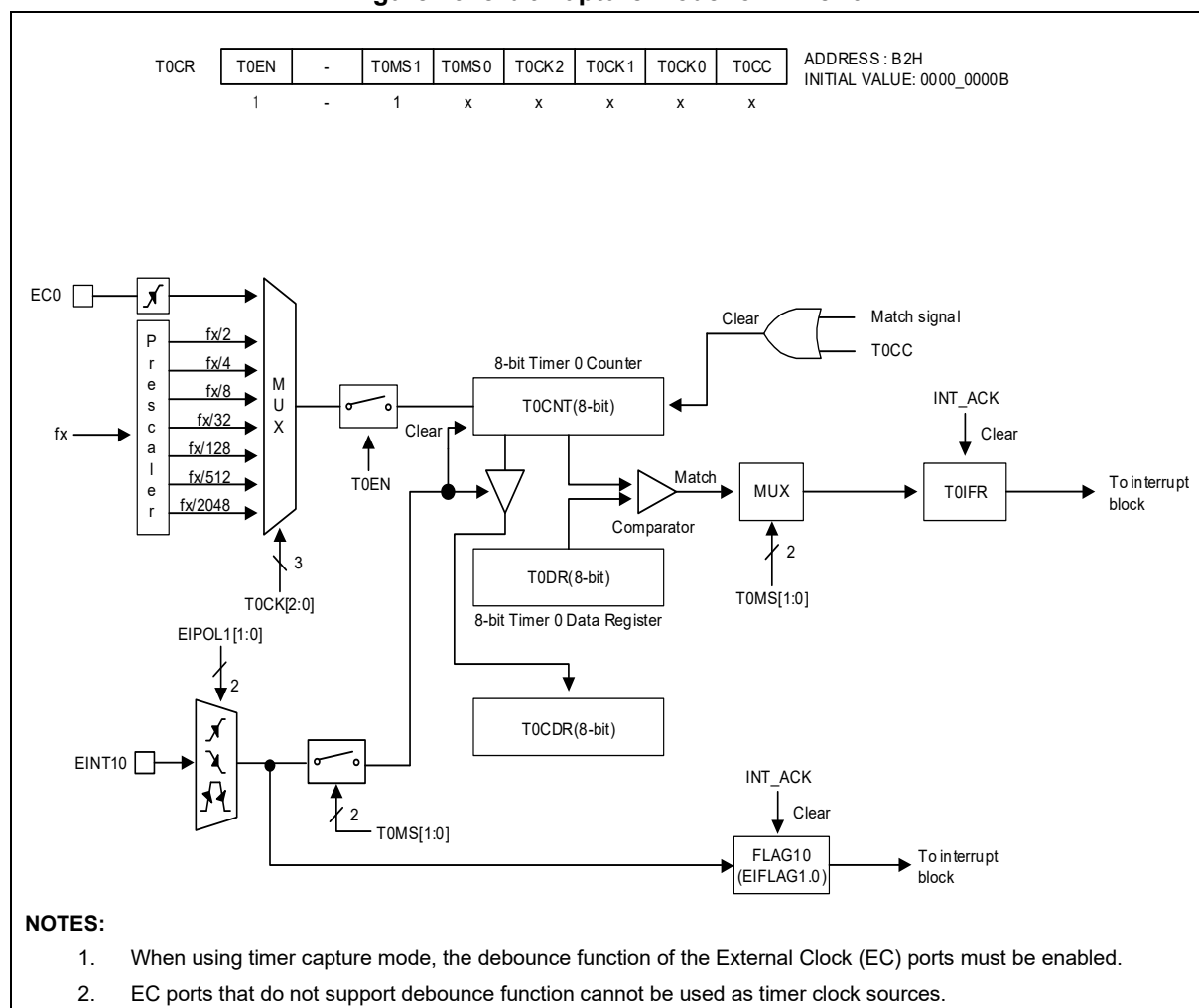


Figure 20. Input Capture Mode Operation for Timer 0

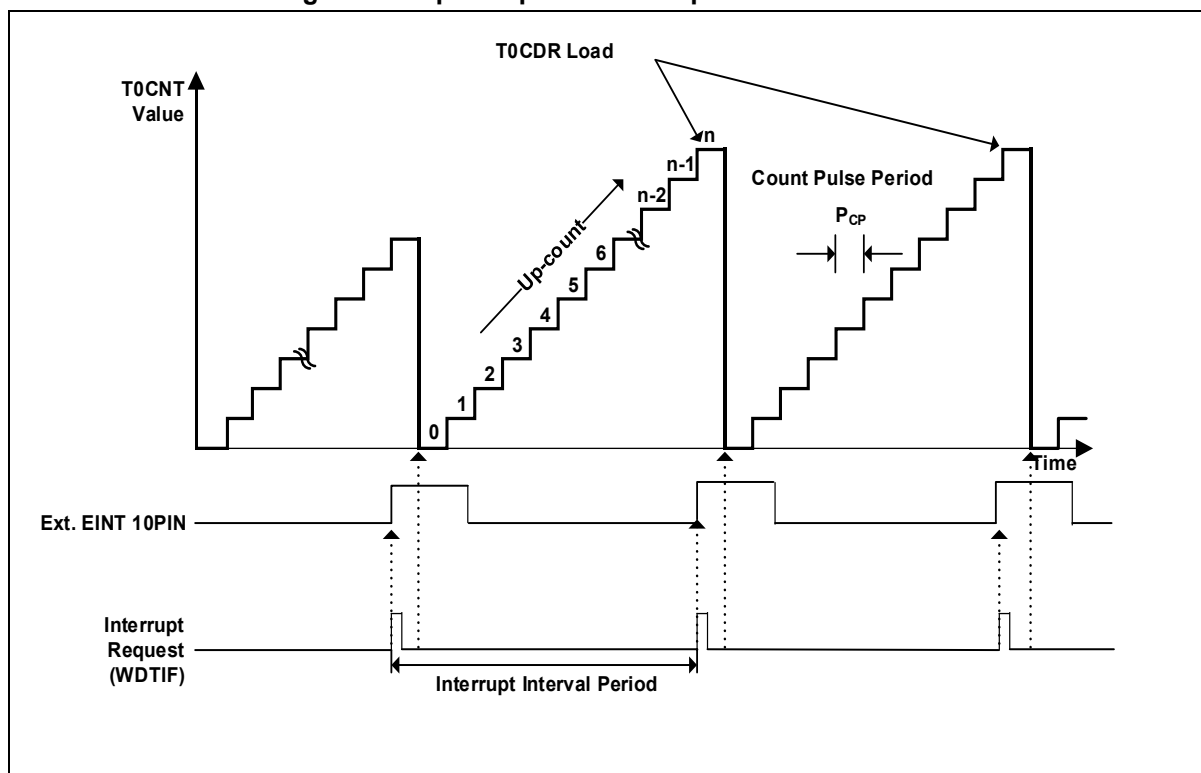
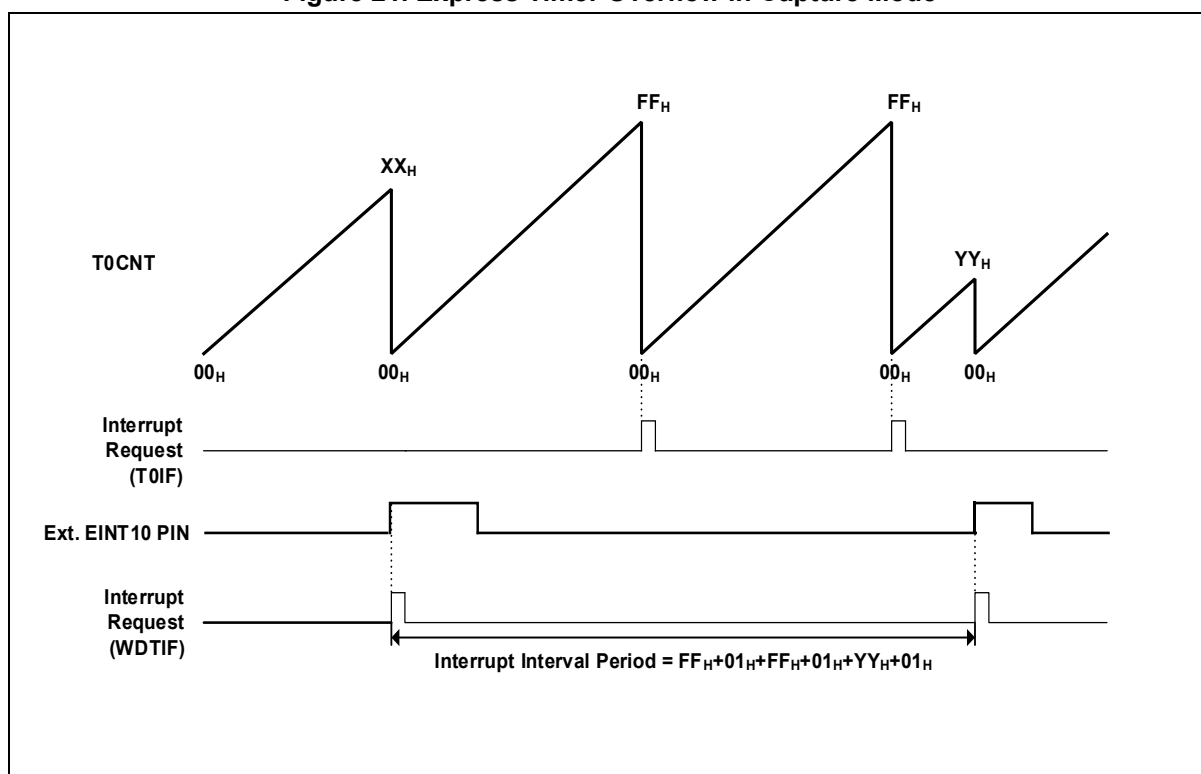
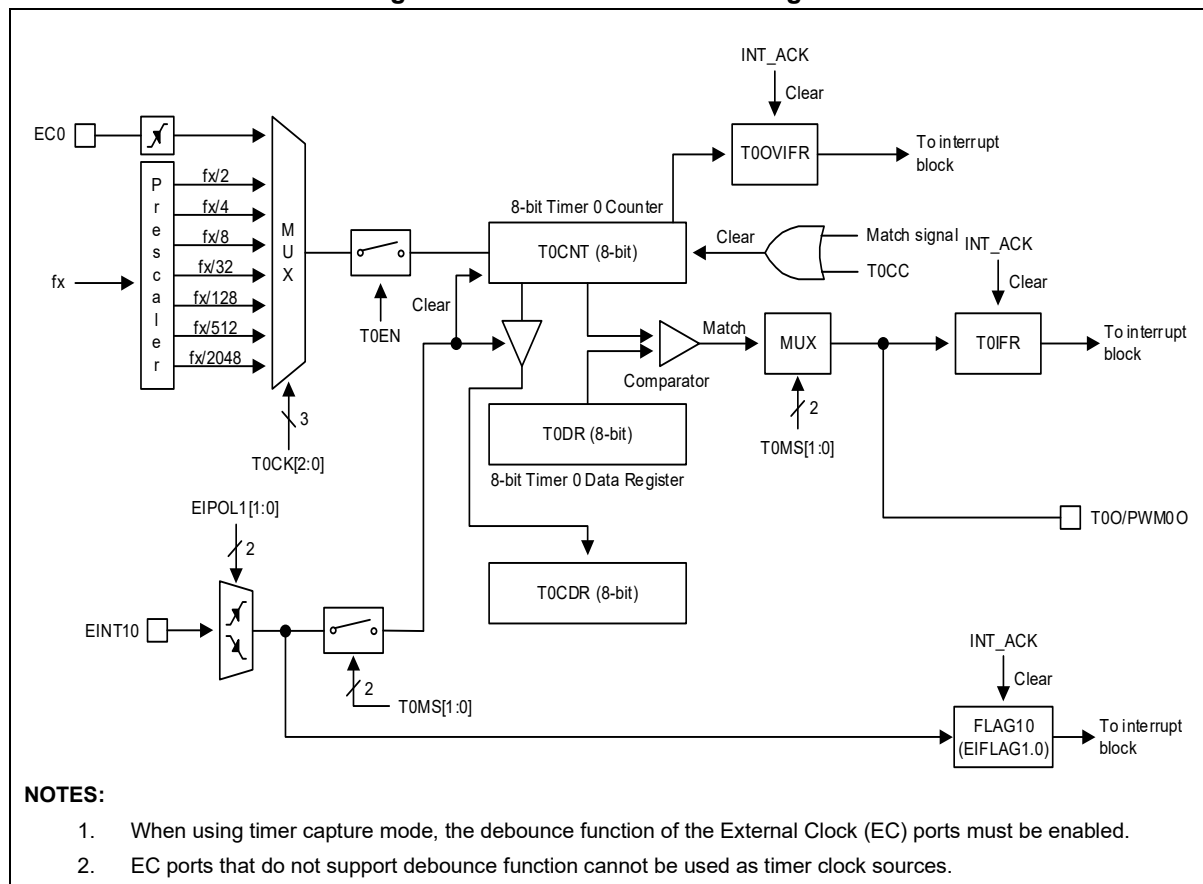


Figure 21. Express Timer Overflow in Capture Mode



Block Diagram

Figure 22. 8-bit Timer 0 Block Diagram



2.4.9.2 Timer 1

The 16-bit timer 1 consists of multiplexer, timer 1 A data register high/low, timer 1 B data register high/low and timer 1 control register high/low (T1ADRH, T1ADRL, T1BDRH, T1BDRL, T1CRH, T1CRL).

Timer 1 operates in one of the following modes:

- 16-bit timer/counter mode
- 16-bit capture mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

The timer/counter 1 uses an internal clock or an external clock (EC1) as an input clock source. The clock sources are described below, and one is selected by clock selection logic which is controlled by clock selection bits (T1CK[2:0]).

- TIMER 1 clock source: fx/1, 2, 4, 8, 64, 512, 2048 and EC1

In capture mode, the data is captured into input capture data register (T1BDRH/T1BDRL) by EINT2. Timer 1 results in the comparison between counter and data register through T1O port in timer/counter mode. In addition, Timer 1 outputs PWM waveform through PWM1O pin in the PPG mode.

Table 11. Timer 1 Operating Modes

T1EN	P1FSRL[1:0]	T1MS[1:0]	T1CK[2:0]	Timer 1
1	11	00	XXX	16-bit Timer/Counter Mode
1	00	01	XXX	16-bit Capture Mode
1	11	10	XXX	16-bit PPG Mode (one-shot mode)
1	11	11	XXX	16-bit PPG Mode (repeat mode)

16-bit Timer/Counter Mode

16-bit timer/counter mode is selected by control registers, and the 16-bit timer/counter has counter registers and data registers as shown in Figure 23. The counter register is increased by internal or external clock input.

Timer 1 can use the input clock with one of 1, 2, 4, 8, 64, 512 and 2048 prescaler division rates (T1CK[2:0]). When the value of T1CNTH, T1CNTL and the value of T1ADRH, T1ADRL are identical to each other in Timer 1, a match signal is generated and the interrupt of Timer1 occurs. The T1CNTH, T1CNTL value is automatically cleared by the match signal. It can be cleared by software (T1CC) too.

The external clock (EC1) counts up the timer at the rising edge. If the EC1 is selected as a clock source by T1CK[2:0], EC1 port should be set to the input port by P14IO bit.

Figure 23. 16-bit Timer/Counter Mode for Timer 1

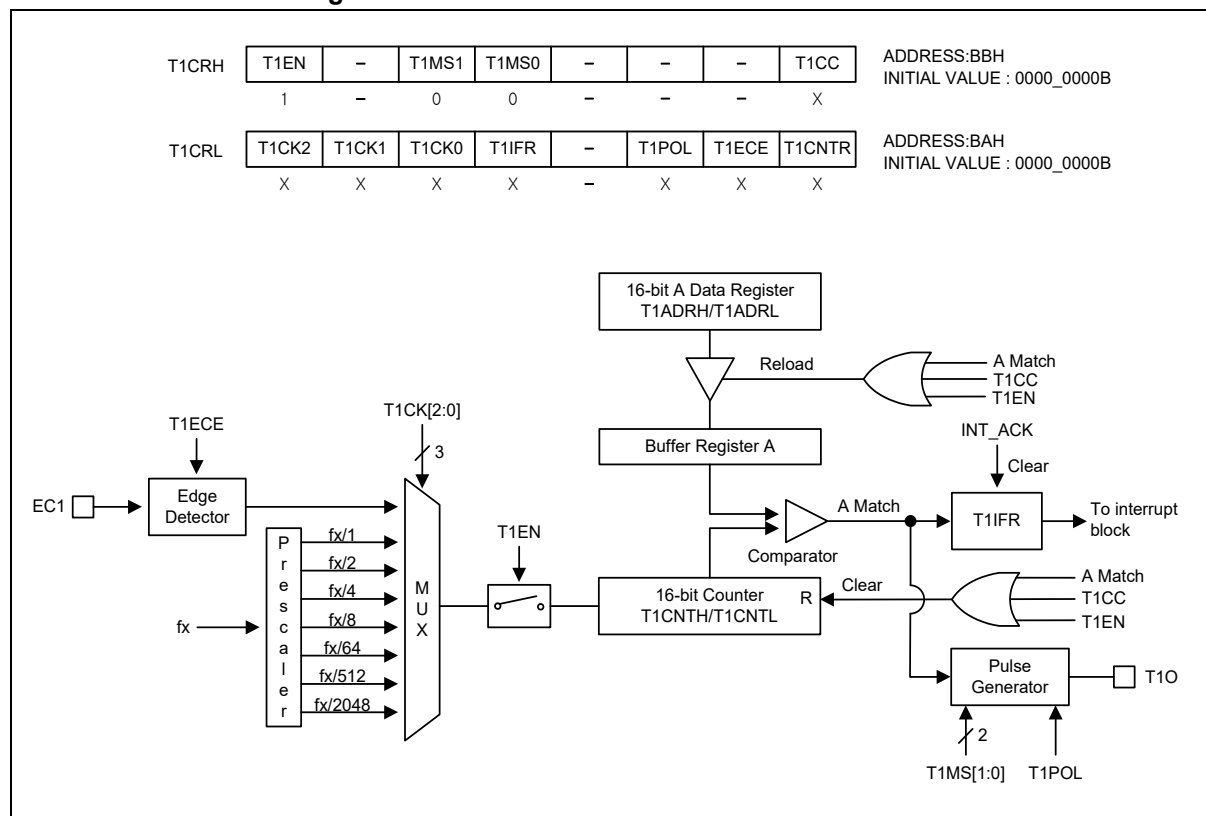
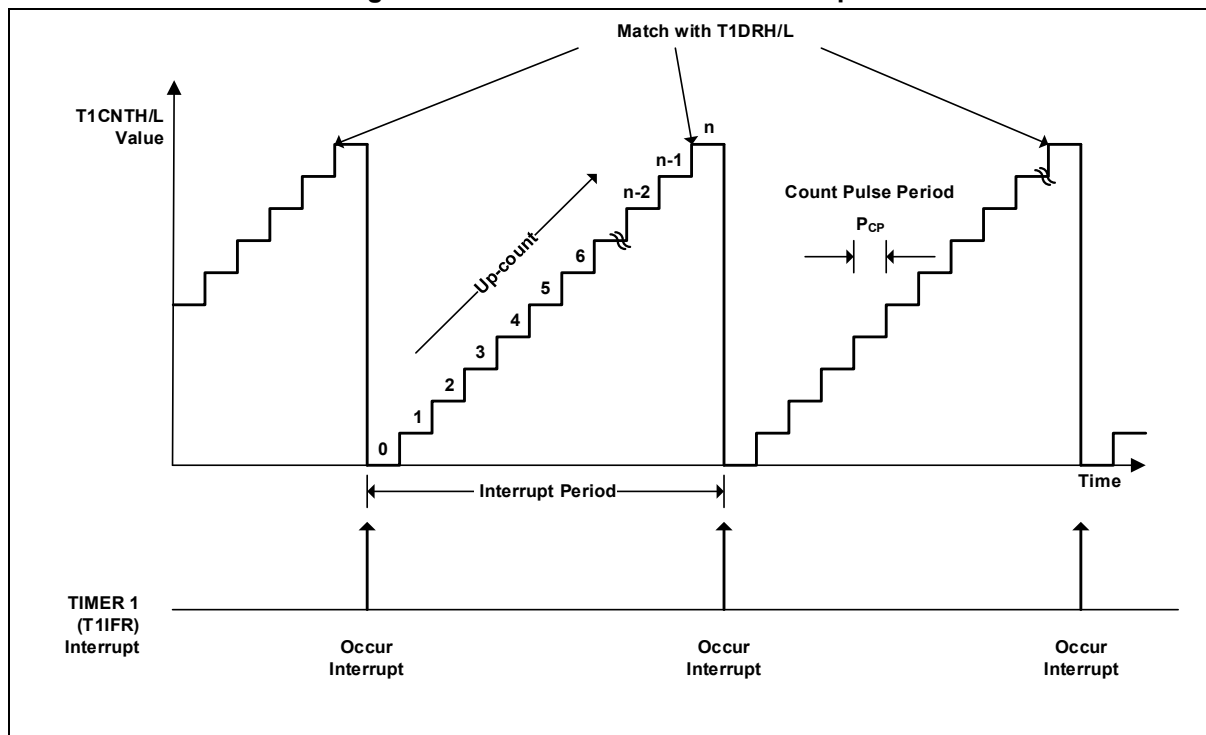


Figure 24. 16-bit Timer/Counter 1 Example



16-bit Capture Mode

It uses an internal/external clock as a clock source. Basically, the 16-bit timer 1 capture mode has the same function as the 16-bit timer/counter mode, and the interrupt occurs when T1CNTH/T1CNTL is equal to T1ADRH/T1ADRL. The T1CNTH, T1CNTL values are automatically cleared by a match signal. It can be cleared by software (T1CC) too.

A timer interrupt in capture mode is very useful when the pulse width of captured signal is wider than the maximum period of timer. Capture result is loaded into T1BDRH/T1BDRL.

According to EIPOL1 registers setting, the external interrupt EINT2 function is selected. EINT2 pin must be set as an input port.

Figure 25. 16-bit Capture Mode for Timer 1

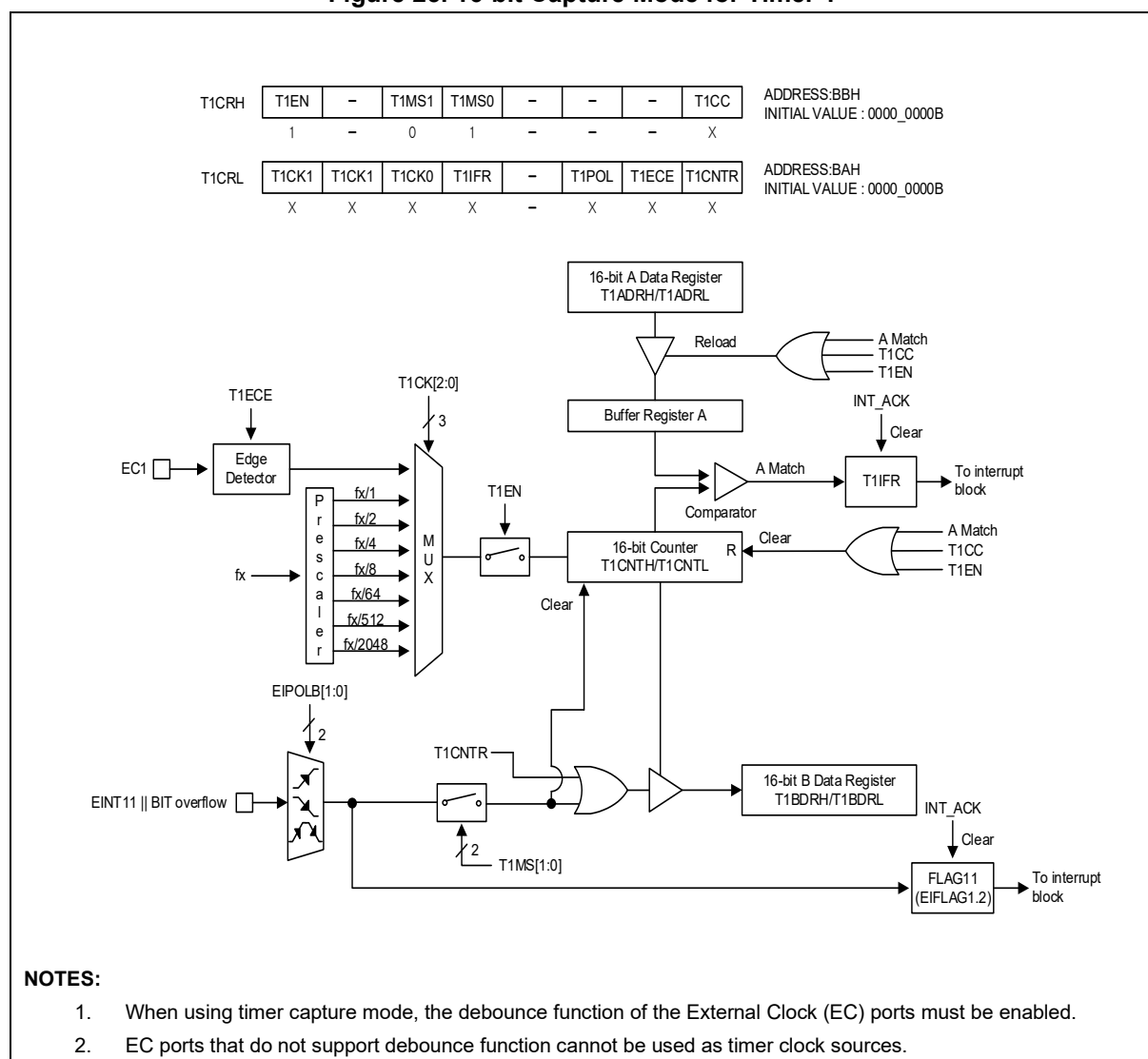


Figure 26. Input Capture Mode Operation for Timer 1

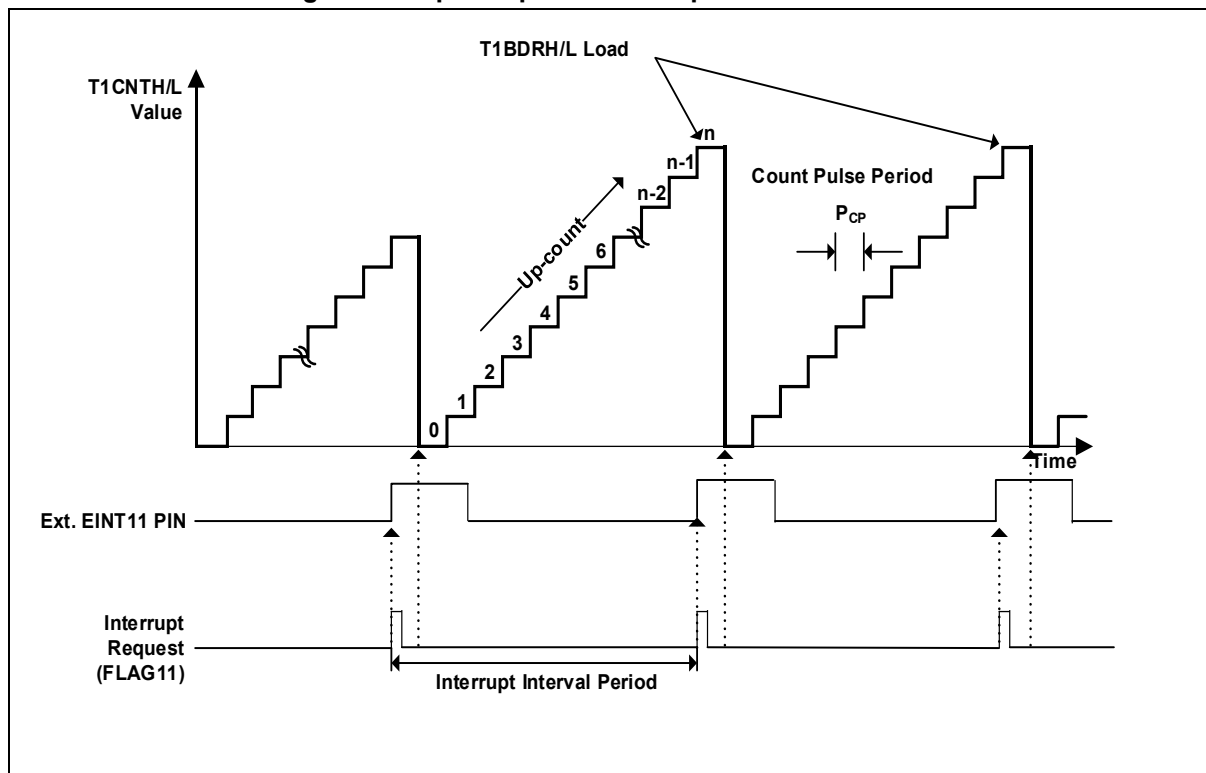
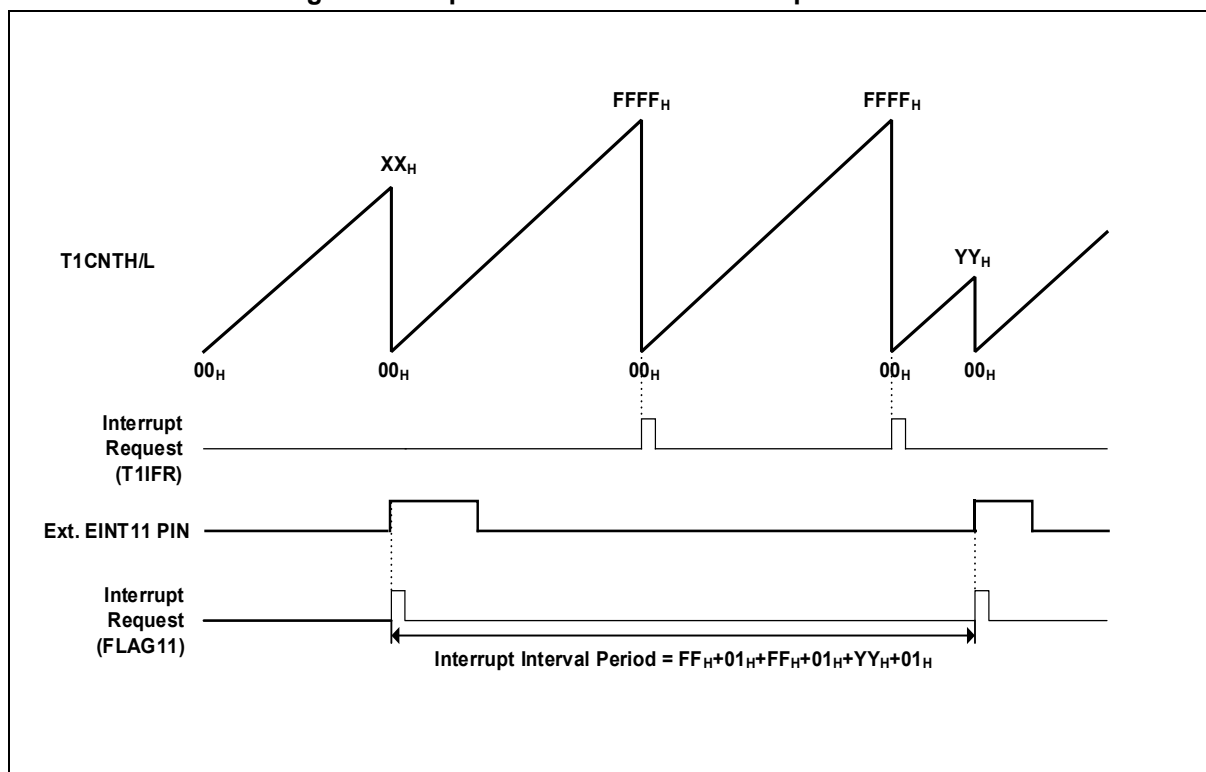


Figure 27. Express Timer Overflow in Capture Mode

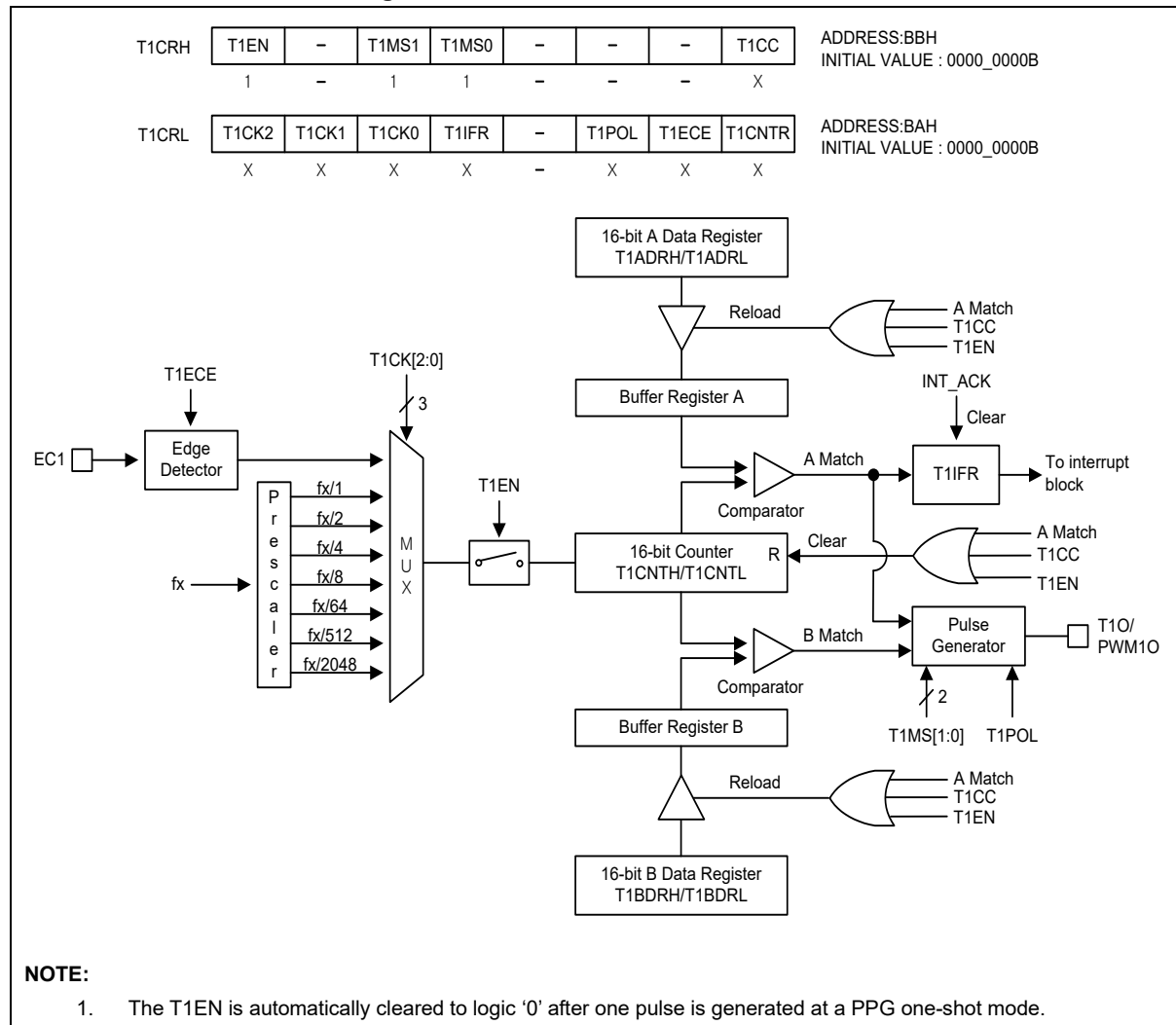


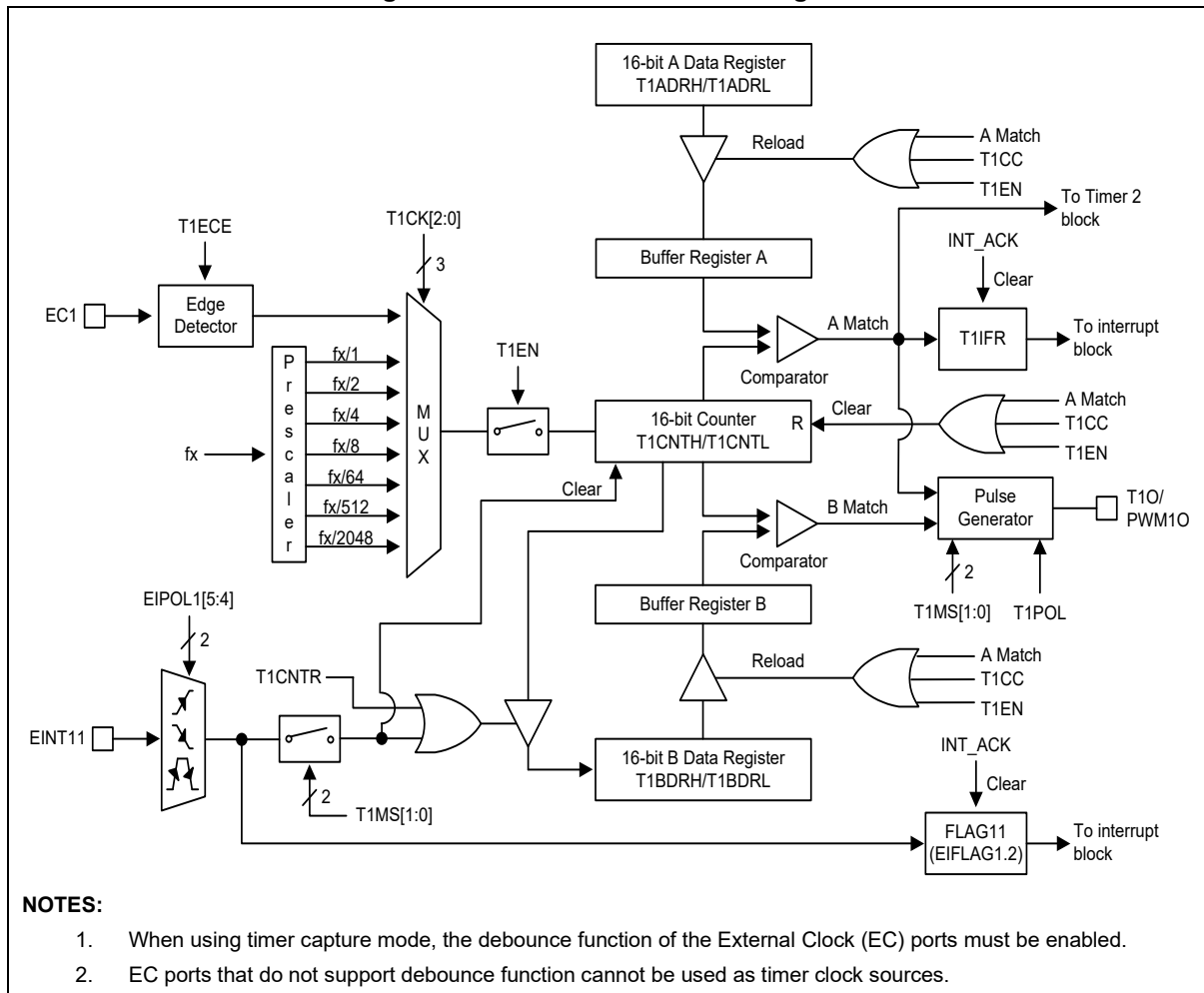
16-bit PPG Mode

TIMER 1 has a PPG (Programmable Pulse Generation) function. In PPG mode, T1O/PWM1O pin outputs up to 16-bit resolution PWM output. For this function, T1O/PWM1O pin must be configured as a PWM output by setting P0FSRL[5:4] to '10'.

The period of the PWM output is determined by T1ADRH/T1ADRL, and duty of the PWM output is determined by T1BDRH/T1BDRL.

Figure 28. 16-bit PPG Mode for Timer 1



Block Diagram**Figure 29. 16-bit Timer 1 Block Diagram**

2.4.9.3 Timer 2

The 16-bit timer 2 consists of a multiplexer, timer 2 A data high/low register, timer 2 B data high/low register and timer 2 control high/low register (T2ADRH, T2ADRL, T2BDRH, T2BDRL, T2CRH, and T2CRL).

Timer 2 operates in one of the following modes:

- 16-bit timer/counter mode
- 16-bit capture mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

The timer/counter 2 can be a divided clock of a system clock which is selected from prescaler output and T1 A Match (timer 1 A match signal). The clock source is selected by a clock selection logic, controlled by clock selection bits (T2CK[2:0]).

- TIMER 2 clock source: fx/1, fx/2, fx/4, fx/8, fx/32, fx/128, fx/512 and T1 A Match

In capture mode, data is captured into input capture data registers (T2BDRH/T2BDRL) by EINT3. In timer/counter mode, whenever counter value is equal to T2ADRH/L, T2O port toggles. In addition, the timer 2 outputs PWM waveform to PWM2O port in the PPG mode.

Table 12. Timer 2 Operating Modes

T2EN	P1FSRL[5:4]	T2MS[1:0]	T2CK[2:0]	Timer 2
1	11	00	XXX	16-bit Timer/Counter Mode
1	00	01	XXX	16-bit Capture Mode
1	11	10	XXX	16-bit PPG Mode (one-shot mode)
1	11	11	XXX	16-bit PPG Mode (repeat mode)

16-bit Timer/Counter Mode

16-bit timer/counter mode is selected by control registers, and the 16-bit timer/counter has counter registers and data registers as shown in Figure 30. The counter register is increased by internal or timer 1 A match clock input.

Timer 2 can use the input clock with one of 1, 2, 4, 8, 32, 128, 512 and T1 A Match prescaler division rates (T2CK[2:0]). When the values of T2CNTH/T2CNTL and T2ADRH/T2ADRL are identical to each other in timer 2, a match signal is generated, and the interrupt of Timer 2 occurs. The T2CNTH/T2CNTL values are automatically cleared by the match signal. It can be cleared by software (T2CC) too.

Figure 30. 16-bit Timer/Counter Mode for Timer 2

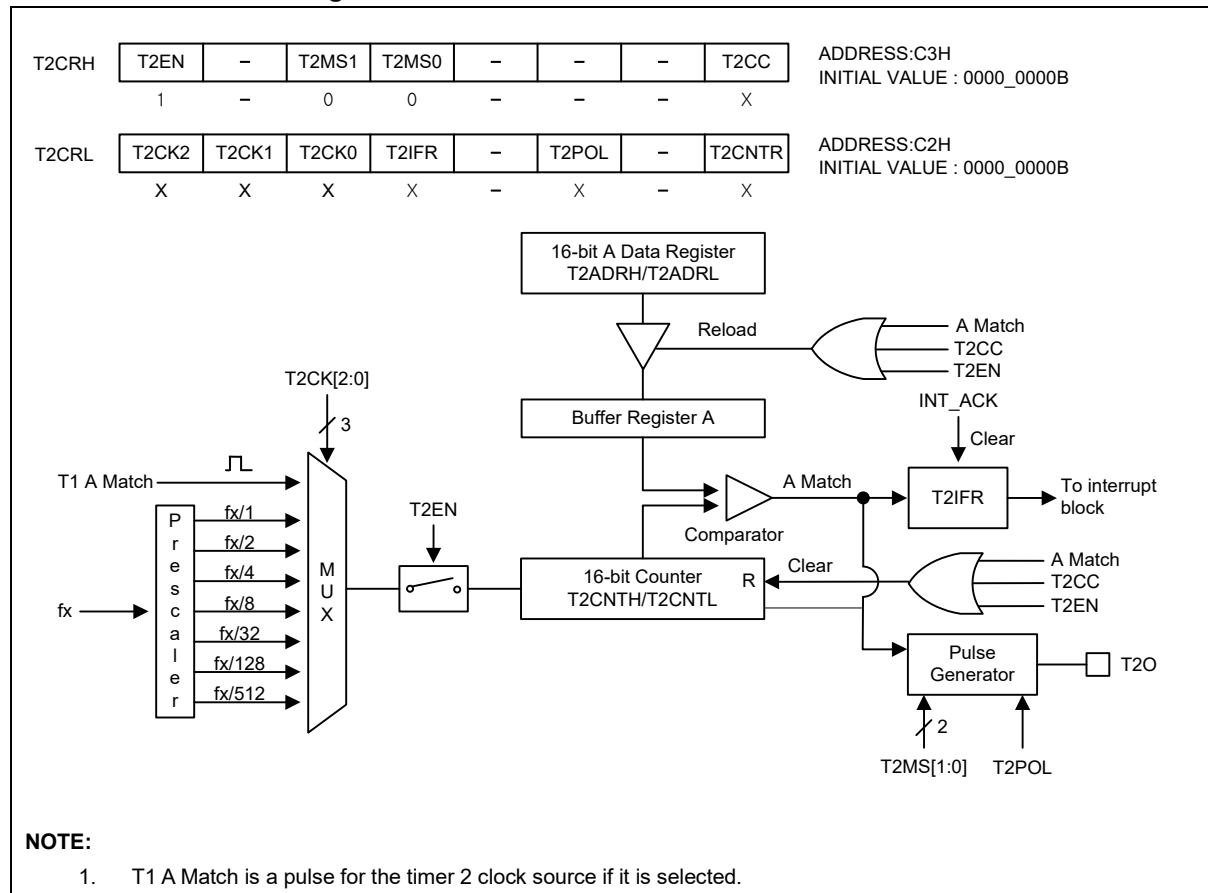


Figure 31. 16-bit Timer/Counter 2 Example

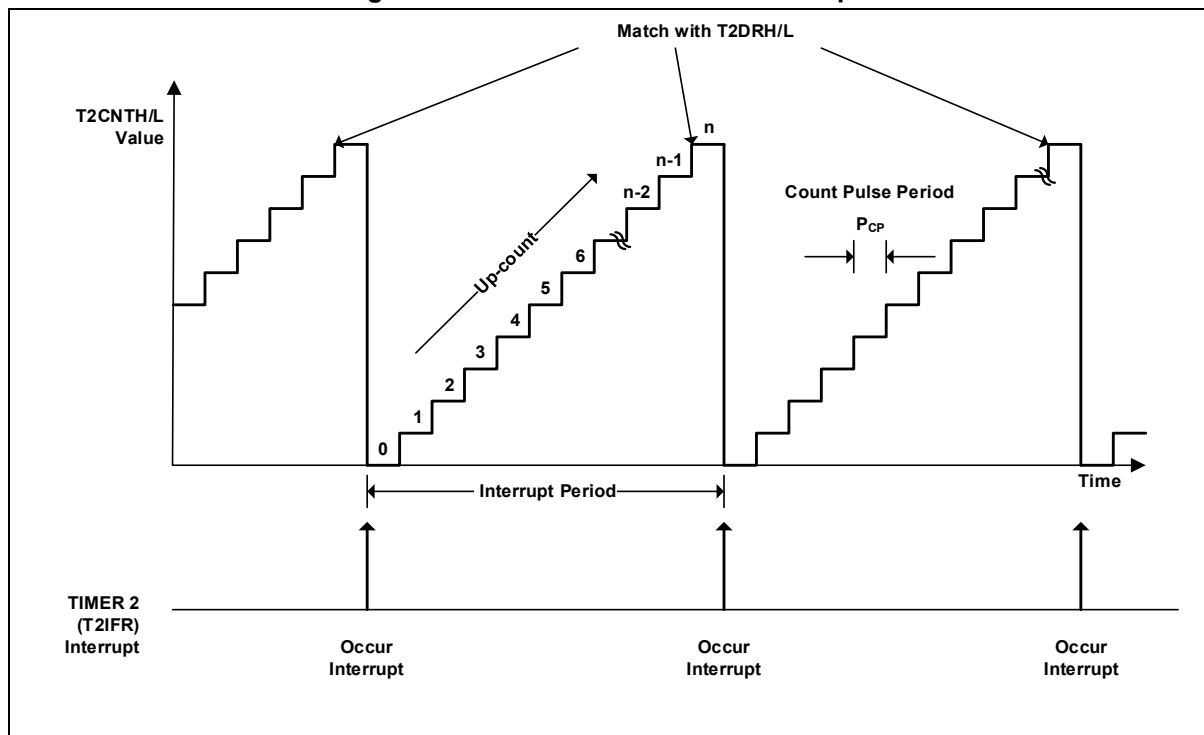


Figure 33. Input Capture Mode Operation for Timer 2

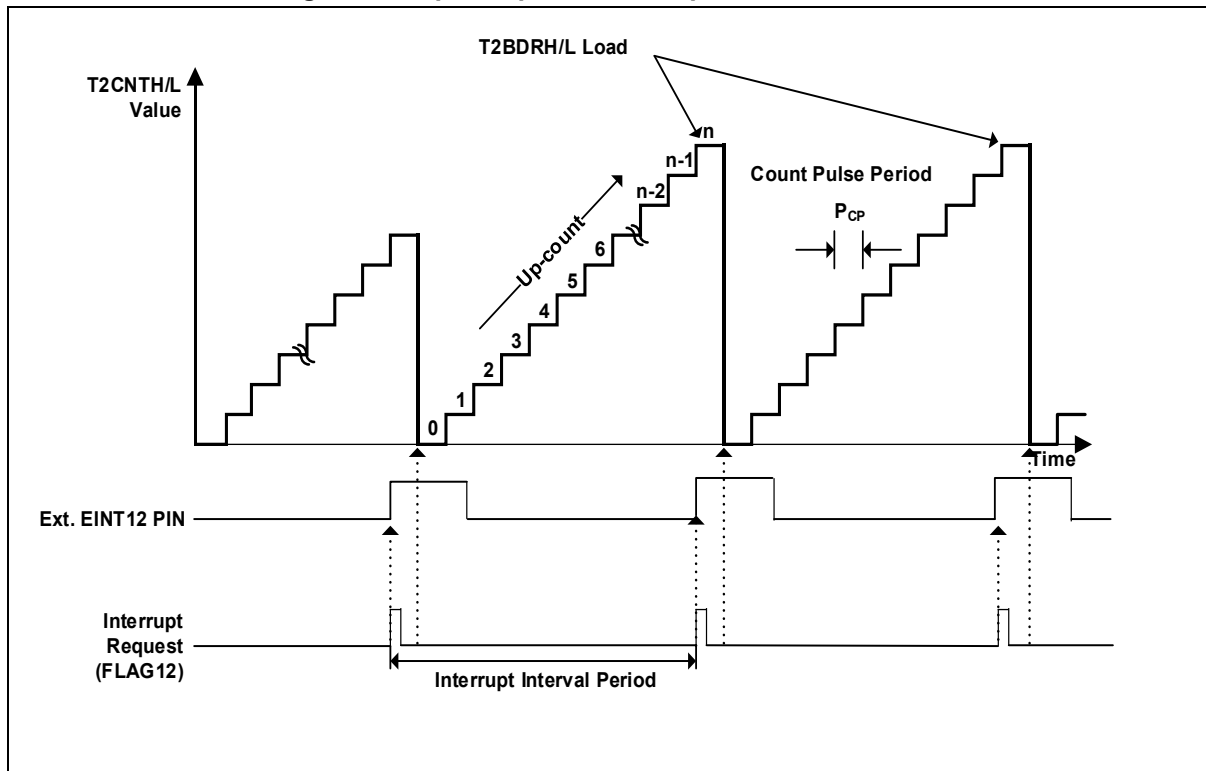
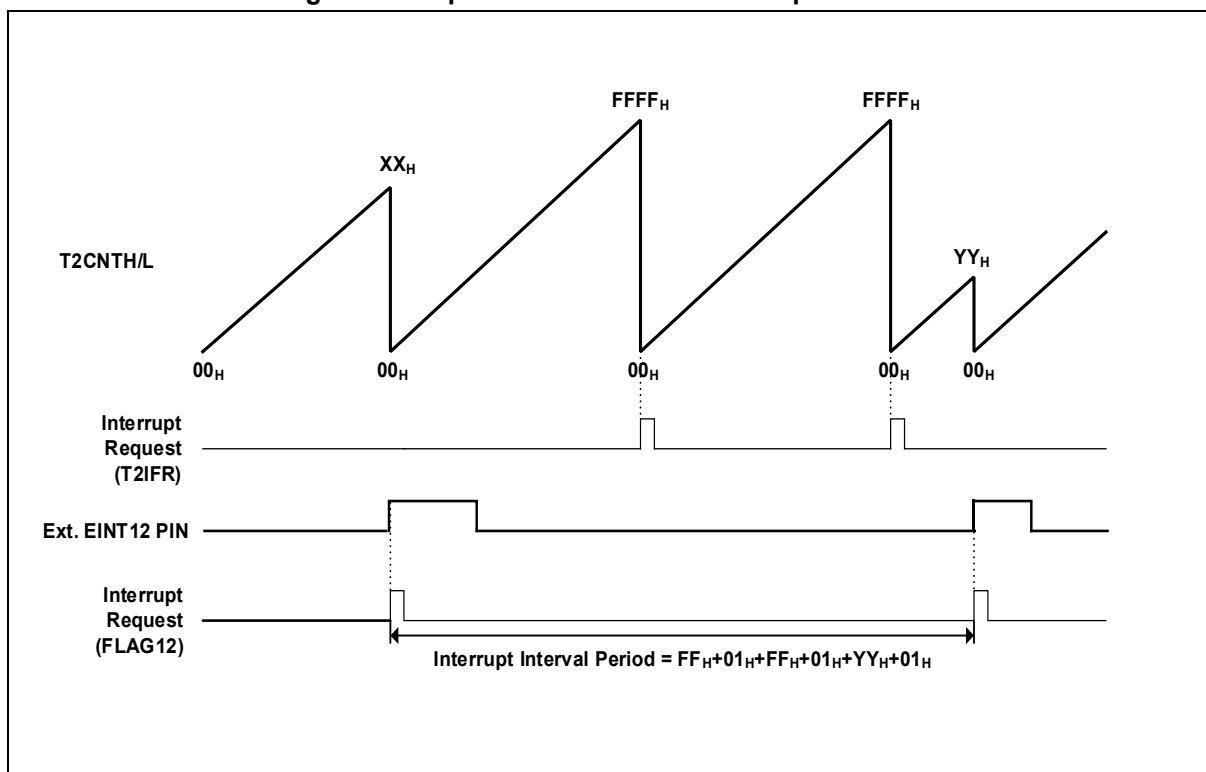


Figure 34. Express Timer Overflow in Capture Mode



16-bit PPG Mode

TIMER 2 has a PPG (Programmable Pulse Generation) function. In PPG mode, T2O/PWM2O pin outputs up to 16-bit resolution PWM output. For this function, T2O/PWM2O pin must be configured as a PWM output by setting P0FSRL[3:2] to '10'.

The period of the PWM output is determined by T2ADRH/T2ADRL, and duty of the PWM output is determined by T2BDRH/T2BDRL.

Figure 35. 16-bit PPG Mode for Timer 2

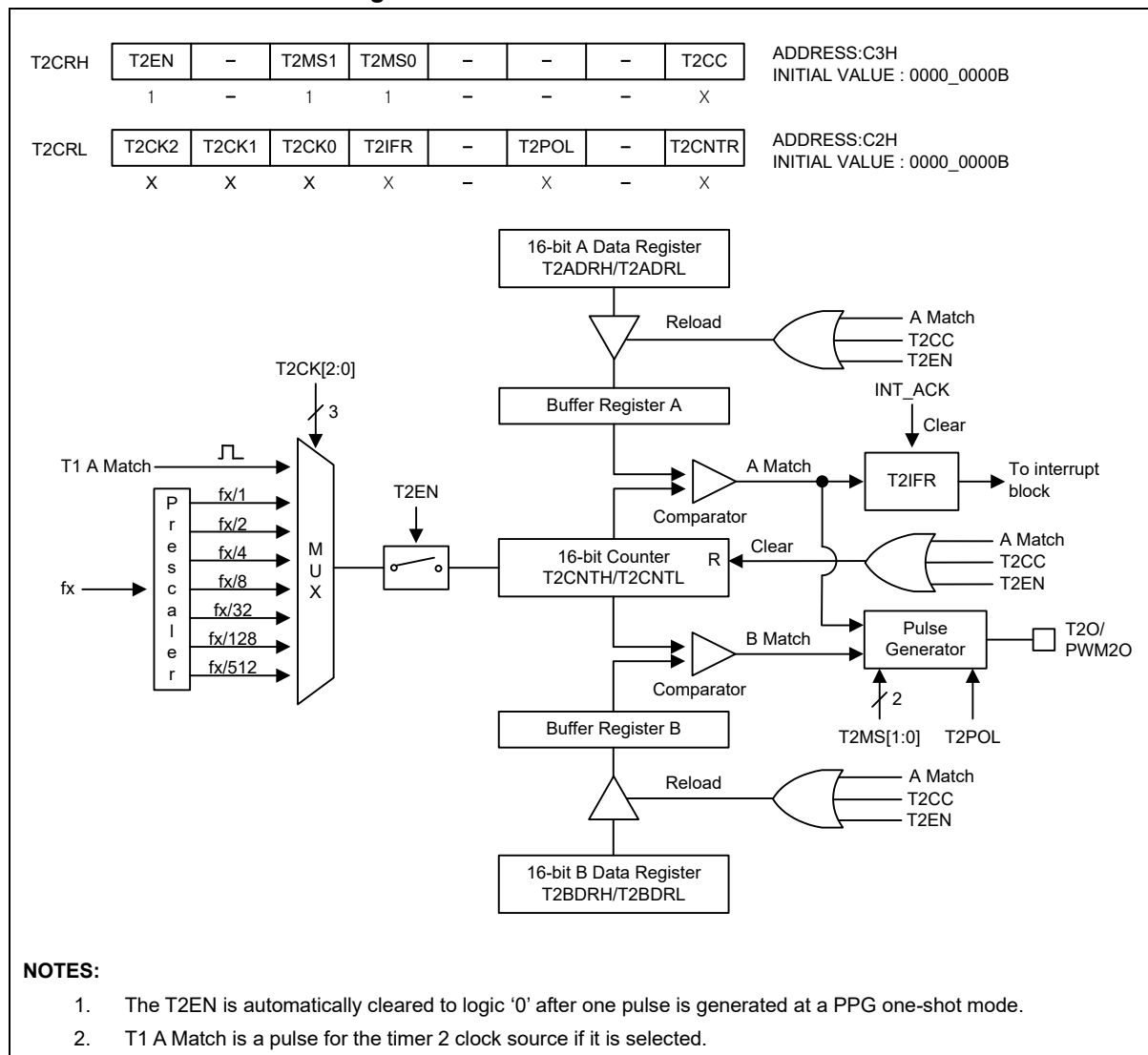
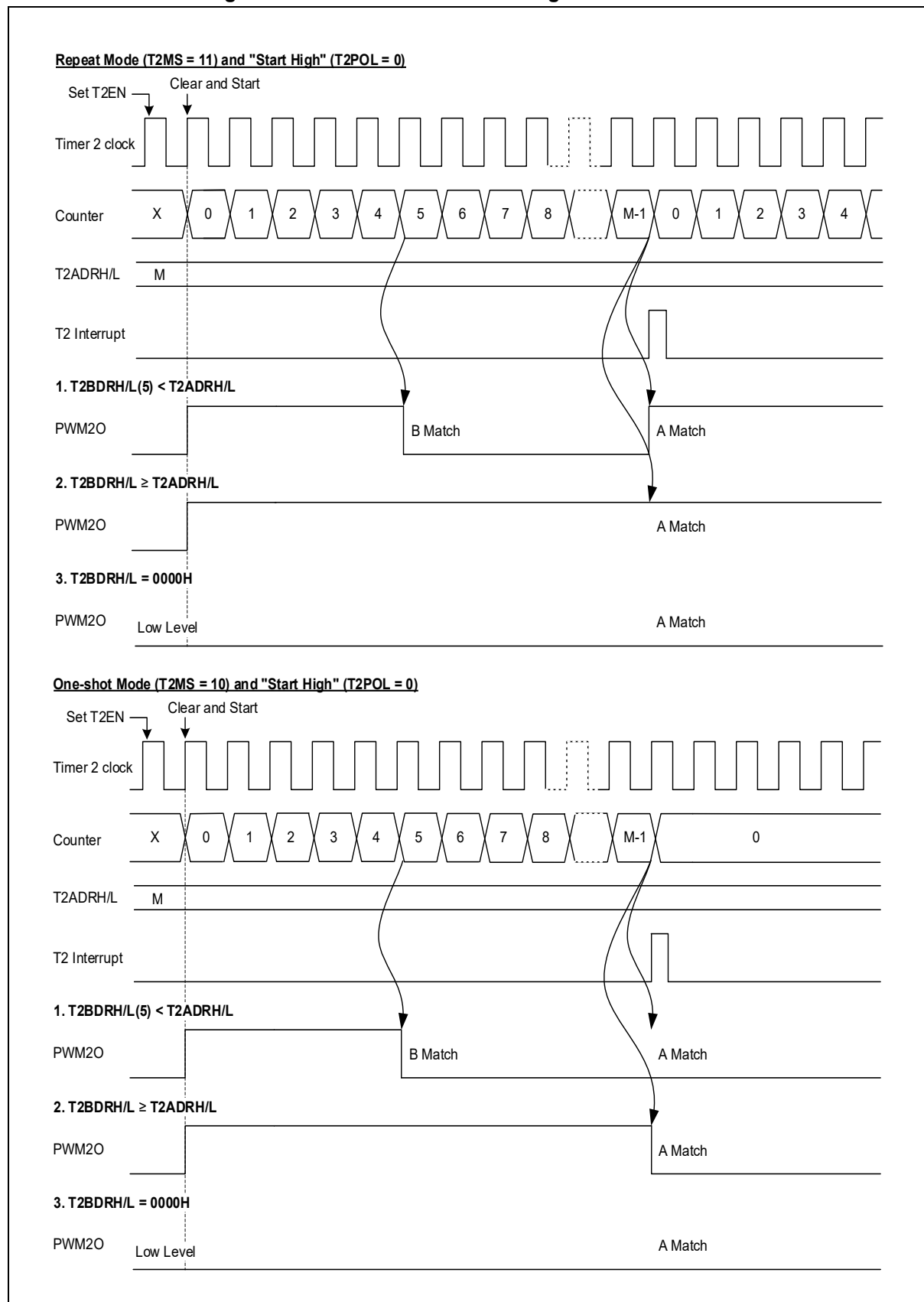
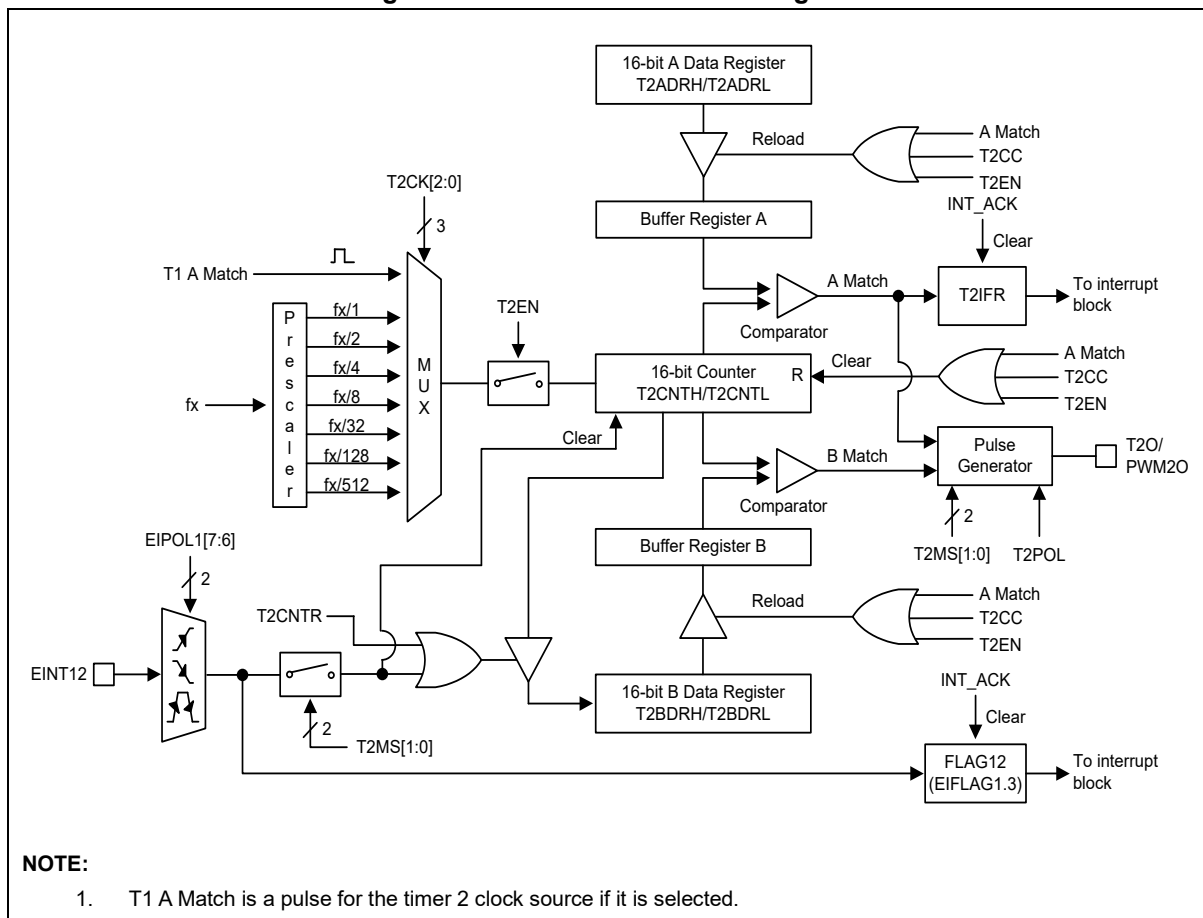


Figure 36. 16-bit PPG Mode Timing Chart for Timer 2



Block Diagram**Figure 37. 16-bit Timer 2 Block Diagram**

2.4.9.4 Timer 3

The 16-bit timer 3 consists of a multiplexer, timer 3 A data high/low register, timer 3 B data high/low register and timer 3 control high/low register (T3ADRH, T3ADRL, T3BDRH, T3BDRL, T3CRH, and T3CRL).

Timer 3 operates in one of the following modes:

- 16-bit timer/counter mode
- 16-bit capture mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

The timer/counter 3 can be clocked by an internal or an external clock source (EC3). The clock source is selected by a clock selection logic controlled by clock selection bits (T3CK[2:0]).

- TIMER 3 clock source: fx/1, fx/2, fx/4, fx/8, fx/64, fx/512, fx/2048 and EC3

In capture mode, data is captured into input capture data registers (T3BDRH/T3BDRL) by EINT43. Timer 3 results in the comparison between counter and data register through T3O port in timer/counter mode. In addition, timer 3 outputs PWM waveform through PWM3O port in the PPG mode.

Table 13. Timer 3 Operating Modes

T3EN	P0FSRL[3:2]	T3MS[1:0]	T3CK[2:0]	Timer 3
1	11	00	XXX	16-bit Timer/Counter Mode
1	00	01	XXX	16-bit Capture Mode
1	11	10	XXX	16-bit PPG Mode (one-shot mode)
1	11	11	XXX	16-bit PPG Mode (repeat mode)

16-bit Timer/Counter Mode

16-bit timer/counter mode is selected by control registers, and the 16-bit timer/counter has counter registers and data registers as shown in Figure 38. The counter register is increased by internal or external clock input. Timer 3 can use the input clock with one of 1, 2, 4, 8, 64, 512 and 2048 prescaler division rates (T3CK[2:0]). When the values of T3CNTH/T3CNTL and T3ADRH/T3ADRL are identical to each other in timer 3, a match signal is generated, and the interrupt of Timer 3 occurs. The T3CNTH/T3CNTL values are automatically cleared by the match signal. It can be cleared by software (T3CC) too.

External clock (EC3) counts up the timer at the rising edge. If the EC3 is selected as a clock source by T3CK[2:0], EC3 port should be set as an input port by configuring P16 IO bit.

Figure 38. 16-bit Timer/Counter Mode for Timer 3

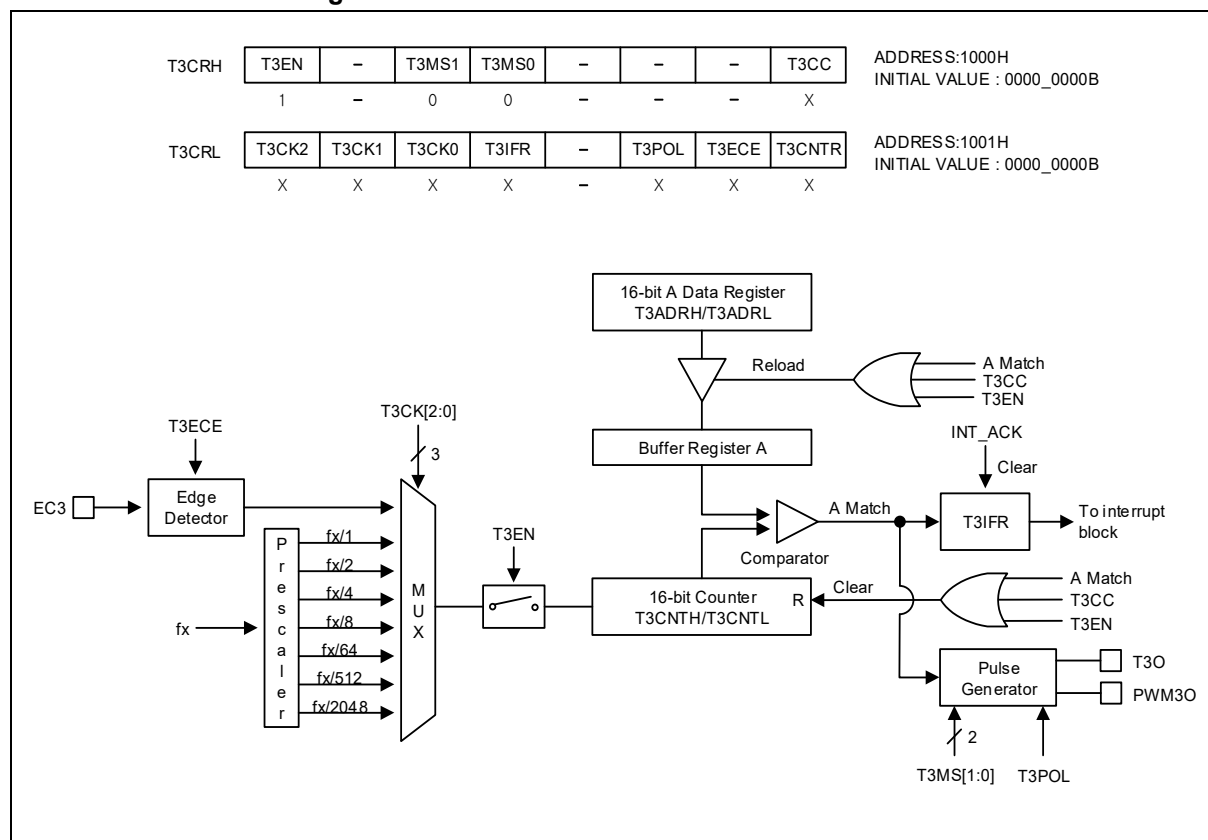
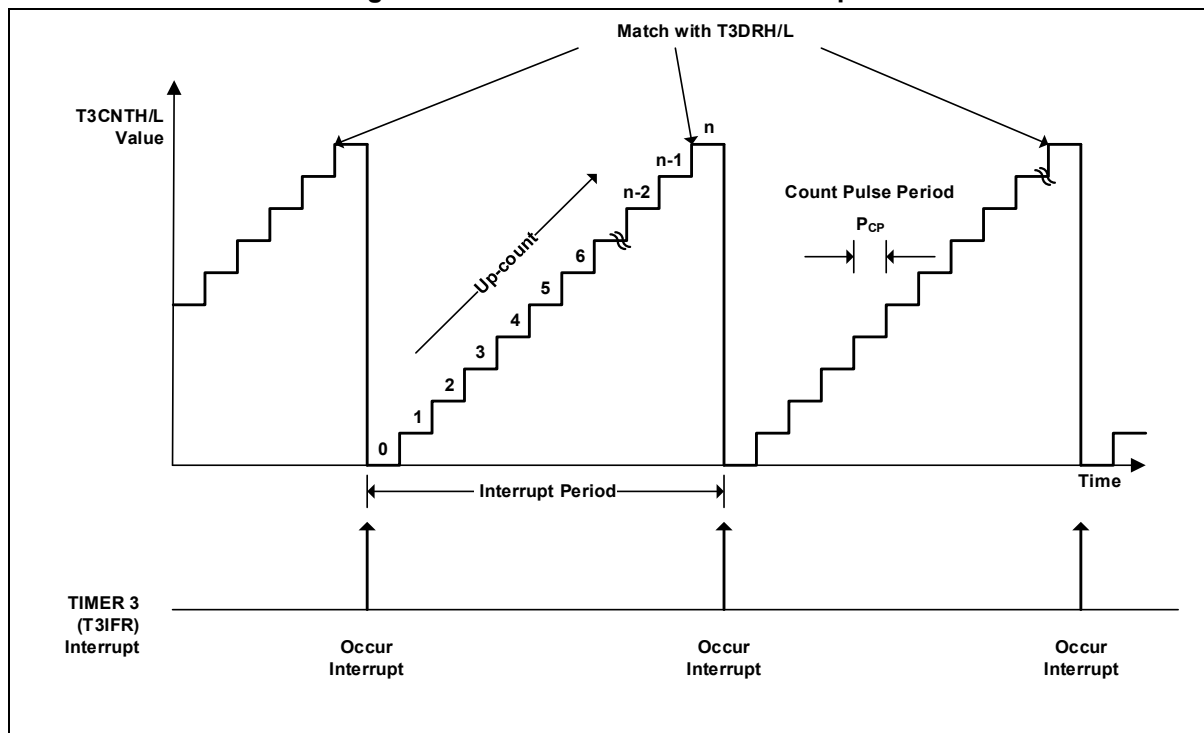


Figure 39. 16-bit Timer/Counter 3 Example



16-bit Capture Mode

Timer 3 capture mode is set by configuring T3MS[1:0] as '01'. It uses an internal/external clock as a clock source. Basically, the 16-bit timer 3 capture mode has the same function as the 16-bit timer/counter mode, and the interrupt occurs when T3CNTH/T3CNTL is equal to T3ADRH/T3ADRL. The T3CNTH, T3CNTL values are automatically cleared by a match signal. It can be cleared by software (T3CC) too.

A timer interrupt in capture mode is very useful when the pulse width of captured signal is wider than the maximum period of timer. Capture result is loaded into T3BDRH/T3BDRL.

According to EIPOL0L registers setting, the external interrupt EINT43 function is selected. EINT43 pin must be set as an input port.

Figure 40. 16-bit Capture Mode for Timer 3

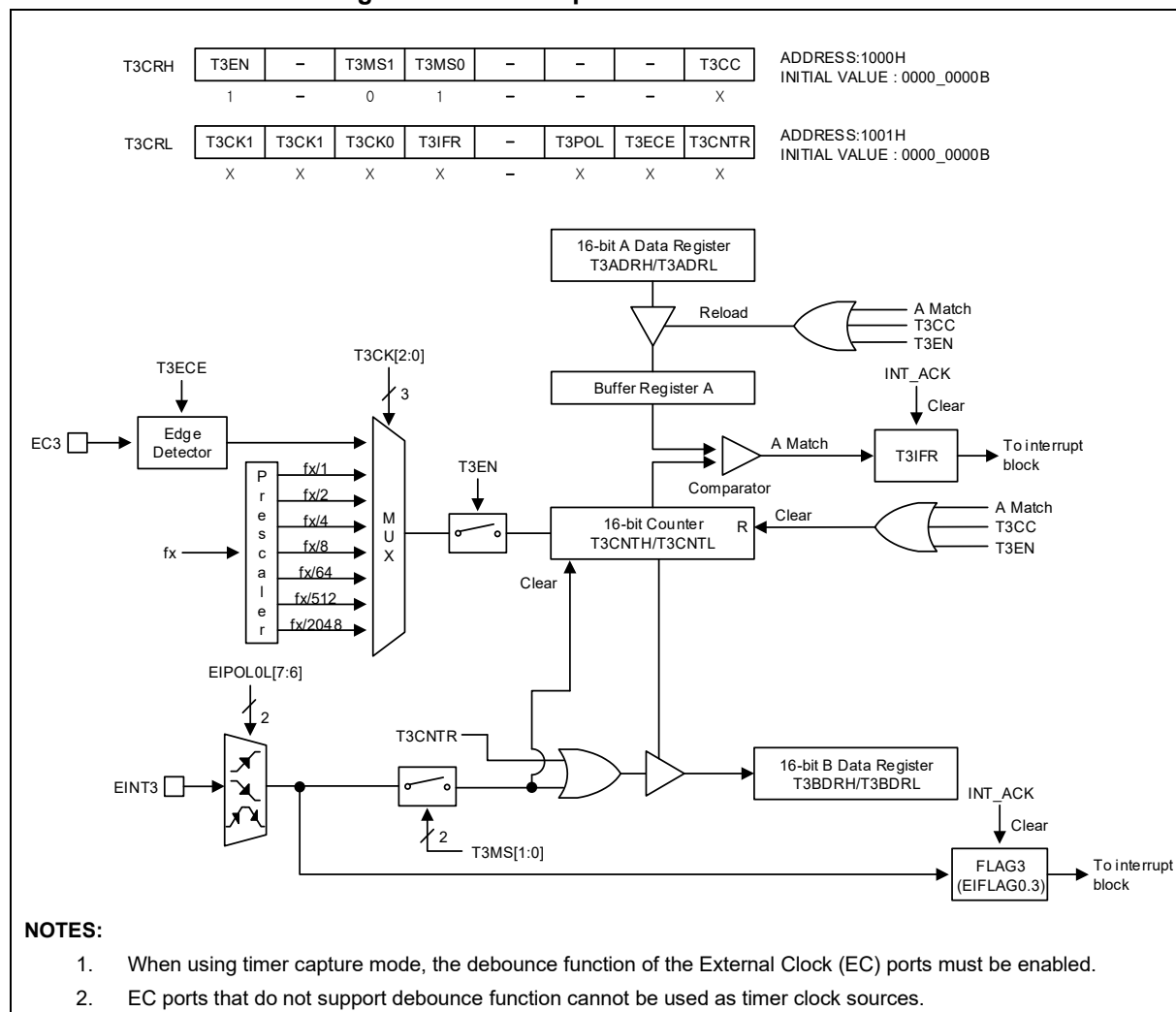


Figure 41. Input Capture Mode Operation for Timer 3

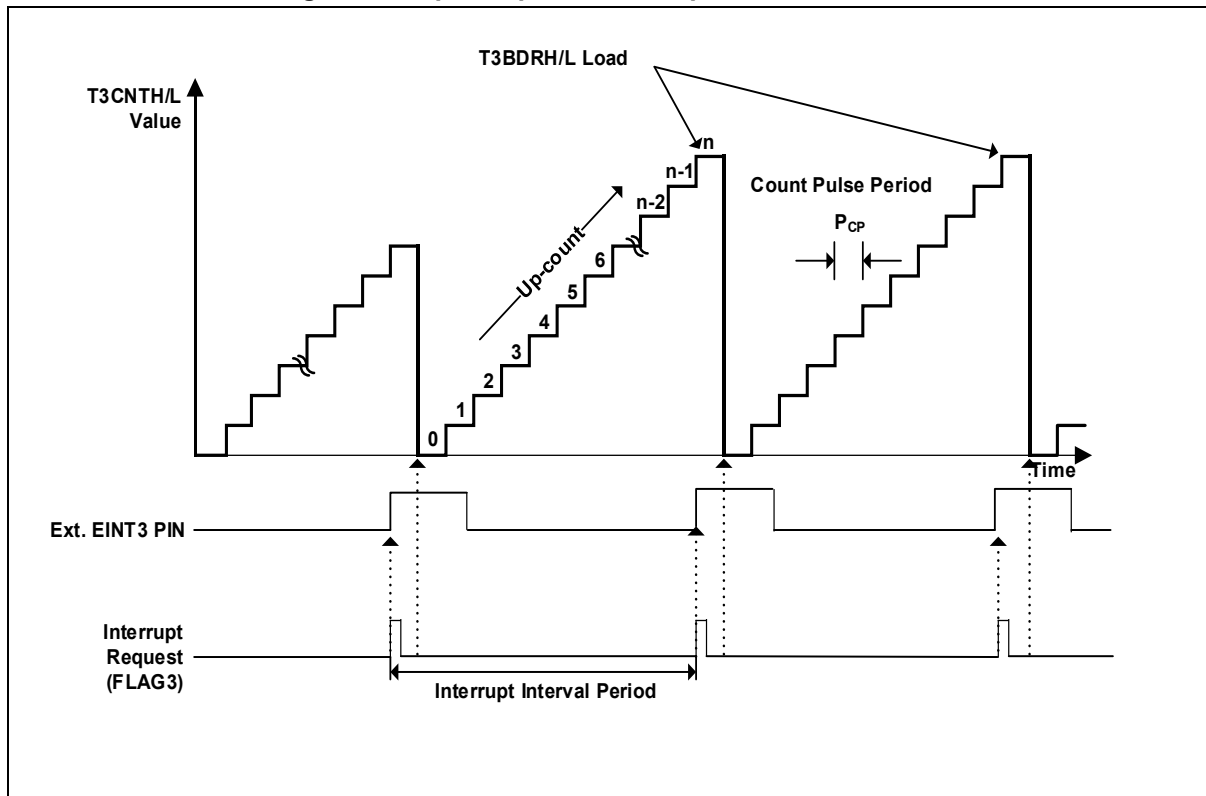
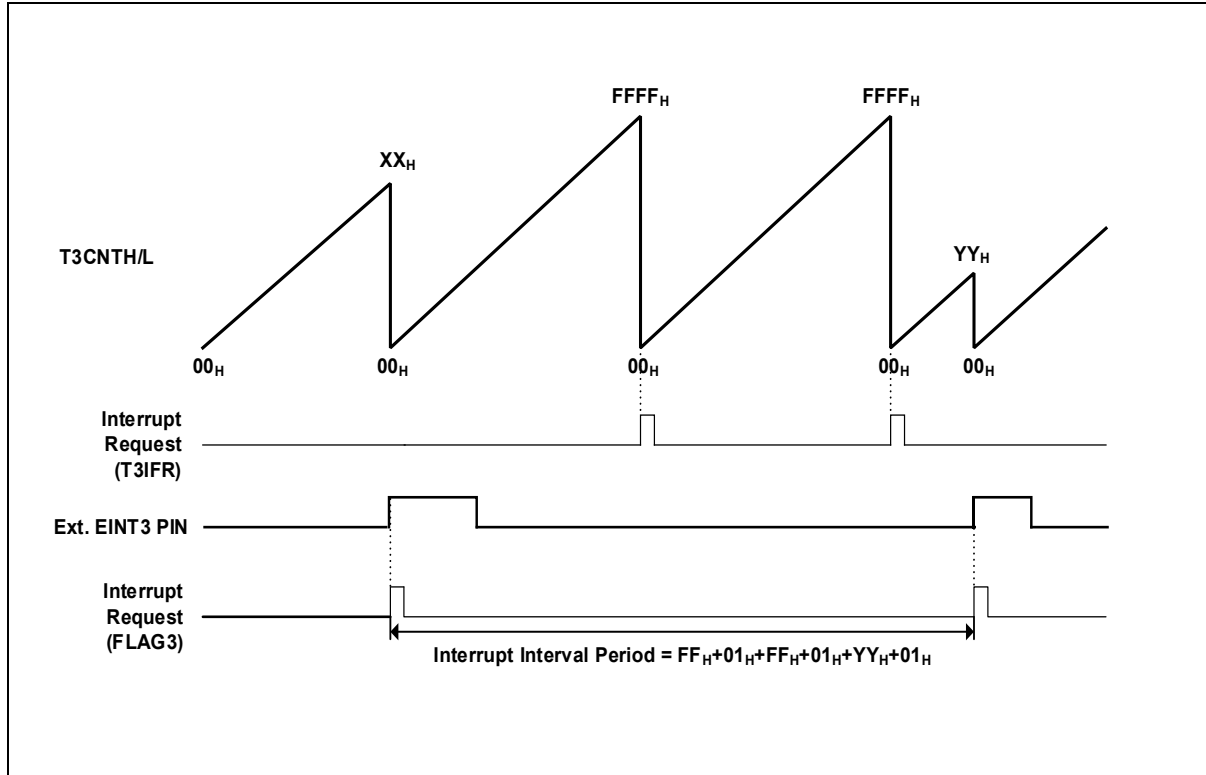


Figure 42. Express Timer Overflow in Capture Mode



16-bit PPG Mode

TIMER 3 has a PPG (Programmable Pulse Generation) function. In PPG mode, T3O/PWM3O pin outputs up to 16-bit resolution PWM output. For this function, T3O/PWM3O pin must be configured as a PWM output by setting P0FSRL[1:0] to '10' or P4FSRH[3:2] to '10'.

The period of the PWM output is determined by T3ADRH/T3ADRL, and duty of the PWM output is determined by T3BDRH/T3BDRL.

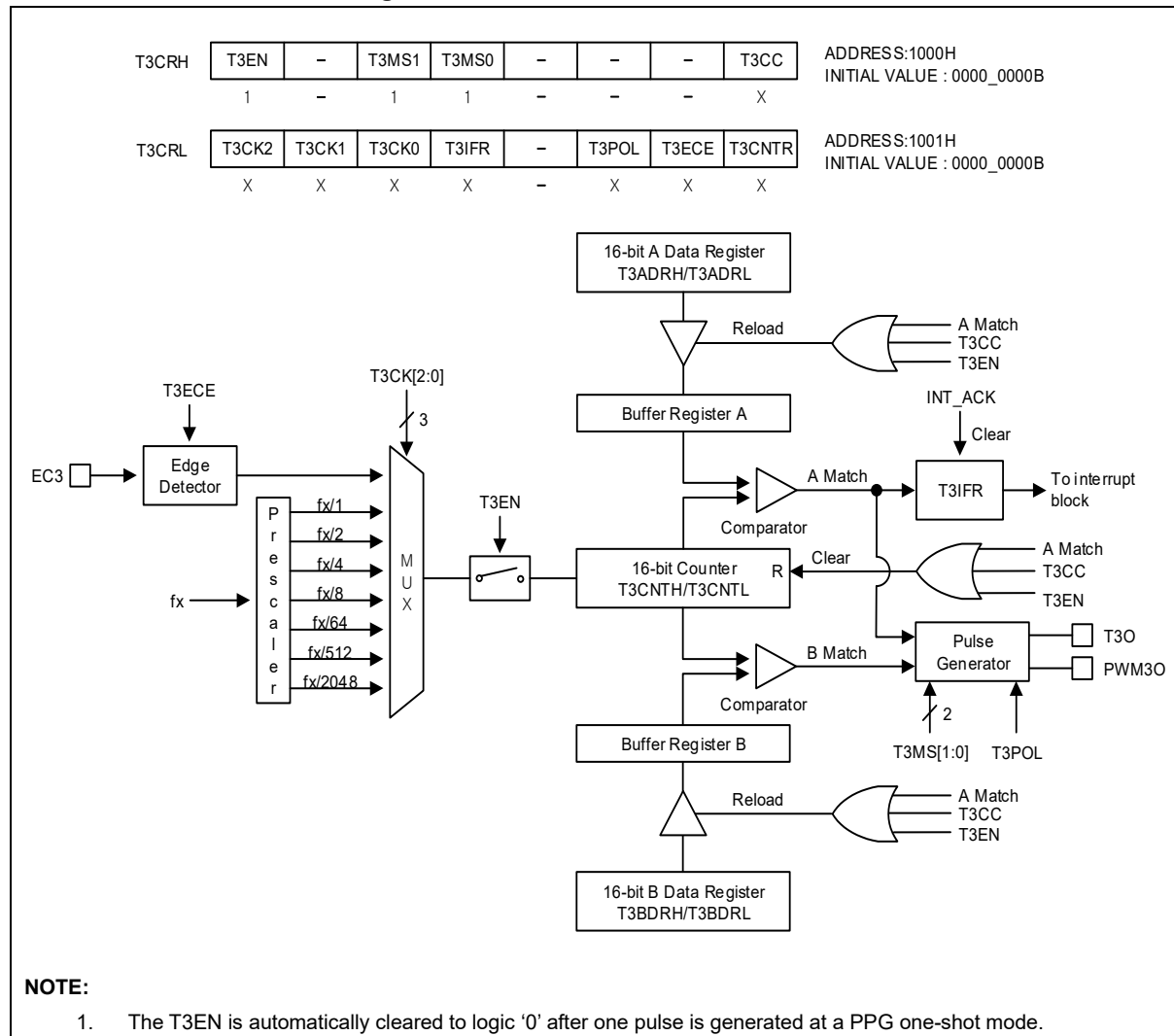
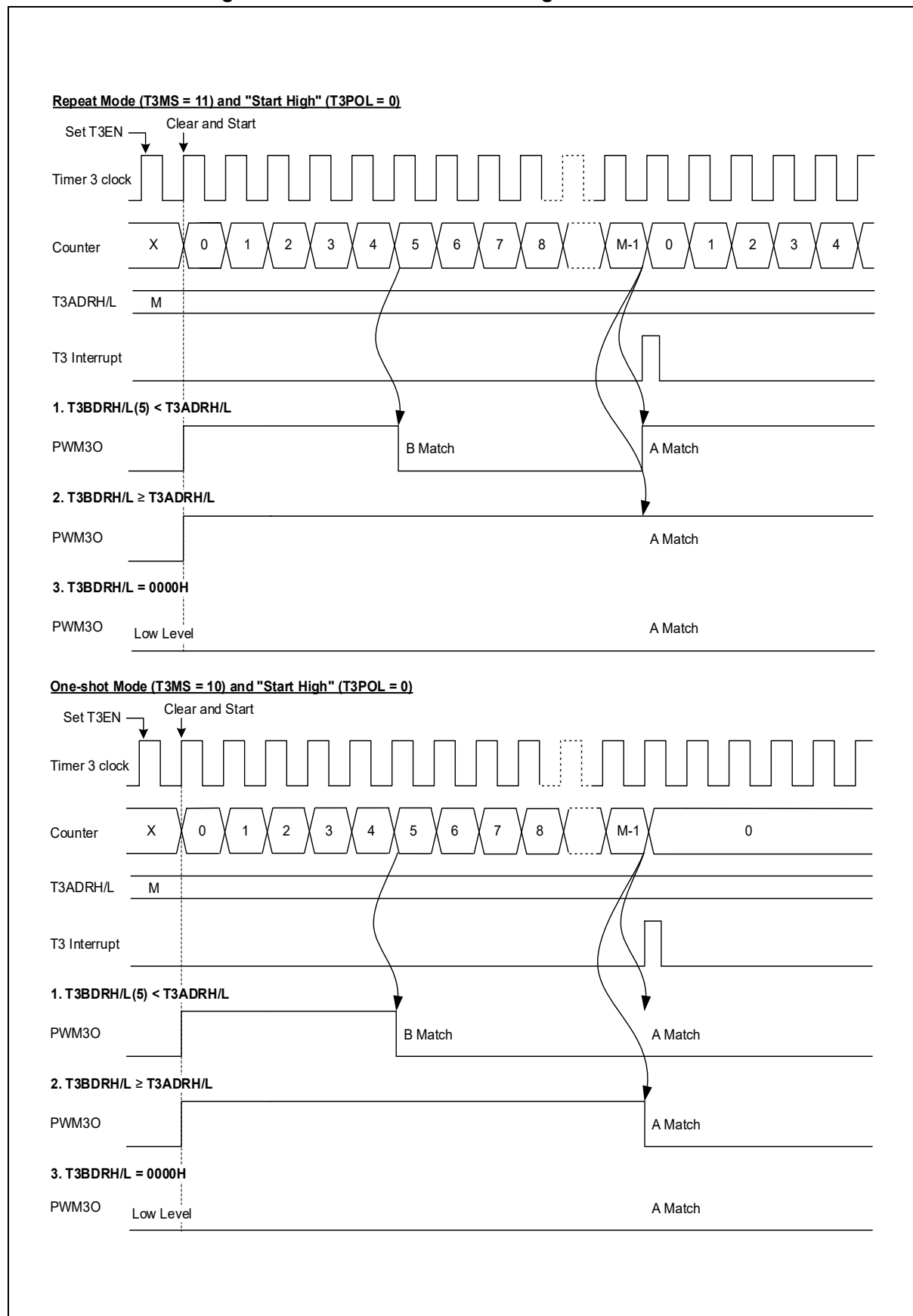
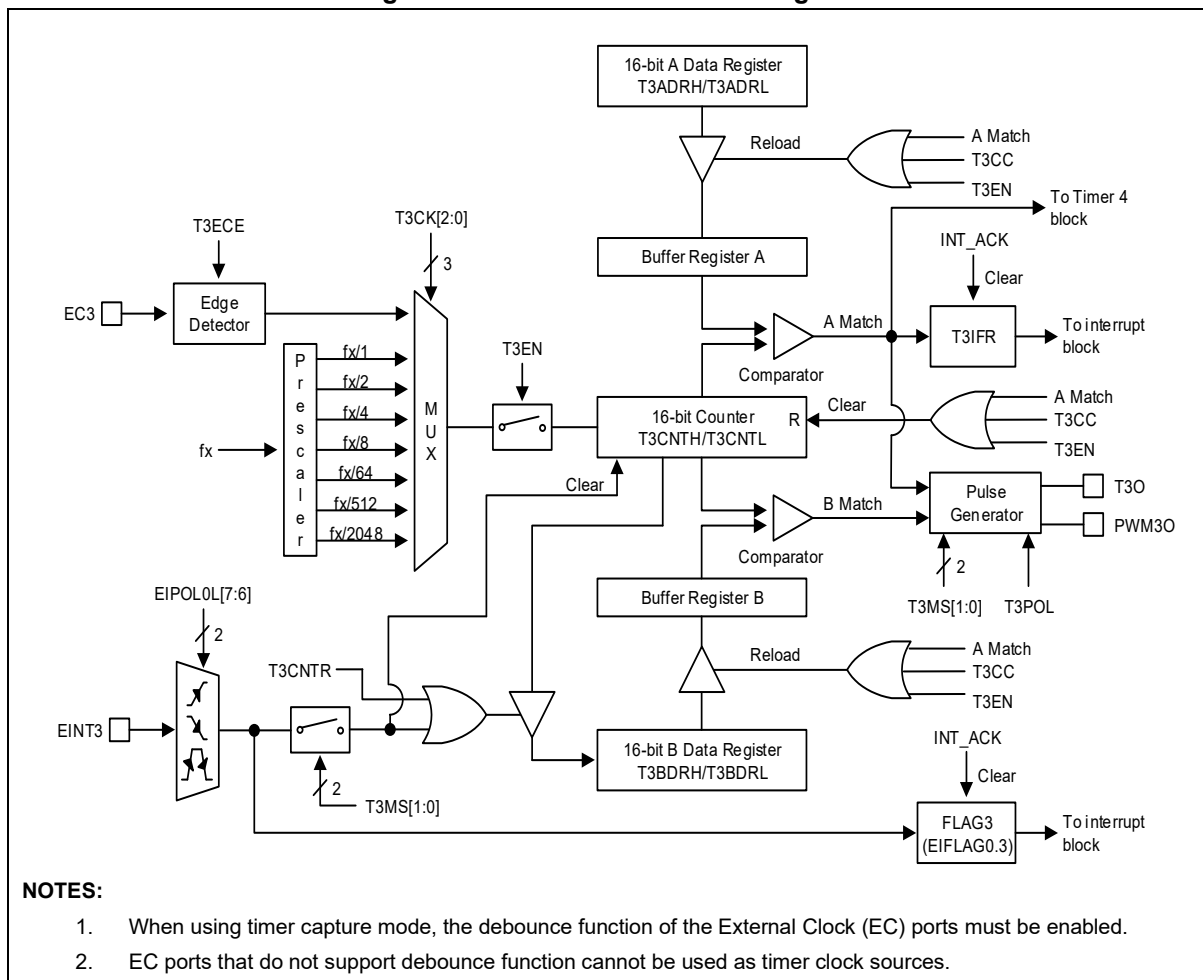
Figure 43. 16-bit PPG Mode for Timer 3

Figure 44. 16-bit PPG Mode Timing Chart for Timer 3



Block Diagram**Figure 45. 16-bit Timer 3 Block Diagram**

2.4.9.5 Timer 4

The 16-bit timer 4 consists of a multiplexer, timer 4 A data high/low register, timer 4 B data high/low register and timer 4 control high/low register (T4ADRH, T4ADRL, T4BDRH, T4BDRL, T4CRH, and T4CRL).

Timer 4 operates in one of the following modes:

- 16-bit timer/counter mode
- 16-bit capture mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

The timer/counter 4 can be a divided clock of a system clock selected from prescaler output and T3 A Match (timer 3 A match signal). The clock source is selected by a clock selection logic controlled by clock selection bits (T4CK[2:0]).

- TIMER 4 clock source: fx/1, fx/2, fx4, fx/8, fx/32, fx/128, fx/512 and T3 A Match

In capture mode, data is captured into input capture data registers (T4BDRH/T4BDRL) by EINT44. In timer/counter mode, whenever counter value is equal to T4ADRH/L, T4O port toggles. In addition, the timer 4 outputs PWM waveform to PWM4O port in the PPG mode.

Table 14. TIMER 4 Operating Modes

T4EN	P0FSRL[3:2]	T4MS[1:0]	T4CK[2:0]	Timer 4
1	11	00	XXX	16-bit Timer/Counter Mode
1	00	01	XXX	16-bit Capture Mode
1	11	10	XXX	16-bit PPG Mode (one-shot mode)
1	11	11	XXX	16-bit PPG Mode (repeat mode)

16-bit Timer/Counter Mode

16-bit timer/counter mode is selected by control registers, and the 16-bit timer/counter has counter registers and data registers as shown in Figure 46. The counter register is increased by internal or timer 4 A match clock input.

Timer 4 can use the input clock with one of 1, 2, 4, 8, 32, 128, 512 and T3 A Match prescaler division rates (T4CK[2:0]). When the values of T4CNTH/T4CNTL and T4ADRH/T4ADRL are identical to each other in timer 4, a match signal is generated, and the interrupt of Timer 4 occurs. The T4CNTH/T4CNTL values are automatically cleared by the match signal. It can be cleared by software (T4CC) too.

Figure 46. 16-bit Timer/Counter Mode for Timer 4

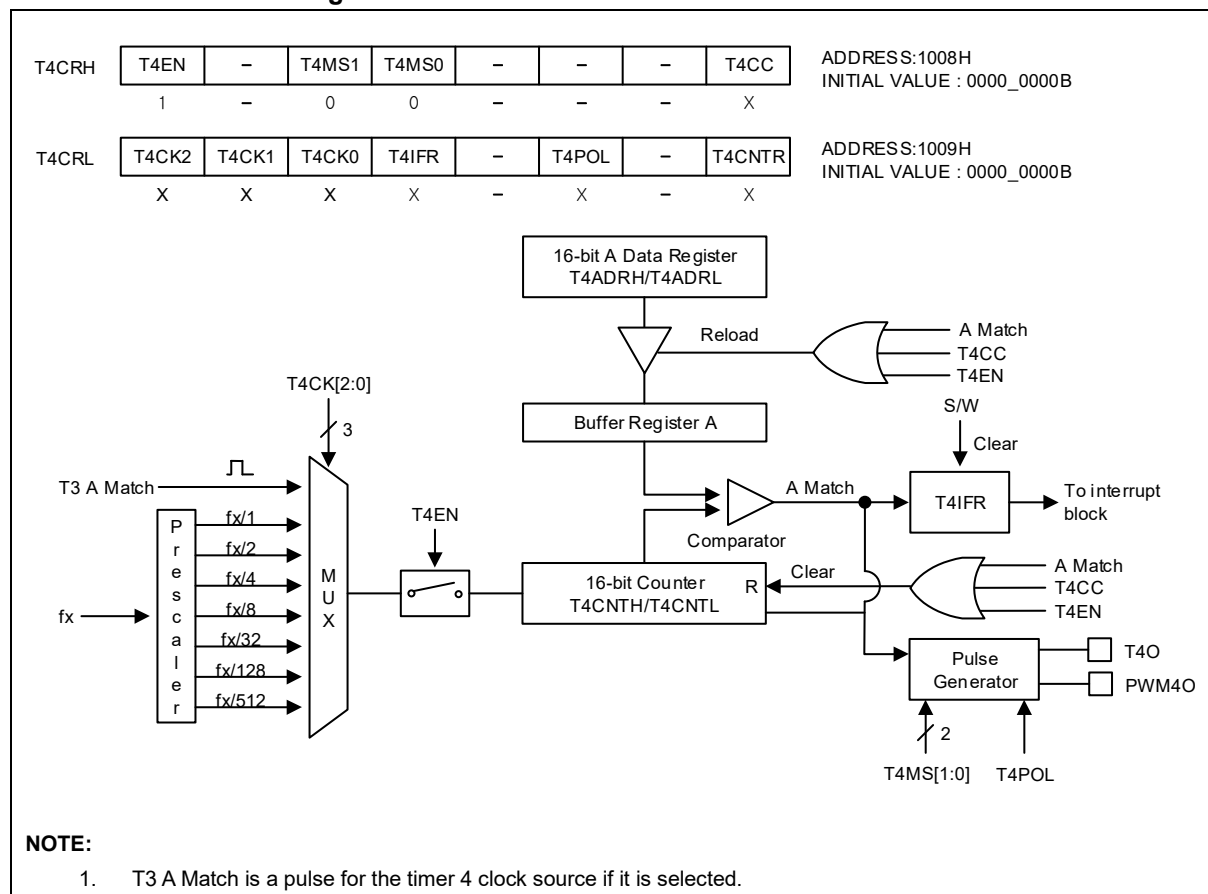
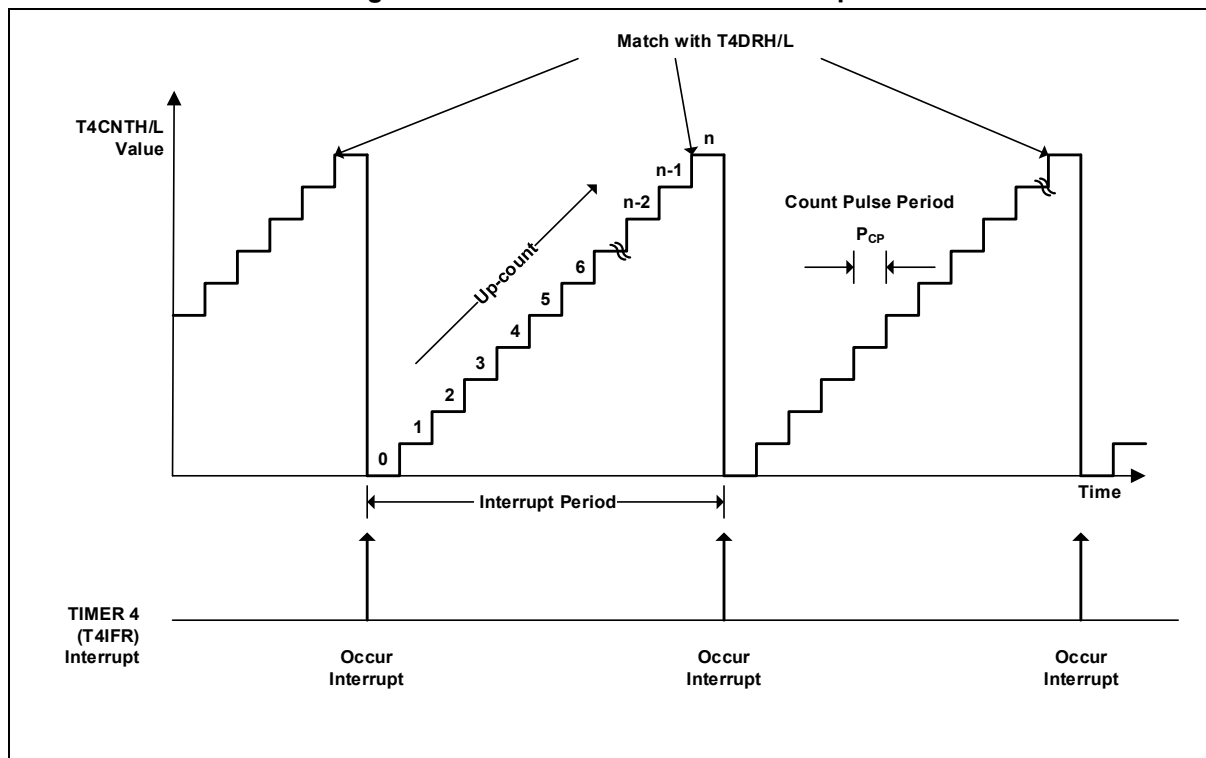


Figure 47. 16-bit Timer/Counter 4 Example



16-bit Capture Mode

Timer 4 capture mode is set by configuring T4MS[1:0] as '01'. It uses an internal clock as a clock source. Basically, the 16-bit timer 4 capture mode has the same function as the 16-bit timer/counter mode, and the interrupt occurs when T4CNTH/T4CNTL is equal to T4ADRH/T4ADRL. The T4CNTH, T4CNTL values are automatically cleared by a match signal. It can be cleared by software (T4CC) too.

A timer interrupt in capture mode is very useful when the pulse width of captured signal is wider than the maximum period of timer. Capture result is loaded into T4BDRH/T4BDRL. In the timer 4 capture mode, timer 4 output (T4O) waveform is not available.

According to EIPOL0L registers setting, the external interrupt EINT44 function is selected. EINT44 pin must be set as an input port.

Figure 48. 16-bit Capture Mode for Timer 4

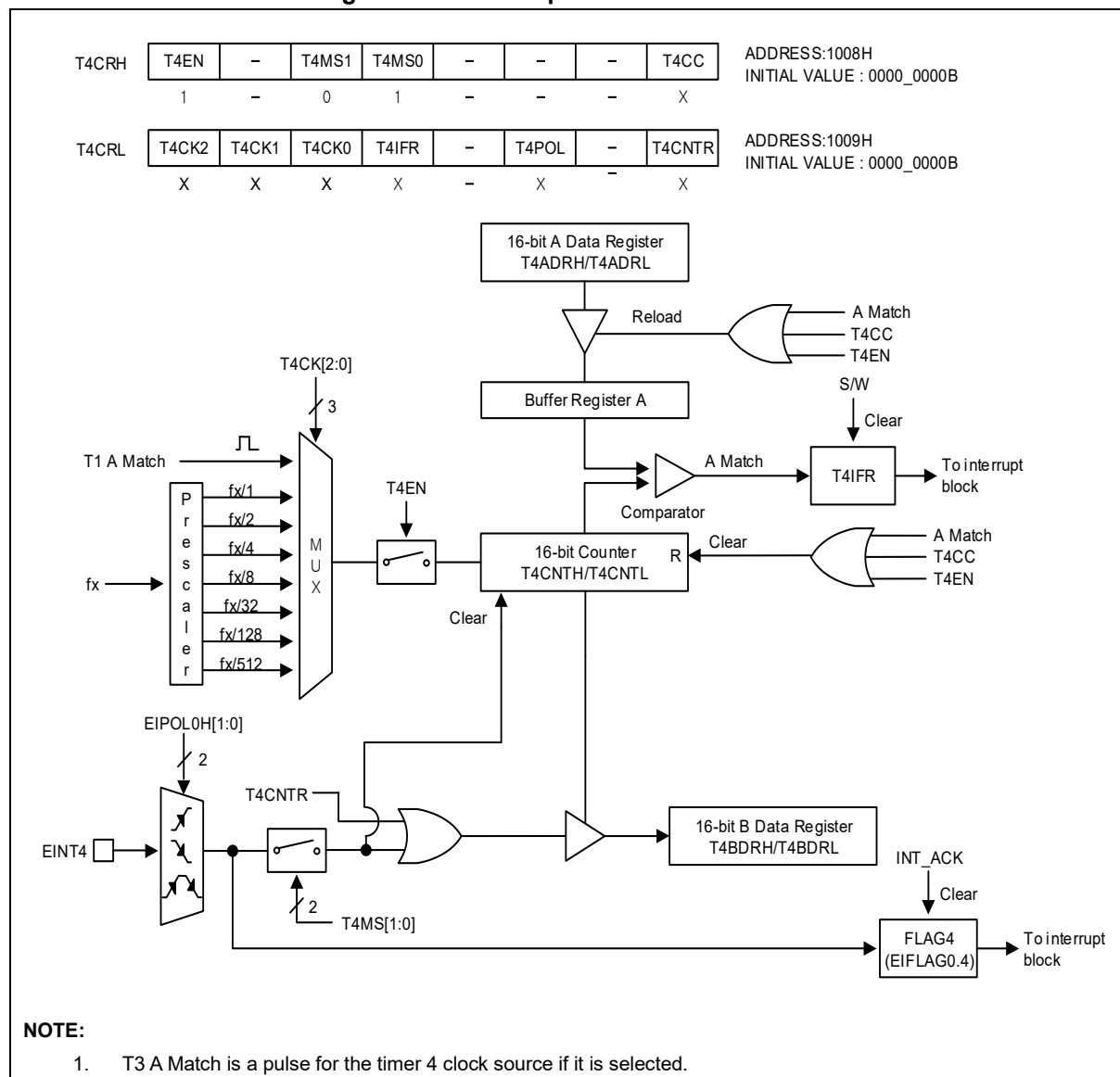


Figure 49. Input Capture Mode Operation for Timer 4

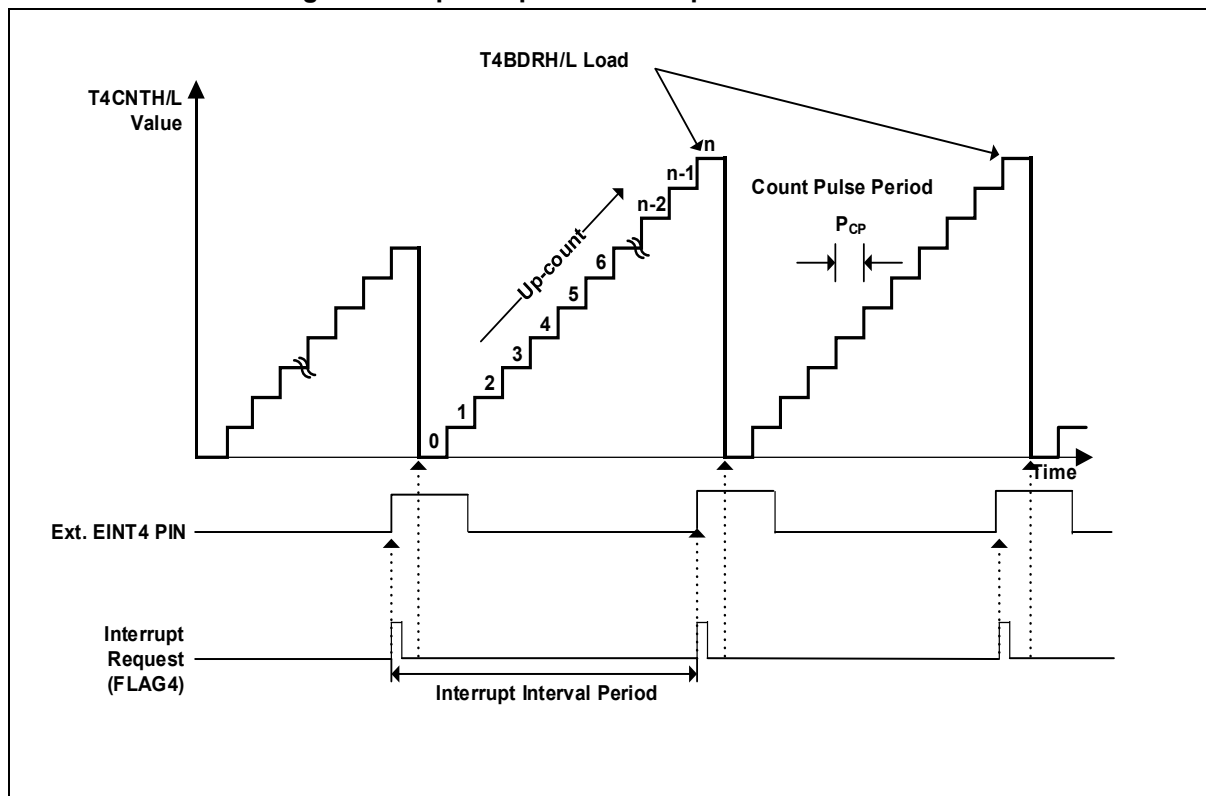
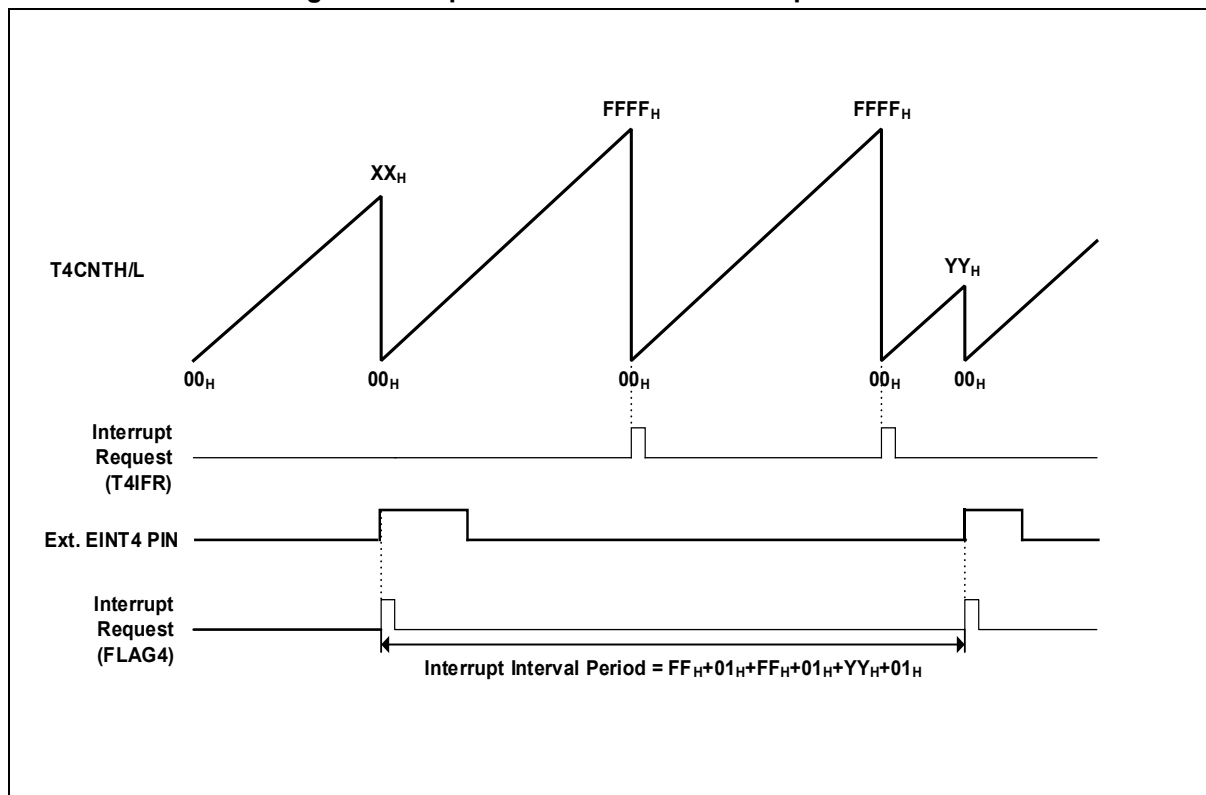


Figure 50. Express Timer Overflow in Capture Mode



16-bit PPG Mode

TIMER 4 has a PPG (Programmable Pulse Generation) function. In PPG mode, T4O/PWM4O pin outputs up to 16-bit resolution PWM output. For this function, T4O/PWM4O pin must be configured as a PWM output by setting P2FSRH[7:6] to '10'.

The period of the PWM output is determined by T4ADRH/T4ADRL, and duty of the PWM output is determined by T4BDRH/T4BDRL.

Figure 51. 16-bit PPG Mode for Timer 4

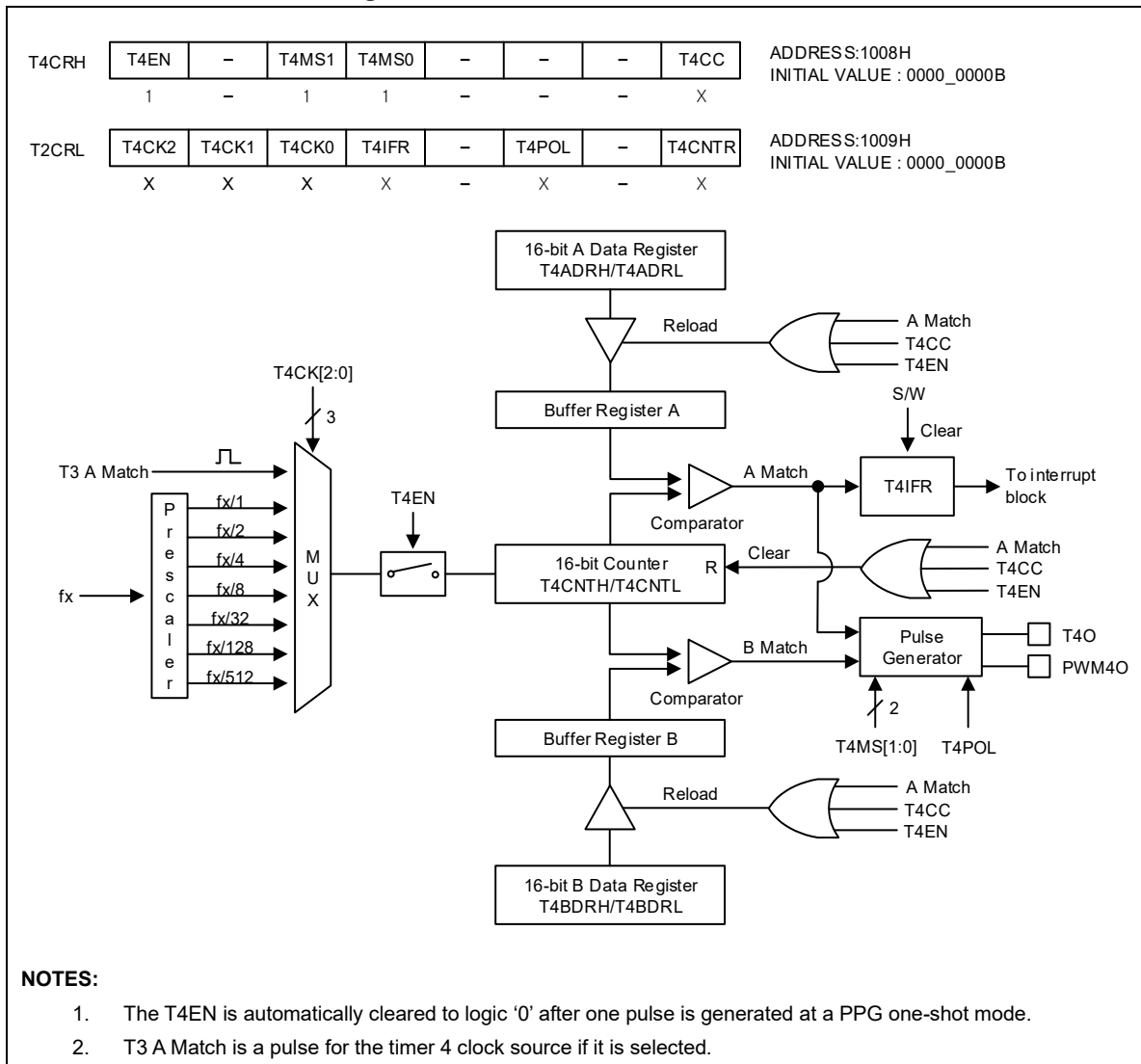
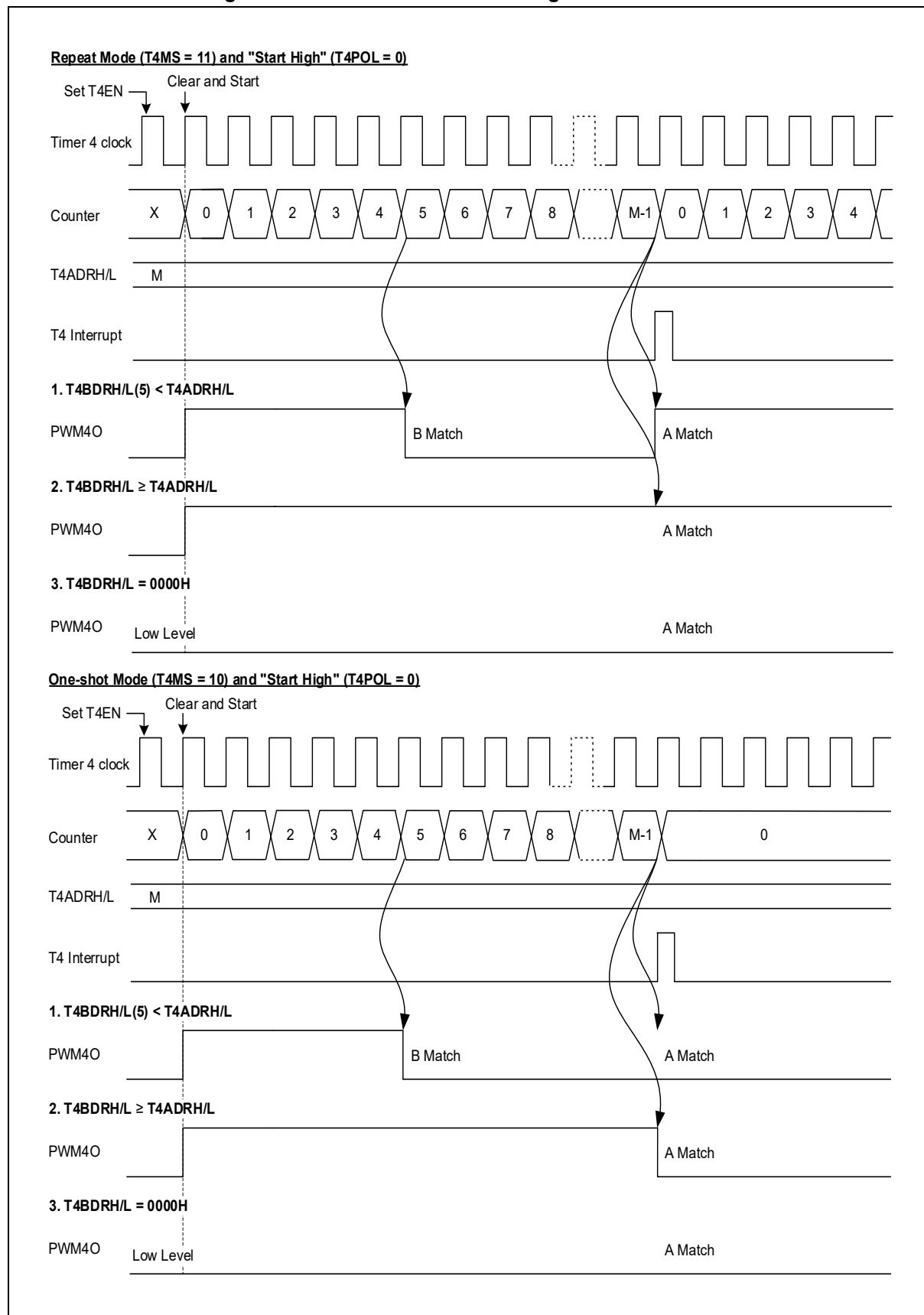
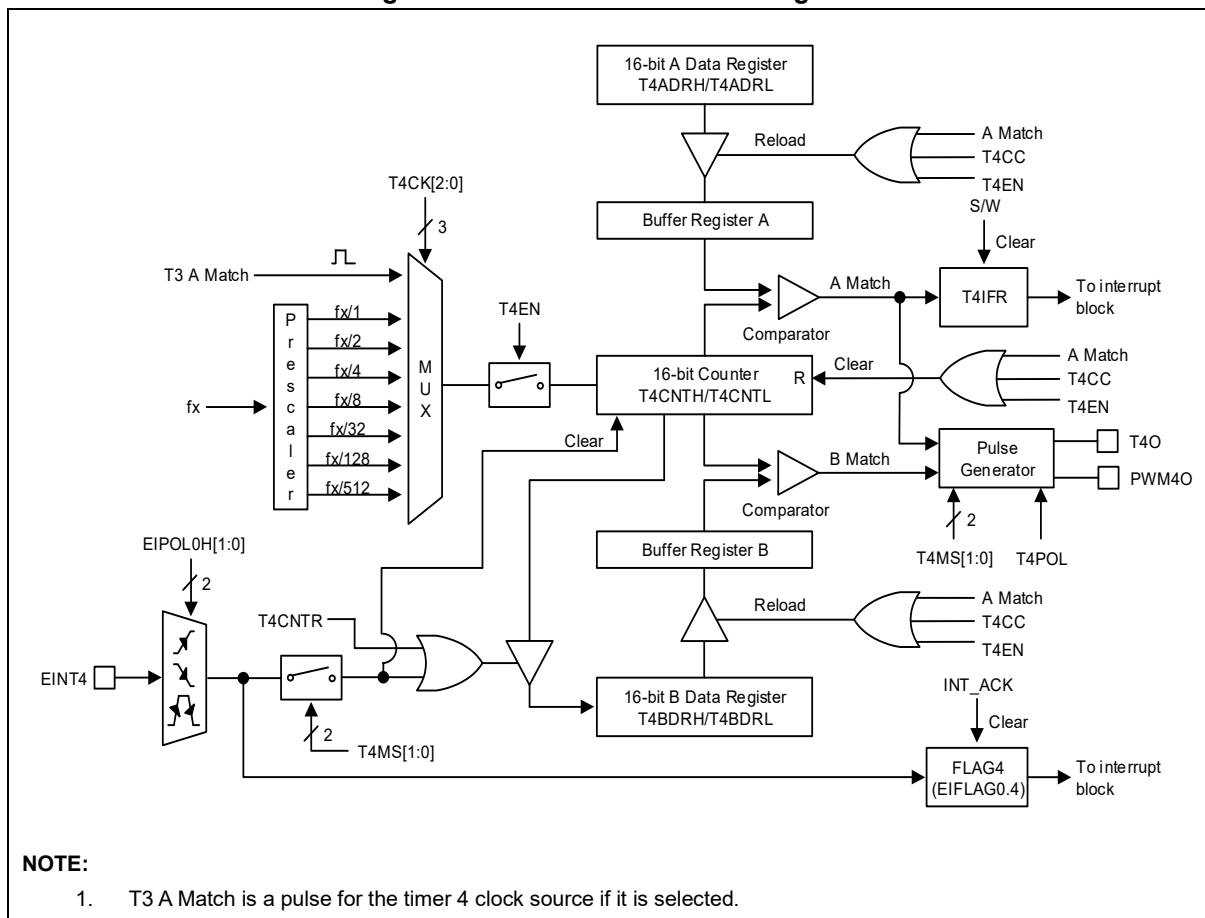


Figure 52. 16-bit PPG Mode Timing Chart for Timer 4



Block Diagram**Figure 53. 16-bit Timer 4 Block Diagram**

2.4.9.6 Timer 5

The 16-bit timer 5 consists of a multiplexer, timer 5 A data high/low register, timer 5 B data high/low register and timer 5 control high/low register (T5ADRH, T5ADRL, T5BDRH, T5BDRL, T5CRH, and T5CRL).

Timer 5 operates in one of the following modes:

- 16-bit timer/counter mode
- 16-bit capture mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

The timer/counter 5 can be a divided clock of a system clock selected from prescaler output. The clock source is selected by clock selection logic controlled by clock selection bits (T5CK[2:0]).

- TIMER 5 clock source: fx/1, fx/2, fx/4, fx/8, fx/32, fx/128, fx/512 and HSIRC

In capture mode, data is captured into input capture data registers (T5BDRH/T5BDRL) by EINT45. In timer/counter mode, whenever counter value is equal to T5ADRH/L, T5O port toggles. In addition, TIMER 5 outputs PWM waveform to PWM5O port in the PPG mode.

Table 15. TIMER 5 Operating Modes

T5EN	P0FSRH[5:4]	T5MS[1:0]	T5CK[2:0]	TIMER 5
1	11	00	XXX	16-bit Timer/Counter Mode
1	00	01	XXX	16-bit Capture Mode
1	11	10	XXX	16-bit PPG Mode (one-shot mode)
1	11	11	XXX	16-bit PPG Mode (repeat mode)

16-bit Timer/Counter Mode

16-bit timer/counter mode is selected by control registers, and the 16-bit timer/counter has counter registers and data registers as shown in Figure 54. The counter register is increased by internal clock input.

Timer 5 can use the input clock with one of 1, 2, 4, 8, 32, 128, 512 and High Frequency Internal Oscillator (HSIRC) prescaler division rates (T5CK[2:0]). When the values of T5CNTH/T5CNTL and T5ADRH/T5ADRL are identical to each other in timer 5, a match signal is generated, and the interrupt of Timer 5 occurs. The T5CNTH/T5CNTL values are automatically cleared by match signal. It can be cleared by software (T5CC) too.

Figure 54. 16-bit Timer/Counter Mode for Timer 5

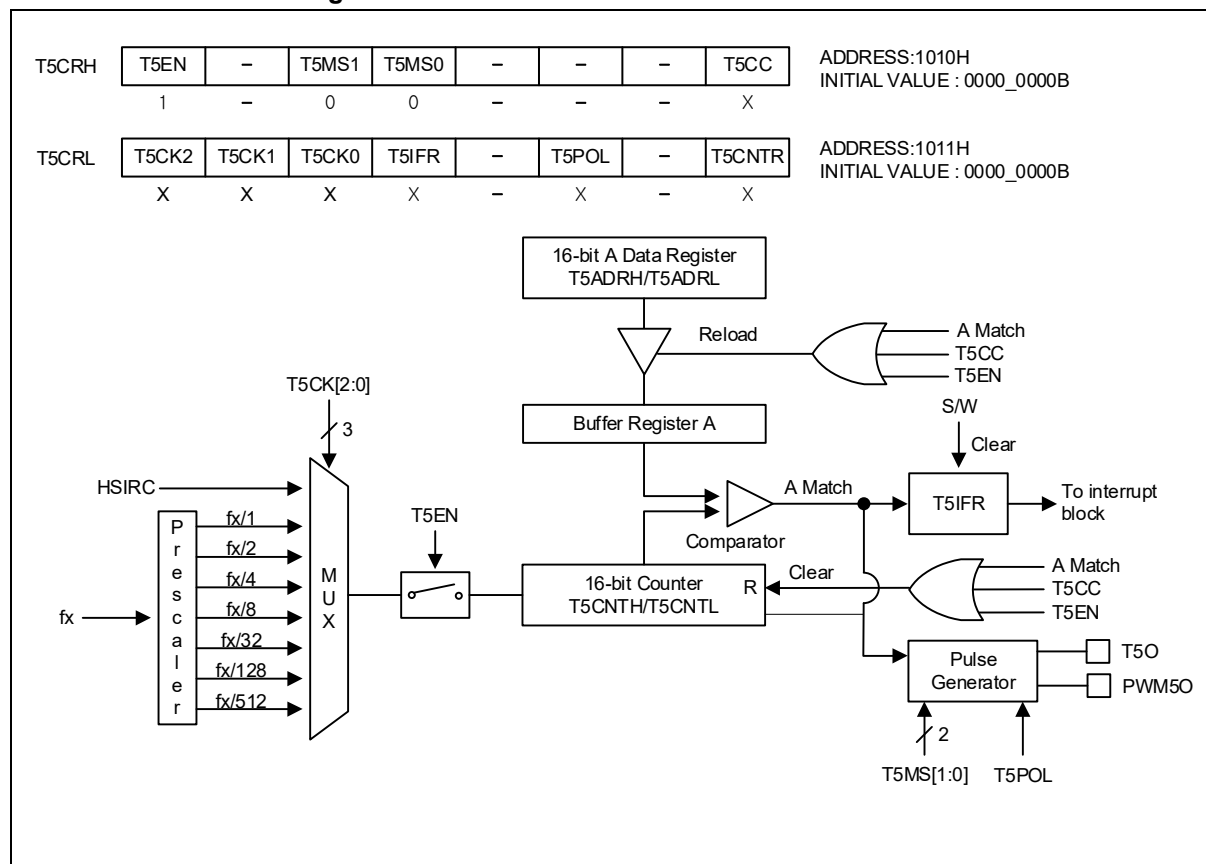
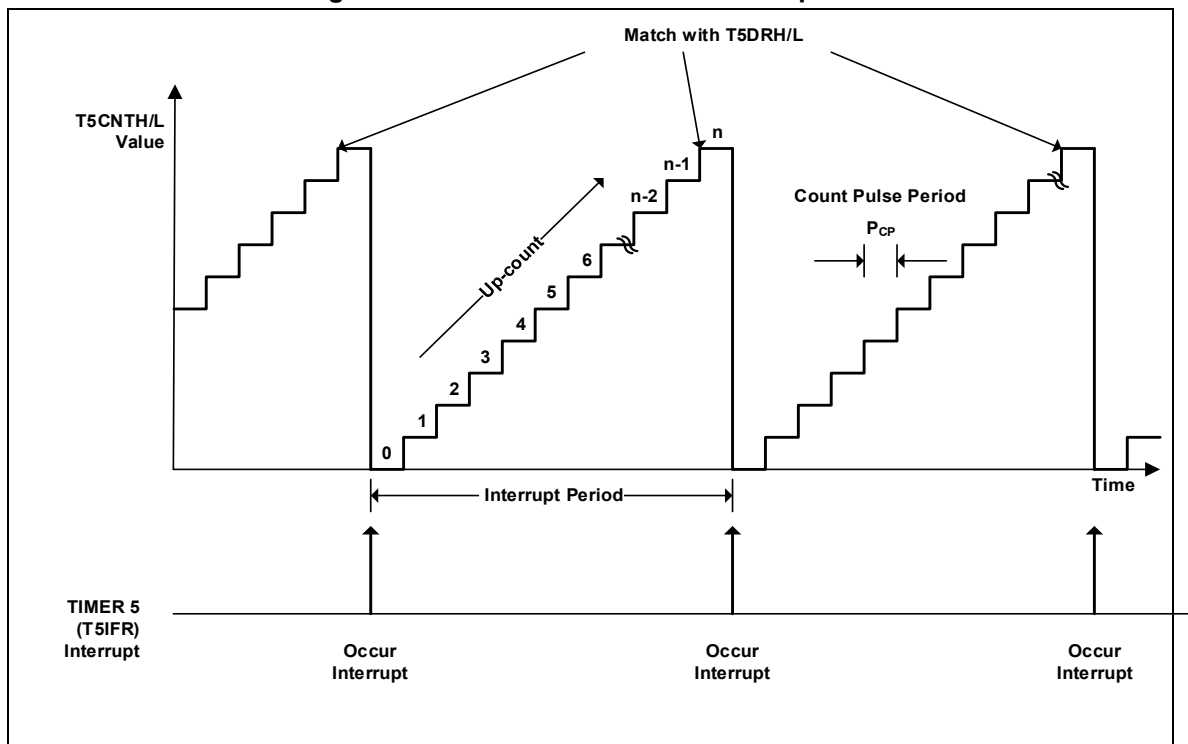


Figure 55. 16-bit Timer/Counter 5 Example



16-bit Capture Mode

Timer 5 capture mode is set by configuring T5MS[1:0] as '01'. It uses an internal clock as a clock source. Basically, the 16-bit timer 5 capture mode has the same function as the 16-bit timer/counter mode, and the interrupt occurs when T5CNTH/T5CNTL is equal to T5ADRH/T5ADRL. The T5CNTH, T5CNTL values are automatically cleared by a match signal. It can be cleared by software (T5CC) too.

A timer interrupt in capture mode is very useful when the pulse width of captured signal is wider than the maximum period of timer. Capture result is loaded into T5BDRH/T5BDRL. In the timer 5 capture mode, timer 5 output (T5O) waveform is not available.

According to EIPOL0H registers setting, the external interrupt EINT45 function is selected. EINT45 pin must be set as an input port.

Figure 56. 16-bit Capture Mode for Timer 5

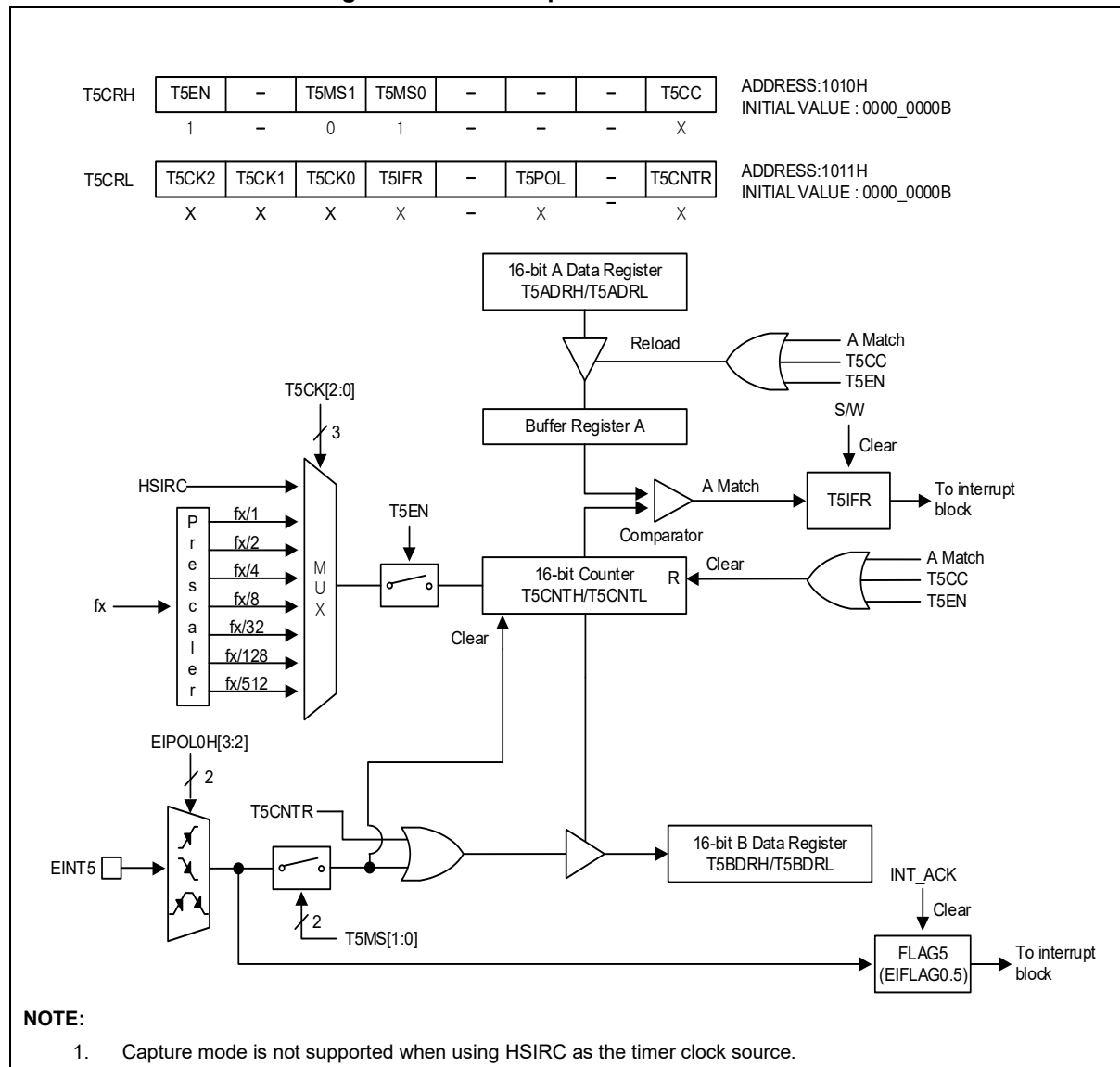


Figure 57. Input Capture Mode Operation for Timer 5

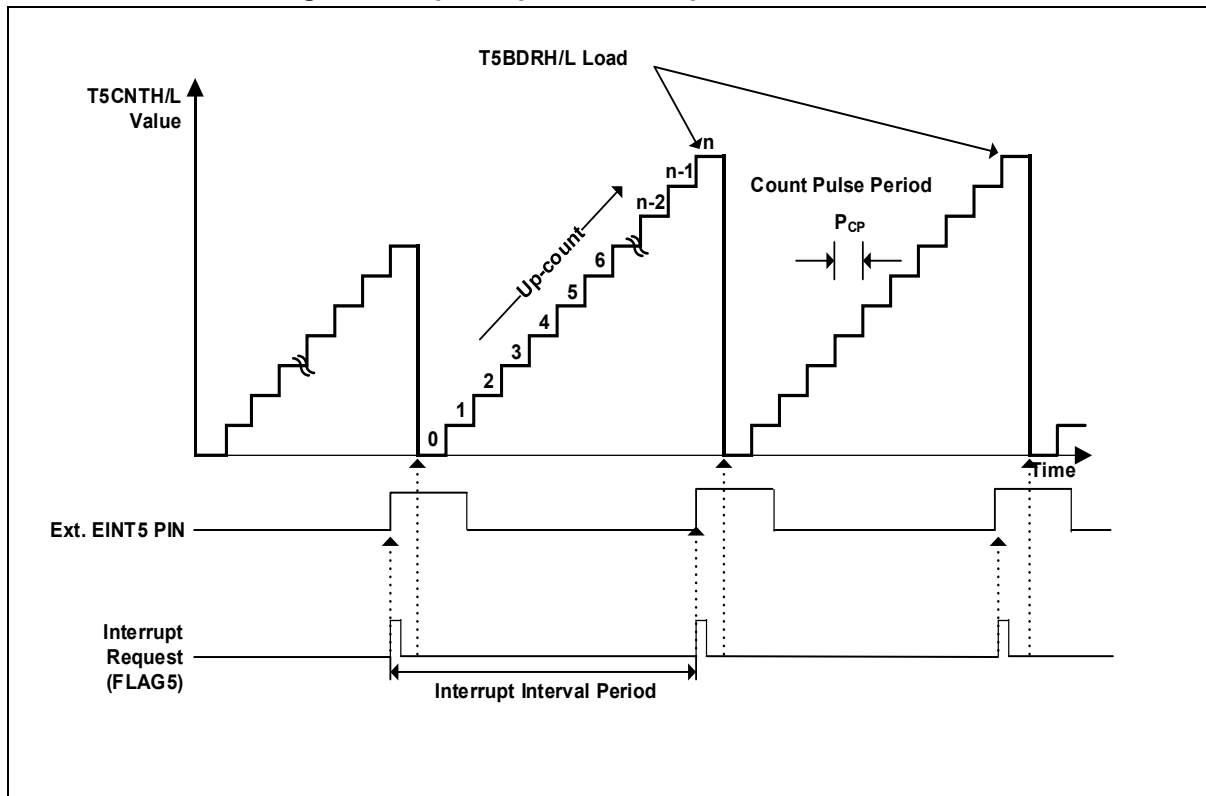
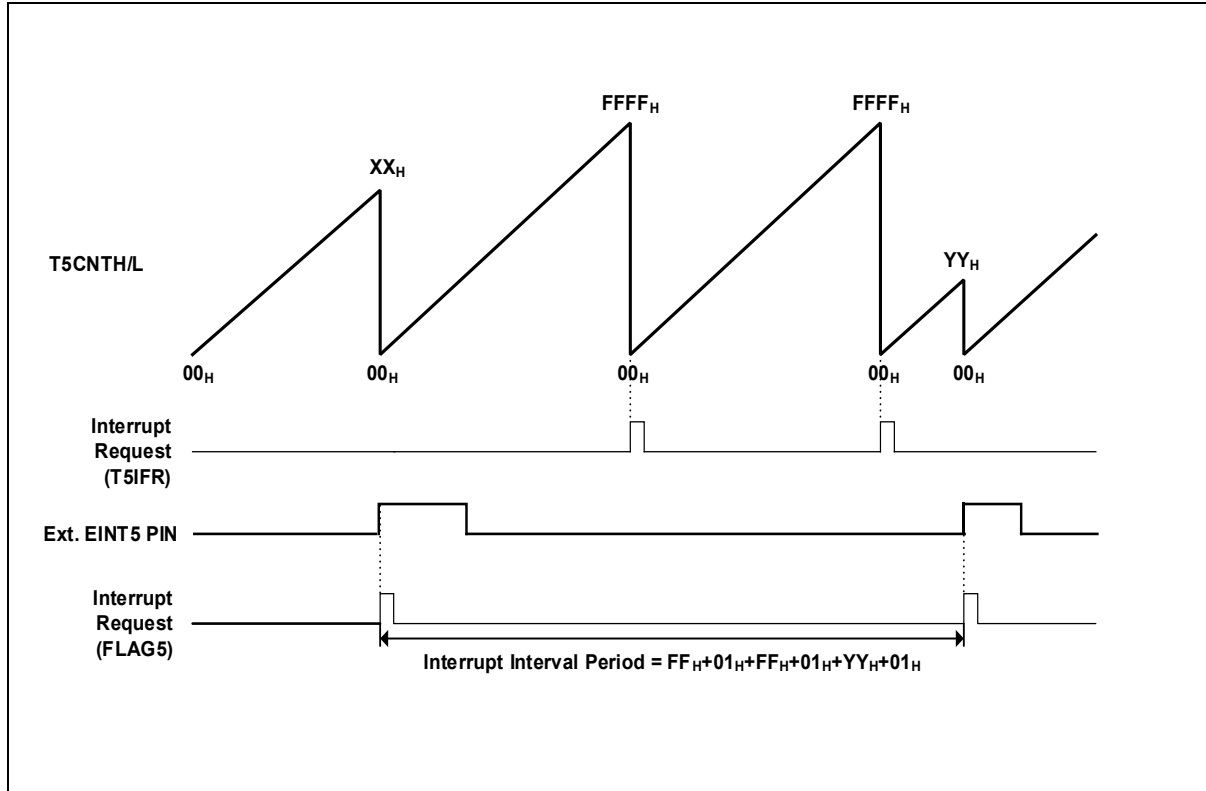


Figure 58. Express Timer Overflow in Capture Mode



16-bit PPG Mode

TIMER 5 has a PPG (Programmable Pulse Generation) function. In PPG mode, T5O/PWM5O pin outputs up to 16-bit resolution PWM output. For this function, T5O/PWM5O pin must be configured as a PWM output by setting P2FSRH[5:4] to '10'.

The period of the PWM output is determined by T5ADRH/T5ADRL, and duty of the PWM output is determined by T5BDRH/T5BDRL.

Figure 59. 16-bit PPG Mode for Timer 5

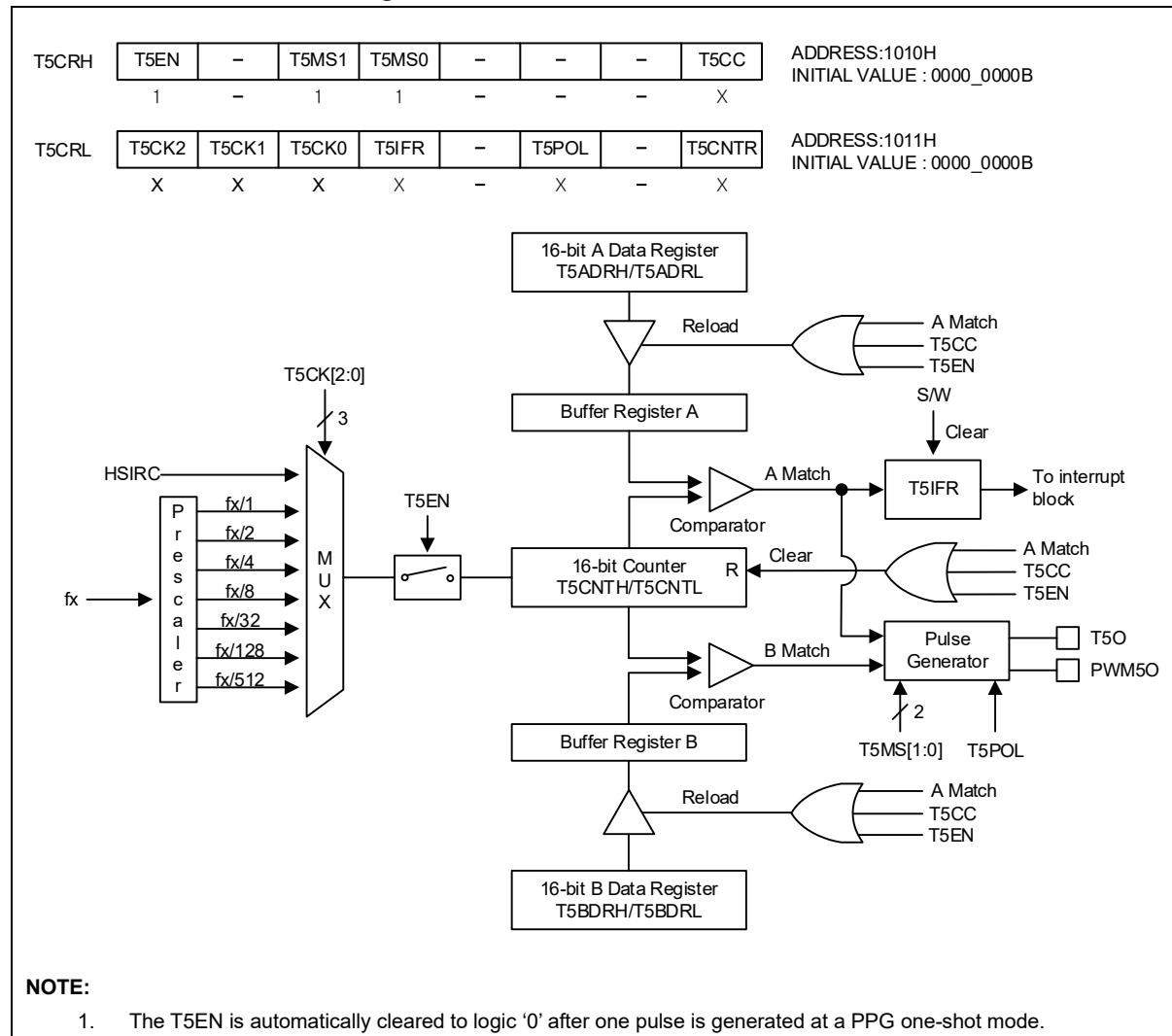
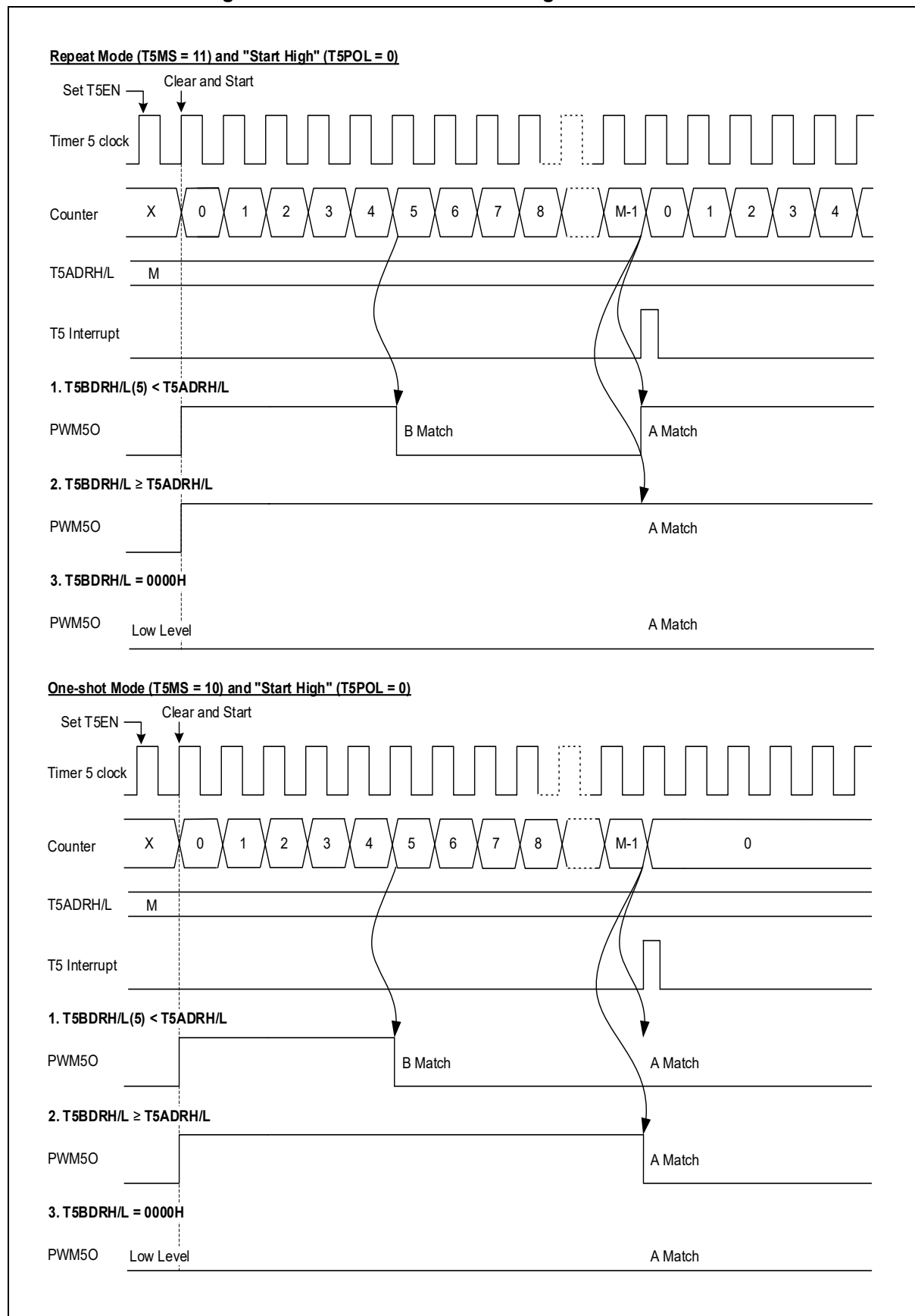
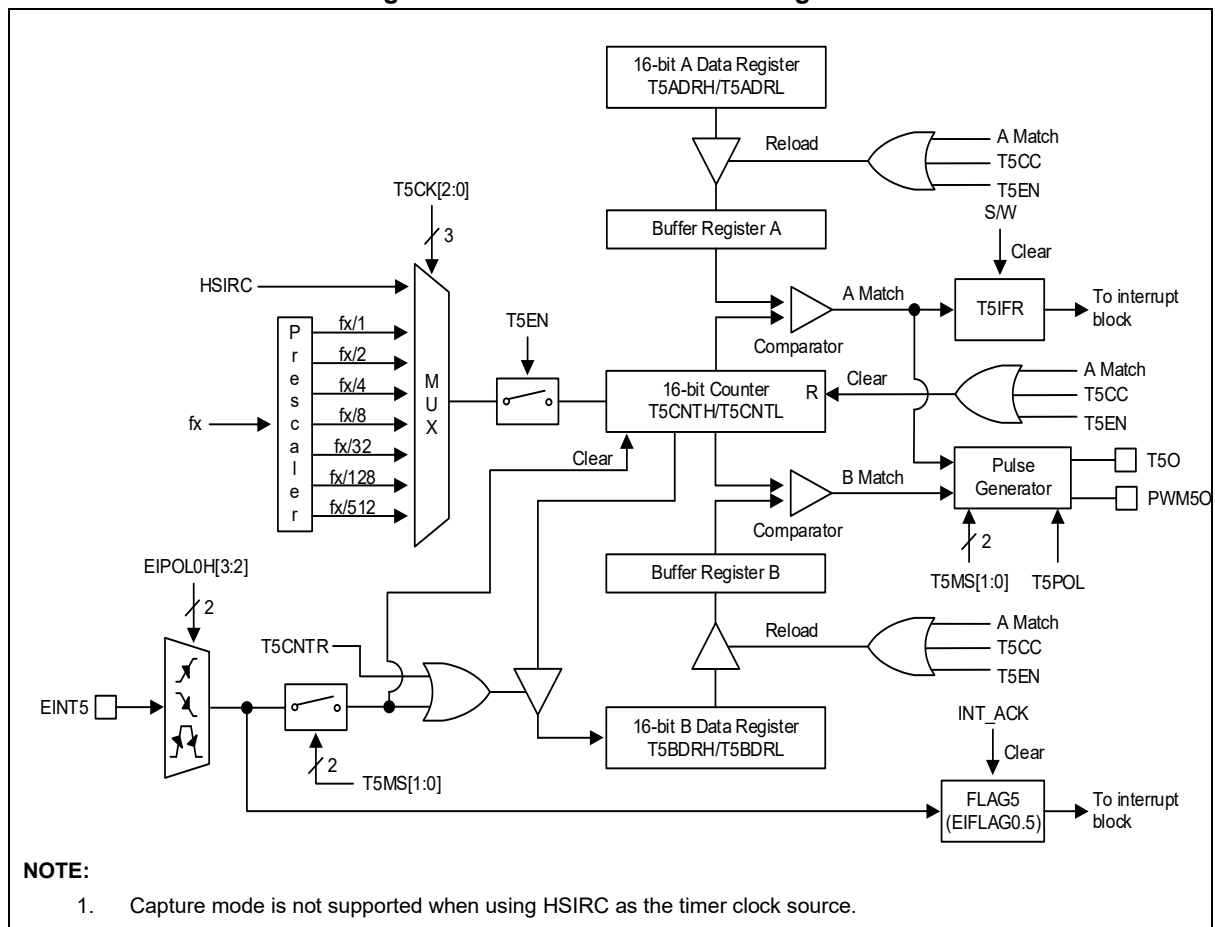


Figure 60. 16-bit PPG Mode Timing Chart for Timer 5

Block Diagram**Figure 61. 16-bit Timer 5 Block Diagram**

2.4.10 Buzzer Driver

Buzzer of the A96T430 consists of 8-bit counter, a buzzer data register (BUZDR), and a buzzer control register (BUZCR). It outputs square wave (61.035 Hz to 125.0 kHz @ 8 MHz) through P53/BUZO pin, and its buzzer data register (BUZDR) controls the buzzer frequency (refer to the following expression). In a buzzer control register (BUZCR), BUCK[1:0] bits select a source clock divided by prescaler.

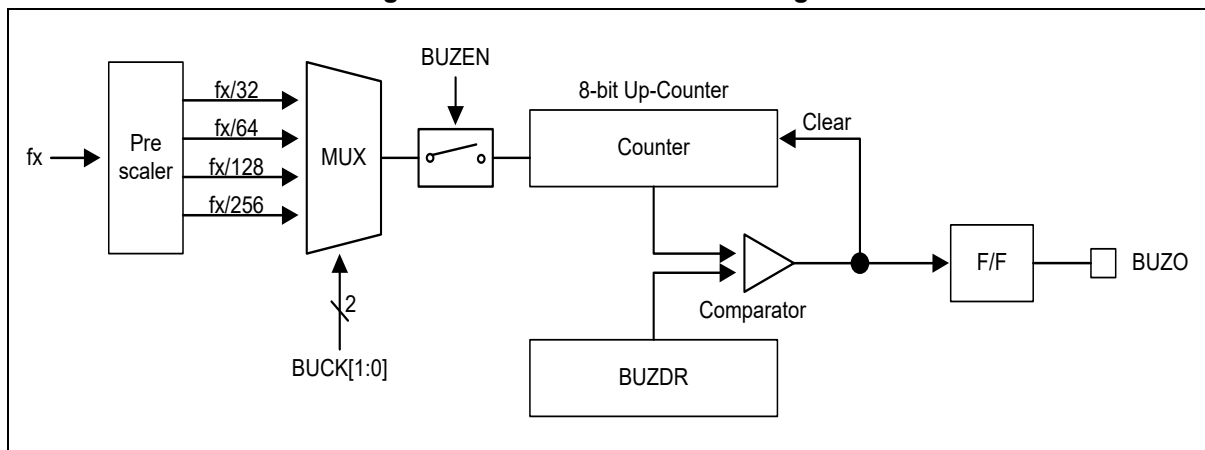
$$f_{\text{Buz}} [\text{Hz}] = \frac{\text{Oscillator Frequency}}{2 \times \text{PrescalerRatio} \times (\text{BUZDR} + 1)}$$

Table 16. Buzzer Frequency at 8 MHz

BUZDR[7:0]	Buzzer Frequency (kHz)			
	BUZCR[2:1]=00	BUZCR[2:1]=01	BUZCR[2:1]=10	BUZCR[2:1]=11
0000_0000	125 kHz	62.5 kHz	31.25 kHz	15.625 kHz
0000_0001	62.5 kHz	31.25 kHz	15.625 kHz	7.812 kHz
...	...	...	...	...
1111_1101	492.126 Hz	246.063 Hz	123.031 Hz	61.515 Hz
1111_1110	490.196 Hz	245.098 Hz	122.549 Hz	61.274 Hz
1111_1111	488.281 Hz	244.141 Hz	122.07 Hz	61.035 Hz

2.4.10.1 Block Diagram

Figure 62. Buzzer Driver Block Diagram



2.4.11 USI

USI stands for Universal Serial Interface, the combination of USART, SPI and I2C. The A96T430 has a USI0. USI consists of USI control registers 1/2/3/4, USI status registers 1/2, USI baud-rate generation register, USI data register, USI SDA hold time register, USI SCL high period register, USI SCL low period register, and USI slave address register (USInCR1, USInCR2, USInCR3, USInCR4, USInST1, USInST2, USInBD, USInDR, USInSDHR, USInSCHR, USInSCLR, USInSAR). The 'n' means '0'.

USI operates in one of the following modes selected by USIn selection bits (USInMS[1:0]):

- Asynchronous mode (UART)
- Synchronous mode (USART)
- SPI mode
- I2C mode

2.4.11.1 USI UART Mode

Universal synchronous and asynchronous serial receiver and transmitter (USART) are highly flexible serial communication devices. Key features are listed below:

- Full Duplex Operation (Independent Serial Receive and Transmit Registers.)
- Asynchronous or Synchronous Operation.
- Baud Rate Generator.
- Supports Serial Frames with 5,6,7,8, or 9 Data bits and 1 or 2 Stop bits.
- Odd- or Even-Parity Generation and Parity Check are supported by hardware.
- Data Over Run Detection.
- Framing Error Detection.
- Three Separate Interrupts on TX Completion, TX Data Register Empty and RX Completion.
- Double Speed Asynchronous communication mode.

The USI comprises clock generator, transmitter and receiver. Clock generation logic consists of synchronization logic for external clock input used by synchronizing or SPI slave operation, and the baud rate generator for asynchronous or master (synchronous or SPI) operation.

Transmitter consists of a single write buffer, a serial shift register, parity generator and control logic for handling different serial frame formats. A write buffer allows continuous transfer of data without any delay between frames.

Receiver is the most complex part of the UART module due to its clock and data recovery units. The recovery unit is used for asynchronous data reception. In addition to the recovery unit, the receiver includes a parity checker, a shift register, a two-level receive FIFO (USInDR) and control logic. The receiver supports the same frame formats as the transmitter and can detect frame errors, data overrun and parity errors.

2.4.11.2 USI SPI Mode

The USI can be set to operate in industrial standard SPI compliant mode. The SPI mode has the following features.

- Full Duplex, Three-wire synchronous data transfer
- Master and Slave Operation
- Supports all four SPI modes of operation (mode 0, 1, 2, and 3)
- Selectable LSB first or MSB first data transfer
- Double buffered transmit and receive
- Programmable transmit bit rate

When SPI mode is enabled (USInMS[1:0]=11), the slave select (SSn) pin becomes active LOW input in slave mode operation or can be output in master mode operation if USInSEN bit is set to '0'.

Note that during SPI mode of operation, the pin RXDn is renamed as MISOn and TXDn is renamed as MOSIn for compatibility to other SPI devices.

2.4.11.3 USI I2C Mode

The USI can be set to operate in industrial standard serial communication protocols mode. The I2C mode uses two bus lines for a serial data line (SDAn) and a serial clock line (SCLn) to exchange data. Because both SDAn and SCLn lines are open-drain output, each line needs pull-up resistor. The features are as shown below.

- Compatible with I2C bus standard
- Multi-master operation
- Up to 400 kHz data transfer read speed
- 7-bit address
- Both master and slave operation
- Bus busy detection

2.4.12 USART

Universal Synchronous and Asynchronous serial Receiver and Transmitter (USART) is a highly flexible serial communication device. USART of the A96T430 features the following:

- Full-Duplex Operation (Independent Serial Receive and Transmit Registers)
- Asynchronous or Synchronous Operation
- Master or Slave Clocked Synchronous and SPI Operation
- Supports all four SPI Modes of Operation (Mode 0, 1, 2, 3)
- LSB First or MSB First Data Transfer @SPI mode
- High Resolution Baud Rate Generator
- Supports Serial Frames with 5,6,7,8, or 9 Data bits and 1 or 2 Stop bits
- Odd or Even Parity Generation and Parity Check Supported by Hardware
- Data Over Run Detection
- Framing Error Detection
- Digital Low Pass Filter
- Three Separate Interrupts on TX Complete, TX Data Register Empty and RX Complete
- Double Speed Asynchronous Communication Mode

USART has three main parts, such as Clock Generator, Transmitter and Receiver.

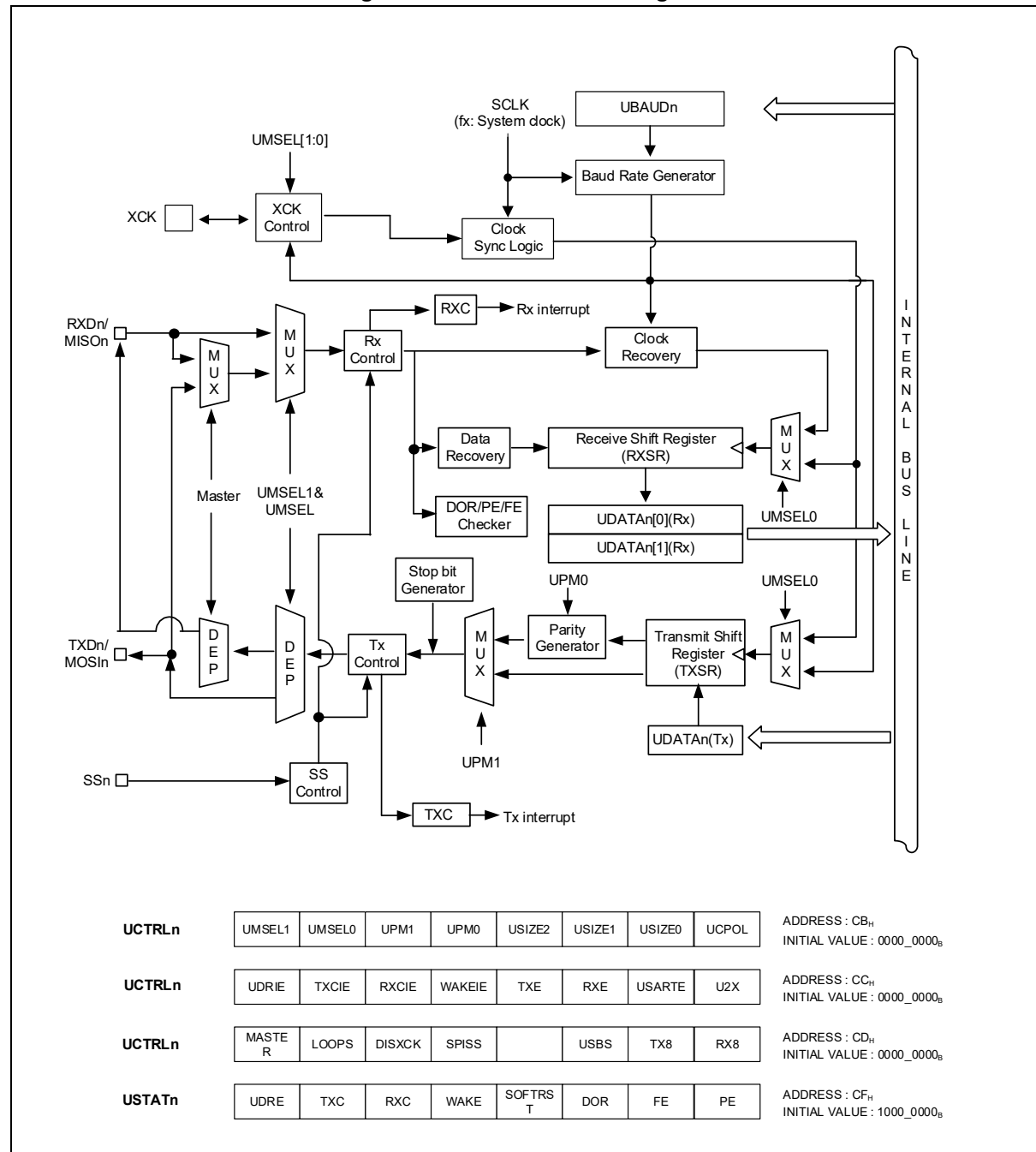
Clock Generation logic consists of a synchronization logic for external clock input used by synchronous or SPI slave operation, and a baud rate generator for asynchronous or master (synchronous or SPI) operation.

Transmitter consists of a single write buffer, a serial shift register, parity generator and control logic for handling different serial frame formats. Write buffer allows a continuous transfer of data without any delay between frames.

Receiver is the most complex part of the USART module due to its clock and data recovery units. Recovery unit is used for asynchronous data reception. In addition to the recovery unit, the Receiver includes a parity checker, a shift register, a two level receive FIFO (UDATAN) and control logic. The Receiver supports the same frame formats as the Transmitter and can detect Frame Error, Data OverRun and Parity Errors.

2.4.12.1 Block Diagram

Figure 63. USART1 Block Diagram



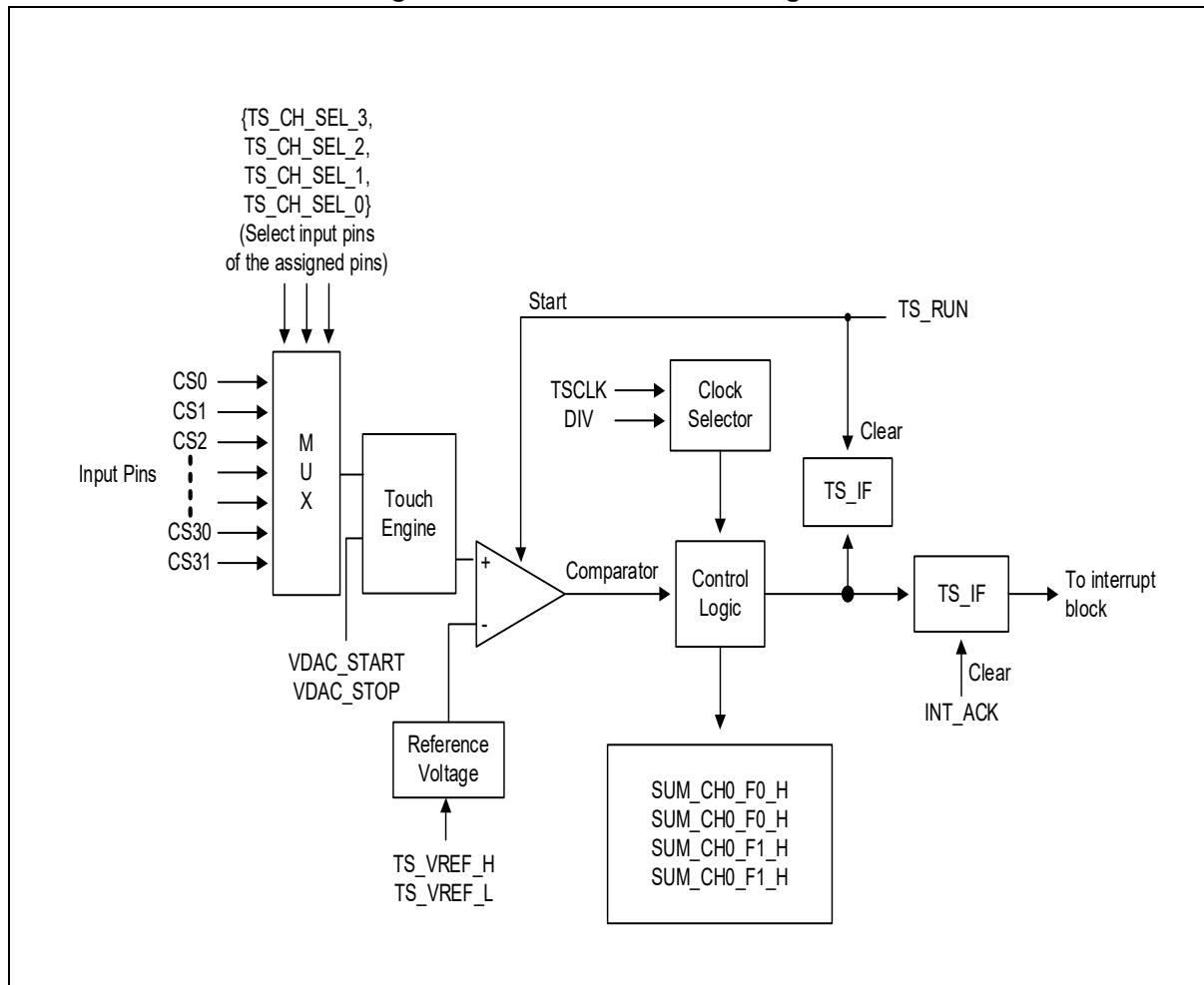
2.4.13 Self-Capacitive Touch Sensor

2.4.13.1 Features

- 10 V Conducted Susceptibility (CS) Immunity
- Self-Capacitive Touch Key Sensor.
- Total 32-channel Touch Key Support.
- 16-bits Sensing Resolutions.
- Fast Initial Self Calibration.
- Key Detection Mode: Single/Multi-Mode.
- Clock Frequency during Sensing Operation: 16 MHz.
- The Improvement of the SNR by Bias-Calibration in Analog Sensing Block.
- VDD Operating Voltage: 2.7 V to 5.5 V.
- Current Consumption: 800 μ A
- Current Consumption at STOP mode: under 1 μ A.
- Operation Temperature: -40°C to 105°C.

2.4.13.2 Block Diagram

Figure 64. 16-bit Touch Block Diagram



2.4.13.3 CAPN Port

Connect the negative terminal of the reference capacitor C_s to CAPN port, and the positive terminal of the C_s capacitor to VDD. C_s capacitors must use 5% precision polyester plug-in capacitors, 10% high precision NPO or X7R chip capacitors. C0G type or Mylar Capacitors are recommended for applications with severe temperature changes.

Figure 65. CAPN Pin with C_s Capacitor (VDD)

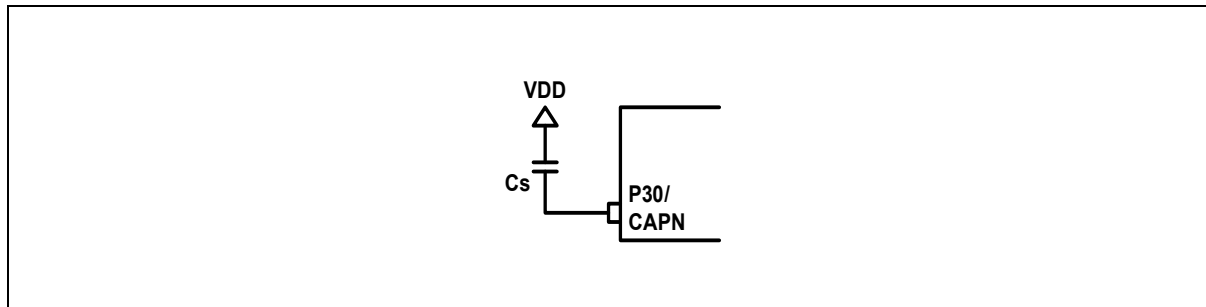
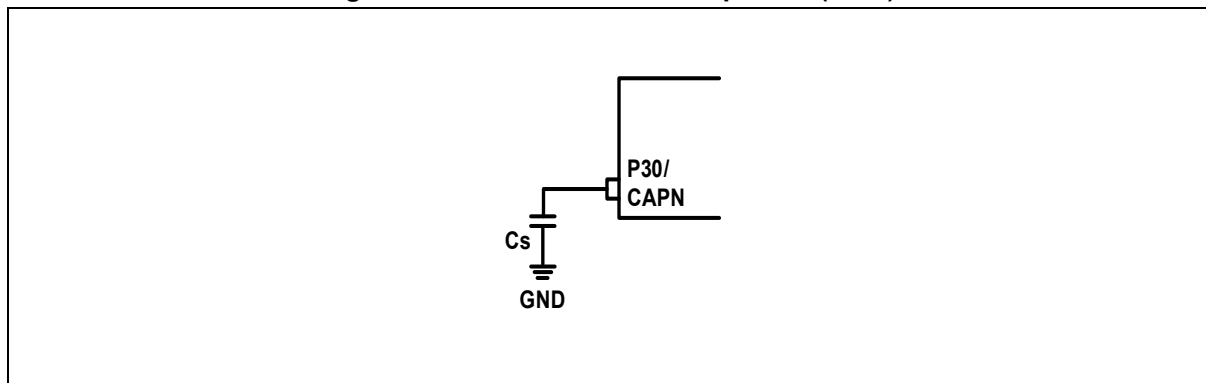


Figure 66. CAPN Pin with C_s Capacitor (GND)



2.4.14 12-bit ADC

The analog-to-digital converter (ADC) allows conversion of an analog input signal to corresponding 12-bit digital value.

The ADC module has eight analog inputs. The output of the multiplexer is the input into the converter which generates the result through successive approximation. The ADC module has four registers which are the ADC control high register (ADCCRH), ADC control low register (ADCCRL), ADC data high register (ADCDRH), and ADC data low register (ADCDRL). The channels to be converted are selected by setting ADSEL[3:0]. To execute A/D conversion, TRIG[2:0] bits should be set to 'xxx'. The register ADCDRH and ADCDRL contains the results of the A/D conversion.

When the conversion is completed, the result is loaded into the ADCDRH and ADCDRL, the A/D conversion status bit AFLAG is set to '1', and the A/D interrupt is set. During A/D conversion, AFLAG bit is read as '0'.

2.4.14.1 Conversion Timing

- ADC operates at typical, MCLK = 8 MHz, Sampling rate = 380 ksps.
- Conversion Time consists of 16-cycle + TSMP + 1-cycle (margin) by default.
- TSMP is Default setting (0x02) which covers four cycles and consists of a typical total of 21 cycles.
- TSMP is 0x02 = 4-cycle; +1-cycle increases as TSMP increases +1-cycle.
- ADC Conversion Time = $ADCLK \times (16\text{-cycle} + TSMP + 1)$

2.4.14.2 Block Diagram

Figure 67. 12-bit ADC Block Diagram

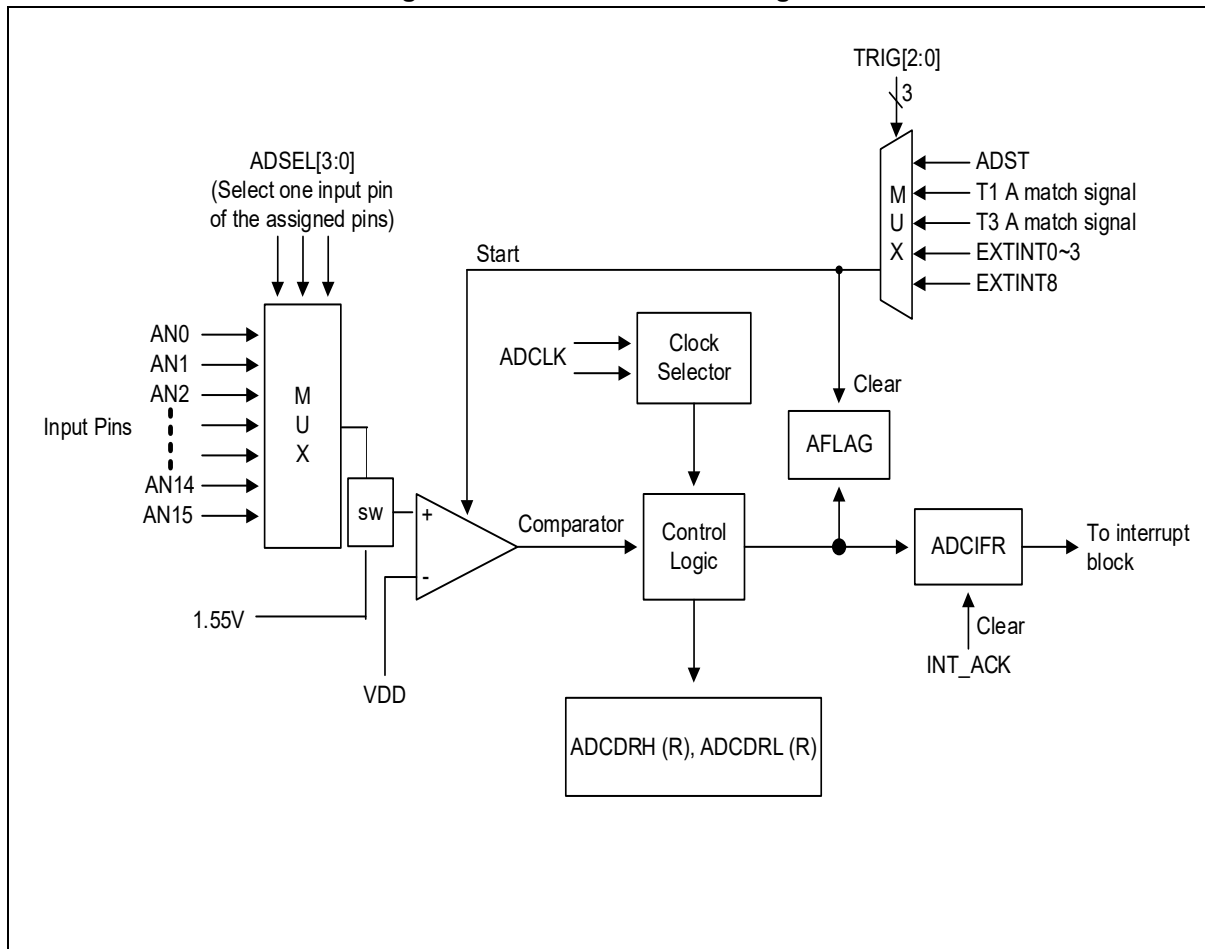
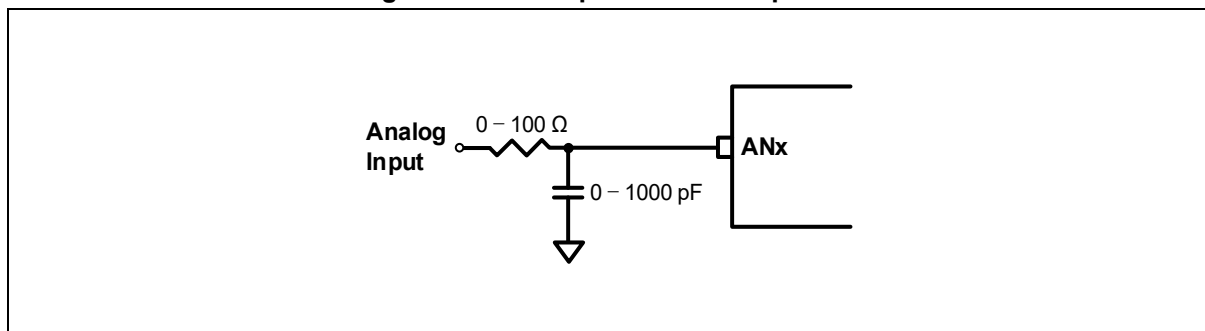


Figure 68. ADC Input Pin with Capacitor



2.4.15 Power-Down Operation

The A96T430 has two power-down modes to minimize the power consumption of the device. In power down mode, power consumption is reduced considerably. The device provides three kinds of power saving functions, Main-IDLE, and STOP mode. In three modes, the program stopped.

2.4.15.1 Peripheral Operation in IDLE/STOP Mode

Table 17. Peripheral Operation During Power-Down Mode

Peripheral	IDLE Mode	STOP Mode
CPU	ALL CPU Operation are Disable	ALL CPU Operation are Disable
RAM	Retain	Retain
Basic Interval Timer	Operates Continuously	Stop (can be operated with WDTRC OSC)
Watchdog Timer	Operates Continuously	Stop (can be operated with WDTRC OSC)
Watch Timer	Operates Continuously	Stop (can be operated with WDTRC OSC)
Timer0 to 4	Operates Continuously	Halted (only when the Event Counter Mode is Enabled, Timer operates Normally)
ADC	Operates Continuously	Stop
BUZ	Operates Continuously	Stop
USI0/1	Operates Continuously	Only operate with external clock
Internal OSC (16 MHz)	Oscillation	Stop when the system clock (fx) is Power down mode
WDTRC OSC (32 kHz)	Can be operated with setting value	Can be operated programmable
Touch OSC (16 MHz)	Oscillation	Stop when the system clock (fx) is Power down mode
I/O Port	Retain	Retain
Control Register	Retain	Retain
Address Data Bus	Retain	Retain
Release Method	By RESET, all Interrupts	By RESET, Timer Interrupt (EC0, EC1, EC3), External Interrupt, USART by RX, WT, WDT USI0/1 by RX, I2C (Slave mode)

2.4.16 RESET

The following is the hardware setting value.

Table 18. Reset State

On-Chip Hardware	Initial Value
Program Counter (PC)	0000h
Accumulator	00h
Stack Pointer (SP)	07h
Peripheral Clock	On
Control Register	Initial value of registers

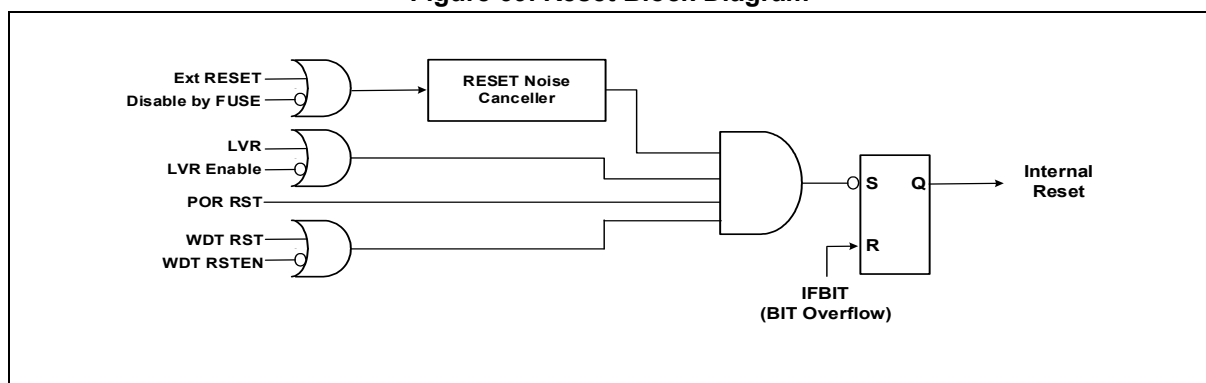
2.4.16.1 Reset Source

The A96T430 has five types of reset sources. The following are the reset sources.

- External RESETB pin
- Power-On Reset (POR)
- WDT Overflow Reset (In the case of WDTEN = 1)
- Low-Voltage Reset (In the case of LVREN = 0)
- OCD (On-Chip Debug) Reset

2.4.16.2 Reset Block Diagram

Figure 69. Reset Block Diagram



2.4.17 Memory Programming

The A96T430 has flash memory to which a program can be written, erased, and overwritten while mounted on the board. Serial ISP mode is supported.

The flash memory of the A96T430 features the following:

- Flash memory size: 64 Kbytes
- Single power supply program and erase
- Command interface for fast program and erase operation
- Up to 10,000 program/erase cycles at typical voltage and temperature for flash memory
- Security feature
- Program/erase unit
 - Program unit: 32 bits
 - Erase unit: 512 bytes for a page, 2 KB for a sector, 64 KB for bulk erase
- Program or erase operation time
 - Program time: 25 μ s
 - Erase time: 2 ms for each page or for each sector and 8 ms for bulk erase
- Read access time: 30 ns

2.4.17.1 Flash Control and Status Register

Registers to control Flash and Data EEPROM are Mode Register (FEMR), Control Register (FEER), Status Register (FESR), Address Low Register (FEARL), Address Middle Register (FEARM). They are mapped to SFR area and can be accessed only in programming mode.

2.4.17.2 Memory Map

Flash Memory Map

Program memory uses 64 KB of Flash memory. It is read by byte and written by 1-word. One page is 512-byte.

Figure 70. Flash Memory Map

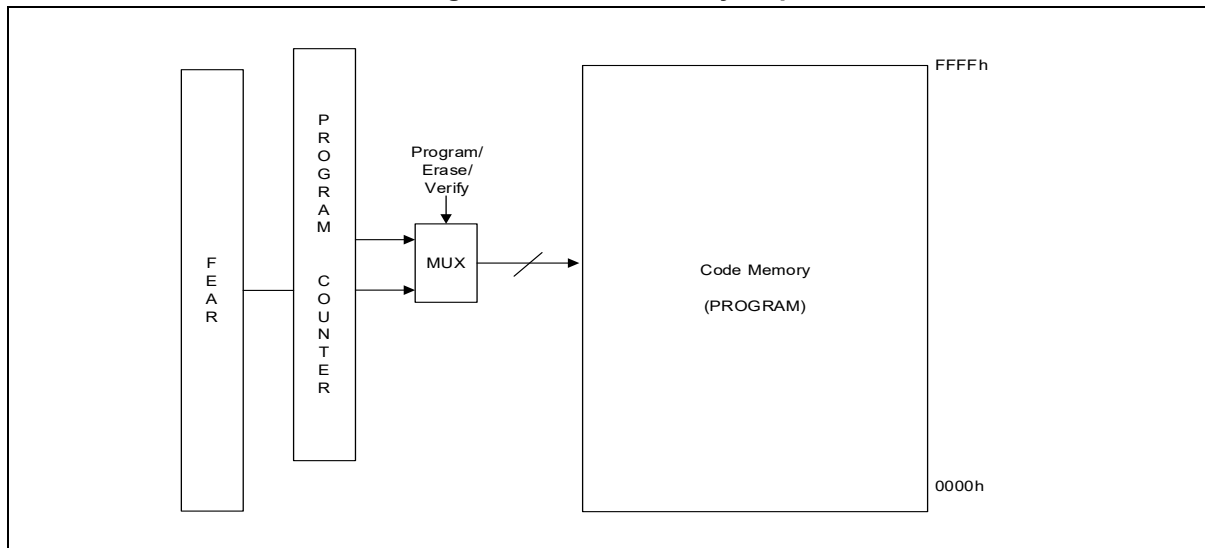
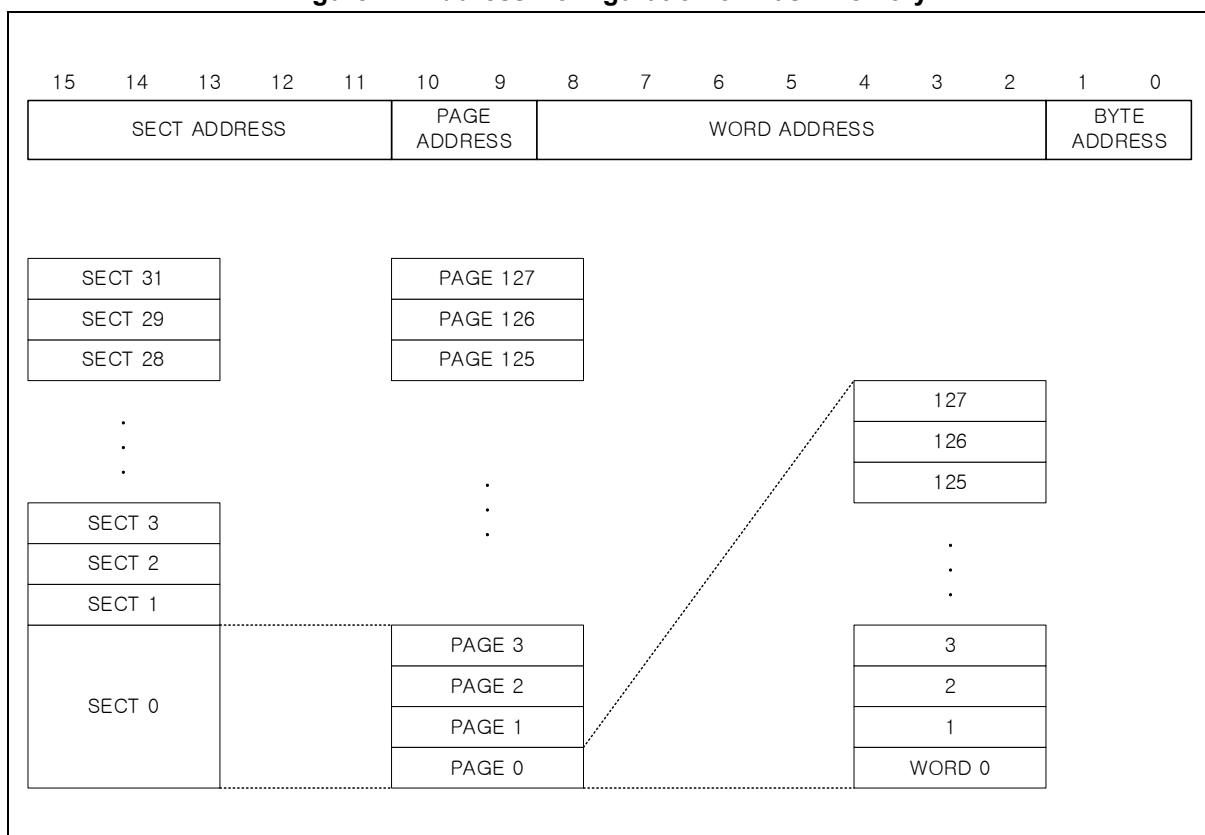


Figure 71. Address Configuration of Flash Memory



2.5 Debug Interface

The A96T430 uses OCD (On-Chip Debugger) interface for debugging, which is ABOV's own interface. The OCD monitors and controls the core and supports the read and write operations of external memory and devices. In addition, it supports memory monitoring and break functions.

Debug interface such as an OCD interface enables a microcontroller to write on internal programmable memory, thereby, allows it to support ISP (In-System Program) which makes it possible to write as a single chip or as an embedded chip in the system.

Table 19 provides information on the core and debug emulation interface.

Table 19. Core and Debug Information

	Value	Description
Device Name	A96T430	
Series	96 series	
Core	M8051	
Extended Stack Pointer	No	94, 97 series only
Debug Interface	OCD 1	
Number of Break Point	8	
Real-time Monitoring	No	OCD 2 only
Run Flag Port	No	OCD 2 option

2.5.1 Core

The A96T430 contains an M8051/CM8051 core that was made by improving the 8051. The M8051/CM8051 core is compatible with the 8051. It reduces time of operation cycles and makes development easy by providing the OCD debug function.

ABOV's 8-bit microcontroller has a core of 94-series, 96-series, or 97-series, which is basically compatible with the 8051 series at the instruction set level. A core of each series uses different Debug Interface respectively as shown in Table 20.

Table 20. Core and Debug Interface by Series

	Core	Debug Interface
96 Series	M8051	OCD 1
97 Series	M8051	OCD 2
94 Series	CM8051	OCD 2

Features of each series are compared in Table 21.

Table 21. Feature Comparison Chart by Series and Cores

	96 Series	97 Series	94 Series
CPU Core	M8051	M8051	CM8051
Cycle Compatible with MCS51	1/6	1/6	No
OCD Function	OCD 1	OCD 2	OCD 2
Program BUS	8-bit		
Data Bus	8-bit IRAM/XRAM separated		8-bit single SRAM
EA Auto Clear ⁽¹⁾	Yes	Yes	Yes
EA=0, Idle/Stop Mode Wake Up	Yes	Yes	Yes
Interrupt Priority ⁽²⁾	6 group x 4 level	Interrupt x 4 level	Interrupt x 2 level
Nested Interrupt Priority	4 level	4 level	Interrupt x 2 level (max. 4 times)
SFR BUS (Read/Write)	Two ports	Two ports	Single port
Stack Extension	X	O	O
Register	SRAM		
Register Bank	4		
CPU/Flash Clock Ratio	x 1		
Pipeline	No	No	2-stage (IF + ID/EX)
DHRY Stone Score (I8051: 1.00)	6.0	6.0	8.4
Average Instruction Set Exe. Cycle Compare with i8051	x 6.0	x 6.0	x 6.4
Power Consumption/DHRY (@synthesis)	52.27 μ A/MHz	52.27 μ A/MHz	30.19 μ A/MHz

NOTES:

1. EA means that All Interrupt Enable bit or Disable bit (Standard 8051).
2. Group: When a programmer selects a specific interrupt (e.g., Interrupt1), the whole interrupts: 0, 6, 12, and 18 have higher priorities.

ABOV's 8-bit microcontrollers maintain the compatibility of binary levels with 8051 cores; however, the cores and series have differences in performances, functions of the core, and debug interfaces.

The following sections describe the differences between each series.

2.5.1.1 Debug Interface

96-series core uses OCD 1 for a debug interface, while the cores of 94-series and 97-series use OCD 2 for debug interfaces. The OCD 1 and OCD 2 use the same method in hardware, but protocols are not compatible with each other.

In the OCD 2, it is able to measure the emulation time through the “Run Flag” pin.

Table 22. OCD Type of Each Series

Series	96-Series	97-Series	94-Series	Remark
OCD type	OCD 1	OCD 2	OCD 2	

In Table 23, debug interfaces of the OCD 1 and OCD 2 are compared.

Table 23. Comparison of OCD 1 and OCD 2

	Value	Description
OCD 1	Break point MAX.8	PC break only
OCD 2	Break point MAX.12	With RAM break Code, XDATA, IDATA 1/8/16/32bit compare
	Real-time monitoring	Code, XDATA, IDATA
	Frequency output	Examine CPU frequency
	Run Flag port	Option for run-time measurement

96 Series – OCD 1

This series supports basic operations such as Run, Stop, Step, Break point, register reading/writing, Memory reading/writing, and SFR reading/writing.

94 Series and 97 Series – OCD 2

This series supports the features of the OCD 1 and the features listed below (however, the protocol is not compatible with the OCD1):

- RTM support: CODE, XDATA, IDATA are updated during the Run Time (Real Time Monitoring available).
- Run Flag support: Emulation Time can be measured in OCD mode (using the Run Flag port).
- RAM Break support: IDATA, SFR, and XDATA break are added.

2.5.1.2 Interrupt Priority

In the M8051, users can set interrupt priorities by group. Thus, the 96-series microcontroller with the basic M8051 core only supports interrupt priorities in group units.

In the 94-series or 97-series microcontroller, users can set interrupt priorities to have more functions than the existing functions and set individual priority over each interrupt source.

Table 24. Interrupt Priorities in Groups and Levels

Series	96-Series	97-Series	94-Series	Remark
Interrupt priority	6 grouped 4 level	Fully 4 level	Fully 4 level	96 series: IP/IP (Interrupt Priority Register) 94, 97 series: IPxL/IPxH (Interrupt Priority Register)

96 Series

- The priorities by groups are available only with IP/IP1 settings.
- With IP/IP1 settings, users can set interrupt priorities by group unit.
- The interrupt priority of a group unit (4 interrupts in a group) can be changed to the level between 0 and 3 according to the value of IP/IP1.

94, 97 Series

- The individual interrupt priority can be set by setting IPxL/IPxH(x=0 to 3).
- The individual interrupt priority can be changed to the level between 0 and 3 according to the value of IPxL/IPxH (x=0 to 3).

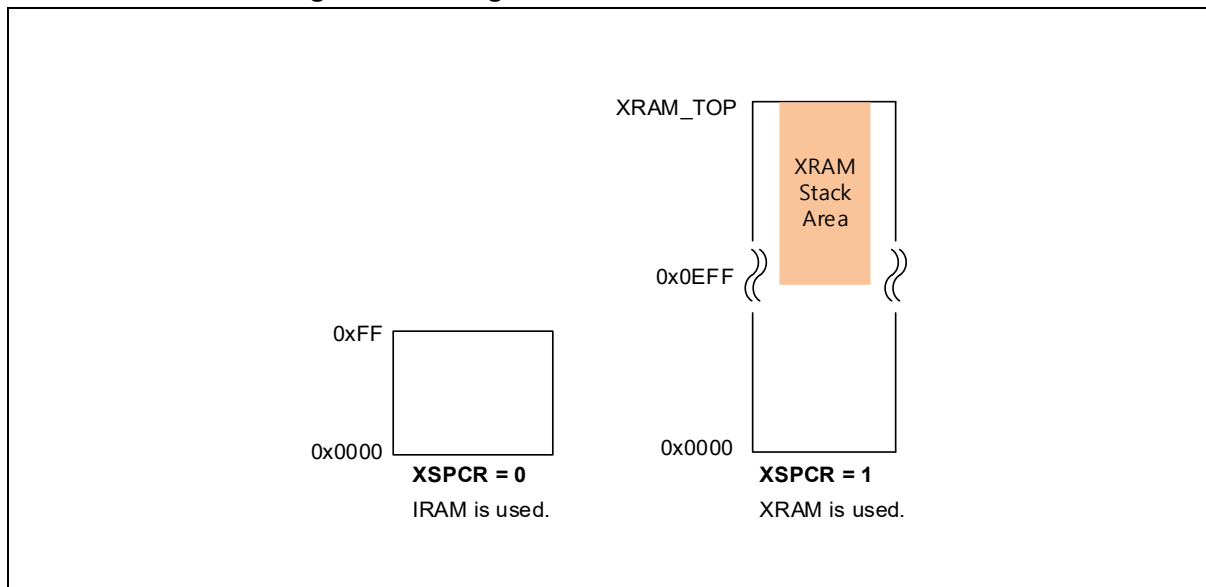
2.5.1.3 Extended Stack Pointer

M8051 uses IRAM area for Stack Pointer. However, 94-series and 97-series microcontrollers use not only IRAM area but also XRAM area for Stack Pointer by configuring additional registers.

The setting procedure is as follows:

1. Configure the XSP/XSPCR registers to use the XRAM area as the Stack Pointer.
2. The XSPCR decides whether to use XRAM for Stack Pointer.
 - A. If XSPCR = '0', IRAM is available for Stack Pointer.
 - B. If XSPCR = '1', XRAM is available for Stack Pointer.
3. The XSP decides the position of XRAM Stack Pointer.
 - A. This is valid only if XSPCR = '1'.

Figure 72. Configuration of Extended Stack Pointer



$$\text{STACK_POINTER} = \{\text{XSP}[7:0], \text{SP}[7:0]\} = \text{XRAM_TOP} - \text{STACK_SIZE}$$

Example) If only 256 bytes of XRAM will be used for stack,

- XRAM_TOP = 4 KB (0x0FFF)
- STACK_SIZE = 256 byte (0x0100)
- XSPCR = 1, XSP = 0x0E
- SP = 0xFF setting
- Stack Pointer Position = 0x0FFF - 0x0100 = 0x0EFF

2.5.2 OCD (On-Chip Debugger) Emulator and Debugger

Microcontroller series that uses an 8051 core has an OCD (On-Chip Debugger), and a debug emulation block. The OCD is connected to a target microcontroller using two lines such as DSCL and DSDA. DSCL is for a clock signal and DSDA is for a bi-directional data.

The two lines work for the core management and control by doing register management and execution, step execution, break point and watch functions. In addition, they control and monitor the internal memory and the device by reading and writing.

Table 25. Debug Feature by Series

Series Name	96-Series	97-Series	94-Series
OCD function	OCD 1	OCD 2	OCD 2
Max. number of breakpoint	8	8	4
Saving stack in XRAM	No	Yes	Yes
Real time monitoring	No	Yes	Yes
Run flag support	No	Yes	Yes

The OCD 2 applied to 94-series and 97-series provides the RTM (Real-time Monitoring) function that enables to monitor internal memory and I/O status without stopping the debugging. In addition, the OCD 2 provides the breakpoint function (RAM Break Function) for the IDATA, SFR, and XDATA.

The following are the functions that have been extended from OCD 2:

- Emulation Time can be measured in OCD mode (using the Run Flag port)
- CODE, XDATA, IDATA are updated during run-time (Real Time Monitoring available).
- IDATA, SFR, XDATA breaks are added (RAM Break support).

Figure 73 shows the standard 10-pin connector of OCD 1 and OCD 2.

Figure 73. OCD 1 and OCD 2 Connector Pin Diagram

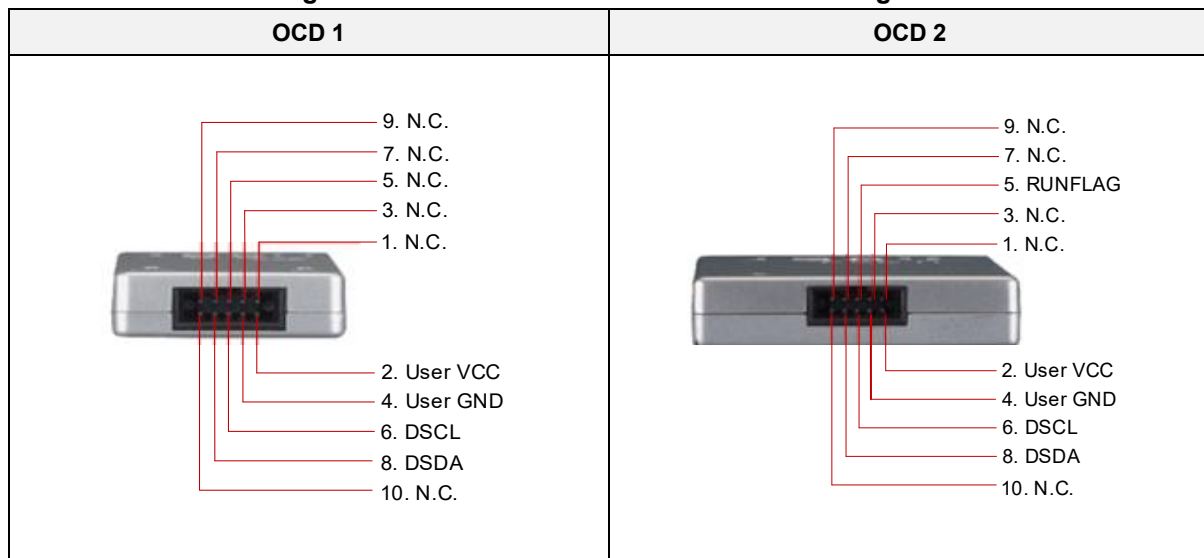


Table 26 describes pins used for OCD 1 and OCD 2.

Table 26. OCD 1 and OCD 2 Pin Description

Pin Name	Microcontroller Function in Debug Mode	
	I/O	Description
DSCL	I	Serial clock pin. Input only pin.
DSDA	I/O	Serial data pin. Output port when reading and input port when programming. IT can be assigned as input/push-pull output port.
VDD,VSS	—	Logic power supply pin.

2.5.2.1 On-Chip Debug System

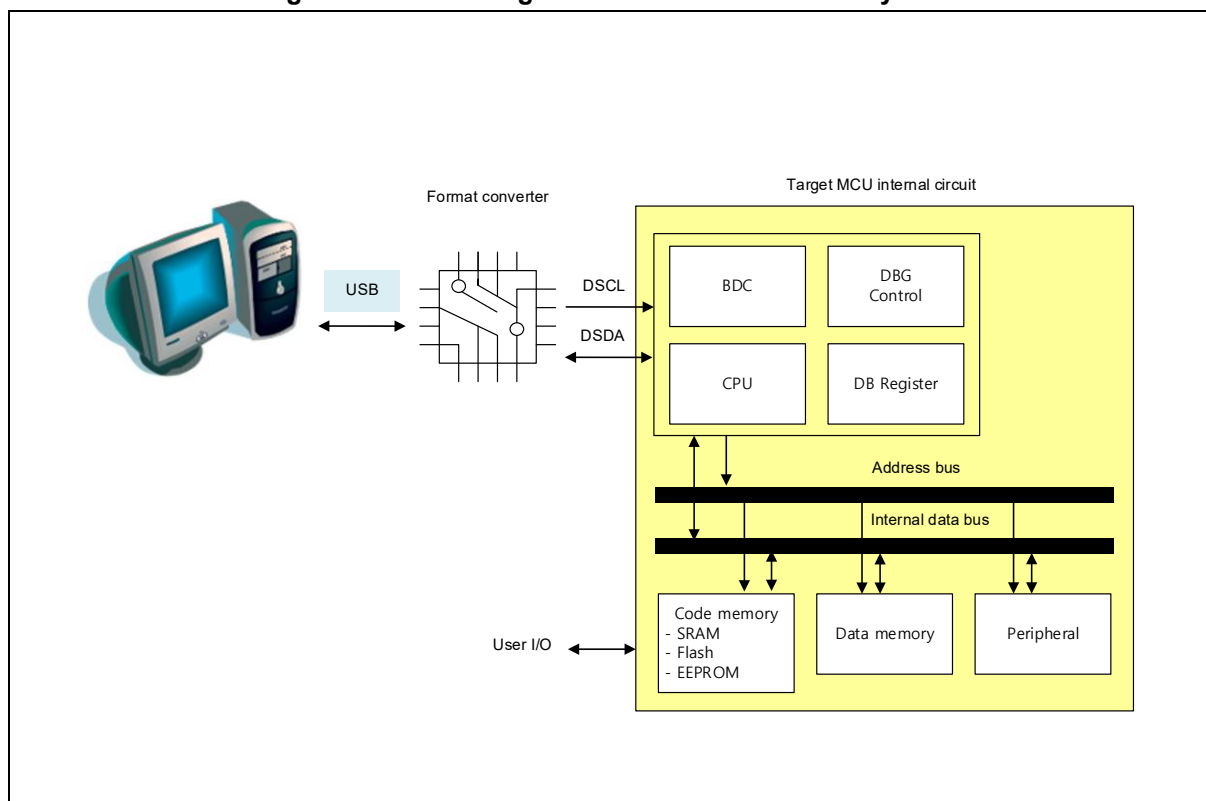
This section describes programming information via OCD interface.

Table 27 describes features of OCD, and Figure 74 shows a block diagram of the OCD interface and the OCD system.

Table 27. Features of OCD

Two Wire External Interface	• 1 for serial clock input • 1 for bi-directional serial data bus
Debugger Accesses	• All internal peripherals • Internal data RAM • Program Counter • Flash memory and data EEPROM memory
Extensive On-Chip Debugging Supports for Break Conditions	• Break instruction • Single step break • Program memory break points on single address • Programming of Flash, EEPROM, Fuses, and Lock bits through the two-wire interface • On-Chip Debugging supported by Dr. Choice®
Operating Frequency	The maximum frequency of a target microcontroller

Figure 74. Block Diagram of OCD Interface and System

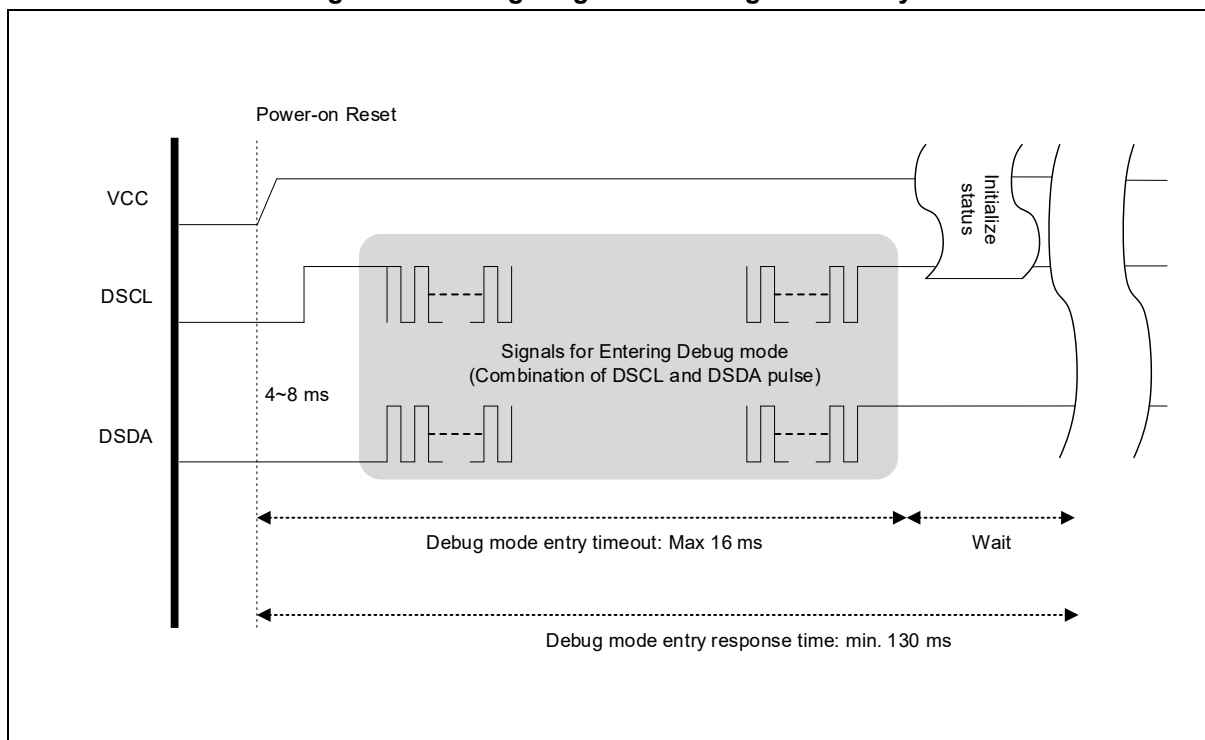


2.5.2.2 Entering Debug Mode

While communicating through the OCD, users can enter the microcontroller into DEBUG mode by applying power to it. This means, the microcontroller enters DEBUG mode by placing specific signals to DSCL and DSDA at the moment of initialization when powering on the microcontroller. To do this, users should be able to control the power of the microcontroller (VCC or VDD) and need to be careful to place a capacitive load such as a large capacity condenser on a power pin.

Please remember that the microcontroller can enter DEBUG mode only when power is applied, and it cannot enter DEBUG mode once the OCD is running.

Figure 75. Timing Diagram of Debug Mode Entry



2.5.2.3 Two-Wire Communication Protocol

For the OCD interface, the semi-duplex communication protocol is used through separate two wires such as DSCL and DSDA. The DSCL is a serial clock signal and the DSDA is a bi-directional serial address and data.

A unit packet of transmission data is 10-bit long and consists of a byte of data, 1-bit of parity, and 1-bit of acknowledge. A parity check bit and a receive acknowledge bit are transmitted to guarantee stability of data communication. In addition, a communication packet includes a start bit and an end bit to indicate a start and an end of the communication.

More detailed information on this communication protocol is listed below:

- A 10-bit packet transmission using two-wire interface.
- A packet consists of 8-bit data, 1-bit parity and 1-bit acknowledge.
- Parity is even of '1' for 8-bit data in transmitter.
- Receiver generates an acknowledge bit as '0' when the transmission for 8-bit data and its parity has no error.
- When transmitter has no acknowledge (acknowledge bit is '1' at tenth clock), error process is executed in transmitter.
- When acknowledge error is generated, host PC makes stop condition and transmits a command which has error again.
- Background debugger command is composed of a bundle of packets.
- Start condition and stop condition notify the start and the stop of background debugger command, respectively.

Figure 76. 10-bit Transmission Packet

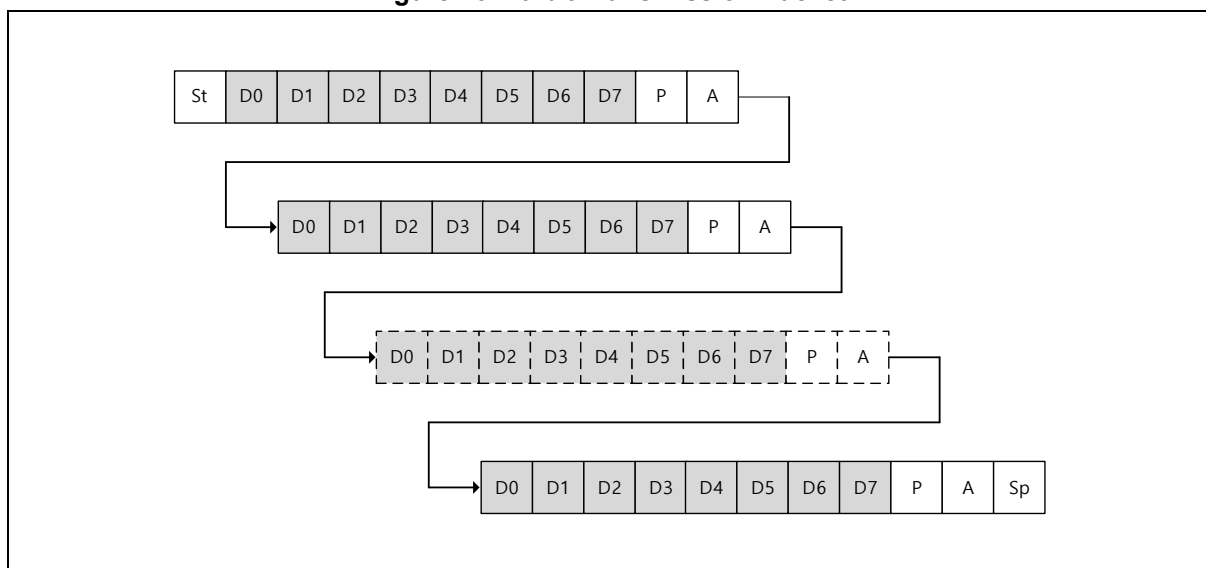


Figure 77 shows a timing diagram of a packet transmission using the OCD communication protocol. The start bit means a start of a packet and is valid when DSDA falls from 'H' to 'L' while External Host maintains DSCL to 'H'. After this, communication data is transferred and received between a Host and a microcontroller. The end bit means an end of the data transmission and is valid when DSDA changes from 'L' to 'H' while a Debugger maintains DSCL to 'H'. Next, the microcontroller places the bus in a wait state and processes the received data.

Figure 77. General Data Transfer Timing in OCD

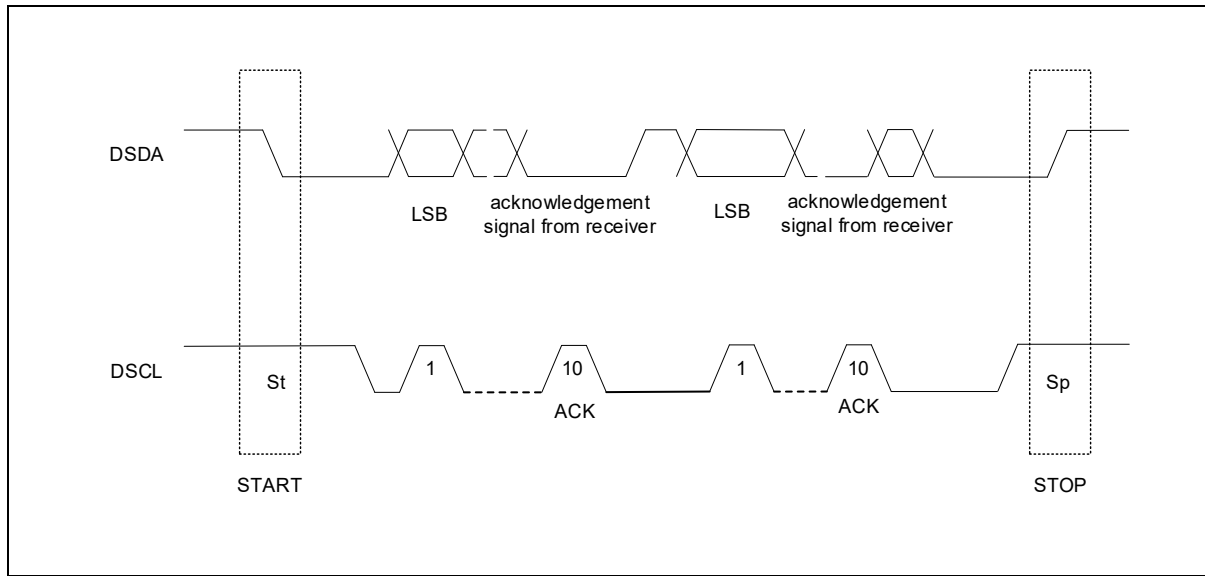


Figure 78 shows a timing diagram of each bit based on the state of DSCL clock and DSDA data. Similar to I2C signal, DSDA data is allowed to change when DSCL is 'L'. If the data changes when DSCL is 'H', the change means 'START' or 'STOP'.

Figure 78. Bit Transfer on OCD Bus

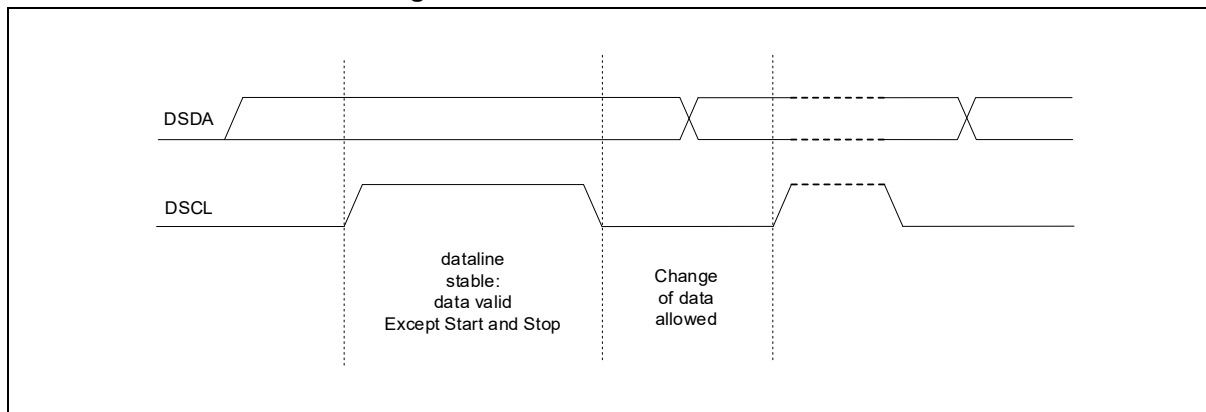
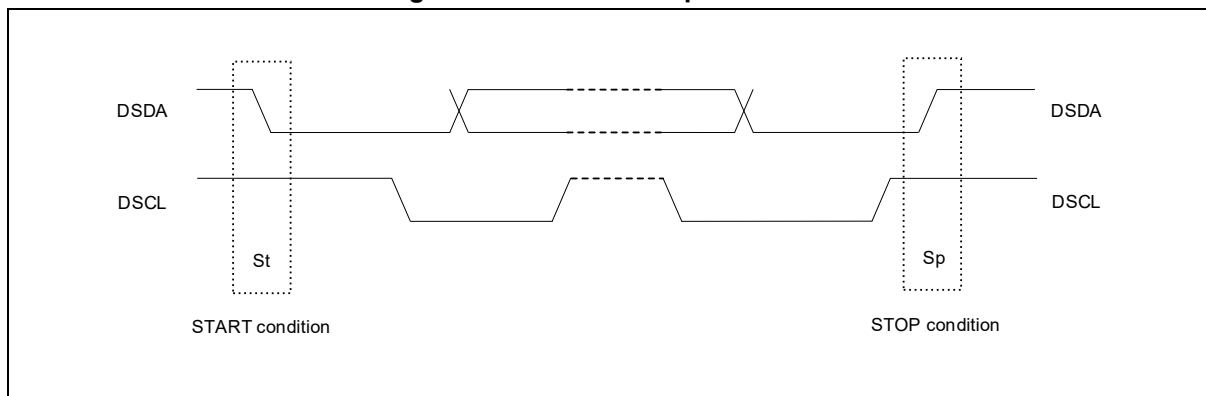


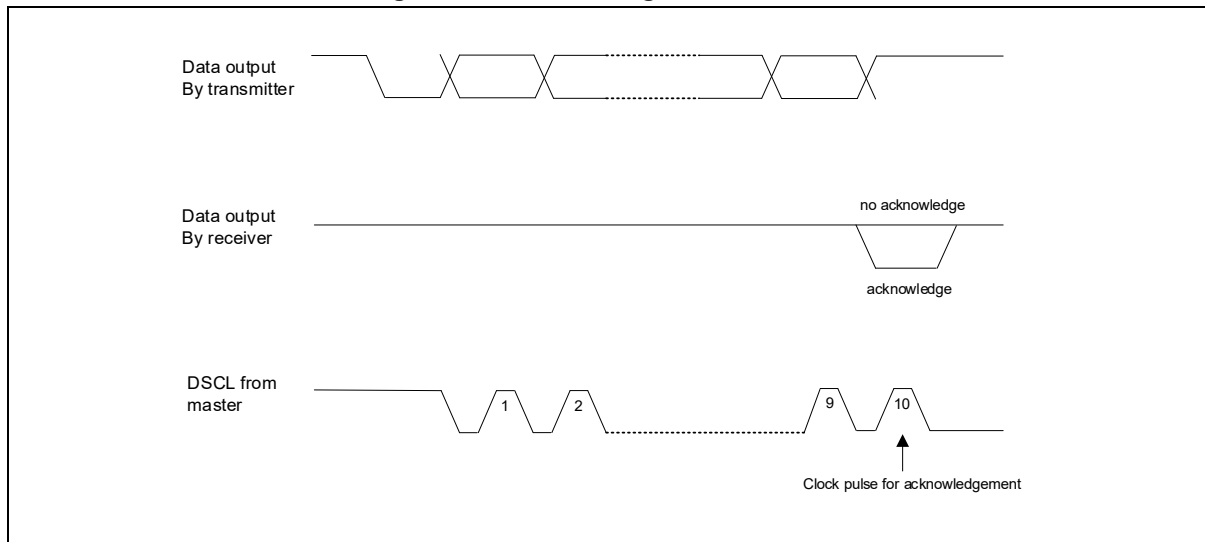
Figure 79. Start and Stop Condition



In OCD communication, each data byte is transferred with an accompanying parity bit. During consecutive data transfers, the receiver returns an acknowledge bit to confirm successful reception of the transmitted data.

As shown in Figure 80, when transferring data, a receiver outputs DSDA to 'L' to inform the normal reception of data. If a receiver outputs DSDA to 'H', it means error reception of data.

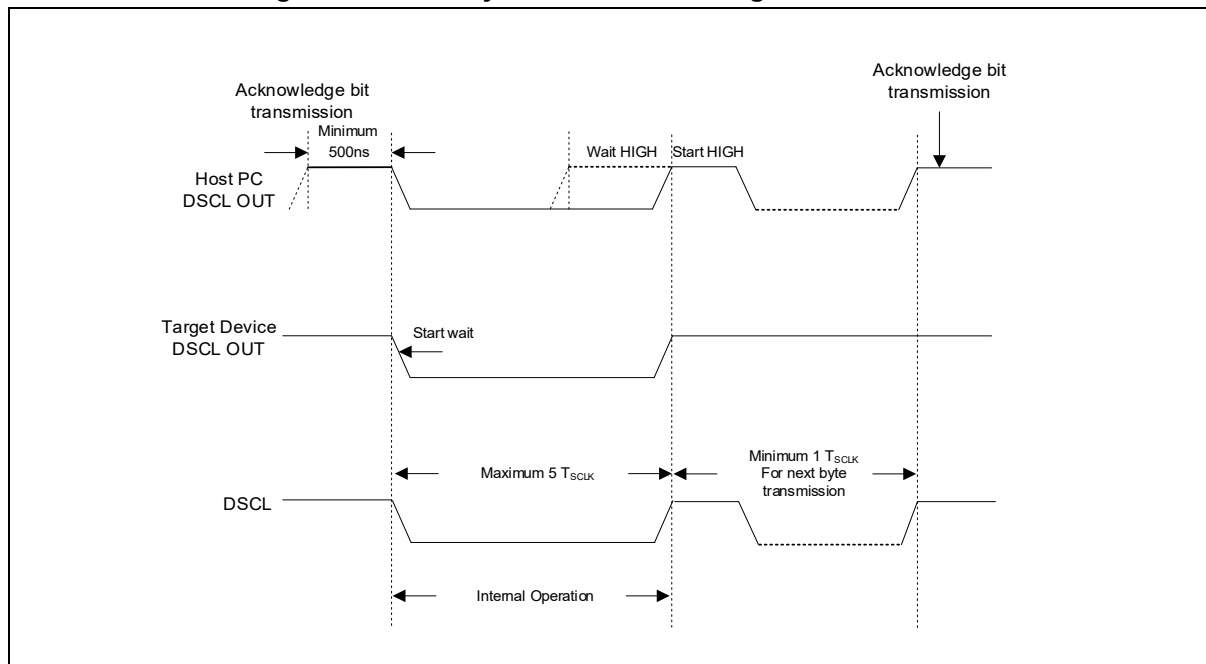
Figure 80. Acknowledge on Serial Bus



While the Host Debugger executes data communications, if a microcontroller needs communication delay or process delay, it can request communication delay to the Host Debugger.

Figure 81 shows timing diagrams where a microcontroller requests communication delay to the Host Debugger. If the microcontroller requests timing delay of the DSCL signal that the Host Debugger outputs, the microcontroller maintains the DSCL signal to 'L' to delay the clock change although the Host Debugger changes DSCL to 'H.'

Figure 81. Clock Synchronization During Wait Procedure



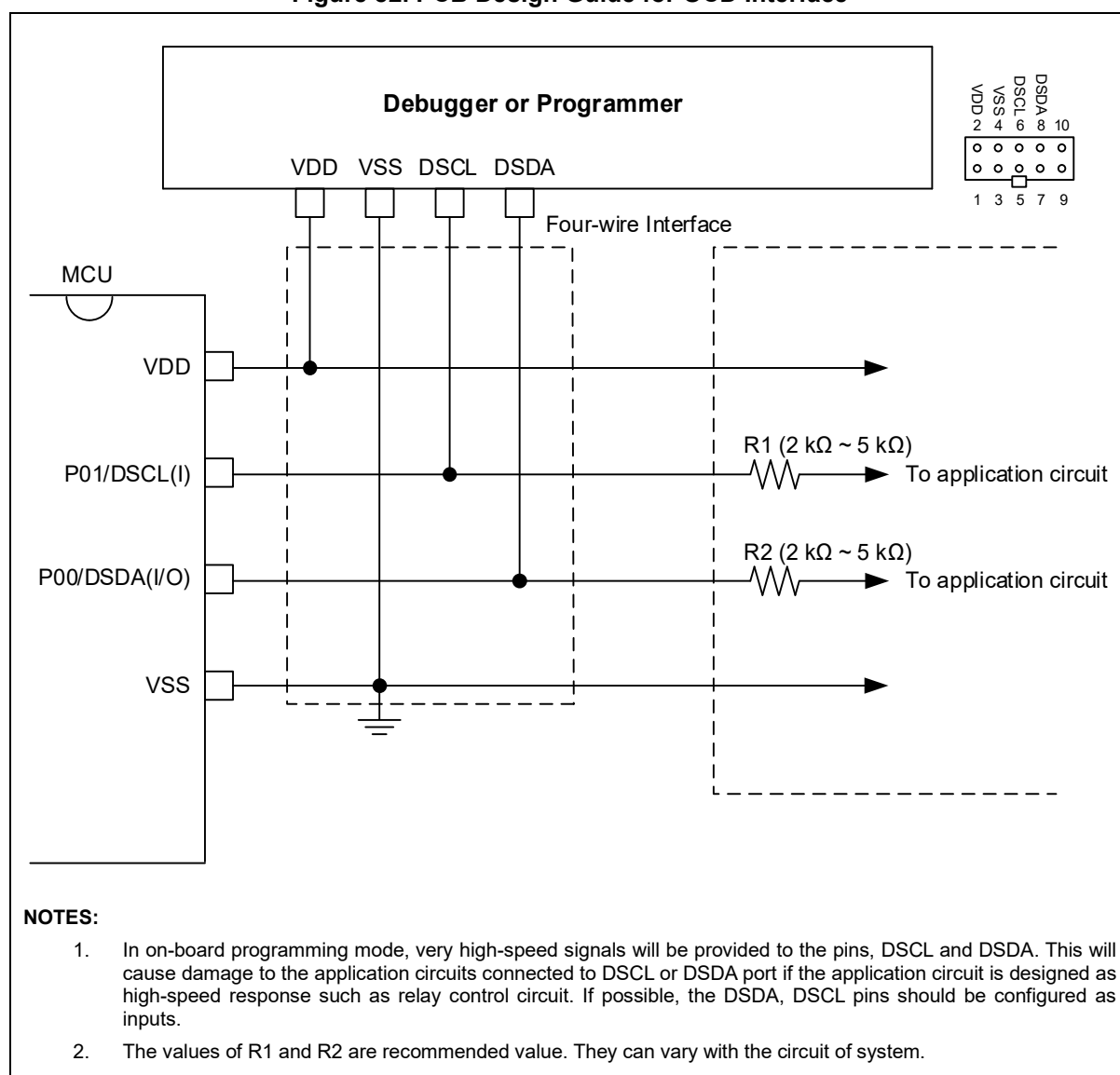
2.5.3 Circuit Design Guide

Special care should be taken depending on whether the OCD pins are dedicated to OCD communication or shared with other functions.

Figure 82 shows an example circuit where the OCD pins (DSCL and DSDA) are shared with other functions. They are required to be connected when debugging or ISP (In System Program) is executed.

Normally, the OCD pins are connected to outside to execute the predefined functions. Even when they are connected for debugging or ISP directly, the OCD pins are shared with other functions by using resistors as shown in Figure 82. By doing this, the OCD pins process the normal external signals and execute the OCD functions first when they are shared.

Figure 82. PCB Design Guide for OCD Interface

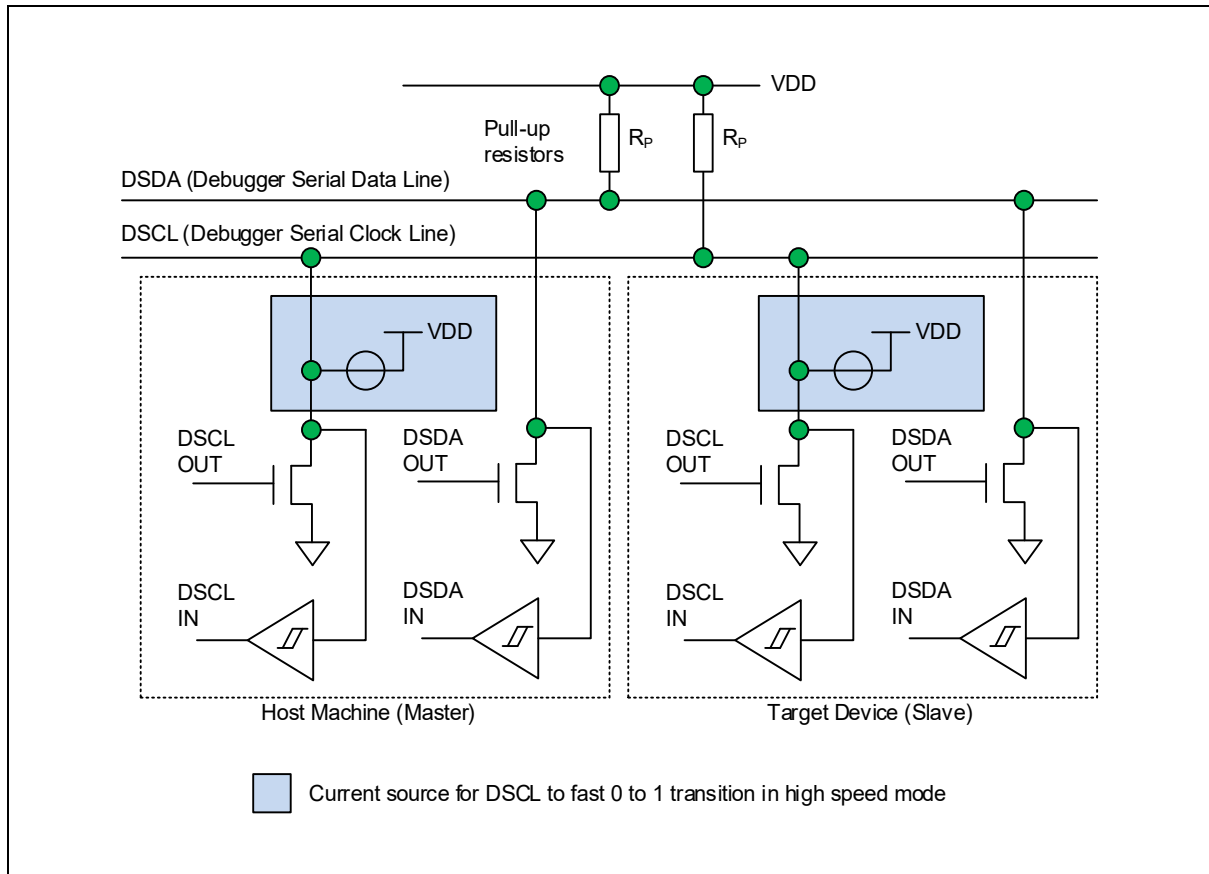


2.5.3.1 Connection of Transmission

OCD's two-wire communication interface uses open-drain Method (wire-AND Bi-Directional I/O).

Normally, it is recommended to place a resistor greater than 4.7 k Ω for DSCL and DSDA respectively. The capacitive load is recommended to be less than 100 pF. Outside these ranges, because communication may not be accomplished, the connection to Debug mode is not guaranteed.

Figure 83. Connection of Transmission



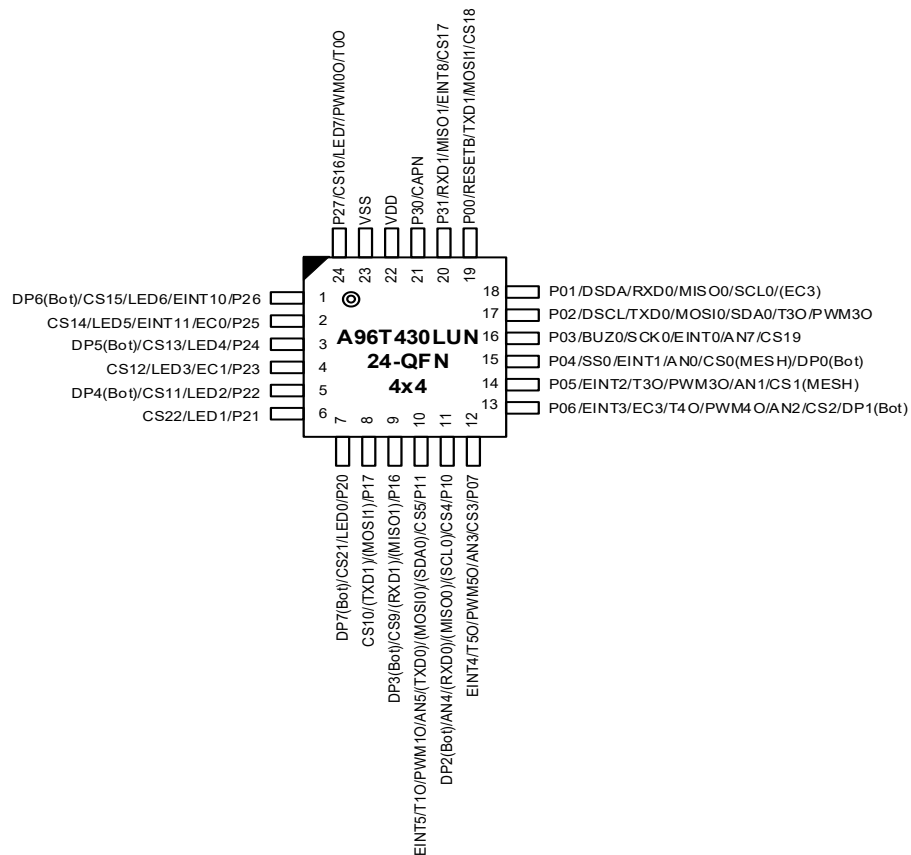
3. Pinouts and Pin Description

This chapter describes pinouts and pin descriptions of the A96T430 series.

3.1 Pinouts

3.1.1 A96T430LUN (24-QFN)

Figure 84. A96T430 24-QFN Pin Assignment

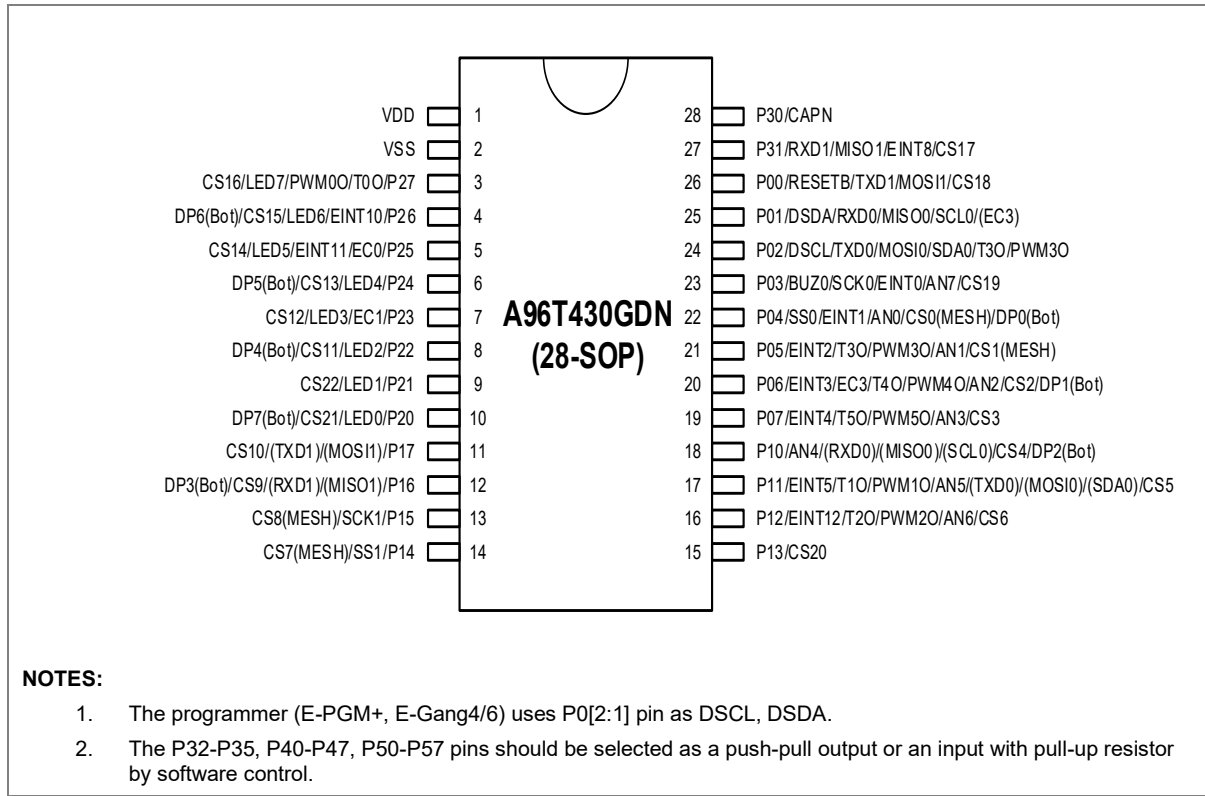


NOTES:

1. The programmer (E-PGM+, E-Gang4/6) uses P0[2:1] pin as DSCL, DSDA.
2. The P12-P15, P32-P35, P40-P47, P52, P53, P56, P57 pins should be selected as a push-pull output or an input with pull-up resistor by software control.

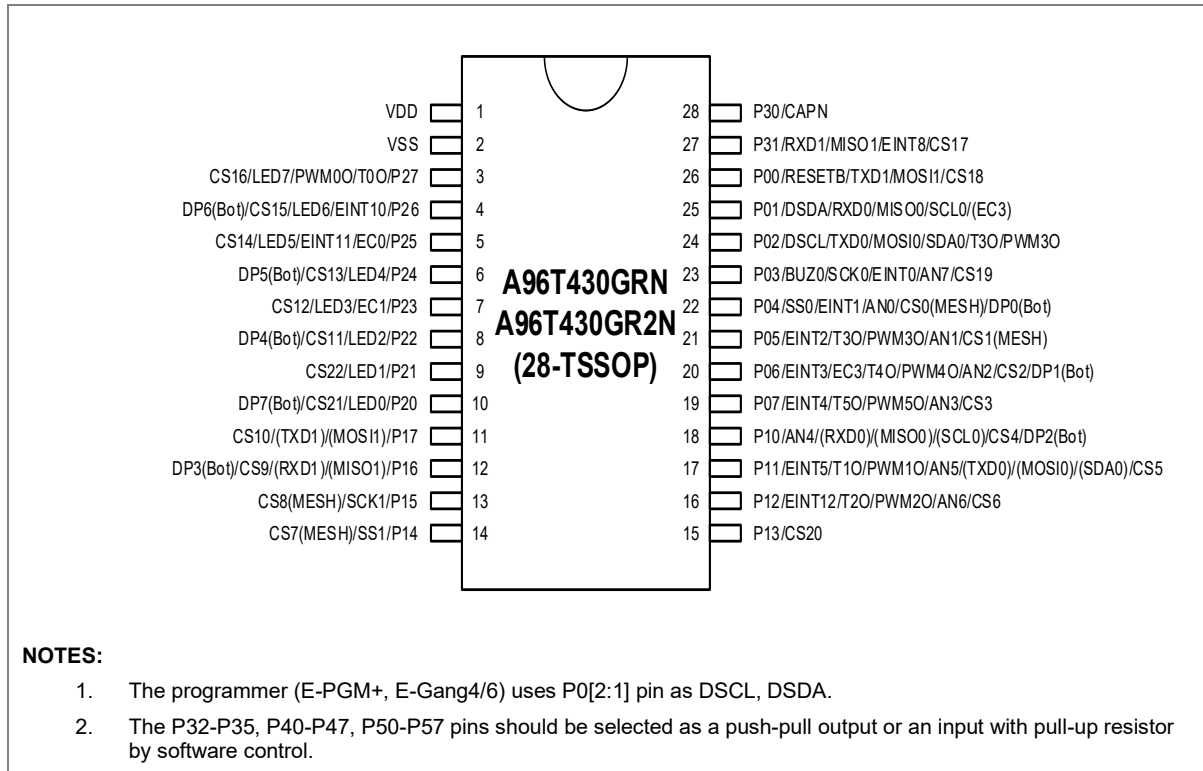
3.1.2 A96T430GDN (28-SOP)

Figure 85. A96T430 28-SOP Pin Assignment



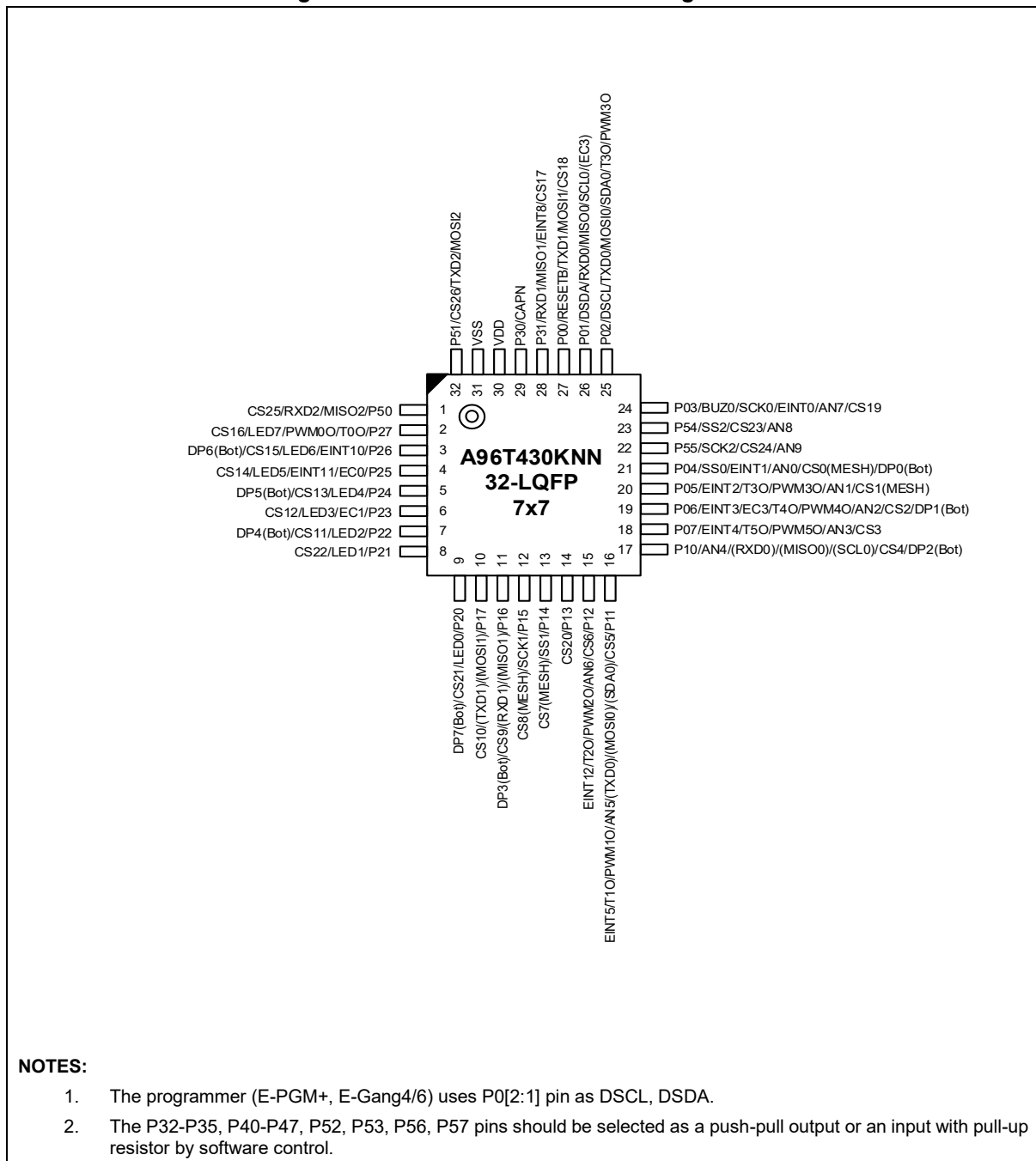
3.1.3 A96T430GRN/A96T420GR2N (28-TSSOP)

Figure 86. A96T430 28-TSSOP Pin Assignment



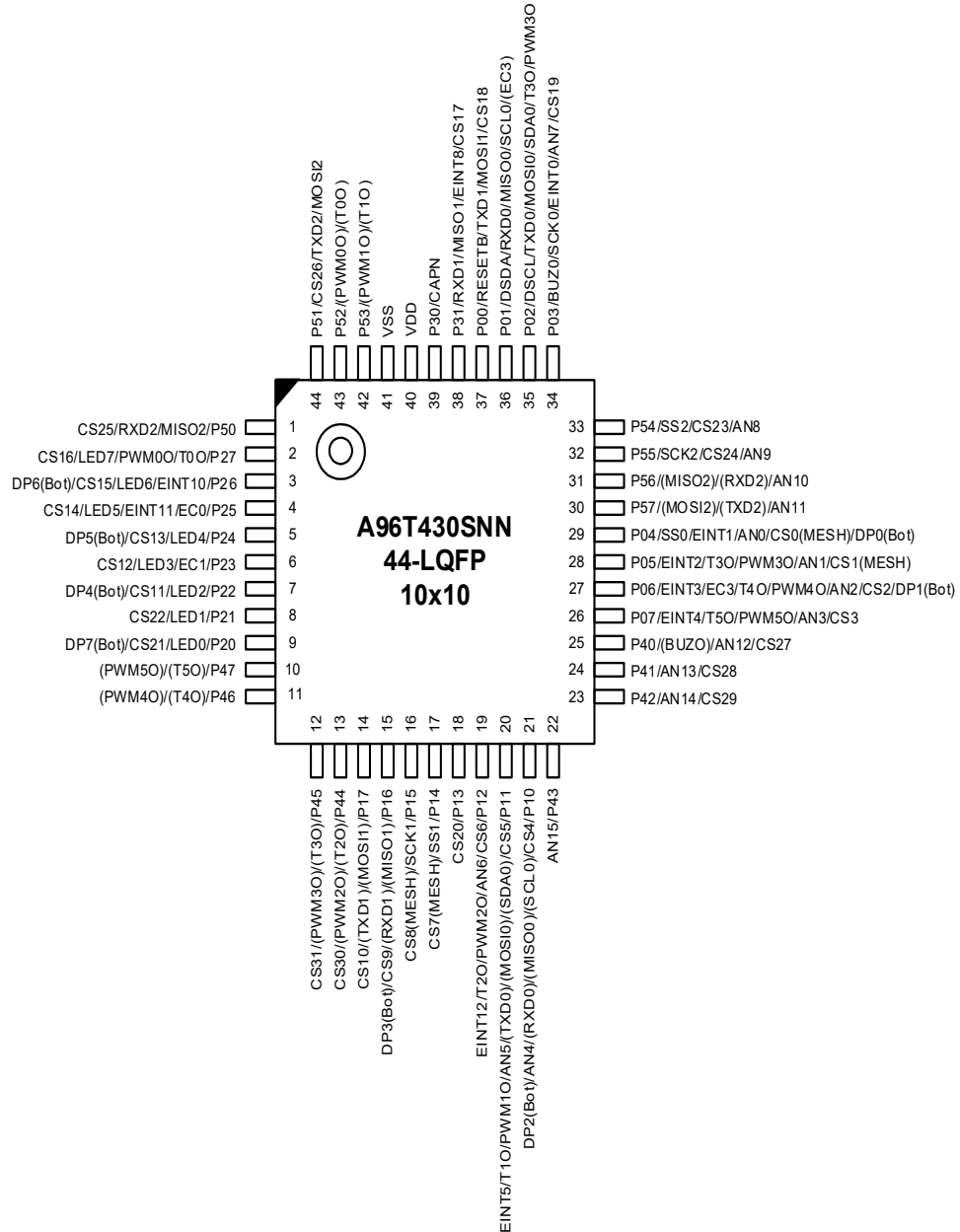
3.1.4 A96T430KNN (32-LQFP)

Figure 87. A96T430 32-LQFP Pin Assignment



3.1.5 A96T430SNN (44-LQFP)

Figure 88. A96T430 44-LQFP Pin Assignment

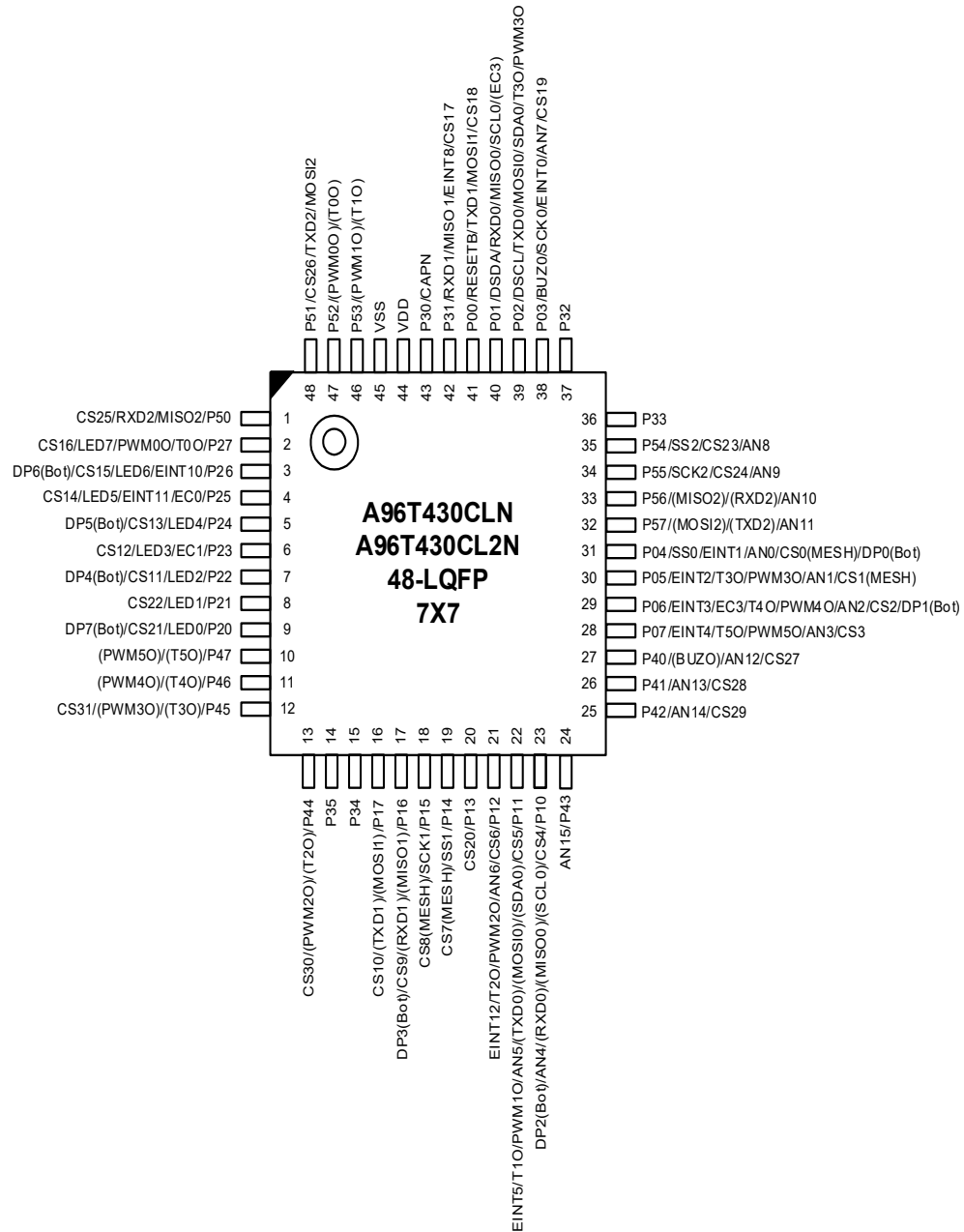


NOTES:

1. The programmer (E-PGM+, E-Gang4/6) uses P0[2:1] pin as DSCL, DSDA.
2. The P32-P35 pins should be selected as a push-pull output or an input with pull-up resistor by software control.

3.1.6 A96T430CLN/A96T430CL2N (48-LQFP)

Figure 89. A96T430 48-LQFP Pin Assignment



NOTE:

1. The programmer (E-PGM+, E-Gang4/6) uses P0[2:1] pin as DSCL, DSDA.

3.2 Pin Description

Table 28. Pin Description

Pin Name	I/O	Function	@RESET	Shared with
P00	I/O	- Port P0 8-bit I/O Port - Can be set in input or output mode in 1-bit units - Internal pull-up register can be used via software when this port is used as input port - Open Drain enable register can be used via software when this port is used as output port	Input	RESETB/TXD1/MOSI1/CS18
P01				DSDA/RXD0/MISO0/SCL0/(EC3)
P02				DSCL/TXD0/MOSI0/SDA0/T3O/PWM3O
P03				BUZ0/SCK0/EINT0/AN7/CS19
P04				SS0/EINT1/AN0/CS0(MESH)/DP0(Bot)
P05				EINT2/T3O/PWM3O/AN1/CS1(MESH)
P06				EINT3/EC3/T4O/PWM4O/AN2/CS2/DP1(Bot)
P07				EINT4/T5O/PWM5O/AN3/CS3
P10	I/O	- Port P1 8-bit I/O Port - Can be set in input or output mode in 1-bit units - Internal pull-up register can be used via software when this port is used as input port - Open Drain enable register can be used via software when this port is used as output port. - The P12 – P15 are not in the 24-pin package.	Input	AN4/CS4/(RXD0)/(MISO0)/(SCL0)/CS4/DP2(Bot)
P11				EINT5/T1O/PWM1O/AN5/CS5/(TXD0)/(MOSI0)/(SDA0)
P12				EINT12/T2O/PWM2O/AN6/CS6
P13				CS20
P14				SS1/CS7(MESH)
P15				SCK1/CS8(MESH)
P16				(RXD1)/(MISO1)/CS9/DP3(Bot)
P17				(TXD1)/(MOSI1)/CS10
P20	I/O	- Port P2 8-bit I/O Port - Can be set in input or output mode in 1-bit units - Internal pull-up register can be used via software when this port is used as input port - Open Drain enable register can be used via software when this port is used as output port.	Input	LED0/CS21/DP7(Bot)
P21				LED1/CS22
P22				LED2/CS11/DP4(Bot)
P23				LED3/EC1/CS12
P24				LED4/CS13/DP5(Bot)
P25				LED5/EINT11/EC0/CS14
P26				LED6/EINT10/CS15/DP6(Bot)
P27				LED7/T0O/PWM0O/CS16
P30	I/O	- Port P3 2-bit I/O Port - Can be set in input or output mode in 1-bit units - Internal pull-up register can be used via software when this port is used as input port - Open Drain enable register can be used via software when this port is used as output port.	Input	CAPN
P31				RXD1/MISO1/EINT8/CS17
P32				-
P33				-
P34				-
P35				-

Table 28. Pin Description (continued)

Pin Name	I/O	Function	@RESET	Shared with
P40	I/O	- Port P4 2-bit I/O Port - Can be set in input or output mode in 1-bit units - Internal pull-up register can be used via software when this port is used as input port - Open Drain enable register can be used via software when this port is used as output port.	Input	CS27/AN12/(BUZ0)
P41				CS28/AN13
P42				CS29/AN14
P43				AN15
P44				CS30/(PWM2O)/(T2O)
P45				CS31/(PWM3O)/(T3O)
P46				(PWM4O)/(T4O)
P47				(PWM5O)/(T5O)
P50	I/O	- Port P5 2-bit I/O Port - Can be set in input or output mode in 1-bit units - Internal pull-up register can be used via software when this port is used as input port - Open Drain enable register can be used via software when this port is used as output port	Input	CS25/RXD2/MISO2
P51				CS26/TXD2/MOSI2
P52				(PWM0O)/(T0O)
P53				(PWM1O)/(T1O)
P54				CS23/AN8/SS2
P55				CS24/AN9/SCK2
P56				AN10/(RXD2)/(MISO2)
P57				AN11/(TXD2)/(MOSI2)
EINT0	I/O	External interrupt inputs	Input	P03/BUZ0/SCK0/AN7/CS19
EINT1	I/O			P04/SS0/AN0/CS0(MESH)/DP0(Bot)
EINT2	I/O	External interrupt input and Timer 3 capture input	Input	P05/T3O/PWM3O/AN1/CS1(MESH)
EINT3	I/O	External interrupt input and Timer 4 capture input	Input	P06/EC3/T4O/PWM4O/AN2/CS2/DP1(Bot)
EINT4	I/O	External interrupt input and Timer 5 capture input	Input	P07/T5O/PWM5O/AN3/CS3
EINT5	I/O	External interrupt input and Timer 1 capture input	Input	P11/T1O/PWM1O/AN5/CS5/(TXD0)/(MOSI0)/(SDA0)
EINT8	I/O	External Interrupt input	Input	P31/RXD1/MISO1/CS17
EINT10	I/O	External interrupt input	Input	P26/LED6/CS15/DP6(Bot)
EINT11	I/O	External interrupt input	Input	P25/LED5/EC0/CS14
EINT12	I/O	External interrupt input and Timer 2 capture input	Input	P12/T2O/PWM2O/AN6/CS6

Table 28. Pin Description (continued)

Pin Name	I/O	Function	@RESET	Shared with
T0O	I/O	Timer 0 interval output	Input	P27/LED7/T0O/PWM0O/CS16 P52/(PWM0O)
T1O	I/O	Timer 1 interval output	Input	P11/EINT5/PWM1O/AN5/CS5/(TXD0)/(MOSI0)/(SDA0) P53/(PWM1O)
T2O	I/O	Timer 2 interval output	Input	P12/EINT12/PWM2O/AN6/CS6 P44/CS30/(PWM2O)
T3O	I/O	Timer 3 interval output	Input	P02/DSCL/TXD0/MOSI0/SDA0/PWM3O P05/EINT2/PWM3O/AN1/CS1(MESH) P45/CS31/(PWM3O)
T4O	I/O	Timer 4 interval output	Input	P06/EINT3/EC3/PWM4O/AN2/CS2/DP1(Bot) P46/(PWM4O)
T5O	I/O	Timer 5 interval output	Input	P07/EINT4/PWM5O/AN3/CS3 P47/(PWM5O)
PWM0O	I/O	Timer 0 PWM output	Input	P27/LED7/T0O/CS16 P52/(T0O)
PWM1O	I/O	Timer 1 PWM output	Input	P11/EINT5/T1O/AN5/CS5/(TXD0)/(MOSI0)/(SDA0) P33/(T1O)
PWM2O	I/O	Timer 2 PWM output	Input	P12/EINT12/T2O/AN6/CS6 P44/CS30/(T2O)
PWM3O	I/O	Timer 3 PWM output	Input	P02/DSCL/TXD0/MOSI0/SDA0/T3O P05/EINT2/T3O/AN1/CS1(MESH) P45/CS31/(T3O)
PWM4O	I/O	Timer 4 PWM output	Input	P06/EINT3/EC3/T4O/AN2/CS2/DP1(Bot) P46/(T4O)
PWM5O	I/O	Timer 5 PWM output	Input	P07/EINT4/T5O/AN3/CS3 P47/(T5O)
EC0	I/O	Timer 0 event count input	Input	P25/LED5/EINT11/CS14
EC1	I/O	Timer 1 event count input	Input	P23/LED3/CS12
EC3	I/O	Timer 3 event count input	Input	P01/DSDA/RXD0/MISO0/SCL0 P06/EINT3/T4O/PWM4O/AN2/CS2/DP1(Bot)
BUZ0	I/O	Buzzer signal output	Input	P03/SCK0/EINT0/AN7/CS19 P40/CS27/AN12
SCK0	I/O	Serial 0 clock input/output	Input	P03/BUZ0/EINT0/AN7/CS19
SCK1	I/O	Serial 1 clock input/output	Input	P15/CS8(MESH)
SCK2	I/O	Serial 2 clock input/output	Input	P55/CS24/AN9

Table 28. Pin Description (continued)

Pin Name	I/O	Function	@RESET	Shared with
MOSI0	I/O	SPI 0 master output, slave input	Input	P02/DSCL/TXD0/SDA0/T3O/PWM3O P11/EINT5/T1O/PWM1O/AN5/CS5/(TXD0)/(SDA0)
MOSI1	I/O	SPI 1 master output, slave input	Input	P00/RESETB/TXD1/CS18 P17/(TXD1)/CS10
MOSI2	I/O	SPI 2 master output, slave input	Input	P51/CS26/TXD2 P57/AN10/(RXD2)
MISO0	I/O	SPI 0 master input, slave output	Input	P01/DSDA/RXD0/SCL0/(EC3) P10/AN4/CS4/(RXD0)/(SCL0)/CS4
MISO1	I/O	SPI 1 master input, slave output	Input	P16/(RXD1)/CS9/DP3(Bot) P31/RXD1/EINT8/CS17
MISO2	I/O	SPI 2 master input, slave output	Input	P50/CS25/RXD2 P56/AN10/(RXD2)
SS0	I/O	SPI 0 slave select input (Slave mode only)	Input	P04/EINT1/AN0/CS0(MESH)/DP0(Bot)
SS1	I/O	SPI 1 slave select input (Slave mode only)	Input	P14/CS7(MESH)
SS2	I/O	SPI 2 slave select input (Slave mode only)	Input	P54/CS23/AN8
TXD0	I/O	UART 0 data output	Input	P02/DSCL/MOSI0/SDA0/T3O/PWM3O P11/EINT5/T1O/PWM1O/AN5/CS5/(MOSI0)/(SDA0)
TXD1	I/O	UART 1 data output	Input	P00/RESETB/MOSI1/CS18 P17/(MOSI1)/CS10
TXD2	I/O	UART 2 data output	Input	P51/CS26/MOSI2 P57/AN11/(MOSI2)
RXD0	I/O	UART 0 data input	Input	P01/DSDA/MISO0/SCL0/(EC3) P10/AN4/CS4/(MISO0)/(SCL0)/CS4/DP2(Bot)
RXD1	I/O	UART 1 data input	Input	P31/MISO1/EINT8/CS17 P16/(MISO1)/CS9/DP3(Bot)
RXD2	I/O	UART 1 data input	Input	P50/CS25/MISO2 P56/AN10/(MISO2)
SCL0	I/O	I2C 0 clock input/output	Input	P01/DSDA/RXD0/MISO0/(EC3) P10/AN4/CS4/(RXD0)/(MISO0)/CS4/DP2(Bot)
SDA0	I/O	I2C 0 data input/output	Input	P02/DSCL/TXD0/MOSI0/T3O/PWM3O P11/EINT5/T1O/PWM1O/AN5/CS5/(TXD0)/(MOSI0)

Table 28. Pin Description (continued)

Pin Name	I/O	Function	@RESET	Shared with
AN0	I/O	ADC analog input channels	Input	P04/SS0/EINT1/CS0(MESH)/DP0(Bot)
AN1	I/O		Input	P05/EINT2/T3O/PWM3O/CS1(MESH)
AN2	I/O		Input	P06/EINT3/EC3/T4O/PWM4O/CS2/DP1(Bot)
AN3	I/O		Input	P07/EINT4/T5O/PWM5O/CS3
AN4	I/O		Input	P10/CS4/(RXD0)/(MISO0)/(SCL0)/CS4/DP2(Bot)
AN5	I/O		Input	P11/EINT5/T1O/PWM1O/CS5/(TXD0)/(MOSI0)/(SDA0)
AN6	I/O		Input	P12/EINT12/T2O/PWM2O/CS6
AN7	I/O		Input	P03/BUZ0/SCK0/EINT0/CS19
AN8	I/O		Input	P54/CS23/SS2
AN9	I/O		Input	P55/CS24/SCK2
AN10	I/O		Input	P56/(RXD2)/(MISO2)
AN11	I/O		Input	P57/(TXD2)/(MOSI2)
AN12	I/O		Input	P40/CS27/(BUZ0)
AN13	I/O		Input	P41/CS28/AN13
AN14	I/O		Input	P42/CS29/AN14
AN15	I/O		Input	P43
CAPN	I/O	Modulation CAP	Input	P30
DP0	I/O	Diff Switch input channels	Input	P04/SS0/EINT1/CS0(MESH)/AN0
DP1	I/O		Input	P06/EINT3/EC3/T4O/PWM4O/CS2/AN2
DP2	I/O		Input	P10/CS4/(RXD0)/(MISO0)/(SCL0)/CS4/AN4
DP3	I/O		Input	P16/(RXD1)/(MISO1)/CS9
DP4	I/O		Input	P22/LED2/CS11
DP5	I/O		Input	P24/LED4/CS13
DP6	I/O		Input	P26/LED6/EINT10/CS15
DP7	I/O		Input	P20/LED0/CS21

Table 28. Pin Description (continued)

Pin Name	I/O	Function	@RESET	Shared with
CS0	I/O	Touch Sensor Inputs	Input	P04/SS0/EINT1/AN0/(MESH)/DP0(Bot)
CS1				P05/EINT2/T3O/PWM3O/AN1/(MESH)
CS2				P06/EINT3/EC3/T4O/PWM4O/AN2/DP1(Bot)
CS3				P07/EINT4/T5O/PWM5O/AN3
CS4				P10/AN4/CS4/(RXD0)/(MISO0)/(SCL0)/DP2(Bot)
CS5				P11/EINT5/T1O/PWM1O/AN5/(TXD0)/(MOSI0)/(SDA0)
CS6				P12/EINT12/T2O/PWM2O/AN6
CS7				P14/SS1/(MESH)
CS8				P15/SCK1/(MESH)
CS9				P16/(RXD1)/(MISO1)/DP3(Bot)
CS10				P17/(TXD1)/(MOSI1)
CS11				P22/LED2/DP4(Bot)
CS12				P23/LED3/EC1
CS13				P24/LED4/DP5(Bot)
CS14				P25/LED5/EINT11/EC0
CS15				P26/LED6/EINT10/DP6(Bot)
CS16				P27/LED7/T0O/PWM0O
CS17				P31/RXD1/MISO1/EINT8
CS18				P00/RESETB/TXD1/MOSI1
CS19				P03/BUZ0/SCK0/EINT0/AN7/
CS20				P13
CS21				P20/LED0/DP7(Bot)
CS22				P21/LED1
CS23				P54/AN8/SS2
CS24				P55/AN9/SCK2
CS25				P50/RXD2/MISO2
CS26				P51/TXD2/MOSI2
CS27				P40/AN12/(BUZ0)
CS28				P41/AN13
CS29				P42/AN14
CS30				P44/(PWM2O)/(T2O)
CS31				P45/(PWM3O)/(T3O)

Table 28. Pin Description (continued)

Pin Name	I/O	Function	@RESET	Shared with
RESETB	I/O	System reset pin with a pull-up resistor when it is selected as the RESETB by CONFIGURE OPTION	Input	P00/TXD1/MOSI1/CS18
DSDA	I/O	In-system programming data input/output	Input	P01/RXD0/MISO0/SCL0/(EC3)
DSCL	I/O	In-system programming clock input	Input	P02/TXD0/MOSI0/SDA0/T3O/PWM3O
VDD, VSS	—	Power input pins	—	—

NOTES:

1. The P12–P15, P32–P35, P40–P47, P50–P57 are not in the 24-pin package.
2. The P32–P35, P40–P47, P50–P57 are not in the 28-pin package.
3. The P32–P35, P40–P47, P52, P53, P56, P57 are not in the 32-pin package.
4. The P32–P35 are not in the 44-pin package.
5. The P00/RESETB pin is configured as one of the P00 and RESETB pin by the “CONFIGURE OPTION.”
6. If the P01/EC3/MISO0/RXD0/SCL0/DSDA and P02/T3O/PWM3O/MOSI0/TXD0/SDA0/DSCL pins are connected to the programmer during power-on reset, the pins are automatically configured as In-system programming pins.
7. The P01/EC3/MISO0/RXD0/SCL0/DSDA and P02/T3O/PWM3O/MOSI0/TXD0/SDA0/DSCL pins are configured as inputs with internal pull-up resistor only during the reset or power-on reset.
8. The P00/RESETB/TXD1/MOSI1/CS18 pin is configured as a function pin by software control.

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 29. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Remark
Supply Voltage	VDD	-0.3 to +6.5	V	–
Normal Voltage Pin	V _I	-0.3 to VDD+0.3	V	Voltage on any pin with respect to VSS
	V _O	-0.3 to VDD+0.3	V	
	I _{OH}	10	mA	Maximum current output sourced by (I _{OH} per I/O pin)
	ΣI _{OH}	100	mA	Maximum current (ΣI _{OH})
	I _{OL1}	25	mA	Maximum current (I _{OL1} per I/O pin)
	ΣI _{OL1}	100	mA	Maximum current (ΣI _{OL1})
	I _{OL2}	130	mA	Maximum current sunk by (I _{OL2} per I/O pin)
	ΣI _{OL2}	130	mA	Maximum current by LED Drive (ΣI _{OL2})
Storage Temperature	T _{STG}	-65 to +150	°C	–

NOTE:

- Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.2 Recommended Operating Conditions

Table 30. Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating Voltage	VDD	f _x = 16 MHz HSIRC	2.0	–	5.5	V
		f _x = 32 kHz LSIRC	2.0	–	5.5	
		Touch, ADC	2.7	–	5.5	
Operating Temperature	T _{OPR}	VDD=2.0 to 5.5V	-40	–	85	°C

4.3 Touch Sensing Characteristics

Table 31. Touch Switch Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Voltage	VDDEXT	-	2.7	5	5.5	V
Operating Temperature	TOP	-	-40	25	105	°C
Maximum Junction Temperature	TJ	-	-	-	125	°C
Load Capacitance	Cload	-	-	-	100	pF
Operating Frequency	Fop	Cload=50 pF (@2 MHz) Cload=100 pF (@1 MHz)	-	4	4	MHz
		VDDEXT ≤ 3.3 V"	0.125	2	2	
VSTART/VSTOP Reference Voltage	-	-	200 mV	-	AVDD-200 mV	V
COMP Reference Voltage	-	-	-	AVDD×50%	-	V
High-SenOperating Current	-	DAC enable, CAPN 22 nF	-	1514	1931	μA
	-	DAC disable, CAPN 22 nF	-	805	897	μA

4.4 ADC Characteristics

Table 32. ADC Characteristics

(TA= -40°C to +85°C or TA= -40°C to 105°C, VDD=2.7 V to 5.5 V, VSS=0 V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Resolution	—	—		—	12	—	bit
Conversion Time	t _{CON}	12-bit resolution, 8 MHz		8	—	—	μs
Integral Linear Error	ILE	AVREF= 2.7 V to 5.5 V fx= 8 MHz		—	5		LSB
Differential Linearity Error	DLE			—	5		
Zero Offset Error	ZOE			—	5		
Full Scale Error	FSE			—	1		
Conversion Time	t _{CON}	12-bit resolution, 8 MHz		3	—	—	μs
Analog Input Voltage	V _{AN}	—		VSS	—	AVREF	V
Analog Reference Voltage	AVREF	NOTE 3		2.7	—	VDD	
ADC Operating Current	I _{ADC}	Enable	VDD=5 V	—	0.7	1	mA
		Disable		—	—	0.1	μA
ADC Clock	—	AVDD	3.6 V	—	8.0	—	MHz
			3.0 V	—	4.0	—	
			2.7 V	—	1.0	—	
			2.5 V	—	0.5	—	

NOTES:

1. Zero offset error is the difference between 000000000000 and the converted output for zero input voltage (VSS).
2. ADC performance is not available under 2.7 V.
3. When AVREF is lower than 2.7 V, the ADC resolution is worse.

4.5 Power-On Reset Characteristics

Table 33. Power-On Reset Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
RESET Release Level	V _{POR}	—	—	1.48	—	V
RESET SET Level	—	—	—	1.28	—	V
VDD Voltage Rising Time	t _R	—	0.05	—	50.0	V/ms
VDD Voltage Falling Time	t _F	—	0.05	—	50.0	V/ms
Minimum Pulse Width	t _{LW}	—	—	—	5	μs
POR Current	I _{POR}	—	—	0.2	—	μA

NOTE:

1. Guaranteed by design.

4.6 Low-Voltage Reset and Low-Voltage Indicator Characteristics

Table 34. LVR and LVI Characteristics

(TA= -40°C to +85°C or TA= -40°C to 105°C, VDD= 2.0 V to 5.5 V, VSS=0 V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Low-Voltage Reset Level	V _{LVR_R0}	VDD rising		1.550	1.700	1.800	V
	V _{LVR_R1}			2.608	2.860	3.029	
	V _{LVR_R2}			3.575	2.920	4.151	
	V _{LVR_R3}			4.077	4.470	4.734	
	V _{LVR_F0}	VDD falling		1.520	1.600	1.760	
	V _{LVR_F1}			2.533	2.700	2.970	
	V _{LVR_F2}			3.470	3.700	4.070	
	V _{LVR_F3}			3.958	4.220	4.642	
Low-Voltage Indicator Level	V _{LVI_R0}	VDD rising		2.134	2.340	2.478	V
	V _{LVI_R1}			2.909	3.190	3.378	
	V _{LVI_R2}			3.867	4.240	4.490	
	V _{LVI_R3}			4.359	4.780	5.062	
	V _{LVI_F0}	VDD falling		2.073	2.200	2.431	
	V _{LVI_F1}			2.823	3.000	3.311	
	V _{LVI_F2}			3.752	4.000	4.400	
	V _{LVI_F3}			4.230	4.510	4.961	
Minimum Pulse Width	t _{LW}	—		—	—	5	μs
LVR and LVI Current	I _{BL}	Enable (Both)	—	—	4.0	—	μA
		Enable (One of two)		—	3.5	—	
		Disable (Both)	—	—	—	0.1	

NOTE:

1. Guaranteed by design.

4.7 High-Speed Internal RC Oscillator Characteristics

Table 35. High-Speed Internal RC Oscillator Characteristics

(TA= -40°C to +85°C, VDD= 2.0 V to 5.5 V, VSS=0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Frequency	f _{HSIRC}	V _{DD} = 2.0 to 5.5 V	–	16	–	MHz
Tolerance	–	T _A =0°C to +60°C	-1.5	–	+1.5	%
		T _A =-40°C to +85°C	-2.5	–	+2.5	
		T _A =-40°C to +105°C	-3.5	–	+3.5	
Clock Duty Ratio	TOD	–	40	50	60	%
Stabilization Time	T _{HFS}	–	–	–	5	μs
HSIRC Current	I _{HSIRC}	Enable	–	280	–	μA
		Disable	–	–	15	nA

NOTE:

1. Guaranteed by design.

4.8 Low-Speed Internal RC Oscillator Characteristics

Table 36. Internal WDTRC Oscillator Characteristics

(TA= -40°C to +85°C or TA= -40°C to 105°C, VDD=2.0 V to 5.0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Frequency	f _{LSIRC}	T _A =-40°C to +85°C	16	32	48	kHz
Stabilization Time	T _{LSIRC}	–	–	–	0.2	ms
LSIRC Current	I _{LSIRC}	Enable	–	0.15	–	μA
		Disable	–	–	0.01	

4.9 DC Characteristics

Table 37. DC Characteristics

(TA= -40°C to +85°C, VDD= 2.0 V to 5.5 V, VSS= 0 V, fSCLK= 16 MHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input High Voltage	VIH	All input pins	0.8VDD	–	–	V
Input Low Voltage	VIL	All input pins	–	–	0.2VDD	V
Output High Voltage	VOH	VDD=5.0 V, All output ports;	0.8VDD	–	–	V
Output Low Voltage	VOL1	VDD=5.0 V, 4 mA; All output ports except VOL2	–	–	0.2VDD	V
	VOL2	VDD=5 V, IOL= 72 mA, TA= 25°C; P2x LED High sink current output	–	1	–	V
Output High Current	IOH	VDD=5.0 V, VOH=0.8*VDD, All output ports;	-4	–	–	mA
Input High Leakage Current	IIH	All input ports	–	–	1	μA
Input Low Leakage Current	IIL	All input ports	-1	–	–	μA
Pull-Up Resistor	R _{PU}	VDD=5.0 V, All Input ports	30	50	70	kΩ
Power Supply Current	IDD1 (RUN)	fHSIRC= 16 MHz, VDD= 5 V±10%	0.7	-	4	mA
	IDD2 (IDLE)	fHSIRC= 16 MHz, VDD= 5 V±10%	0.5	-	3	mA
	IDD3 (STOP1)	STOP @ WDT on, VDD= 5.5 V±10%, TA= 25°C	–	-	22	μA
	IDD4 (STOP2)	STOP @ WDT off & LVR off, VDD= 5.5 V±10%, TA= 25°C	–	-	7	

NOTES:

1. All supply current items do not include the current of an internal WDTRC oscillator and a peripheral block.
2. All supply current items include the current of the power-on reset (POR) block.

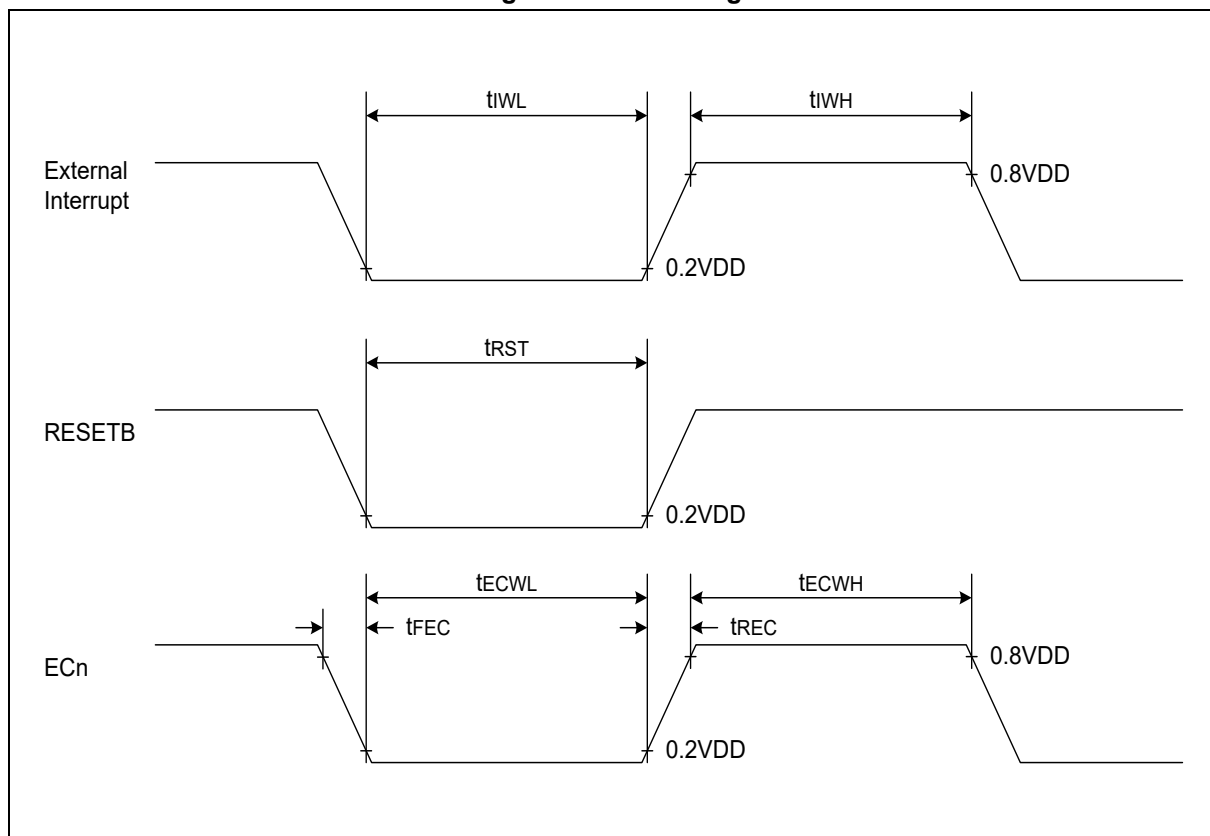
4.10 AC Characteristics

Table 38. AC Characteristics

(TA= -40°C to +85°C or TA= -40°C to +105°C, VDD= 2.0 V to 5.5 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
RESETB input low width	t_{RSL}	Input, VDD= 5 V	10	—	—	μs
Interrupt input high, low width	t_{INTH} , t_{INTL}	All interrupt, VDD= 5 V	200	—	—	ns
External Counter Input High, Low Pulse Width	t_{ECWH} , t_{ECWL}	ECn, VDD = 5 V (n= 0, 1, 3)	200	—	—	
External Counter Transition Time	t_{REC} , t_{FEC}	ECn, VDD = 5 V (n= 0, 1, 3)	20	—	—	

Figure 90. AC Timing



4.11 USART Characteristics

The following table and figures show USART timing condition in SPI or Synchronous mode operation.

Table 39. USART Timing Characteristics in SPI or Synchronous Mode Operations

($T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ or $T_A = -40^{\circ}\text{C}$ to 105°C , $V_{DD} = 1.8\text{ V}$ to 5.5 V)

Parameter		Symbol	Min.	Max.	Unit
System clock period (0.5 MHz ~ 16 MHz)		t_{SCLK}	62.5	2000	ns
Clock (XCK) period		t_{XCK}	$4 \times t_{\text{SCLK}}$	$1028 \times t_{\text{SCLK}}$	ns
Clock (XCK) high time		t_{XCKH}	$2 \times t_{\text{SCLK}}$	$514 \times t_{\text{SCLK}}$	ns
Clock (XCK) low time		t_{XCKL}	$2 \times t_{\text{SCLK}}$	$514 \times t_{\text{SCLK}}$	ns
Lead time	Master	t_{LEAD}	$0.5 \times t_{\text{XCK}}$	$0.5 \times t_{\text{XCK}}$	ns
	Slave	t_{LEAD}	$2 \times t_{\text{SCLK}}$	—	
Lag time	Master	t_{LAG}	$0.5 \times t_{\text{XCK}}$	$0.5 \times t_{\text{XCK}}$	ns
	Slave	t_{LAG}	$2 \times t_{\text{SCLK}}$	—	
Data setup time (inputs)	Master	t_{SIM}	$2 \times t_{\text{SCLK}}$	$2 \times t_{\text{SCLK}}$	ns
	Slave	t_{SIS}	$2 \times t_{\text{SCLK}}$	$2 \times t_{\text{SCLK}}$	
Data hold time (inputs)	Master	t_{HIM}	10	—	ns
	Slave	t_{HSI}	10	—	
Data setup time (outputs)	Master	t_{SOM}	$2 \times t_{\text{SCLK}}$	$2 \times t_{\text{SCLK}}$	ns
	Slave	t_{SOS}	$2 \times t_{\text{SCLK}}$	$2 \times t_{\text{SCLK}}$	
Data hold time (outputs)	Master	t_{HOM}	-10	—	ns
	Slave	t_{HOS}	-10	—	
Disable time		t_{DIS}	$1 \times t_{\text{SCLK}}$	$2 \times t_{\text{SCLK}}$	ns

NOTES:

1. In synchronous mode, Lead and Lag time for SS pin is ignored. And the case of "UCPHA=0" is also only applied to SPI mode.
2. All timing is shown between 20% VDD and 80% VDD.

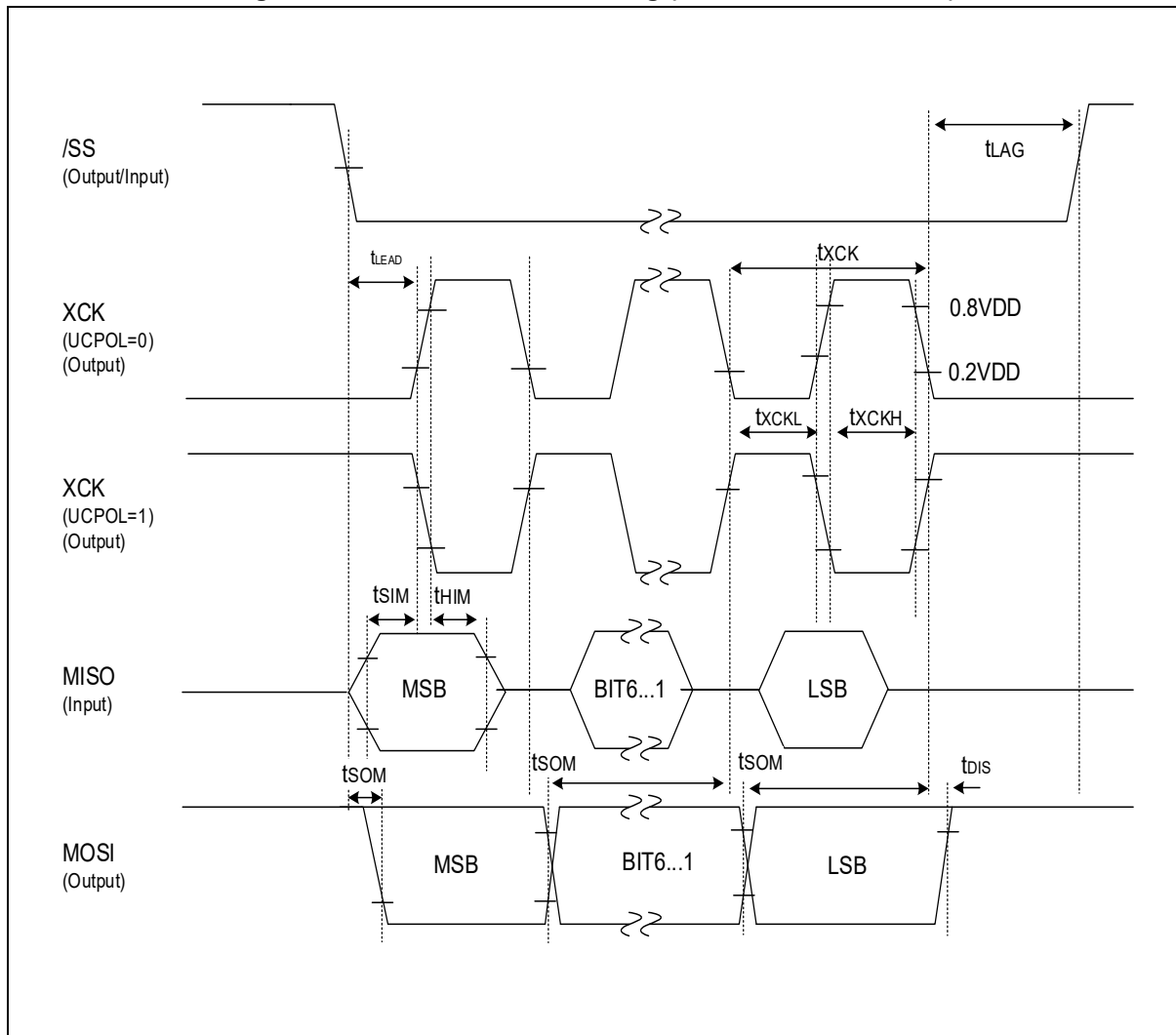
Figure 91. SPI Master Mode Timing (UCPHA = 0, MSB First)

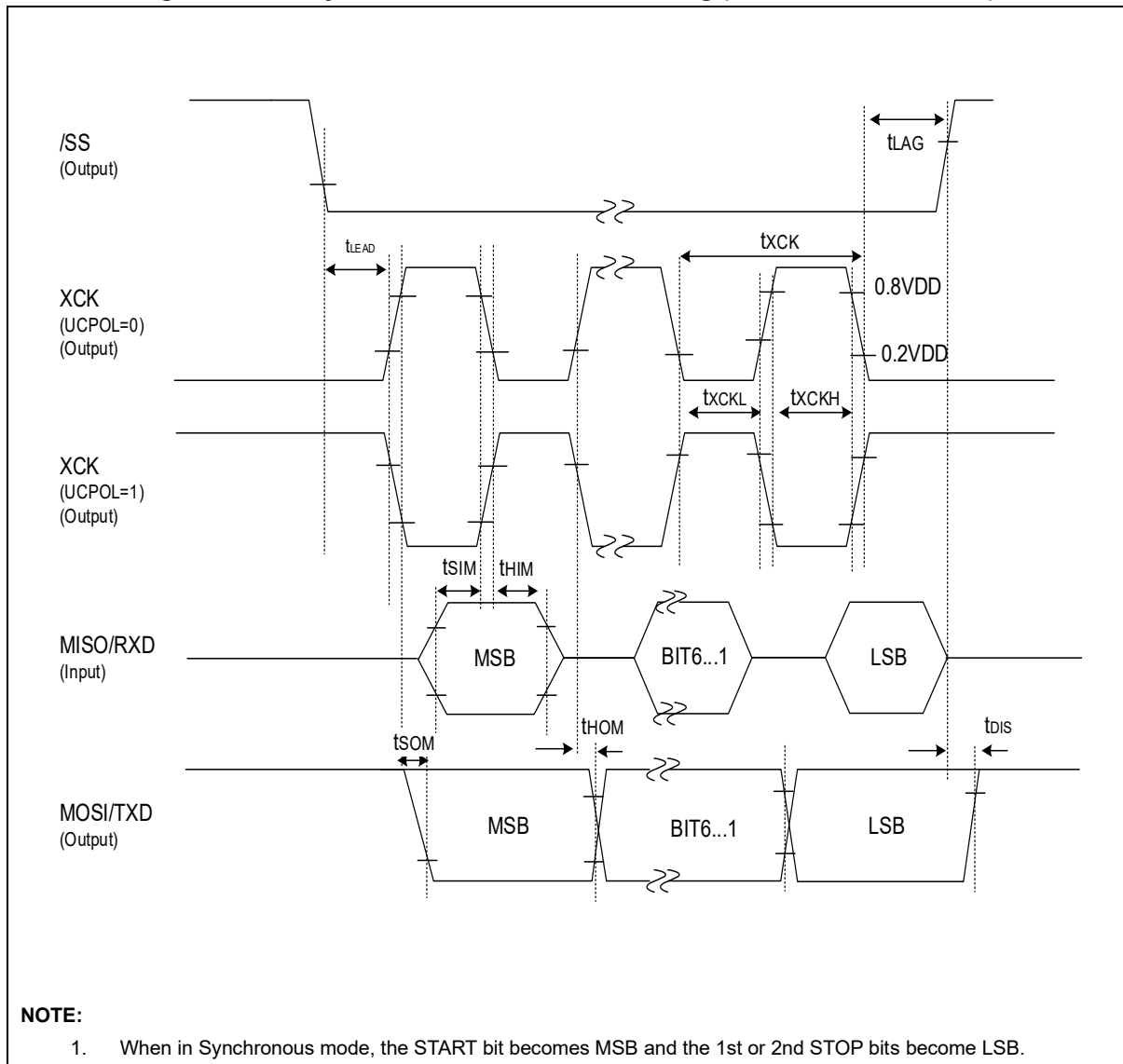
Figure 92. SPI/Synchronous Master Mode Timing (UCPHA = 1, MSB First)

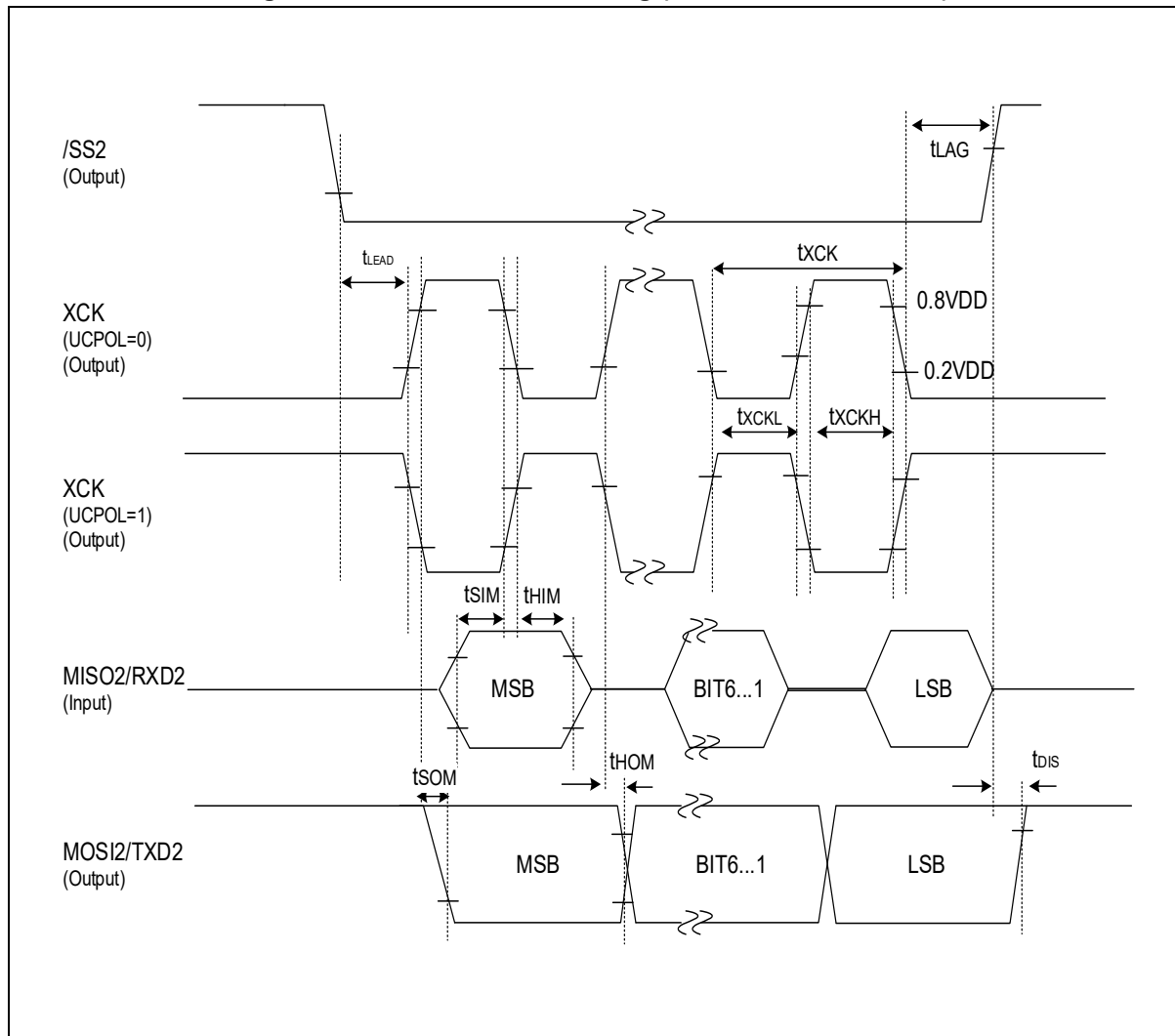
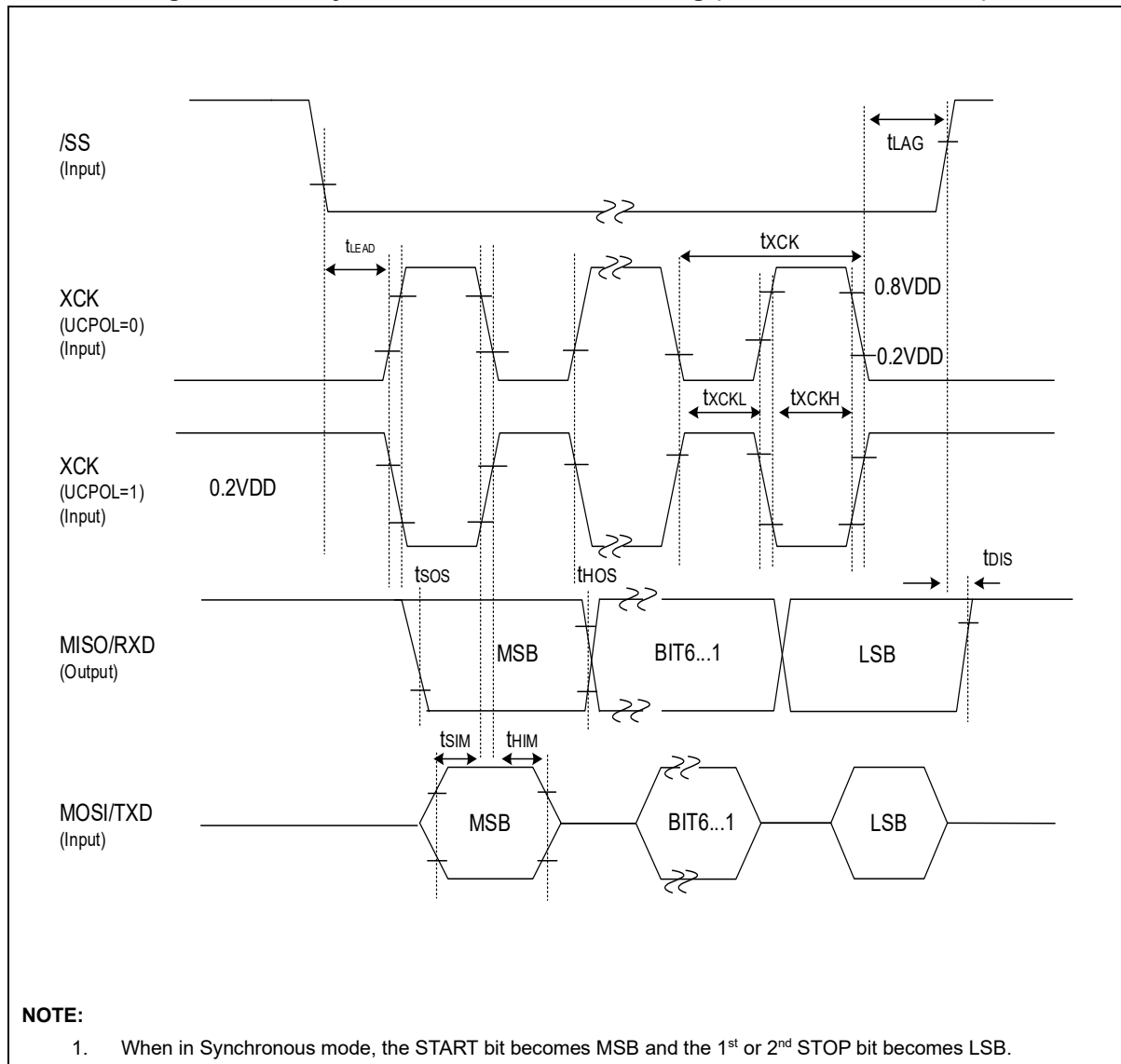
Figure 93. SPI Slave Mode Timing (UCPHA = 0, MSB First)

Figure 94. SPI/Synchronous Slave Mode Timing (UCPHA = 1, MSB First)

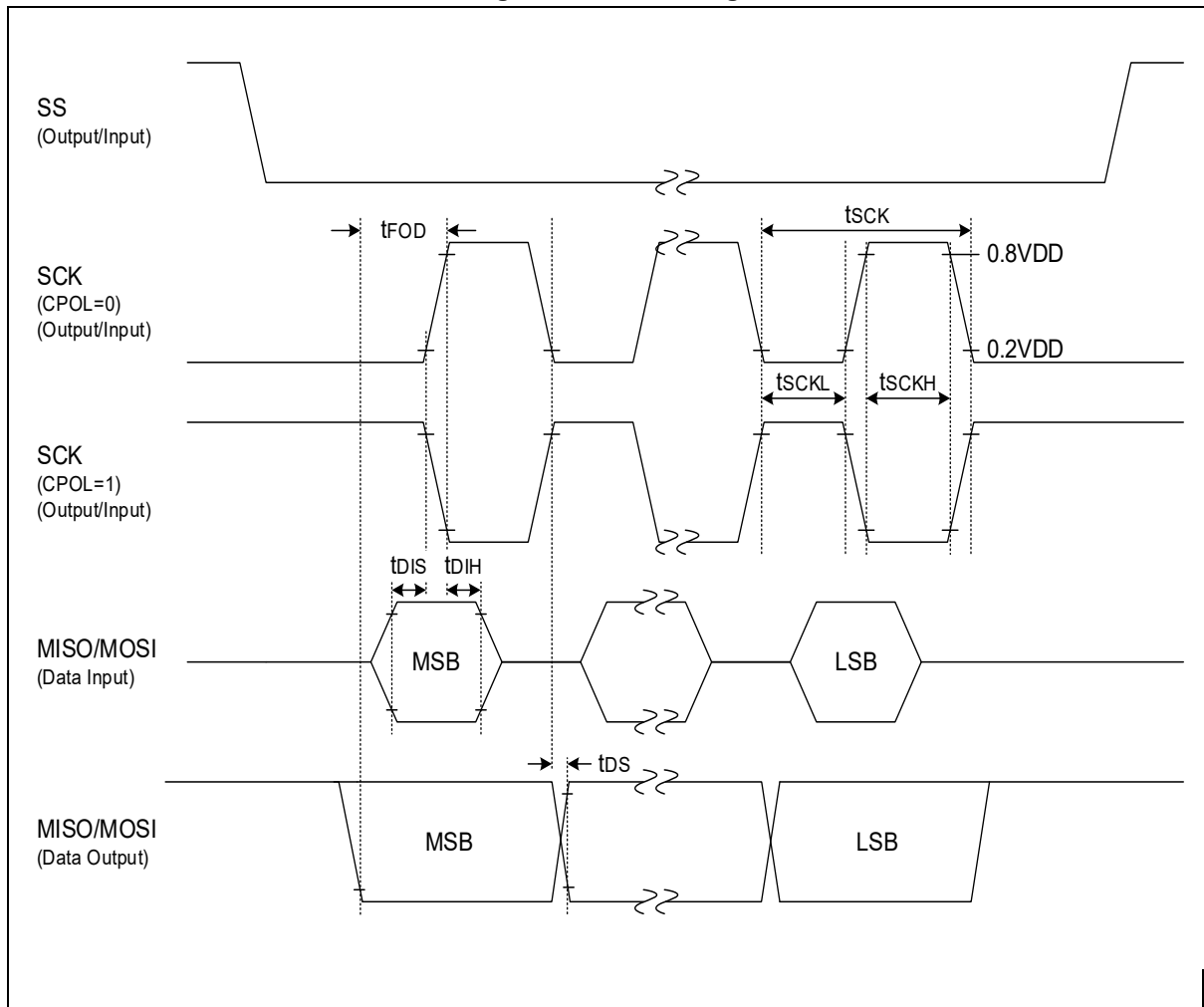
4.12 SPI Characteristics

Table 40. SPI Characteristics

(TA= -40°C to +85°C or TA= -40°C to 105°C, VDD= 2.0 V to 5.5 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Clock Pulse Period	tSCK	Internal SCK source	200	–	–	ns
Input Clock Pulse Period		External SCK source	200	–	–	
Output Clock High, Low Pulse Width	tSCKH,	Internal SCK source	70	–	–	
Input Clock High, Low Pulse Width	tSCKL	External SCK source	70	–	–	
First Output Clock Delay Time	tFOD	Internal/External SCK source	100	–	–	
Output Clock Delay Time	tDS	–	–	–	50	
Input Setup Time	tDIS	–	100	–	–	
Input Hold Time	tDIH	–	150	–	–	

Figure 95. SPI Timing



4.13 UART Characteristics

Table 41. UART Characteristics

(TA= -40°C to +85°C or TA= -40°C to 105°C, VDD= 2.0 V to 5.5 V, fSCLK=8 MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Serial port clock cycle time	t_{SCK}	1800	$t_{CPU} \times 16$	2200	ns
Output data setup to clock rising edge	t_{s1}	810	$t_{CPU} \times 13$	—	ns
Clock rising edge to input data valid	t_{s2}	—	—	590	ns
Output data hold after clock rising edge	t_{H1}	$t_{CPU} - 50$	t_{CPU}	—	ns
Input data hold after clock rising edge	t_{H2}	0	—	—	ns
Serial port clock High, Low level width	t_{HIGH}, t_{LOW}	720	$t_{CPU} \times 8$	1280	ns

Figure 96. Waveform for UART Timing Characteristics

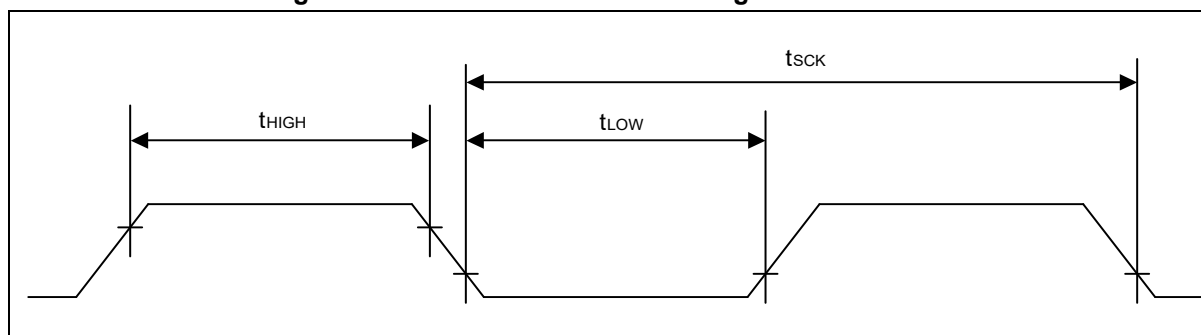
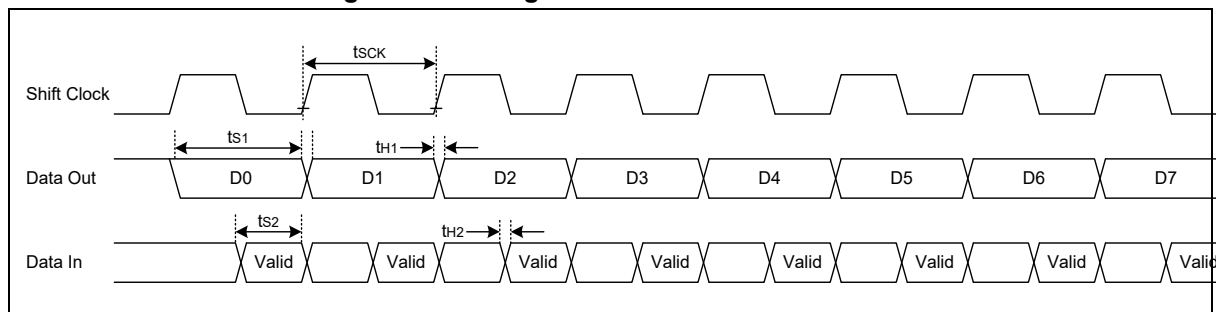


Figure 97. Timing Waveform for UART Module



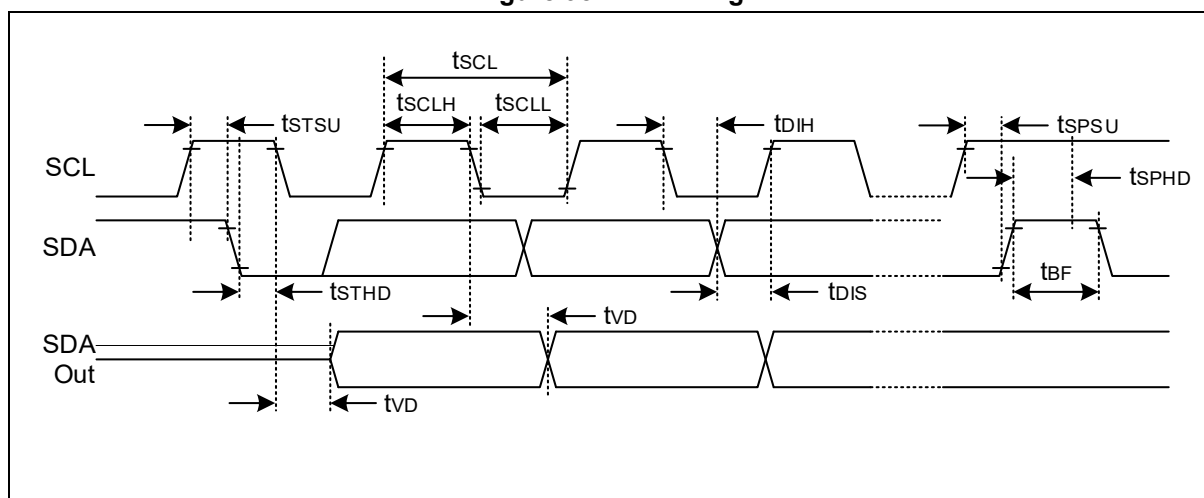
4.14 I2C Characteristics

Table 42. I2C Characteristics

(TA= -40°C to +85°C or TA= -40°C to 105°C, VDD= 2.0 V to 5.5 V)

Parameter	Symbol	Standard Mode		High-Speed Mode		Unit
		Min.	Max.	Min.	Max.	
Clock frequency	tSCL	0	100	0	400	kHz
Clock High Pulse Width	tSCLH	4.0	–	0.6	–	μs
Clock Low Pulse Width	tSCLL	4.7	–	1.3	–	
Bus Free Time	tBF	4.7	–	1.3	–	
Start Condition Setup Time	tSTSU	4.7	–	0.6	–	
Start Condition Hold Time	tSTHD	4.0	–	0.6	–	
Stop Condition Setup Time	tSPSU	4.0	–	0.6	–	
Stop Condition Hold Time	tSPHD	4.0	–	0.6	–	
Output Valid from Clock	tVD	0	–	0	–	
Data Input Hold Time	tDIH	0	–	0	1.0	ns
Data Input Setup Time	tDIS	250	–	100	–	

Figure 98. I2C Timing



4.15 Data Retention Voltage in STOP Mode

Table 43. Data Retention Voltage in STOP Mode

($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ or $T_A = -40^\circ\text{C}$ to 105°C , $V_{DD} = 2.0\text{ V}$ to 5.5 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data retention supply voltage	V_{DDDR}	—	2.0	—	5.5	V
Data retention supply current	I_{DDDR}	$V_{DDR} = 2.0\text{ V}$, ($T_A = 25^\circ\text{C}$), STOP mode	—	—	1	μA

Figure 99. STOP Mode Release Timing when Initiated by Interrupts

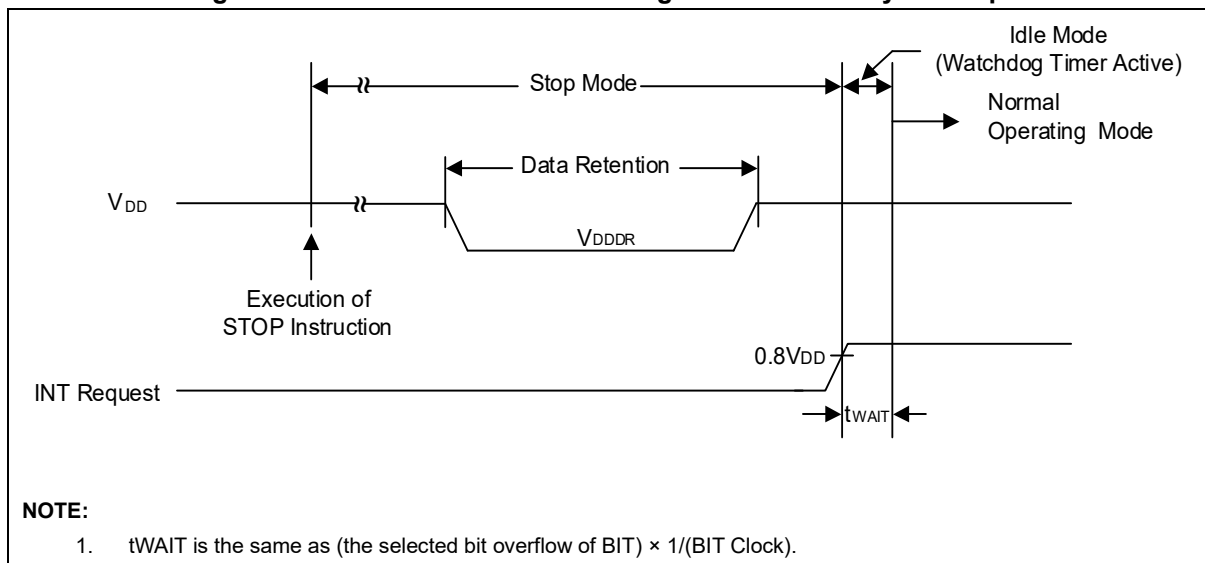
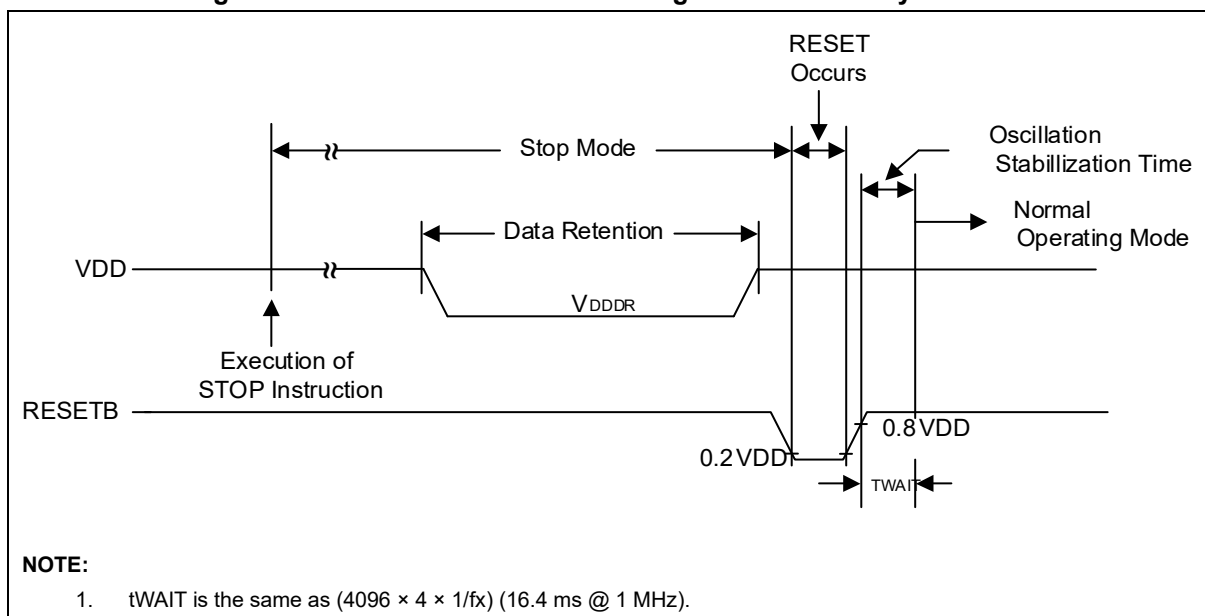


Figure 100. STOP Mode Release Timing when Initiated by RESETB



4.16 Internal Flash ROM Characteristics

Table 44. Internal Flash ROM Characteristics

(TA= -40°C to +85°C or TA= -40°C to 105°C, VDD= 2.0 V to 5.5 V, VSS= 0 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Max available clock Frequency	—	—	—	—	16	MHz
Normal Program Cycle Time	tPGMBUSY	—	21	25	32.5	μs
Normal Page Erase Cycle Time	tPERSBUSY	—	1.4	2	2.6	ms
Sector Erase Cycle Time	tSERSBUSY	—	1.4	2	2.6	ms
Chip Erase Cycle Time	tMERSBUSY	—	5.6	8	10.4	ms
Endurance of Write/Erase	NF _{WE}	TA=25°C, page unit	10,000	—	—	times
Retention time	tFRT	—	10	—	—	years

NOTE:

1. During a Flash operation, SCLK[1:0] of SCCR must be set to "00" or "01" (INT-RC OSC for system clock).

4.17 Input/Output Capacitance

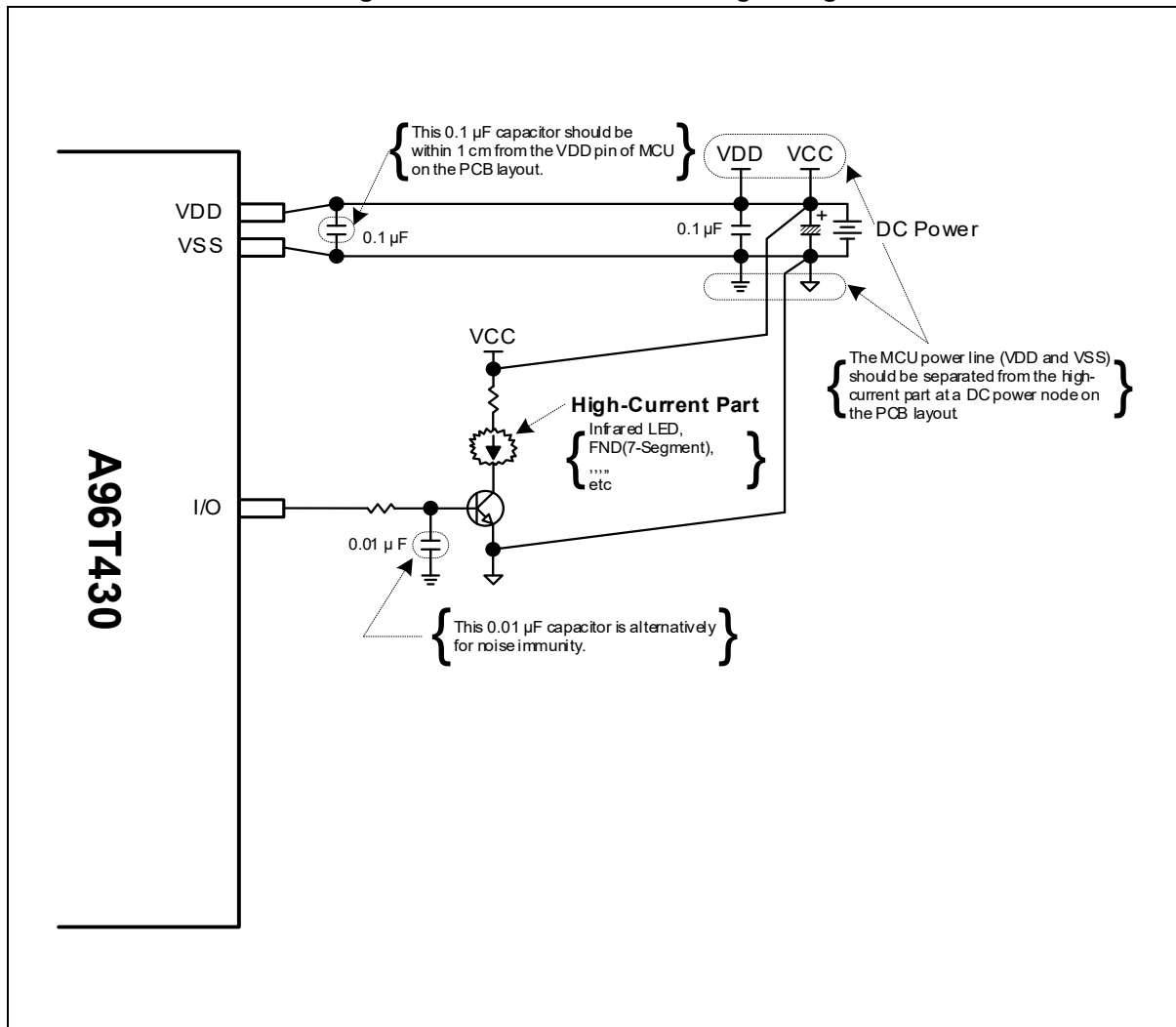
Table 45. Input/Output Capacitance

(TA= -40°C to +85°C or TA= -40°C to 105°C, VDD=0 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Capacitance	C _{IN}	fx= 1 MHz Unmeasured pins are connected to VSS	—	—	10	pF
Output Capacitance	C _{OUT}					
I/O Capacitance	C _{IO}					

4.18 Recommended Circuit and Layout

Figure 101. Recommended Voltage Range



4.19 Typical Characteristics

These graphs and tables provided in this section are only for design guidance and are not tested or guaranteed. In graphs or tables some data is out of the specified operating range (e.g. out of specified VDD range). This is only for information, and devices are guaranteed to operate properly only within the specified range.

Figure 102. IDD1 (RUN) Current

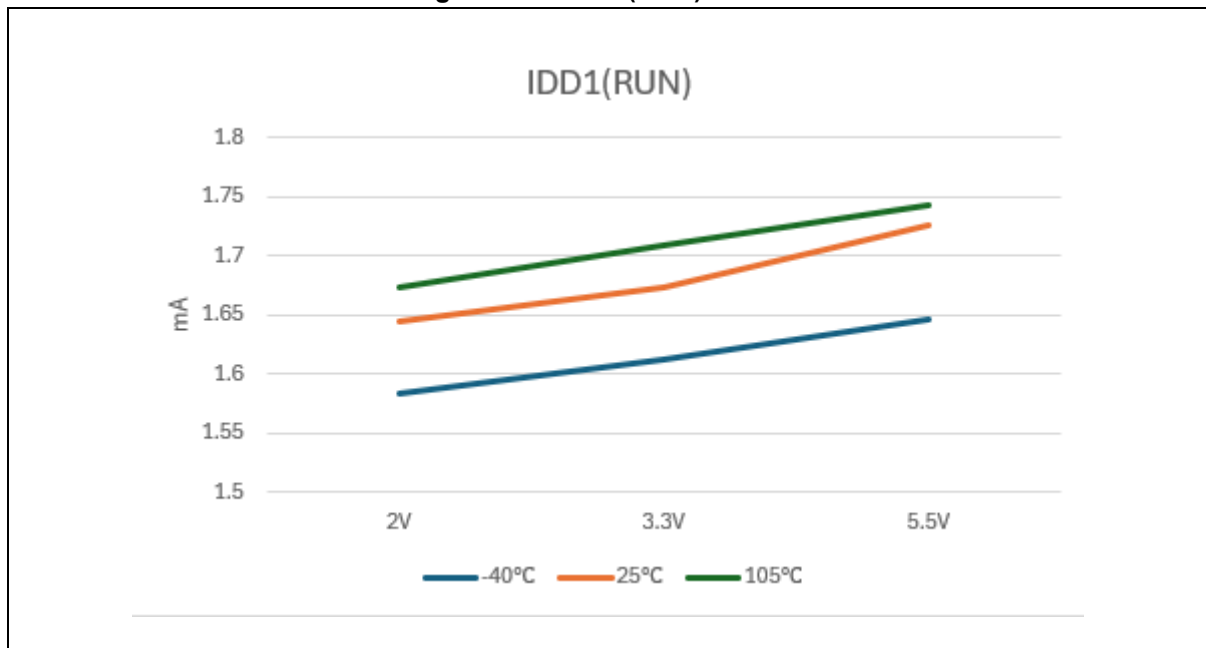


Figure 103. IDD2 (IDLE) Current

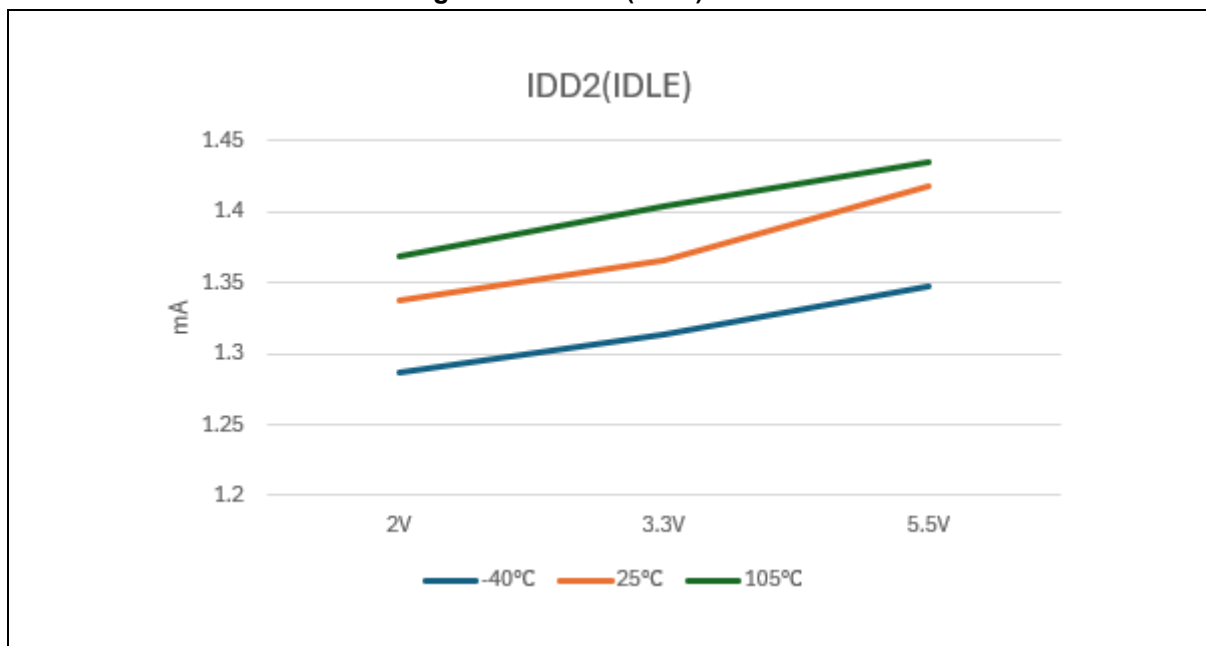


Figure 104. IDD3 (STOP1) Current

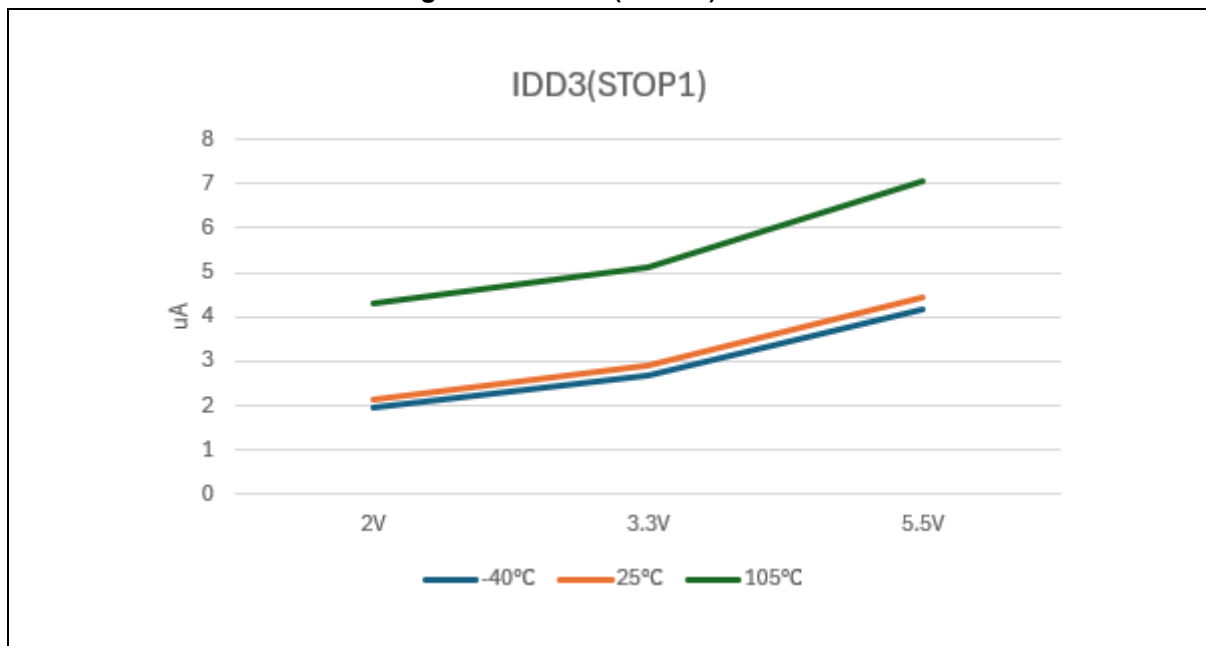
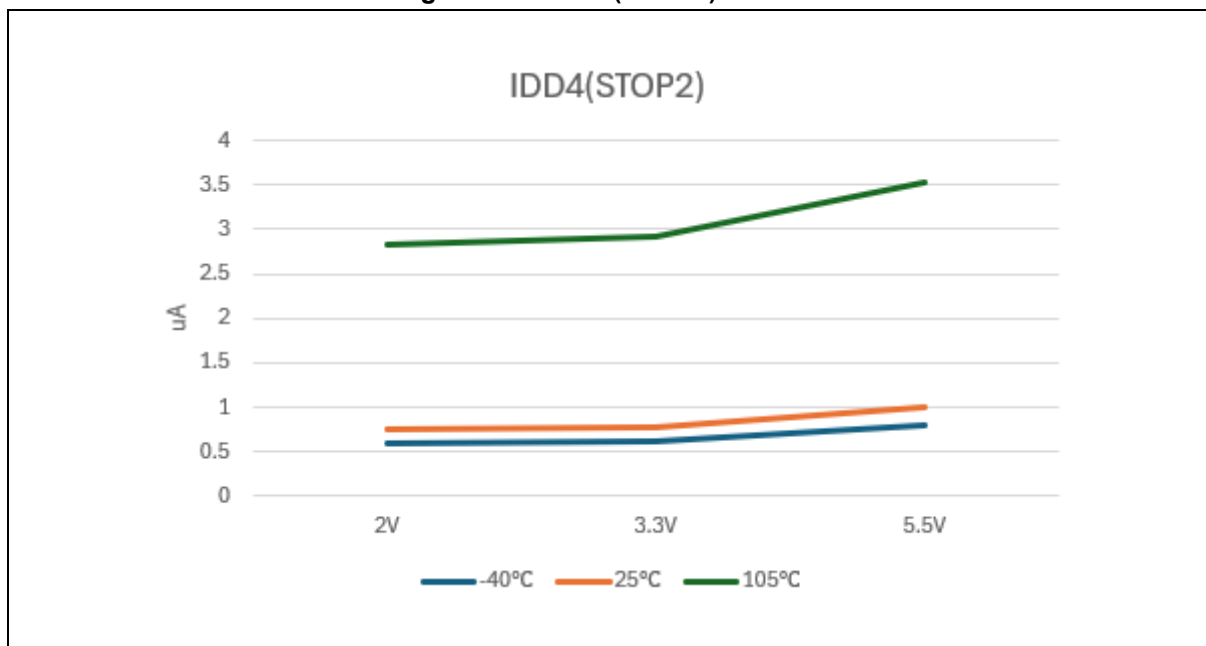


Figure 105. IDD4 (STOP2) Current

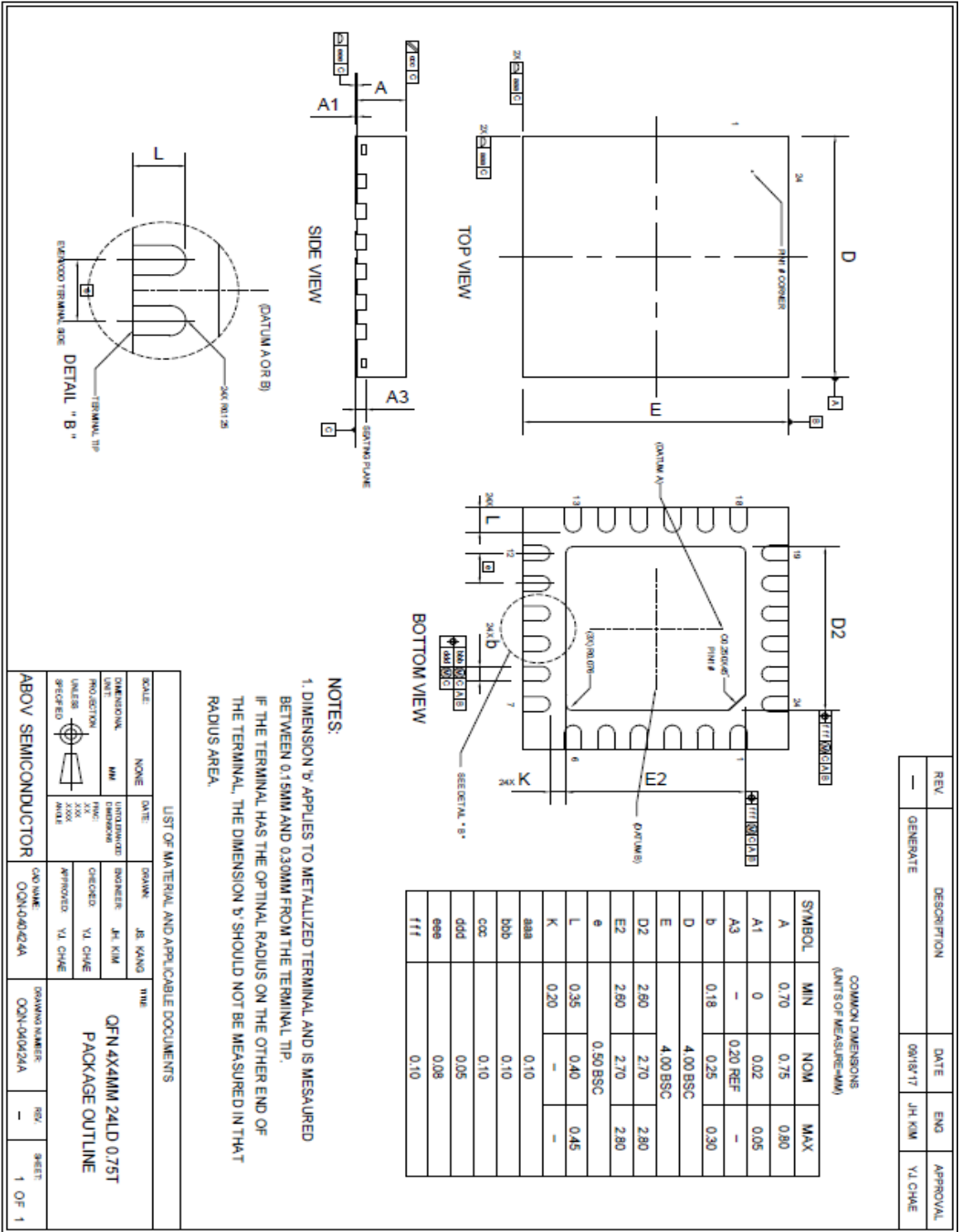


5. Package Information

5.1 24-QFN Package Information

24-QFN is a 24-pin, 4x4 mm Quad Flat No-lead Package.

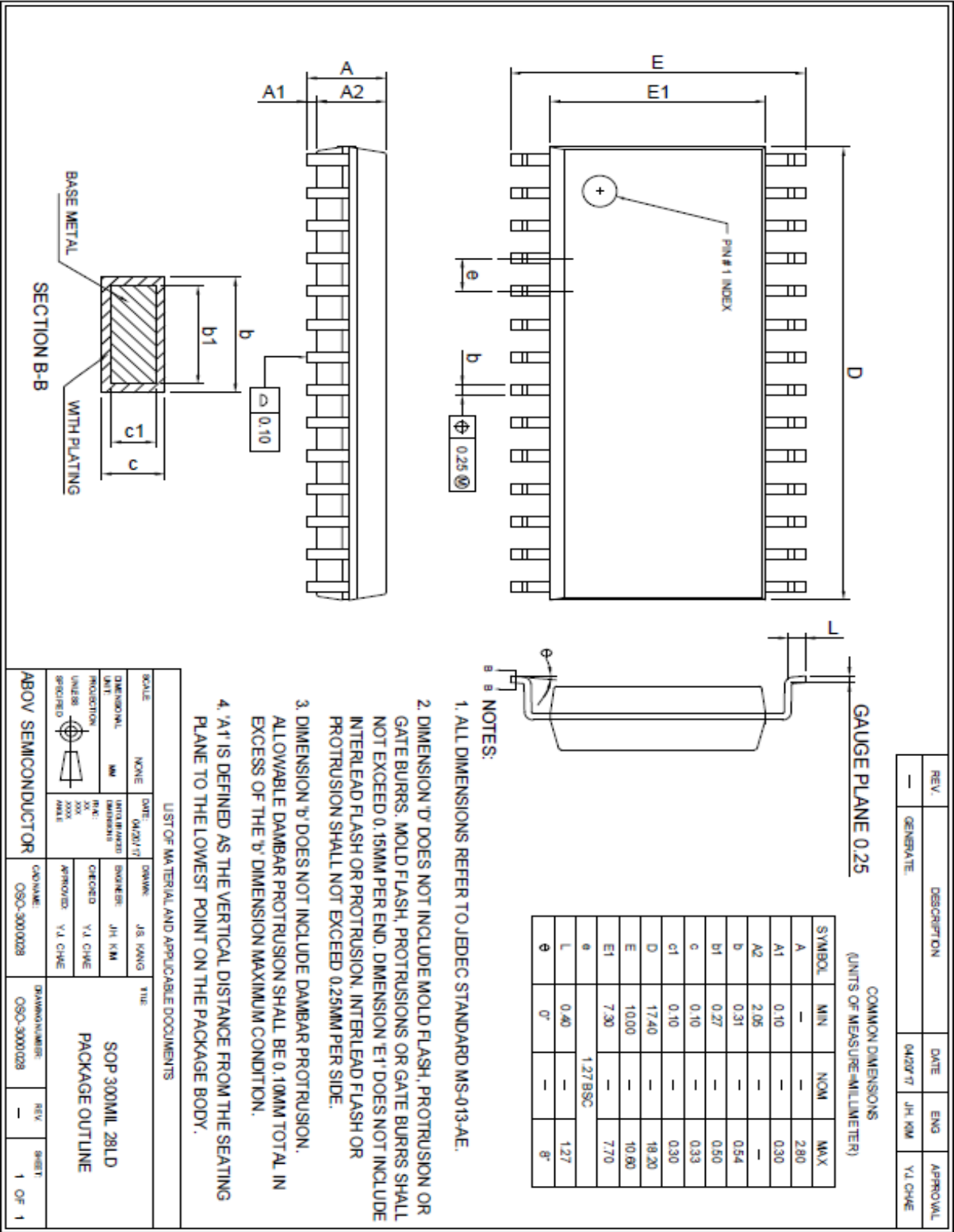
Figure 106. Package Dimension (24-QFN)



5.2 28-SOP Package Information

28-SOP is a 28-pin 300-MIL Small Outline Package.

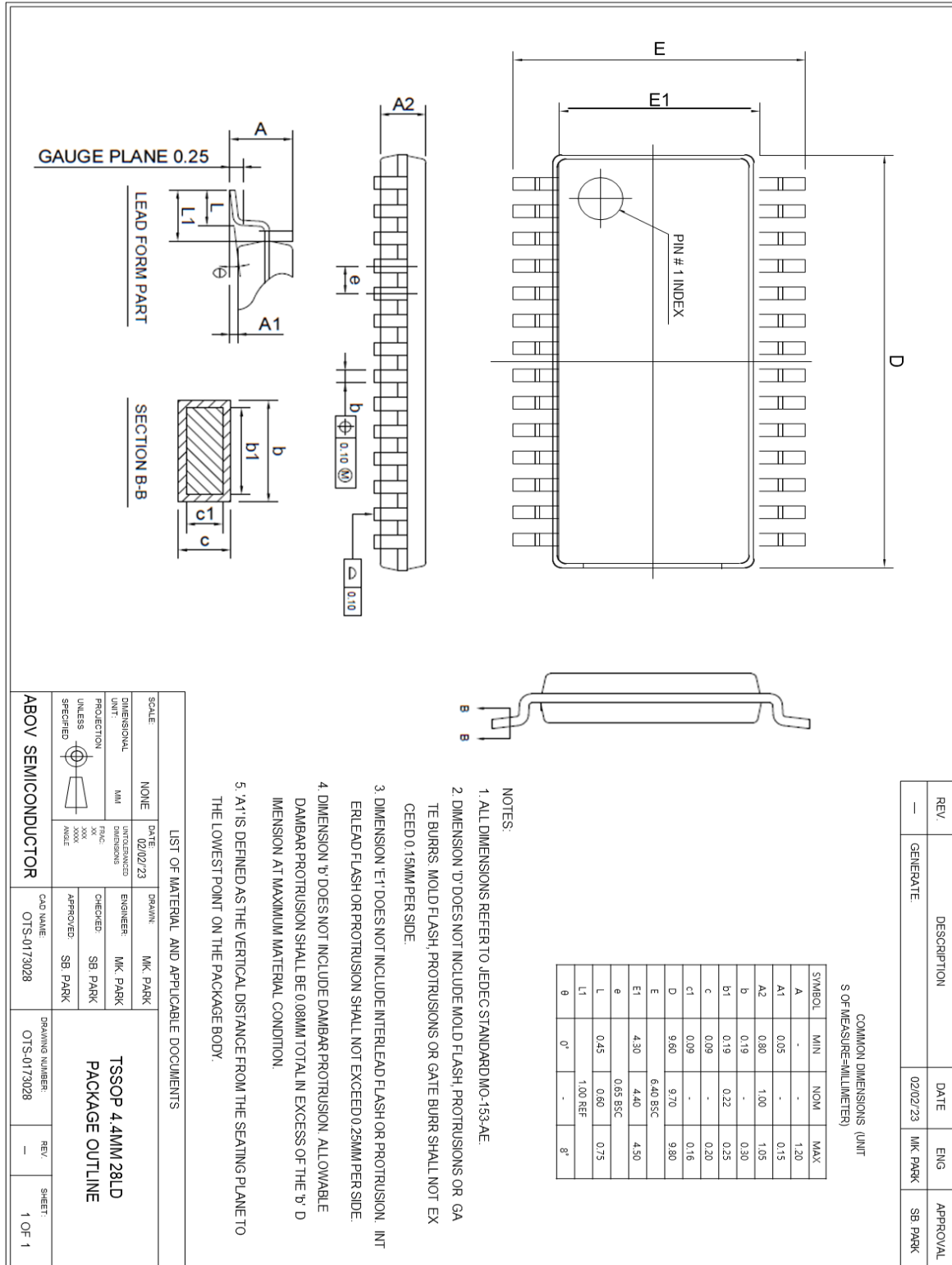
Figure 107. Package Dimension (28-SOP)



5.3 28-TSSOP Package Information

28-TSSOP is a 28-pin 170-MIL Small Outline Package.

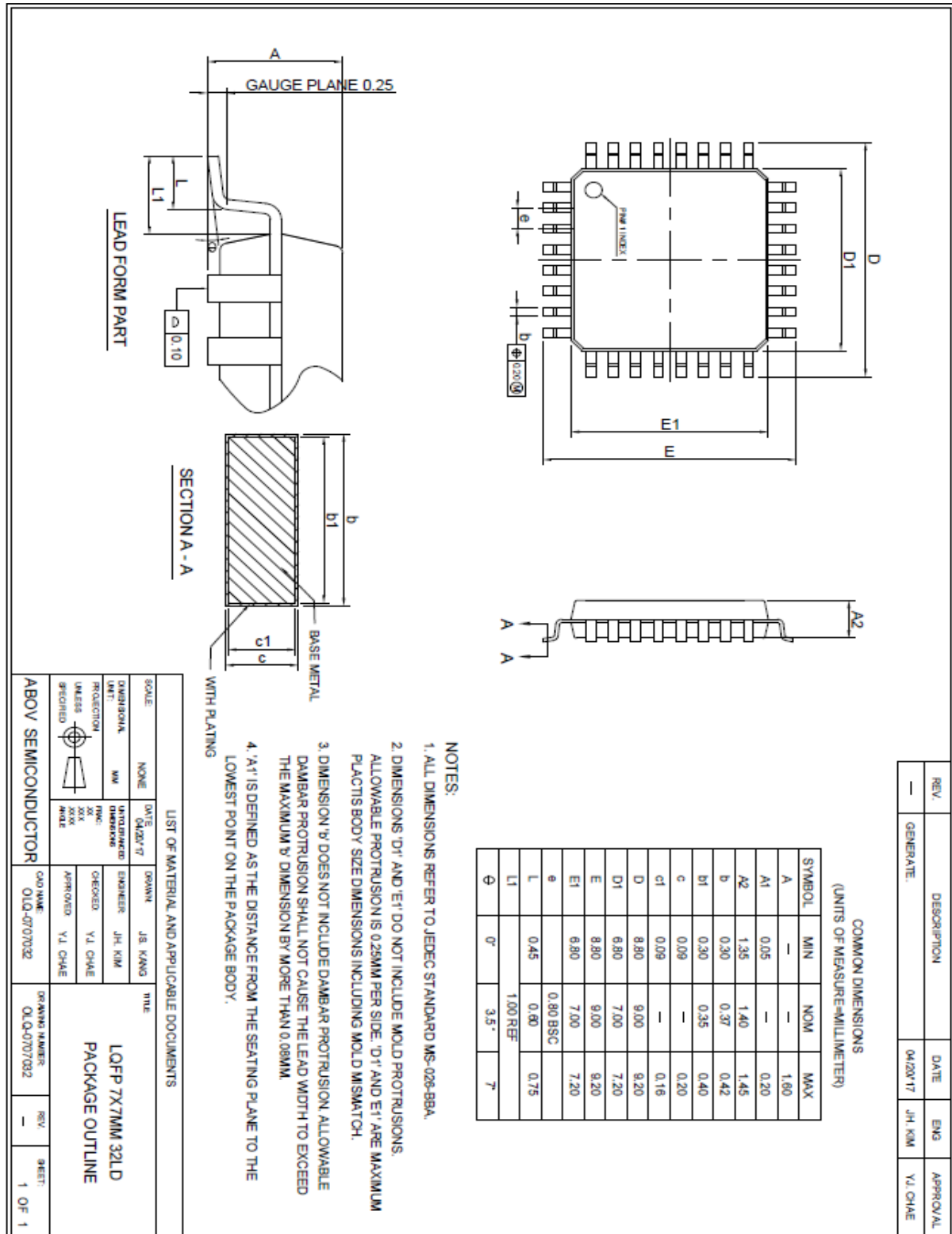
Figure 108. Package Dimension (28-TSSOP)



5.4 32-LQFP Package Information

32-LQFP is a 32-pin, 7x7 mm Quad Flat Package.

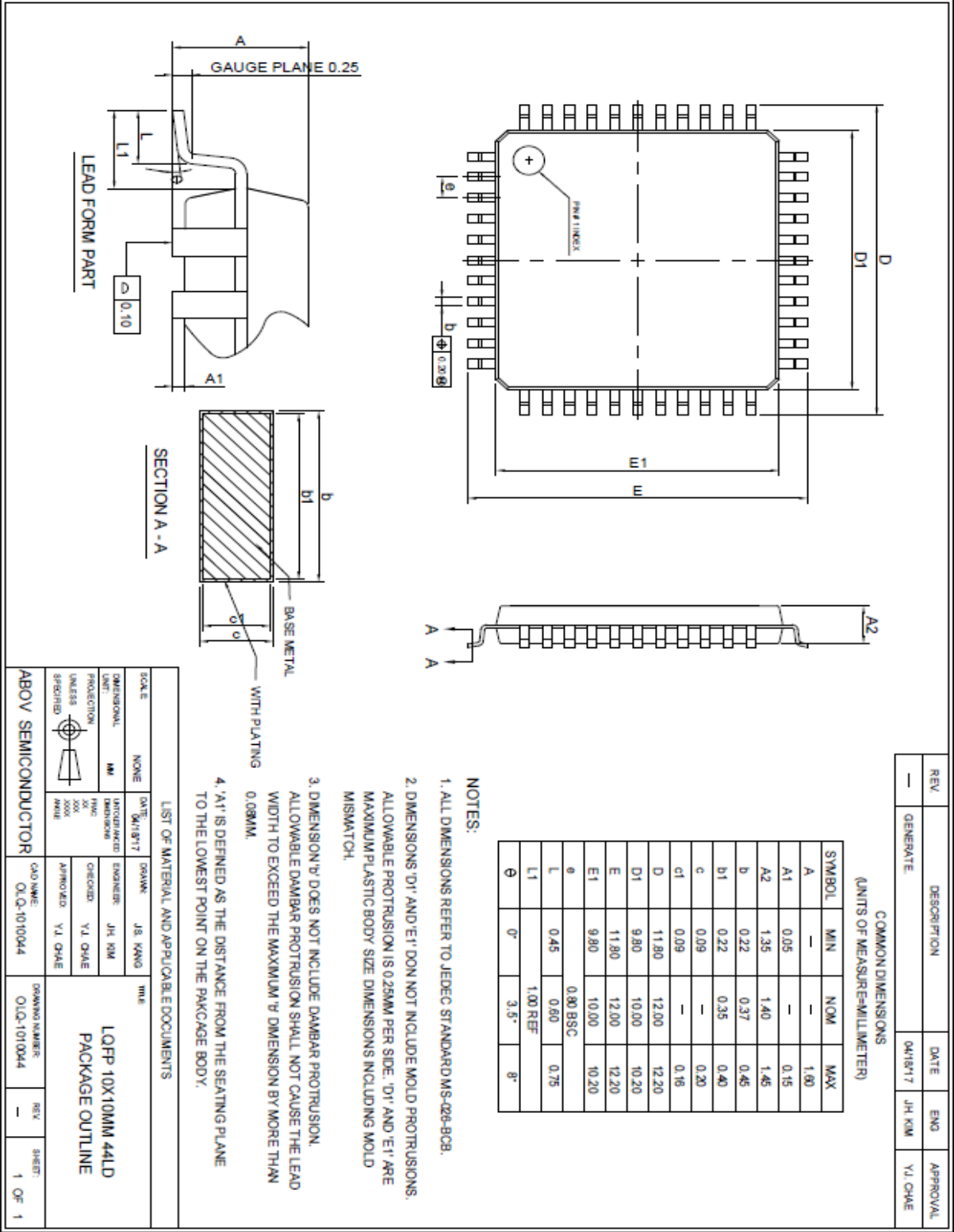
Figure 109. Package Dimension (32-LQFP)



5.5 44-LQFP Package Information

44-LQFP is a 44-pin, 10x10 mm Quad Flat Package.

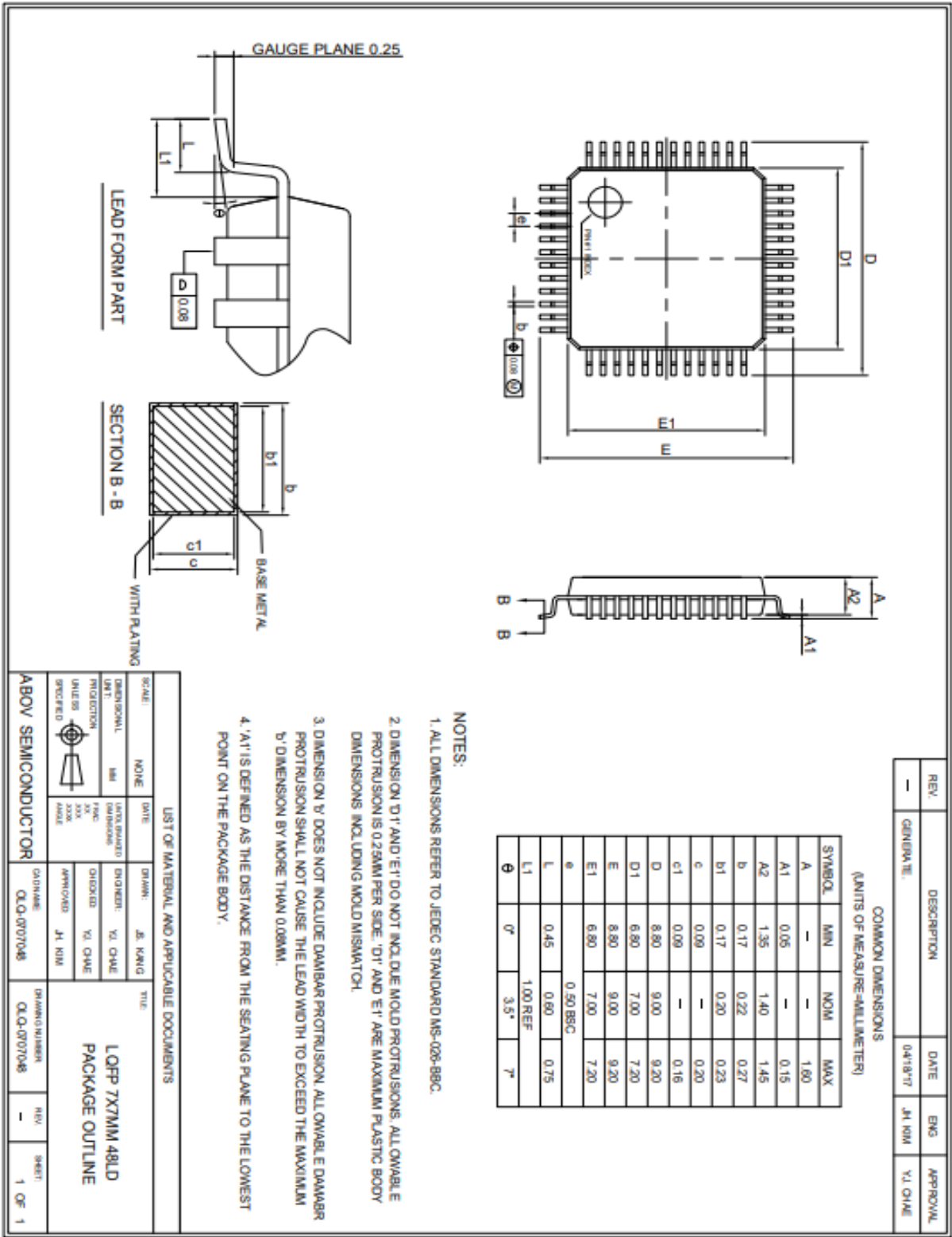
Figure 110. Package Dimension (44-LQFP)



5.6 48-LQFP Package Information

48-LQFP is a 48-pin, 7x7 mm Quad Flat Package.

Figure 111. Package Dimension (48-LQFP)



6. Ordering Information

Figure 112. A96T430 Device Numbering Nomenclature

		A96T4	X	X	C	L	()	N	(T)
Device family name									
A96T4 Family Name									
Version									
3	version								
Memory									
0	64 KB								
Pin count									
C	48-pin								
S	44-pin								
K	32-pin								
G	28-pin								
L	24-pin								
Package type									
L	LQFP1 (0.5 mm pin pitch)								
N	LQFP3 (0.8 mm pin pitch)								
U	QFN1 (0.5 mm pin pitch)								
D	SOP (1.27mm pin pitch)								
R	TSSOP (0.65 mm pin pitch)								
Temperature									
None	-40°C to +85°C								
2	-40°C to +105°C								
Bonding wire									
None	Au wire								
N	Pd-Cu wire								
Packing									
(T)	Tape & reel								
(W)	Wafer								
(C)	Chip carrier								

Revision History

Revision	Date	Notes
1.00	May 23, 2025	Initial release
1.01	Jun. 18, 2025	Corrected typos.
1.02	Jun. 16, 2025	Added the 28-TSSOP package and updated the details.
1.03	Dec. 3, 2025	Spec updates for items 4.1 and 4.9 of the Electrical Characteristics
1.04	Jan. 27, 2026	Spec updates for items 4.6 and 4.16 of the Electrical Characteristics
1.05	Apr. 29, 2026	Part Number Change: A96T430KLN to A96T430KNN
1.06	Aug. 18, 2026	Updated the Development Tools chapter and fixed typos

Korea**Regional Office, Seoul
R&D, Marketing & Sales**

8th Fl., 330, Yeongdong-daero, Gangnam-gu, Seoul,
06177, Korea

Tel: +82-2-2193-2200

Fax: +82-2-508-6903

www.abovsemi.com

HQ, Ochang**R&D, QA, and Test Center**

37, Gangni 1-gil, Ochang-eup, Cheongwon-gun,
Chungcheongbuk-do, 28126, Korea

Tel: +82-43-219-5200

Fax: +82-43-217-3534

www.abovsemi.com

Domestic Sales

Tel: +82-2-2193-2206

Fax: +82-2-508-6903

Email: sales_kr@abov.co.kr

Global Sales

Tel: +82-2-2193-2281

Fax: +82-2-508-6903

Email: sales_gl@abov.co.kr

China Sales

Tel: +86-755-8287-2205

Fax: +86-755-8287-2204

Email: sales_cn@abov.co.kr

Japan Sales

Tel: +81-6-6225-7758

Email: sales_jp@abov.co.kr

ABOV Disclaimer**IMPORTANT NOTICE – PLEASE READ CAREFULLY**

ABOV Semiconductor (“ABOV”) reserves the right to make changes, corrections, enhancements, modifications, and improvements to ABOV products and/or to this document at any time without notice. **ABOV DOES NOT GIVE WARRANTIES AS TO THE ACCURACY OR COMPLETENESS OF THE INFORMATION INCLUDED HEREIN.** Purchasers should obtain the latest relevant information on ABOV products before placing orders. Purchasers are entirely responsible for the choice, selection, and use of ABOV products and ABOV assumes no liability for application assistance or the design of purchasers’ products. **NO LICENSE, EXPRESS OR IMPLIED, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY ABOV HEREIN. ABOV DISCLAIMS ALL EXPRESS AND IMPLIED WARRANTIES AND SHALL NOT BE RESPONSIBLE OR LIABLE FOR ANY INJURIES OR DAMAGES RELATED TO USE OF ABOV PRODUCTS IN SUCH UNAUTHORIZED APPLICATIONS.** ABOV and the ABOV logo are trademarks of ABOV. For additional information about ABOV trademarks, please refer to https://www.abovsemi.com/en/about/corporate_identity.php. All other products or service names are the property of their respective owners. Information in this document supersedes and replaces the information previously supplied in any former versions of this document.

© 2025 - 2026 ABOV Semiconductor – All rights reserved