A34M466, A34M464 Datasheet

Cortex-M4 32-bit Microcontroller + FPU, 120 MHz, Up to 256 KB Code Flash, 16 KB SRAM, 3-Phase PWM, 12-bit ADC for Motor Control Applications

DS Rev. 1.02

Features

Core

- Arm 32-bit Cortex-M4 CPU
- Up to 120 MHz with FPU, 175 DMIPS
- Cache buffer (Flash accelerator) support

Memories

- 128 KB / 256 KB of Code Flash
- Up to 16 KB of SRAM
- Error Correction Code (ECC)

Reset and Power Management

- Power-on/power-down reset (POR/LVR/LVI)
- Low-power modes: SLEEP, DEEP-SLEEP

Clock Management

- High-speed internal (HSI) oscillator 8 MHz
  - ±2.0% @ -40°C to 105°C
- Low-speed internal oscillator 500 kHz (LSI)
  - ±30% @ -40°C to +105°C
- External main oscillator (HSE)
  - 4 MHz to 12 MHz
- PLL (Phase-locked loop) frequency generator
  - Up to 120 MHz

GPIO

- Up to 42 general-purpose I/O pins with interrupt capability
- All mappable on external interrupt vectors
- Multi-function pins have up to five selections of functions, including GPIO.

WDT

- 32-bit down-count timer
- Reset and periodic interrupts
- Eight prescaler selection

FRT

- 32-bit free-run timer

16-bit Timer

- 6 units of general-purpose timers
- 6 channel I/Os
  - 6 timer n capture port input channels
  - 6 timer n output port output channels
- Timer operating modes
  - Periodic timer mode
  - One-shot mode
  - PWM mode
  - Capture mode
- 10-bit prescaler

MPWM

- One Motor PWM generator
- Six channels (high and low signals of phases U, V, and W) generate different waveforms.
- 16-bit up and up/down-counters
- Eight ADC trigger sources
  - 6-Variable Triggers
  - 2-Fixed Trigger (Bottom, Period Match)

12-bit ADC

- Two independent ADC blocks
- Up to 2.0 Msps sampling rate
- 20 external analog input channels
- Adjustable sample and hold time
- Multiple operating modes:
  - Single conversion
  - Sequence conversion
  - Burst conversion
  - Multiple conversion
  - Inject conversion

OPAMP

- Three-unit
- Compatible with ADC for joint operation

10-bit DAC
- One unit
- DACO output channels

DMA Controller
- 4-channel DMA Controller
- 8-/16-/32-bit data transfers
- Operates in conjunction with 6 types of peripherals

Serial Interfaces
- UART (2 units)
- SPI (1 unit)
- I2C (1 unit)

CRC Calculation Unit
- CRC operating modes:
  - CRC32 (0x04C1_1DB7)
  - CRC16 (0x8005)
  - CRC8 (0x07)
  - CRC7 (0x09)
- Support for byte reversal of input/output data
- Compatible with DMA

Development Support
- Serial Wire Debug (SWD)

Package
- 48-LQFP-7x7

Operating Voltage
- 2.7 V to 5.5 V

Operating Temperature
- Commercial grade (-40°C to + 105°C)

Applications
- Inverter motor controller
- Compressor and Fan
- Air-conditioner, Refrigerator

Product Selection Table

Table 1. Device Summary

Device Name	Code Flash	SRAM	SPI	UART	I2C	MPWM	ADC	I/O Ports	Package
A34M466CL2N	256 KB	16 KB	1	2	1	1	20	42	48-LQFP-7x7
A34M464CL2N	128 KB	16 KB	1	2	1	1	20	42	48-LQFP-7x7

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1. Descriptions

1.1 General Information

The A34M46x series is a 32-bit high-performance microcontroller with up to 256 KB of flash memory. It is a powerful microcontroller that provides effective solutions to various electrical appliances that require both low power consumption and high performance (Arm Cortex-M4 with FPU core).

The A34M46x series is a 32-bit microcontroller based on the high-performance Arm Cortex-M4F+ core. It has up to 256 KB of code flash memory, and 16 KB of SRAM. It is well-suited for a wide range of home appliances, such as air conditioners, refrigerators, washing machines, clothes dryers, dishwashers, water purifiers, and blenders. It is also suitable for use in high-performance inverters for motor control.

1.2 Product Category Definition

Table 2 provides an overview of the memory capacity for available devices in the A34M46x series.

This document provides an overview of each device's supported features, including high-level information and brief explanations for each feature.

Refer to Table 3 for the list of features supported by each product category.

Table 2. A34M46x Series Memory Density

Memory Density		Category
Flash	**RAM**	
256 KB	16 KB	A34M466
128 KB	16 KB	A34M464

1.3 Availability of Peripherals

Table 3 summarizes and lists product-specific features available in the A34M46x series, considering the largest package.

Table 3. A34M46x Series Features and Peripherals

Peripherals		Description
Core	CPU	• Maximum operating frequency: 120 MHz • 32-bit Arm Cortex-M4F CPU - 32-bit Thumb®-2 instruction set • Register settings in CPU: - General-purpose registers specified - Main stack pointer (MSP) and process stack pointer (PSP): R13 - Link register (LR): R14 - Program counter (PC): R15 • Data ordering format: Little-Endian • Harvard Architecture • AHB/APB
	Interrupt	• NVIC (Nested-Vectored Interrupt Controller) • Up to 48 peripheral interrupts supported • Assignable with 16 different priority levels
	FPU	• Rendered by extending and transforming the ARMv7 floating-point arithmetic functionality • Compliant with the ANSI/IEEE 754 standard • Capable of binary floating-point arithmetic and computation

Table 3. A34M46x Series Features and Peripherals (continued)

Peripherals		Description
Memory	Code Flash	• Capacity: - A34M466: 256 KB Code Flash memory - A34M464: 128 KB Code Flash memory • 512 bytes, 2 KB erases • Bulk (chip) erase • Read protection • Self-programming • CRC code generation and verification for the Flash memory • Endurance: 10,000 cycles • Lifetime: 10 years
	BootROM	• Executes the processor's boot mode when receiving an input at the nBOOT pin from an external circuit • UART boot modes • In-system programming • A user can program data into the internal Flash memory by setting up an application board.
	SRAM	• Capacity: 16 KB • Usable as a program's work area • High-speed execution enables the execution of time-critical codes • Part of the SRAM can be remapped into an interrupt vector area
SCU (System Control Unit)	Clock	• High-speed internal oscillator (HSI) - 8 MHz (±2.0% @ -40°C to +105°C) • Low-speed internal oscillator (LSI) - 500 kHz (±30% @-40°C to +105°C) • External main oscillator (HSE): 4 MHz to 12 MHz • PLL (Phase-locked loop) frequency generator generates a high-speed clock (up to 120 MHz)
	Clock Monitoring	• System Fail-Safe function by Clock Monitoring - External main oscillator (HSE) - Main system clock (MCLK)

Table 3. A34M46x Series Features and Peripherals (continued)

Peripherals		Description
SCU (System Control Unit)	Reset	• nRESET pin reset • Core reset • Software reset • POR (Power-On Reset) • LVR (Low-Voltage Reset) • WDTR (Watch Dog Timer Reset) • Reset due to clock oscillating error
	LDO	LDO (Low-dropout) regulator built in for low-voltage operation
	POR	The POR generator detects an internal 1.92 V voltage and generates a reset signal.
	LVI	• 10 low-voltage detection levels • Supports interrupts • Supports wake-up from SLEEP mode
	Wake-up	• Wake-up by GPIO pins • Wake up by FRT (Free-run Timer) • Wake-up by WDT (Watchdog Timer) • Wake-up by LVI (Low-Voltage Indicator)
GPIO (General-Purpose I/O)		• I/O ports for general purpose • 48-LQFP I/O pins: 42 • Each pin can be set for one of the following modes: - Push-pull output - Open drain output - Input • The use of each pin can be set by setting the multiplexer. • Each pin can be configured as an external interrupt source, either the high-level/low-level interrupt or the rising-edge/falling-edge interrupt • Pull-up or pull-down resistor, and debouncing can be set for each pin. • Drive strength can be adjusted for each port pin. • Each pin bit can be individually set or reset. • Wake-up events triggered by external asynchronous inputs

Table 3. A34M46x Series Features and Peripherals (continued)

Peripherals		Description
DMA (Direct Memory Access Controller)		• 4-channel DMA supports peripherals • 8-/ 16-/ 32-bit data transfers • Operates in conjunction with 6 types of peripherals - SPI (SPI) - UARTx (UART0, UART1) - CRC - ADC (ADC0, ADC1)
TIMER	16-bit timer	• General-purpose 16-bit up-count timer • 6 channels - 6 timer n capture port (TnIO) input channels - 6 timer n output port (TnIO) output channels • Timer operating modes - Periodic timer mode - One-shot mode - PWM mode - Capture mode • Interrupt events - Timer/counter-match interrupt - Timer overflow interrupt • Input clock selection - Clocks are freely selectable through the miscellaneous clock control registers (SCU_MCCRx) - External clocks are selectable • Timer signals can be generated through TnIO pins • 10-bit prescaler
	WDT	• 32-bit down-count timer • Reset and periodic interrupts • Clocks are freely selectable through the miscellaneous clock control registers (SCU_MCCRx) • Eight different prescalers are selectable
	FRT	• One unit • 32-bit free-run timer - Capable of calculating the internal system time - 32-bit up-count timer • Interrupt events - Period interrupt - Overflow interrupt

Table 3. A34M46x Series Features and Peripherals (continued)

Peripherals		Description
TIMER	MPWM (Motor Pulse-Width Modulator)	• One unit • Motor PWM generator • Six channels (high and low signals of phases U, V, and W) generate different waveforms • 16-bit up counter and up-down counter • Eight ADC Trigger Source - 6-Variable Triggers - 2-Fixed Trigger (Bottom, Period Match) • Interrupt events - Bottom interrupts - Top (period) interrupts - Interval interrupt mode • Falling/rising dead-time applicable • A special operating mode: • Protection and over-current detection supported
Serial Interface	UART	• Two units • A total of six 16450 asynchronous serial communication ports • Configurable standard asynchronous communication bits (start, stop, and parity) • Flexible communication available through programming - 5- to 8-bit data transfers - Even/Odd/Non-parity generation and checking - 1-bit, 1.5-bit, or 2-bit stop-bit generation and checking • 8-bit fraction controller and 16-bit baud rate generator
	SPI	• One unit • Two synchronous serial communication port channels • Master/slave operation • Loop-back mode • Programmable and flexible communication • 8-/9-/16-/17-bit data transmit/receive - SPI clock speed - Both least significant bit (LSB)-first and most significant bit (MSB)-first modes available
	I2C	• One unit • Standard I2C communication protocol • Master and slave modes supported for each channel • 7-bit addressing supported for slave mode • SCL signal's high/low periods and SDA signal's hold time settable

Table 3. A34M46x Series Features and Peripherals (continued)

Peripherals		Description
Security	CRC	• CRC operating modes: - CRC-32 (0x04C1_1DB7) - CRC-16-IBM (0x8005) - CRC-8 (0x07) - CRC-7 (0x09) • Input/output data reversion supported • Compatible with DMA
Analog Block	12-bit ADC	• Two units • 20 analog input pins • Five operating modes: - Single conversion - Sequence conversion - Burst conversion - Multiple conversion - Inject conversion • Up to eight sequential conversions supported • Software triggers supported • Three internal trigger sources (MPWM, and Timers) supported • Sample and hold time are adjustable
	OPAMP	• Three units • Each OPAMP with 2 input sources • Available to connect with ADC
	10-bit DAC	• One unit • 10-bit resolution
Operating Voltage		2.7 V to 5.5 V
Operating Temperature		Commercial grade (-40°C to +105°C)
Package		• One type of package option - 48-LQFP 7 x 7 mm

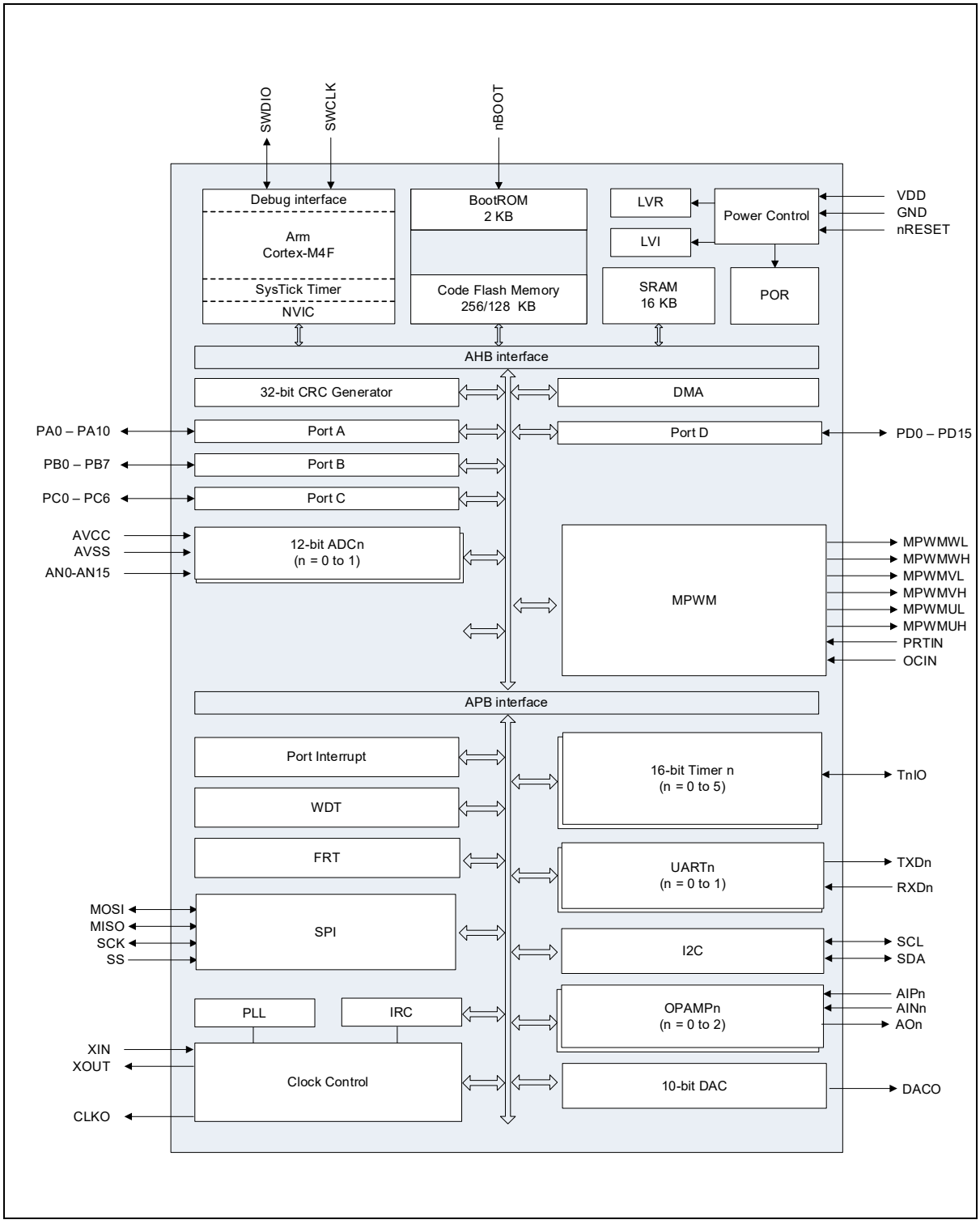
Table 4. Summary of A34M46x Peripherals

Peripheral		A34M466CL	A34M464CL
CPU Frequency		Up to 120 MHz	
Code Flash Memory		256 KB	128 KB
SRAM		16 KB	
GPIO		42	
DMA		4	
Timers	WDT	1	
	General purpose	6	
	FRT	1	
	SysTick	1	
	MPWM	1	
Communication interfaces	UART	2	
	SPI	1	
	I2C	1	
ADCs		Up to 2.0 Msps	
Number of channels		20	
OPAMP		3	
DAC		2	
CRC		1	
Operating Voltage		2.7 V to 5.5 V	
Operating Temperature		Ambient operating temperature: -40°C to 105°C	
Packages		48-LQFP	

1.4 Block Diagram

Figure 1 shows a block diagram of A34M46x series.

Figure 1. A34M46x Block Diagram



1.5 Functional Overview

The following sections provide overviews of the features of the A34M46x series microcontroller.

1.5.1 Cortex-M4F Core

The Arm Cortex-M4F has the same functions as the Cortex-M4 and includes optional floating-point arithmetic functionality. The processors are intended for deeply embedded applications that require fast interrupt response features.

1.5.2 FPU (Floating Point Unit)

Cortex-M4 FPU is an implementation of the single precision variant of the ARMv7-M Floating-Point Extension (FPv4-SP). It provides floating-point computation functionality that is compliant with the ANSI/IEEE Std 754-2008, IEEE Standard for Binary Floating-Point Arithmetic, referred to as the IEEE 754 standard. The FPU supports all single-precision data-processing instructions and data types described in the ARM®v7-M Architecture Reference Manual.

1.5.3 Embedded SRAM

The A34M46x series has a block of 0-wait on-chip SRAM. The SRAM is 16 KB in size, and its base address is 0x2000_0000.

The SRAM memory area is commonly utilized for storing data and as a stack memory. It can also be utilized for storing program code for faster execution or during Flash erase/programming operations.

1.5.4 Boot Configuration

The A34M46x series has a boot mode option to program internal Flash memory. Boot mode can be entered by setting nBOOT pin to ‘L’ at reset timing (normal state is ‘H’).

Boot mode supports UART boot: Pins for boot mode are listed in Table 5.

Table 5. Boot Mode Pin List

Block	Pin Name	Pin Direction	Description
SYSTEM	nRESET/PA2	Input	Reset input signal
	nBOOT/PA1	Input	Boot mode setting pin
UART0	RXD0/PB1	Input	UART boot receive data
	TXD0/PB0	Output	UART boot transmit data

1.5.5 Power Supply

The device requires a 2.7 V to 5.5 V operating voltage supply (VDD).

Table 6. Power Supply

Parameter	Symbol	Min	Max	Unit
Supply Voltage	VDD/AVDD	2.7	5.5	V

During a power-up process, a reset plays an important role and affects the entire process of system booting. The A34M46x series has two power-related reset options as described below:

- POR_RST (Power-On Reset) that controls the voltage less than V_{RESET}
- LVD_RST (Low-Voltage Detect Reset) that controls the voltage less than V_{LVR0}(default)

If the power level is higher than the POR and below the flash memory operating voltage, the Code Read operation may malfunction. To prevent this abnormal Code Read operation, the LVD_RST operates to generate the SYSRESETn internal signal and enter the microcontroller into reset mode to prevent the abnormal operation.

1.5.6 Operation Mode

1.5.6.1 Transition of Operation Mode

INIT mode is the initial state of the chip when a reset is asserted. In RUN mode, the CPU operates at the maximum performance with the high-speed clock system.

SLEEP mode and DEEP-SLEEP mode can be used as low power consumption mode. In the low power consumption mode, power is effectively managed to reduce power consumption by halting the processor core and any unused peripherals.

1.5.6.2 RUN Mode

In RUN mode, the CPU and peripheral hardware operate with a high-speed clock. If the INIT state occurs after a reset, the system enters RUN mode.

1.5.6.3 SLEEP Mode

Once the microcontroller enters SLEEP mode, the CPU becomes inactive. By setting the SCU_PER and SCU_PCER, users can determine which peripherals are to be inactive in SLEEP mode.

1.5.6.4 DEEP-SLEEP (STOP1, STOP2) Mode

When the core goes into a stop state using the WFI instruction, the chip enters DEEP-SLEEP mode, which is divided into DEEP-SLEEP (STOP 1) and DEEP-SLEEP (STOP 2) modes.

1.5.6.5 Reset Mode

The A34M46x series has two system reset options. One is a cold reset, which is effective during power up or down sequence; the other is a warm reset, which is generated by several reset sources.

The reset features of the A34M46x series are as follows:

- POR (Power-On reset)
- LVR (Low-Voltage Detect Reset)
- nRESET pin reset
- WDT reset
- Software reset
- Clock oscillating error reset
- CPU request reset

1.5.7 Clocks and Startup

The A34M46x series has two main operating clocks: HCLK, which generates clock signals for CPU and AHB systems, and PCLK, which generates clock signals for peripheral systems.

1.5.7.1 HCLK Clock

The Cortex-M4F CPU requires two clocks, the HCLK and FCLK. The HCLK is fed to the CPU and AHB. The FCLK stays enabled except in DEEP-SLEEP mode, whereas the HCLK can be disabled in SLEEP mode.

The buses and memories are clocked by the HCLK. As the bus clock frequency is limited to a maximum of 120 MHz, the HCLK frequency must not exceed 120 MHz.

1.5.7.2 PCLK Clock

The PCLK can be used as a clock for any peripherals. Whether to enable or disable the PCLK for each peripheral is determined with the SCU_PCER registers; each peripheral block's registers cannot be read unless its PCLK input is enabled. And the PCLK stops operating in DEEP-SLEEP mode.

1.5.7.3 Clock Configuration Procedure

After powering on the device, the HSI can be enabled with the SCU_CSCR register (Clock source control register). Before enabling the HSE block, the pin mux configuration must be completed for XIN and XOUT. Users must be careful not to affect other bits of the PC_MR and PC_CR registers during this process. Once the HSE block has been enabled, the users must wait for crystal oscillation to stabilize.

1.5.8 Interrupts and Events

1.5.8.1 NVIC (Nested Vectored-Interrupt Controller)

The A34M46x series includes up to 65 maskable interrupt channels that manage sixteen priority levels and the Nested Vector Interrupt Controller (NVIC) that controls 16 interrupt lines of the Cortex®-M4.

The NVIC has the following advantages:

- NVIC enables interrupt processing while reducing interrupt latency.
- Interrupt Vector Table (IVT) address delivered directly to the core
- The fast interrupt processing capability
- Higher priority interrupts are completed before lower priority interrupts, although they are generated later than the lower priority interrupts.
- Tail Chaining
- Automatic saving of processor state
- Interrupt restoring without instructional overhead at the end of the interrupt

The NVIC hardware block provides flexible and efficient interrupt management with minimal interrupt latency.

1.5.8.2 EXTI (Extended Interrupt)

The Extended Interrupt feature enables the system to generate event requests or wake up from STOP mode. Each external line can be configured independently to detect trigger events such as rising or falling edges, or both edges, as well as level events such as Low or High.

1.5.9 GPIO

1.5.9.1 PCU Module

The A34M46x series has a Port Control Unit (PCU) module that controls the external input and output (I/O) ports. By setting the PCU registers, users can configure the pins' uses, input/output direction, Pull-up/Pull-down, and debouncing for their applications as needed.

1.5.9.2 GPIO Module

Pins except the VDD, GND, and certain specific-purpose pins can be used as General-Purpose Input/Output (GPIO) pins. The GPIO module controls the general I/O ports. Output pins can be set to generate high or low-level signals by configuring the corresponding bits of the GPIO control register, while logic input pins can be monitored for their input status in the control registers.

1.5.10 Embedded Flash Memory

The Flash memory controller is an interface controller for embedded flash memory. It manages data stored on flash memory and communicates with other electronic devices.

Code Flash memory of the A34M46x series has key features as listed below:

- 256/128 KB with write protection bits
- 512 bytes, 2 KB erases
- Bulk (full chip) erases
- Zero wait (less than 30 MHz), 1- to 15-wait, and cache (flash acceleration) access
- Instruction and Data Cache
- Read Protection
- Built-in 16-bit CCITT CRC for Flash memory

1.5.11 DMA

The Direct Memory Access (DMA) controller is used for high-speed data transfers between peripherals and memories. The DMA allows quick data transfers by copying or moving data between memory locations or between memory and peripherals, without involving the core.

- Four channels
- Only single-ended signaling
- 8-/ 16-/ 32-bit data transfers
- Multiple buffers of the same size
- DMA transfers are triggered by peripheral interrupts

1.5.12 Timers

1.5.12.1 16-bit Timer

The A34M46x series has a general-purpose timer module configured with six units. This 16-bit Timer supports four operating modes: Periodic mode, PWM mode, One-shot mode, and Capture mode.

Users can use a divided PCLK or an external clock as a clock source for the 16-bit Timer. An internal 10-bit prescaler allows the generation of a variety of timer base clocks.

Interrupts can be triggered at regular intervals when the timer is used in Periodic mode. Users can set the period and duty to form a PWM signal that is used in PWM mode.

In One-shot mode, the timer can generate one PWM waveform. The Capture mode allows measuring the pulse intervals of an external input signal based on the predefined conditions. In addition, this timer can transmit signals to control other devices and is primarily used as a periodic tick timer or as a wake-up source.

1.5.12.2 FRT

The A34M46x series has one built-in Free-Run Timer (FRT) that is 32-bit up-count timers. According to their register setting, the FRT can run with an overflow interrupt or a match interrupt and can remain active in DEEP-SLEEP (STOP 1) mode.

1.5.12.3 WDT

Watchdog Timer (WDT) is used to detect errors in the microcontroller caused by external interference or logically unexpected conditions. These errors cause the application program to deviate from its normal sequence. If the microcontroller loses control, the WDT will reset the microcontroller, allowing it to return to normal operation.

The A34M46x series' WDT is a 32-bit down counter. If the WDT is set as a reset source, the microcontroller restarts when the down counter reaches zero.

When it is not used to monitor the microcontroller, the WDT can be used as a cycle timer along with an interrupt.

1.5.12.4 SysTick Timer

Although the SysTick timer is primarily designed for real-time operating systems, it can also be utilized as a standard down-counter.

The SysTick timer has the following features:

- 24-bit down-counter
- Automatic refreshing
- Maskable system interrupt generation when the counter reaches zero.
- Programmable clock source

1.5.13 UART

The A34M46x series has a two-channel UART module. The built-in UART module allows users to specify settings for transmitting and receiving data and provides the ability to read the current status of the UART. By providing information about the current state of transmission and reception processes, including types and conditions, the UART module enables users to monitor potential errors such as parity, overrun, framing, or break interrupts during data reception.

The UART module includes a programmable baud-rate generator for each channel, which generates an internal clock for its corresponding UART unit. This is achieved by dividing a prescaled clock using a baud-rate divisor that ranges from 1 to 65535 and then dividing the result by 16.

Users can program interrupts that can control UART communication.

Furthermore, the built-in DMA allows the UART module to transfer data directly to or from memory without involving the CPU, reducing CPU usage, and increasing the speed of data transfer.

1.5.14 SPI

The A34M46x series has one built-in Serial Peripheral Interface (SPI) module. The SPI modules are synchronized by clocks, and the specifications of the transfer clocks are adjustable.

The SPI module supports communication between one master and slaves. Slaves can be selected by the Slave Select (SS) signal.

The SPI module performs four-wire synchronous transfers via four signal terminals (SS, SCK, MOSI, and MISO). Its separate Transmit and Receive Buffers enable full-duplex communication, which can read and write data simultaneously.

Specifically, the SPI module of the A34M46x series can enhance the Port Drive Strength so that the SPI rate can be supported up to 16 MHz with the enhanced Port Drive Strength.

1.5.15 I2C

The I2C (Inter-integrated Circuit) interface built in the A34M46x series satisfies the standard I2C communication protocol and is used for serial communication with internal and external devices via the I2C protocol.

Equipped with one unit, it supports both master and slave modes and can transmit and receive data in bytes using interrupts or polling.

The I2C of the A34M46x series operates in Standard mode (100 kHz) or Fast mode (400 kHz) and supports General calls.

It helps communicate with various peripherals that have the same bus type. To use the I2C, it is recommended to set the SCL and SDA pins to open-drain and then connect external pull-up resistors to render their output signals 'HIGH'.

Table 7. Features of I2C

I2C Features	I2C
7-bit addressing mode	O
Standard-mode (up to 100 kbit/s)	O
Fast-mode (up to 400 kbit/s)	O
General call	O

1.5.16 MPWM

The A34M46x series supports one Motor Pulse-Width Modulation (MPWM) unit. The MPWM in the A34M46x series operates a total of 3 PWM modes as shown below to support various applications:

- Motor PWM mode0 and Motor PWM mode1 for motor control
- Normal PWM mode for a variety of PWM applications

In Motor or Normal PWM mode, the MPWM module of the A34M46x series supports many different PWM control functionalities, such as up to six channels' outputs, dead-time, up to eight ADC triggers, a variety of interrupt event generations in many different conditions, protection events, and so on.

Table 8. PWM Modes of MPWM

PWM Mode	Counter Mode	Symmetric/Asymmetric Mode
Motor PWM mode 0	Up-down counter	2-channel symmetric mode
		1-channel asymmetric mode
		1-channel symmetric mode
Motor PWM mode 1	Up counter	-
Normal PWM mode	Up counter	-

1.5.17 ADC

The A34M46x series ADC module is a 12-bit resolution Analog-to-Digital Converter (ADC) that consists of two independent controllable units and has up to 24 analog input channels. Input channels consist of 20 external pin inputs and two internal input channels.

This ADC module can process the A/D conversion of many different channels in Single mode, Sequential mode, Multiple mode, and Burst mode. It can also sample the voltage inputs of multiple channels at critical times, which is required for various applications and can be achieved using the triggering functionality in association with TIMER and MPWM.

Once the A/D conversion is complete, the result is left aligned in 16-bit data registers.

The ADC is mapped to the AHB and capable of high-speed operation based on the internal clock source. In addition, it uses built-in DMA to reduce microcontroller core load while enabling fast data sampling.

The analog input monitoring and comparison capabilities of the ADC allow the applications to determine whether the input voltage is above or below the predefined level.

1.5.18 OPAMP

OPAMP each with two inputs and one output. The OPAMP of the A34M46x series has the following features:

- Three OPAMP units
- OPAMP 0/1/2 can utilize the external analog input signals PD1, PD7, and PD9 as its (+) input.
- OPAMP 0/1/2 can utilize the external analog input signals PD2, PD6, and PD10 as its (−) input.
- OPAMP 0/1/2 can utilize the analog output signals PD3, PD5, and PD11 as its output.

The output of each OPAMP 0/1/2 is internally connected to the corresponding analog input of ADC modules.

1.5.19 10-bit DAC

The Digital-to-Analog Converter (DAC) in the A34M46x series provides a function to convert 10-bit digital value to analog output level.

1.5.20 CRC

A Cyclic Redundancy Check (CRC) module is used to get 32-, 16-, 8-, and 7-bit CRC codes from 8-bit or 32-bit data sizes. The user application can utilize CRC-based technologies to ensure the integrity of data transfers, storage, and Flash memories in compliance with functional safety standards.

Specifically, the CRC module of the A34M46x series supports DMA.

1.6 Development Support

This chapter describes the development support features of the device. The device provides standard Arm® development support, including toolchain compatibility, debug interface, trace support, and on-board debug/programming connection.

Refer to the feature list, pin description, and electrical characteristics for detailed information.

1.6.1 Toolchain Support

The device supports software development using standard Arm-compatible tool chains, including Arm® Keil® MDK, IAR Embedded Workbench® for Arm, and GCC-based toolchains.

Device-specific startup files, linker scripts, header files, and software examples are provided separately for each product series and software package.

1.6.2 Debug Interface

1.6.2.1 Serial Wire Debug Port (SW-DP)

The device provides an Arm® Serial Wire Debug Port (SW-DP) for software debugging and in-system flash memory programming. The SW-DP uses a two-pin debug interface, SWDIO and SWCLK, to access the CPU debug logic, memory, registers, and on-chip debug resources.

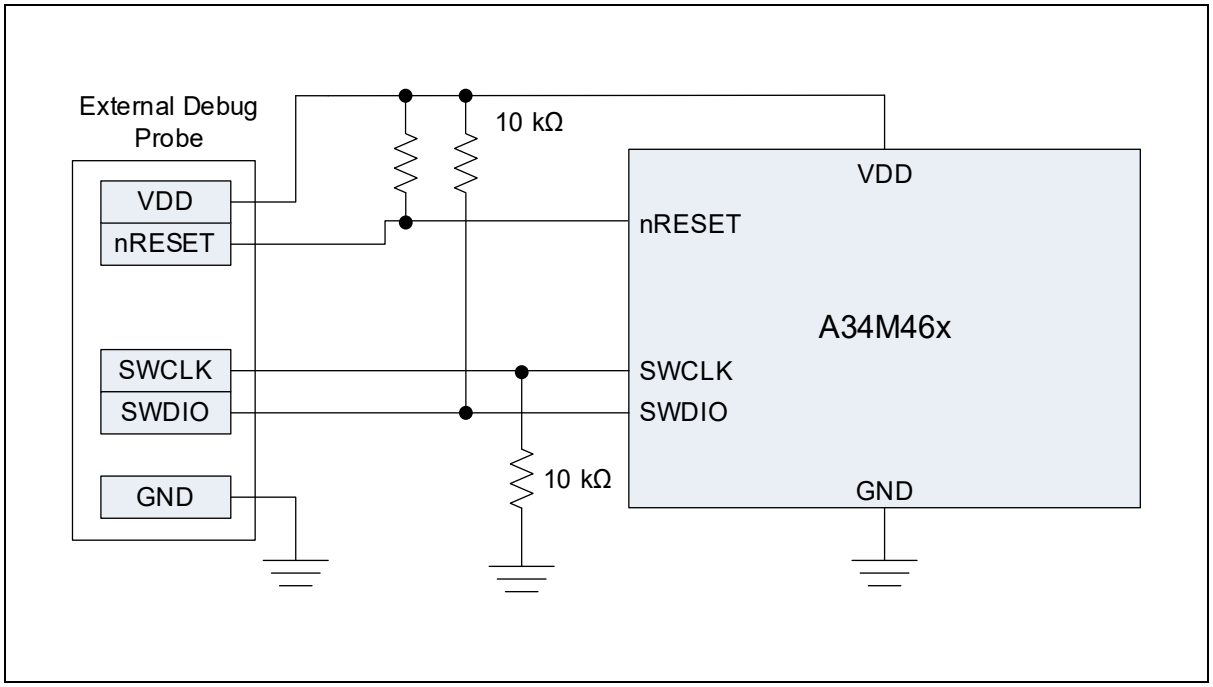
The SWD pins may be multiplexed with GPIO or other alternate functions depending on the product and package. If the SWD pins are used for application functions, the target board and firmware must be designed so that the pins remain accessible during debugging or programming.

1.6.2.2 SWD Connection Guide

For on-board debugging and programming, the target board should provide access to SWDIO, SWCLK, VDD, VSS, and nRESET. The nRESET connection is recommended to improve debug connection reliability and device recovery.

The VDD pin provides the target voltage reference for the external debug probe. It should be connected to the target board supply voltage unless otherwise specified by the debug probe manufacturer.

Figure 2. SWD Interface Connection



2. Pinouts and Pin Descriptions

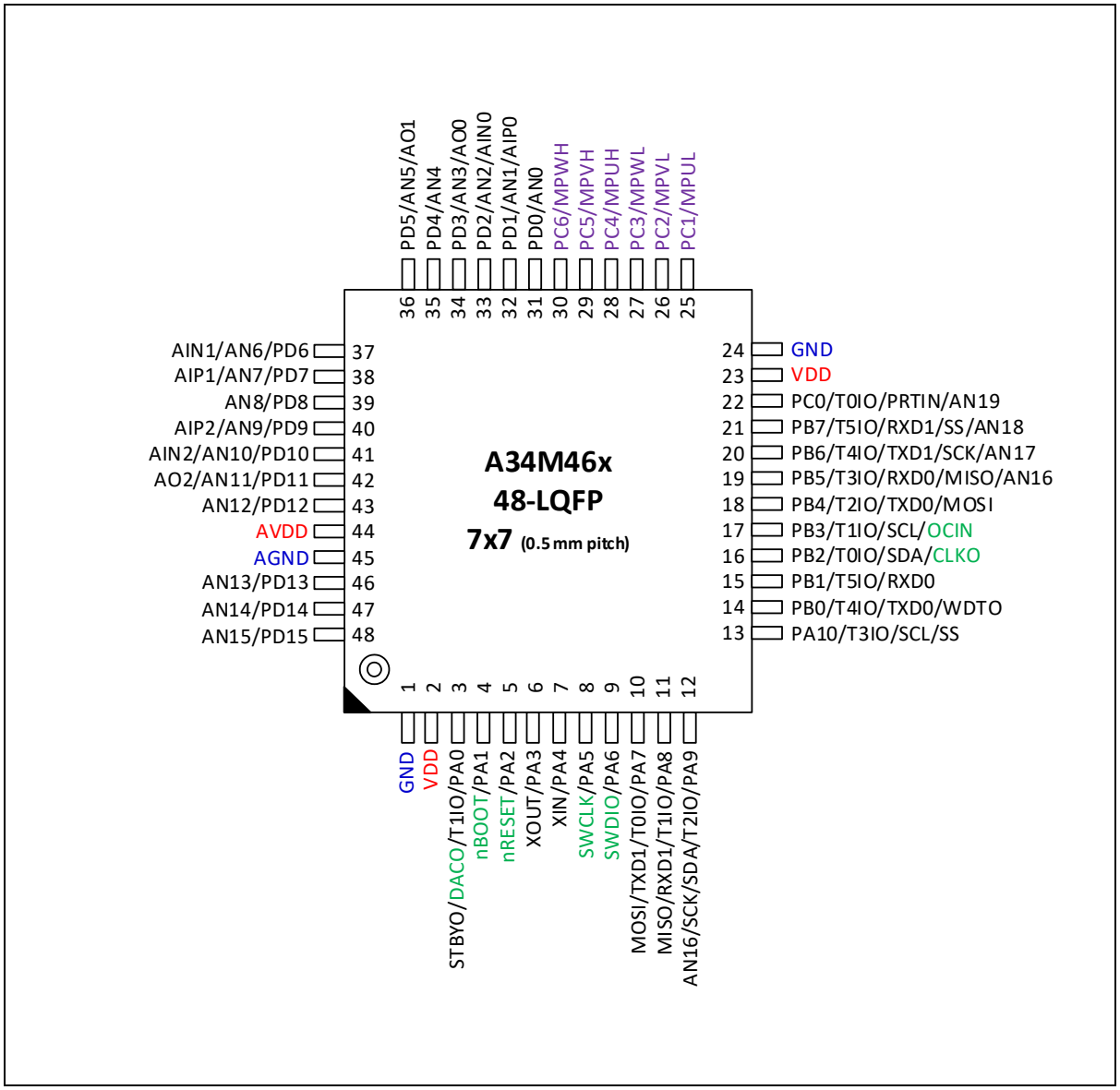
In this chapter, pinouts and pin descriptions of the A34M46x series are introduced.

2.1 Pinouts

Figure 3 show the top views of the packages.

2.1.1 A34M46xCL2N (48-LQFP)

Figure 3. 48-LQFP Pinouts



2.2 Pin Description

Table 9. Legend and Abbreviations Used in Pin Description

Classification	Description	
Pin name	• The pin name is always the same. • Users can set a function on the pin using the alternate function.	
Classification	**Abbreviation**	**Definition**
Pin type	I	Input
	O	Output
	U	Pull-up
	D	Pull-down
	S	Schmitt-Trigger Input Type
	C	CMOS Input Type
	A	Analog
	P	Power
Pin function	Alternate functions	Functions selected through Pn_MR1/2 (PORT n mux1/2 select register) registers

NOTES:

1. '*' means the 'selected pin function after reset condition'.
2. nBOOT, nRESET, SWDIO, and SWCLK are the default pull-up pins.
3. The SWCLK and SWDIO pins should not be switched to other functions while they are being used.
4. Do not configure unused pins as floating inputs.

Pin configuration information in Table 10 contains two pairs of power/ground and other dedicated pins. These multi-function pins have up to five selections of functions including GPIO. Configuration including pin ordering can be changed without notice.

Table 10. Pin Description

Pin No. 48-pin	Pin Name	Type	Description	Remark
1	GND	P	GND	
2	VDD	P	VDD	
3	PA0	IOUS	PORT A Bit 0 Input/Output	
	T1IO	IO	Timer 1 Input/Output	
	STBYO	Output	Power-Down Mode Indication Signal	
	DACO	Output	DA Convertor Output	
4	PA1	IOUS	PORT A Bit 1 Input/Output	
	nBOOT*	Input	Boot Mode Selection Input	Pull-Up
5	PA2	IOUS	PORT A Bit 2 Input/Output	
	nRESET*	Input	External Reset Input	Pull-Up
6	PA3	IOUS	PORT A Bit 3 Input/Output	
	XOUT*	OA	External Crystal Oscillator Output	
7	PA4	IOUS	PORT A Bit 4 Input/Output	
	XIN*	IA	External Crystal Oscillator Input	
8	PA5	IOUS	PORT A Bit 5 Input/Output	
	SWCLK	IO	SWD Clock Input	Pull-Up
9	PA6	IOUS	PORT A Bit 6 Input/Output	
	SWDIO	IOUS	SWD Data Input/Output	Pull-Up
10	PA7	IOUS	PORT A Bit 7 Input/Output	
	MOSI	IO	SPI Channel Master Out/Slave in Signal	
	T0IO	IO	Timer 0 Input/Output	
	TXD1	Output	UART Channel 1 TXD Output	
11	PA8	IOUS	PORT A Bit 8 Input/Output	
	MISO	IO	SPI Channel Master In/Slave Out Signal	
	T1IO	IO	Timer 1 Input/Output	
	RXD1	Input	UART Channel 1 RXD Input	
12	PA9	IOUS	PORT A Bit 9 Input/Output	
	SCK	IO	SPI Channel Clock Input/Output	
	T2IO	IO	Timer 2 Input/Output	
	SDA	IO	I2C Channel SDA Input/Output	Open-Drain

Table 10. Pin Description(continued)

Pin No. 48-pin	Pin Name	Type	Description	Remark
13	PA10	IOUS	PORT A Bit 10 Input/Output	
	SS	IO	SPI Channel Select Signal Input/Output	
	T3IO	IO	Timer 3 Input/Output	
	SCL	IO	I2C Channel Output	Open-Drain
14	PB0	IOUS	PORT B Bit 0 Input/Output	
	TXD0	Output	UART Channel 0 TXD Output	
	T4IO	IO	Timer 4 Input/Output	
	WDTO	Output	WDT Output	
15	PB1	IOUS	PORT B Bit 1 Input/Output	
	RXD0	Input	UART Channel 0 RXD Input	
	T5IO	IO	Timer 5 Input/Output	
16	PB2	IOUS	PORT B Bit 2 Input/Output	
	SDA	IO	I2C Channel SDA Input/Output	Open-Drain
	T0IO	IO	Timer 0 Input/Output	
	CLKO	Output	System Clock Output	
17	PB3	IOUS	PORT B Bit 3 Input/Output	
	SCL	IO	I2C Channel Output	Open-Drain
	T1IO	IO	Timer 1 Input/Output	
	OCIN	Input	MPWM Over-Current Input	
18	PB4	IOUS	PORT B Bit 4 Input/Output	
	MOSI	IO	SPI Channel Master Out/Slave in Signal	
	T2IO	IO	Timer 2 Input/Output	
	TXD0	Output	UART Channel 0 TXD Output	
19	PB5	IOUS	PORT B Bit 5 Input/Output	
	MISO	IO	SPI Channel Master In/Slave Out Signal	
	T3IO	IO	Timer 3 Input/Output	
	RXD0	Input	UART Channel 0 RXD Input	
	AN16*	IA	Analog Input 16	
20	PB6	IOUS	PORT B Bit 6 Input/Output	
	SCK	IO	SPI Channel Clock Input/Output	
	T4IO	IO	Timer 4 Input/Output	
	TXD1	Output	UART Channel 1 TXD Output	
	AN17*	IA	Analog Input 17	
21	PB7	IOUS	PORT B Bit 7 Input/Output	
	SS	IO	SPI Channel Select Signal Input/Output	
	T5IO	IO	Timer 5 Input/Output	
	RXD1	Input	UART Channel 1 RXD Input	
	AN18*	IA	Analog Input 18	

Table 10. Pin Description(continued)

Pin No. 48-pin	Pin Name	Type	Description	Remark
22	PC0	IOUS	PORT C Bit 0 Input/Output	
	T0IO	IO	Timer 0 Input/Output	
	PRITIN	Input	MPWM Protection Input	
	AN19*	IA	Analog Input 19	
23	VDD	P	VDD	
24	GND	P	GND	
25	PC1	IOUS	PORT C Bit 1 Input/Output	
	MPUL	Output	MPWM U-phase low side output	
26	PC2	IOUS	PORT C Bit 2 Input/Output	
	MPVL	Output	MPWM V-Phase low side output	
27	PC3	IOUS	PORT C Bit 3 Input/Output	
	MPWL	Output	MPWM W-phase low side output	
28	PC4	IOUS	PORT C Bit 4 Input/Output	
	MPUH	Output	MPWM U-phase high side output	
29	PC5	IOUS	PORT C Bit 5 Input/Output	
	MPVH	Output	MPWM V-phase high side output	
30	PC6	IOUS	PORT C Bit 6 Input/Output	
	MPWH	Output	MPWM W-phase high side output	
31	PD0	IOUS	PORT D Bit 0 Input/Output	
	AN0*	IA	Analog Input 0	
32	PD1	IOUS	PORT D Bit 1 Input/Output	
	AN1*	IA	Analog Input 1	
	AIP0	IA	OPAMP 0 positive Input	
33	PD2	IOUS	PORT D Bit 2 Input/Output	
	AN2*	IA	Analog Input 2	
	AIN0	IA	OPAMP 0 negative Input	
34	PD3	IOUS	PORT D Bit 3 Input/Output	
	AN3*	IA	Analog Input 3	
	AO0	IA	OPAMP 0 Output	
35	PD4	IOUS	PORT D Bit 4 Input/Output	
	AN4*	IA	Analog Input 4	
36	PD5	IOUS	PORT D Bit 5 Input/Output	
	AN5*	IA	Analog Input 5	
	AO1	IA	OPAMP 1 Output	
37	PD6	IOUS	PORT D Bit 6 Input/Output	
	AN6*	IA	Analog Input 6	
	AIN1	IA	OPAMP 1 negative Input	
38	PD7	IOUS	PORT D Bit 7 Input/Output	

Table 10. Pin Description(continued)

Pin No. 48-pin	Pin Name	Type	Description	Remark
	AN7*	IA	Analog Input 7	
	AIP1	IA	OPAMP 1 positive Input	
39	PD8	IOUS	PORT D Bit 8 Input/Output	
	AN8*	IA	Analog Input 8	
40	PD9	IOUS	PORT D Bit 9 Input/Output	
	AN9*	IA	Analog Input 9	
	AIP2	IA	OPAMP 2 positive Input	
41	PD10	IOUS	PORT D Bit 10 Input/Output	
	AN10*	IA	Analog Input 10	
	AIN2	IA	OPAMP 2 negative Input	
42	PD11	IOUS	PORT D Bit 11 Input/Output	
	AN11*	IA	Analog Input 11	
	AO2	IA	OPAMP 2 Output	
43	PD12	IOUS	PORT D Bit 12 Input/Output	
	AN12*	IA	Analog Input 12	
44	AVDD	P	Analog VDD	
45	AGND	P	Analog GND	
46	PD13	IOUS	PORT D Bit 13 Input/Output	
	AN13*	IA	Analog Input 13	
47	PD14	IOUS	PORT D Bit 14 Input/Output	
	AN14*	IA	Analog Input 14	
48	PD15	IOUS	PORT D Bit 15 Input/Output	
	AN15*	IA	Analog Input 15	

NOTES:

1. I = Input, O = Output, U = Pull-up, D = Pull-down, S = Schmitt-Trigger Input Type, C = CMOS Input Type, A = Analog, P = Power
2. '*' It means "selected pin function after reset condition."
3. nBOOT(PA1), PA6 (SWDIO), PA5 (SWCLK), nRESET(PA2) are the default pull-up pins.
4. Do not configure unused pins as floating inputs.
5. After a reset, the internal pull-up for the boot pin is enabled.
6. After a reset, the internal pull-up for the serial wire clock (SWCLK) and the serial wire data I/O (SWDIO) are enabled.
7. The SWCLK and SWDIO pins should not be switched to other functions while they are being used.
8. VDD and AVDD must be common, likewise GND and AGND must share a common ground.

2.3 Alternate Function Pins

GPIO pins have alternate functions as described in Table 11.

Table 11. GPIO Alternate Function (1)

Pin Name	Alternate Function				
	AF0	AF1	AF2	AF3	AF7
PA0	PA0		T1IO	STBYO	DACO*
PA1	PA1			nBOOT*	
PA2	PA2			nRESET*	
PA3	PA3				XOUT*
PA4	PA4				XIN*
PA5	PA5			SWCLK*	
PA6	PA6			SWDIO*	
PA7	PA7	MOSI	T0IO	TXD1	*
PA8	PA8	MISO	T1IO	RXD1	*
PA9	PA9	SCK	T2IO	SDA	*
PA10	PA10	SS	T3IO	SCL	*
PB0	PB0	TXD0	T4IO	WDTO	*
PB1	PB1	RXD0	T5IO		*
PB2	PB2	SDA	T0IO	CLKO	*
PB3	PB3	SCL	T1IO	OCIN	*
PB4	PB4	MOSI	T2IO	TXD0	*
PB5	PB5	MISO	T3IO	RXD0	AN16*
PB6	PB6	SCK	T4IO	TXD1	AN17*
PB7	PB7	SS	T5IO	RXD1	AN18*
PC0	PC0		T0IO	PRTIN	AN19*
PC1	PC1			MPUL	*
PC2	PC2			MPVL	*
PC3	PC3			MPWL	*
PC4	PC4			MPUH	*
PC5	PC5			MPVH	*
PC6	PC6			MPWH	*
PD0	PD0				AN0
PD1	PD1				AN1/AIP0*
PD2	PD2				AN2/AIN0*
PD3	PD3				AN3/AO0
PD4	PD4				AN4
PD5	PD5				AN5/AO1 *
PD6	PD6				AN6/AIN1*
PD7	PD7				AN7/AIP1*
PD8	PD8				AN8*
PD9	PD9				AN9/AIP0*
PD10	PD10				AN10/AIN0*
PD11	PD11				AN11/AO1*
PD12	PD12				AN12*
PD13	PD13				AN13*
PD14	PD14				AN14*
PD15	PD15				AN15*

NOTES:

1. It means ‘selected pin function after reset condition’. (The initial value of the pin is different depending on the package type)
2. Unused pins are set to output from firmware (low output is recommended).

3. Electrical Characteristics

3.1 Parameter Conditions

Unless otherwise specified, all voltages are referenced to GND.

3.1.1 Minimum and Maximum Values

Unless otherwise specified, our production tests guarantee the minimum and maximum values of the device under the worst-case conditions of ambient temperature, supply voltage, and frequency.

Data based on characterization result, design simulation, and/or technical characteristics are not tested in production but indicated in the table footnotes.

3.1.2 Typical Values

Unless otherwise specified, typical data are based on the conditions of T_A = 25°C and VDD = AVDD = 5.0 V. The typical data are provided only as design recommendations and are not tested.

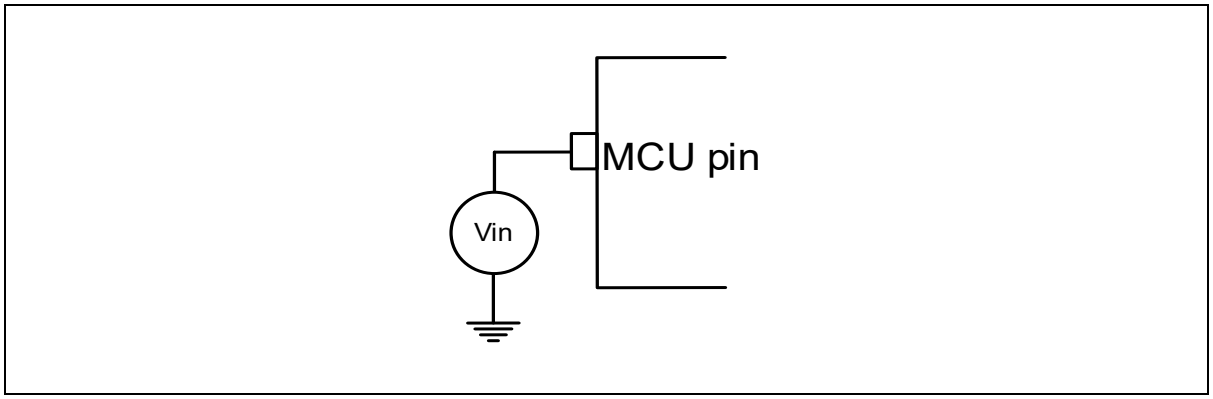
3.1.3 Typical Curves

Unless otherwise specified, all typical curves are provided only as design recommendations and are not tested.

3.1.4 Pin Input Voltage

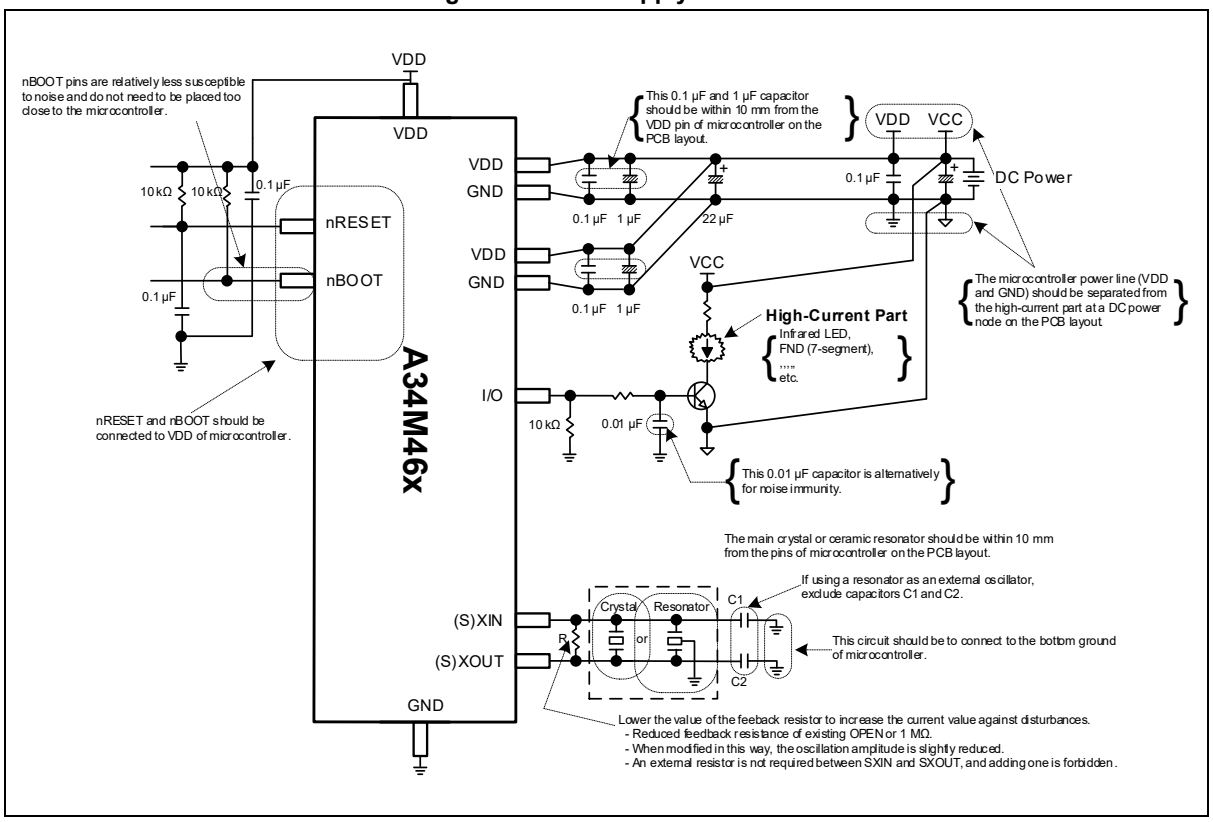
The input voltage measurement on a pin of the device is described in Figure 4.

Figure 4. Pin Input Voltage



3.1.5 Power Supply Scheme

Figure 5. Power Supply Scheme

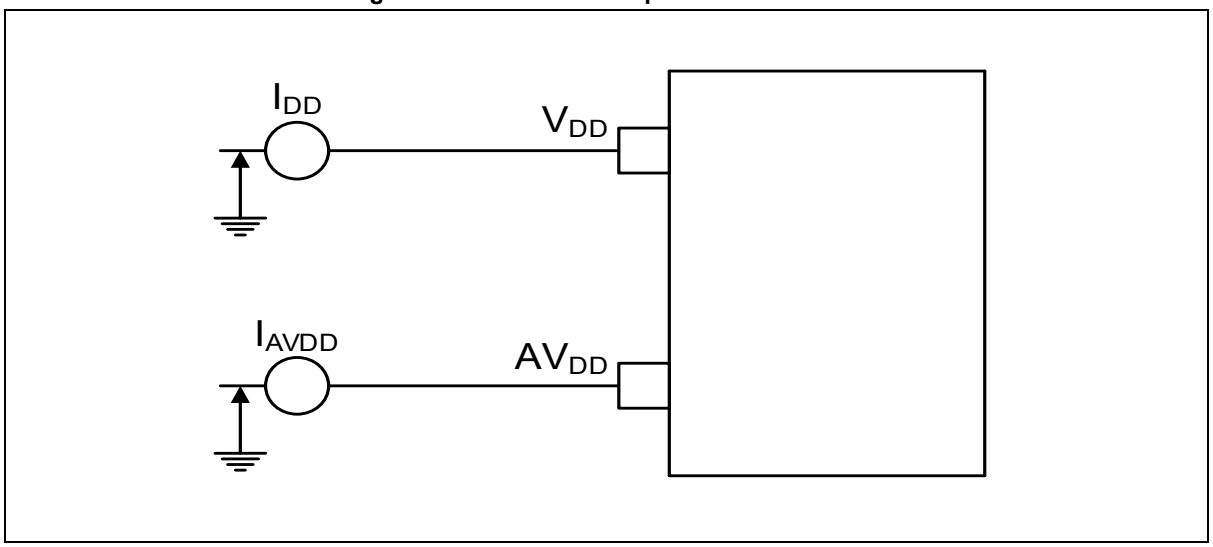


NOTE:

1. Each power supply pair (VDD/GND, etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

3.1.6 Current Consumption Measurement

Figure 6. Current Consumption Measurement



NOTES:

1. The I_{DD} and I_{AVDD} parameters represent the microcontroller's total consumption including the current supplying V_{DD} and AV_{DD}.
2. VDD and AVDD must be common, likewise GND and AGND must share a common ground.

3.2 Absolute Maximum Ratings

Exceeding stresses specified in the Table 12 for voltage characteristics, Table 13 for current characteristics, or Table 14 for thermal characteristics may result in permanent damage to the device. The values listed in the tables are stress ratings only and do not imply that the device will function properly under these conditions. Prolonged exposure to these maximum rating conditions may impact on the reliability of the device. It is important to operate the device within its specified maximum ratings to ensure reliable performance.

Table 12. Voltage Characteristics

Symbol	Ratings	Min.	Max.	Unit
VDD-GND (1)	External main supply voltage (including V_{DD}, AV_{DD})	-0.5	6.0	V
V_I (2)	Input voltage on I/O	-0.5	Max (V_{DD}, AV_{DD})+0.5	V
V_O	Output voltage on I/O	-0.5	Max (V_{DD}, AV_{DD})+0.5	V

NOTES:

1. All main power (VDD, AVDD) and ground (GND, AGND) pins must always be connected to the external power supply, in the permitted range.
2. VI maximum must always be respected.
3. VDD and AVDD must be common, likewise GND and AGND must share a common ground.

Table 13. Current Characteristics

Symbol	Ratings	Max.	Unit
$I_{IO(PIN)}$	Output current sunk by any I/O	20	mA
	Output current sourced by any I/O and control pin	-10	mA
$\sum I_{IOL(PIN)}$ (1)	TBD	90	mA
	Ports other than those above	117	mA
$\sum I_{IOH(PIN)}$ (1)	TBD	-45	mA
	Ports other than those above	-54	mA
I_{IH}	Input high leakage current	1	µA
I_{IL}	Input low leakage current	1	µA
P_T	Total power dissipation	600	mW

NOTE:

1. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.

Table 14. Thermal Characteristics

Symbol	Ratings	Value	Unit
T_{OP}	Operating temperature	-40 to +105	°C
T_{STG}	Storage temperature range	-55 to +125	°C
T_J	Maximum junction temperature	+125	°C

3.3 Operating Condition

3.3.1 General Operating Condition

Table 15. General Operating Condition

(Temperature: -40°C to +105°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	-	2.7(1)	-	5.5	V
AV_{DD}	Analog supply voltage	ADC used	2.7	-	5.5	V
F	Operating frequency	HSE	4	-	12	MHz
		HSI	7.92	8.00	8.08	MHz
		LSI	350	500	650	kHz
V_{IN}	I/O input voltage	5 V I/O	-0.3	-	VDD	V
T_A	Ambient temperature	-	-40	-	105	°C
T_J	Junction temperature range	-	-40	-	125	°C

NOTE:

1. When RESET is released, functionality is guaranteed down to V_{LVR} Min.

3.3.2 Power-On Reset Characteristics

Table 16. POR Electrical Characteristics

(Temperature: -40°C to +105°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{DD}	Operating current	-	-	5.0	10	μA
V_{set}	POR set level	-	1.66	1.84	2.02	V
t_R	VDD voltage rising time	-	0.02	-	20	ms/V
t_F	VDD voltage falling time	-	0.4	-	20	ms/V
V_{reset}	POR reset level	-	1.38	1.53	1.68	V

3.3.3 Operating Condition at Power-Up/Power-Down

The parameters in Table 17 are derived from tests performed under the ambient temperature conditions summarized in Table 15.

Table 17. Operating Condition at Power-Up/Power-Down

(Temperature: -40°C to +105°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{VDD}	V_{DD} rise time rate	-	0.02	-	20	ms/V
	V_{DD} fall time rate	-	0.4	-	20	ms/V

3.3.4 Embedded Reset and Power Control Block Characteristics (LVR, LVI)

The parameters in Table 18 and Table 19 are derived from tests performed under the ambient temperature conditions summarized in Table 15.

Table 18. Low Voltage Reset Characteristics

(Temperature: -40°C to +105°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VDD	Operating voltage	-	0.8	5.0	5.5	V
V_{LVR0_F}	Detection level	Falling voltage	-	-	-	V
V_{LVR1_F}			-	-	-	
V_{LVR2_F}			-	-	-	
V_{LVR3_F}			-	-	-	
V_{LVR4_F}			-	-	-	
V_{LVR5_F}			-	-	-	
V_{LVR6_F}			1.80	2.00	2.20	
V_{LVR7_F}			1.92	2.13	2.34	
V_{LVR8_F}			2.03	2.26	2.49	
V_{LVR9_F}			2.16	2.40	2.64	
V_{LVR10_F}			2.30	2.56	2.82	
V_{LVR11_F}			2.48	2.75	3.03	
V_{LVR12_F}			2.66	2.96	3.26	
V_{LVR13_F}			2.88	3.20	3.52	
V_{LVR14_F}			3.15	3.50	3.85	
V_{LVR15_F}			3.46	3.85	4.24	
V_{LVR0_R}	Detection level	Rising voltage	-	-	-	V
V_{LVR1_R}			-	-	-	
V_{LVR2_R}			-	-	-	
V_{LVR3_R}			-	-	-	
V_{LVR4_R}			-	-	-	
V_{LVR5_R}			-	-	-	
V_{LVR6_R}			2.08	2.20	2.42	
V_{LVR7_R}			2.20	2.32	2.54	
V_{LVR8_R}			2.34	2.46	2.68	
V_{LVR9_R}			2.49	2.61	2.83	
V_{LVR10_R}			2.67	2.79	3.01	
V_{LVR11_R}			2.87	2.99	3.21	
V_{LVR12_R}			3.10	3.22	3.44	
V_{LVR13_R}			3.36	3.48	3.70	
V_{LVR14_R}			3.68	3.80	4.02	
V_{LVR15_R}			4.06	4.18	4.40	
-	Hysteresis	-	-	200	-	mV
-	Noise cancelling time	-	-	3	-	μs
I_{DD}	Operation current	-	-	3.5	5	μA
$I_{DD, STOP}$	Operation current (STOP)	-	-	3	125	nA

Table 19. Low Voltage Indicator Characteristics

(Temperature: -40°C to +105°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VDD	Operating voltage	-	0.8	5.0	5.5	V
V_{LVI0_F}	Detection level	T_A = –40°C to +105°C, Falling voltage	-	-	-	V
V_{LVI1_F}			-	-	-	
V_{LVI2_F}			-	-	-	
V_{LVI3_F}			-	-	-	
V_{LVI4_F}			-	-	-	
V_{LVI5_F}			-	-	-	
V_{LVI6_F}			1.80	2.00	2.20	
V_{LVI7_F}			1.92	2.13	2.34	
V_{LVI8_F}			2.03	2.26	2.49	
V_{LVI9_F}			2.16	2.40	2.64	
V_{LVI10_F}			2.30	2.56	2.82	
V_{LVI11_F}			2.48	2.75	3.03	
V_{LVI12_F}			2.66	2.96	3.26	
V_{LVI13_F}			2.88	3.20	3.52	
V_{LVI14_F}			3.15	3.50	3.85	
V_{LVI15_F}			3.47	3.85	4.24	
V_{LVI0_R}	Detection level	T_A = –40°C to +105°C, Rising voltage	-	-	-	V
V_{LVI1_R}			-	-	-	
V_{LVI2_R}			-	-	-	
V_{LVI3_R}			-	-	-	
V_{LVI4_R}			-	-	-	
V_{LVI5_R}			-	-	-	
V_{LVI6_R}			2.04	2.20	2.42	
V_{LVI7_R}			2.09	2.32	2.55	
V_{LVI8_R}			2.21	2.46	2.71	
V_{LVI9_R}			2.35	2.61	2.87	
V_{LVI10_R}			2.51	2.79	3.07	
V_{LVI11_R}			2.69	2.99	3.29	
V_{LVI12_R}			2.90	3.22	3.54	
V_{LVI13_R}			3.13	3.48	3.83	
V_{LVI14_R}			3.42	3.80	4.18	
V_{LVI15_R}			3.76	4.18	4.60	
-	Hysteresis	-	-	200	-	mV
-	Noise cancelling time	-	-	3	-	µs
I_{DD}	Operation current	-	-	3.5	5	µA
$I_{DD, STOP}$	Operation current (STOP)	-	-	3	125	nA

3.3.5 Embedded Voltage Reference

Table 20. Embedded Internal Voltage Reference (1)

(Temperature: -40°C to +105°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{REFINT}	Internal reference voltage	-40°C ≤ T ≤ +105°C	0.95	1.00	1.05	V

NOTES:

1. The shortest sampling time is determined in the application by multiple iterations.
2. Guaranteed by design.

3.3.6 Supply Current Characteristics

The amount of current consumed by the device is determined by various factors and parameters, including but not limited to the operating voltage, ambient temperature, load on I/O pins, software configuration, operating frequency, switching rate of I/O pins, location of the program in memory, and the binary code being executed.

The current consumption is measured under the conditions specified in Table 21.

3.3.6.1 Supply Current Consumption

Table 21. Supply Current Characteristics

(Temperature: -40°C to +105°C)

Symbol	Operation Mode	Condition					Voltage Scaling	Typ.	Max.	Unit
		LSI	HSI	HSE (8 MHz)	PLL (120 MHz)	f_{MCLK}				
I_{DD_RUN} (RUN)	Normal operation	STOP	STOP	RUN	RUN	f_{PLL}	5.0 V	38	-	mA
		STOP	RUN	STOP	STOP	f_{HSI}	5.0 V	3.8	-	
		STOP	STOP	RUN	STOP	f_{HSE}	5.0 V	4.3	-	
I_{DD_SLEEP} (SLEEP)	SLEEP(1)	STOP	STOP	RUN	RUN	f_{PLL}	5.0 V	21.6	-	mA
		STOP	RUN	STOP	STOP	f_{HSI}	5.0 V	2.8	-	
		STOP	STOP	RUN	STOP	f_{HSE}	5.0 V	3.2	-	
I_{DD_STOP2} (STOP 2)	DEEP-SLEEP(1)(2)	VDC (STOP), LVD (RUN)					5.0 V	944		µA
		VDC (STOP), LVD (STOP)					5.0 V	940		

NOTES:

1. All peripherals are off.
2. In DEEP-SLEEP mode, all clocks are disabled.

3.3.6.2 I/O System Current Consumption

The current consumption in the I/O system is due to the two components, Static and Dynamic.

3.3.6.3 I/O Static Current Consumption

All I/O pins used as inputs with pull-ups cause current consumption when the pins remain Low from the outside. This current consumption value can be calculated simply using the Pull-up/Pull-down resistor value provided in the I/O port characteristics.

To estimate the current consumption at the output pins, users need to consider external Pull-downs or external load.

Additional I/O current consumption can be caused due to the I/Os configured as inputs if the medium voltage level is applied externally. This current is consumed by the input Schmitt trigger circuit used to tell the input value. Unless the application requires a specific configuration, users can prevent this supply current consumption by configuring the I/Os in analog mode instead of using the Schmitt circuit.

Specifically, input pins of the ADC, OPAMP, and CMP must be configured as analog inputs.

3.3.6.4 I/O Dynamic Current Consumption

The I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin.

3.3.7 External Clock Source Characteristics

3.3.7.1 High-Speed External Clock Generated from Crystal/Ceramic Resonator

A high-speed external clock (HSE) can be supplied with crystal/ceramic resonator oscillators in the range of 4 to 12 MHz. All information provided in this section is based on the design simulation results obtained by the typical external components specified in Table 22.

To minimize the outputs in the application, the resonator and load capacitor must be placed as close to the oscillator pin as possible.

For more information on the distortion and stabilization time, and the resonator characteristics (frequency, package, and accuracy), contact the manufacturer of the crystal resonator.

Table 22. HSE Oscillator Characteristics [1]

(Temperature: -40°C to +105°C)

Symbol	Parameter	Conditions[2]	Min.	Typ.	Max.	Unit
V_{DD}	Operating voltage	-	2.7	5.0	5.5	V
$I_{DD(HSE)}$	HSE current consumption	-	-	-	2.5	mA
I_{STOP}	Power down current	-	-	1	60	nA
f_{OSC_IN}	Oscillator frequency	-	4	8	12	MHz
f_{OUT}	Output Frequency	VDD ≥ 2.7 V[4][5][6][7]	4	-	12	MHz
V_{IL}	Crystal input (low)	-	-	-	0.2 V_{DD}	V
V_{IH}	Crystal input (high)	-	0.8 V_{DD}	-	-	V
V_{OL}	Crystal out (low)	-	-	-	0.2 V_{DD}	V
V_{OH}	Crystal out (high)	-	0.8 V_{DD}	-	-	V
C_L	External Load Capacitor	TBD				
		4 MHz < f_{OUT} ≤ 12 MHz	10	18	26	pF
		TBD				
R_F	Feedback resistor	VDD = 5 V	0.7	1.0	1.3	MΩ
$t_{SU(HSE)}$[3]	Startup time	-	-	1	-	ms

NOTES:

1. Guaranteed by design.
2. Resonator characteristics are given by the crystal/ceramic resonator manufacturer.
3. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator, and it can vary significantly with the crystal manufacturer.
4. HSEISEL = 0x3, HSENFSEL = 0x3
5. HSEISEL = 0x2, HSENFSEL = 0x2
6. HSEISEL = 0x1, HSENFSEL = 0x1
7. HSEISEL = 0x0, HSENFSEL = 0x0

Figure 7. Crystal/Ceramic Oscillator

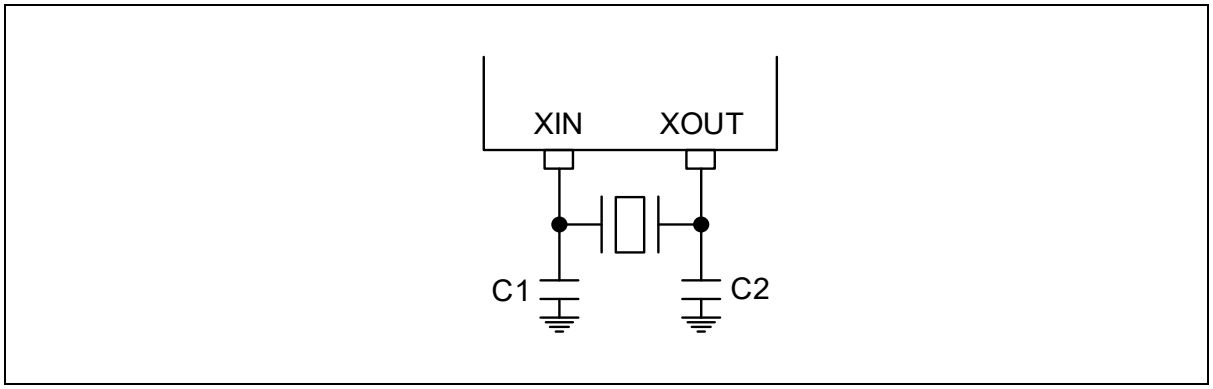


Figure 8. External Clock

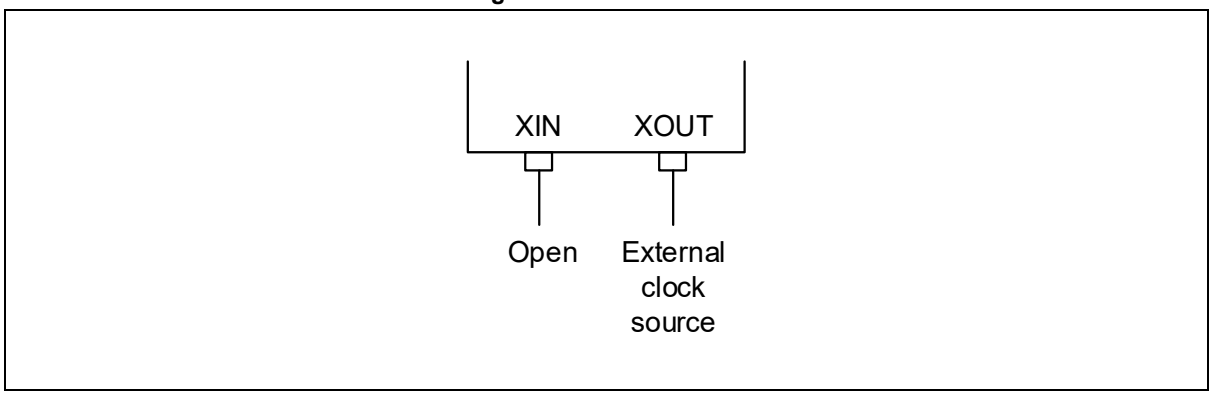
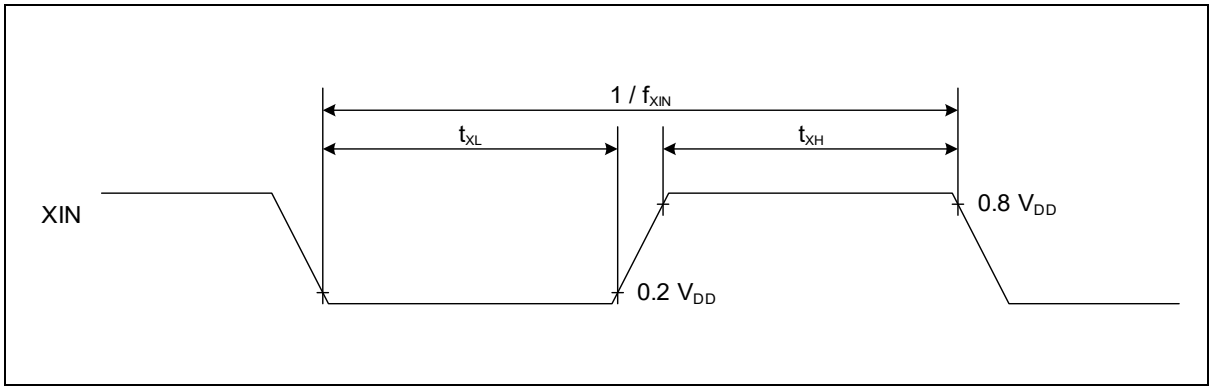


Figure 9. Clock Timing Measurement at XIN

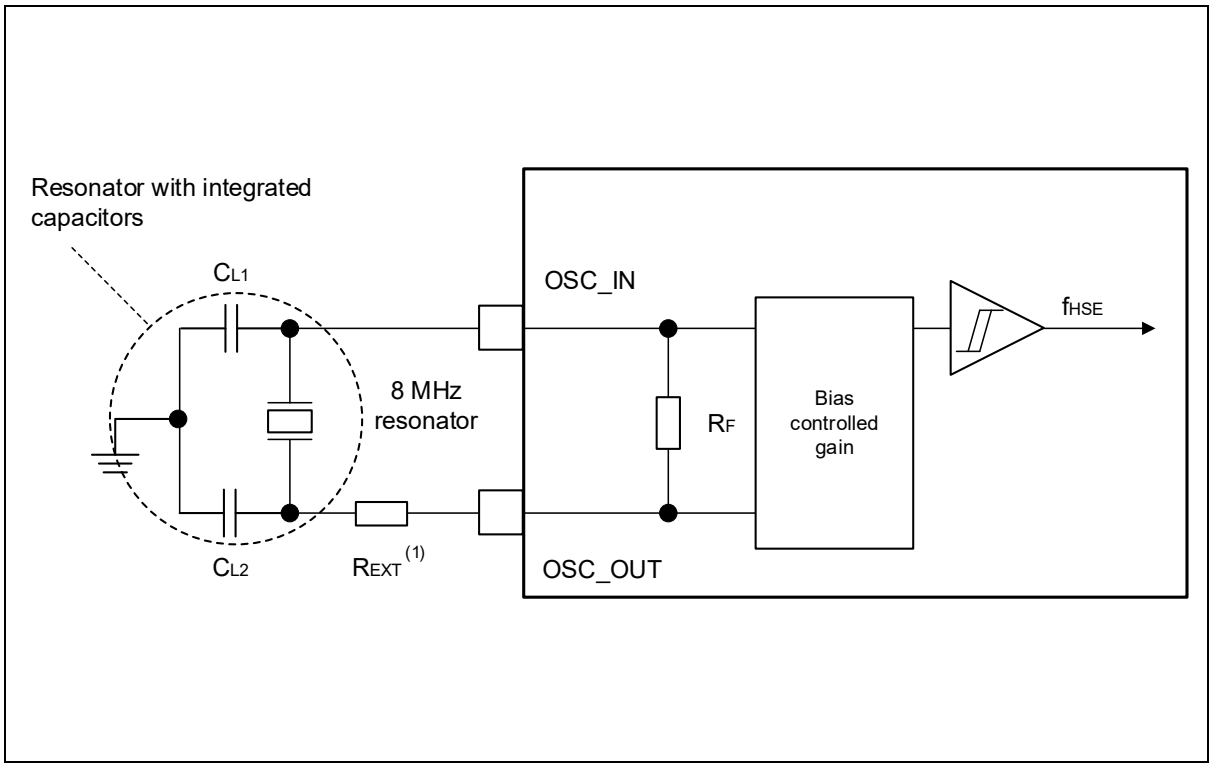


It is recommended to use high-quality external ceramic capacitors designed for high-frequency applications and selected to match the requirements of the crystal or resonator. The capacitance of the C_{L1} and C_{L2} capacitors should be between 5 pF to 20 pF.

The C_{L1} and C_{L2} capacitors are usually the same size, and the crystal manufacturer typically specifies a load capacitance that is the series combination of both capacitors. However, the capacitance of the printed circuit board (PCB) and the microcontroller's pin should also be considered, which must be included in the calculation of the overall capacitance. A rough estimate of the combined pin and board capacitance is around 10 pF, which can be used to size C_{L1} and C_{L2} appropriately.

Figure 10 shows a circuit diagram of a typical application with an 8 MHz crystal.

Figure 10. Typical Application with 8 MHz Crystal



3.3.8 Internal Clock Source Characteristics

The parameters listed in Table 23 and Table 24 are obtained through tests conducted under ambient temperature and supply voltage conditions, which are specified in Table 15.

3.3.8.1 HSI (High-Speed Internal) Oscillator

Table 23. HSI Oscillator Characteristics (1)

(Temperature: -40°C to +105°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating voltage	-	2.7	-	5.5	V
f_{HSI}	HSI frequency	V_{DD}=5.0 V, T_A=40°C	7.92	8	8.08	MHz
		@ -40°C to +105°C, user trim	-1	-	1	%
DuCy (HSI8)	Duty cycle	-	45	-	55	%
Δ_{VDD} (HSI8)	HSI8 oscillator Frequency drift over V_{DD}	V_{DD}=2.7 V to 5.5 V	-0.2	-	0.2	%
t_{su} (HSI8)	HSI8 oscillator start-up time	-	-	6	11	µs
t_{stab} (HSI8)	HSI8 oscillator stabilization time	-	-	-	35	µs
I_{DD} (HSI8)	HSI8 oscillator power consumption	-	-	250	350	µA

NOTE:

1. Guaranteed by characterization results and design.

3.3.8.2 LSI (Low-Speed Internal) 500 kHz Oscillator

Table 24. LSI Oscillator Characteristics

(Temperature: -40°C to +105°C)

Symbol	Parameter	Conditions(2)	Min.	Typ.	Max.	Unit
V_{DD}	Operating voltage	-	2.7	-	5.5	V
f_{OUT}	Output frequency	V_{DD} = 2.7 to 5.5 V	350	500	650	kHz
t_{VREG_SU} (1)	500 kHz oscillator V_{REG} start-up time (after LSI enabled)	V_{DD} = 5.0 V	-	25	40	µs
t_{STAB} (1)	500 kHz oscillator stabilization time (after LSI enabled)	5 % of target frequency	-	20	120	µs
I_{LIRC}(1)	500 kHz oscillator power consumption	The LSI oscillator is enabled. V_{DD}=2.7 to 5.5 V	-	1.5	2.0	µA
		The LSI oscillator is disabled. V_{DD}=2.7 to 5.5 V	-	-	100	nA

NOTE:

1. Guaranteed by design.

3.3.9 PLL Characteristics

The parameters listed in Table 25 are obtained through tests conducted under ambient temperature and supply voltage conditions, which are specified in Table 15.

Table 25. PLL Characteristics (1)

(Temperature: -40°C to +105°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VDD	Operating voltage	-	2.7	-	5.5	V
I_{DD} (PLL)	PLL power consumption on V_{DD}	VCO freq = 240 MHz	-	1	-	mA
$f_{PLL_P_OUT}$	PLL output clock	Voltage scaling range	-	-	120	MHz
f_{VCO_OUT}	PLL VCO output	VCO frequency range	240	-	280	MHz
f_{DUTY}	Duty	-	40	-	60	%
f_{IN}	Input frequency	$f_{PLLINCLK}$ / (PREDIV+1)	2		3	MHz
$f_{PLLINCLK}$	PLL block Input frequency	-	2	8	32	MHz
t_{JITTER}	P-P jitter	@ Lock state	-	-	40	ps
t_{LOCK}	PLL lock time	-	-	50	100	µs

NOTE:

1. Guaranteed by design.

3.3.10 Flash Memory Characteristics

Table 26. Code Flash Memory Characteristics

(Temperature: -40°C to +105°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{PROG}	Program time	-	-	-	30	µs
t_{PER}	Page erase time	-	-	-	4	ms
t_{SER}	Sector erase time		-	-	4	ms
t_{MER}	Mass (chip) erase time	-	-	-	8	ms
N_{FWE}	Endurance of write/erase	T_A=25°C, page unit	10,000	-	-	times
t_{RT}	Retention time	-	10	-	-	years

3.3.11 I/O Port Characteristics

3.3.11.1 General Input/Output Characteristics

Unless otherwise specified, the parameters in Table 27 are obtained through tests conducted under the conditions which are specified in Table 15. All I/Os conform to CMOS standards.

Table 27. I/O Static Characteristics

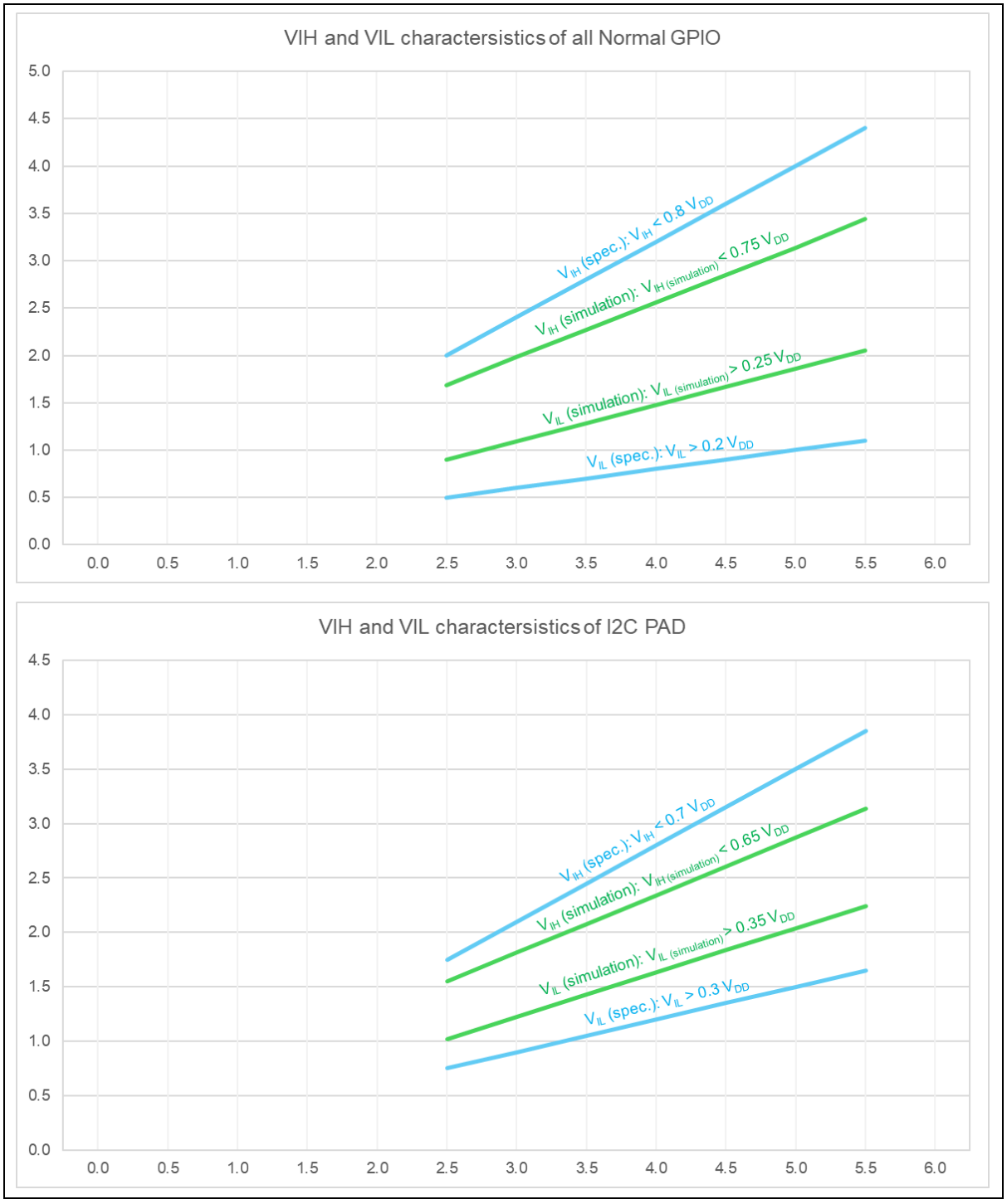
(Temperature: -40°C to +105°C)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{IL1} (1)	I/O input low-level voltage	5 V GPIO	2.7 V < V_{DD} < 5.5 V	-	-	0.2×V_{DD}	V
V_{IH1} (1)	I/O input high-level voltage	5 V GPIO	2.7 V < V_{DD} < 5.5 V	0.8×V_{DD}	-	-	V
V_{IL2} (1)	I2C I/O Input high voltage	5 V GPIO	2.7 V < V_{DD} < 5.5 V	-	-	0.3×V_{DD}	
V_{IH2} (1)	I2C I/O Input low voltage	5 V GPIO	2.7 V < V_{DD} < 5.5 V	0.7×V_{DD}	-	-	
I_{leak}	Input leakage current (2)	5 V GPIO	2.7 < V_{IN} ≤ 5.5 V	-	-	±1	µA
R_{PU}	Weak pull-up equivalent resistor	V_{IN} = GND		30	50	70	kΩ
R_{PU}	Weak pull-down equivalent resistor	V_{IN} = V_{DD}		30	50	70	

NOTES:

1. Data based on characterization results are not tested in production.
2. Guaranteed by design.

Figure 11. I/O Input Characteristics (Temperature: 25°C)



NOTE:

1. X-axis is VDD, Y-axis is VIHL Spec.

3.3.11.2 Output Driving Current

The GPIOs can sink or source currents up to ±3 mA and can also sink or source currents up to ±9 mA when the V_{OL}/V_{OH} limits are relaxed.

To ensure compliance with the absolute maximum ratings specified in chapter 3.2, it is necessary to limit the number of I/O pins driving current in the user application.

3.3.11.3 Output Voltage Levels

Unless otherwise specified, parameters in Table 28 are obtained through tests conducted under ambient temperature and supply voltage conditions, which are specified in Table 15.

Table 28. Output Voltage Characteristics (1)

(Temperature: -40°C to +105°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OH}	Output high voltage	Normal GPIO, V_{DD} = 5 V, I_{OH1} = -3 mA, I_{OH2} = -9 mA	$0.8V_{DD}$	-	-	V
		I2C PAD, V_{DD} = 5 V, I_{OH1} = -3 mA, I_{OH2} = -9 mA	$0.7V_{DD}$	-	-	
V_{OL}	Output low voltage	Normal GPIO, V_{DD} = 5 V, I_{OL1} = 3 mA, I_{OL2} = 9 mA	-	-	$0.2V_{DD}$	V
		I2C PAD, V_{DD} = 5 V, I_{OL1} = 3 mA, I_{OL2} = 9 mA	-	-	$0.3V_{DD}$	

NOTE:

1. Guaranteed by design.

3.3.12 Analog-to-Digital Converter Characteristics

Table 29. ADC Electrical Characteristics

(Temperature: -40°C to +105°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
AV_{DD}	Operating voltage	-	2.7	5	5.5	V
-	Resolution	-	-	-	12	bit
I_{DDA}	Operating current	AVDD = 5.0 VA @ f_{MCLK} = 25 MHz	-	2.2	-	mA
		AVDD = 5.0 VA @ f_{MCLK} = 42 MHz	-	2.6	-	mA
V_{AN}	Analog input range	-	GND	-	AV_{DD}	V
t_{CONV}	Conversion time	-	18 / f_{ACLK}	-	48 / f_{ACLK}	μs
f_{CONV}	Conversion frequency	@ AVDD > 3.7 V	-	-	2.0	MHz
		@ AVDD > 3.1 V	-	-	1.6	MHz
		@ AVDD > 2.7 V	-	-	1.0	MHz
f_{ACLK}	Operating frequency	-	-	-	42	MHz
INL	DC accuracy	-	-	±4	-	LSB
DNL		-	-	±3	-	LSB
ZOE	Zero offset error	-	-	±3	-	LSB
FSE	Full-scale error	-	-	±3	-	LSB

3.3.13 Digital-to-Analog Converter Characteristics

Table 30. DAC Electrical Characteristics

(Temperature: -40°C to +105°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
AV_{DD}	Analog Power Supply		2.7	-	5.5	V
C_L	Capacitive load	DAC output buffer on	-	-	100	pF
PSRR	Power supply rejection ratio	DAC output buffer on (C_L =50 pF, R_L =5 kΩ)	-	-60	-28	dB
I_{AVDD}	AV_{DD} Current	DAC output buffer on (No load, middle code)	-	315	500	µA
		DAC output buffer off (No load, middle code)	-	-	0.2	
V_{DAC_OUT}	Conversion Voltage Range	DAC output buffer on	0.2	-	AV_{DD} -0.2	V
$T_{setting}$	Setting time	DAC output buffer on (C_L =50 pF, R_L =5 kΩ)	-	-	3	µs
T_{wakeup}	Wakeup time from off state	DAC output buffer on (C_L =50 pF, R_L =5 kΩ)	-	4.2	7.5	µs
$T_{W_to_W}$	DAC output for a small variation of the input code (1LSB)	-	1	-	-	µs
Offset	Offset error at full code (0x400)	DAC output buffer on	-	-	±1	LSB
EGAIN	Gain error	DAC output buffer on	-	-	±0.2	% (FSR)
TUE	Total unadjusted error	DAC output buffer on	-	-	±5	LSB
ENOB	Effective number of bits	DAC output buffer on	-	9	-	bits
DNL	Differential nonlinearity	-	-	-	±1.5	LSB
INL	Integrated nonlinearity	-	-	-	±2	LSB
SINAD	Signal-to-noise and distortion ratio	-	-	55	-	dB
Offset/Dt	Gain Error temperature coefficient	-	-	-	±5	ppm/°C (FSR)

3.3.14 Operational Amplifier Characteristics

Table 31. OPAMP Characteristics

(Temperature: −40°C to +105°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
AV_{DD}	Analog Power Supply	-	2.7	-	5.5	V
I_{DD} (RMS) (1)	Operating current(1)	-	-	630	-	μA
F_{GB}(1)	Gain bandwidth(1)	CL=50 pF, RL=20kΩ	-	6	-	MHz
A_V(1)	Open loop voltage gain(1)	-	-	100	-	dB
PM(1)	Phase margin(1)	CL=50 pF, RL=20kΩ	-	70	-	Degree
V_{IO}	Input offset voltage	-	-	-	±1.5	mV
V_I	Input voltage range	-	0	-	AV_{DD}	V
V_O	Output voltage range	-	0.1V	-	AV_{DD}-0.1V	V
CMRR(1)	Common mode rejection ratio(1)	-	-	130	-	dB
PSRR(1)	Power supply rejection ratio(1)	-	-	85	-	dB
SR(1)	Slew rate(1)	CL=50pF, RL=20kΩ	-	12	-	V/μs
T_{PR}(1)	Pulse response(1)	-	-	-	1	μs

3.3.14.1 General PCB Design Guidelines

The power supplier must be separated conforming to the scheme shown in Figure 5. The de-coupling capacitors across the V_{DD}/AV_{DD} are ceramic (good quality) capacitors and must be located as close as possible to the device.

3.3.15 Communication Interfaces Characteristics

3.3.15.1 I2C Interface Characteristics

The I2C interface conforms to the timing requirements specified in the I2C-bus specification, in addition to the user timing requirements listed below:

- Standard mode (Sm): up to 100 kbps bit rate
- Fast mode (Fm): up to 400 kbps bit rate

The I2C timing requirements are guaranteed by design when the I2C peripheral is configured correctly, and the I2C clock frequency is equal to or greater than the minimum value listed in the table below.

Table 32. I2C Characteristics

(Temperature: -40°C to +105°C)

Symbol	Parameter	Standard		Fast		Unit
		Min.	Max.	Min.	Max.	
f_{SCL}	Clock frequency	0	100	0	400	kHz
t_{SCLH}	Clock high pulse width	4.0	-	0.6	-	µs
t_{SCLL}	clock low pulse width	4.7	-	1.3	-	
t_{BF}	Bus free time	4.7	-	1.3	-	
t_{STSU}	Start condition setup time	4.7	-	0.6	-	
t_{STHD}	Start condition hold time	4.0	-	0.6	-	
t_{SPSU}	Stop condition setup time	4.0	-	0.6	-	
t_{SPHD}	Stop condition hold time	4.0	-	0.6	-	
t_{VD}	Output valid from clock	0	-	0	-	
t_{DIH}	Data input hold time	0	-	0	1.0	
t_{DIS}	Data input setup time	250	-	100	-	ns

3.3.15.2 SPI Interface Characteristics

Unless otherwise specified, the parameters in Table 33 are obtained through tests conducted under ambient temperature, f_{PCLK} frequency and supply voltage conditions, which are specified in Table 15.

- Capacitive load C = 30 pF
- Measurement points are performed at the CMOS level: 0.5 V_{DD}

For more information about I/O alternate function characteristics (SS, SCK, MOSI, and MISO for SPI), refer to section 3.3.11.1.

Table 33. SPI Characteristics

(Temperature: -40°C to +105°C)

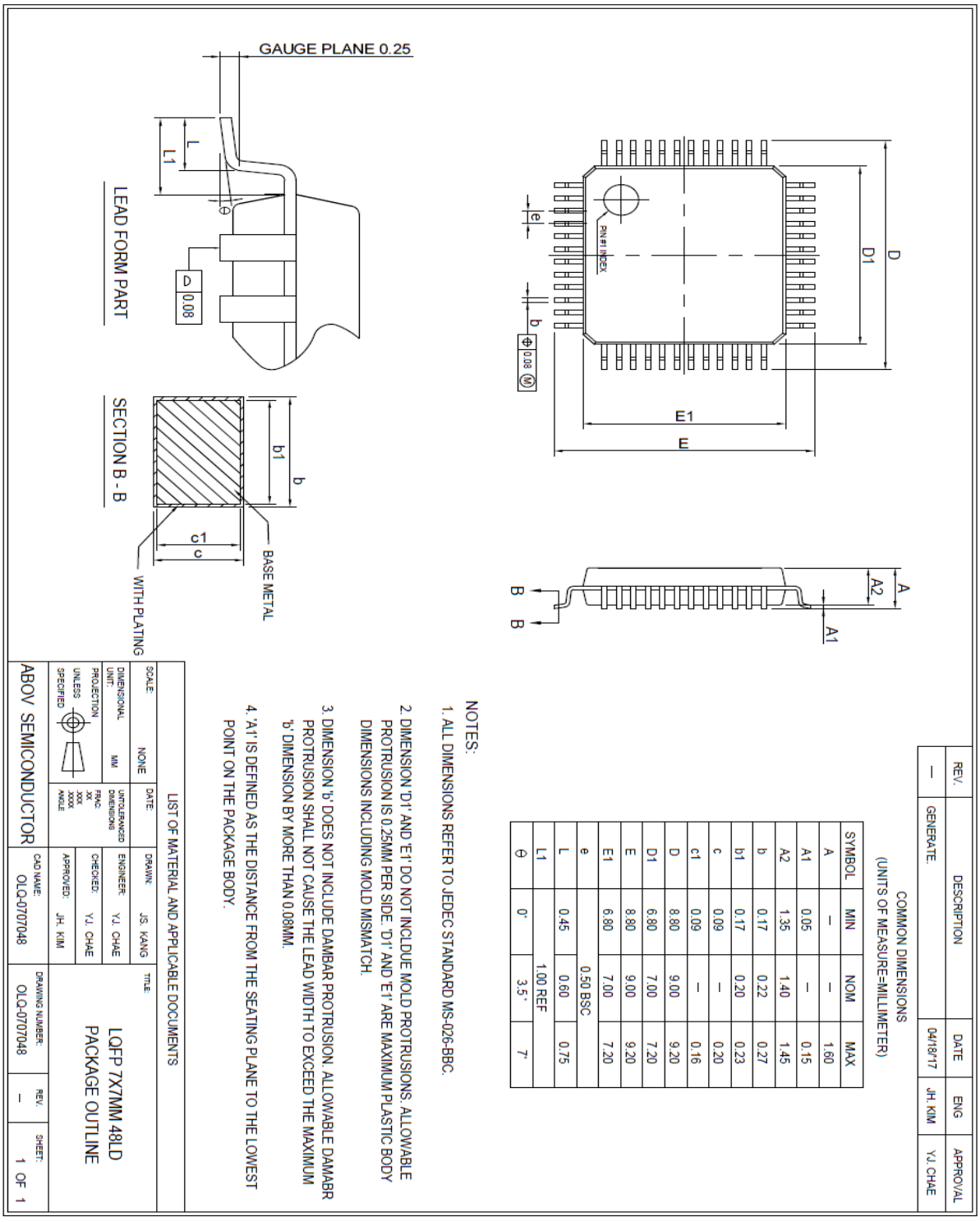
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{SCK1}	SPI clock frequency with strength on	SPI, SPI1, SPI2 2.7 V≤V_{DD}≤3.3 V	-	-	16	MHz
f_{SCK2}		SPI, SPI1, SPI2 V_{DD}≤5.5 V	-	-	16	MHz
f_{SCK3}	SPI clock frequency with strength off	SPI, SPI1, SPI2 2.7 V≤V_{DD}≤3.3 V	-	-	10	MHz
f_{SCK4}		SPI, SPI1, SPI2 V_{DD} ≤ 5.5 V	-	-	15	MHz
Duty	Duty cycle of SPI frequency (SCK)	Slave Mode	30	50	70	%
C_{CL}	Capacitance load	-	-	-	30	pF

4. Package Information

4.1 48-LQFP Package Information

48-LQFP is a 48-pin, 7 x 7 mm quad flat package.

Figure 12. Package Dimension (48-LQFP)

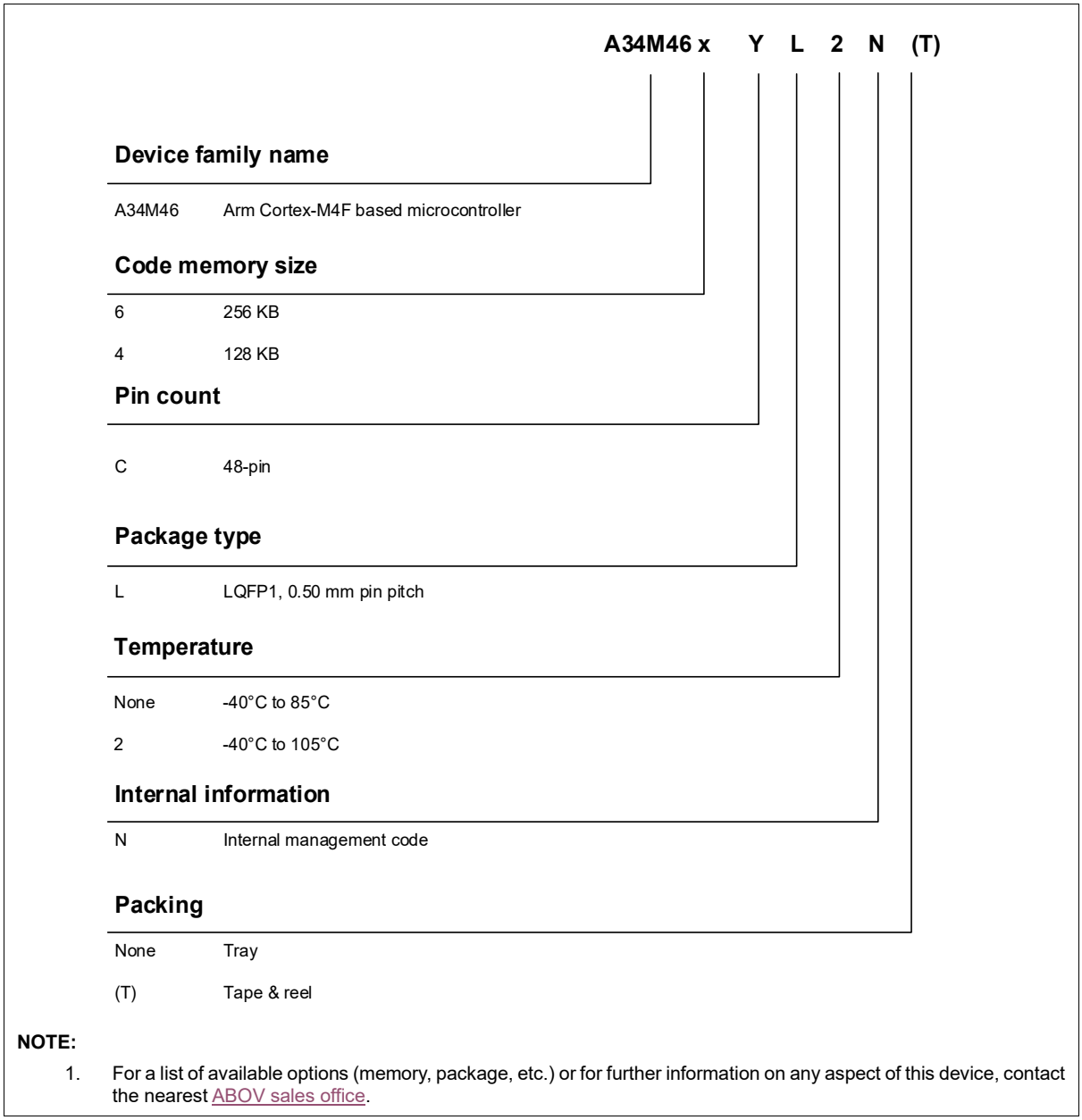


SYMBOL	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	—	0.20
c1	0.09	—	0.16
D	8.80	9.00	9.20
D1	6.80	7.00	7.20
E	8.80	9.00	9.20
E1	6.80	7.00	7.20
e		0.50 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	3.5°	7°

REV.	DESCRIPTION	DATE	ENG	APPROVAL
—	GENERATE.	04/18/17	JH. KIM	YJ. CHAE

5. Ordering Information

Figure 13. A34M46x Series Device Ordering Information



NOTE:

1. For a list of available options (memory, package, etc.) or for further information on any aspect of this device, contact the nearest ABOV sales office.

Revision History

Revision	Date	Notes
1.00	May 28, 2026	Initial release
1.01	Jul. 22, 2026	Corrected subtitle
1.02	Aug. 10, 2026	• Added A34M464 device • Updated POR set/reset level

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