
Cortex-M4 32-bit Microcontroller + FPU, 140 MHz, Up to 256 KB Code Flash, 32 KB Data Flash, 32 KB SRAM, 3-Phase PWM, 12-bit ADC for Motor Control Applications

DS Rev. 1.02

Features

Core and Memory

- Arm 32-bit Cortex-M4 CPU
- Up to 140 MHz with FPU, 175 DMIPS
- Cache buffer (Flash accelerator) support

Memories

- Up to 256 KB of Code Flash (28 MHz Flash access speed)
- 32 KB of Data Flash
- Up to 32 KB of SRAM
- Error Correction Code (ECC)

Reset and Power Management

- Power-on/power-down reset (POR/LVR/LVI)
- Low-power modes: SLEEP, DEEP-SLEEP

Clock Management

- High-speed internal (HSI) oscillator 8 MHz
 - $\pm 1.0\%$ @ -40°C ~ 105°C
- Low-speed internal oscillator 500 kHz (LSI)
 - $\pm 30\%$ @ -40°C to $+105^{\circ}\text{C}$
- External main oscillator (HSE)
 - 4 MHz to 16 MHz
- External sub-oscillator (LSE)
 - 32.768 kHz
- Phase-locked loop (PLL) frequency generator
 - Up to 140 MHz

GPIO (General-Purpose Input/Output)

- Up to 88 I/O pins with interrupt capability
- All mappable on external interrupt vectors
- Multi-function pins have up to 5 selections of functions, including GPIO

DMA Controller

- 8-ch DMA Controller
- 8-/ 16-/ 32-bit data transfers
- Compatible with 24 different types of peripherals

16-bit Timer

- 10 units
- 10 channels I/O
 - 10 timer n capture port input channels
 - 10 timer n output port output channels
- Timer operating modes
 - Periodic timer mode
 - One-shot mode
 - PWM mode
 - Capture mode
- 10-bit prescaler

Watchdog Timer

- 32-bit down-count timer
- Reset and periodic interrupts
- Eight different prescalers are selectable

Free-Run Timer

- Two units
- 32-bit free-run timer

Motor PWM

- Two MPWM generators
- Six channels (high and low signals of phases U, V, and W) generate different waveforms
- 16-bit up and up/down-counters
- Eight ADC trigger sources
 - 6-Variable Triggers
 - 2-Fixed Trigger (Bottom, Period Match)

PFCP

- Power-Factor Correction PWM generator
- 1 PFC control unit and 2 PFC PWM outputs
- Supports three PFC PWM modes
 - Single PFC mode
 - Interleaved PFC mode
 - Complementary PFC mode
- 16-bit up and up/down-counters
- Eight ADC trigger sources
 - 6-Variable Triggers
 - 2-Fixed Trigger (Bottom, Period Match)
- Supports dead-time in Complementary PFC mode

Serial Interfaces

- UART (6 units)
- SPI (2 units)
- I2C (2 units)

12-bit ADC

- Three independent ADC blocks
- Max. 2.0 Msps
- 24 analog input channels
- Adjustable sample time and hold time
- Multiple operating modes:
 - Single conversion
 - Sequence conversion
 - Burst conversion
 - Multiple conversion

10-bit DAC

- Two units
- DAC00, DAC01 output channels
- Comparator reference

Comparator

- Four units
- Propagation delay of less than 150 ns
- DAC0 can be a reference or source to the comparator.
- Support for byte reversal of input/output data
- Compatible with DMA

Development Support

- Serial Wire Debug (SWD)

Package

- 100-pin LQFP
- 80-pin LQFP
- 64-pin LQFP

Operating Voltage

- 2.7 V to 5.5 V

Operating Temperature

- Commercial grade (-40°C to + 105°C)

Applications

Inverter motor controller

Compressor and Fan

Air-conditioner, Refrigerator

Product Selection Table

Table 1. Device Summary

Device Name	Code Flash	Data Flash	SRAM	SPI	UART	I2C	MPWM	ADC	I/O Ports	Package
A34M456VL2N	256 KB	32 KB	32 KB	2	6	2	2	22	88	100-LQFP-14x14
A34M456MM2N	256 KB	32 KB	32 KB	2	6	2	2	22	68	80-LQFP-14x14
A34M456RL2N*	256 KB	32 KB	32 KB	2	4	2	2	12	55	64-LQFP-10x10
A34M456RK2N*	256 KB	32 KB	32 KB	2	4	2	2	14	53	64-LQFP-10x10

* For available options or further information on the devices with “*” marks, please contact the [ABOV sales office](#).

Contents

Features	1
Applications	2
Product Selection Table	3
1. Descriptions	9
1.1 General Information	9
1.2 Product Category Definition	9
1.3 Availability of Peripherals	10
1.4 Block Diagram	18
1.5 Functional Overview	19
1.5.1 Cortex-M4F Core	19
1.5.2 FPU (Floating Point Unit)	19
1.5.3 Embedded SRAM	19
1.5.4 Boot Configuration	19
1.5.5 Power Supply	20
1.5.6 Operation Mode	21
1.5.6.1 Transition of Operation Mode	21
1.5.6.2 RUN Mode	21
1.5.6.3 SLEEP Mode	21
1.5.6.4 DEEP-SLEEP (STOP1, STOP2) Mode	21
1.5.6.5 Reset Mode	21
1.5.7 Clocks and Startup	22
1.5.7.1 HCLK Clock	22
1.5.7.2 PCLK Clock	22
1.5.7.3 Clock Configuration Procedure	22
1.5.8 Interrupts and Events	23
1.5.8.1 NVIC (Nested Vectored-Interrupt Controller)	23
1.5.8.2 Extended Interrupt (EXTI)	23
1.5.9 GPIO	24
1.5.9.1 PCU Module	24
1.5.9.2 GPIO Module	24
1.5.10 Embedded Flash Memory	24
1.5.11 DMA	25
1.5.12 Timers	26
1.5.12.1 16-bit Timer	26
1.5.12.2 FRT	26
1.5.12.3 WDT	26
1.5.12.4 SysTick Timer	27
1.5.13 UART	28
1.5.14 SPI	28
1.5.15 I2C	29
1.5.16 MPWM	29
1.5.17 PFCP	30
1.5.18 ADC	30
1.5.19 Comparator	30
1.5.20 DAC	31
1.5.21 RNG	31
1.5.22 CRC	31

1.6	Development Support	32
1.6.1	Toolchain Support	32
1.6.2	Debug Interface	33
1.6.2.1	Serial Wire Debug Port (SWJ-DP)	33
1.6.2.2	SWD Connection Guide	33
1.6.3	Trace Support	34
1.6.3.1	Serial Wire Output (SWO)	34
2.	Pinouts and Pin Descriptions	35
2.1	Pinouts	35
2.1.1	A34M456VL (100-LQFP)	35
2.1.2	A34M456MM (80-LQFP)	36
2.1.3	A34M456RL (64-LQFP)	37
2.1.4	A34M456RK (64-LQFP)	38
2.2	Pin Description	39
2.3	Alternate Function Pins	47
3.	Electrical Characteristics	50
3.1	Parameter Conditions	50
3.1.1	Minimum and Maximum Values	50
3.1.2	Typical Values	50
3.1.3	Typical Curves	50
3.1.4	Pin Input Voltage	50
3.1.5	Power Supply Scheme	51
3.1.6	Current Consumption Measurement	52
3.2	Absolute Maximum Ratings	53
3.3	Operating Condition	54
3.3.1	General Operating Condition	54
3.3.2	Power-On Reset Characteristics	54
3.3.3	Operating Condition at Power-Up/Power-Down	54
3.3.4	Embedded Reset and Power Control Block Characteristics (LVR, LVI)	55
3.3.5	Embedded Voltage Reference	57
3.3.6	Supply Current Characteristics	58
3.3.6.1	Supply Current Consumption	58
3.3.6.2	I/O System Current Consumption	58
3.3.6.3	I/O Static Current Consumption	59
3.3.6.4	I/O Dynamic Current Consumption	59
3.3.7	External Clock Source Characteristics	60
3.3.7.1	High-Speed External Clock Generated from Crystal/Ceramic Resonator	60
3.3.7.2	Low-Speed External Clock Generated from Crystal Resonator	63
3.3.8	Internal Clock Source Characteristics	65
3.3.8.1	High-Speed Internal (HSI) RC Oscillator	65
3.3.8.2	Low-Speed Internal (LSI) 500 kHz RC Oscillator	65
3.3.9	PLL Characteristics	66
3.3.10	Flash Memory Characteristics	66
3.3.11	I/O Port Characteristics	67
3.3.11.1	General Input/Output Characteristics	67
3.3.11.2	Output Driving Current	69
3.3.11.3	Output Voltage Levels	69
3.3.12	ADC Characteristics	70
3.3.13	DAC Characteristics	71

3.3.14	Comparator Characteristics	72
3.3.14.1	General PCB Design Guidelines	72
3.3.15	Communication Interfaces Characteristics	73
3.3.15.1	I2C Interface Characteristics	73
3.3.15.2	SPI Interface Characteristics	74
4.	Package Information	75
4.1	100-LQFP Package Information	75
4.2	80-LQFP Package Information	76
4.3	64-LQFP Package Information	77
5.	Ordering Information	78
	Glossary	79
	Revision History	80

List of Tables

Table 1. Device Summary	3
Table 2. A34M456 Series Memory Density	9
Table 3. A34M456 Series Features and Peripherals	10
Table 4. Summary of A34M456 Peripherals	17
Table 5. Boot Mode Pin List	19
Table 6. Power Supply	20
Table 7. Features of I2Cn (n = 0 to 1)	29
Table 8. PWM Modes of MPWM	29
Table 9. Legend and Abbreviations Used in Pin Description	39
Table 10. Pin Description	40
Table 11. GPIO Alternate Function ⁽¹⁾	47
Table 12. Voltage Characteristics	53
Table 13. Current Characteristics	53
Table 14. Thermal Characteristics	53
Table 15. General Operating Condition	54
Table 16. POR Electrical Characteristics	54
Table 17. Operating Condition at Power-Up/Power-Down	54
Table 18. Low Voltage Reset Characteristics	55
Table 19. Low Voltage Indicator Characteristics	56
Table 20. Embedded Internal Voltage Reference ⁽¹⁾	57
Table 21. Supply Current Characteristics	58
Table 22. HSE Oscillator Characteristics ⁽¹⁾	60
Table 23. LSE Oscillator Characteristics ⁽¹⁾ (f _{LSE} = 32.768 kHz)	63
Table 24. HSI Oscillator Characteristics ⁽¹⁾	65
Table 25. LSI Oscillator Characteristics	65
Table 26. PLL Characteristics ⁽¹⁾	66
Table 27. Code Flash Memory Characteristics	66
Table 28. Data Flash Memory Characteristics	66
Table 29. I/O Static Characteristics	67
Table 30. Output Voltage Characteristics ⁽¹⁾	69
Table 31. ADC Electrical Characteristics	70
Table 32. DAC Electrical Characteristics	71
Table 33. Comparator Characteristics	72
Table 34. I2C Characteristics	73
Table 35. SPI Characteristics	74

List of Figures

Figure 1. A34M456 Block Diagram	18
Figure 2. SWD Interface Connection	33
Figure 3. 100-LQFP Pinouts	35
Figure 4. 80-LQFP Pinouts	36
Figure 5. 64-LQFP Pinouts	37
Figure 6. 64-LQFP Pinouts	38
Figure 7. Pin Input Voltage	50
Figure 8. Power Supply Scheme	51
Figure 9. Current Consumption Measurement	52
Figure 10. Crystal/Ceramic Oscillator	61
Figure 11. External Clock	61
Figure 12. Clock Timing Measurement at XIN	61
Figure 13. Typical Application with 8 MHz Crystal	62
Figure 14. Crystal Oscillator	64
Figure 15. Clock Timing Measurement at SXIN	64
Figure 16. Typical Application with a 32.768 kHz Crystal	64
Figure 17. I/O Input Characteristics (Temperature: 25°C)	68
Figure 18. Package Dimension (100-LQFP)	75
Figure 19. Package Dimension (80-LQFP)	76
Figure 20. Package Dimension (64-LQFP)	77
Figure 21. A34M456 Series Device Ordering Information	78

1. Descriptions

1.1 General Information

The A34M456 series is a 32-bit high-performance microcontroller with up to 256 KB of flash memory. It is a powerful microcontroller that provides effective solutions to various electrical appliances that require both low power consumption and high performance (Arm Cortex-M4 with FPU core).

The A34M456 series is a 32-bit microcontroller based on the high-performance Arm Cortex-M4F+ core. It has up to 256 KB of code flash memory, 32 KB of data flash memory, and 32 KB of SRAM. It is well-suited for a wide range of home appliances, such as air conditioners, refrigerators, washing machines, clothes dryers, dishwashers, water purifiers, and blenders. It is also suitable for use in high-performance inverters for motor control.

1.2 Product Category Definition

Table 2 provides an overview of the memory capacity for available devices in the A34M456 series.

This document provides an overview of each device's supported features, including high-level information and brief explanations for each feature.

Refer to Table 3 for the list of features supported by each product category.

Table 2. A34M456 Series Memory Density

Memory Density		Category
Flash	RAM	
256 KB	32 KB	A34M456

1.3 Availability of Peripherals

Table 3 summarizes and lists product-specific features available in the A34M456 series, considering the largest package.

Table 3. A34M456 Series Features and Peripherals

Peripherals		Description
Core	CPU	• Maximum operating frequency: 140 MHz • 32-bit ARM Cortex-M4F CPU 1. 32-bit Thumb@-2 instruction set • Register settings in CPU: 2. General-purpose registers specified 3. Main stack pointer (MSP) and process stack pointer (PSP): R13 4. Link register (LR): R14 5. Program counter (PC): R15 • Data ordering format: Little-Endian • Harvard Architecture • AHB/APB
	Interrupt	• NVIC (Nested-Vectored Interrupt Controller) • Up to 86 peripheral interrupts supported • Assignable with 16 different priority levels
	FPU	• Rendered by extending and transforming the ARMv7 floating-point arithmetic functionality • Compliant with the ANSI/IEEE 754 standard • Capable of binary floating-point arithmetic and computation

Table 3. A34M456 Series Features and Peripherals (continued)

Peripherals		Description
Memory	Code Flash	- Capacity: 6. A34M456: 256 KB Code Flash memory - Built-in high-capacity Code Flash memory 512 bytes, 2 KB erases - Bulk (full chip) erase - Read protection - Self-programming - CRC code generation and verification for the Flash memory - Endurance: 10,000 cycles - Lifetime: 10 years
	Data Flash	- Capacity: 32 KB 512 bytes, 2 KB erases - CRC code generation and verification for the Flash memory - Endurance: 100,000 Cycles - Lifetime: 10 years
	BootROM	- Executes the processor's boot mode when receiving an input at the nBOOT pin from an external circuit. - UART boot modes - In-system programming - Users can program data into the internal Flash memory by setting up an application board.
	SRAM	- Capacity: 32 KB - Usable as a program's work area - High-speed execution enables the execution of time-critical codes. - Part of the SRAM can be remapped into an interrupt vector area
System Control Unit (SCU)	Clock	- High-speed internal oscillator (HSI) 7. 8 MHz ($\pm 1.0\%$ @ -40°C to $+105^{\circ}\text{C}$) - Low-speed internal oscillator (LSI) 8. 500 kHz ($\pm 30\%$ @ -40°C to $+105^{\circ}\text{C}$) - External main oscillator (HSE): 4 MHz to 16 MHz - External sub-oscillator (LSE): 32.768 kHz - Phase-locked loop (PLL) frequency generator generates a high-speed clock (up to 140 MHz)
	Clock monitoring	- System Fail-Safe function by Clock Monitoring 9. External main oscillator (HSE) 10. External sub oscillator (LSE) 11. Main system clock (MCLK)

Table 3. A34M456 Series Features and Peripherals (continued)

Peripherals		Description
System Control Unit (SCU)	Reset	• nRESET pin reset • Core reset • Software reset • POR (Power-On Reset) • LVR (Low-Voltage Reset) • WDTR (Watch Dog Timer Reset) • Reset due to clock oscillating error
	LDO	Low-dropout (LDO) regulator built in for low-voltage operation
	POR	The POR generator detects an internal 1.92V voltage and generates a reset signal.
	LVI	• 10 low-voltage detection levels • Supports interrupts • Supports wake-up from SLEEP mode
	Wake-up	• Wake-up by GPIO pin • Wake up by FRT • Wake-up by WDT • Wake-up by LVI
General-Purpose I/O (GPIO)		• Input/output (I/O) port for general purposes. • 100-LQFP 12. I/O pins: 88 • 80-LQFP 13. I/O pins: 68 • 64-LQFP 14. I/O pins: 55(RL), 53(RK) • Each pin can be set for one of the following modes: 15. Push-pull output 16. Open drain output 17. Input • The use of each pin can be set by setting the multiplexer. • Each pin can be configured as an external interrupt source, either the high-level/low-level interrupt or the rising-edge/falling-edge interrupt. • Pull-up or pull-down resistor, and debouncing can be set for each pin. • Drive strength can be adjusted for each port pin. • Each pin bit can be individually set/reset. • Wake-up events triggered by external asynchronous inputs.

Table 3. A34M456 Series Features and Peripherals (continued)

Peripherals		Description
DMA Controller		8-channel direct memory access (DMA) support peripherals 8-/ 16-/ 32-bit data transfers - Operates in conjunction with 12 peripherals: - SPIx (SPI0, SPI1) - UARTx (UART0, UART1, UART2, UART3, UART4, UART5) - CRC - ADC (ADC0, ADC1, ADC2)
TIMER	16-bit Timer	- General-purpose 16-bit up-count timer 10 channels 10 timer n capture port (TnIO) input channels 10 timer n output port (TnIO) output channels - Timer operating modes - Periodic timer mode - One-shot mode - PWM mode - Capture mode - Interrupt events - Timer/counter-match interrupt - Timer overflow interrupt - Input clock selection - Clocks are freely selectable through the miscellaneous clock control registers (SCU_MCCRx) - External clocks are selectable. - Timer signals can be generated through TnIO pins. 10-bit prescaler
	WDT	32-bit down-count timer - Reset and periodic interrupts - Clocks are freely selectable through the miscellaneous clock control registers (SCU_MCCRx) - Eight different prescalers are selectable
	FRT	- Two units 32-bit free-run timer - Capable of calculating the internal system time. 32-bit up-count timer - Interrupt events - Period interrupt - Overflow interrupt

Table 3. A34M456 Series Features and Peripherals (continued)

Peripherals		Description
Serial Interface	UART	• Six units • A total of six 16450 asynchronous serial communication ports • Configurable standard asynchronous communication bits (start, stop, and parity) • Flexible communication available through programming 36. 5- to 8-bit data transfers 37. Even/Odd/Non-parity generation and checking 38. 1-bit, 1.5-bit, or 2-bit stop-bit generation and checking • 8-bit fraction controller and 16-bit baud rate generator
	SPI	• Two units • Two synchronous serial communication port channels • Master/slave operation • Loop-back mode • Programmable and flexible communication • 8-/ 9-/ 16-/ 17-bit data transmit/receive 39. SPI clock speed 40. Both least significant bit (LSB)-first and most significant bit (MSB)-first modes available
	I2C	• Two units • Standard I2C communication protocol • Master and slave modes supported for each channel. • 7-bit addressing supported for slave mode • SCL signal's high/low periods and SDA signal's hold time settable
PWM	MPWM	• Two units • Motor PWM generator • Six channels (high and low signals of phases U, V, and W) generate different waveforms. • 16-bit up counter and up-down counter • Eight ADC Trigger Sources 41. 6-Variable Triggers 42. 2-Fixed Trigger (Bottom, Period Match) • Interrupt events 43. Bottom interrupts 44. Top (period) interrupts 45. Interval interrupt mode • Falling/rising dead-time applicable • A special operating mode: • Protection and over-current detection supported

Table 3. A34M456 Series Features and Peripherals (continued)

Peripherals		Description
PWM	PFCP	• PFC (Power-Factor Correction) PWM • Single/Interleaved/Complementary mode • Dead-time support • Protection supported • Eight ADC Trigger Sources 46. 6-Variable Triggers 47. 2-Fixed Trigger (Bottom, Period Match)
Analog Block	12-bit ADC	• Three units • 22 analog input pins • Four operating modes: 48. Single conversion 49. Sequence conversion 50. Burst conversion 51. Multiple conversion • Up to eight sequential conversions supported. • Software triggers supported • Three internal trigger sources (MPWM, PFCP, and Timers) supported. • Sample time and hold time are adjustable
	10-bit DAC	• Two units • Comparator reference supported • 10-bit resolution
	Comparator	• Four units • Equipped with comparators 0 and 2, each of which has four input sources. • Equipped with comparators 1 and 3, each of which has four input sources. • Signals from the DAC can be a reference or source to the comparator.
Security	RNG	• Random-number generator • Interrupt events • Generator ready interrupt • Error interrupt
	CRC	• CRC operating modes: 52. CRC-32 (0x04C1_1DB7) 53. CRC-16-IBM (0x8005) 54. CRC-8 (0x07) 55. CRC-7 (0x09) • Input/output data reversion supported. • Compatible with DMA

Table 3. A34M456 Series Features and Peripherals (continued)

Peripherals	Description
Operating Voltage	2.7 V to 5.5 V
Operating temperature	Commercial grade (-40°C to +105°C)
Package	• Three types of package options 56. 100-LQFP (VL) 57. 80-LQFP (MM) 58. 64-LQFP (RL, RK)

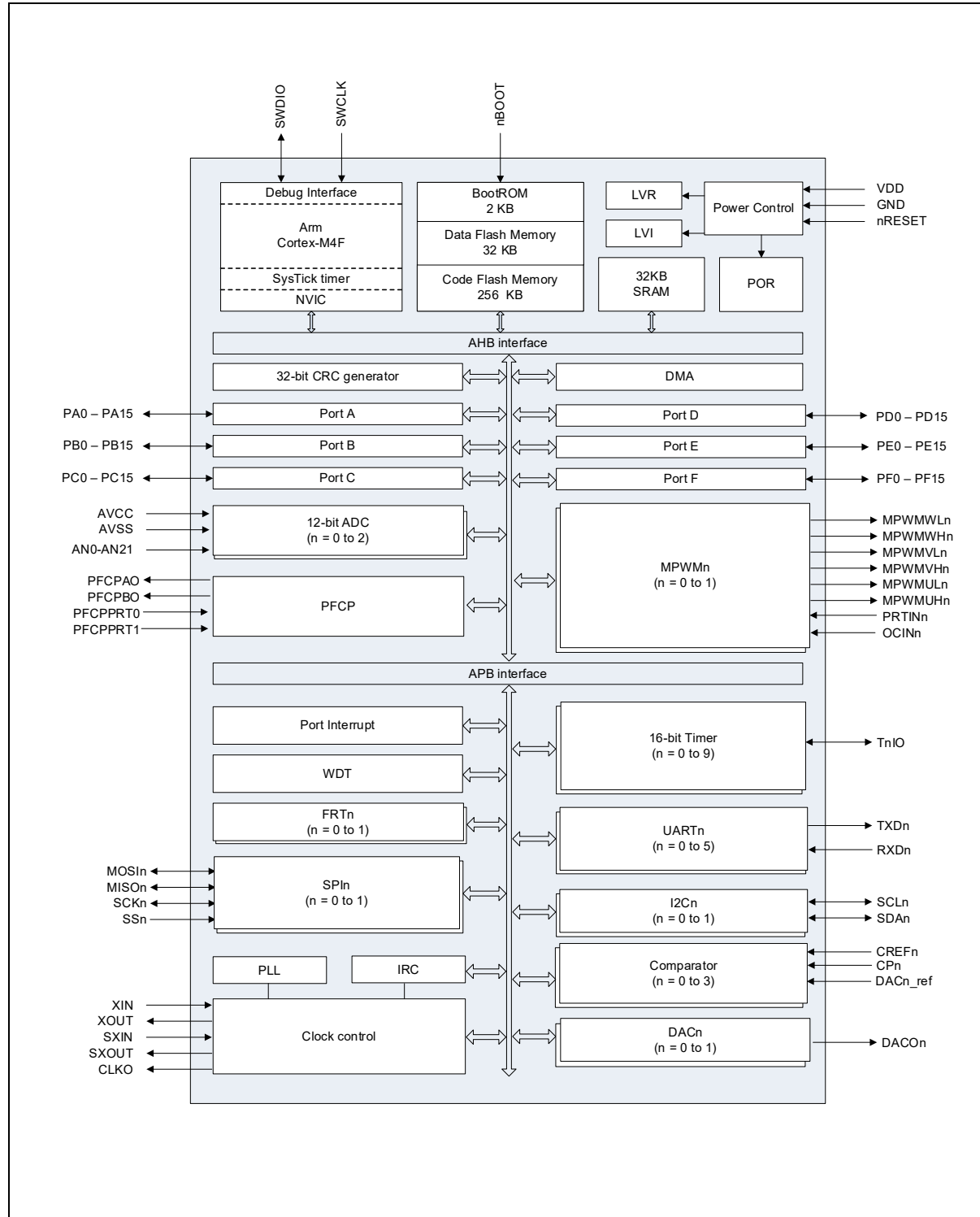
Table 4. Summary of A34M456 Peripherals

Peripheral		A34M456VL	A34M456MM	A34M456RL (RK)
Core		Cortex-M4F		
Max. Operating frequency		140 MHz		
Memory	Code Flash	256 KB		
	Data Flash	32 KB		
	SRAM	32 KB		
GPIO		88	68	55 (53)
DMA		8		
Timer	WDT	1		
	FRT	2		
	GP Timer	10		
	SysTick timer	1		
Communication Interface	UART	6	4	4
	SPI	2	2	1
	I2C	2	2	1
Analog Block	MPWM	2		
	PFCP	1		
	ADC Number of channels	2.0 Msps	2.0 Msps	2.0 Msps
		22	19	12 (14)
	DAC	2		
	Comparator	4		
Security	RNG	1		
	CRC	1		
Operating voltage		2.7 V to 5.5 V		
Operating temperature		Ambient operating temperature: -40°C to 105°C		
Packages		100-LQFP	80-LQFP	64-LQFP

1.4 Block Diagram

Figure 1 shows a block diagram of A34M456 series.

Figure 1. A34M456 Block Diagram



1.5 Functional Overview

The following sections provide overviews of the features of the A34M456 series microcontroller.

1.5.1 Cortex-M4F Core

The Arm Cortex-M4F has the same functions as the Cortex-M4 and includes optional floating-point arithmetic functionality. The processors are intended for deeply embedded applications that require fast interrupt response features.

1.5.2 FPU (Floating Point Unit)

Cortex-M4 FPU is an implementation of the single precision variant of the ARMv7-M Floating-Point Extension (FPv4-SP). It provides floating-point computation functionality that is compliant with the ANSI/IEEE Std 754-2008, IEEE Standard for Binary Floating-Point Arithmetic, referred to as the IEEE 754 standard. The FPU supports all single-precision data-processing instructions and data types described in the ARM®v7-M Architecture Reference Manual.

1.5.3 Embedded SRAM

The A34M456 series has a block of 0-wait on-chip SRAM. The SRAM is 32 KB in size, and its base address is 0x2000_0000.

The SRAM memory area is commonly utilized for storing data and as a stack memory. It can also be utilized for storing program code for faster execution or during Flash erase/programming operations. This device does not support a memory remap strategy. Therefore, it is necessary to perform a jump and return to execute the code stored in the SRAM memory area.

1.5.4 Boot Configuration

The A34M456 series has a boot mode option to program internal Flash memory. Boot mode can be entered by setting nBOOT pin to 'L' at reset timing (normal state is 'H').

UART Boot mode: pins for the boot mode are listed in Table 5.

Table 5. Boot Mode Pin List

Block	Pin Name	Pin Direction	Description
SYSTEM	nRESET/PA6	Input	Reset input signal
	nBOOT/PA4	Input	Boot mode setting pin
UART0	RXD0/PD2	Input	UART boot receive data
	TXD0/PD3	Output	UART boot transmit data

1.5.5 Power Supply

The device requires a 2.7 V to 5.5 V operating voltage supply (VDD).

Table 6. Power Supply

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	VDD	2.7	5.5	V
	AVDD (Analog VDD)	2.7	5.5	V

During a power-up process, a reset plays an important role and affects the entire process of system booting. The A34M456 series has two power-related reset options as described below:

- POR_RST (Power-On Reset) is asserted when the voltage drops below V_{RESET} .
- LVD_RST (Low-Voltage Detect Reset) is asserted when the voltage drops below V_{LVR0} (default).

If the power level is higher than the POR and below the flash memory operating voltage, the Code Read operation may malfunction. To prevent this abnormal Code Read operation, the LVD_RST operates to generate the SYSRESETn internal signal and enter the microcontroller into reset mode to prevent the abnormal operation.

1.5.6 Operation Mode

1.5.6.1 Transition of Operation Mode

INIT mode is the initial state of the chip when a reset is asserted. In RUN mode, the CPU operates at the maximum performance with the high-speed clock system.

SLEEP mode and DEEP-SLEEP mode can be used as low power consumption mode. In the low power consumption mode, power is effectively managed to reduce power consumption by halting the processor core and any unused peripherals.

1.5.6.2 RUN Mode

In RUN mode, the CPU and peripheral hardware operate with a high-speed clock. If the INIT state occurs after a reset, the system enters RUN mode.

1.5.6.3 SLEEP Mode

Once the microcontroller enters SLEEP mode, the CPU becomes inactive. By setting the SCU_PER and SCU_PCER, users can determine which peripherals are to be inactive in SLEEP mode.

1.5.6.4 DEEP-SLEEP (STOP1, STOP2) Mode

When the core goes into a stop state using the WFI instruction, the chip enters DEEP-SLEEP mode, which is divided into DEEP-SLEEP (STOP 1) and DEEP-SLEEP (STOP 2) modes.

1.5.6.5 Reset Mode

The A34M456 series has two system reset options. One is a cold reset, which is effective during power up or down sequence; the other is a warm reset, which is generated by several reset sources.

The reset features of the A34M456 series are as follows:

- Power-On reset (POR)
- Low-Voltage Detect Reset (LVR)
- nRESET pin reset
- Watchdog timer (WDT) reset
- Software reset
- Clock oscillating error reset
- CPU request reset

1.5.7 Clocks and Startup

The A34M456 series has two main operating clocks: HCLK, which generates clock signals for CPU and AHB systems, and PCLK, which generates clock signals for peripheral systems.

1.5.7.1 HCLK Clock

The Cortex-M4F CPU requires two clocks, the HCLK and FCLK. The HCLK is fed to the CPU and AHB. The FCLK stays enabled except in DEEP-SLEEP mode, whereas the HCLK can be disabled in SLEEP mode.

The buses and memories are clocked by the HCLK. As the bus clock frequency is limited to a maximum of 140 MHz, the HCLK frequency must not exceed 140 MHz.

1.5.7.2 PCLK Clock

The PCLK can be used as a clock for any peripherals. Whether to enable or disable the PCLK for each peripheral is determined with the SCU_PCER registers; each peripheral block's registers cannot be read unless its PCLK input is enabled. And the PCLK stops operating in DEEP-SLEEP mode.

1.5.7.3 Clock Configuration Procedure

After powering on the device, the HSI can be enabled with the SCU_CSCR register (Clock source control register). Before enabling the HSE block, the pin mux configuration must be completed for XIN and XOUT. Users must be careful not to affect other bits of the PC_MR and PC_CR registers during this process. Once the HSE block has been enabled, the users must wait for crystal oscillation to stabilize.

The secondary LSE (32.768 kHz) clock can be enabled with the SCU_CSCR register. Likewise, with pins XIN and XOUT for the HSE, the LSE must be enabled after the pin mux configuration is completed for SXIN and SXOUT and the stabilizing time has elapsed.

1.5.8 Interrupts and Events

1.5.8.1 NVIC (Nested Vectored-Interrupt Controller)

The A34M456 series includes up to 65 maskable interrupt channels that manage sixteen priority levels and the Nested Vector Interrupt Controller (NVIC) that controls 16 interrupt lines of the Cortex®-M4.

The NVIC has the following advantages:

- NVIC enables interrupt processing while reducing interrupt latency.
- Interrupt Vector Table (IVT) address delivered directly to the core.
- The fast interrupt processing capability
- Higher priority interrupts are completed before lower priority interrupts, although they are generated later than the lower priority interrupts.
- Tail chaining
- Automatic saving of processor state
- Interrupt restoring without instructional overhead at the end of the interrupt.

The NVIC hardware block provides flexible and efficient interrupt management with minimal interrupt latency.

1.5.8.2 Extended Interrupt (EXTI)

The Extended Interrupt feature enables the system to generate event requests or wake up from STOP mode. Each external line can be configured independently to detect trigger events such as rising or falling edges, or both edges, as well as level events such as Low or High.

1.5.9 GPIO

1.5.9.1 PCU Module

A34M456 series has a Port Control Unit (PCU) module that controls the external input and output (I/O) ports. By setting the PCU registers, users can configure the pins' uses, input/output direction, Pull-up/Pull-down, and debouncing for their applications as needed.

1.5.9.2 GPIO Module

Pins except the VDD, GND, and certain specific-purpose pins can be used as General-Purpose Input/Output (GPIO) pins. The GPIO module controls the general I/O ports. Output pins can be set to generate high or low-level signals by configuring the corresponding bits of the GPIO control register, while logic input pins can be monitored for their input status in the control registers.

1.5.10 Embedded Flash Memory

The Flash memory controller is an interface controller for embedded flash memory. It manages data stored on flash memory and communicates with other electronic devices.

Code Flash memory of the A34M456 series has key features as listed below:

- 256 KB with write protection bits
- 512 bytes, 2 KB erases
- Bulk (full chip) erases
- Zero wait (less than 28 MHz), 1- to 15-wait, and cache (Flash acceleration) access
- Instruction and Data Cache
- Read Protection
- Built-in 16-bit CCITT CRC for Flash memory

Data Flash memory of the A34M456 series has key features as listed below:

- 32 KB with write protection bits
- 512 bytes, 2 KB erases
- Bulk erases
- Zero wait (less than 28 MHz), 1- to 15-wait
- Built-in 16-bit CCITT CRC for Flash memory

1.5.11 DMA

The direct memory access (DMA) controller is used for high-speed data transfers between peripherals and memories. The DMA allows quick data transfers by copying or moving data between memory locations or between memory and peripherals, without involving the core.

- 8 channels
- Only single-ended signaling
- 8-bit/ 16-bit/ 32-bit data transfers
- Multiple buffers of the same size
- DMA transfers are triggered by peripheral interrupts

1.5.12 Timers

1.5.12.1 16-bit Timer

A34M456 series has a Timer module configured with 10 units. This 16-bit Timer supports four operating modes: Periodic mode, PWM mode, One-shot mode, and Capture mode.

Users can use a divided PCLK or an external clock as a clock source for the 16-bit Timer. An internal 10-bit prescaler allows the generation of a variety of timer base clocks.

Interrupts can be triggered at regular intervals when the timer is used in Periodic mode. Users can set the period and duty to form a PWM signal that is used in PWM mode.

In One-shot mode, the timer can generate one PWM waveform. The Capture mode allows measuring the pulse intervals of an external input signal based on the predefined conditions. In addition, this timer can transmit signals to control other devices and is primarily used as a periodic tick timer or as a wake-up source.

1.5.12.2 FRT

The A34M456 series has two built-in Free-run Timers (FRT) that are 32-bit up-count timers. According to their register setting, the FRT can run with an overflow interrupt or a match interrupt and can remain active in DEEP-SLEEP (STOP 1) mode.

1.5.12.3 WDT

The Watchdog Timer (WDT) is used to detect errors in the microcontroller caused by external interference or unexpected conditions. These errors cause the application program to deviate from its normal sequence. If the microcontroller loses control, the WDT will reset the microcontroller, allowing it to return to normal operation.

The A34M456 series' WDT is a 32-bit down counter. If the WDT is set as a reset source, the microcontroller restarts when the down counter reaches zero.

When it is not used to monitor the microcontroller, the WDT can be used as a cycle timer along with an interrupt.

1.5.12.4 SysTick Timer

Although the SysTick timer is primarily designed for real-time operating systems, it can also be utilized as a standard down-counter.

The SysTick timer has the following features:

- 24-bit down-counter
- Automatic refreshing
- Maskable system interrupt generation when the counter reaches zero.
- Programmable clock source

1.5.13 UART

The A34M456 series has a six-channel UART module. The built-in UART module allows users to specify settings for transmitting and receiving data and provides the ability to read the current status of the UART. By providing information about the current state of transmission and reception processes, including types and conditions, the UART module enables users to monitor potential errors such as parity, overrun, framing, or break interrupts during data reception.

The UART module includes a programmable baud-rate generator for each channel, which generates an internal clock for its corresponding UART unit. This is achieved by dividing a prescaled clock using a baud-rate divisor that ranges from 1 to 65535 and then dividing the result by 16.

Users can program interrupts that can control UART communication.

Furthermore, the built-in DMA allows the UART module to transfer data directly to or from memory without involving the CPU, reducing CPU usage, and increasing the speed of data transfer.

1.5.14 SPI

The A34M456 series has two built-in Serial Peripheral Interface (SPI) modules. The SPI modules are synchronized by clocks, and the specifications of the transfer clocks are adjustable.

The SPI module supports communication between one master and slaves. Slaves can be selected by the Slave Select (SS) signal.

The SPI module performs four-wire synchronous transfers via four signal terminals (SS, SCK, MOSI, and MISO). Its separate Transmit and Receive Buffers enable full-duplex communication, which can read and write data simultaneously.

Specifically, the SPI module of the A34M456 series can enhance the Port Drive Strength so that the SPI rate can be supported up to 16 MHz with the enhanced Port Drive Strength.

1.5.15 I2C

The I2C (Inter-integrated Circuit) interface built in the A34M456 series satisfies the standard I2C communication protocol and is used for serial communication with internal and external devices via the I2C protocol.

Equipped with two units, it supports both master and slave modes and can transmit and receive data in bytes using interrupts or polling.

The I2C of the A34M456 series operates in Standard mode (100 kHz) or Fast mode (400 kHz) and supports General calls.

It helps communicate with various peripherals that have the same bus type. To use the I2C, it is recommended to set the SCL and SDA pins to open-drain and then connect external pull-up resistors to render their output signals 'HIGH'.

Table 7. Features of I2Cn (n = 0 to 1)

I2C Features	I2C0	I2C1
7-bit addressing mode	O	O
Standard-mode (up to 100 kbit/s)	O	O
Fast-mode (up to 400 kbit/s)	O	O
General call	O	O

1.5.16 MPWM

The A34M456 series supports two Motor Pulse-Width Modulation (MPWM) units. The MPWM in the A34M456 series operates a total of 3 PWM modes as shown below to support various applications:

- Motor PWM mode-0 and Motor PWM mode-1 for motor control
- Normal PWM mode for a variety of PWM applications

In Motor or Normal PWM mode, the MPWM module of the A34M456 series supports many different PWM control functionalities, such as up to 6 channels' outputs, dead-time, up to 8 ADC triggers, a variety of interrupt event generations in many different conditions, protection events, and so on.

Table 8. PWM Modes of MPWM

PWM Mode	Counter Mode	Symmetric/Asymmetric Mode
Motor PWM mode 0	Up-down counter	2-channel symmetric mode
		1-channel asymmetric mode
		1-channel symmetric mode
Motor PWM mode 1	Up counter	-
Normal PWM mode	Up counter	-

1.5.17 PFCP

The PFCP is a power factor correction (PFC) PWM module designed to minimize the phase difference between voltage and current, improve the power factor, and suppress the harmonic currents.

The A34M456 series has three PFCP modes to support various applications for PFC control:

- Single PFC mode
- Interleaved PFC mode
- Complementary PFC mode

It supports up count and up-down count in all PFC PWM modes and provides two-channel outputs, up to 8 ADC triggers, generation of various interrupt events under various conditions, protection events, etc. In complementary PFC mode, dead-time can be applied to prevent shoot-through.

1.5.18 ADC

The A34M456 series ADC module is a 12-bit resolution Analog-to-Digital Converter (ADC) that consists of three independent controllable units and has up to 24 analog input channels. Input channels consist of 22 external pin inputs and two internal input channels.

This ADC module can process the A/D conversion of different channels in Single mode, Sequential mode, Multiple mode, and Burst mode. It can also sample the voltage inputs of multiple channels at critical times, which is required for various applications and can be achieved using the triggering functionality in association with Timer and MPWM.

Once the A/D conversion is complete, the result is left-aligned in 16-bit data registers.

The ADC is mapped to the AHB and capable of high-speed operation based on the internal clock source. In addition, it uses built-in DMA to reduce microcontroller core load while enabling fast data sampling.

The analog input monitoring and comparison capabilities of the ADC allow the applications to determine whether the input voltage is above or below the predefined level.

1.5.19 Comparator

The A34M456 series has four comparators. Each comparator outputs the comparison result of two analog voltages via an I/O pin or generates interrupts.

1.5.20 DAC

The Digital-to-Analog Convertor (DAC) in the A34M456 series provides a function to convert 10-bit digital value to analog output level for Comparator reference.

1.5.21 RNG

The A34M456 series has a built-in Random Number Generator (RNG) that operates with an RNG clock, which users can select from the clock source.

The RNG generates a random number based on the set seed value. If the users read data before the random number generation is completed, an error interrupt is flagged to prevent the users from reading the false data.

1.5.22 CRC

A Cyclic Redundancy Check (CRC) module is used to get 32-bit, 16-bit, 8-bit, and 7-bit CRC codes from 8-bit or 32-bit data sizes. The user application can utilize CRC-based technologies to ensure the integrity of data transfers, storage, and Flash memories in compliance with functional safety standards.

Specifically, the CRC module of the A34M456 series supports DMA.

1.6 Development Support

This chapter describes the development support features of the device. The device provides standard Arm® development support, including toolchain compatibility, debug interface, trace support, and on-board debug/programming connection.

The available debug and trace features may differ depending on the package and device option. Refer to the feature list, pin description, and electrical characteristics for detailed information.

1.6.1 Toolchain Support

The device supports software development using standard Arm-compatible toolchains, including Arm® Keil® MDK, IAR Embedded Workbench® for Arm, and GCC-based toolchains.

Device-specific startup files, linker scripts, header files, and software examples are provided separately for each product series and software package.

1.6.2 Debug Interface

1.6.2.1 Serial Wire Debug Port (SWJ-DP)

The device provides an Arm® Serial Wire Debug Port (SW-DP) for software debugging and in-system flash memory programming. The SW-DP uses a two-pin debug interface, SWDIO and SWCLK, to access the CPU debug logic, memory, registers, and on-chip debug resources.

The SWD pins may be multiplexed with GPIO or other alternate functions depending on the product and package. If the SWD pins are used for application functions, the target board and firmware must be designed so that the pins remain accessible during debugging or programming.

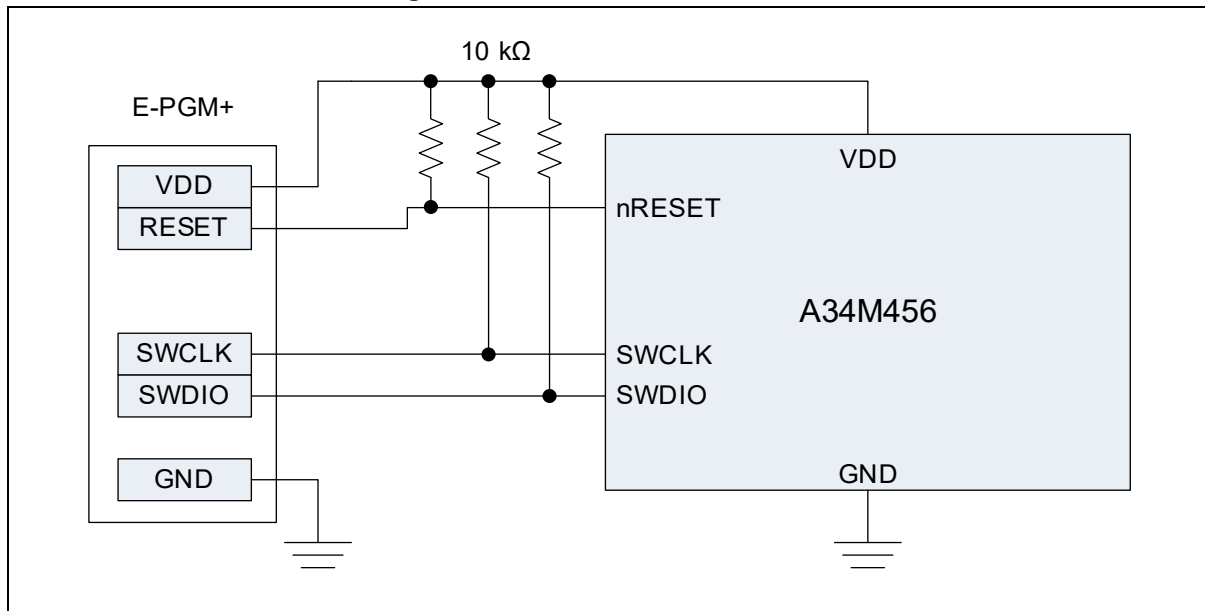
1.6.2.2 SWD Connection Guide

For on-board debugging and programming, the target board should provide access to SWDIO, SWCLK, VDD, VSS, and nRESET. The nRESET connection is recommended to improve debug connection reliability and device recovery.

The VDD pin provides the target voltage reference for the external debug probe. It should be connected to the target board supply voltage unless otherwise specified by the debug probe manufacturer.

If SWO trace is used, the target board should also provide access to the SWO pin.

Figure 2. SWD Interface Connection



1.6.3 Trace Support

1.6.3.1 Serial Wire Output (SWO)

The device supports Serial Wire Output (SWO) for trace output during debugging. SWO provides a single-pin trace output that can be used with the SWD interface to output software to trace messages and selected debug event information to an external debug probe.

SWO is intended for lightweight trace and debug monitoring. It does not provide full instruction trace reconstruction such as ETM.

To use SWO trace, the SWO pin must be assigned to the trace function and connected to the external debug/trace connector. Refer to the pin description for the available SWO pin.

2. Pinouts and Pin Descriptions

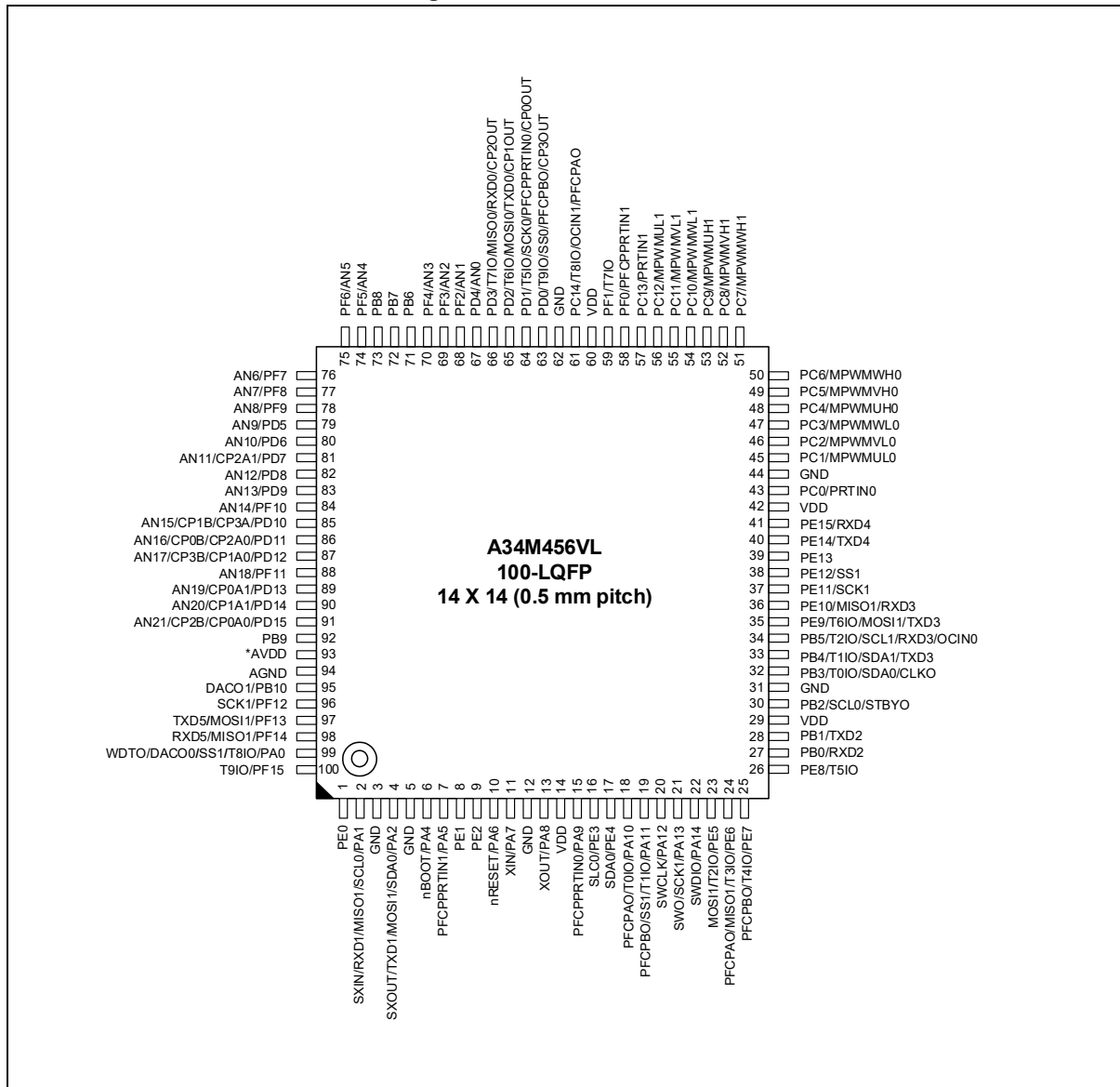
In this chapter, pinouts and pin descriptions of the A34M456 series are described.

2.1 Pinouts

Figure 3, Figure 4, Figure 5, and Figure 6 show the top views of the packages.

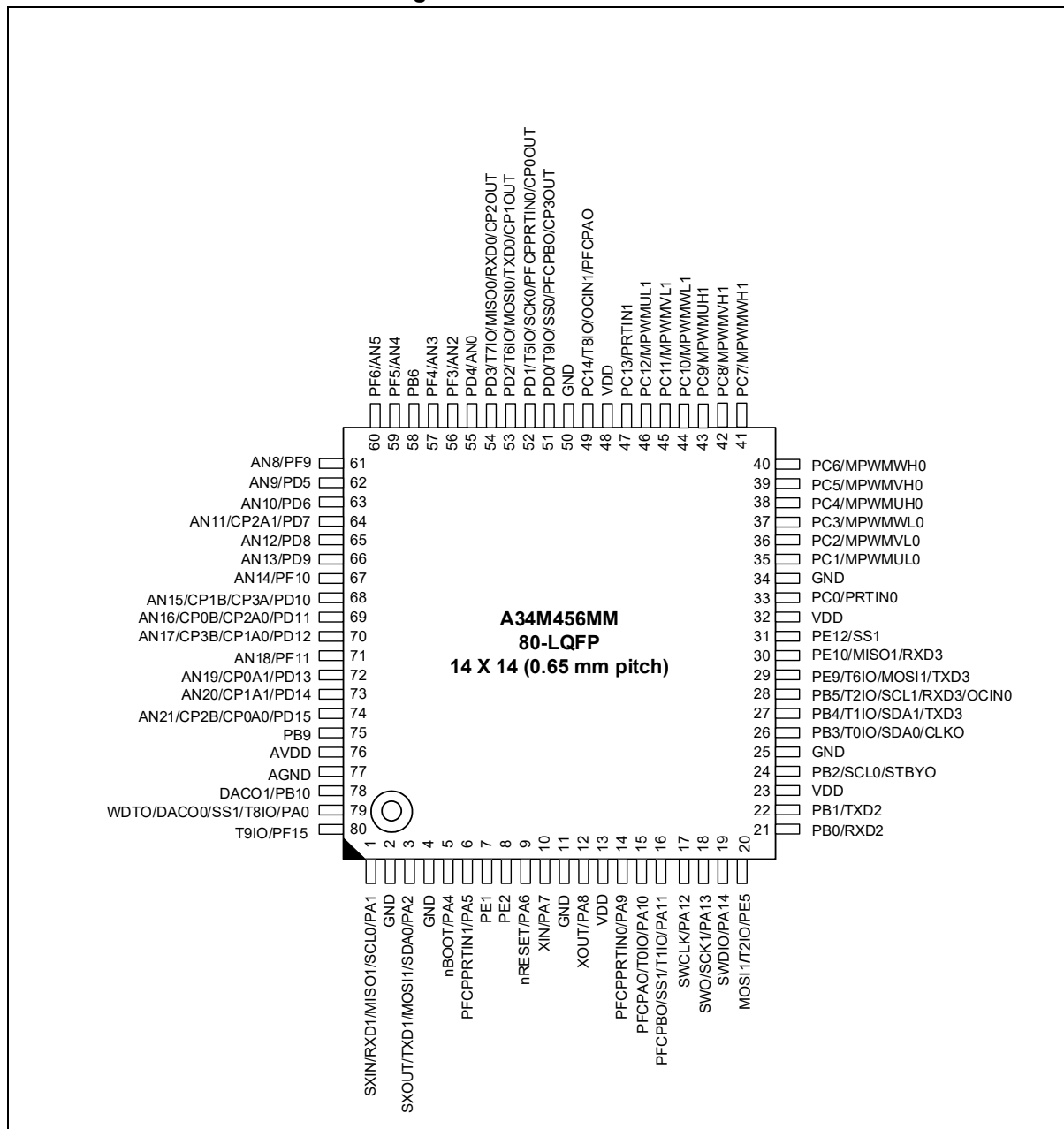
2.1.1 A34M456VL (100-LQFP)

Figure 3. 100-LQFP Pinouts



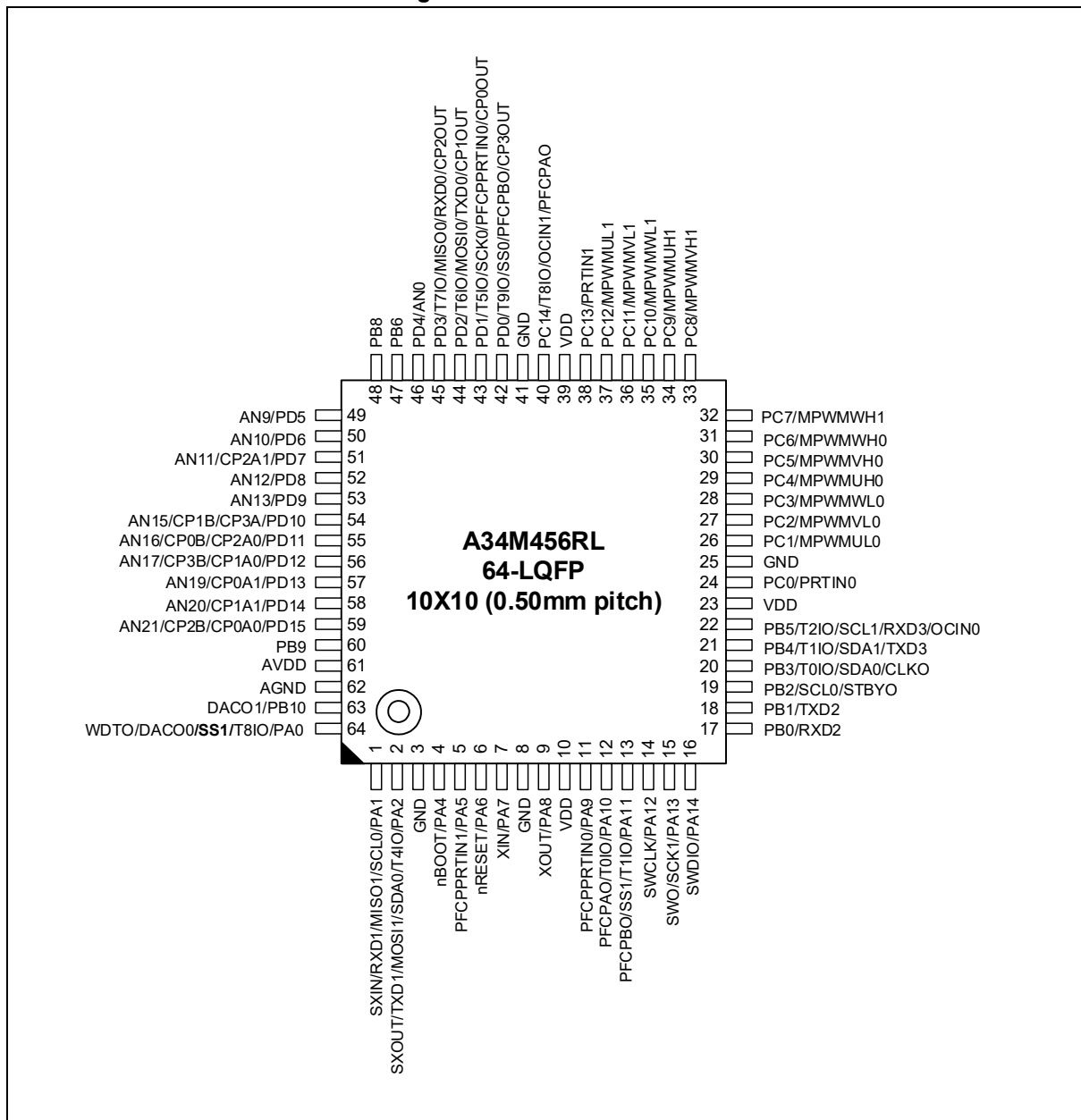
2.1.2 A34M456MM (80-LQFP)

Figure 4. 80-LQFP Pinouts



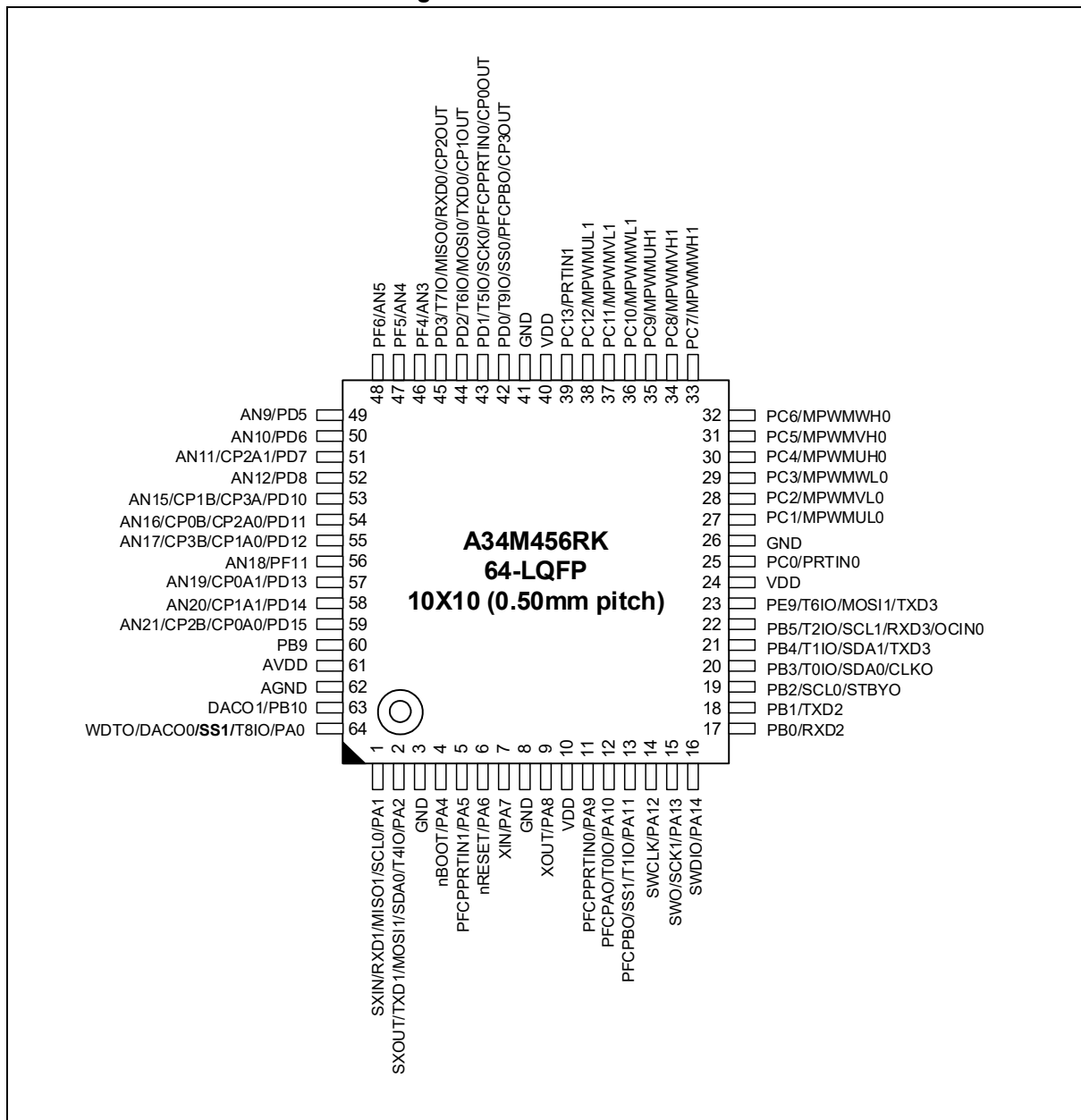
2.1.3 A34M456RL (64-LQFP)

Figure 5. 64-LQFP Pinouts



2.1.4 A34M456RK (64-LQFP)

Figure 6. 64-LQFP Pinouts



2.2 Pin Description

Table 9. Legend and Abbreviations Used in Pin Description

Classification	Description	
Pin name	- The pin name is always the same. - Users can set a function on the pin using the alternate function.	
Classification	Abbreviation	Definition
Pin type	I	Input
	O	Output
	U	Pull-up
	D	Pull-down
	S	Schmitt-Trigger Input Type
	C	CMOS Input Type
	A	Analog
	P	Power
Pin function	Alternate functions	Functions selected through Pn_MR1/2 (PORT n mux1/2 select register) registers

NOTES:

- After a reset, all the pins are configured to function defined by their initial values. The initial value of the pin depends on the package type. This configuration follows the 100-pin standard.
- nBOOT(PA4), nRESET(PA6), SWCLK(PA12), SWDIO(PA14) are the default pull-up pins.
- Do not configure unused pins as floating inputs. (Low output is recommended.)
- After a reset, the internal pull-up for the boot pin is enabled.
- After a reset, the internal pull-up for the serial wire clock (SWCLK) and the serial wire data I/O (SWDIO) are enabled.
- The SWCLK and SWDIO pins should not be switched to other functions while they are being used.
- PA1, PA2, PB2, PB3, PB4, PB5, PE3, PE4 pins are open-drain ports.
- When the PA7 (XIN), PA8 (XOUT), PA2 (SXOUT), and PA1 (SXIN) pins are configured for a function other than a clock, and if the clock is enabled by software, the other functions may not operate normally.

Pin configuration information in Table 10 contains two pairs of power/ground and other dedicated pins. These multi-function pins have up to five selections of functions including GPIO. Configuration including pin ordering can be changed without notice.

Table 10. Pin Description

Pin No.				Pin Name	Type	Description	Remark
100-Pin	80-Pin	64-Pin (RL)	64-Pin (RK)				
1	-	-	-	PE0	IOUS	PORT E Bit 0 Input/Output	
2	1	1	1	PA1	IOUS	PORT A Bit 1 Input/Output	
				SCL0	IO	I2C Channel 0 Output	Open-drain
				MISO0	IO	SPI Channel 0 Master In/Slave Out Signal	
				RXD1	Input	UART Channel 1 RXD Input	
				SXIN	Input	Sub X-TAL Input	
3	2	-		GND	P	GND	
4	3	2	2	PA2	IOUS	PORT A Bit 2 Input/Output	
				SDA0	IO	I2C Channel 0 SDA Input/Output	Open-drain
				MOSI1	IO	SPI Channel 1 Master Out/Slave in Signal	
				TXD1	Output	UART Channel 1 TXD Output	
				SXOUT	Output	Sub X-TAL Output	
5	4	3	3	GND	P	GND	
6	5	4	4	PA4	IOUS	PORT A Bit 4 Input/Output	
				nBoot	Input	Boot Mode Selection Input	Pull-up
7	6	5	5	PA5	IOUS	PORT A Bit 5 Input/Output	
				PFCPPRTIN1	Input	PFCP Protection 1 Input	
8	7	-	-	PE1	IOUS	PORT E Bit 1 Input/Output	
9	8	-	-	PE2	IOUS	PORT E Bit 2 Input/Output	
10	9	6	6	PA6	IOUS	PORT A Bit 6 Input/Output	
				nRESET*	Input	External Reset Input	Pull-up
11	10	7	7	PA7	IOUS	PORT A Bit 7 Input/Output	
				XIN*	IA	External Crystal Oscillator Input	
12	11	8	8	GND	P	GND	
13	12	9	9	PA8	IOUS	PORT A Bit 8 Input/Output	
				XOUT	OA	External Crystal Oscillator Output	
14	13	10	10	VDD	P	VDD	
15	14	11	11	PA9	IOUS	PORT A Bit 9 Input/Output	
				PFCPPRTIN0	Input	PFCP Protection 0 Input Signal	
16	-	-	-	PE3	IOUS	PORT E Bit 3 Input/Output	
				SCL0	IO	I2C Channel 0 Output	Open-drain
17	-	-	-	PE4	IOUS	PORT E Bit 4 Input/Output	
				SDA0	IO	I2C Channel 0 SDA Input/Output	Open-drain

Table 10. Pin Description (continued)

Pin No.				Pin Name	Type	Description	Remark
100-Pin	80-Pin	64-Pin (RL)	64-Pin (RK)				
18	15	12	12	PA10	IOUS	PORT A Bit 10 Input/Output	
				T0IO	IO	Timer 0 Input/Output	
				PFCPAO	IO	PFCPA PWM Output	
19	16	13	13	PA11	IOUS	PORT A Bit 11 Input/Output	
				T1IO	IO	Timer 3 Input/Output	
				SS1	IO	SPI Channel 1 Select Signal Input/Output	
				PFCPBO	IO	PFCPB PWM Output	
20	17	14	14	PA12	IOUS	PORT A Bit 12 Input/Output	
				SWCLK	IO	SWD Clock Input	Pull up
21	18	15	15	PA13	IOUS	PORT A Bit 13 Input/Output	
				SCK1	IO	SPI Channel 1 Clock Input/Output	
				SWO	IO	Serial Wire Output	Output low
22	19	16	16	PA14	IOUS	PORT A Bit 14 Input/Output	
				SWDIO	IOUS	SWD Data Input/Output	Pull up
23	20	-	-	PE5	IOUS	PORT E Bit 5 Input/Output	
				T2IO	IO	Timer 2 Input/Output	
				MOSI1	IO	SPI Channel 1 Master Out/Slave in Signal	
24	-	-	-	PE6	IOUS	PORT E Bit 6 Input/Output	
				T3IO	IO	Timer 3 Input/Output	
				PFCPAO	IO	PFCP A PWM Output	
				MISO1	IO	SPI Channel 1 Master In/Slave Out Signal	
25	-	-	-	PE7	IOUS	PORT E Bit 7 Input/Output	
				T4IO	IO	Timer 4 Input/Output	
				PFCPBO	IO	PFCP B PWM Output	
26	-	-	-	PE8	IOUS	PORT E Bit 8 Input/Output	
				T5IO	IO	Timer 5 Input/Output	
27	21	17	17	PB0	IOUS	PORT B Bit 0 Input/Output	
				RXD2	Input	UART Channel 2 RXD Input	
28	22	18	18	PB1	IOUS	PORT B Bit 1 Input/Output	
				TXD2	Output	UART Channel 2 TXD Output	
29	23	-	-	VDD	P	VDD	
30	24	19	19	PB2	IOUS	PORT B Bit 2 Input/Output	
				SCL0	IO	I2C Channel 0 Output	Open-drain
				STBYO	Output	Power-down Mode Indication Signal	
31	25	-	-	GND	P	GND	
32	26	20	20	PB3	IOUS	PORT B Bit 3 Input/Output	

Table 10. Pin Description (continued)

Pin No.				Pin Name	Type	Description	Remark
100-Pin	80-Pin	64-Pin (RL)	64-Pin (RK)				
				T0IO	IO	Timer 0 Input/Output	
				SDA0	IO	I2C Channel 0 SDA Input/Output	Open-drain
				CLKO	Output	System Clock Output	
33	27	21	21	PB4	IOUS	PORT B Bit 4 Input/Output	
				T1IO	IO	Timer 1 Input/Output	
				SDA1	IO	I2C Channel 1 SDA Input/Output	Open-drain
				TXD3	Output	UART Channel 3 TXD Output	
34	28	22	22	PB5	IOUS	PORT B Bit 5 Input/Output	
				T2IO	IO	Timer 2 Input/Output	
				SCL1	IO	I2C Channel 1 Output	Open-drain
				RXD3	Input	UART Channel 3 RXD Input	
				OCIN0	Input	MPWM 0 Over-Current Input	
35	29	-	23	PE9	IOUS	PORT E Bit 9 Input/Output	
				T6IO	IO	Timer 6 Input/Output	
				MOSI1	IO	SPI Channel 1 Master Out/Slave in Signal	
				TXD3	Output	UART Channel 3 TXD Output	
36	30	-	-	PE10	IOUS	PORT E Bit 10 Input/Output	
				MISO1	IO	SPI Channel 1 Master In/Slave Out Signal	
				RXD3	Input	UART Channel 3 RXD Input	
37	-	-	-	PE11	IOUS	PORT E Bit 11 Input/Output	
				SCK1	IO	SPI Channel 1 Clock Input/Output	
38	31	-	-	PE12	IOUS	PORT E Bit 12 Input/Output	
				SS1	IO	SPI Channel 1 Select Signal Input/Output	
39	-	-	-	PE13	IOUS	PORT E Bit 13 Input/Output	
40	-	-	-	PE14	IOUS	PORT E Bit 14 Input/Output	
				TXD4	Output	UART Channel 4 TXD Output	
41	-	-	-	PE15	IOUS	PORT E Bit 15 Input/Output	
				RXD4	Input	UART Channel 4 RXD Input	
42	32	23	24	VDD	P	VDD	
43	33	24	25	PC0	IOUS	PORT C Bit 0 Input/Output	
				PRTIN0	Input	MPWM 0 Protection Input	
44	34	25	26	GND	P	GND	
45	35	26	27	PC1	IOUS	PORT C Bit 1 Input/Output	
				MPWMUL0	Output	MPWM Channel 0 UL Output	
46	36	27	28	PC2	IOUS	PORT C Bit 2 Input/Output	
				MPWMVL0	Output	MPWM Channel 0 VL Output	
47	37	28	29	PC3	IOUS	PORT C Bit 3 Input/Output	

Table 10. Pin Description (continued)

Pin No.				Pin Name	Type	Description	Remark
100-Pin	80-Pin	64-Pin (RL)	64-Pin (RK)				
				MPWMWL0	Output	MPWM Channel 0 WL Output	
48	38	29	30	PC4	IOUS	PORT C Bit 4 Input/Output	
				MPWMUH0	Output	MPWM Channel 0 UH Output	
49	39	30	31	PC5	IOUS	PORT C Bit 5 Input/Output	
				MPWMVH0	Output	MPWM Channel 0 VH Output	
50	40	31	32	PC6	IOUS	PORT C Bit 6 Input/Output	
				MPWMWH0	Output	MPWM Channel 0 WH Output	
51	41	32	33	PC7	IOUS	PORT C Bit 7 Input/Output	
				MPWMWH1	Output	MPWM Channel 1 WH Output	
52	42	33	34	PC8	IOUS	PORT C Bit 8 Input/Output	
				MPWMVH1	Output	MPWM Channel 1 VH Output	
53	43	34	35	PC9	IOUS	PORT C Bit 9 Input/Output	
				MPWMUH1	Output	MPWM Channel 1 UH Output	
54	44	35	36	PC10	IOUS	PORT C Bit 10 Input/Output	
				MPWMWL1	Output	MPWM Channel 1 WL Output	
55	45	36	37	PC11	IOUS	PORT C Bit 11 Input/Output	
				MPWMVL1	Output	MPWM Channel 1 VL Output	
56	46	37	38	PC12	IOUS	PORT C Bit 12 Input/Output	
				MPWMUL1	Output	MPWM Channel 1 UH Output	
57	47	38	39	PC13	IOUS	PORT C Bit 13 Input/Output	
				PRTIN1	Input	MPWM 1 Protection Input	
58	-	-	-	PF0	IOUS	PORT F Bit 0 Input/Output	
				PFCPPRTIN1	Input	PFCP Protection 1 Input	
59	-	-	-	PF1	IOUS	PORT F Bit 1 Input/Output	
				T7IO	IO	Timer 7 Input/Output	
60	48	39	40	VDD	P	VDD	
61	49	40	-	PC14	IOUS	PORT C Bit 14 Input/Output	
				T8IO	IO	Timer 8 Input/Output	
				OCIN1	Input	MPWM 1 Over-Current Input	
				PFCPAO	IO	PFCPA PWM Output	
62	50	41	41	GND	P	GND	
63	51	42	42	PD0	IOUS	PORT D Bit 0 Input/Output	
				T9IO	IO	Timer 9 Input/Output	
				SS0	IO	SPI Channel 0 Select Signal Input/Output	
				PFCPBO	IO	PFCPB PWM Output	
				CP3OUT	Output	Comparator 3 Output	
64	52	43	43	PD1	IOUS	PORT D Bit 1 Input/Output	

Table 10. Pin Description (continued)

Pin No.				Pin Name	Type	Description	Remark
100-Pin	80-Pin	64-Pin (RL)	64-Pin (RK)				
				T5IO	IO	Timer 5 Input/Output	
				SCK0	IO	SPI Channel 0 Clock Input/Output	
				PFCPPRTIN0	Input	PFCP Protection 0 Input	
				CP0OUT	Output	Comparator 0 Output	
65	53	44	44	PD2	IOUS	PORT D Bit 2 Input/Output	
				T6IO	IO	Timer 6 Input/Output	
				MOSI0	IO	SPI Channel 0 Master Out/Slave in Signal	
				TXD0	Output	UART Channel 0 TXD Output	
				CP1OUT	Output	Comparator 1 Output	
66	54	45	45	PD3	IOUS	PORT D Bit 3 Input/Output	
				T7IO	IO	Timer 7 Input/Output	
				MISO0	IO	SPI Channel 0 Master In/Slave Out Signal	
				RXD0	Input	UART Channel 0 RXD Input	
				CP2OUT	Output	Comparator 2 Output	
67	55	46	-	PD4	IOUS	PORT D Bit 4 Input/Output	
				AN0*	Input	Analog Input 0	
68	-	-	-	PF2	IOUS	PORT F Bit 2 Input/Output	
				AN1*	Input	Analog Input 1	
69	56	-	-	PF3	IOUS	PORT F Bit 3 Input/Output	
				AN2*	Input	Analog Input 2	
70	57	-	46	PF4	IOUS	PORT F Bit 4 Input/Output	
				AN3*	Input	Analog Input 3	
71	58	47	-	PB6	IOUS	PORT B Bit 6 Input/Output	
72	-	-	-	PB7	IOUS	PORT B Bit 7 Input/Output	
73	-	48	-	PB8	IOUS	PORT B Bit 8 Input/Output	
74	59	-	47	PF5	IOUS	PORT F Bit 5 Input/Output	
				AN4*	Input	Analog Input 4	
75	60	-	48	PF6	IOUS	PORT F Bit 6 Input/Output	
				AN5*	Input	Analog Input 5	
76	-	-	-	PF7	IOUS	PORT F Bit 7 Input/Output	
				AN6*	Input	Analog Input 6	
77	-	-	-	PF8	IOUS	PORT F Bit 8 Input/Output	
				AN7*	Input	Analog Input 7	
78	61	-	-	PF9	IOUS	PORT F Bit 9 Input/Output	
				AN8*	Input	Analog Input 8	
79	62	49	49	PD5	IOUS	PORT D Bit 5 Input/Output	
				AN9*	Input	Analog Input 9	

Table 10. Pin Description (continued)

Pin No.				Pin Name	Type	Description	Remark
100-Pin	80-Pin	64-Pin (RL)	64-Pin (RK)				
80	63	50	50	PD6	IOUS	PORT D Bit 6 Input/Output	
				AN10*	Input	Analog Input 10	
81	64	51	51	PD7	IOUS	PORT D Bit 7 Input/Output	
				CP2A1	Input	Comparator 2 A1 Input	
				AN11*	Input	Analog Input 11	
82	65	52	52	PD8	IOUS	PORT D Bit 8 Input/Output	
				AN12*	Input	Analog Input 12	
83	66	53	-	PD9	IOUS	PORT D Bit 9 Input/Output	
				AN13*	Input	Analog Input 13	
84	67	-	-	PF10	IOUS	PORT F Bit 10 Input/Output	
				AN14*	Input	Analog Input 14	
85	68	54	53	PD10	IOUS	PORT D Bit 10 Input/Output	
				CP3A	Input	Comparator 3 A Input	
				CP1B	Input	Comparator 1 B Input	
				AN15*	Input	Analog Input 15	
86	69	55	54	PD11	IOUS	PORT D Bit 11 Input/Output	
				CP2A0	Input	Comparator 2 A0 Input	
				CP0B	Input	Comparator 0 B Input	
				AN16*	Input	Analog Input 16	
87	70	56	55	PD12	IOUS	PORT D Bit 12 Input/Output	
				CP1A0	Input	Comparator 1 A0 Input	
				CP0B	Input	Comparator 3 B Input	
				AN17*	Input	Analog Input 17	
88	71	-	56	PF11	IOUS	PORT F Bit 11 Input/Output	
				AN18*	Input	Analog Input 18	
89	72	57	57	PD13	IOUS	PORT D Bit 13 Input/Output	
				CP0A1	Input	Comparator 0 A1 Input	
				AN19*	Input	Analog Input 19	
90	73	58	58	PD14	IOUS	PORT D Bit 14 Input/Output	
				CP1A1	Input	Comparator 1 A1 Input	
				AN20*	Input	Analog Input 20	
91	74	59	59	PD15	IOUS	PORT D Bit 15 Input/Output	
				CP0A0	Input	Comparator 0 A0 Input	
				CP2B	Input	Comparator 2 B Input	
				AN21*	Input	Analog Input 21	
92	75	60	60	PB9	IOUS	PORT B Bit 9 Input/Output	
93	76	61	61	AVDD	P	Analog VDD	

Table 10. Pin Description (continued)

Pin No.				Pin Name	Type	Description	Remark
100-Pin	80-Pin	64-Pin (RL)	64-Pin (RK)				
94	77	62	62	AGND	P	Analog GND	
95	78	63	63	PB10	IOUS	PORT B Bit 10 Input/Output	
				DACO1	Output	DA1 Convertor Output	
96	-	-	-	PF12	IOUS	PORT F Bit 12 Input/Output	
				SCK1	IO	SPI Channel 1 Clock Input/Output	
97	-	-	-	PF13	IOUS	PORT F Bit 13 Input/Output	
				MOSI1	IO	SPI Channel 1 Master Out/Slave in Signal	
				TXD5	Output	UART Channel 5 TXD Output	
98	-	-	-	PF14	IOUS	PORT F Bit 14 Input/Output	
				MISO1	IO	SPI Channel 1 Master In/Slave Out Signal	
				RXD5	Input	UART Channel 5 RXD Input	
99	79	64	64	PA0	IOUS	PORT A Bit 0 Input/Output	
				T8IO	IO	Timer 8 Input/Output	
				SS1	IO	SPI Channel 1 Select Signal Input/Output	
				DACO0	Output	DA0 Convertor Output	
				WDTO	Output	WDT Output	
100	80	-	-	PF15	IOUS	PORT F Bit 15 Input/Output	
				T9IO	IO	Timer 9 Input/Output	

NOTES:

1. I = Input, O = Output, U = Pull-up, D = Pull-down, S = Schmitt-Trigger Input Type, C = CMOS Input Type, A = Analog, P = Power
2. “*” means ‘selected pin function after reset condition’.
3. nBOOT, nRESET, PA14 (SWDIO), PA12 (SWCLK), nTRST and nRESET are the default pull-up pins.
4. Do not configure unused pins as floating inputs.
5. After a reset, the internal pull-up for the boot pin is enabled.
6. After a reset, the internal pull-up for the serial wire clock (SWCLK) and the serial wire data I/O (SWDIO) is enabled.
7. The SWCLK and SWDIO pins should not be switched to other functions while they are being used.

2.3 Alternate Function Pins

GPIO pins have alternate functions as described in Table 11.

Table 11. GPIO Alternate Function ⁽¹⁾

Pin Name	Alternate Function					
	AF0	AF1	AF2	AF3	AF4	AF7
PA0	PA0	SS1	T8IO	WDTO		DAC00*
PA1	PA1	MISO1	SCL0	RXD1		SXIN*
PA2	PA2	MOSI1	SDA0	TXD1		SXOUT*
PA3	PA3					*
PA4	PA4			nBOOT*		*
PA5	PA5			PFCPPRTIN1		*
PA6	PA6			nRESET		*
PA7	PA7					XIN*
PA8	PA8					XOUT*
PA9	PA9			PFCPPRTIN0		*
PA10	PA10		T0IO	PFCPAO		*
PA11	PA11	SS1	T1IO	PFCPBO		*
PA12	PA12			SWCLK*		*
PA13	PA13	SCK1		SWO *		*
PA14	PA14			SWDIO*		*
PA15	PA15					*
PB0	PB0	RXD2				*
PB1	PB1	TXD2				*
PB2	PB2	SCL0		STBYO		*
PB3	PB3	SDA0	T0IO	CLKO		*
PB4	PB4	TXD3	T1IO	SDA1		*
PB5	PB5	RXD3	T2IO	SCL1	OCIN0	*
PB6	PB6					*
PB7	PB7					*
PB8	PB8					*
PB9	PB9					*
PB10	PB10					DAC01*
PB11	PB11					*
PB12	PB12					*
PB13	PB13					*
PB14	PB14					*
PB15	PB15					*
PC0	PC0			PRTIN0		*
PC1	PC1			MPWMUL0		*
PC2	PC2			MPWMVL0		*
PC3	PC3			MPWMWL0		*
PC4	PC4			MPWMUH0		*
PC5	PC5			MPWMVH0		*
PC6	PC6			MPWMWH0		*
PC7	PC7			MPWMWH1		*

Table 11. GPIO Alternate Function ⁽¹⁾ (continued)

Pin Name	Alternate Function					
	AF0	AF1	AF2	AF3	AF4	AF7
PC8	PC8			MPWMVH1		*
PC9	PC9			MPWMUH1		*
PC10	PC10			MPWMWL1		*
PC11	PC11			MPWMVL1		*
PC12	PC12			MPWMUL1		*
PC13	PC13			PRTIN1		*
PC14	PC14		T8IO	PFCPAO	OCIN1	*
PC15	PC15					*
D0	PD0	SS0	T9IO	PFCPBO	CP3OUT	*
PD1	PD1	SCK0	T5IO	PFCPPRTIN0	CP0OUT	*
PD2	PD2	MOSI0	T6IO	TXD0	CP1OUT	*
PD3	PD3	MISO0	T7IO	RXD0	CP2OUT	*
PD4	PD4					*AN0
PD5	PD5					*AN9
PD6	PD6					*AN10
PD7	PD7					*AN11/CP2A1
PD8	PD8					*AN12
PD9	PD9					*AN13
PD10	PD10					*AN15/CP3A/CP1B
PD11	PD11					*AN16/CP2A0/CP0B
PD12	PD12					*AN17/CP1A0/CP3B
PD13	PD13					*AN19/CP0A1
PD14	PD14					*AN20/CP1A1
PD15	PD15					*AN21/CP0A0/CP2B
PE0	PE0					*
PE1	PE1					*
PE2	PE2					*
PE3	PE3	SCL0				*
PE4	PE4	SDA0				*
PE5	PE5	MOSI1	T2IO			*
PE6	PE6	MISO1	T3IO	PFCPAO		*
PE7	PE7		T4IO	PFCPBO		*
PE8	PE8		T5IO			*
PE9	PE9	MOSI1	T6IO	TXD3		*
PE10	PE10	MISO1		RXD3		*
PE11	PE11	SCK1				*
PE12	PE12	SS1				*
PE13	PE13					*
PE14	PE14	TXD4				*
PE15	PE15	RXD4				*

Table 11. GPIO Alternate Function ⁽¹⁾ (continued)

Pin Name	Alternate Function					
	AF0	AF1	AF2	AF3	AF4	AF7
PF0	PF0			PFCPPRTIN1		*
PF1	PF1		T7IO			*
PF2	PF2					AN1*
PF3	PF3					AN2*
PF4	PF4					AN3*
PF5	PF5					AN4*
PF6	PF6					AN5*
PF7	PF7					AN6*
PF8	PF8					AN7*
PF9	PF9					AN8*
PF10	PF10					AN14*
PF11	PF11					AN18
PF12	PF12	SCK1				*
PF13	PF13	MOSI1	TXD5			*
PF14	PF14	MISO1	RXD5			*
PF15	PF15		T9IO			*

NOTES:

1. It means 'selected pin function after reset condition'. (The initial value of the pin is different depending on the package type)
2. Unused pins are set to output from firmware (low output is recommended).

3. Electrical Characteristics

3.1 Parameter Conditions

Unless otherwise specified, all voltages are referenced to GND.

3.1.1 Minimum and Maximum Values

Unless otherwise specified, our production tests guarantee the minimum and maximum values of the device under the worst-case conditions of ambient temperature, supply voltage, and frequency.

Data based on characterization result, design simulation, and/or technical characteristics are not tested in production but indicated in the table footnotes.

3.1.2 Typical Values

Unless otherwise specified, typical data are based on the conditions of $T_A = 25^\circ\text{C}$ and $V_{DD} = AV_{DD} = 5.0\text{ V}$. The typical data are provided only as design recommendations and are not tested.

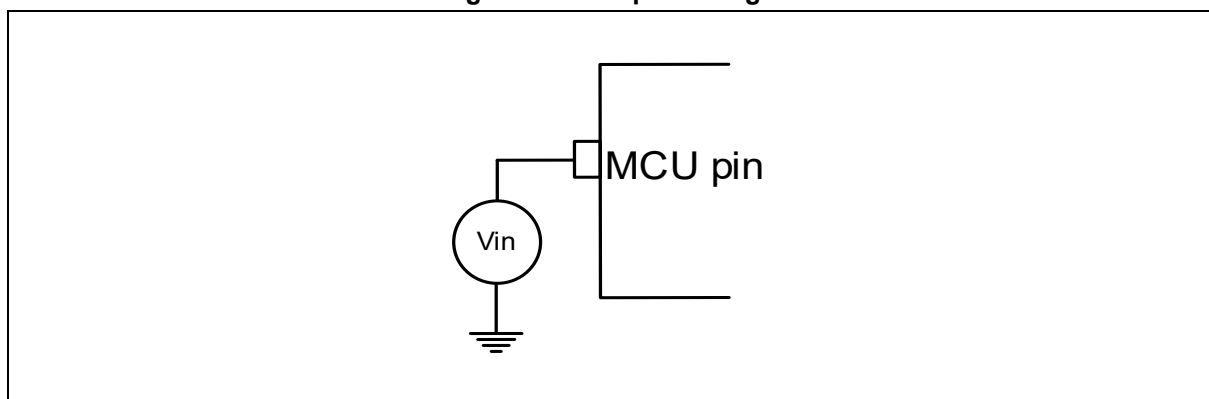
3.1.3 Typical Curves

Unless otherwise specified, all typical curves are provided only as design recommendations and are not tested.

3.1.4 Pin Input Voltage

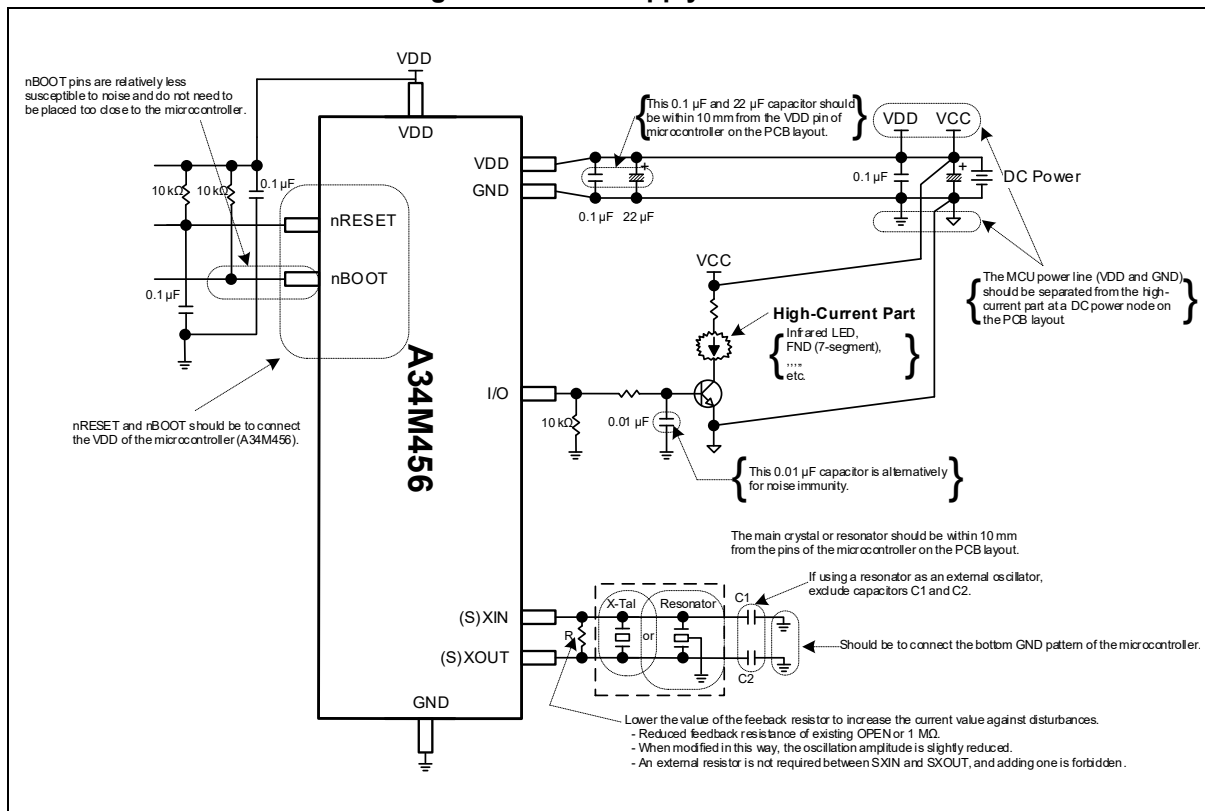
The input voltage measurement on a pin of the device is described in Figure 7.

Figure 7. Pin Input Voltage



3.1.5 Power Supply Scheme

Figure 8. Power Supply Scheme

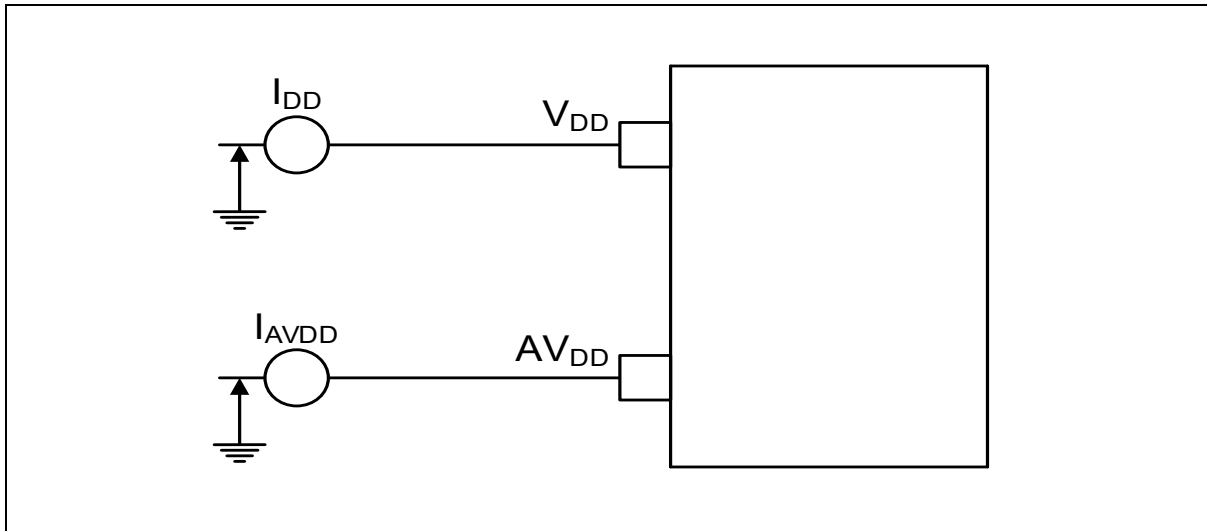


NOTE:

- Each power supply pair (VDD/GND etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

3.1.6 Current Consumption Measurement

Figure 9. Current Consumption Measurement



NOTE:

1. The I_{DD} and I_{AVDD} parameters represent the microcontroller's total consumption including the current supplying V_{DD} and AV_{DD} .

3.2 Absolute Maximum Ratings

Exceeding stresses specified in the Table 12 for voltage characteristics, Table 13 for current characteristics, or Table 14 for thermal characteristics may result in permanent damage to the device. The values listed in the tables are stress ratings only and do not imply that the device will function properly under these conditions. Prolonged exposure to these maximum rating conditions may impact on the reliability of the device. It is important to operate the device within its specified maximum ratings to ensure reliable performance.

Table 12. Voltage Characteristics

Symbol	Ratings	Min.	Max.	Unit
VDD-GND ⁽¹⁾	External main supply voltage (including V _{DD} , AV _{DD})	-0.5	6.0	V
V _I ⁽²⁾	Input voltage on I/O	-0.5	Max. (V _{DD} , AV _{DD}) + 0.5	V
V _O	Output voltage on I/O	-0.5	Max. (V _{DD} , AV _{DD}) + 0.5	V

NOTES:

1. All main power (VDD, AVDD) and ground (GND, AGND) pins must always be connected to the external power supply, in the permitted range.
2. V_I maximum must always be respected.

Table 13. Current Characteristics

Symbol	Ratings	Max.	Unit
I _{IO(PIN)}	Output current sunk by any I/O	20	mA
	Output current sourced by any I/O and control pin	-10	mA
$\Sigma I_{OL(PIN)}$ ⁽¹⁾	PA0 to PA1, PB6 to PB10, PD5 to PD15, PE0, PF5 to PF15	90	mA
	Ports other than those above	117	mA
$\Sigma I_{OH(PIN)}$ ⁽¹⁾	PA0 to PA1, PB6 to PB10, PD5 to PD15, PE0, PF5 to PF15	-45	mA
	Ports other than those above	-54	mA
I _{IH}	Input high leakage current	1	μA
I _{IL}	Input low leakage current	1	μA
P _T	Total power dissipation	600	mW

NOTE:

1. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.

Table 14. Thermal Characteristics

Symbol	Ratings	Value	Unit
T _{OP}	Operating temperature	-40 to +105	°C
T _{STG}	Storage temperature range	-55 to +125	°C
T _J	Maximum junction temperature	+125	°C

3.3 Operating Condition

3.3.1 General Operating Condition

Table 15. General Operating Condition

(Temperature: -40°C to +105°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V _{DD}	Supply voltage	-	2.7 ⁽¹⁾	-	5.5	V
AV _{DD}	Analog supply voltage	ADC used	2.7	-	5.5	V
F	Operating frequency	HSE	4	-	16	MHz
		LSE	-	32.768	-	kHz
		HSI	7.92	8.00	8.08	MHz
		LSI	350	500	650	kHz
V _{IN}	I/O input voltage	5 V I/O	-0.3	-	V _{DD}	V
T _A	Ambient temperature	-	-40	-	105	°C
T _J	Junction temperature range	-	-40	-	125	°C

NOTE:

1. When RESET is released, functionality is guaranteed down to V_{LVR} Min.

3.3.2 Power-On Reset Characteristics

Table 16. POR Electrical Characteristics

(Temperature: -40°C to +105°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I _{DD}	Operating current	-	-	5.0	10	μA
V _{set}	POR set level	-	1.80	1.94	2.08	V
t _R	V _{DD} voltage rising time	-	0.02	-	20	ms/V
t _F	V _{DD} voltage falling time	-	0.4	-	20	ms/V
V _{reset}	POR reset level	-	1.35	1.48	1.60	V

3.3.3 Operating Condition at Power-Up/Power-Down

The parameters in Table 17 are derived from tests performed under the ambient temperature conditions summarized in Table 15.

Table 17. Operating Condition at Power-Up/Power-Down

(Temperature: -40°C to +105°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t _{VDD}	V _{DD} rise time rate	-	0.02	-	20	ms/V
	V _{DD} fall time rate	-	0.4	-	20	ms/V

3.3.4 Embedded Reset and Power Control Block Characteristics (LVR, LVI)

The parameters in Table 18 and Table 19 are derived from tests performed under the ambient temperature conditions summarized in Table 15.

Table 18. Low Voltage Reset Characteristics

(Temperature: -40°C to +105°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VDD	Operating voltage	-	0.8	5.0	5.5	V
V _{LVR0_F}	Detection level	Falling voltage	-	-	-	V
V _{LVR1_F}			-	-	-	
V _{LVR2_F}			-	-	-	
V _{LVR3_F}			-	-	-	
V _{LVR4_F}			-	-	-	
V _{LVR5_F}			-	-	-	
V _{LVR6_F}			1.80 V	2.00 V	2.20 V	
V _{LVR7_F}			1.92 V	2.13 V	2.34 V	
V _{LVR8_F}			2.03 V	2.26 V	2.49 V	
V _{LVR9_F}			2.16 V	2.40 V	2.64 V	
V _{LVR10_F}			2.30 V	2.56 V	2.82 V	
V _{LVR11_F}			2.48 V	2.75 V	3.03 V	
V _{LVR12_F}			2.66 V	2.96 V	3.26 V	
V _{LVR13_F}			2.88 V	3.20 V	3.52 V	
V _{LVR14_F}			3.15 V	3.50 V	3.85 V	
V _{LVR15_F}			3.46 V	3.85 V	4.24 V	
V _{LVR0_R}	Detection level	Rising voltage	-	-	-	V
V _{LVR1_R}			-	-	-	
V _{LVR2_R}			-	-	-	
V _{LVR3_R}			-	-	-	
V _{LVR4_R}			-	-	-	
V _{LVR5_R}			-	-	-	
V _{LVR6_R}			2.08 V	2.20 V	2.42 V	
V _{LVR7_R}			2.20 V	2.32 V	2.54 V	
V _{LVR8_R}			2.34 V	2.46 V	2.68 V	
V _{LVR9_R}			2.49 V	2.61 V	2.83 V	
V _{LVR10_R}			2.67 V	2.79 V	3.01 V	
V _{LVR11_R}			2.87 V	2.99 V	3.21 V	
V _{LVR12_R}			3.10 V	3.22 V	3.44 V	
V _{LVR13_R}			3.36 V	3.48 V	3.70 V	
V _{LVR14_R}			3.68 V	3.80 V	4.02 V	
V _{LVR15_R}			4.06 V	4.18 V	4.40 V	
-	Hysteresis	-	-	200	-	mV
-	Noise cancelling time	-	-	3	-	μs
I _{DD}	Operation current	-	-	3.5	5	μA
I _{DD, STOP}	Operation current (STOP)	-	-	3	125	nA

Table 19. Low Voltage Indicator Characteristics

(Temperature: -40°C to +105°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VDD	Operating voltage	-	0.8	5.0	5.5	V
V _{LVI0_F}	Detection level	T _A = -40°C to +105°C, Falling voltage	-	-	-	V
V _{LVI1_F}			-	-	-	
V _{LVI2_F}			-	-	-	
V _{LVI3_F}			-	-	-	
V _{LVI4_F}			-	-	-	
V _{LVI5_F}			-	-	-	
V _{LVI6_F}			1.80 V	2.00 V	2.20 V	
V _{LVI7_F}			1.92 V	2.13 V	2.34 V	
V _{LVI8_F}			2.03 V	2.26 V	2.49 V	
V _{LVI9_F}			2.16 V	2.40 V	2.64 V	
V _{LVI10_F}			2.30 V	2.56 V	2.82 V	
V _{LVI11_F}			2.48 V	2.75 V	3.03 V	
V _{LVI12_F}			2.66 V	2.96 V	3.26 V	
V _{LVI13_F}			2.88 V	3.20 V	3.52 V	
V _{LVI14_F}			3.15 V	3.50 V	3.85 V	
V _{LVI15_F}			3.47 V	3.85 V	4.24 V	
V _{LVI0_R}	Detection level	T _A = -40°C to +105°C, Rising voltage	-	-	-	V
V _{LVI1_R}			-	-	-	
V _{LVI2_R}			-	-	-	
V _{LVI3_R}			-	-	-	
V _{LVI4_R}			-	-	-	
V _{LVI5_R}			-	-	-	
V _{LVI6_R}			2.04 V	2.20 V	2.42 V	
V _{LVI7_R}			2.09 V	2.32 V	2.55 V	
V _{LVI8_R}			2.21 V	2.46 V	2.71 V	
V _{LVI9_R}			2.35 V	2.61 V	2.87 V	
V _{LVI10_R}			2.51 V	2.79 V	3.07 V	
V _{LVI11_R}			2.69 V	2.99 V	3.29 V	
V _{LVI12_R}			2.90 V	3.22 V	3.54 V	
V _{LVI13_R}			3.13 V	3.48 V	3.83 V	
V _{LVI14_R}			3.42 V	3.80 V	4.18 V	
V _{LVI15_R}			3.76 V	4.18 V	4.60 V	
-	Hysteresis	-	-	200	-	mV
-	Noise cancelling time	-	-	3	-	us
I _{DD}	Operation current	-	-	3.5	5	μA
I _{DD, STOP}	Operation current (STOP)	-	-	3	125	nA

3.3.5 Embedded Voltage Reference

Table 20. Embedded Internal Voltage Reference ⁽¹⁾

(Temperature: -40°C to +105°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V _{REFINT}	Internal reference voltage	-40°C ≤ T ≤ +105°C	0.95	1.00	1.05	V

NOTES:

1. The shortest sampling time is determined in the application by multiple iterations.
2. Guaranteed by design.

3.3.6 Supply Current Characteristics

The amount of current consumed by the device is determined by various factors and parameters, including but not limited to the operating voltage, ambient temperature, load on I/O pins, software configuration, operating frequency, switching rate of I/O pins, location of the program in memory, and the binary code being executed.

The current consumption is measured under the conditions specified in Table 21.

3.3.6.1 Supply Current Consumption

Table 21. Supply Current Characteristics

(Temperature: -40°C to +105°C)

Symbol	Operation Mode	Condition					Voltage Scaling	Typ.	Max.	Unit
		LSI	HSI	HSE (8 MHz)	LSE (32.768 kHz)	f _{MCLK}				
I _{DD_RUN} (RUN)	Normal operation	RUN	RUN	RUN	RUN	f _{LSI}	5.0 V	12	-	mA
		RUN	RUN	RUN	RUN	f _{HSI}	5.0 V	4.5	-	
		RUN	RUN	RUN	RUN	f _{HSE}	5.0 V	4.5	-	
		RUN	RUN	RUN	RUN	f _{LSE}	5.0 V	1.5	-	
I _{DD_SLEEP} (SLEEP)	SLEEP ⁽¹⁾	RUN	STOP	STOP	STOP	f _{LSI}	5.0 V	7	-	mA
		STOP	RUN	STOP	STOP	f _{HSI}	5.0 V	4.5	-	
		STOP	STOP	RUN	STOP	f _{HSE}	5.0 V	4.5	-	
		STOP	STOP	STOP	RUN	f _{LSE}	5.0 V	1.4	-	
I _{DD_STOP2} (STOP 2)	DEEP-SLEEP ⁽¹⁾⁽²⁾	VDC (STOP), LVD (RUN)					5.0 V	500		μA
		VDC (STOP), LVD (STOP)					5.0 V	490		

NOTES:

1. All peripherals are off.
2. In DEEP-SLEEP mode, all clocks are disabled.

3.3.6.2 I/O System Current Consumption

The current consumption in the I/O system is due to the two components, Static and Dynamic.

3.3.6.3 I/O Static Current Consumption

All I/O pins used as inputs with Pull-ups cause current consumption when the pins remain Low from the outside. This current consumption value can be calculated simply using the Pull-up/Pull-down resistor value provided in the I/O port characteristics.

To estimate the current consumption at the output pins, users need to consider external Pull-downs or external load.

Additional I/O current consumption can be caused due to the I/Os configured as inputs if the medium voltage level is applied externally. This current is consumed by the input Schmitt trigger circuit used to tell the input value. Unless the application requires a specific configuration, users can prevent this supply current consumption by configuring the I/Os in analog mode instead of using the Schmitt circuit.

Specifically, input pins of the ADC, OPAMP, and CMP must be configured as analog inputs.

3.3.6.4 I/O Dynamic Current Consumption

The I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin.

3.3.7 External Clock Source Characteristics

3.3.7.1 High-Speed External Clock Generated from Crystal/Ceramic Resonator

A high-speed external clock (HSE) can be supplied with crystal/ceramic resonator oscillators in the range of 4 to 16 MHz. All information provided in this section is based on the design simulation results obtained by the typical external components specified in Table 22.

To minimize the outputs in the application, the resonator and load capacitor must be placed as close to the oscillator pin as possible.

For more information on the distortion and stabilization time, and the resonator characteristics (frequency, package, and accuracy), contact the manufacturer of the crystal resonator.

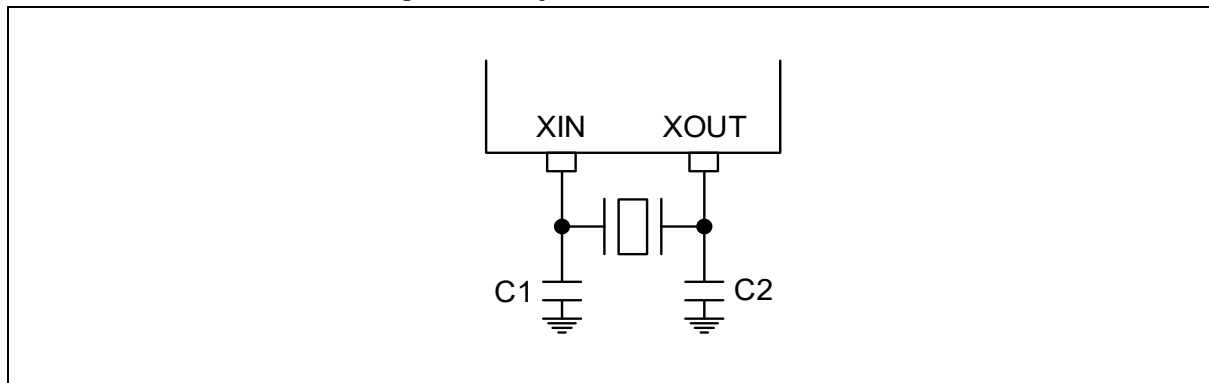
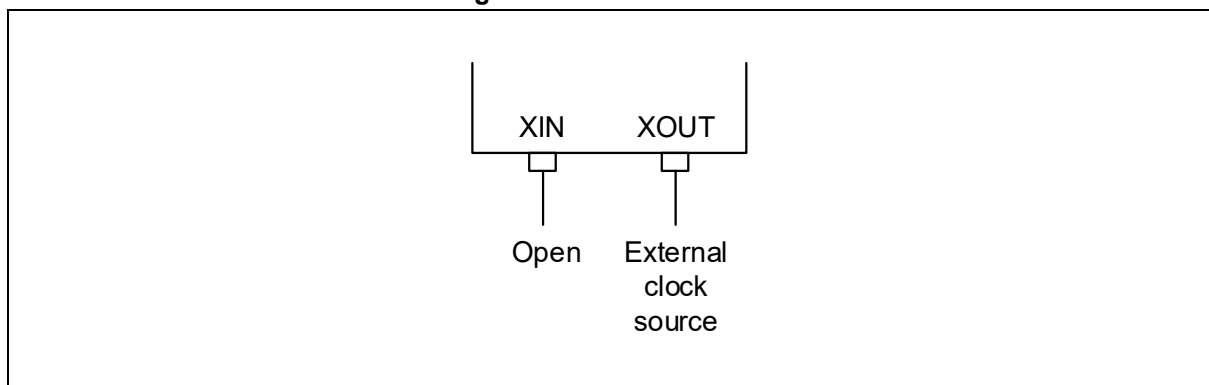
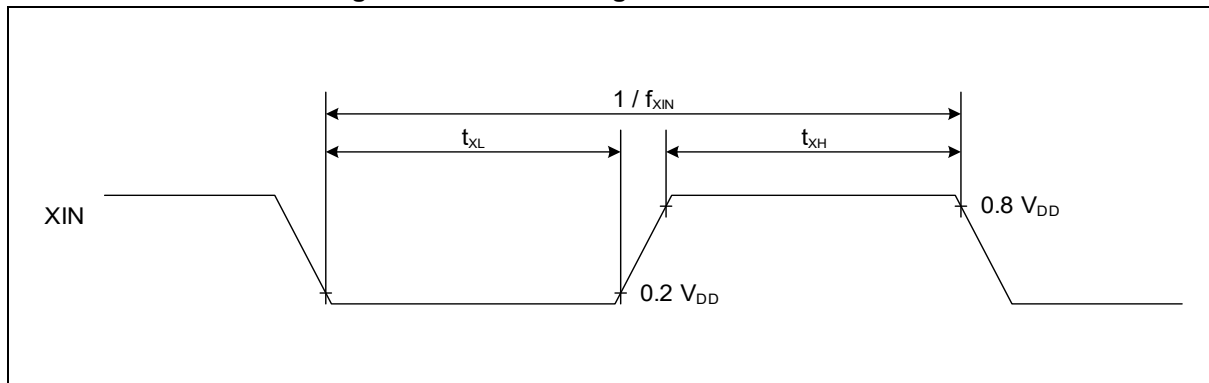
Table 22. HSE Oscillator Characteristics ⁽¹⁾

(Temperature: -40°C to +105°C)

Symbol	Parameter	Conditions ⁽²⁾	Min.	Typ.	Max.	Unit
V _{DD}	Operating voltage	-	2.7	5.0	5.5	V
I _{DD(HSE)}	HSE current consumption	-	-	-	2.5	mA
I _{STOP}	Power down current	-	-	1	60	nA
f _{OSC_IN}	Oscillator frequency	-	4	8	16	MHz
f _{OUT}	Output Frequency	V _{DD} ≥ 2.7 V ⁽⁴⁾⁽⁵⁾⁽⁶⁾⁽⁷⁾	4	-	16	MHz
V _{IL}	Crystal input (low)	-	-	-	0.2 V _{DD}	V
V _{IH}	Crystal input (high)	-	0.8 V _{DD}	-	-	V
V _{OL}	Crystal out (low)	-	-	-	0.2 V _{DD}	V
V _{OH}	Crystal out (high)	-	0.8 V _{DD}	-	-	V
C _L	External Load Capacitor	1 MHz < f _{OUT} ≤ 4 MHz	18	24	30	pF
		4 MHz < f _{OUT} ≤ 12 MHz	10	18	26	pF
		12 MHz < f _{OUT} ≤ 16 MHz	7	15	22	pF
R _F	Feedback resistor	V _{DD} = 5 V	0.7	1.0	1.3	MΩ
t _{SU(HSE)} ⁽³⁾	Startup time	-	-	1	-	ms

NOTES:

1. Guaranteed by design.
2. Resonator characteristics are given by the crystal/ceramic resonator manufacturer.
3. t_{SU(HSE)} is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator, and it can vary significantly with the crystal manufacturer.
4. HSEISEL = 0x3, HSENFSEL = 0x3
5. HSEISEL = 0x2, HSENFSEL = 0x2
6. HSEISEL = 0x1, HSENFSEL = 0x1
7. HSEISEL = 0x0, HSENFSEL = 0x0

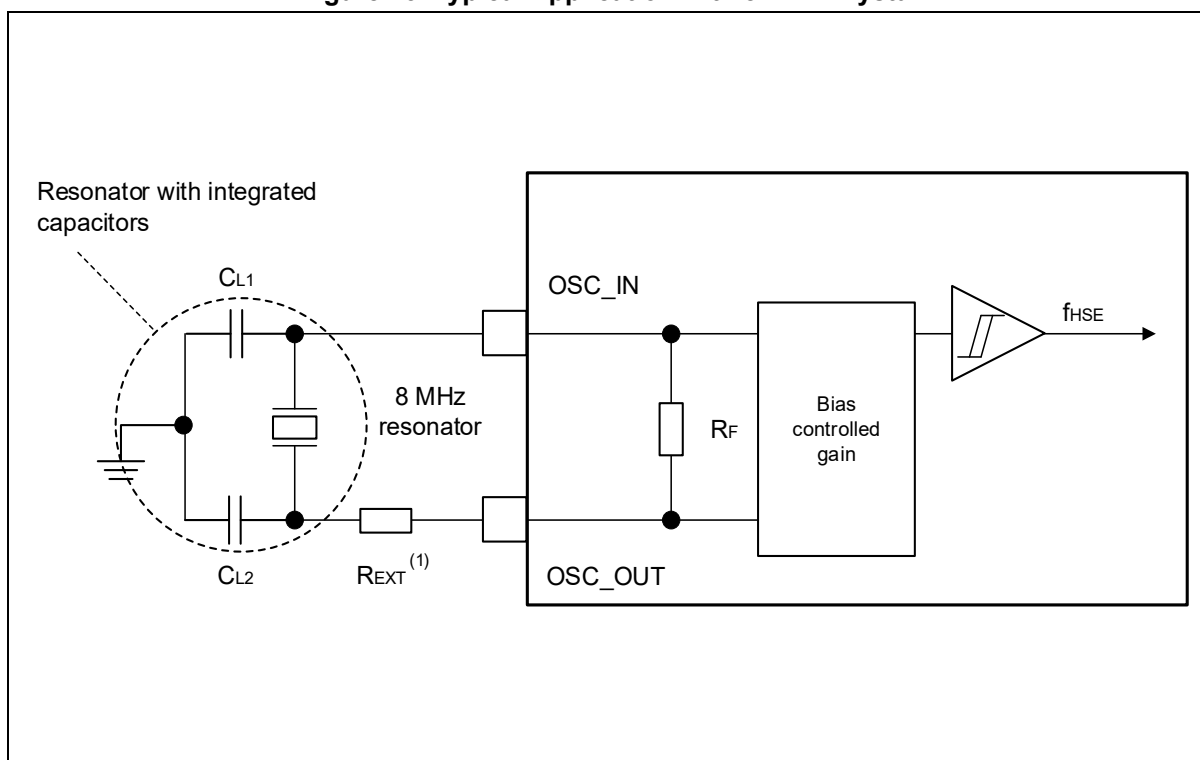
Figure 10. Crystal/Ceramic Oscillator**Figure 11. External Clock****Figure 12. Clock Timing Measurement at XIN**

It is recommended to use high-quality external ceramic capacitors designed for high-frequency applications and selected to match the requirements of the crystal or resonator. The capacitance of the C_{L1} and C_{L2} capacitors should be between 5 pF to 20 pF.

The C_{L1} and C_{L2} capacitors are usually the same size, and the crystal manufacturer typically specifies a load capacitance that is the series combination of both capacitors. However, the capacitance of the printed circuit board (PCB) and the microcontroller's pin should also be considered, which must be included in the calculation of the overall capacitance. A rough estimate of the combined pin and board capacitance is around 10 pF, which can be used to size C_{L1} and C_{L2} appropriately.

Figure 13 shows a circuit diagram of a typical application with an 8 MHz crystal.

Figure 13. Typical Application with 8 MHz Crystal



3.3.7.2 Low-Speed External Clock Generated from Crystal Resonator

The low-speed external (LSE) clock can be generated using a crystal/ceramic resonator oscillator with 32.768 kHz. The information provided in this paragraph is based on characterization results obtained using typical external components listed in Table 23.

To minimize output distortion and startup stabilization time, it is recommended that the resonator and load capacitors be placed as close as possible to the oscillator pins in the application.

It is advisable to consult the crystal resonator manufacturer for further information on resonator characteristics such as frequency, package, and accuracy.

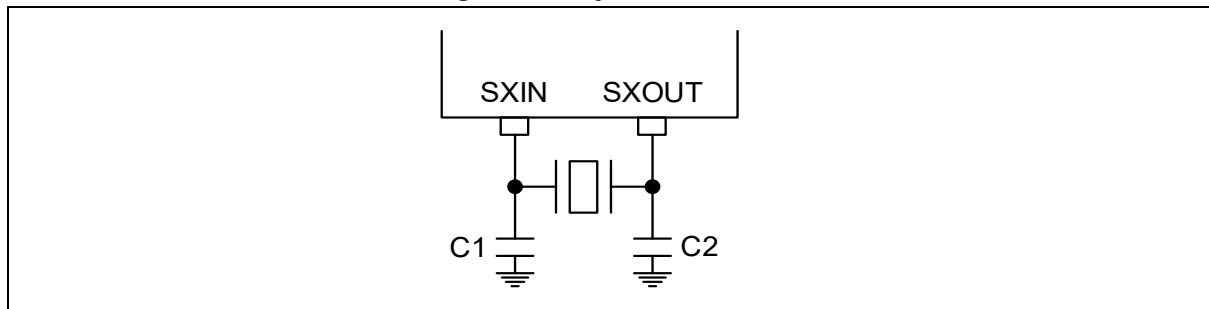
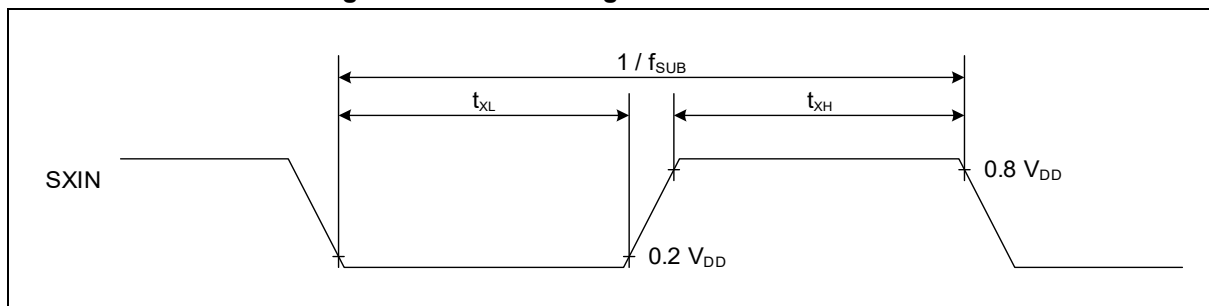
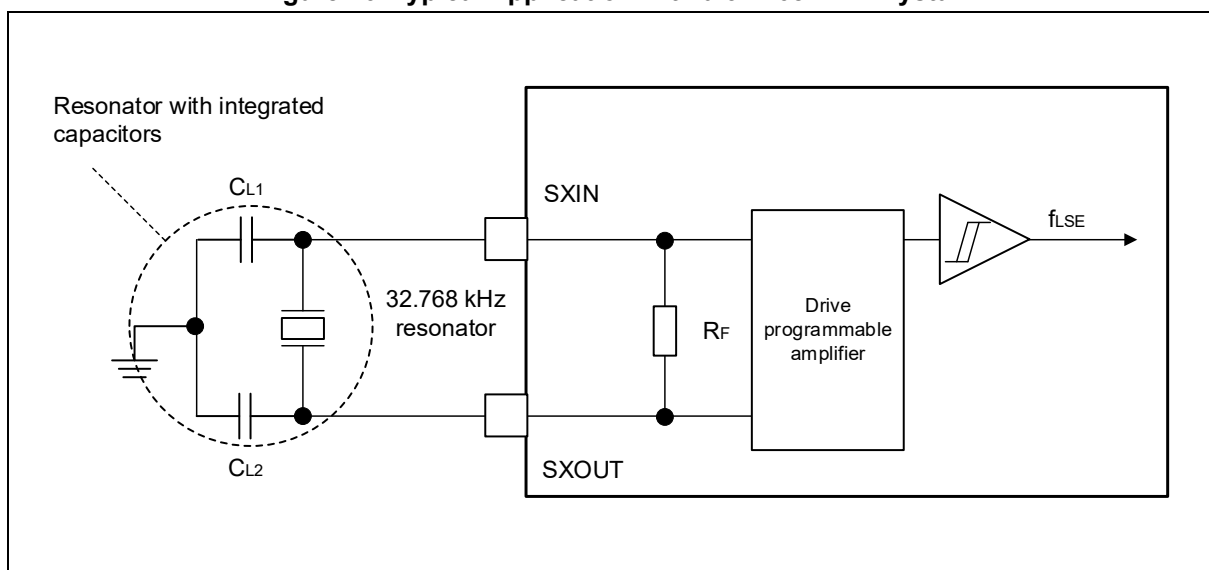
Table 23. LSE Oscillator Characteristics ⁽¹⁾ ($f_{LSE} = 32.768$ kHz)

(Temperature: -40°C to +105°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating voltage	-	2.7	5.0	5.5	V
$I_{DD(LSE)}$	LSE current consumption	-	-	1	2	μA
I_{STOP}	Power down current	-	-	0.5	25	nA
f_{OSC_IN}	Oscillator frequency	-	-	32.768	-	kHz
V_{IL}	Crystal input (low)	-	-	-	$0.2 V_{DD}$	V
V_{IH}	Crystal input (High)	-	$0.8 V_{DD}$	-	-	V
V_{OL}	Crystal out (low)	-	-	-	$0.2 V_{DD}$	V
V_{OH}	Crystal out (high)	-	$0.8 V_{DD}$	-	-	V
C_L	Load capacitor	-	5	10	15	pF
R_F	Feedback resistor	-	7	10	13	MΩ
$t_{SU(LSE)}^{(2)}$	Startup time	-	-	-	1	s

NOTES:

1. Guaranteed by design.
2. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal, and it can vary significantly with the crystal manufacturer.

Figure 14. Crystal Oscillator**Figure 15. Clock Timing Measurement at SXIN****Figure 16. Typical Application with a 32.768 kHz Crystal****NOTE:**

1. An external resistor is not required between SXIN and SXOUT and it is forbidden to add one.

3.3.8 Internal Clock Source Characteristics

The parameters listed in Table 24 and Table 25 are obtained through tests conducted under ambient temperature and supply voltage conditions, which are specified in Table 15.

3.3.8.1 High-Speed Internal (HSI) RC Oscillator

Table 24. HSI Oscillator Characteristics ⁽¹⁾

(Temperature: -40°C to +105°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V _{DD}	Operating voltage	-	2.7	-	5.5	V
f _{HSI}	HSI frequency	V _{DD} =5.0 V, T _A =40°C	7.92	8	8.08	MHz
		@ -40°C to +105°C, user trim	-1	-	1	%
DuCy (HSI8)	Duty cycle	-	45	-	55	%
ΔV _{DD} (HSI8)	HSI8 oscillator Frequency drift over V _{DD}	V _{DD} =2.7 V to 5.5 V	-0.2	-	0.2	%
t _{su} (HSI8)	HSI8 oscillator start-up time	-	-	6	11	μs
t _{stab} (HSI8)	HSI8 oscillator stabilization time	-	-	-	35	μs
I _{DD} (HSI8)	HSI8 oscillator power consumption	-	-	250	350	μA

NOTE:

1. Guaranteed by characterization results and design.

3.3.8.2 Low-Speed Internal (LSI) 500 kHz RC Oscillator

Table 25. LSI Oscillator Characteristics

(Temperature: -40°C to +105°C)

Symbol	Parameter	Conditions ⁽²⁾	Min.	Typ.	Max.	Unit
V _{DD}	Operating voltage	-	2.7	-	5.5	V
f _{OUT}	Output frequency	V _{DD} = 2.7 to 5.5 V	350	500	650	kHz
t _{VREG_SU} ⁽¹⁾	500 kHz oscillator V _{REG} start-up time (after LSI enabled)	V _{DD} = 5.0 V	-	25	40	us
t _{STAB} ⁽¹⁾	500 kHz oscillator stabilization time (after LSI enabled)	5 % of target frequency	-	20	120	us
I _{LIRC} ⁽¹⁾	500 kHz oscillator power consumption	The LSI oscillator is enabled. V _{DD} =2.7 to 5.5 V	-	1.5	2.0	μA
		The LSI oscillator is disabled. V _{DD} =2.7 to 5.5 V	-	-	100	nA

NOTE:

1. Guaranteed by design.

3.3.9 PLL Characteristics

The parameters listed in Table 26 are obtained through tests conducted under ambient temperature and supply voltage conditions, which are specified in Table 15.

Table 26. PLL Characteristics ⁽¹⁾

(Temperature: -40°C to +105°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VDD	Operating voltage	-	2.7	-	5.5	V
I _{DD} (PLL)	PLL power consumption on V _{DD}	VCO freq = 280 MHz	-	1	-	mA
f _{PLL_P_OUT}	PLL output clock	Voltage scaling range	-	-	140	MHz
f _{VCO_OUT}	PLL VCO output	VCO frequency range	250	-	300	MHz
f _{DUTY}	Duty	-	40	-	60	%
f _{IN}	Input frequency	f _{PLLINCLK} / (PREDIV+1)	2	-	3	MHz
f _{PLLINCLK}	PLL block Input frequency	-	2	8	32	MHz
t _{JITTER}	P-P jitter	@ Lock state	-	-	40	ps
t _{LOCK}	PLL lock time	-	-	50	100	μs

NOTE:

1. Guaranteed by design.

3.3.10 Flash Memory Characteristics

Table 27. Code Flash Memory Characteristics

(Temperature: -40°C to +105°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t _{PROG}	Program time	-	-	-	30	μs
t _{PER}	Page erase time	-	-	-	4	Ms
t _{SER}	Sector erase time	-	-	-	4	Ms
t _{MER}	Mass (chip) erase time	-	-	-	8	Ms
N _{FWE}	Endurance of write/erase	T _A =25°C, page unit	10,000	-	-	times
t _{RT}	Retention time	-	10	-	-	years

Table 28. Data Flash Memory Characteristics

(Temperature: -40°C to +105°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t _{PROG}	Program time	-	-	-	30	μs
t _{PER}	Page erase time	-	-	-	4	ms
t _{SER}	Sector erase time	-	-	-	4	ms
t _{MER}	Mass (chip) erase time	-	-	-	8	ms
N _{FWE}	Endurance of write/erase	T _A =25°C, page unit	100,000	-	-	times
t _{RT}	Retention time	-	10	-	-	years

3.3.11 I/O Port Characteristics

3.3.11.1 General Input/Output Characteristics

Unless otherwise specified, the parameters in Table 29 are obtained through tests conducted under the conditions which are specified in Table 15. All I/Os conform to CMOS standards.

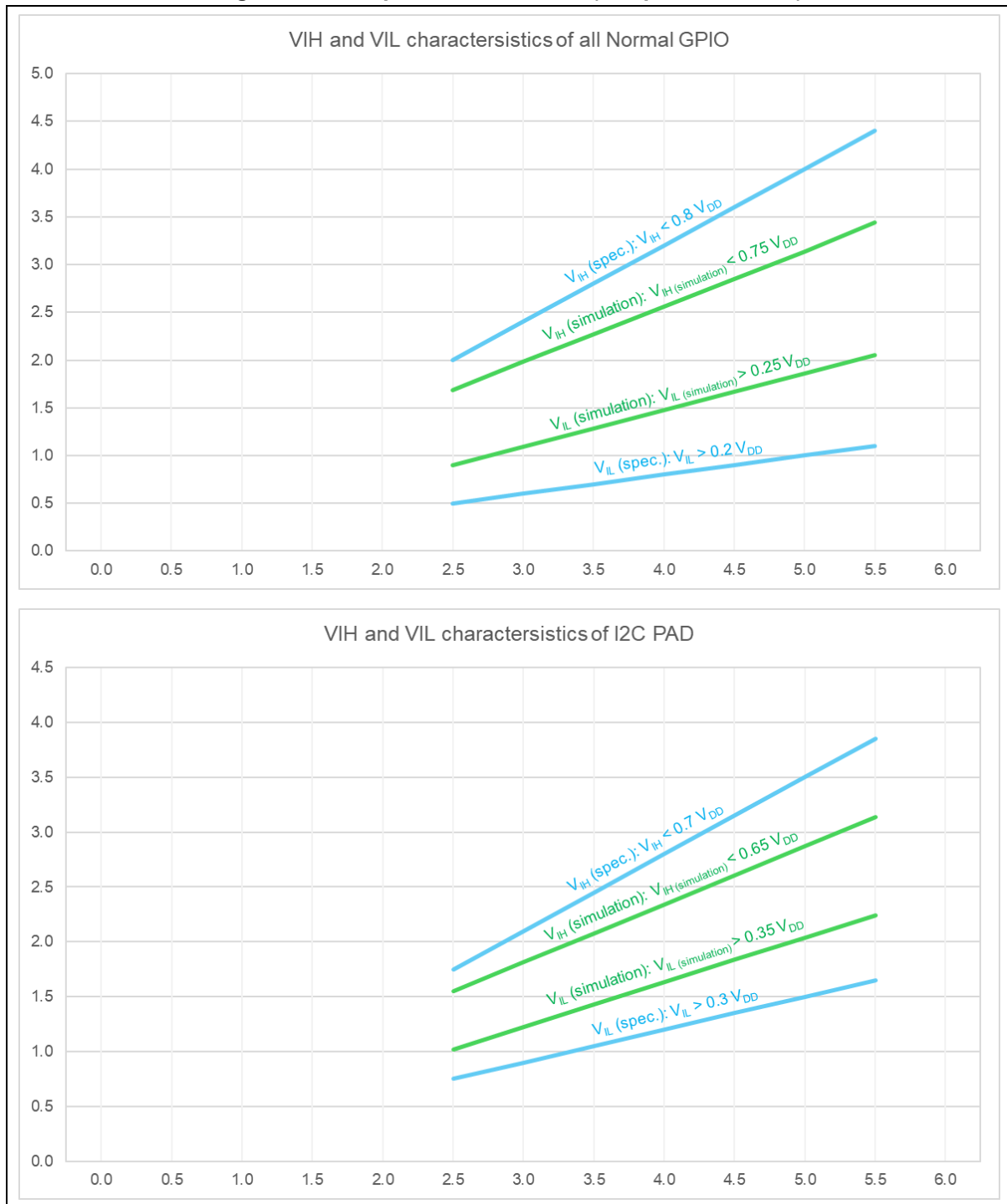
Table 29. I/O Static Characteristics

(Temperature: -40°C to +105°C)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
$V_{IL1}^{(1)}$	I/O input low-level voltage	5 V GPIO	$2.7\text{ V} < V_{DD} < 5.5\text{ V}$	-	-	$0.2 \times V_{DD}$	V
$V_{IH1}^{(1)}$	I/O input high-level voltage	5 V GPIO	$2.7\text{ V} < V_{DD} < 5.5\text{ V}$	$0.8 \times V_{DD}$	-	-	V
$V_{IL2}^{(1)}$	I2C I/O Input high voltage	5 V GPIO	$2.7\text{ V} < V_{DD} < 5.5\text{ V}$	-	-	$0.3 \times V_{DD}$	
$V_{IH2}^{(1)}$	I2C I/O Input low voltage	5 V GPIO	$2.7\text{ V} < V_{DD} < 5.5\text{ V}$	$0.7 \times V_{DD}$	-	-	
I_{leak}	Input leakage current ⁽²⁾	5 V GPIO	$2.7 < V_{IN} \leq 5.5\text{ V}$	-	-	± 1	μA
R_{PU}	Weak pull-up equivalent resistor	$V_{IN} = \text{GND}$		30	50	70	k Ω
R_{PD}	Weak pull-down equivalent resistor	$V_{IN} = V_{DD}$		30	50	70	

NOTES:

1. Data based on characterization results are not tested in production.
2. Guaranteed by design

Figure 17. I/O Input Characteristics (Temperature: 25°C)**NOTE:**

1. X-axis is VDD, Y-axis is VIH/L Spec.

3.3.11.2 Output Driving Current

The GPIOs can sink or source currents up to ± 3 mA and can also sink or source currents up to ± 9 mA when the V_{OL}/V_{OH} limits are relaxed.

To ensure compliance with the absolute maximum ratings specified in chapter 3.2, it is necessary to limit the number of I/O pins driving current in the user application.

3.3.11.3 Output Voltage Levels

Unless otherwise specified, parameters in Table 30 are obtained through tests conducted under ambient temperature and supply voltage conditions, which are specified in Table 15.

Table 30. Output Voltage Characteristics ⁽¹⁾

(Temperature: -40°C to $+105^{\circ}\text{C}$)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OH}	Output high voltage	Normal GPIO, $V_{DD} = 5\text{ V}$, $I_{OH1} = -3\text{ mA}$, $I_{OH2} = -9\text{ mA}$	$0.8V_{DD}$	-	-	V
		I2C PAD, $V_{DD} = 5\text{ V}$, $I_{OH1} = -3\text{ mA}$, $I_{OH2} = -9\text{ mA}$	$0.7V_{DD}$	-	-	
V_{OL}	Output low voltage	Normal GPIO, $V_{DD} = 5\text{ V}$, $I_{OL1} = 3\text{ mA}$, $I_{OL2} = 9\text{ mA}$	-	-	$0.2V_{DD}$	V
		I2C PAD, $V_{DD} = 5\text{ V}$, $I_{OL1} = 3\text{ mA}$, $I_{OL2} = 9\text{ mA}$	-	-	$0.3V_{DD}$	

NOTE:

1. Guaranteed by design.

3.3.12 ADC Characteristics

Table 31. ADC Electrical Characteristics

(Temperature: -40°C to +105°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
AV _{DD}	Operating voltage	-	2.7	5	5.5	V
-	Resolution	-	-	-	12	bit
I _{DDA}	Operating current	AVDD = 5.0 V @ f _{MCLK} = 25 MHz	-	2.2	-	mA
		AVDD = 5.0 V @ f _{MCLK} = 42 MHz	-	2.6	-	mA
V _{AN}	Analog input range	-	GND	-	AV _{DD}	V
t _{CONV}	Conversion time	-	18 / f _{ACLK}	-	48 / f _{ACLK}	μs
f _{CONV}	Conversion frequency	@ AVDD > 3.7 V	-	-	2.0	MHz
		@ AVDD > 3.1 V	-	-	1.6	MHz
		@ AVDD > 2.7 V	-	-	1.0	MHz
f _{ACLK}	Operating frequency	-	-	-	42	MHz
INL	DC accuracy	-	-	±4	-	LSB
DNL		-	-	±3	-	LSB
ZOE	Zero offset error	-	-	±3	-	LSB
FSE	Full-scale error	-	-	±3	-	LSB

3.3.13 DAC Characteristics

Table 32. DAC Electrical Characteristics

(Temperature: -40°C to +105°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
AV _{DD}	Analog Power Supply		2.7	-	5.5	V
C _L	Capacitive load	DAC output buffer on	-	-	100	pF
PSRR	Power supply rejection ratio	DAC output buffer on (C _L =50 pF, R _L =5 kΩ)	-	-60	-28	dB
I _{AVDD}	AV _{DD} Current	DAC output buffer on (No load, middle code)	-	315	500	μA
		DAC output buffer off (No load, middle code)	-	-	0.2	
V _{DAC_OUT}	Conversion Voltage Range	DAC output buffer on	0.2	-	AV _{DD} -0.2	V
T _{setting}	Setting time	DAC output buffer on (C _L =50 pF, R _L =5 kΩ)	-	-	3	μs
T _{wakeup}	Wakeup time from off state	DAC output buffer on (C _L =50 pF, R _L =5 kΩ)	-	4.2	7.5	μs
T _{W_to_W}	DAC output for a small variation of the input code (1LSB)	-	1	-	-	μs
Offset	Offset error at full code (0x400)	DAC output buffer on	-	-	±1	LSB
EGAIN	Gain error	DAC output buffer on	-	-	±0.2	% of FSR
TUE	Total unadjusted error	DAC output buffer on	-	-	±5	LSB
ENOB	Effective number of bits	DAC output buffer on	-	9	-	bits
DNL	Differential nonlinearity	-	-	-	±1.5	LSB
INL	Integrated nonlinearity	-	-	-	±2	LSB
SINAD	Signal-to-noise and distortion ratio	-	-	55	-	dB
Offset/Dt	Gain Error temperature coefficient	-	-	-	±5	ppm of/FSR/°C

3.3.14 Comparator Characteristics

Table 33. Comparator Characteristics

(Temperature: -40°C to +105°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V _{DD}	Operating voltage	-	2.7	-	5.5	V
I _{DD}	Operating current	-	-	160		μA
V _{IVR}	Input voltage range	-	0	-	5.5	V
V _{IO}	Input offset voltage	-	-5	-	+5	mV
t _D	Propagation delay	Overdrive voltage 100 mV	-	-	150	ns
V _{HYS} I _{DD}	Hysteresis Operating current	HYSSEL[1:0] = '00'	20	40	60	mV
		HYSSEL[1:0] = '01'	40	80	120	mV
		HYSSEL[1:0] = '10'	60	120	180	mV
		HYSSEL[1:0] = '11'	80	160	240	mV

3.3.14.1 General PCB Design Guidelines

The power supplier must be separated conforming to the scheme shown in Figure 8. The de-coupling capacitors across the V_{DD}/AV_{DD} are ceramic (good quality) capacitors and must be located as close as possible to the chip.

3.3.15 Communication Interfaces Characteristics

3.3.15.1 I2C Interface Characteristics

The I2C interface conforms to the timing requirements specified in the I2C-bus specification, in addition to the user timing requirements listed below:

- Standard mode (Sm): up to 100 kbps bit rate
- Fast mode (Fm): up to 400 kbps bit rate

The I2C timing requirements are guaranteed by design when the I2C peripheral is configured correctly, and the I2C clock frequency is equal to or greater than the minimum value listed in the table below.

Table 34. I2C Characteristics

(Temperature: -40°C to +105°C)

Symbol	Parameter	Standard		Fast		Unit
		Min.	Max.	Min.	Max.	
t _{SCL}	Clock frequency	0	100	0	400	kHz
t _{SCLH}	Clock high pulse width	4.0	-	0.6	-	μs
t _{SCLL}	clock low pulse width	4.7	-	1.3	-	
t _{BF}	Bus free time	4.7	-	1.3	-	
t _{STSU}	Start condition setup time	4.7	-	0.6	-	
t _{STHD}	Start condition hold time	4.0	-	0.6	-	
t _{SPSU}	Stop condition setup time	4.0	-	0.6	-	
t _{SPHD}	Stop condition hold time	4.0	-	0.6	-	
t _{VD}	Output valid from clock	0	-	0	-	
t _{DIH}	Data input hold time	0	-	0	1.0	
t _{DIS}	Data input setup time	250	-	100	-	ns

3.3.15.2 SPI Interface Characteristics

Unless otherwise specified, the parameters in Table 35 are obtained through tests conducted under ambient temperature, f_{CLK} frequency and supply voltage conditions, which are specified in Table 15.

- Capacitive load $C = 30 \text{ pF}$
- Measurement points are performed at the CMOS level: $0.5 V_{DD}$

For more information about I/O alternate function characteristics (SS, SCK, MOSI, and MISO for SPI), refer to section 0.

Table 35. SPI Characteristics

(Temperature: -40°C to $+105^{\circ}\text{C}$)

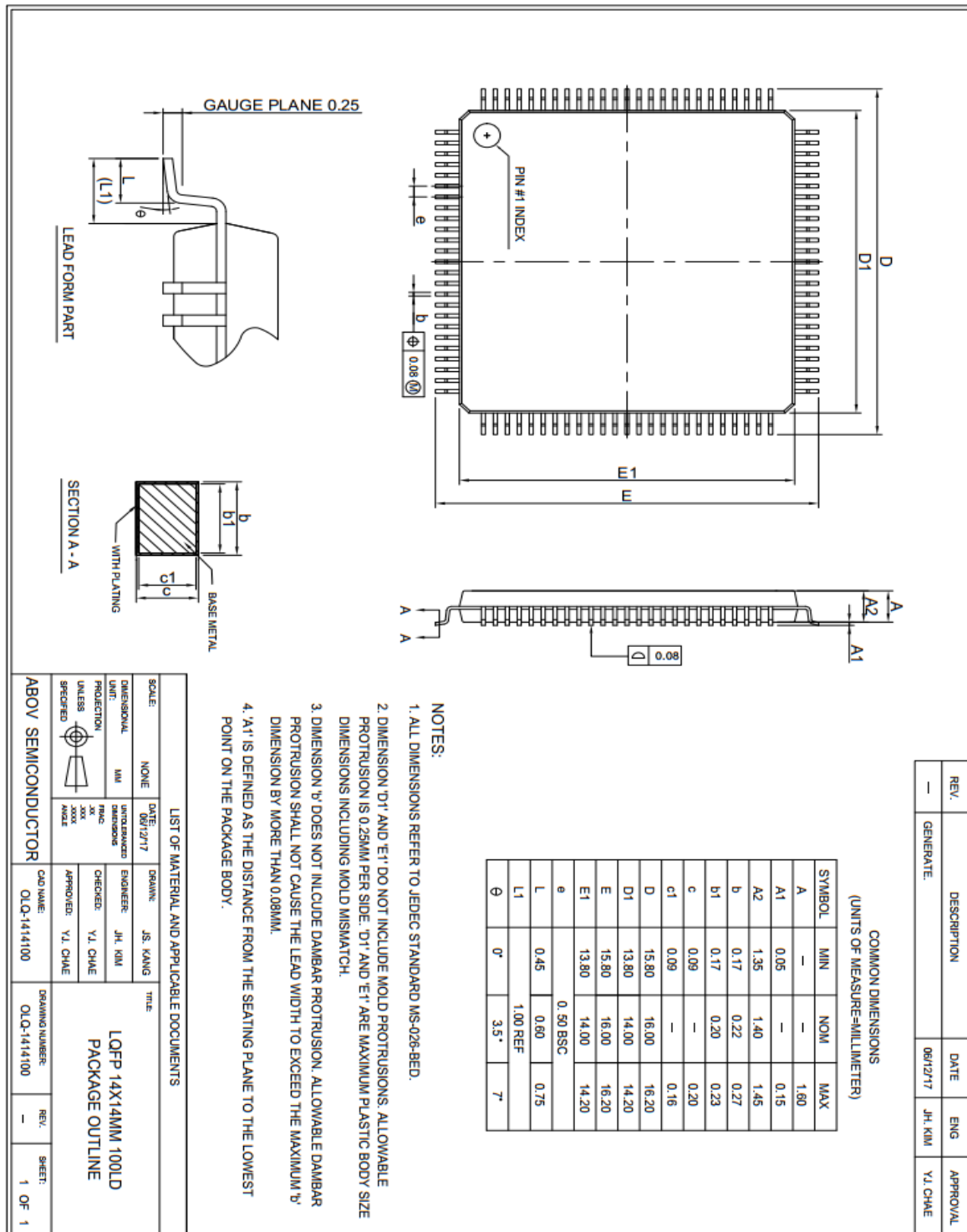
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{SCK1}	SPI clock frequency with strength on	SPI0, SPI1, SPI2 $2.7 \text{ V} \leq V_{DD} \leq 3.3 \text{ V}$	-	-	16	MHz
f_{SCK2}		SPI0, SPI1, SPI2 $V_{DD} \leq 5.5 \text{ V}$	-	-	16	MHz
f_{SCK3}	SPI clock frequency with strength off	SPI0, SPI1, SPI2 $2.7 \text{ V} \leq V_{DD} \leq 3.3 \text{ V}$	-	-	10	MHz
f_{SCK4}		SPI0, SPI1, SPI2 $V_{DD} \leq 5.5 \text{ V}$	-	-	15	MHz
Duty	Duty cycle of SPI frequency (SCK)	Slave Mode	30	50	70	%
C_{CL}	Capacitance load	-	-	-	30	pF

4. Package Information

4.1 100-LQFP Package Information

100-LQFP is a 100-pin, 14 x 14 mm quad flat package.

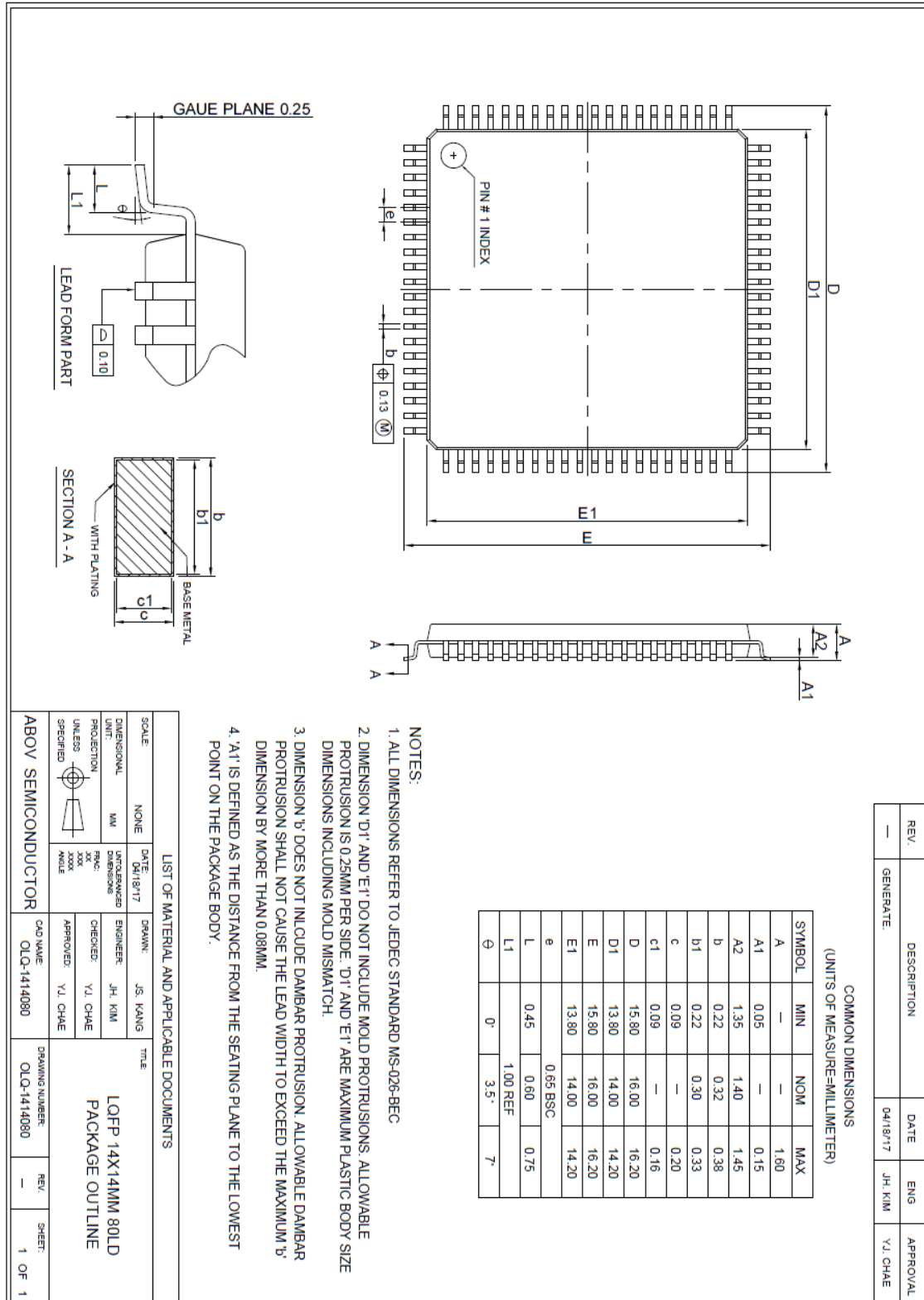
Figure 18. Package Dimension (100-LQFP)



4.2 80-LQFP Package Information

80-LQFP is an 80-pin, 14 x 14 mm quad flat package.

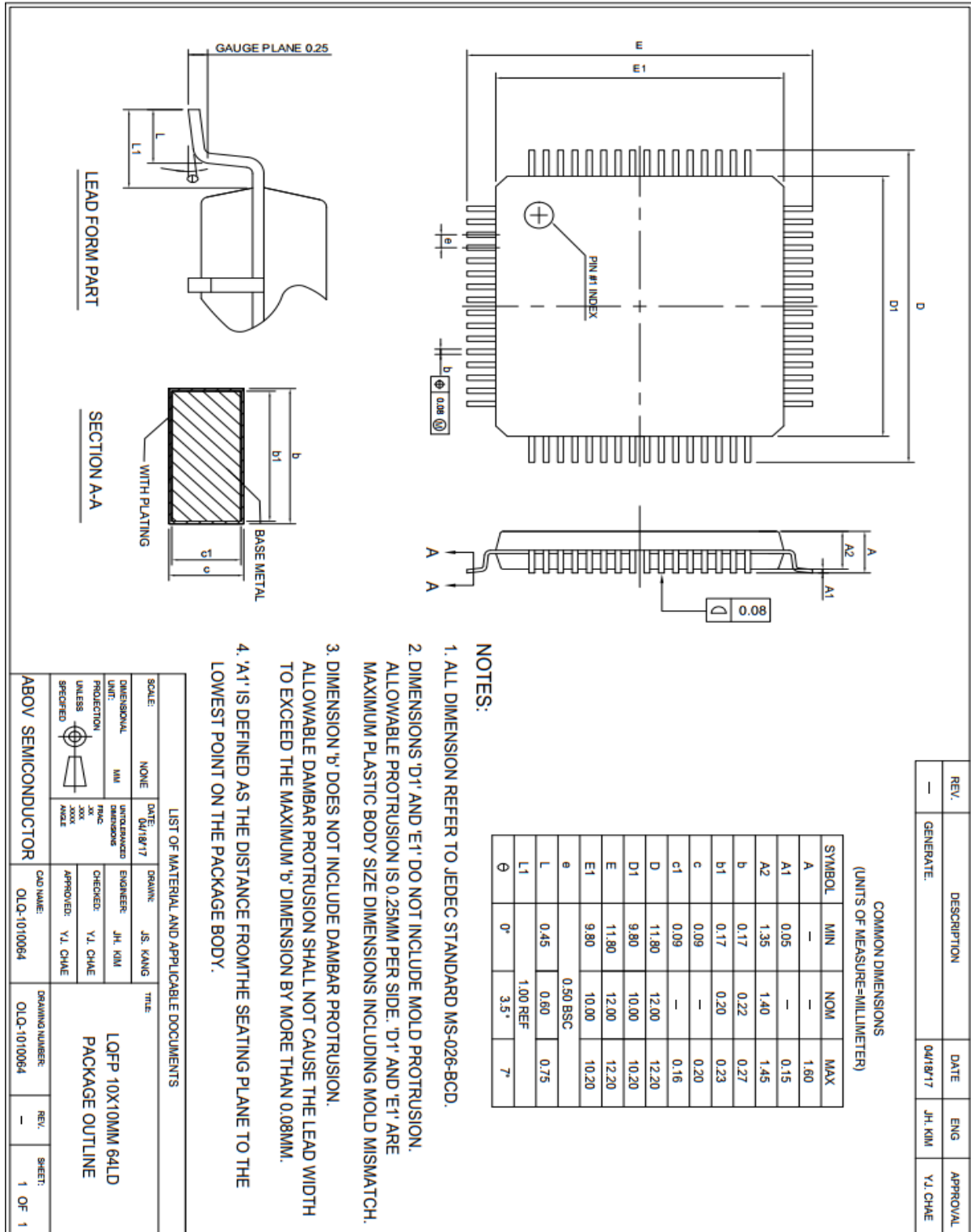
Figure 19. Package Dimension (80-LQFP)



4.3 64-LQFP Package Information

64-LQFP is a 64-pin, 10 x 10 mm quad flat package.

Figure 20. Package Dimension (64-LQFP)



5. Ordering Information

Figure 21. A34M456 Series Device Ordering Information

		A34M45 6	V	L	2	N	(T)
Device family name							
A34M45	ARM Cortex-M4F based microcontroller						
Code memory size							
6	256 KB						
Pin count							
V	100-pin						
M	80-pin						
R	64-pin						
Package type							
L	LQFP1, 0.50 mm pin pitch						
M	LQFP2, 0.65 mm pin pitch						
Temperature							
None	-40°C ~ 85°C						
2	-40°C ~ 105°C						
Internal information							
N	Internal management code						
Packing							
None	Tray						
(T)	Tape & reel						

NOTE:

1. For a list of available options (memory, package, etc.) or for further information on any aspect of this device, contact the nearest [ABOV sales office](#).

Glossary

This section gives a brief definition of acronyms and abbreviations used in this document:

- Word: Data of 32-bit length.
- AHB: Advanced high-performance bus.
- APB: Advanced peripheral bus.
- CRC: Cyclic Redundancy Check
- DMA: Direct Memory Access
- FRT: Free-Run Timer
- HSE: High-Speed External
- HSI: High-Speed Internal
- I2C: Inter-Integrated Circuit
- LSB: Least Significant Bit
- MSB: Most Significant Bit
- LQFP: Low-profile Quad Flat Package
- LSE: Low-Speed External
- LSI: Low-Speed Internal
- LVI: Low-Voltage Indicator
- LVR: Low-Voltage Reset
- MPWM: Motor Pulse-Width Modulator
- PFCP: Power-Factor Correction PWM
- PGM: Programming
- PLL: Phase Locked Loop
- POR: Power On Reset
- SCU: System Control Unit
- SPI: Serial Peripheral Interface
- UART: Universal Asynchronous Receiver and Transmitter
- WDT: Watchdog Timer

Revision History

Revision	Date	Notes
1.00	Dec. 20, 2024	Initial release
1.01	Jan. 10, 2025	Modified Table 1. Device Summary
1.02	Jun. 6, 2026	Updated 80-LQFP

Korea**Regional Office, Seoul****R&D, Marketing, and Sales**

8th Fl., 330, Yeongdong-daero, Gangnam-gu, Seoul,
06177, Korea

Tel: +82-2-2193-2200

Fax: +82-2-508-6903

www.abovsemi.com

HQ, Ochang**R&D, QA, and Test Center**

37, Gangni 1-gil, Ochang-eup, Cheongwon-gun,
Chungcheongbuk-do, 28126, Korea

Tel: +82-43-219-5200

Fax: +82-43-217-3534

www.abovsemi.com

Domestic Sales

Tel: +82-2-2193-2206

Fax: +82-2-508-6903

Email: sales_kr@abov.co.kr

Global Sales

Tel: +82-2-2193-2281

Fax: +82-2-508-6903

Email: sales_gl@abov.co.kr

China Sales

Tel: +86-755-8287-2205

Fax: +86-755-8287-2204

Email: sales_cn@abov.co.kr

Japan Sales

Tel: +81-6-6225-7758

Email: sales_jp@abov.co.kr

ABOV Disclaimer**IMPORTANT NOTICE – PLEASE READ CAREFULLY**

ABOV Semiconductor (“ABOV”) reserves the right to make changes, corrections, enhancements, modifications, and improvements to ABOV products and/or to this document at any time without notice. **ABOV DOES NOT GIVE WARRANTIES AS TO THE ACCURACY OR COMPLETENESS OF THE INFORMATION INCLUDED HEREIN.** Purchasers should obtain the latest relevant information on ABOV products before placing orders. Purchasers are entirely responsible for the choice, selection, and use of ABOV products and ABOV assumes no liability for application assistance or the design of purchasers’ products. **NO LICENSE, EXPRESS OR IMPLIED, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY ABOV HEREIN. ABOV DISCLAIMS ALL EXPRESS AND IMPLIED WARRANTIES AND SHALL NOT BE RESPONSIBLE OR LIABLE FOR ANY INJURIES OR DAMAGES RELATED TO USE OF ABOV PRODUCTS IN SUCH UNAUTHORIZED APPLICATIONS.** ABOV and the ABOV logo are trademarks of ABOV. For additional information about ABOV trademarks, please refer to https://www.abovsemi.com/en/about/corporate_identity.php. All other products or service names are the property of their respective owners. Information in this document supersedes and replaces the information previously supplied in any former versions of this document.

© 2024 - 2026 ABOV Semiconductor – All rights reserved