A34M438 Datasheet

Cortex®-M4 32-bit Microcontroller with FPU, 120 MHz, Up to 512 KB Code Flash, 64 KB SRAM, 3-Phase PWM, 12-bit ADC for Motor Control Application

DS Rev. 1.00

Features

Core and Memory

- Arm® 32-bit Cortex®-M4F Core
- Up to 120 MHz with FPU, 150 DMIPS
- Cache buffer (flash accelerator) support

Memories

- Up to 512 KB Code Flash Memory
- Up to 64 KB SRAM
- ECC (Error Correction Code)

Reset and Power Management

- Power-on/power-down reset (POR/LVR/LVI)
- Low-power modes: SLEEP, DEEP-SLEEP

Clock Management

- High-Speed Internal (HSI) oscillator 32 MHz
  - ±1.2% @ +25°C
  - ±3.0% @ −40°C to + 85°C
- Low-Speed Internal (LSI) oscillator 500 kHz
  - ±20% @ −40°C to +85°C
- High-Speed External (HSE) main oscillator
  - 4 MHz to 16 MHz
- Low-Speed External (LSE) sub-oscillator
  - 32.768 kHz
- Phase-Locked Loop (PLL) frequency generator
  - Up to 120 MHz

General-Purpose Input/Output (GPIO)

- Up to 89 I/O pins with interrupt capability
- All mappable on external interrupt vectors
- Multi-function pins have up to five selections of functions including GPIO

DMA Controller

- 16 channels
- 8-/16-/32-bit data transfers
- Compatible with 24 different types of peripherals

12-bit ADC

- Three independent ADC blocks
- 24 analog input channels
- Adjustable sample time and hold time
- Multiple operating modes:
  - Single conversion
  - Sequence conversion
  - Burst conversion
  - Multiple conversion

Internal Low-DropOut Regulator (LVD)

16-bit Timer

- 10 channels
  - 10 input capture channels
  - 10 output channels
- Timer operating modes:
  - Periodic timer mode
  - One-shot mode
  - PWM mode
  - Capture mode
- 10-bit prescaler

Watchdog Timer (WDT)

- 32-bit down-count timer
- Reset and periodic interrupts
- Eight different prescalers

Free-Run Timer (FRT)

- Two 32-bit free-run timer

Motor Pulse-Width Modulation (MPWM)

- Two MPWM generators
- Generating different waveforms through six channels with high- and low-signals of U, V, and W phases
- 16-bit up-/down-counters
- Six ADC trigger sources

Serial Interfaces

- UART
  - Six 16450 asynchronous serial communication ports
- SPI
  - Two synchronous serial communication ports
- I2C
  - Two communication ports

CRC Calculation Unit

- CRC operating modes:
  - CRC-32 (0x04C1_1DB7)
  - CRC-16-IBM (0x8005)
  - CRC-8 (0x07)
  - CRC-7 (0x09)
- Support for byte reversal of input/output data
- Compatible with DMA

Development Support

- Serial Wire Debug (SWD), JTAG interfaces

Packages

- 100-LQFP-1414 (0.5 mm pitch)
- 64-LQFP-1010 (0.5 mm pitch)

Operating Voltage

- 2.7 V to 5.5 V (ADC: 2.7 V to 5.5 V)

Operating Temperature

- Commercial grade (−40°C to + 85°C)

Applications

Inverter motor controller

Electric Pumps and Fans

Home Appliances (HA) display controller

Product Selection Table

Table 1. Device Summary

Device Name	Code Flash	SRAM	SPI	UART	I2C	MPWM	ADC	I/O Ports	Package
A34M438VL	512 KB	64 KB	2	6	2	2	24	89	100-LQFP
A34M438RL*	512 KB	64 KB	1	3	1	2	16	51	64-LQFP

* For available options or further information on the devices with "*" marks, please contact the ABOV sales office.

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1. Introduction

This document provides an overview of the device features, including high-level information and brief descriptions of each feature.

Refer to Table 3 for the list of supported features.

2. Descriptions

The A34M438 series is a 32-bit microcontroller based on the high-performance Arm Cortex-M4F core, with up to 512 KB of single bank code flash memory and 64 KB of SRAM. It is a powerful microcontroller with a Floating-Point Unit (FPU) that provides effective solutions for various electrical appliances requiring low power consumption and high performance, such as refrigerators, washing machines, dryers, dishwashers, water purifiers, and blenders. It is also suitable for controlling inverter motors where high-performance is critical.

2.1 Product Category Definition

Table 2 provides an overview of the memory capacity for available devices in the A34M438 series.

This document provides an overview of the features supported by each device, including high-level information and brief explanations for each feature.

Refer to Table 3 for the list of features supported by each product category.

Table 2. A34M438 Series Memory Density

Memory Density		Category
Flash	RAM	
512 KB	64 KB	A34M438

2.2 Device Overview

Table 3 summarizes and lists product specific features available in the A34M438 series considering the largest package.

Table 3. A34M438 Series Features and Peripherals

Peripherals		Description
Core	CPU	• Maximum operating frequency: 120 MHz • 32-bit Arm Cortex-M4F core - 32-bit Thumb®-2 instruction set • Register settings in CPU: - General-purpose registers specified - Main stack pointer (MSP) and process stack pointer (PSP): R13 - Link register (LR): R14 - Program counter (PC): R15 • Data ordering format: Little-Endian • Harvard Architecture • AHB/APB
	Interrupt	• NVIC (Nested-Vectored Interrupt Controller) • Up to 51 peripheral interrupts supported • Assignable with 16 different priority levels
	FPU	• Rendered by extending and transforming the ARMv7 floating-point arithmetic functionality • Compliant with the ANSI/IEEE 754 standard • Capable of binary floating-point arithmetic and computation

Table 3. A34M438 Series Features and Peripherals (continued)

Peripherals		Description
Memory	Code Flash	• Capacity: - A34M438: 512 KB code flash memory • A high-capacity code flash memory built in • Max 30 MHz flash access speed • One-word (4-byte) program • Bulk (full-chip), 512-byte and 2 KB erases • Read protection • Self-programming (Supports updating data in a code flash memory region during the execution of user program in the code area.) • CRC code generation and verification for the Flash memory • Single Bank code flash memory (512 KB) • Support ECC (Error Correct Code) • Endurance: 10,000 cycles • Lifetime: 10 years
	BootROM	• Entering the boot mode by setting the nBOOT pin to low-level during a reset procedure. • UART boot mode • In-System Programming • The boot mode can program the internal flash memory via UART.
	SRAM	• Capacity: 64 KB • Usable as a program's work area • High-speed execution enables the execution of time-critical codes. • Part of the SRAM can be remapped into an interrupt vector area.

Table 3. A34M438 Series Features and Peripherals (continued)

Peripherals		Description
System Control Unit (SCU)	Operating Frequency	• Up to 120 MHz
	Clock	• High-speed internal oscillator (HSI) • 32 MHz - ±1.2% @ +25˚C - ±3.0% @ −40˚C to +85˚C • Low-speed internal oscillator (LSI) - 500 kHz (±20% at −40˚C to +85˚C) • External main oscillator (HSE): 4 MHz to 16 MHz • External sub-oscillator (LSE): 32.768 kHz • Phase-Locked Loop (PLL) frequency generator generates a high-speed clock (up to 120 MHz)
	Clock Monitoring	• System Fail-Safe function by Clock Monitoring - External main oscillator (HSE) - External sub oscillator (LSE) - Main system clock (MCLK)
	Operating Mode	• Run mode • Sleep mode • Deep sleep (STOP1, STOP2) mode
	Reset	• nRESET pin reset • Core reset • Software reset • POR (Power-On Reset) • LVR (Low Voltage Reset) • WDTR (Watchdog Timer Reset) • Reset due to clock oscillating error
	LDO	• Low-dropout (LDO) regulator built in for low-voltage operation
	POR	• The POR generator detects an internal 1.4 V voltage and generates a reset signal.
	LVI	• 16 low-voltage detection levels • Supports LVD interrupt • Supports wake-up from SLEEP mode

Table 3. A34M438 Series Features and Peripherals (continued)

Peripherals		Description
System Control Unit (SCU)	Wake-up	• Wake-up by a general-purpose input/output (GPIO) pin • Wake-up by a free-run timer (FRT) • Wake-up by a Watchdog Timer (WDT) • Wake-up by a low-voltage indicator (LVI)
General-Purpose I/O (GPIO)		• Input/output (I/O) port for general purposes • 100-LQFP - I/O pins: 89 • 64-LQFP - I/O pins: 51 • Each pin can be set for one of the following modes: - Push-pull output - Open drain output - Input • The use of each pin can be set by setting the pin multiplexer. • Each pin can be configured as an external interrupt source, either the high-level/low-level interrupt or the rising-edge/falling-edge interrupt • Pull-up or pull-down resistor, and debouncing can be set for each pin. • Drive strength can be adjusted for each port pin. • Each pin bit can be individually set and reset. • Wake-up events triggered by external asynchronous inputs
Direct Memory Access Controller (DMA)		• 16-ch direct memory access (DMA) supports peripherals • 8-/16-/32-bit data transfers • Compatible with 22 different types of peripherals - SPIn (SPI0, SPI1) - UARTn (UART0, UART1, UART2, UART3, UART4, UART5) - CRC - ADC (ADC0, ADC1, ADC2)

Table 3. A34M438 Series Features and Peripherals (continued)

Peripherals		Description
Timer	16-bit timer	• General-purpose 16-bit up-count timer • 10 channels - 10 timer *n* capture port (T*n*IO) input channels - 10 timer *n* output port (T*n*IO) output channels • Timer operating modes - Periodic timer mode - One-shot mode - PWM mode - Capture mode • Interrupt events - Timer/counter match interrupt - Timer overflow interrupt • Input clock selection - Clocks are freely selectable through the miscellaneous clock control registers (SCU_MCCRx) - External clocks are selectable • Timer signals can be generated through T*n*IO pins • 10-bit prescaler
	WDT	• 32-bit down-count timer • Reset and periodic interrupts • Clocks are freely selectable through the miscellaneous clock control registers (SCU_MCCRx) • Eight different prescalers are selectable
	FRT	• 32-bit free-run timer - Capable of calculating the internal system time - 32-bit up-count timer • Interrupt events - Period interrupt - Overflow interrupt

Table 3. A34M438 Series Features and Peripherals (continued)

Peripherals		Description
Serial Interface	UART	• A total of six 16450 asynchronous serial communication ports • Configurable standard asynchronous communication bits (start, stop, and parity) • Flexible communication available through programming - 5- to 8-bit data transfers - Even/Odd/Non-parity generation and checking - 1-bit, 1.5-bit, or 2-bit stop bit generation and checking • 8-bit fraction controller and 16-bit baud rate generator
	SPI	• Two synchronous serial communication port channels • Master/slave operation • Loop-back mode • Programmable and flexible communication • 8-/9-/16-/17-bit data transmit and receive - SPI clock speed - Both least significant bit (LSB)-first and most significant bit (MSB)-first modes available
	I2C	• Standard I2C communication protocol • Two channels supported • Master and slave modes supported for each channel • 7-bit addressing supported for slave mode • SCL signal's high/low periods and SDA signal's hold time settable
Motor Pulse-Width Modulation	MPWM	• Two MPWM generators • Six channels (high and low signals of phases U, V, and W) generate different waveforms • 16-bit up/down counters • Six ADC trigger sources • Interrupt events - Bottom interrupts - Top (period) interrupts • Interval interrupt mode

Table 3. A34M438 Series Features and Peripherals (continued)

Peripherals		Description
Motor Pulse-Width Modulation	MPWM	• Falling and rising dead-time applicable • Phases U, V, and W are independently controlled. • A special operating mode: - Different carrier counters running for phases U, V, and W - Different duty and periods configurable for phases U, V, and W - Different interrupts used for phases U, V, and W • Capture functionality • Protection and over-voltage detection supported
12-bit A/D Converter	ADC	• Three independent ADC blocks • 24 analog input channels • Operating modes: - Single conversion - Sequence conversion - Burst conversion - Multiple conversion • Up to eight sequential conversions supported • Software triggers supported • Three internal trigger sources (MPWM and timers) supported • Sample time and hold time are adjustable

Table 3. A34M438 Series Features and Peripherals (continued)

Peripherals		Description
Cyclic Redundancy Check	CRC	• CRC operating modes: - CRC-32 (0x04C1_1DB7) - CRC-16-IBM (0x8005) - CRC-8 (0x07) - CRC-7 (0x09) • Input/output data reversion supported • Compatible with DMA
Operating Voltage		• 2.5 V to 5.5 V
Operating temperature		• Commercial grade (−40˚C to +85˚C)
Package		• Three types of package options - 100-pin LQFP - 64-pin LQFP

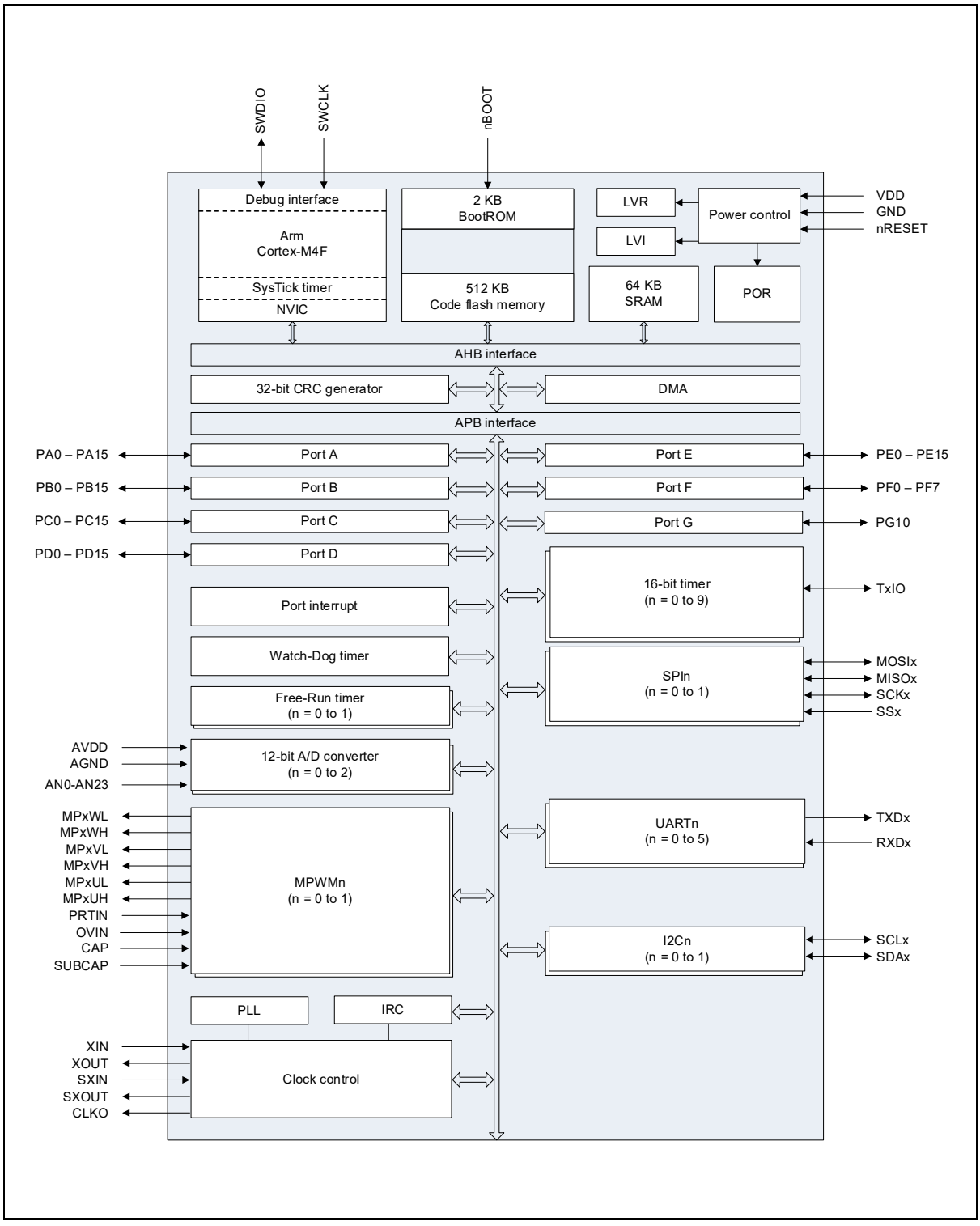
Table 4. Summary of A34M438 Peripherals

Peripheral		A34M438VL	A34M438RL
Code Flash Memory		512 KB	512 KB
SRAM		64 KB	64 KB
Timers	MPWM	2 (16-bit)	
	General-Purpose Timer	10 (16-bit)	
	SysTick Timer	1	
	Watchdog Timer	1	
	Free-Run Timer	2	
Communication Interfaces	SPI	2	1
	I2C	2	1
	UART	6	3
DMA (Direct Memory Access)		16	
GPIO		89	51
12-bit ADCs		1.5 Msps x 3 units	
Number of Channels		24	16
CRC		1	
Operating Frequency		Max. 120 MHz	
Operating Voltage		2.5 V to 5.5 V	
Operating Temperature		Ambient operating temperature: −40°C to +85°C	
Packages		100-LQFP	64-LQFP

2.3 Block Diagram

Figure 1 shows a block diagram of A34M438 series.

Figure 1. A34M438 Block Diagram



2.4 Functional Overview

The following sections provide overviews of the features of the A34M438 series microcontroller.

2.4.1 Cortex-M4F Core

The Arm® Cortex-M4F has the same functions as the Cortex-M4 and includes optional floating point arithmetic functionality. The two processors are intended for deeply embedded applications that require fast interrupt response features.

Refer to the technical reference manual “ARM ID061113” for detailed information of Cortex-M4F.

2.4.2 Floating Point Unit (FPU)

The Cortex-M4 FPU is an implementation of the single precision variant of the ARMv7-M Floating-Point Extension (FPv4-SP). It provides floating-point computation functionality that is compliant with the ANSI/IEEE Std 754-2008, IEEE Standard for Binary Floating-Point Arithmetic, referred to as the IEEE 754 standard. The FPU supports all single-precision data-processing instructions and data types described in the ARM®v7-M Architecture Reference Manual.

2.4.3 Embedded SRAM

The A34M438 series has a block of 0-wait on-chip SRAM. The size of the SRAM is 64 KB and its base address is 0x2000_0000.

The SRAM memory area is commonly utilized for data storage and stack memory. It can also be used to store program code for faster execution or during flash erase or programming operations.

2.4.4 Boot Configuration

The A34M438 series offers one boot mode for programming internal flash memory. The boot mode can be entered by setting nBOOT pin to 'Low' during the system reset process (the normal state is 'High').

Boot mode supports UART boot, and the UART boot uses TXD0 and RXD0 ports.

Pins for the boot mode are listed in Table 5.

Table 5. Boot Mode Pin List

Block	Pin Name	Pin Direction	Description
SYSTEM	nRESET/PC10	Input	Reset input signal
	nBOOT/PC11	Input	Boot mode setting pin
UART0	RXD0/PC14	Input	UART boot receive data
	TXD0/PC15	Output	UART boot transmit data

2.4.5 Power Supply

The device requires a 2.5 V to 5.5 V operating voltage supply (VDD) and analog peripherals are supplied through the independent power domain AVDD.

Table 6. Power Supply

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	2.5	5.5	V
	AV_{DD} (Analog V_{DD})	2.7	5.5	V

During a power-up process, a reset is fundamental and affects the entire system booting process. A34M438 series has two power-related reset options as described below:

- POR_RST (Power-On Reset) that controls the voltage less than 1.4 V.
- LVD_RST (Low-Voltage Detect Reset) that controls the voltage less than 2.2 V (default).

If the power level is higher than the POR and below the flash memory operating voltage (min. 1.35 V), code read operation may malfunction. To prevent this abnormal code read operation, the LVD_RST generates the SYSRESETn internal signal and enter the microcontroller into reset mode to prevent the abnormal operation. The minimum level that can be set by the LVR is 1.6 V, which satisfies the minimum operating voltage of flash memory.

2.4.6 Operation Mode

2.4.6.1 Transition of Operation Mode

INIT mode is the initial state of the chip when a reset signal is asserted.

In RUN mode, the CPU can operate at the maximum performance with the high-speed clock system.

SLEEP and DEEP-SLEEP modes can be used as low power consumption mode. In the low power consumption mode, power is effectively managed to reduce power consumption by halting the processor core and any unused peripherals.

2.4.6.2 RUN Mode

In RUN mode, the CPU and peripheral hardware operate with a high-speed clock. After a reset, the system will enter RUN mode if the INIT state is detected.

2.4.6.3 SLEEP Mode

Once the microcontroller enters SLEEP mode, the CPU becomes inactive. By setting the SCU_PER and SCU_PCER registers, users can determine which peripherals are to be inactive in SLEEP mode.

2.4.6.4 DEEP-SLEEP (STOP1, STOP2) Mode

When the core goes under stop state using WFI instruction, the chip enters in DEEP-SLEEP mode. DEEP-SLEEP mode is divided into DEEP-SLEEP (STOP 1) and DEEP-SLEEP (STOP 2) modes.

2.4.6.5 Reset Mode

The A34M438 series has two system reset options: a cold reset, which is effective during power up or down sequences, and a warm reset, which is triggered by multiple reset sources.

The reset features of the A34M438 series are as follows:

- Power-On reset (POR)
- Low-Voltage Detect Reset (LVR)
- nRESET pin reset
- Watchdog Timer (WDT) reset
- Software reset
- Clock oscillating error reset
- CPU request reset

2.4.7 Clocks and Startup

The A34M438 series has two main operating clocks: HCLK, which generates clock signals for CPU and AHB system, and PCLK, which generates clock signals for peripheral systems.

2.4.7.1 HCLK Clock

The Cortex-M4F core requires two clocks: HCLK and FCLK. While the HCLK supplies the clocks of both the CPU and AHB, the FCLK remains enabled unless the system enters DEEP-SLEEP mode. Conversely, during SLEEP mode, the HCLK can be disabled while the FCLK continues to function.

The buses and memories are clocked by the HCLK. As the bus clock frequency is limited to a maximum of 120 MHz, the HCLK frequency must not exceed 120 MHz.

2.4.7.2 PCLK Clock

The PCLK is used as a clock source for peripherals. The SCU_PCER registers can enable or disable the PCLK for each peripheral. If a peripheral block's PCLK input is not enabled, its registers cannot be read. Additionally, it is important to note that the PCLK stops operating in DEEP-SLEEP mode.

2.4.7.3 Clock Configuration Procedure

When the microcontroller is powered up, the LSI (500 kHz) operates as the default system clock. Later, during system initialization, the system clock changes from LSI (500 kHz) to HSI (4 MHz = 32 MHz/8). HSI (32 MHz) and HSE can be configured under user control using the SCU_CSCR (clock source control register).

Before enabling the HSE block, the pin mux for XIN and XOUT must be configured. During this process, it is important to avoid affecting other bits of the PC_MR and PC_CR registers. After enabling the HSE block, it is necessary to wait for the crystal oscillation to be stabilized before proceeding.

The sub-oscillator, Low Speed External (LSE, operating at 32.768 kHz) clock, can be enabled using the SCU_CSCR register (Clock Source Control Register). Like the HSE, the LSE must be enabled after configuring the pin mux for SXIN and SXOUT and allowing sufficient time for the oscillation to be stabilized.

2.4.8 Interrupts and Events

2.4.8.1 Nested Vectored-Interrupt Controller (NVIC)

The A34M438 series includes up to 51 maskable interrupt sources that manage sixteen priority levels and the Nested Vector Interrupt Controller (NVIC) that controls the interrupt lines of the Cortex®-M4.

The NVIC has the following advantages:

- NVIC enables interrupt processing while reducing interrupt latency.
- Interrupt Vector Table (IVT) address delivered directly to the core.
- Fast interrupt processing capability
- Higher priority interrupts are completed before lower priority interrupts, although they are generated later than the lower priority interrupts.
- Tail Chaining
- Automatic saving of processor state
- Interrupt restoring without instructional overhead at the end of the interrupt

The NVIC hardware block provides flexible and efficient interrupt management with minimal interrupt latency.

2.4.8.2 Extended Interrupt (EXTI)

The Extended Interrupt feature enables the system to generate event requests or wake up from STOP mode. Each external line can be configured independently to detect trigger events such as rising or falling edges, or both edges, as well as level events such as Low or High.

2.4.9 GPIO (General-Purpose Input/Output)

2.4.9.1 PCU Module

The A34M438 series has a Port Control Unit (PCU) module that controls the external input and output (I/O) ports. By setting the PCU registers, users can configure the pins' uses, input/output direction, pull-up/pull-down, and debouncing for their applications as needed.

2.4.9.2 GPIO Module

Pins except the VDD, GND, and certain specific-purpose pins can be used as General-Purpose Input/Output (GPIO) pins.

The GPIO module controls the general I/O ports. Output pins can be set to generate high- or low-level signals by configuring the corresponding bits of the GPIO control register, while logic input pins can be monitored for their input status in the control registers.

2.4.10 Embedded Flash Memory

The flash memory controller is an interface controller for embedded flash memory. It manages data stored on the flash memory and communicates with other electronic devices.

The flash memory of the A34M438 series has features as listed below:

- Code flash memory for 512 KB with write protection bits
- Erase units
  - Page (512 bytes)
  - Sector (2 KB)
  - Bulk (up to 512 KB, code flash memory)
- Program unit: Word (four bytes)
- Zero wait (less than 30 MHz), 1- to 15-wait, and cache (flash acceleration) access
- Data and instruction caches for code flash memory
- Built-in 16-bit specific polynomial for code memories
- ECC (Error-Correction Code)
- Self-programming of the code flash memory
  - Supports updating data in a code flash memory region while executing user programs in the code flash area.

2.4.11 DMA (Direct Memory Access) Controller

The direct memory access (DMA) controller is used for high-speed data transfers between peripherals and memories. The DMA allows quick data transfers by copying or moving data between memory locations or between memory and peripherals, without involving the core.

- 16 channels
- Single-ended signaling only
- 8-/16-/32-bit data transfers
- Multiple buffers of the same size
- DMA transfers are triggered by peripheral interrupts

2.4.12 Timers

2.4.12.1 16-bit Timer

The A34M438 series has a TIMER module configured with 10 units. This 16-bit Timer supports four operating modes: Periodic Mode, PWM Mode, One-shot Mode, and Capture Mode.

Users can use a divided PCLK or an external clock as a clock source for the 16-bit Timer. An internal 10-bit prescaler allows to generate a variety of timer base clocks.

Interrupts can be triggered at regular intervals when the timer is used in Periodic Mode. Users can set the period and duty to form a PWM signal that is used in PWM Mode.

In One-shot Mode, the timer can generate one PWM waveform. The Capture Mode allows measuring the pulse intervals of an external input signal based on the predefined conditions. In addition, this timer can transmit signals to control other devices and is primarily used as a periodic tick timer or as a wake-up source.

2.4.12.2 Free-Run Timers (FRT)

The A34M438 series has two built-in Free-run Timer (FRT) that are 32-bit up count timers. The FRT can run with an overflow interrupt or a match interrupt according to their register setting and can remain active in DEEP-SLEEP (STOP 1) mode.

2.4.12.3 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is used to detect errors in the microcontroller caused by external interference or unexpected logical conditions. These errors cause the application program to deviate from its normal sequence. If the microcontroller loses control, the WDT will reset the microcontroller, allowing it to return to normal operation.

The WDT of the A34M438 series is a 32-bit down counter. If the WDT is set as a reset source, the microcontroller restarts when the down counter reaches zero.

When it is not used to monitor the microcontroller, the WDT can be used as a cycle timer along with an interrupt.

2.4.12.4 SysTick Timer

Although the SysTick timer is primarily designed for real-time operating systems, it can also be utilized as a standard down-counter.

The SysTick timer has the following features:

- 24-bit down-counter
- Automatic refreshing
- Maskable system interrupt generation when counter reaches zero.
- Programmable clock source

2.4.13 UART (Universal Asynchronous Receiver/Transmitter)

The A34M438 series has a six-channel UART module. The built-in UART module allows users to specify settings for transmitting and receiving data and provides the ability to read the current status of the UART. By providing information about the current state of transmission and reception processes, including types and conditions, the UART module enables users to monitor potential errors such as parity, overrun, framing, or break interrupts during data reception.

The UART module includes a programmable baud-rate generator for each channel, which generates an internal clock for its corresponding UART unit. This is achieved by dividing a prescaled clock using a baud-rate divisor that ranges from 1 to 65535 and then dividing the result by 16.

Users can program interrupts that can control UART communication.

Furthermore, the built-in DMA allows the UART module to transfer data directly to or from memory without involving the CPU, reducing CPU usage, and increasing the speed of data transfer.

2.4.14 SPI (Serial Peripheral Interface)

The A34M438 series has two built-in Serial Peripheral Interface (SPI) modules. The SPI modules are synchronized by clocks, and the specifications of the transfer clocks are adjustable.

The SPI module supports communication between one master and slaves. Slaves can be selected by the Slave Select (SS) signal.

The SPI module performs four-wire synchronous transfers via four signal terminals (SS, SCK, MOSI, and MISO). Its separate Transmit and Receive Buffers enable full-duplex communication, which is capable of reading and writing data simultaneously.

Specifically, the SPI module of the A34M438 series can enhance the Port Drive Strength so that the SPI rate can be supported up to 12 MHz with the enhanced Port Drive Strength.

2.4.15 I2C (Inter-Integrated Circuit) Interface

The I2C (Inter-integrated Circuit) interface built in the A34M438 series satisfies the standard I2C communication protocol and is used for serial communication with internal and external devices via the I2C protocol.

Equipped with two units, it supports both master and slave modes and is capable of transmitting and receiving data in bytes by using interrupts or polling.

The I2C of the A34M438 series operates in Standard mode (100 kHz) or Fast mode (400 kHz) and supports General call.

It helps communicate with various peripherals that have the same bus type. To use the I2C, it is recommended to set the SCL and SDA pins to open-drain and then connect external pull-up resistors to render their output signals 'HIGH'.

Table 7. Features of I2C

I2C Features	I2C0	I2C1
7-bit addressing mode	O	O
Standard-mode (up to 100 kbit/s)	O	O
Fast-mode (up to 400 kbit/s)	O	O
General call	O	O

2.4.16 MPWM (Motor Pulse-Width Modulation)

The A34M438 series supports two Motor Pulse-Width Modulation (MPWM) units. The MPWM in the A34M438 series operates in total of three PWM modes as shown below to support various applications:

- Motor PWM mode for motor control
- Normal PWM mode for a variety of PWM applications
- Individual PWM mode for specific applications such as IH cooker

The MPWM module of the A34M438 series provides a range of PWM control functionalities in both Motor and Normal PWM modes, including up to six channel outputs, dead-time management, up to six ADC triggers, a variety of interrupt event generations under different conditions, and protection events.

In Individual PWM mode, unlike Motor and Normal PWM modes, the MPWM module operates separately for each phase, and controls up to three outputs individually.

2.4.17 ADC (Analog-to-Digital Converter)

The A34M438 series features a 12-bit resolution Analog-to-Digital Converter (ADC) module. It consists of three independent controllable units and supports up to 24 different analog inputs.

The ADC module supports A/D conversion of multiple channels in different modes, including single mode, sequential mode, multiple mode, inject mode and burst mode. It supports the sampling of voltage inputs from multiple channels at critical times, which is essential for various applications. This can be accomplished using the triggering functionality in conjunction with TIMER and MPWM.

Once the A/D conversion is complete, the result is stored in 16-bit data registers with left alignment.

The ADC is mapped to the APB and capable of high-speed operation based on the internal clock source. In addition, it uses built-in DMA to reduce microcontroller core load while enabling fast data sampling.

The analog input monitoring and comparison capabilities of the ADC allow the applications to determine whether the input voltage is above or below the predefined level.

2.4.18 CRC (Cyclic Redundancy Check Calculation) Module

A Cyclic Redundancy Check (CRC) module is used to get 32-bit, 16-bit, 8-bit and 7-bit CRC codes from 8-bit or 32-bit data size. The user application can utilize CRC-based technologies to ensure the integrity of data transfers, storage, and flash memories in compliance with functional safety standards.

Specifically, the CRC module of the A34M438 series supports DMA.

3. Pinouts and Pin Descriptions

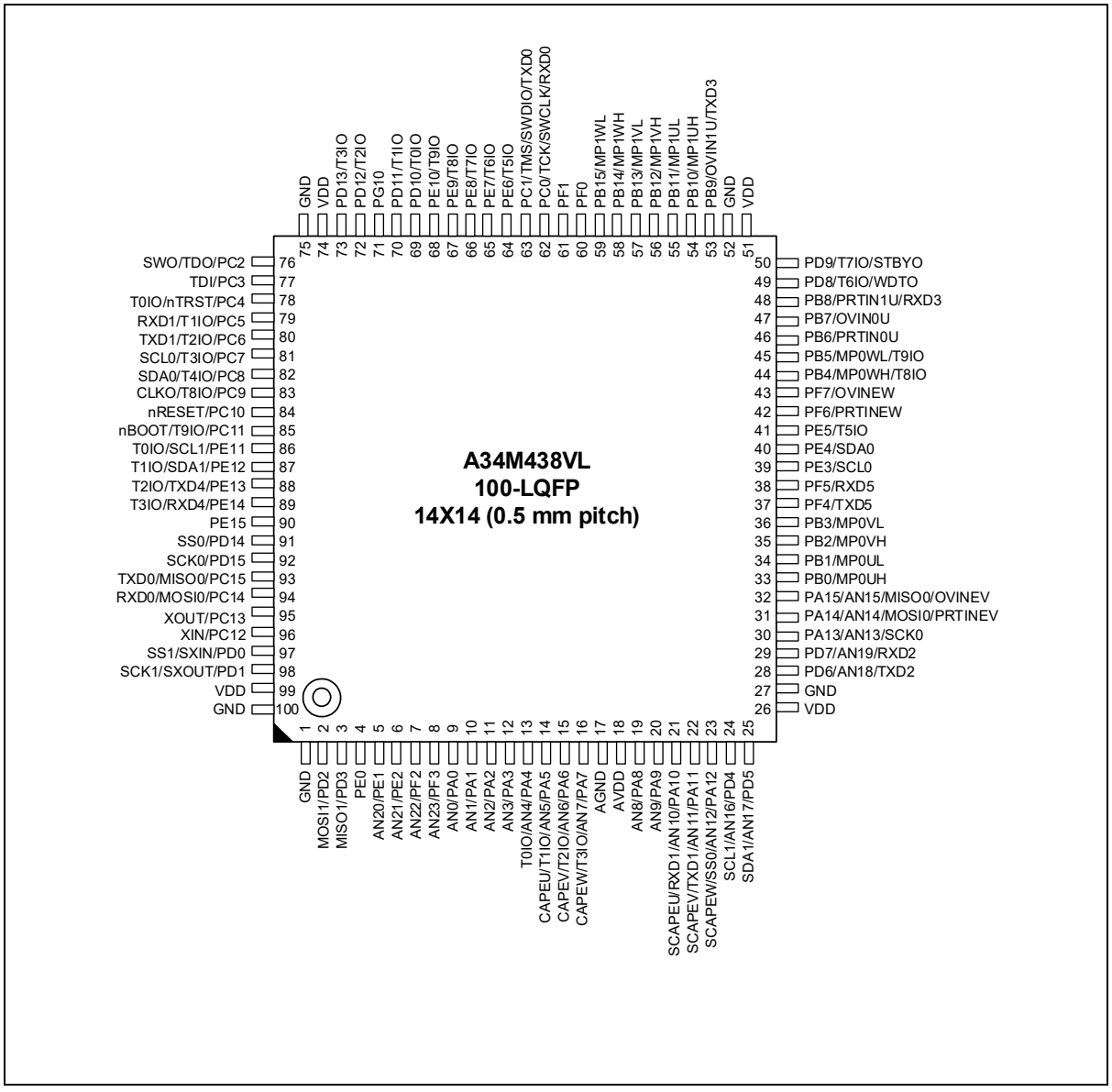
In this chapter, pinouts, and pin descriptions of the A34M438 series are described.

3.1 Pinouts

Figure 2, and Figure 3 show the top views of the packages.

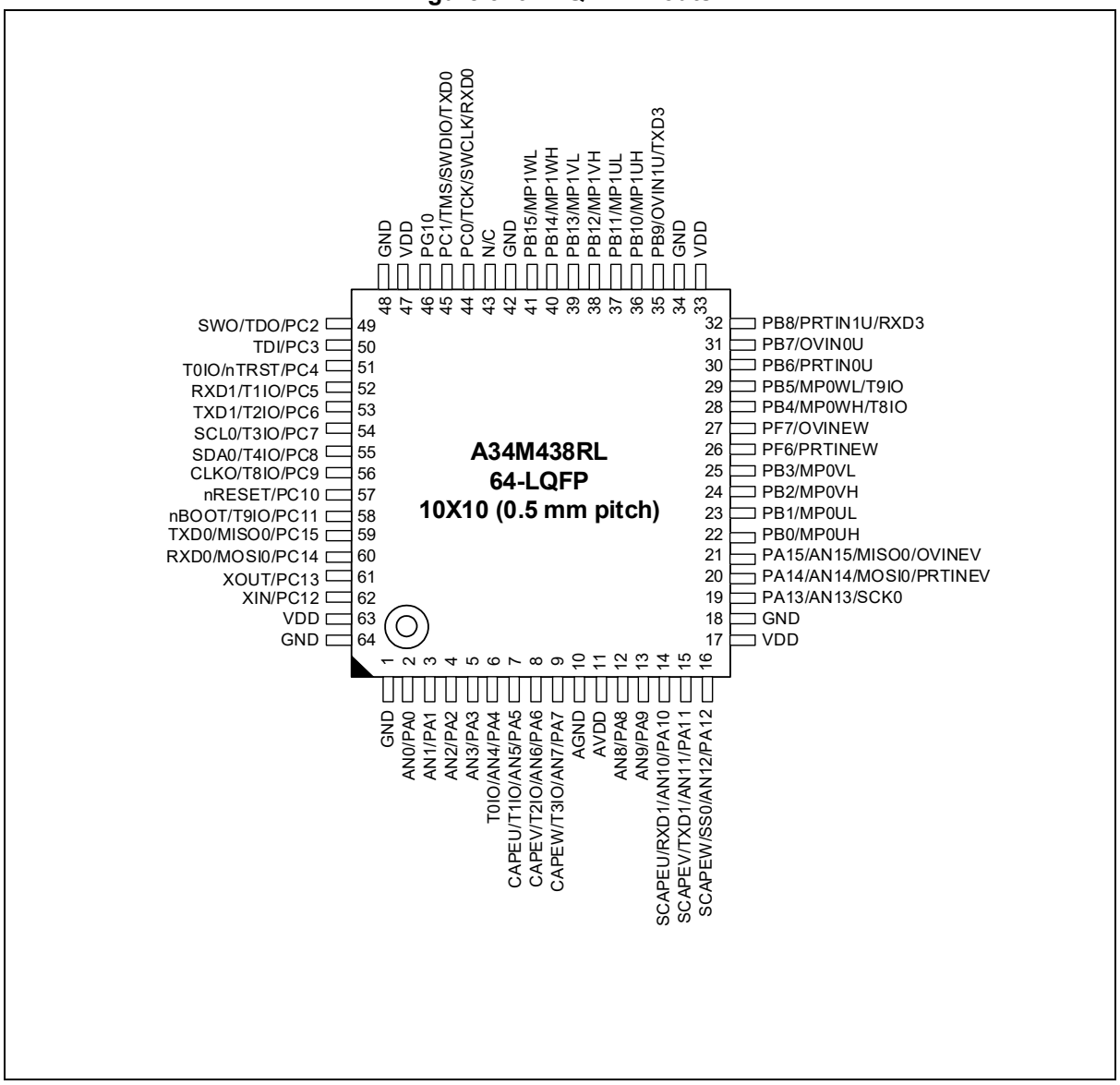
3.1.1 A34M438VL (100-LQFP)

Figure 2. 100-LQFP Pinouts



3.1.2 A34M438RL (64-LQFP)

Figure 3. 64-LQFP Pinouts



3.2 Pin Description

Table 8. Legend and Abbreviations Used in Pin Description

Name	Abbreviation	Definition
Pin Name	• Pin name is always the same. • Users can set a function on the pin using the alternate function.	
Notes	1. I = Input, O = Output, U = Pull-up, D = Pull-down, S = Schmitt-Trigger Input Type, C = CMOS Input Type, A = Analog, P = Power 2. After a reset, all the pins are configured to function defined by their initial values. The initial value of the pin depends on the package type. This configuration is in compliance with the 120-pin standard. 3. nBOOT, nRESET, PC1 (SWDIO), PC0 (SWCLK), PC3 and PC4 are the default pull-up pins. 4. Do not configure unused pins as floating inputs. (low output is recommended). 5. After a reset, the internal pull-up for the boot pin is enabled. 6. After a reset, the internal pull-up for the serial wire clock (SWCLK) and the serial wire data I/O (SWDIO) is enabled. 7. The SWCLK and SWDIO pins should not be switched to other functions while they are being used. 8. PC7, PC8, PD4, PD5, PE3, PE4, PE11, PE12 pins are open-drain ports. 9. When the PC12 (XIN), PC13 (XOUT), PD1 (SXOUT), and PD0 (SXIN) pins are configured for a function other than a clock, and if the clock is enabled by software, the other functions may not operate normally.	
Pin Function	Alternate Functions	Functions selected through Pn_MR1/2 (PORT n MUX1/2 select register) registers

Pin configuration information in Table 9 contains two pairs of power/ground and other dedicated pins. These multi-function pins have up to five selections of functions including GPIO. The Configuration including pin ordering can be changed without notice.

Table 9. Pin Description

Pin No.		Pin Name	Type	Description	Remark
100-pin	64-pin				
1	1	GND	P	Ground	
2	-	PD2	IOUS	PORT D bit 2 input/output	
		MOSI1	IO	SPI channel 1 MOSI (Master out/Slave in) signal	
3	-	PD3	IOUS	PORT D bit 3 input/output	
		MISO1	IO	SPI channel 1 MISO (Master in/Slave out) signal	
4	-	PE0	IOUS	PORT E bit 0 input/output	
5	-	PE1	IOUS	PORT E bit 1 input/output	
		AN20(2)	IA	Analog input 20	
6	-	PE2	IOUS	PORT E bit 2 input/output	
		AN21(2)	IA	Analog input 21	
7	-	PF2	IOUS	PORT F bit 2 input/output	
		AN22(2)	IA	Analog input 22	
8	-	PF3	IOUS	PORT F bit 3 input/output	
		AN23(2)	IA	Analog input 23	
9	2	PA0	IOUS	PORT A bit 0 input/output	
		AN0(2)	IA	Analog input 0	
10	3	PA1	IOUS	PORT A bit 1 input/output	
		AN1(2)	IA	Analog input 1	
11	4	PA2	IOUS	PORT A bit 2 input/output	
		AN2(2)	IA	Analog input 2	
12	5	PA3	IOUS	PORT A bit 3 input/output	
		AN3(2)	IA	Analog input 3	
13	6	PA4	IOUS	PORT A bit 4 input/output	
		AN4(2)	IA	Analog input 4	
		T0IO	IO	Timer 0 input/output	

Table 9. Pin Description (continued)

Pin No.		Pin Name	Type[1]	Description	Remark
100-pin	64-pin				
14	7	PA5	IOUS	PORT A bit 5 input/output	
		AN5[2]	IA	Analog input 5	
		T1IO	IO	Timer 1 input/output	
		CAPEU	Input	Individual PWM capture U phase	
15	8	PA6	IOUS	PORT A bit 6 input/output	
		AN6[2]	IA	Analog input 6	
		T2IO	IO	Timer 2 input/output	
		CAPEV	Input	Individual PWM capture V phase	
16	9	PA7	IOUS	PORT A bit 7 input/output	
		AN7[2]	IA	Analog input 7	
		T3IO	IO	Timer 3 input/output	
		CAPEW	Input	Individual PWM capture W phase	
17	10	AGND	P	Analog Ground	
18	11	AVDD	P	Analog VDD	
19	12	PA8	IOUS	PORT A bit 8 input/output	
		AN8[2]	IA	Analog input 8	
20	13	PA9	IOUS	PORT A bit 9 input/output	
		AN9[2]	IA	Analog input 9	
21	14	PA10	IOUS	PORT A bit 10 input/output	
		AN10[2]	IA	Analog input 10	
		RXD1	Input	UART channel 1 RXD input	
		SCAPEU	Input	Individual PWM sub capture U phase	
22	15	PA11	IOUS	PORT A bit 11 input/output	
		AN11[2]	IA	Analog input 11	
		TXD1	Output	UART channel 1 TXD output	
		SCAPEV	Input	Individual PWM sub capture V phase	
23	16	PA12	IOUS	PORT A bit 12 input/output	
		AN12[2]	IA	Analog input 12	
		SS0	IO	SPI channel 0 select signal input/output	
		SCAPEW	Input	Individual PWM sub capture W phase	
24	-	PD4	IOUS	PORT D bit 4 input/output	
		AN16[2]	IA	Analog input 16	
		SCL1[9]	IO	I2C channel 1 SCL input/output	Open-drain
25	-	PD5	IOUS	PORT D bit 5 input/output	
		AN17[2]	IA	Analog input 17	
		SDA1[9]	IO	I2C channel 1 SDA input/output	Open-drain
26	17	VDD	P	VDD	
27	18	GND	P	Ground	

Table 9. Pin Description (continued)

Pin No.		Pin Name	Type[1]	Description	Remark
100-pin	64-pin				
28	-	PD6	IOUS	PORT D bit 6 input/output	
		AN18[2]	IA	Analog input 18	
		TXD2	Output	UART channel 2 TXD output	
29	-	PD7	IOUS	PORT D bit 7 input/output	
		AN19[2]	IA	Analog input 19	
		RXD2	Input	UART channel 2 RXD input	
30	19	PA13	IOUS	PORT A bit 13 input/output	
		AN13[2]	IA	Analog input 13	
		SCK0	IO	SPI channel 0 clock input/output	
31	20	PA14	IOUS	PORT A bit 14 input/output	
		AN14[2]	IA	Analog input 14	
		MOSI0	IO	SPI channel 0 MOSI (Master put/Slave in signal)	
		PRTINEV	Input	Individual PWM phase V protection input	
32	21	PA15	IOUS	PORT A bit 15 input/output	
		AN15[2]	IA	Analog input 15	
		MISO0	IO	SPI channel 0 MISO (Master in/Slave out signal)	
		OVINEV	Input	Individual PWM phase V over-voltage input	
33	22	PB0	IOUS	PORT B bit 0 input/output	
		MP0UH	Output	PWM0 UH output	
34	23	PB1	IOUS	PORT B bit 1 input/output	
		MP0UL	Output	PWM channel 0 UL output	
35	24	PB2	IOUS	PORT B bit 2 input/output	
		MP0VH	Output	PWM channel 0 VH output	
36	25	PB3	IOUS	PORT B bit 3 input/output	
		MP0VL	Output	PWM channel 0 VL output	
37	-	PF4	IOUS	PORT F bit 4 input/output	
		TXD5	Output	UART channel 5 TXD output	
38	-	PF5	IOUS	PORT F bit 5 input/output	
		RXD5	Input	UART channel 5 RXD input	
39	-	PE3	IOUS	PORT E bit 3 input/output	
		SCL0[9]	IO	I2C channel 0 SCL input/output	Open-drain
40	-	PE4	IOUS	PORT E bit 4 input/output	
		SDA0[9]	IO	I2C channel 0 SDA input/output	Open-drain
41	-	PE5	IOUS	PORT E bit 5 input/output	
		T5IO	IO	Timer 5 input/output	
42	26	PF6	IOUS	PORT F bit 6 input/output	
		PRTINEW	Input	Individual PWM phase W protection input	
43	27	PF7	IOUS	PORT F bit 7 input/output	
		OVINEW	Input	Individual PWM phase W over-voltage input	
44	28	PB4	IOUS	PORT B bit 4 input/output	
		MP0WH	Output	PWM channel 0 WH output	
		T8IO	IO	Timer 8 input/output	

Table 9. Pin Description (continued)

Pin No.		Pin Name	Type[1]	Description	Remark
100-pin	64-pin				
45	29	PB5	IOUS	PORT B bit 5 input/output	
		MP0WL	Output	PWM channel 0 WL output	
		T9IO	IO	Timer 9 input/output	
46	30	PB6	IOUS	PORT B bit 6 input/output	
		PRTIN0U	Input	PWM0 Protection input Signal Individual PWM 0 Phase U Protection input	
47	31	PB7	IOUS	PORT B bit 7 input/output	
		OVIN0U	Input	PWM0 Over-voltage input Signal Individual PWM 0 Phase U Over voltage input	
48	32	PB8	IOUS	PORT B bit 8 input/output	
		PRTIN1U	Input	PWM1 Protection input Signal Individual PWM 1 Phase U Protection input	
		RXD3	Input	UART channel 3 RXD input	
49	-	PD8	IOUS	PORT D bit 8 input/output	
		T6IO	IO	Timer 6 input/output	
		WDTO	Output	WDT output	
50	-	PD9	IOUS	PORT D bit 9 input/output	
		T7IO	IO	Timer 7 input/output	
		STBYO	Output	Power-down Mode Indication Signal	
51	33	VDD	P	VDD	
52	34	GND	P	Ground	
53	35	PB9	IOUS	PORT B bit 9 input/output	
		OVIN1U	Input	PWM1 Overvoltage input Signal Individual PWM 1 Phase U Over voltage input	
		TXD3	Output	UART channel 3 TXD output	
54	36	PB10	IOUS	PORT B bit 10 input/output	
		MP1UH	Output	PWM channel 1 UH output	
55	37	PB11	IOUS	PORT B bit 11 input/output	
		MP1UL	Output	PWM channel 1 UL output	
56	38	PB12	IOUS	PORT B bit 12 input/output	
		MP1VH	Output	PWM channel 1 VH output	
57	39	PB13	IOUS	PORT B bit 13 input/output	
		MP1VL	Output	PWM channel 1 VL output	
58	40	PB14	IOUS	PORT B bit 14 input/output	
		MP1WH	Output	PWM channel 1 WH output	
59	41	PB15	IOUS	PORT B bit 15 input/output	
		MP1WL	Output	PWM channel 1 WL output	
60	-	PF0	IOUS	PORT F bit 0 input/output	
61	-	PF1	IOUS	PORT F bit 1 input/output	

Table 9. Pin Description (continued)

Pin No.		Pin Name	Type[1]	Description	Remark
100-pin	64-pin				
-	42	GND	P	Ground	
-	43	N/C	-	N/C	
62	44	PC0	IOUS	PORT C bit 0 input/output	
		TCK/SWCLK[2][3][6][7]	Input	JTAG TCK, SWD clock input	Pull-up
		RXD0	Input	UART channel 0 RXD input	
63	45	PC1	IOUS	PORT C bit 1 input/output	
		TMS/SWDIO[2][3][6][7]	IO	JTAG TMS, SWD data input/output	Pull-up
		TXD0	Output	UART channel 0 TXD output	
64	-	PE6	IOUS	PORT E bit 6 input/output	
		T5IO	IO	Timer 5 input/output	
65	-	PE7	IOUS	PORT E bit 7 input/output	
		T6IO	IO	Timer 6 input/output	
66	-	PE8	IOUS	PORT E bit 8 input/output	
		T7IO	IO	Timer 7 input/output	
67	-	PE9	IOUS	PORT E bit 9 input/output	
		T8IO	IO	Timer 8 input/output	
68	-	PE10	IOUS	PORT E bit 10 input/output	
		T9IO	IO	Timer 9 input/output	
69	-	PD10	IOUS	PORT D bit 10 input/output	
		T0IO	IO	Timer 0 input/output	
70	-	PD11	IOUS	PORT D bit 11 input/output	
		T1IO	IO	Timer 1 input/output	
71	46	PG10	IOUS	PORT G bit 10 input/output	
72	-	PD12	IOUS	PORT D bit 12 input/output	
		T2IO	IO	Timer 2 input/output	
73	-	PD13	IOUS	PORT D bit 13 input/output	
		T3IO	IO	Timer 3 input/output	

Table 9. Pin Description (continued)

Pin No.		Pin Name	Type[1]	Description	Remark
100-pin	64-pin				
74	47	VDD	P	VDD	
75	48	GND	P	Ground	
76	49	PC2	IOUS	PORT C bit 2 input/output	
		TDO/SWO[2]	Output	JTAG TDO output, Serial Wire Output	Output Low
77	50	PC3	IOUS	PORT C bit 3 input/output	
		TDI[2]	Input	JTAG TDI input	Pull-up
78	51	PC4	IOUS	PORT C bit 4 input/output	
		nTRST[2]	Input	JTAG nTRST input	Pull-up
		T0IO	IO	Timer 0 input/output	
79	52	PC5	IOUS	PORT C bit 5 input/output	
		T1IO	IO	Timer 1 input/output	
		RXD1	Input	UART channel 1 RXD input	
80	53	PC6	IOUS	PORT C bit 6 input/output	
		T2IO	IO	Timer 2 input/output	
		TXD1	Output	UART channel 1 TXD output	
81	54	PC7	IOUS	PORT C bit 7 input/output	
		T3IO	IO	Timer 3 input/output	
		SCL0[9]	IO	I2C channel 0 SCL input/output	Open-drain
82	55	PC8	IOUS	PORT C bit 8 input/output	
		T4IO	IO	Timer 4 input/output	
		SDA0[9]	IO	I2C channel 0 SDA input/output	Open-drain
83	56	PC9	IOUS	PORT C bit 9 input/output	
		T8IO	IO	Timer 8 input/output	
		CLKO	Output	System Clock output	
84	57	PC10	IOUS	PORT C bit 10 input/output	
		nRESET[2][3]	Input	External Reset input	Pull-up
85	58	PC11	IOUS	PORT C bit 11 input/output	
		T9IO	IO	Timer 9 input/output	
		nBOOT[2][3][5]	Input	Boot Mode Selection input	Pull-up
86	-	PE11	IOUS	PORT E bit 11 input/output	
		SCL1[9]	IO	I2C channel 1 SCL input/output	Open-drain
		T0IO	IO	Timer 0 input/output	
87	-	PE12	IOUS	PORT E bit 12 input/output	
		SDA1[9]	IO	I2C channel 1 SDA input/output	Open-drain
		T1IO	IO	Timer 1 input/output	
88	-	PE13	IOUS	PORT E bit 13 input/output	
		TXD4	Output	UART channel 4 TXD output	
		T2IO	IO	Timer 2 input/output	

Table 9. Pin Description (continued)

Pin No.		Pin Name	Type[1]	Description	Remark
100-pin	64-pin				
89	-	PE14	IOUS	PORT E bit 14 input/output	
		RXD4	Input	UART channel 4 RXD input	
		T3IO	IO	Timer 3 input/output	
90	-	PE15	IOUS	PORT E bit 15 input/output	
91	-	PD14	IOUS	PORT D bit 14 input/output	
		SS0	IO	SPI channel 0 select signal input/output	
92	-	PD15	IOUS	PORT D bit 15 input/output	
		SCK0	IO	SPI channel 0 clock input/output	
93	59	PC15	IOUS	PORT C bit 15 input/output	
		MISO0	IO	SPI channel 0 MISO (Master in/Slave out) signal	
		TXD0	Output	UART channel 0 TXD output	
94	60	PC14	IOUS	PORT C bit 14 input/output	
		MOSI0	IO	SPI channel 0 MOSI (Master out/Slave in) signal	
		RXD0	Input	UART channel 0 RXD input	
95	61	PC13	IOUS	PORT C bit 13 input/output	
		XOUT[2][9]	OA	External crystal oscillator output	
96	62	PC12	IOUS	PORT C bit 12 input/output	
		XIN[2][9]	IA	External crystal oscillator input	
97	-	PD0	IOUS	PORT D bit 0 input/output	
		SXIN[2][9]	IA	Sub crystal oscillator input	
		SS1	IO	SPI channel 1 select signal input/output	
98	-	PD1	IOUS	PORT D bit 1 input/output	
		SXOUT[2][9]	OA	Sub crystal oscillator output	
		SCK1	IO	SPI channel 1 clock input/output	
99	63	VDD	P	VDD	
100	64	GND	P	Ground	

NOTES:

1. I = Input, O = Output, U = Pull-up, D = Pull-down, S = Schmitt-Trigger Input Type, C = CMOS Input Type, A = Analog, P = Power
2. After a reset, all the pins are configured to function defined by their initial values. The initial value of the pin depends on the package type. This configuration is in compliance with the 100-pin standard.
3. nBOOT, nRESET, PC1 (SWDIO), PC0 (SWCLK), PC3 and PC4 are the default pull-up pins.
4. Do not configure unused pins as floating inputs.
5. After a reset, the internal pull-up for the boot pin is enabled.
6. After a reset, the internal pull-up for the serial wire clock (SWCLK) and the serial wire data I/O (SWDIO) is enabled.
7. The SWCLK and SWDIO pins should not be switched to other functions while they are being used.
8. PC7, PC8, PD4, PD5, PE3, PE4, PE11, and PE12 pins are configured as open-drain ports when used as I2C ports.
9. When the PC12 (XIN), PC13 (XOUT), PD1 (SXOUT), and PD0 (SXIN) pins are configured for a function other than a clock, and if the clock is enabled by software, the other functions may not operate normally.

3.3 Alternate Function Pins

GPIO pins have alternate functions as described in Table 10.

Table 10. GPIO Alternate Function

Pin Name	Alternate Function				
	AF0	AF1	AF2	AF3	AF7
PA0	PA0				AN0(1)
PA1	PA1				AN1(1)
PA2	PA2				AN2(1)
PA3	PA3				AN3(1)
PA4	PA4		T0IO		AN4 (1)
PA5	PA5		T1IO	CAPEU	AN5 (1)
PA6	PA6		T2IO	CAPEV	AN6 (1)
PA7	PA7		T3IO	CAPEW	AN7 (1)
PA8	PA8				AN8 (1)
PA9	PA9				AN9 (1)
PA10	PA10	RXD1		SCAPEU	AN10 (1)
PA11	PA11	TXD1		SCAPEV	AN11 (1)
PA12	PA12	SS0		SCAPEW	AN12(1)
PA13	PA13	SCK0			AN13(1)
PA14	PA14	MOSI0		PRTINEV	AN14(1)
PA15	PA15	MISO0		OVINEV	AN15(1)
PB0	PB0			MP0UH	(1)
PB1	PB1			MP0UL	(1)
PB2	PB2			MP0VH	(1)
PB3	PB3			MP0VL	(1)
PB4	PB4		T8IO	MP0WH	(1)
PB5	PB5		T9IO	MP0WL	(1)
PB6	PB6			PRTIN0U	(1)
PB7	PB7			OVIN0U	(1)
PB8	PB8	RXD3		PRTIN1U	(1)
PB9	PB9	TXD3		OVIN1U	(1)
PB10	PB10			MP1UH	(1)
PB11	PB11			MP1UL	(1)
PB12	PB12			MP1VH	(1)
PB13	PB13			MP1VL	(1)
PB14	PB14			MP1WH	(1)
PB15	PB15			MP1WL	(1)
PC0	PC0	RXD0		TCK/SWCLK(1)	
PC1	PC1	TXD0		TMS/SWDIO(1)	
PC2	PC2			TDO/SWO(1)	
PC3	PC3			TDI(1)	
PC4	PC4		T0IO	nTRST(1)	
PC5	PC5	RXD1	T1IO		(1)
PC6	PC6	TXD1	T2IO		(1)
PC7	PC7	SCL0	T3IO		(1)
PC8	PC8	SDA0	T4IO		(1)
PC9	PC9		T8IO	CLKO	(1)

Table 10. GPIO Alternate Function (continued)

Pin Name	Alternate Function				
	AF0	AF1	AF2	AF3	AF7
PC10	PC10			nRESET(1)	
PC11	PC11		T9IO	nBOOT(1)	
PC12	PC12				XIN(1)
PC13	PC13				XOUT(1)
PC14	PC14	MOSI0		RXD0	(1)
PC15	PC15	MISO0		TXD0	(1)
PD0	PD0	SS1			SXIN(1)
PD1	PD1	SCK1			SXOUT(1)
PD2	PD2	MOSI1			(1)
PD3	PD3	MISO1			(1)
PD4	PD4	SCL1			AN16(1)
PD5	PD5	SDA1			AN17(1)
PD6	PD6	TXD2			AN18(1)
PD7	PD7	RXD2			AN19(1)
PD8	PD8		T6IO	WDTO	(1)
PD9	PD9		T7IO	STBYO	(1)
PD10	PD10		T0IO		(1)
PD11	PD11		T1IO		(1)
PD12	PD12		T2IO		(1)
PD13	PD13		T3IO		(1)
PD14	PD14	SS0			(1)
PD15	PD15	SCK0			(1)
PE0	PE0				(1)
PE1	PE1				AN20(1)
PE2	PE2				AN21(1)
PE3	PE3	SCL0			(1)
PE4	PE4	SDA0			(1)
PE5	PE5		T5IO		(1)
PE6	PE6		T5IO		(1)
PE7	PE7		T6IO		(1)
PE8	PE8		T7IO		(1)
PE9	PE9		T8IO		(1)
PE10	PE10		T9IO		(1)
PE11	PE11	SCL1	T0IO		(1)
PE12	PE12	SDA1	T1IO		(1)
PE13	PE13	TXD4	T2IO		(1)
PE14	PE14	RXD4	T3IO		(1)
PE15	PE15				(1)
PF0	PF0				(1)
PF1	PF1				(1)
PF2	PF2				AN22(1)
PF3	PF3				AN23(1)
PF4	PF4	TXD5			(1)
PF5	PF5	RXD5			(1)
PF6	PF6			PRTINEW	(1)
PF7	PF7			OVINEW	(1)

Table 10. GPIO Alternate Function (continued)

Pin Name	Alternate Function				
	AF0	AF1	AF2	AF3	AF7
PG10	PG10				(1)

NOTES:

1. It means ‘selected pin function after reset condition’.
2. Unused pins must be set to output by software (low output is recommended).

4. Electrical Characteristics

4.1 Parameter Conditions

Unless otherwise specified, all voltages are referenced to GND.

4.1.1 Minimum and Maximum Values

Unless otherwise specified, our production tests guarantee the minimum and maximum values of the device under the worst-case conditions including ambient temperature, supply voltage, and frequency.

Data based on characterization result, design simulation, and/or technical characteristics are not tested in production but are indicated in the table footnotes.

4.1.2 Typical Values

Unless otherwise specified, typical data are based on the conditions of T_A = 25°C and VDD = AVDD = 5.0 V. The typical data are provided only as design recommendations and are not tested.

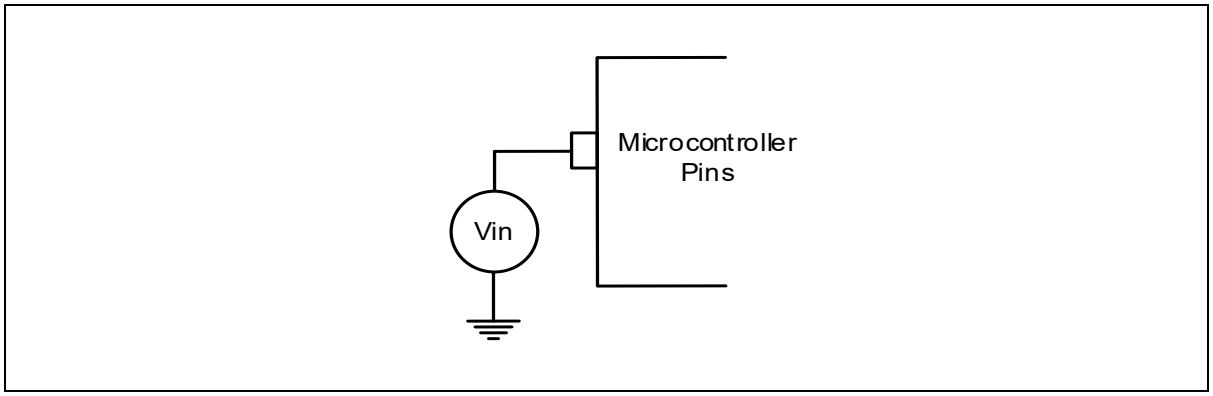
4.1.3 Typical Curves

Unless otherwise specified, all typical curves are provided only as design recommendations and are not tested.

4.1.4 Pin Input Voltage

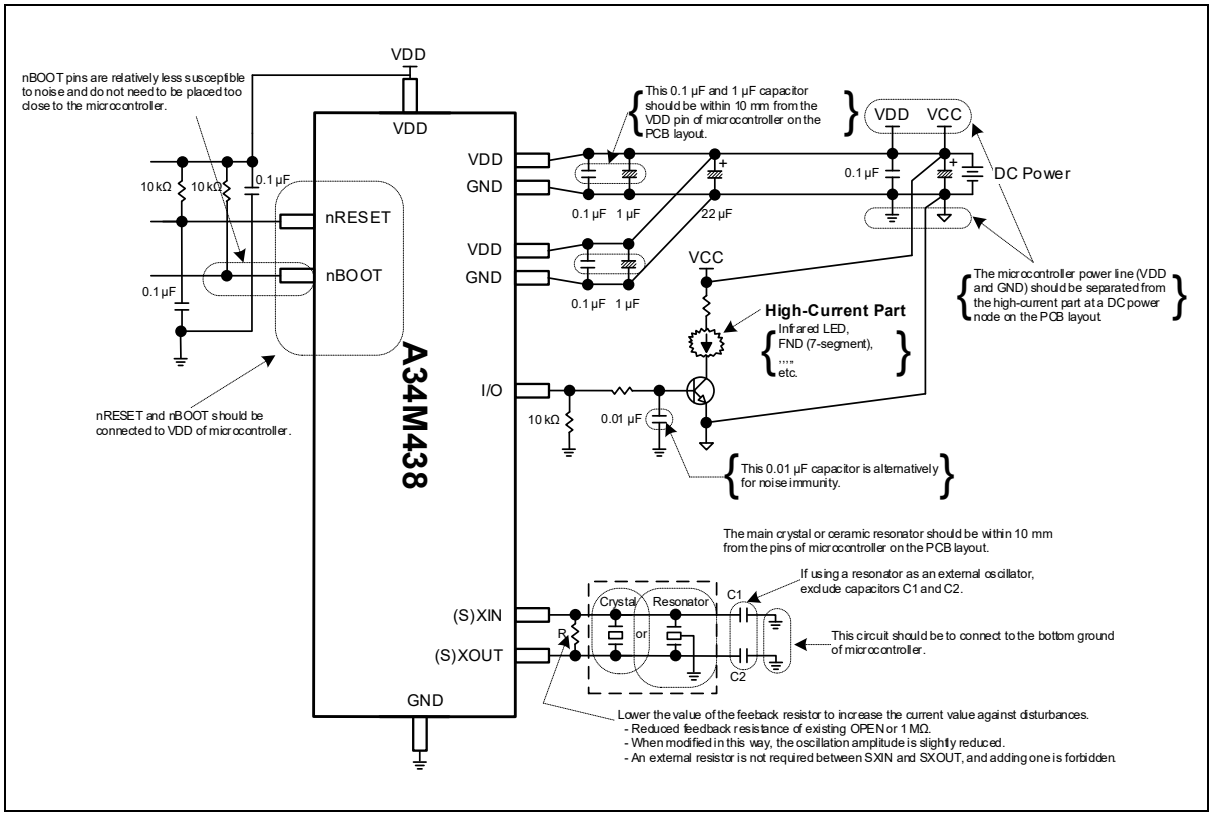
The input voltage measurement on a pin of the device is described in Figure 4.

Figure 4. Pin Input Voltage



4.1.5 Power Supply Scheme

Figure 5. Power Supply Scheme

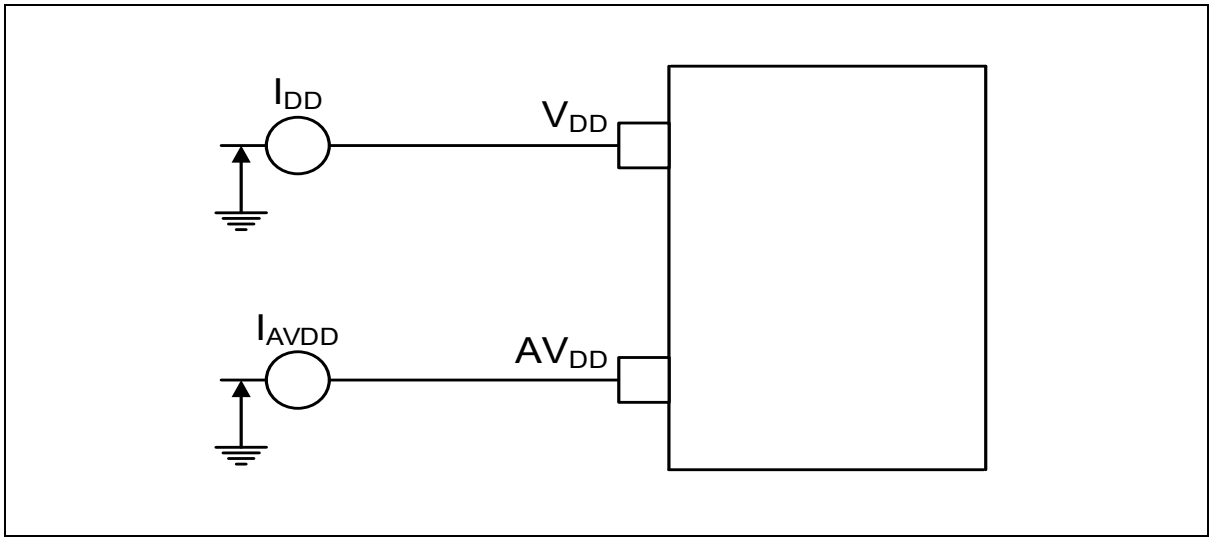


NOTE:

1. Each power supply pair (VDD, GND, etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

4.1.6 Current Consumption Measurement

Figure 6. Current Consumption Measurement



NOTE:

1. The I_{DD} and I_{AVDD} parameters represent the total microcontroller consumption including the current supplying V_{DD} and AV_{DD}.

4.2 Absolute Maximum Ratings

Exceeding stresses specified in the Table 11 for voltage characteristics, Table 12 for current characteristics, or Table 13 for thermal characteristics may result in permanent damage to the device. The values listed in the tables are stress ratings only, and do not imply that the device will function properly under these conditions. Prolonged exposure to these maximum rating conditions may impact on the reliability of the device. It is important to operate the device within its specified maximum ratings to ensure reliable performance.

Table 11. Voltage Characteristics

Symbol	Ratings	Min.	Max.	Unit
VDD − GND(1)	External main supply voltage (including V_{DD}, AV_{DD})	−0.5	6.0	V
V_I(2)	Input voltage on I/O	−0.5	Max (V_{DD}, AV_{DD}) + 0.5	V
V_O	Output voltage on I/O	−0.5	Max (V_{DD}, AV_{DD}) + 0.5	V

NOTES:

1. All main power (VDD, AVDD) and ground (GND, AGND) pins must always be connected to the external power supply, within the permitted range.
2. V_I maximum must always be respected.

Table 12. Current Characteristics

Symbol	Ratings	Max.	Unit
$\sum I_{VDD}$	Total current into sum of all V_{DD} power lines (source)(1)	TBD	mA
$\sum I_{GND}$	Total current out of sum of all GND ground lines (sink)(1)	TBD	mA
$I_{VDD(PIN)}$	Maximum current into each V_{DD} power pin (source)(1)	TBD	mA
$I_{GND(PIN)}$	Maximum current out of each GND ground pin (sink)(1)	TBD	mA
$I_{IO(PIN)}$	Output current sunk by any I/O	TBD	mA
	Output current sourced by any I/O and control pin	TBD	mA
$\sum I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	TBD	mA
	Total output current sourced by sum of all I/Os and control pins(2)	TBD	mA
I_{IL}	Input low leakage current	−1	µA
I_{IH}	Input high leakage current	1	µA
P_T	Total power dissipation	600	mW

NOTES:

1. All main power (V_{DD}, AV_{DD}) and ground (GND, AGND) pins must always be connected to the external power supplies, within the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.

Table 13. Thermal Characteristics

Symbol	Ratings	Value	Unit
T_{OP}	Operating temperature	−40 to +85	°C
T_{STG}	Storage temperature range	−55 to +125	°C
T_J	Maximum junction temperature	+105	°C

4.3 Operating Condition

4.3.1 General Operating Condition

Table 14. General Operating Condition

(Temperature: −40°C to +85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	-	2.7(1)	-	5.5	V
AV_{DD}	Analog supply voltage	ADC used	2.7	-	5.5	V
f	Operating frequency	HSE	4	-	16	MHz
		LSE	-	32.768	-	kHz
		HSI	31.04	32.00	32.96	MHz
		LSI	400	500	600	kHz
V_{IN}	I/O input voltage	5 V I/O	−0.3	-	VDD	V
T_A	Ambient temperature	-	−40	-	85	°C
T_J	Junction temperature range	-	-	-	105	°C

NOTE:

1. When RESET is released, functionality is guaranteed down to V_{LVR0} Min.

4.3.2 Power-On Reset Characteristics

Table 15. POR Electrical Characteristics

(Temperature: −40°C to +85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{DD}	Operating current	-	-	5	12	μA
V_{set}	POR set level	-	1.4	1.65	1.9	V
V_{reset}	POR reset level	-	1.3	1.5	1.7	V
t_R	VDD voltage rising time	-	0.02	-	20	ms/V
t_F	VDD voltage falling time	-	0.4	-	20	ms/V

4.3.3 Operating Condition at Power-Up/Power-Down

The parameters in Table 16 are derived from tests performed under the ambient temperature conditions summarized in Table 14.

Table 16. Operating Condition at Power-Up and Power-Down

(Temperature: −40°C to +85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{VDD}	V_{DD} rise time rate	-	0.02	-	20	ms/V
	V_{DD} fall time rate	-	0.4	-	20	ms/V

4.3.4 Embedded Reset and Power Control Block Characteristics (LVR, LVI)

The parameters in Table 17 and Table 18 are derived from tests performed under the ambient temperature conditions summarized in Table 14.

Table 17. Low-Voltage Reset Characteristics

(Temperature: −40°C to +85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{LVR0_F}	Detection level	Falling voltage	1.52	1.60	1.68	V
V_{LVR1_F}			1.61	1.69	1.77	
V_{LVR2_F}			1.69	1.78	1.87	
V_{LVR3_F}			1.81	1.90	2.00	
V_{LVR4_F}			1.89	1.99	2.09	
V_{LVR5_F}			1.95	2.12	2.23	
V_{LVR6_F}			2.19	2.30	2.42	
V_{LVR7_F}			2.35	2.47	2.59	
V_{LVR8_F}			2.54	2.67	2.80	
V_{LVR9_F}			2.89	3.04	3.19	
V_{LVR10_F}			3.02	3.18	3.34	
V_{LVR11_F}			3.41	3.59	3.77	
V_{LVR12_F}			3.53	3.72	3.91	
V_{LVR13_F}			3.83	4.03	4.23	
V_{LVR14_F}			3.99	4.20	4.41	
V_{LVR15_F}			4.26	4.48	4.70	
V_{LVR0_R}	Detection level	Rising voltage	1.58	1.66	1.74	V
V_{LVR1_R}			1.66	1.75	1.84	
V_{LVR2_R}			1.76	1.85	1.94	
V_{LVR3_R}			1.87	1.97	2.07	
V_{LVR4_R}			1.97	2.07	2.17	
V_{LVR5_R}			2.00	2.20	2.40	
V_{LVR6_R}			2.26	2.38	2.50	
V_{LVR7_R}			2.43	2.56	2.69	
V_{LVR8_R}			2.63	2.77	2.91	
V_{LVR9_R}			2.99	3.15	3.31	
V_{LVR10_R}			3.14	3.30	3.47	
V_{LVR11_R}			3.53	3.72	3.91	
V_{LVR12_R}			3.67	3.86	4.05	
V_{LVR13_R}			3.97	4.18	4.39	
V_{LVR14_R}			4.14	4.36	4.58	
V_{LVR15_R}			4.41	4.64	4.87	
-	Hysteresis	-	-	75	200	mV
-	Noise cancelling time	-	-	2	-	μs
I_{DD}	Operation current	-	-	3.5	5	μA
$I_{DD,\ STOP}$	Operation current (STOP)	-	-	5	250	nA

Table 18. Low-Voltage Indicator Characteristics

(Temperature: −40°C to +85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{LVI0_F}	Detection level	Falling voltage	1.52	1.60	1.68	V
V_{LVI1_F}			1.61	1.69	1.77	
V_{LVI2_F}			1.69	1.78	1.87	
V_{LVI3_F}			1.81	1.90	2.00	
V_{LVI4_F}			1.89	1.99	2.09	
V_{LVI5_F}			1.95	2.12	2.23	
V_{LVI6_F}			2.19	2.30	2.42	
V_{LVI7_F}			2.35	2.47	2.59	
V_{LVI8_F}			2.54	2.67	2.80	
V_{LVI9_F}			2.89	3.04	3.19	
V_{LVI10_F}			3.02	3.18	3.34	
V_{LVI11_F}			3.41	3.59	3.77	
V_{LVI12_F}			3.53	3.72	3.91	
V_{LVI13_F}			3.83	4.03	4.23	
V_{LVI14_F}			3.99	4.20	4.41	
V_{LVI15_F}			4.26	4.48	4.70	
V_{LVI0_R}	Detection level	Rising voltage	1.58	1.66	1.74	V
V_{LVI1_R}			1.66	1.75	1.84	
V_{LVI2_R}			1.76	1.85	1.94	
V_{LVI3_R}			1.87	1.97	2.07	
V_{LVI4_R}			1.97	2.07	2.17	
V_{LVI5_R}			2.00	2.20	2.40	
V_{LVI6_R}			2.26	2.38	2.50	
V_{LVI7_R}			2.43	2.56	2.69	
V_{LVI8_R}			2.63	2.77	2.91	
V_{LVI9_R}			2.99	3.15	3.31	
V_{LVI10_R}			3.14	3.30	3.47	
V_{LVI11_R}			3.53	3.72	3.91	
V_{LVI12_R}			3.67	3.86	4.05	
V_{LVI13_R}			3.97	4.18	4.39	
V_{LVI14_R}			4.14	4.36	4.58	
V_{LVI15_R}			4.41	4.64	4.87	
-	Hysteresis	-	-	100	200	mV
-	Noise cancelling time	-	-	2	-	μs
I_{DD}	Operation current	-	-	3.5	5	μA
$I_{DD, STOP}$	Operation current (STOP)	-	-	5	250	nA

4.3.5 Supply Current Characteristics

The amount of current consumed by the device is determined by various factors and parameters, including but not limited to the operating voltage, ambient temperature, load on I/O pins, software configuration, operating frequency, switching rate of I/O pins, location of the program in memory, and the binary code being executed.

The current consumption is measured under the conditions specified in Table 19.

4.3.5.1 Supply Current Consumption

Table 19. Supply Current Characteristics

(Temperature: −40°C to +85°C)

Symbol	Operation Mode	Condition						Voltage Scaling	Typ.	Max.	Unit
		LSI (500 kHz)	HSI (32 MHz)	LSE (32.768 kHz)	HSE (8 MHz)	PLL (120 MHz)	f_{MCLK}				
I_{DD_RUN} (RUN)	Normal operation	STOP	RUN	STOP	STOP	STOP	f_{HSI}	5.0 V	12	-	mA
		STOP	STOP	STOP	RUN	STOP	f_{HSE}	5.0 V	4.5	-	
		STOP	STOP	STOP	RUN	RUN	f_{HSEPLL}	5.0 V	45	-	
		RUN	STOP	STOP	STOP	STOP	f_{LSI}	5.0 V	1.4	-	
		STOP	STOP	RUN	STOP	STOP	f_{LSE}	5.0 V	1.4	-	
I_{DD_SLEEP} (SLEEP)	SLEEP(1)	STOP	RUN	STOP	STOP	STOP	f_{HSI}	5.0 V	6.5	-	mA
		STOP	STOP	STOP	RUN	STOP	f_{HSE}	5.0 V	3.5	-	
		STOP	STOP	STOP	RUN	RUN	f_{HSEPLL}	5.0 V	23	-	
		RUN	STOP	STOP	STOP	STOP	f_{LSI}	5.0 V	1.3	-	
		STOP	STOP	RUN	STOP	STOP	f_{LSE}	5.0 V	1.3	-	
I_{DD_STOP2} (STOP 2)	DEEP-SLEEP(1)(2)	VDC (STOP), LVD (RUN)						5.0 V	260	7,500	µA
		VDC (STOP), LVD (STOP)						5.0 V	250	7,500	

NOTES:

1. All peripherals are turned off.
2. In DEEP-SLEEP mode, all clocks are disabled.

4.3.5.2 I/O System Current Consumption

The current consumption in the I/O system is due to the two components, Static and Dynamic.

4.3.5.3 I/O Static Current Consumption

All I/O pins used as inputs with pull-ups cause the current consumption when the pins remain Low from the outside. This current consumption value can be calculated simply using the pull-up/pull-down resistor value provided in the I/O port characteristics.

To estimate the current consumption at the output pins, users need to consider external Pull-downs or external load.

Additional I/O current consumption can be caused due to the I/Os configured as inputs if the medium voltage level is applied externally. This current is consumed by the input Schmitt-trigger circuit used to tell the input value. Unless the application requires a specific configuration, users can prevent this supply current consumption by configuring the I/Os in analog mode instead of using the Schmitt-trigger circuit. Specifically, input pins of the ADC, OPAMP, and CMP must be configured as analog inputs.

4.3.5.4 I/O Dynamic Current Consumption

The I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin.

4.3.6 External Clock Source Characteristics

4.3.6.1 High-Speed External Clock Generated from Crystal/Ceramic Resonator

A high-speed external clock (HSE) can be supplied with crystal/ceramic resonator oscillators in the range from 4 to 16 MHz. All information provided in this section is based on the design simulation results obtained by the typical external components specified in Table 20.

To minimize the outputs in the application, the resonator and load capacitor must be placed as close to the oscillator pin as possible.

For more information on the distortion and stabilization time, and the resonator characteristics (frequency, package, and accuracy), contact the manufacturer of the crystal resonator.

Table 20. HSE Oscillator Characteristics(1)

(Temperature: −40°C to +85°C)

Symbol	Parameter	Conditions(2)	Min.	Typ.	Max.	Unit
V_{DD}	Operating voltage	-	2.7	5.0	5.5	V
$I_{DD(HSE)}$	HSE current consumption	-	-	-	2.5	mA
I_{STOP}	Power down current	-	-	1	100	nA
f_{OSC_IN}	Oscillator frequency	-	4	8	16	MHz
f_{OUT}	Output Frequency	VDD ≥ 2.7 V(4)(5)(6)(7)	1	-	16	MHz
V_{IL}	Crystal input (low)	-	-	-	0.2×V_{DD}	V
V_{IH}	Crystal input (high)	-	0.8×V_{DD}	-	-	V
V_{OL}	Crystal out (low)	-	-	-	0.2×V_{DD}	V
V_{OH}	Crystal out (high)	-	0.8×V_{DD}	-	-	V
C_L	External Load Capacitor	1 MHz ≤ f_{OUT} ≤ 4 MHz	18	30	35	pF
		4 MHz ≤ f_{OUT} ≤ 12 MHz	10	22	30	pF
		12 MHz ≤ f_{OUT} ≤ 16 MHz	7	18	22	pF
R_F	Feedback resistor	VDD = 5 V	0.7	1.0	1.3	MΩ
$t_{SU(HSE)}$(3)	Startup time	-	-	1	-	ms

NOTES:

1. Guaranteed by design.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator, and it can vary significantly with the crystal manufacturer.
4. HSEISEL = 0x3, HSENFSEL = 0x0
5. HSEISEL = 0x2, HSENFSEL = 0x1
6. HSEISEL = 0x1, HSENFSEL = 0x2
7. HSEISEL = 0x0, HSENFSEL = 0x3

Figure 7. Crystal/Ceramic Oscillator

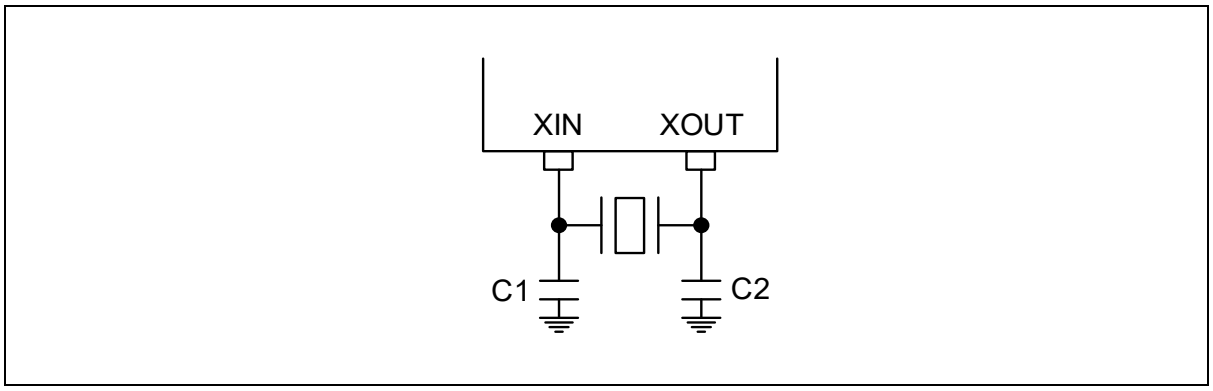


Figure 8. External Clock

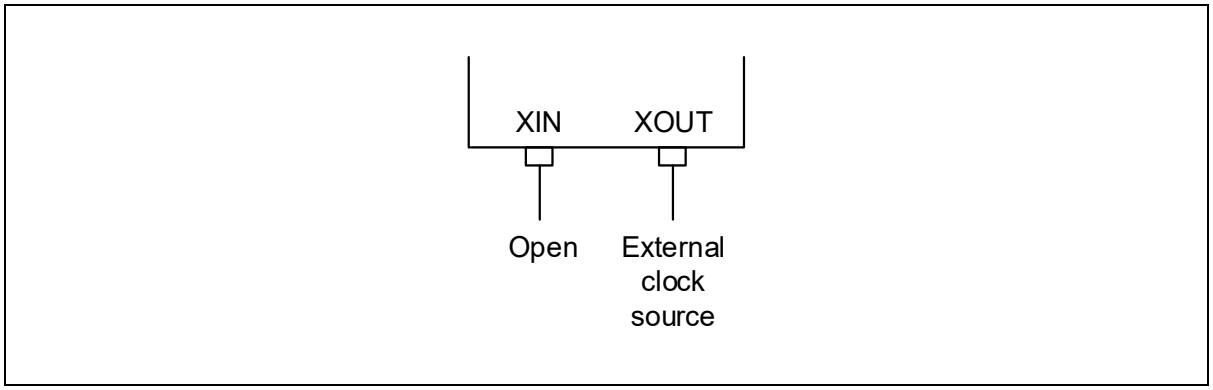
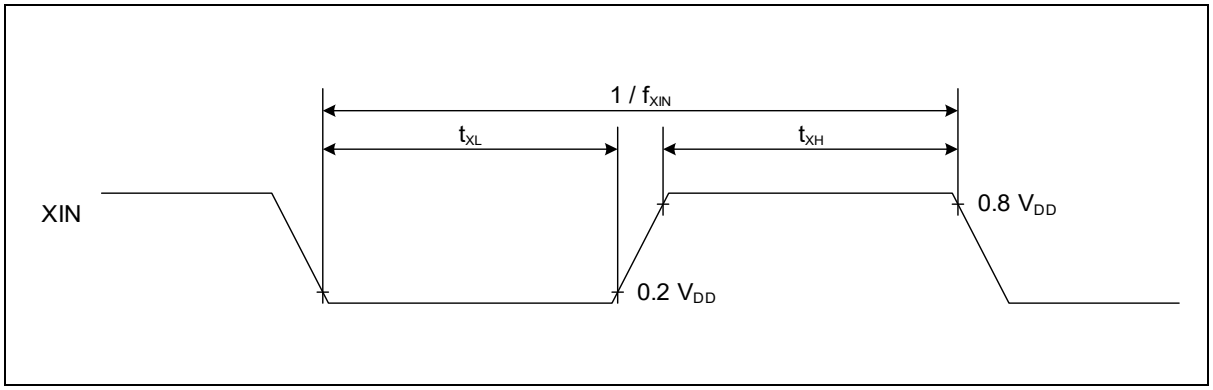


Figure 9. Clock Timing Measurement at XIN Pin

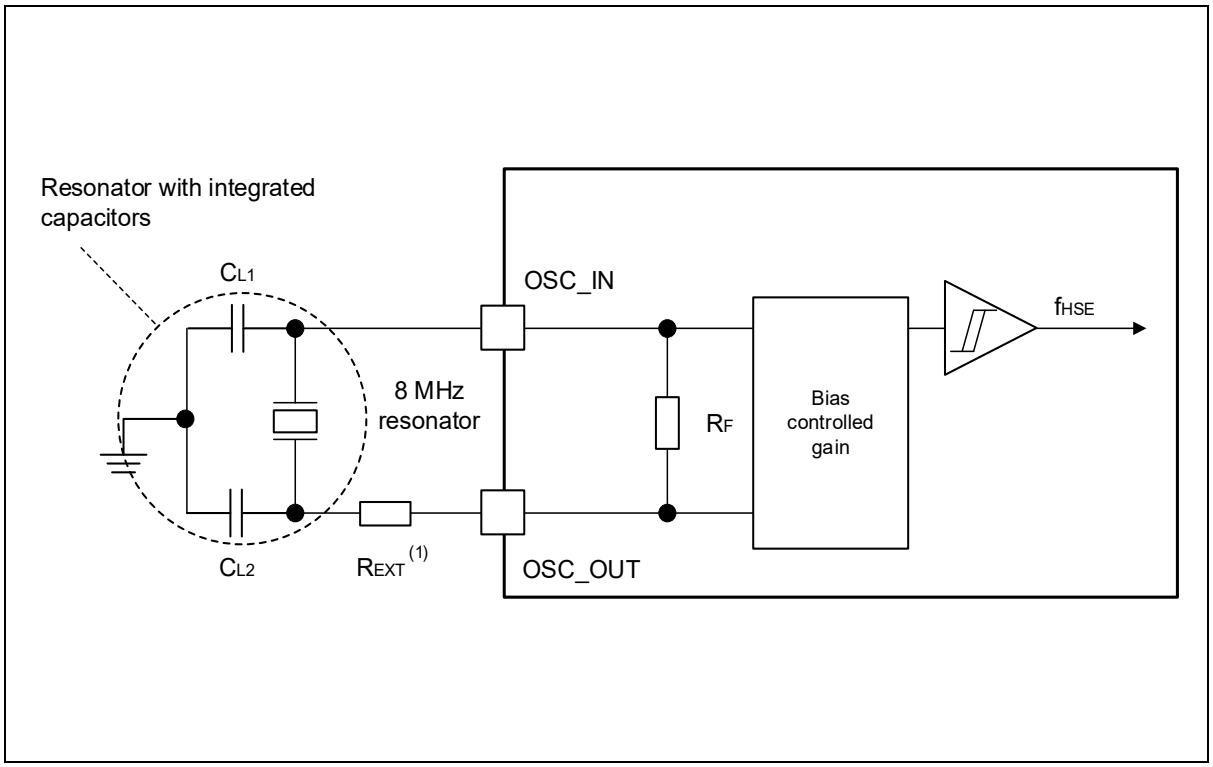


It is recommended to use high-quality external ceramic capacitors designed for high-frequency applications and selected to match the requirements of the crystal or resonator. The capacitance of the C_{L1} and C_{L2} capacitors should be between 5 pF to 20 pF.

The C_{L1} and C_{L2} capacitors are usually of the same size, and the crystal manufacturer typically specifies a load capacitance, which is the series combination of both capacitors. However, the capacitance of the printed circuit board (PCB) and microcontroller pin should also be considered, which must be included in the calculation of the overall capacitance.

Figure 10 shows a circuit diagram of a typical application with an 8 MHz crystal.

Figure 10. Typical Application with 8 MHz Crystal



4.3.6.2 Low-Speed External Clock Generated from Crystal Resonator

The low-speed external (LSE) clock can be generated using a crystal/ceramic resonator oscillator with 32.768 kHz. The information provided in this paragraph is based on characterization results obtained using typical external components listed in Table 21.

To minimize output distortion and startup stabilization time, it is recommended to place the resonator and load capacitors as close as possible to the oscillator pins in the application.

For further information on the resonator characteristics such as frequency, package, and accuracy, it is advisable to refer to the crystal resonator manufacturer.

Table 21. LSE Oscillator Characteristics(1) (f_{LSE} = 32.768 kHz)

(Temperature: −40°C to +85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating voltage	-	2.7	5.0	5.5	V
$I_{DD(LSE)}$	LSE current consumption	-	-	0.8	2	μA
I_{STOP}	Power down current	-	-	1	20	μA
f_{OSC_IN}	Oscillator frequency	-	-	32.768	-	kHz
C_L	External Load Capacitor	-	10	25	30	pF
R_F	Feedback resistor	-	5	11	20	MΩ
$t_{SU(LSE)}$(2)	Startup time	-	-	-	2.5	s

NOTES:

1. Guaranteed by design.
2. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal, and it can vary significantly with the crystal manufacturer.

Figure 11. Crystal Oscillator

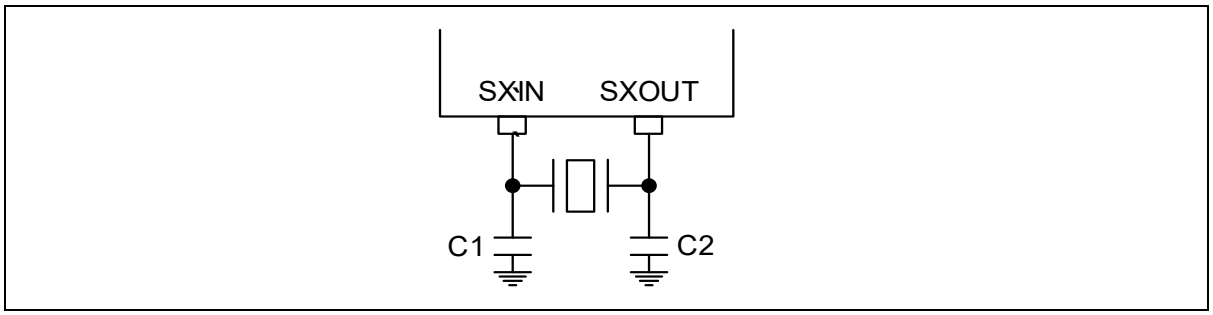


Figure 12. Clock Timing Measurement at SXIN Pin

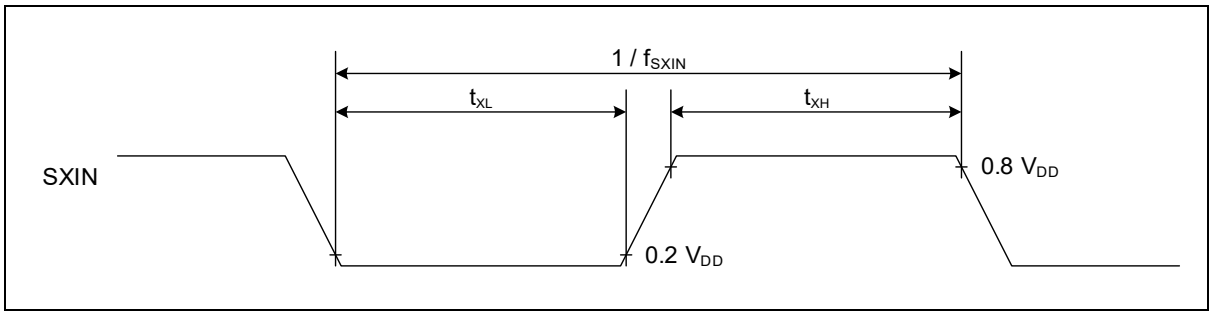
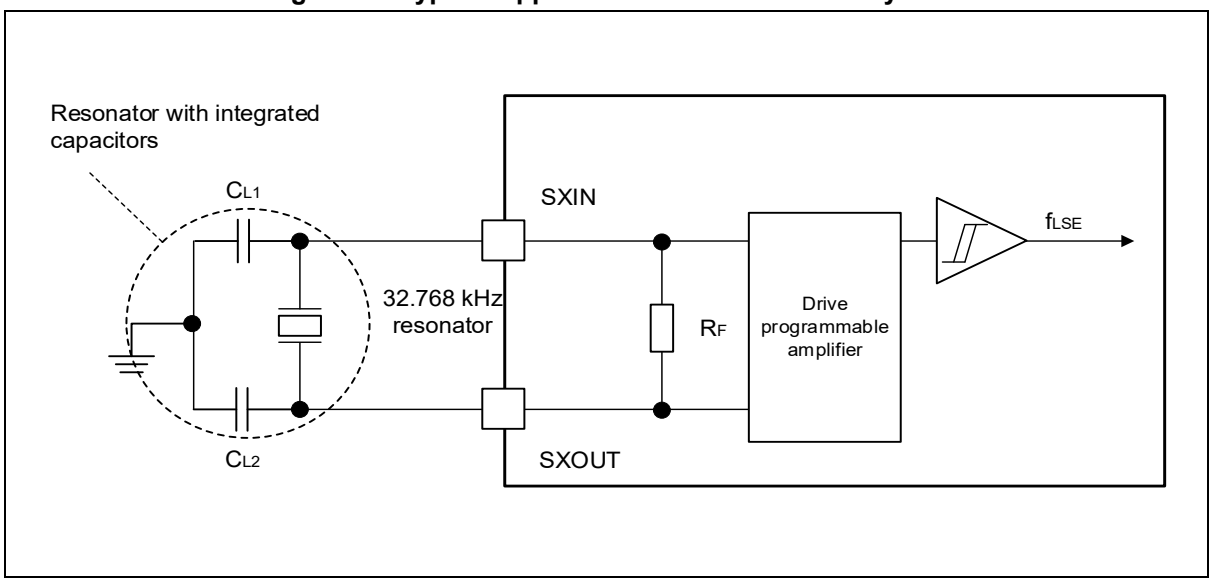


Figure 13. Typical Application with 32.768 kHz Crystal



NOTE:

1. An external resistor is not required between SXIN and SXOUT and it is forbidden to add one.

4.3.7 Internal Clock Source Characteristics

The parameters listed in Table 22 and Table 23 are obtained through tests conducted under ambient temperature and supply voltage conditions, which are specified in Table 14.

4.3.7.1 High-Speed Internal (HSI) RC Oscillator

Table 22. HSI Oscillator Characteristics(1)

(Temperature: −40°C to +85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating voltage	-	2.7	-	5.5	V
f_{HSI}	HSI frequency	V_{DD}=3.0 V, T_A=30°C	31.616	32	32.384	MHz
Δ_F	Frequency error	@ 25°C	−1.2	-	1.2	%
		@ −40°C to +85°C	−3	-	3	%
DuCy (HSI32)	Duty cycle	-	45	-	55	%
Δ_{VDD} (HSI32)	HSI32 oscillator Frequency drift over V_{DD}	V_{DD}=2.5 V to 5.5 V	−0.2	-	0.2	%
t_{SU} (HSI32)	HSI32 oscillator start-up time	-	-	5	10	µs
t_{STAB} (HSI32)	HSI32 oscillator stabilization time	-	-	4	10	µs
I_{DD} (HSI32)	HSI32 oscillator power consumption	-	-	420	550	µA

NOTE:

1. Guaranteed by characterization results and design.

4.3.7.2 Low-Speed Internal (LSI) 500 kHz RC Oscillator

Table 23. LSI Oscillator Characteristics

(Temperature: −40°C to +85°C)

Symbol	Parameter	Conditions(2)	Min.	Typ.	Max.	Unit
V_{DD}	Operating voltage		2.5	-	5.5	V
f_{LSI}	LSI frequency	V_{DD} = 2.5 to 5.5 V	400	500	600	kHz
t_{SU}(1)	500 kHz oscillator VREG start-up time (after LSI enabled)	V_{DD} = 5.0 V	-	5	10	µs
t_{STAB}(1)	500 kHz oscillator stabilization time (after LSI enabled)	5% of target frequency	-	20	50	µs
I_{LSI}(1)	500 kHz oscillator power consumption	The LSI oscillator is enabled. V_{DD}=2.5 to 5.5 V	-	4	8	µA
		The LSI oscillator is disabled. V_{DD}=2.5 to 5.5 V	-	1	100	nA

NOTE:

1. Guaranteed by design.

4.3.8 PLL Characteristics

The parameters listed in Table 24 are obtained through tests conducted under ambient temperature and supply voltage conditions, which are specified in Table 14.

Table 24. PLL Characteristics(1)

(Temperature: −40°C to +85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VDD	Operating voltage	-	2.5	-	5.5	V
I_{DD}(PLL)	PLL power consumption on V_{DD}	VCO freq = 240 MHz	-	1	-	mA
f_{PLLOUT}	PLL output clock	Voltage scaling range	-	-	120	MHz
f_{VCO}	PLL VCO output	VCO frequency range	200	-	280	MHz
f_{DUTY}	Duty	-	40	-	60	%
f_{IN}	Input frequency	$f_{PLLINCLK}$ / (PREDIV+1)	-	2	3	MHz
$f_{PLLINCLK}$	PLL block Input frequency	-	2	8	16	MHz
t_{JITTER}	P-P jitter	@ Lock state	-	-	100	ps
t_{LOCK}	PLL lock time	-	-	100	200	μs

NOTE:

1. Guaranteed by design.

4.3.9 Flash Memory Characteristics

Table 25. Code Flash Memory Characteristics

(Temperature: −40°C to +85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{PROG}	Program time	-	-	-	30	μs
t_{PER}	Page erase time	-	-	-	4	ms
t_{SER}	Sector erase time		-	-	4	ms
t_{MER}	Mass (chip) erase time	-	-	-	8	ms
N_{FWE}	Endurance of write/erase	T_A=25°C, page unit	10,000	-	-	times
t_{RT}	Retention time	-	10	-	-	years

4.3.10 I/O Port Characteristics

Table 26. DC Electrical Characteristics

(Temperature: −40°C to +85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low voltage	All GPIOs, nRESET, nBOOT	-	-	$0.2\times V_{DD}$	V
V_{IH}	Input high voltage	All GPIOs, nRESET, nBOOT	$0.8\times V_{DD}$	-	-	V
V_{OL}	Output low voltage	VDD = 5 V, I_{OL1} = 3 mA, I_{OL2} = 9 mA(1) VDD = 3.3 V, I_{OL3} = 1.3 mA, I_{OL4} = 4 mA(2)	-	-	$0.2\times V_{DD}$	V
V_{OH}	Output high voltage	VDD = 5 V, I_{OH1} = −3 mA, I_{OH2} = −9 mA(1) VDD = 3.3 V, I_{OH3} = −1.3 mA, I_{OH4} = −4 mA(2)	$0.8\times V_{DD}$	-	-	V
I_{OL1}	Output low current	VDD = 5 V, V_{OL} = 0.2 V_{DD}	-	-	3(1)	mA
I_{OH1}	Output high current	VDD = 5 V, V_{OH} = 0.8 V_{DD}	−3(1)	-	-	
I_{OL2}	Output low current	VDD = 5 V, V_{OL} = 0.2 V_{DD}	-	-	9(1)	
I_{OH2}	Output high current	VDD = 5 V, V_{OH} = 0.8 V_{DD}	−9(1)	-	-	
I_{OL3}	Output low current	VDD = 3.3 V, V_{OL} = 0.2 V_{DD}	-	-	1.3(2)	
I_{OH3}	Output high current	VDD = 3.3 V, V_{OH} = 0.8 V_{DD}	−1.3(2)	-	-	
I_{OL4}	Output low current	VDD = 3.3 V, V_{OL} = 0.2 V_{DD}	-	-	4(2)	
I_{OH4}	Output high current	VDD = 3.3 V, V_{OH} = 0.8 V_{DD}	−4(2)	-	-	
I_{IL}	Input low leakage current	All input ports	−1	-	-	µA
I_{IH}	Input high leakage current	All input ports	-	-	1	µA
R_{PU}	Pull-up resistor	R_{MAX} : V_{DD} = 2.7 V R_{MIN} : V_{DD} = 5.5 V	30	-	70	kΩ

NOTES:

1. Each pin can adjust the drive strength, and the difference between $I_{OH/L1}$ and $I_{OH/L2}$ (5V condition) is due to the difference in strength.
2. Under 3.3V conditions, drive strengths are specified by $I_{OH/L3}$ and $I_{OH/L4}$.

4.3.10.1 General Input/Output Characteristics

Unless otherwise specified, the parameters in Table 27 are obtained through tests conducted under the conditions which are specified in Table 14. All I/Os conform to CMOS standards.

Table 27. I/O Static Characteristics

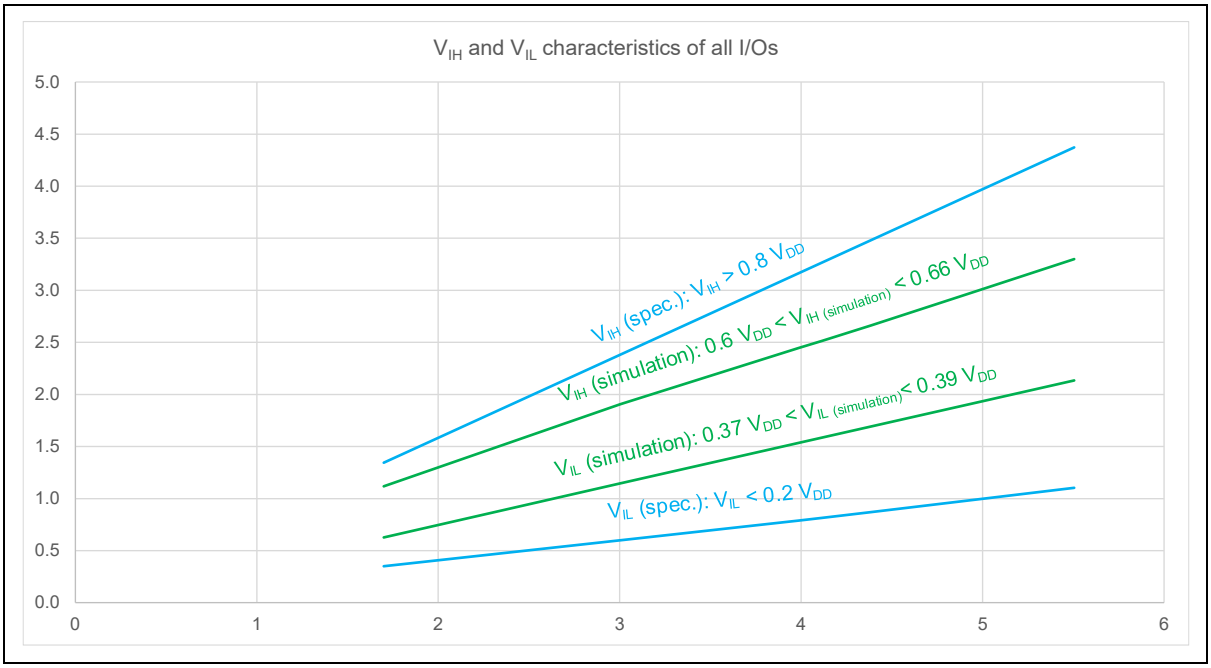
(Temperature: −40°C to +85°C)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{IL}(1)(2)	I/O input low level voltage	5 V GPIO	2.7 V ≤ V_{DD} ≤ 5.5 V	-	-	0.2×V_{DD}	V
V_{IH}(1)(2)	I/O input high level voltage	5 V GPIO	2.7 V ≤ V_{DD} ≤ 5.5 V	0.8×V_{DD}	-	-	V
V_{HYS}(3)	Input hysteresis	5 V GPIO	2.7 V ≤ V_{DD} ≤ 5.5 V $V_{DDTYPICAL}$ = 5 V	-	1	-	V
I_{leak}(3)	Input leakage current	5 V GPIO	0 ≤ V_{IN} ≤ V_{DD}	-	-	±1	μA
R_{PU}	Weak pullup equivalent resistor	V_{IN} = GND		30	50	70	kΩ
R_{PD}	Weak pulldown equivalent resistor	V_{IN} = V_{DD}		30	50	70	
C_{IO}	I/O pin capacitance	I/O pin capacitance		-	5	-	pF

NOTES:

1. Refer to Figure 14. I/O Input Characteristics
2. Data based on characterization results are not tested in production.
3. Guaranteed by design.

Figure 14. I/O Input Characteristics



NOTE:

1. X-axis is VDD, Y-axis is VIHL Spec.

4.3.10.2 Output Driving Current

The GPIOs are capable of sinking or sourcing currents up to ±8 mA and can also sink or source currents up to ±20 mA when the V_{OL}/V_{OH} limits are relaxed.

To ensure compliance with the absolute maximum ratings specified in chapter 4.2, it is necessary to limit the number of I/O pins driving current in the user application.

- The total current sourced by all I/O pins on VDD and the maximum operating current of the microcontroller on VDD (during Run mode) must not exceed the absolute maximum rating ΣI_{VDD} specified in Table 11.
- The total current sunk by all I/O pins on GND and the maximum operating current of the microcontroller on GND (during Run mode) must not exceed the absolute maximum rating ΣI_{GND} specified in Table 11.

4.3.10.3 Output Voltage Levels

Unless otherwise specified, parameters in Table 28 are obtained through tests conducted under ambient temperature and supply voltage conditions, which are specified in Table 14.

Table 28. Output Voltage Characteristics(1)

(Temperature: −40°C to +85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OL}	Output low voltage	VDD = 5 V, I_{OL1} = 3 mA, I_{OL2} = 9 mA VDD = 3.3 V, I_{OL3} = 1.3 mA, I_{OL4} = 4 mA	-	-	$0.2\times V_{DD}$	V
V_{OH}	Output high voltage	VDD = 5 V, I_{OH1} = −3 mA, I_{OH2} = −9 mA VDD = 3.3 V, I_{OH3} = −1.3 mA, I_{OH4} = −4 mA	$0.8\times V_{DD}$	-	-	
I_{OL1}	Output low current	VDD = 5 V, V_{OL} = 0.2 V_{DD}	-	-	3(1)	mA
I_{OH1}	Output high current	VDD = 5 V, V_{OH} = 0.8 V_{DD}	−3(1)	-	-	
I_{OL2}	Output low current	VDD = 5 V, V_{OL} = 0.2 V_{DD}	-	-	9(1)	
I_{OH2}	Output high current	VDD = 5 V, V_{OH} = 0.8 V_{DD}	−9(1)	-	-	
I_{OL3}	Output low current	VDD = 3.3 V, V_{OL} = 0.2 V_{DD}	-	-	1.3(1)	
I_{OH3}	Output high current	VDD = 3.3 V, V_{OH} = 0.8 V_{DD}	−1.3(1)	-	-	
I_{OL4}	Output low current	VDD = 3.3 V, V_{OL} = 0.2 V_{DD}	-	-	4(1)	
I_{OH4}	Output high current	VDD = 3.3 V, V_{OH} = 0.8 V_{DD}	−4(1)	-	-	

NOTE:

1. Guaranteed by design.

4.3.11 Analog-to-Digital Converter Characteristics

Table 29. ADC Electrical Characteristics

(Temperature: −40°C to +85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	unit
AV_{DD}	Operating voltage	-	2.7	5	5.5	V
-	Resolution	-	-	-	12	bit
I_{DDA}	Operating current	AVDD = 5.0 VA @ f_{MCLK} = 25 MHz	-	2.0	-	mA
		AVDD = 5.0 VA @ f_{MCLK} = 42 MHz	-	2.3	-	mA
V_{AN}	Analog input range	-	GND	-	AV_{DD}	V
t_{CONV}	Conversion time	-	18 / f_{ACLK}	-	48 / f_{ACLK}	μs
f_{CONV}	Conversion frequency	@ AVDD ≥ 3.7 V	-	-	1.5	MHz
		@ AVDD ≥ 3.1 V	-	-	1.5	MHz
		@ AVDD ≥ 2.7 V	-	-	1.0	MHz
f_{ACLK}	Operating frequency	-	-	-	42	MHz
INL	DC accuracy	-	-	-	±4	LSB
DNL		-	-	-	±2	LSB
ZOE	Zero offset error	TBD	-	±3	-	LSB
FSE	Full scale error	TBD	-	±3	-	LSB

4.3.11.1 General PCB Design Guidelines

The power supplier must be separated conforming to the scheme shown in Figure 5. The de-coupling capacitors across the V_{DD} and AV_{DD} are ceramic (good quality) capacitors and must be located as close as possible to the chip.

4.3.12 Communication Interfaces Characteristics

4.3.12.1 I2C Interface Characteristics

The I2C interface conforms to the timing requirements specified in the I2C-bus specification, in addition to the user timing requirements listed below:

- Standard mode (Sm): up to 100 kbps bit rate
- Fast mode (Fm): up to 400 kbps bit rate

The I2C timing requirements are guaranteed by design when the I2C peripheral is configured correctly and the I2C clock frequency is equal to or greater than the minimum value listed in the table below.

Table 30. I2C Characteristics

(Temperature: −40°C to +85°C)

Symbol	Parameter	Standard		Fast		Unit
		Min.	Max.	Min.	Max.	
f_{SCL}	Clock frequency	0	100	0	400	kHz
t_{SCLH}	Clock high pulse width	4.0	-	0.6	-	µs
t_{SCLL}	clock low pulse width	4.7	-	1.3	-	
t_{BF}	Bus free time	4.7	-	1.3	-	
t_{STSU}	Start condition setup time	4.7	-	0.6	-	
t_{STHD}	Start condition hold time	4.0	-	0.6	-	
t_{SPSU}	Stop condition setup time	4.0	-	0.6	-	
t_{SPHD}	Stop condition hold time	4.0	-	0.6	-	
t_{VD}	Output valid from clock	0	-	0	-	
t_{DIH}	Data input hold time	0	-	0	1.0	
t_{DIS}	Data input setup time	250	-	100	-	ns

4.3.12.2 SPI Interface Characteristics

Unless otherwise specified, the parameters in Table 31 are obtained through tests conducted under ambient temperature, f_{PCLK} frequency and supply voltage conditions, which are specified in Table 14.

- Capacitive load C = 30 pF
- Measurement points are performed at the CMOS level: $0.5 \times V_{DD}$

For more information about I/O alternate function characteristics (SS, SCK, MOSI, and MISO pins for SPI), refer to section 4.3.10.

Table 31. SPI Characteristics

(Temperature: −40°C to +85°C)

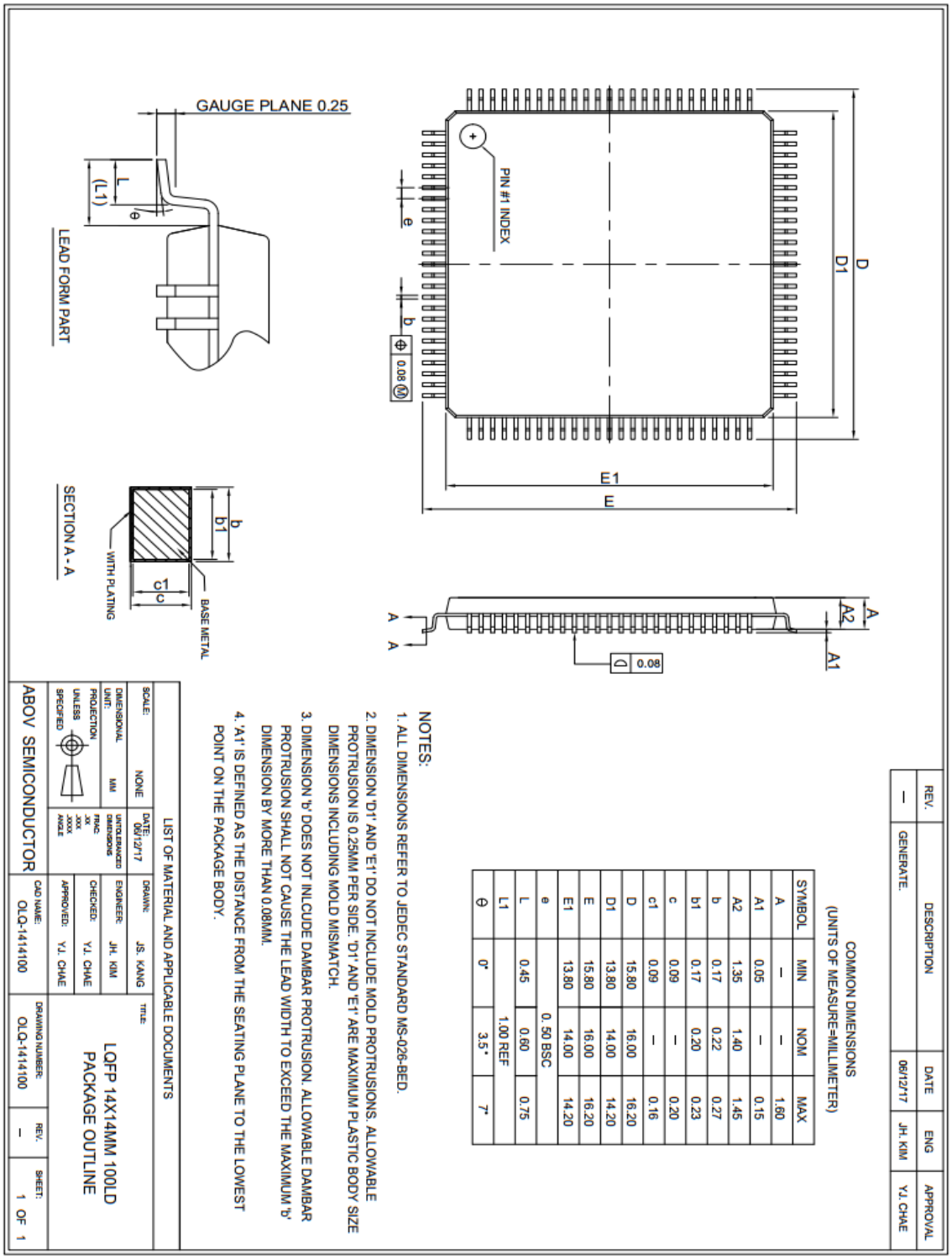
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{SCK1}	SPI clock frequency with strength on	SPI0, SPI1 2.7 V ≤ V_{DD} ≤ 3.3 V	-	-	12	MHz
f_{SCK2}		SPI0, SPI1 V_{DD} ≤ 5.5 V	-	-	12	MHz
f_{SCK3}	SPI clock frequency with strength off	SPI0, SPI1 2.7 V ≤ V_{DD} ≤ 3.3 V	-	-	5	MHz
f_{SCK4}		SPI0, SPI1 V_{DD} ≤ 5.5 V	-	-	10	MHz
Duty	Duty cycle of SPI frequency (SCK)	Slave Mode	30	50	70	%

5. Package Information

5.1 100-LQFP Package Information

100-LQFP is a 100-pin, 14 x 14 mm quad flat package.

Figure 15. Package Dimension (100-LQFP)



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	–	0.20
c1	0.09	–	0.16
D	15.80	16.00	16.20
D1	13.80	14.00	14.20
E	15.80	16.00	16.20
E1	13.80	14.00	14.20
e		0. 50 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	3.5°	7°

NOTES:
1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026-BED.
2. DIMENSION 'D1' AND 'E1' DO NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. 'D1' AND 'E1' ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION 'b' DOES NOT INLCUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM 'b' DIMENSION BY MORE THAN 0.08MM.
4. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

REV.	DESCRIPTION	DATE	ENG	APPROVAL
–	GENERATE.	06/12/17	JH. KIM	YJ. CHAE

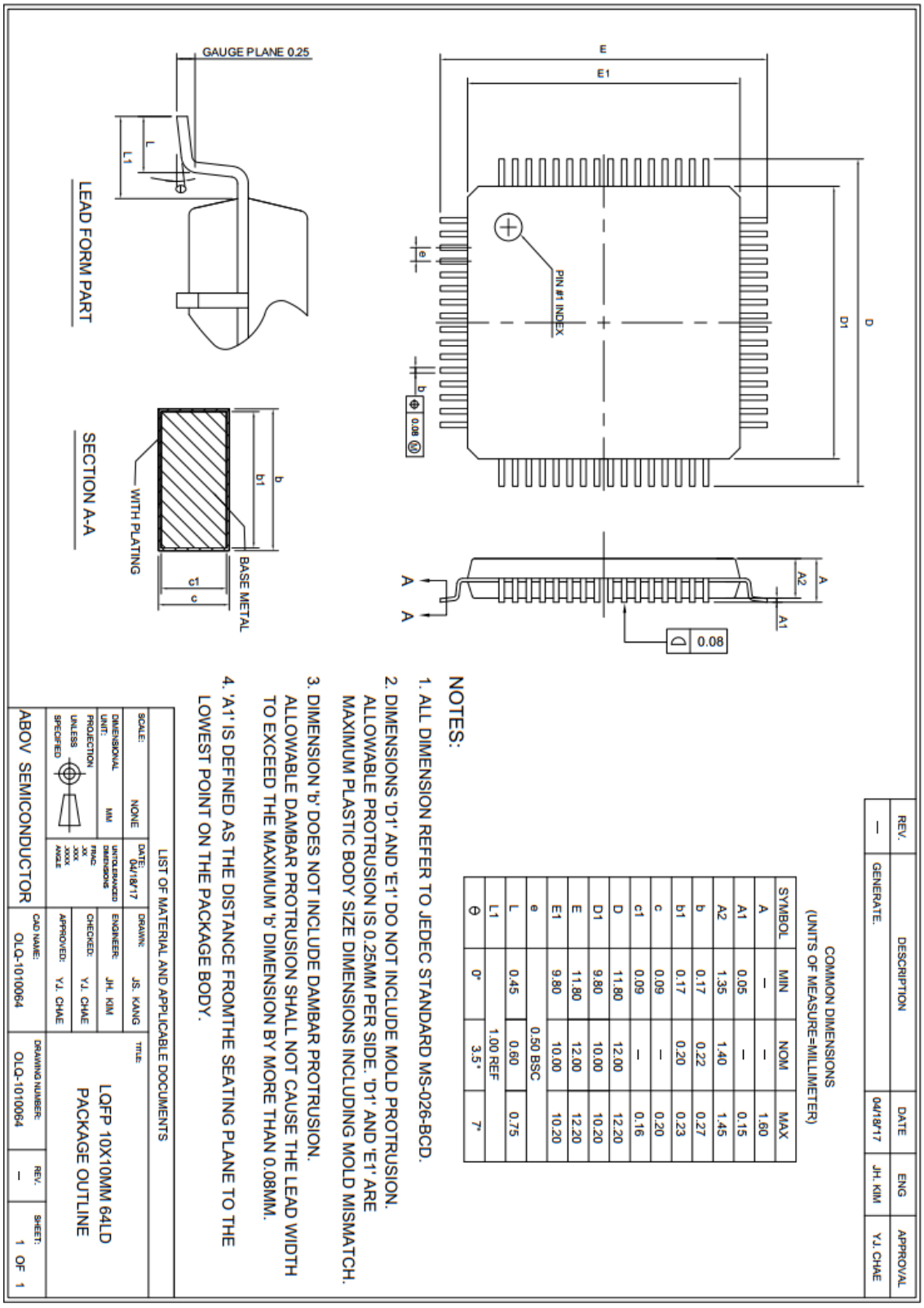
LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE: NONE	DATE: 06/12/17	DRAWN: JS. KANG	TITLE: LQFP 14X14MM 100LD PACKAGE OUTLINE
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS FRAC: .XX: .XXX: ANGLE:	ENGINEER: JH. KIM	
PROJECTION UNLESS SPECIFIED		CHECKED: YJ. CHAE	
ABOV SEMICONDUCTOR	CAD NAME: OLQ-1414100	APPROVED: YJ. CHAE	DRAWING NUMBER: OLQ-1414100 / REV: – / SHEET: 1 OF 1

5.2 64-LQFP Package Information

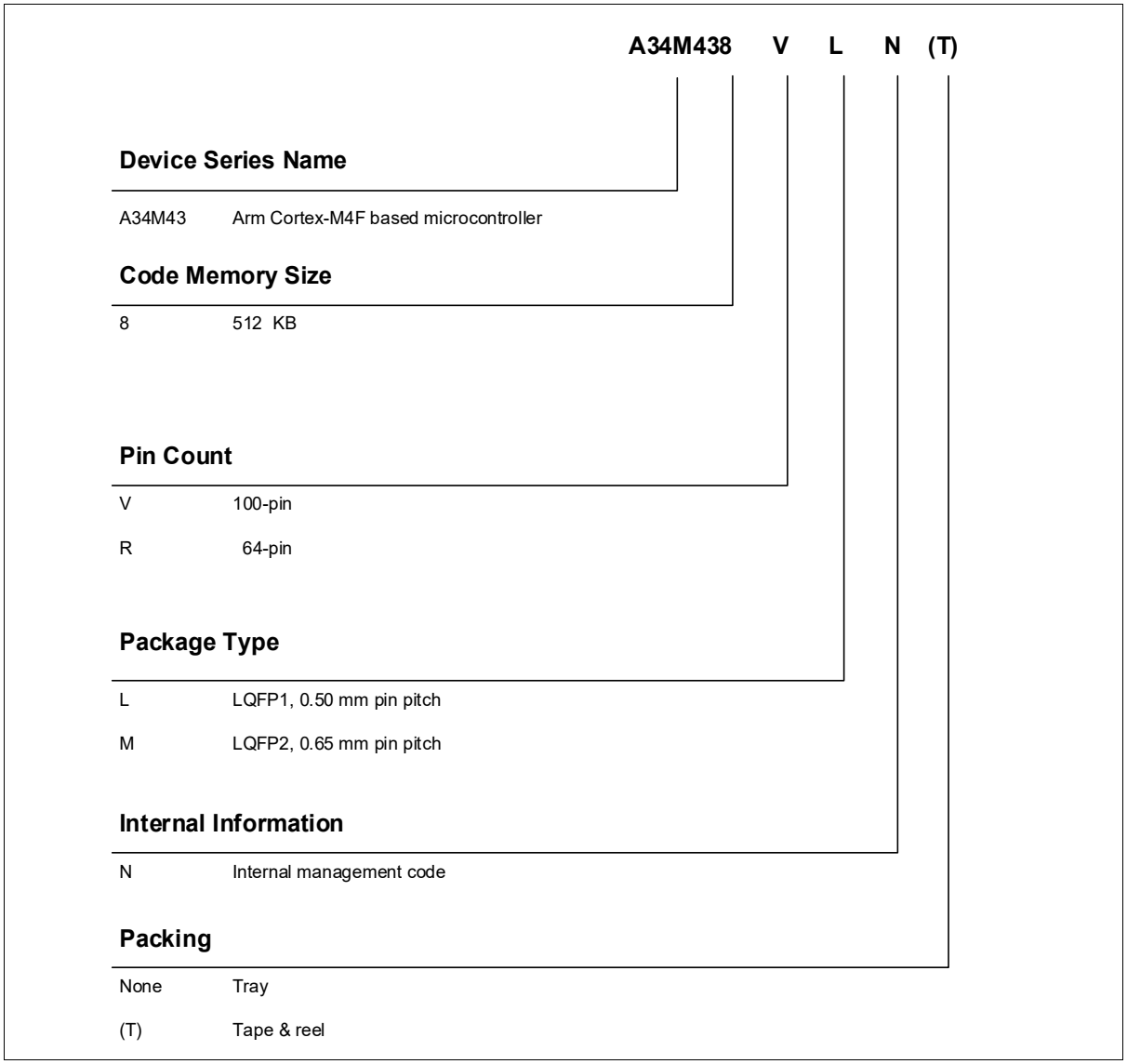
64-LQFP is a 64-pin, 10 x 10 mm quad flat package.

Figure 16. Package Dimension (64-LQFP)



6. Ordering Information

Figure 17. A34M438 Series Device Ordering Information



NOTE:

1. For a list of available options (memory, package, and so on) or for further information on any aspect of this device, contact the nearest ABOV sales office.

Revision History

Revision	Date	Notes
1.00	May 15, 2026	Initial release

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