
**Low-Power Cortex®-M4F 32-bit Microcontroller with FPU,
32 MHz, 256 KB Code Flash, 32 KB Data Flash, 24 KB SRAM**

DS Rev. 1.03

Features

Core

- Arm® 32-bit Cortex® -M4 CPU with FPU
- Maximum operating frequency 32 MHz

Memories

- 256 KB code flash memory with ECC
- 32 KB data flash memory with ECC
- 24 KB SRAM

Reset and Power Management

- Power-on/power-down reset (POR/LVR/LVI)
- Low-power modes: SLEEP, DEEP-SLEEP

Clock Management

- High-speed internal oscillator 32 MHz (HSI)
 - $\pm 0.5\%$ @-40°C to +85°C (HSICMU ON)
 - $\pm 3.0\%$ @-10°C to +70°C (HSICMU OFF)
 - $\pm 5.0\%$ @-20°C to +85°C (HSICMU OFF)
- Low-speed internal oscillator 40 kHz (LSI)
 - $\pm 30\%$ @-40°C to +85°C
- External main oscillator (HSE)
 - 1 MHz to 16 MHz
- External sub-oscillator (LSE)
 - 32.768 kHz
- Phase-locked loop (PLL) frequency generator
 - Up to 48 MHz
- Monitoring System
 - MCLK, HSE, and LSE clock monitoring

Interrupt Management

- Nested Vector Interrupt Controller (NVIC) with 86 interrupt sources

General-purpose Input/Output

- All mappable on external interrupt vectors
- Multi-function pins capable of selecting up to 7 different functions, including GPIO

DMA Controller

- 7-channel
- 8-/16-/32-bit data transfers
- Compatible with 18 different types of peripherals

12-bit ADC

- Two independent ADC blocks
- 24 analog input channels
- Adjustable sample time and hold time
- Multiple operating modes:
 - Single conversion
 - Sequence conversion
 - Burst conversion
 - Multiple conversion

12-bit DAC

- Two independent DAC blocks
- Two analog output channels

OPAMP

- Two operational amplifiers
- Compatible with ADC for joint operation

LCD Driver

- Up to 4x44 or 8x40 segments
- 8-step contrast control
- Resistor/Cap bias

Internal Low-dropout Regulator**16-bit Timer**

- 8 channels
 - 8 input capture channels
 - 8 output channels
- Timer operating modes:
 - Periodic timer mode
 - One-shot mode
 - PWM mode
 - Capture mode
- 10-bit prescaler

WDT

- 32-bit down-count timer
- Reset and periodic interrupts
- Eight different prescalers

FRT

- 32-bit free-run timer

Real Time Clock and Calendar**128-bit Unique ID****Serial Interfaces**

- USART x 2
- UART x 1
 - Asynchronous serial communication ports
- LPUART x 2
- SPI x 2
 - Two synchronous serial communication ports
- I2C x 2
 - Two communication ports
- USB 2.0 Full Speed
 - Crystal-less with clock recovery system
 - Number of endpoints from 1 to 5 in addition to Endpoint-0

CRC Calculation Unit

- CRC operating modes:
 - CRC32 (0x04C1_1DB7)
 - CRC16-USB (0x8005)
 - CRC16-CCITT (0x1021)
 - CRC8-CCITT (0x07)
- Support for byte reversal of input/output data
- Compatible with DMA

Development Support

- Serial Wire Debug (SWD), JTAG interface

Package

- 100-LQFP-1414 (0.5 mm pitch)
- 64-LQFP-1010 (0.5 mm pitch)
- 56-QFN-0707 (0.4 mm pitch)

Operating Voltage

- 1.8 V to 3.6 V

Operating Temperature

- Commercial grade (-40°C to + 85°C)

Product Selection Table

Table 1. Device Summary

Part Number	Flash	SRAM	SPI	UART	I2C	USART	LPUART	USB	ADC (ch)	DAC	OPAMP	I/O Ports	Package
A34L716VLN	256 KB	24 KB	2	1	2	2	2	1	2(24)	2	2	86	100-LQFP-1414
A34L716RLN	256 KB	24 KB	2	1	2	2	2	1	2(17)	2	2	53	64-LQFP-1010
A34L716JYN	256 KB	24 KB	2	1	2	1	1	1	2(17)	2	2	48	56-QFN-0707

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1. Introduction

The A34L716 series is a 32-bit high-performance microcontroller with up to 256 KB of flash memory and 24 KB SRAM. It is a powerful microcontroller that provides effective solutions to various electrical appliances that require both low power consumption and high performance (Arm Cortex-M4 core with FPU).

2. Description

2.1 Product Category Definition

This document provides an overview of the features supported by each device, including high-level information and brief explanations for each feature.

Table 2 provides an overview of the memory capacity for available devices in the A34L716 series. (Refer to Table 3 for the list of features supported by each product category.)

Table 2. A34L716 Series Memory Density

Memory Density		Category
Flash	RAM	
256 KB	24 KB	A34L716

2.2 Device Overview

Table 3 summarizes and lists product-specific features available in the A34L716 series, considering the largest package.

Table 3. A34L716 Series Features

Peripherals		Description
Core	CPU	• Maximum operating frequency: 32 MHz • 32-bit ARM Cortex-M4F core - 32-bit Thumb®-2 instruction set • CPU register set: - Uses general-purpose registers specified - Main stack pointer (MSP) and process stack pointer (PSP): R13 - Link register (LR): R14 - Program counter (PC): R15 • Data ordering format: Little-Endian • Harvard Architecture • AHB/APB
	Interrupt	• NVIC (Nested-Vectored Interrupt Controller) • Up to 86 peripheral interrupts are supported. • Assignable with 16 different priority levels
	FPU	• Rendered by extending and transforming the ARMv7 floating-point arithmetic functionality • Compliant with the ANSI/IEEE 754 standard • Capable of binary floating-point arithmetic and computation
Memory	Code Flash	• Capacity: 256 KB • A high-capacity Code Flash memory built-in • Max 25 MHz Flash access speed • 512 bytes, 2 KB erases • Bulk erase • Read protection • Self-programming • CRC code generation and verification for the Flash memory • Endurance: 10,000 cycles • Lifetime: 10 years
	Data Flash	• Capacity: 32 KB • Max 25 MHz access speed • 512 bytes, 2 KB erases • CRC code generation and verification for the Flash memory • Endurance: 100,000 Cycles • Lifetime: 10 years

Table 3. A34L716 Series Feature (continued)

Peripherals		Description
Memory	BOOT ROM	• Executes the processor's boot mode when receiving an input at the nBOOT pin from an external circuit • UART boot modes • In-system programming - A user can program data into the internal Flash memory by setting up an application board.
	SRAM	• Capacity: 24 KB • Usable as a program's work area • High-speed execution enables the execution of time-critical codes • Part of the SRAM can be remapped into an interrupt vector area
System Control Unit (SCU)	Operating frequency	Up to 32 MHz
	Clock	• High speed internal oscillator (HSI): 32 MHz - HSICMU ON: $\pm 0.5\%$ @ -40°C to +85°C - HSICMU OFF: $\pm 3.0\%$ @ -10°C to +70°C, $\pm 5.0\%$ @ -20°C to +85°C • Low speed internal oscillator (LSI): 40 kHz ($\pm 30\%$ @ -40°C to +85°C) • External main oscillator (HSE): 1 MHz to 16 MHz • External sub-oscillator (LSE): 32.768 kHz • Phase-locked loop (PLL) frequency generator generates a high-speed clock (up to 48 MHz)
	Clock monitoring	• System Fail-Safe function by Clock Monitoring - External main oscillator (HSE) - External sub oscillator (LSE) - Main system clock (MCLK)
	Operating mode	• RUN mode • SLEEP mode • DEEP-SLEEP (STOP1, STOP2) mode
	Reset	• nRESET pin reset (PC12) • Core reset • Software reset • POR (Power-On Reset) • LVR (Low-Voltage Reset) • WDTR (Watchdog Timer Reset) • Reset due to clock oscillating error
	VDC	Low-dropout (LDO) regulator built in for low-voltage operation
	POR	The POR generator detects an internal 1.4 V voltage and generates a reset signal.

Table 3. A34L716 Series Feature (continued)

Peripherals		Description
System Control Unit (SCU)	LVI	• Seven low-voltage detection levels • Supports interrupts • Supports wake-up from DEEP-SLEEP mode
	Wake-up	• Wake-up by a General-Purpose Input/Output (GPIO) pin • Wake-up by a Free-Run Timer (FRT) • Wake-up by a Watchdog Timer (WDT) • Wake-up by a Low-Voltage Indicator (LVI) • Wake-up by a Real-Time Clock and Calendar (RTCC) • Wake-up by an Inter-Integrated Circuit (I2C) • Wake-up by a Universal Synchronous and Asynchronous Receiver/Transmitter (USART) • Wake-up by a Low Power Universal Asynchronous Receiver/Transmitter (LPUART) • Wake-up by a USB
General Purpose I/O (GPIO)		• Input/output (I/O) port for general purposes • 100-LQFP - I/O pins: 86 • 64-LQFP - I/O pins: 53 • 56-QFN - I/O pins: 48 • Selectable input and output configuration for each pin: - Push-pull output - Open drain output - Input • Pin configurations through multiplexer settings • Configurable as an external interrupt source with the following options: - Rising-edge (high-level) - Falling-edge (low-level) - Edge-triggered (both rising-edge and falling-edge) • Configurable pull-up/down resistors and debouncing • Adjustable drive strength • Configurable independently to be set or reset through its corresponding bit • Wake-up events triggered by external asynchronous inputs
Direct Memory Access Controller (DMA)		• 7-channel direct memory access (DMA) support peripherals • 8-bit/ 16-bit/ 32-bit data transfers • Compatible with 18 different types of peripherals • UART, USART10, USART11, LPUART0, LPUART1, SPI0, SPI1, ADC0, ADC1, CRC

Table 3. A34L716 Series Feature (continued)

Peripherals		Description
TIMER	16-bit Timer	• General-purpose 16-bit up-count timer • 8 channels - 8 (TnIO) input capture channels - 8 (TnIO) output channels • Timer operating modes - Periodic timer mode - One-shot mode - PWM mode - Capture mode • Interrupt events - Timer/Counter match interrupt - Timer overflow interrupt • Selectable clock sources: - PCLK configurable through the peripheral clock enable register1 (SCU_PCER1) - LSI, LSE, MCLK, HSI, HSE or PLL configurable through the miscellaneous clock control register 3 (SCU_MCCR3) • Timer signals can be generated through TnIO pins • 10-bit prescaler
	WDT	• 32-bit down-count timer • Reset and periodic interrupts • Selectable clock sources: - LSI, LSE, MCLK, HSI, HSE or PLL configurable through the miscellaneous clock control register 1 (SCU_MCCR1) • Selectable eight different prescalers
	FRT	• 32-bit Free-run Timer - Timer for system time measurement - 32-bit up-count timer • Interrupt event - Period interrupt - Overflow interrupt

Table 3. A34L716 Series Feature (continued)

Peripherals		Description
TIMER	RTCC	• Real-time clock and Calendar • LSE clock as RTCC clock (f_{RTCC}) • Counters of year, month, week, day, hour, minute, and second (up to 99 years) • Interrupt event - Constant period matching interrupt function (period: 0.5 seconds, 1 second, 1 minute, 1 hour, 1 day, 1 month) - Alarm interrupt function (alarm: week, hour, minute) - Timestamp interrupt and function • Pin output of 1 Hz clock • Error correction by 1.53 ppm resolution when using 32768 Hz LSE
Serial Interface	UART	• One Asynchronous serial communication port • Configurable standard asynchronous communication bits (start, stop, and parity) • Flexible communication available through programming - 5- to 8-bit data transfers - Even/ Odd/ Non-parity generation and checking - 1-bit, 1.5-bit, or 2-bit stop bit generation and checking • 8-bit fraction controller and 16-bit baud rate generator
	SPI	• Two synchronous serial communication port channels • Master/Slave operation • Loop-back mode • Programmable and flexible communication - 8-bit/ 9-bit/ 16-bit/ 17-bit data transmission/reception - SPI clock speed - Both Least Significant Bit (LSB)-first and Most Significant Bit (MSB)-first modes available
	I2C	• Standard I2C communication protocol • Two channels support • Master and slave modes • 7-bit addressing for slave mode • Configurable SCL signal's high/low periods and SDA signal's hold time

Table 3. A34L716 Series Feature (continued)

Peripherals		Description
Serial Interface	LPUART	• Full-duplex and Half-duplex • Configurable standard asynchronous communication bits (start, stop, and parity) • Flexible communication available through programming - 5- to 8-bit data transfers - Even/ Odd/ Non-parity generation and checking - 1-bit, 2-bit stop bit generation and checking • Receive Character Detection & Receive Time Out function • Baud rate compensation • Up to 9,600 bps with 32.768 kHz LSE • Data overrun & Frame error detection
	USART	• Full Duplex Operation. (Independent Serial Receive and Transmit Registers) • Two Channels USART module • Asynchronous or Synchronous Operation. • 8-bit fraction controller and 16-bit baud rate generator • Flexible communication available through programming - 5- to 9-bit data transfers - Even/ Odd/ Non-parity generation and checking - 1-bit, 2-bit stop bit generation and checking • Receive Character Detection & Receive Time Out function • Data overrun and Frame error detection • Three Separate Interrupts on TX Completion, TX Data Register Empty and RX Completion. • Double Speed Asynchronous communication mode.
	USB	• Crystal-less with clock recovery system • Compliant with USB 2.0 Full-Speed • 1 KB SRAM dedicated to USB • Endpoint 1 to 5 support. • IN and OUT Endpoint. • DMA 2 channels, 64 bytes buffer size

Table 3. A34L716 Series Feature (continued)

Peripherals	Description
12-bit A/D Converter (ADC)	• Two independent ADC blocks • 24 analog input channels • Multiple operating modes: - Single conversion - Sequence conversion - Burst conversion - Multiple conversion • Up to 26 sequential conversions supported • Software triggers • One internal trigger source (timers) • Sample time and hold time are adjustable • Support for the simultaneous start of two ADC blocks • In Burst mode, support for Continuous mode
12-bit D/A Converter (DAC)	• Two units of 12-bit DAC • Selectable output to the AIPn pin of OPAMP block.
Operational Amplifier (OPAMP)	• Two OPAMPs, each with two input sources • Compatible with ADC for joint operation
Cyclic Redundancy Check (CRC)	• CRC operating modes: - CRC32 (0x04C1_1DB7) - CRC16_USB (0x8005) - CRC16_CCITT (0x1021) - CRC8_CCITT (0x07) • Support for byte reversal of input/output data • Compatible with DMA
LCD Driver	• 8-COM x 40-SEG or 4-COM x 44-SEG (100-LQFP) • 8-COM x 18-SEG or 4-COM x 22-SEG (64-LQFP) • 8-COM x 13-SEG or 4-COM x 17-SEG (56-QFN) • Resistor/Capacitor bias • 8-step contrast control
Operating Voltage	1.8 V to 3.6 V
Operating temperature	Commercial grade (-40°C to +85°C)
Package	• Three types of package options - 100-pin LQFP - 64-pin LQFP - 56-pin QFN

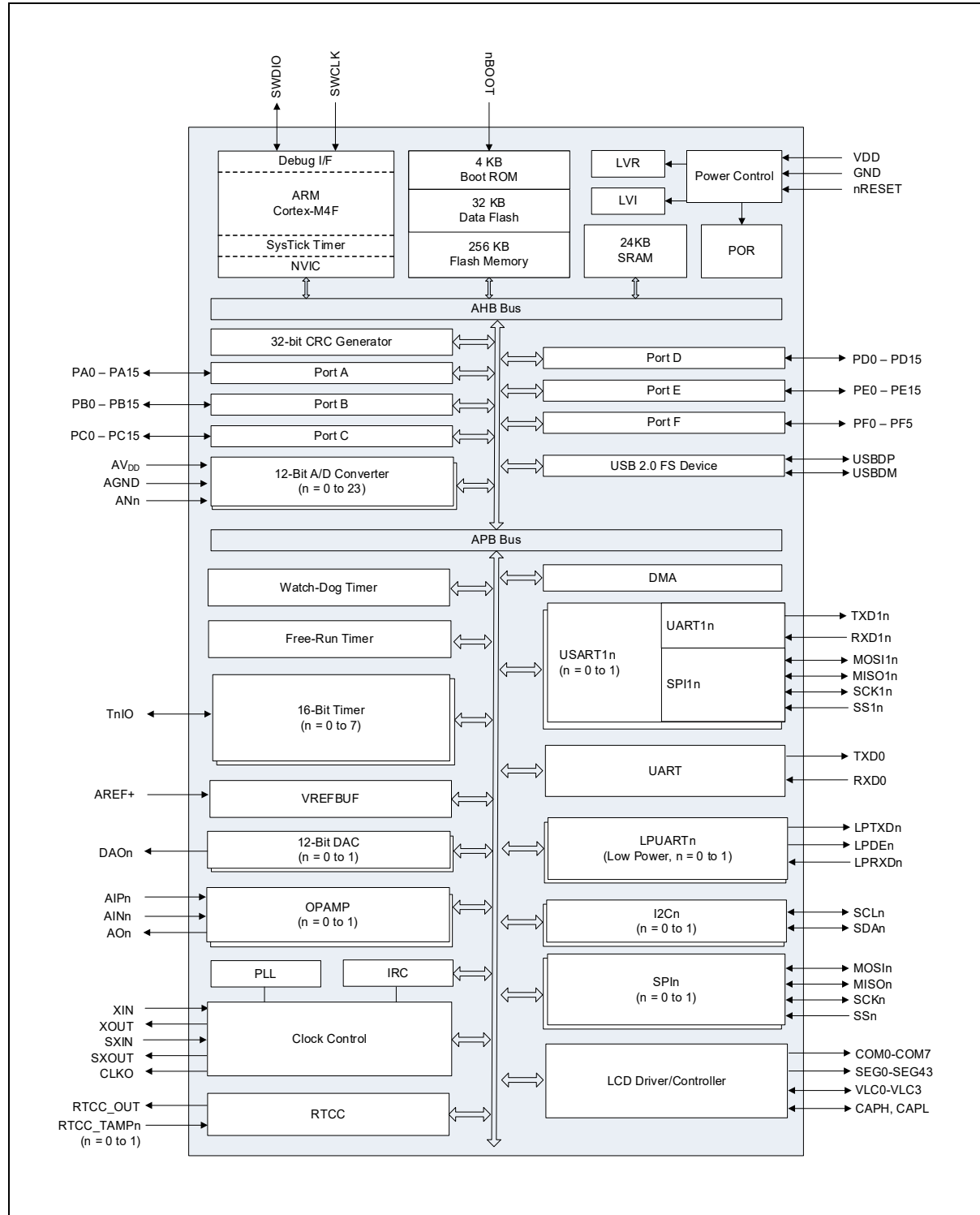
Table 4. Summary of A34L716 Peripherals

Peripheral		A34L716VLN	A34L716RLN	A34L716JYN
Code flash memory		256 KB		
Data flash memory		32 KB		
SRAM		24 KB		
Timers	General purpose	8 (16-bit)		
	SysTick timer	1		
	Watchdog timer	1		
	Free-run Timer	1		
	RTCC	1		
Communication interfaces	SPI	2		
	I2C	2		
	UART	1		
	USART	2		1
	LPUART	2		1
	USB	1		
LCD (COM x SEG)		4 x 44 or 8 x 40	4 x 22 or 8 x 18	4 x 17 or 8 x 13
DMA (Direct Memory Access)		7		
GPIO		86	54	46
ADCs		2 (12-bit 1.0 Msps)		
Number of channels		24	17	
DACs		2		
OPAMPs		2		
Max. CPU frequency		32 MHz		
CRC		1		
Operating voltage		1.8 V to 3.6 V		
Operating temperature		Ambient operating temperature: -40°C to 85°C		
Packages		100-LQFP	64-LQFP	56-QFN

2.3 Block Diagram

Figure 1 shows a block diagram of the A34L716 series.

Figure 1. A34L716 Series Block Diagram



2.4 Functional Overview

The following sections describe the features of the A34L716 series microcontrollers.

2.4.1 Cortex-M4F Core

The Arm® Cortex-M4F has the same functions as the Cortex-M4 and includes optional floating-point arithmetic functionality. The two processors are intended for deeply embedded applications that require fast interrupt response features.

For detailed information on the Cortex-M4F, refer to document ID061113 provided by the ARM.

2.4.2 Floating Point Unit (FPU)

Cortex-M4 FPU is an implementation of the single precision variant of the ARMv7-M Floating-Point Extension (FPv4-SP). It provides floating-point computation functionality that is compliant with the ANSI/IEEE Std 754-2008, IEEE Standard for Binary Floating-Point Arithmetic, referred to as the IEEE 754 standard. The FPU supports all single-precision data-processing instructions and data types described in the ARM®v7-M Architecture Reference Manual.

2.4.3 Embedded SRAM

The A34L716 series has a block of zero-wait on-chip SRAM. The size of the SRAM is 24 KB, and its base address is 0x2000_0000.

The SRAM memory area is commonly utilized for storing data and as a stack memory. Additionally, it can also be utilized for storing program code for faster execution or during flash erase/programming operations. This device does not support a memory remap strategy. Therefore, it is necessary to perform a jump and return to execute the code stored in the SRAM memory area.

2.4.4 Boot Configuration

The A34L716 series offers one boot mode for programming internal flash memory. The boot mode can be entered by setting the nBOOT pin to 'L' during the system reset process (the normal state is 'H').

The boot mode supports the UART boot, which uses the UART interface to transmit and receive boot data (TXD0/RXD0).

The pins for the boot mode are listed in Table 5.

Table 5. Boot Mode Pin List

Block	Pin Name	I/O	Pin Direction	Description
SYSTEM	nRESET	PC12	Input	Receive the reset signal.
	nBOOT	PC13	Input	Set the boot mode.
UART0	RXD0	PD0	Input	Receive the UART boot data.
	TXD0	PD1	Output	Transmit the UART boot data.

2.4.5 Power Supply

The device requires a 1.8 V to 3.6 V operating voltage supply (V_{DD}) and analog peripherals are supplied through the independent power domain AV_{DD} .

Table 6. Power Supply

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	1.8	3.6	V
	AV_{DD} (Analog V_{DD}) ⁽¹⁾	1.8	3.6	V

NOTE:

1. AV_{DD} must always be supplied at the exact same voltage level as V_{DD} without exception. ($AV_{DD} = V_{DD}$)

During a power-up process, a reset plays an important role and affects the entire process of system booting. The A34L716 series has two power-related reset options, as described below:

- POR_RST (Power-On Reset) controls the voltage less than 1.4 V(Typ.).
- LVD_RST (Low-Voltage Detect Reset) controls the voltage less than 1.69 V (Typ.).

If the power level is higher than the POR and below the Flash operating voltage, the Code Read operation may malfunction. To prevent this abnormal Code Read operation, the LVD_RST operates to generate the SYSRESETn internal signal and enter the microcontroller into reset mode. The minimum level that the LVR can set is 1.69 V(Typ.), which satisfies the minimum flash operating voltage.

2.4.6 Operation Mode

2.4.6.1 Transition of Operation Mode

INIT mode is the initial state of the chip when a reset is asserted. In RUN mode, the CPU shows the maximum performance with a high-speed clock system. SLEEP mode and DEEP-SLEEP mode can be used as low power consumption mode. In the low power consumption mode, power is effectively managed to reduce power consumption by halting the processor core and unused peripherals.

2.4.6.2 RUN Mode

In RUN mode, the CPU and peripheral hardware operate with a high-speed clock. If the INIT state occurs after a reset, the system enters RUN mode.

2.4.6.3 SLEEP Mode

Once the microcontroller enters SLEEP mode, the CPU becomes inactive. By setting the SCU_PER and SCU_PCER registers, users can determine which peripherals are to be inactive in SLEEP mode.

2.4.6.4 DEEP-SLEEP (STOP1, STOP2) Mode

When the core goes under stop state using WFI instruction, the chip enters DEEP-SLEEP mode. DEEP-SLEEP mode is divided into DEEP-SLEEP (STOP 1) and DEEP-SLEEP (STOP 2) modes.

2.4.6.5 Reset Mode

The A34L716 series has two system reset options. One is a cold reset, which is effective during power up or down sequence; the other is a warm reset, which is generated by several reset sources.

The reset features of the A34L716 series are as follows:

- Power-on reset (POR)
- Low-Voltage Detect Reset (LVR)
- nRESET pin reset
- Watchdog timer reset (WDT)
- Software reset
- Clock oscillating error reset
- CPU request reset

2.4.7 Clocks and Startup

The A34L716 series has two main operating clocks. One is HCLK, which generates clock signals both for the CPU and AHB bus system; the other is PCLK, which generates clock signals for peripheral systems.

2.4.7.1 HCLK Clock

The Cortex-M4F CPU requires two clocks, the HCLK and FCLK. The HCLK is fed to the CPU and AHB. The FCLK stays enabled except in DEEP-SLEEP mode, whereas the HCLK can be disabled in Idle mode.

The HCLK clocks the buses and memories. As the bus clock frequency is limited to a maximum of 32 MHz, the HCLK frequency must not exceed 32 MHz.

2.4.7.2 PCLK Clock

The PCLK can be used as a clock for any peripherals. Whether to enable or disable the PCLK for each peripheral is determined with the SCU_PCER registers; each peripheral block's registers cannot be read unless its PCLK input is enabled. And the PCLK stops operating in DEEP-SLEEP mode.

2.4.7.3 Clock Configuration Procedure

After the microcontroller is powered on, the HSI (4 MHz = 32 MHz / 8) is initially enabled as a system clock source by default in the system operation sequence. Users can set another clock source as the system clock while the HSI is clocking the system.

Before enabling the HSE block, the pin mux configuration must be completed for XIN and XOUT. Users must be careful not to affect other bits of the PC_MR and PC_CR registers during this process. Once the HSE block has been enabled, the users must wait for crystal oscillation to stabilize.

The secondary LSE (32.768 kHz) clock can be enabled with the SCU_CSCR register. Likewise, with pins XIN and XOUT for the HSE, the LSE must be enabled after the pin mux configuration is completed for SXIN and SXOUT, and then the stabilizing time is elapsed.

2.4.8 Interrupts and Events

2.4.8.1 Nested Vectored-Interrupt Controller (NVIC)

The A34L716 series includes up to 86 maskable interrupt channels that manage sixteen priority levels and the Nested Vector Interrupt Controller (NVIC) that controls 16 interrupt lines of the Cortex®-M4.

The NVIC has the following advantages:

- The NVIC enables interrupt processing while reducing interrupt latency.
- Interrupt Vector Table (IVT) address delivered directly to the core
- The fast interrupt processing capability
- Higher priority interrupts are completed before lower priority interrupts, although they are generated later than the lower priority interrupts.
- Tail Chaining
- Automatic saving of processor state
- Interrupt restoring without instructional overhead at the end of the interrupt

The NVIC hardware block provides flexible and efficient interrupt management with minimal interrupt latency.

2.4.8.2 Extended Interrupt (EXTI)

External interrupt is used to generate event requests or wake up the system from STOP mode. Users can configure each external line to select a trigger event (rising edge, falling edge, and both edges) and level event (Low, High) independently.

2.4.9 General Purpose Input/Output (GPIO)

2.4.9.1 PCU Introduction

The A34L716 series has a Port Control Unit (PCU) module that controls the external input and output (I/O) ports. By setting the PCU registers, users can configure the pins' uses, input/output direction, Pull-up/Pull-down, and debouncing for their applications as needed.

2.4.9.2 GPIO Introduction

Pins, except the V_{DD} , GND, and certain specific-purpose pins, can be used as General-Purpose Input/Output (GPIO) pins.

The GPIO module controls the general I/O ports. Output pins can be set to generate high or low-level signals by configuring the corresponding bits of the GPIO control register; logic input pins can be monitored for their input status in the control registers.

2.4.10 Embedded Flash Memory

The flash memory controller is an interface controller for embedded flash memory. It manages data stored on the flash memory and communicates with other electronic devices.

Code flash memory of the A34L716 series has several key features as listed below:

- Code Flash memory for 256 KB with write protection bits
- Bulk (full-chip), 512 bytes, 2 KB erases
- Zero wait (less than 25 MHz), 1 to 15 wait
- Code Flash Read Protection

Data flash memory of the A34L716 series has several key features as listed below:

- Data Flash memory for 32 KB with write protection bits
- Bulk (full-chip), 512 bytes, 2 KB erases
- Zero wait (less than 25 MHz), 1 to 15 wait

2.4.11 High-Speed Internal OSC Clock Management Unit (HSICMU)

The High-Speed Internal OSC Clock Management Unit (HSICMU) integrated into the A34L716 is designed for the auto-trimming of the Internal OSC clock used for the X'tal-less USB.

The following are characteristics of the High-Speed Internal OSC Clock Management Unit (HSICMU) built in the A34L716. It is used to auto-trim the Internal OSC clock of X'tal-less USB.

The HSICMU is ideally suited to provide a precise clock for the USB peripheral. In such a case, the synchronization signal can be derived from the Start-of-Frame (SOF) packet signalization on the USB bus, which a USB host sends at 1 ms intervals.

The synchronization signal can also be derived from the LSE oscillator output, or it can be generated by user software.

- Selectable synchronization source with programmable prescaler and polarity:
 - USB SOF (Start of Frame) sent received toggle
 - LSE
 - External SYNC pin (PD0)
- Possibility to generate synchronization pulses by software
- Automatic oscillator trimming capability without requiring CPU action
- 16-bit frequency error counter with automatic error value capture and reload
- Programmable limit for automatic frequency error value evaluation and status reporting

2.4.12 Direct Memory Access Controller (DMA)

The direct memory access (DMA) controller is used for high-speed data transfers between peripherals and memories. DMA enables quick data transfers having memory to memory copying or moving of data within memory.

- Seven channels
- Only single-ended signaling supported
- 8-bit/ 16-bit/ 32-bit data transfers supported
- Various buffers of the same size supported
- DMA transfers are triggered through peripheral interrupts

2.4.13 Timers

2.4.13.1 Watchdog Timer (WDT)

A Watchdog Timer (WDT) is used to detect microcontroller errors due to external interference or unexpected logical conditions. These errors cause the application program to give up the normal sequence. If the microcontroller is out of control, the WDT resets the microcontroller and returns it to normal.

The WDT of the A34L716 series is a 32-bit down counter. If the WDT is set as a reset source, the microcontroller restarts when the down counter reaches 0.

When it is not used to monitor the microcontroller, the WDT can be used as a cycle timer along with an interrupt.

2.4.13.2 16-bit Timer Introduction

The A34L716 series has a TIMER module, each configured with eight units. This 16-bit Timer supports four operating modes: Periodic Mode, PWM Mode, One-shot Mode, and Capture Mode.

Users can use a divided PCLK or an external clock as an input clock source for the 16-bit Timer. An internal 10-bit prescaler allows to generate a variety of timer base clocks.

Interrupts can be triggered at regular intervals when the timer is used in Periodic Mode. Users can set the period and duty to form a PWM signal that is used in PWM Mode.

In One-shot Modes, the timer can generate one PWM waveform. In Capture Mode, the external input signal's pulse intervals can be measured based on the preset condition. Moreover, the timer can export signals to other devices to control them. This timer is primarily used as a periodic tick timer or wake-up source.

2.4.13.3 Free-run Timers (FRT)

The A34L716 series has one built-in Free-run Timer (FRT) that is a 32-bit up count timer. The FRT can run with an overflow interrupt or a match interrupt according to their register setting and can remain active in DEEP-SLEEP STOP 1 mode.

2.4.13.4 SysTick Timer

The SysTick timer is exclusively used for real-time operating systems but can also be used as a standard down counter.

It has the key features as shown below:

- 24-bit down-counter
- Automatic refreshing
- Maskable system interrupt generation when the counter reaches '0'
- Programmable clock source

2.4.14 Universal Asynchronous Receiver/Transmitter (UART)

The A34L716 series has a one-channel UART module. This built-in UART module transmits and receives data according to user-specified settings and reads the current UART status.

The UART status information includes the type and conditions of the current UART transmission/reception process. It can be used to check for errors (Parity, overrun, framing, or break interrupts) that may occur during data reception.

The UART channel has a programmable baud-rate generator that generates an internal clock for the corresponding UART unit by dividing the prescaled clock using a baud-rate divisor (Ranging from 1 to 65535) and then dividing the result by 16.

Users can program interrupts that can control UART communication.

Using Direct Memory Access (DMA), users can perform high-speed data communication.

2.4.15 Serial Peripheral Interface (SPI)

The A34L716 series has two built-in Serial Peripheral Interface (SPI) modules. Clocks synchronize the SPI modules, and the specifications of the transfer clocks are adjustable.

The SPI module supports communication between one master and slaves. Slaves can be selected by the Slave Select (SS) signal.

The SPI module performs four-wire synchronous transfers via four signal terminals (SS, SCK, MOSI, and MISO). Its separate Transmit and Receive Buffers enable full-duplex communication, which is capable of reading and writing data simultaneously.

2.4.16 Inter-integrated Circuit (I2C) Interface

The I2C (Inter-integrated Circuit) interface built in the A34L716 series satisfies the standard I2C communication protocol and is used for serial communication with internal and external devices via the I2C protocol.

Equipped with two units, it supports both master and slave modes and is capable of transmitting and receiving data in bytes by using interrupts or polling.

The I2C of the A34L716 series operates in Standard mode (100 kHz) or Fast mode (400 kHz) and supports general calls.

It helps communicate with various peripherals that have the same bus type. When using the I2C, it is recommended to set the SCL and SDA pins to open-drain and then connect external pull-up resistors to render their output signals 'HIGH'.

Table 7. Features of I2Cn (n = 0 to 1)

I2C Features	I2C0	I2C1
7-bit addressing mode	O	O
Standard-mode (up to 100 kbit/s)	O	O
Fast-mode (up to 400 kbit/s)	O	O
General call	O	O

2.4.17 Universal Synchronous and Asynchronous Receiver/Transmitter (USART)

Universal Synchronous and Asynchronous serial Receiver and Transmitter (USART) is a highly flexible serial communication device.

The main features are listed below:

- Full Duplex Operation. (Independent Serial Receive and Transmit Registers)
- Asynchronous or Synchronous Operation.
- Baud Rate Generator.
- Supports Serial Frames with 5, 6, 7, 8, or 9 Data bits and 1 or 2 Stop bits.
- Hardware supports odd or Even Parity Generation and Parity Check.
- Data Over Run Detection.
- Framing Error Detection.
- Three Separate Interrupts on TX Completion, TX Data Register Empty, and RX Completion.
- Double Speed Asynchronous communication mode.

Additional features are listed below:

- 0% Error Baud Rate by floating-point count register.
- Supports receive time-out interrupt.
- Supports direct memory access and interrupt.

Table 8. Pin Assignment of USART: External Pins

Pin Name	Type	Description
TXDn	O	UART transmit output
RXDn	I	UART transmit input
SSn	I/O	SPI serial port I/O signal for slave selection
SCKn	I/O	SPI clock I/O (Master: output/slave: input)
MOSIn	I/O	SPI transmit and receive data (Master: output/slave: input)
MISO _n	I/O	SPI transmit and receive data (Master: input/slave: output)

NOTE:

1. n = 10, 11

2.4.18 Low Power Universal Asynchronous Receiver/Transmitter (LPUART)

The A34L716 series has a built-in two-channel low-power UART module (Universal Asynchronous Receiver/Transmitter).

This Low Power UART (LPUART) supports asynchronous serial communication up to 9600bps in DEEP-SLEEP mode with a 32.768 kHz sub-oscillator. It also supports 1-wire half-duplex communication.

LPUART 0/1 of the A34L716 series features the following:

- Full-duplex and half-duplex operations
- Baud rate generator
- Supports serial frames with 5, 6, 7, or 8 Data bits and 1 or 2 Stop bits
- Odd or even parity generation and parity check supported by hardware
- Supports the receive character detection and receive time-out function
- Baud rate compensation function
- Supports up to 9,600 pbs with 32.768 kHz sub-oscillator
- Data overrun detection
- Framing error detection
- Double-speed asynchronous communication mode

2.4.19 USB Full-speed Device Interface

The USB block of the A34L716 series controls an interface between a full-speed USB bus and the AHB bus.

There are 5 endpoints in this controller. Each endpoint can be configured as an IN or OUT endpoint. It is compliant with USB 2.0 full-speed device specification and supports control/bulk/interrupt transfer types.

Isochronous transfers are used for transmitting data, but it is difficult to use in practice because the buffer size is small.

USB suspend/resume is supported, which allows to stop of the device clocks for low-power consumption. Please refer to *Universal Serial Bus Specification Revision 1.1* for details.

The USB of the A34L716 series features the following:

- Compliant with USB 2.0 Full-Speed specification
- Provides 1 interrupt vector with 3 different interrupt events (WAKEUP, USB, and BUS).
- Supports the Control/Bulk/Interrupt transfer type.
- Supports the suspend function when no bus activity exists for 3 ms.
- Provides remote wake-up capability.
- Supports Only Full-Speed (FS, 12 Mbps)
- Configurable number of endpoints from 1 to 5
- Two USB DMA channels, 64 bytes buffer size

2.4.20 LCD Driver/Controller

The LCD drives up to eight common terminals and 44 segment terminals to drive up to 320 pixels.

The LCD can continue its operation even during SLEEP mode and DEEP-SLEEP mode if it uses a selected clock for the LCD driver.

A clock and the duty of the LCD driver are initialized by hardware whenever a value is written to the control register. Therefore, it is recommended not to rewrite the LCD_CR frequently.

The LCD of the A34L716 series features the following:

- Supports resistor bias, capacitor bias
- Supports 1/2, 1/3, 1/4, 1/5, 1/6 and 1/8 duty
- Supports 1/2, 1/3, and 1/4 bias

2.4.21 Analog-to-Digital Converter (ADC)

The A34L716 series features a 12-bit resolution Analog-to-Digital Converter (ADC) module. It consists of two independently controllable units and supports up to 24 different analog inputs.

This ADC module can process AD conversion of many different channels in Single mode, Sequential mode, Multiple mode, and Burst mode. It can sample the voltage inputs of multiple channels at critical times, which is required for various applications and can be achieved using the triggering functionality in association with TIMER.

Once the AD conversion is complete, the result is left aligned in 16-bit data registers.

The ADC is mapped to the AHB and capable of high-speed operation based on the internal clock source. In addition, it uses built-in DMA to reduce the microcontroller's core load while enabling fast data sampling.

The analog input monitoring and comparison capabilities of the ADC allow the applications to determine whether the input voltage is above or below the predefined level.

2.4.22 Voltage Reference Buffer (VREFBUF)

The A34L716 device embeds a voltage reference buffer, which can be used as a voltage reference for ADCs and DACs. It can also be used as a voltage reference for external components via the AREF+ pin.

The internal voltage reference buffer supports two voltages:

- 2.0 V
- 2.5 V

An external voltage reference can be provided via the AREF+ pin when the internal voltage reference buffer is off. Even when external voltage reference is used, it is needed to select a reference source via the VREFBUF_CR register.

VREFBUF must be set before using ADC, DAC, and OPAMP.

2.4.23 Operational Amplifier (OPAMP)

The following are characteristics of the operational amplifiers (OPAMP) built in the A34L716.

- Two OPAMP units are available
- OPAMP outputs are used in connection with ADC channels

2.4.24 Digital-to-Analog Converter (DAC)

The DAC module is a 12-bit, voltage output digital-to-analog converter. The DAC features two output channels, each with its converter. An input reference pin, AREF+ (shared with other analog peripherals), is available for better resolution. An internal reference can also be set on the same input. For more information, see the voltage reference buffer (VREFBUF) section.

The DAOn pin can be used as general-purpose input/output (GPIO) when the DAC output is disconnected from the output pad and connected to the on-chip peripheral.

The DAC output buffer can be optionally enabled to allow a high drive output current.

The DAC of the A34L716 has the following features.

- Two DAC converters: one output channel each
- Synchronized update capability
- Dual DAC channel for independent conversions
- DAC output channel buffered/unbuffered modes
- Each DAC output can be disconnected from the DAOn output pin
- DAC output connection to on-chip peripherals
- Input voltage reference, AREF+

2.4.25 Cyclic Redundancy Check Calculation Module (CRC)

A Cyclic Redundancy Check (CRC) module is used to get 32-bit, 16-bit USB, 16-bit CCITT, and 8-bit CCITT codes from 8-bit or 32-bit data sizes. Application programs employ CRC-based technologies to examine the integrity of data transfers, storage, and Flash memories in conformance with functional safety standards.

The CRC module allows users to examine the integrity of transfer data and Flash memory data. Specifically, the CRC module of the A34L716 supports DMA.

2.4.26 Real Time Clock and Calendar (RTCC)

The Real Time Clock and Calendar (RTCC) of the A34L716 series provides an automatic wakeup function to manage all low-power modes.

The RTCC is an independent BCD timer/counter. It provides a time-of-day clock/calendar with a programmable alarm interrupt. In addition, it includes a periodic programmable wakeup flag with interrupt capability. Eight RTCC counters contain the sub-seconds, seconds, minutes, hours, weeks, days, months, and years expressed in binary-coded decimal format (BCD). Compensations for 28-, 29- (leap year), 30-, and 31-day months are performed automatically. An error correction is available to compensate for variations in crystal oscillator accuracy.

In any mode of operation, the sub-second counter is never accessible. In normal operating mode, seven RTCC counters are protected from read and write access. Read and write operation is possible only in RW mode. If the supply voltage remains in the operating range, the RTCC never stops, regardless of the status of the device.

The RTCC of the A34L716 series has the following features.

- LSI40 kHz and MCCR2 clock as RTCC clock (f_{RTCC})
- Counters of year, month, week, day, hour, minute, and second (up to 99 years)
- Constant-period matching interrupt function (period: 0.5 seconds, 1 second, 1 minute, 1 hour, 1 day, 1 month)
- Alarm interrupt function (alarm: week, hour, minute)
- Timestamp interrupt and function
- Pin output of 1 Hz clock
- Error correction by 1.53 ppm resolution when using 32,768 Hz LSE

2.5 Development Tools

This chapter describes a wide range of development tools for the A34L716. ABOV offers software tools, debuggers, and programmers to help a user generate the right results to match target applications. ABOV supports the entire development ecosystem of the customers.

2.5.1 Compiler

ABOV semiconductor does not provide any compiler for the A34L716. However, since the A34L716 has ARM's high-speed 32-bit Cortex-M4F Cores for their CPU, you can use all kinds of third-party standard compilers such as Keil C Compiler. These compilers' output debug information can be integrated with our A-Link and A-Link Pro.

Please visit our website, www.abovsemi.com, for more information regarding the A-Link and A-Link Pro.

2.5.2 Debugger

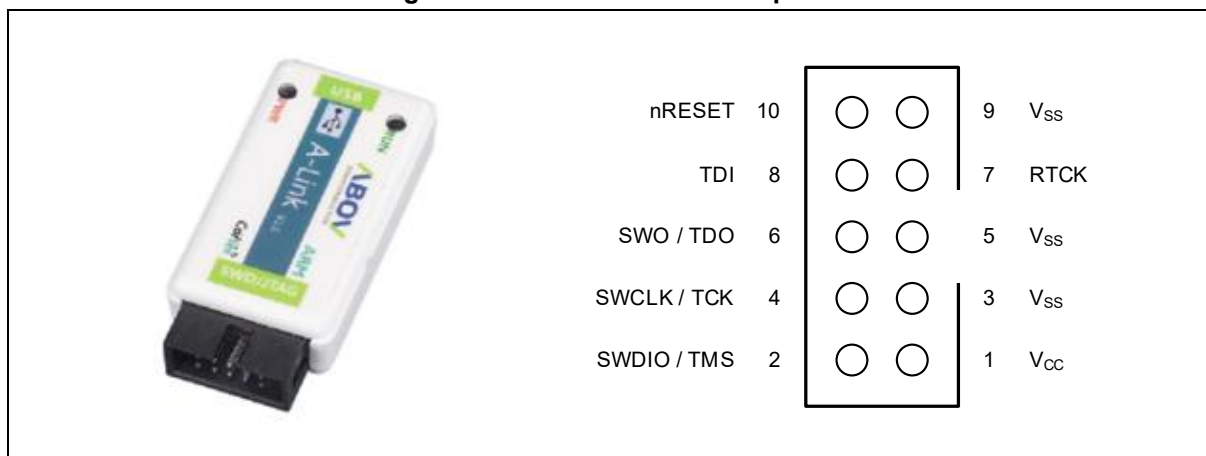
The A-Link and A-Link Pro support the A34L716 microcontroller's emulation in SWD Interface. The A-Link and A-Link Pro use two wires interfacing between the PC and microcontroller, which is attached to the user's system. The A-Link and A-Link Pro can read or change the value of the microcontroller's internal memory and I/O peripherals. In addition, the A-Link and A-Link Pro control the microcontroller's internal debugging logic. This means that A-Link and A-Link Pro control emulation, step run, monitoring and many more functions regarding debugging.

The A-Link and A-Link Pro run underneath MS operating systems such as MS-Windows as below.

Windows NT/ 2000/ XP/ Vista/ 7/ 8/ 8.1/ 10/ 11 (32-bit, 64-bit).

Programming information using the A-Link and A-Link Pro are provided in. For more detailed information about the A-Link and A-Link Pro, please visit our website, www.abovsemi.com and download the debugger software and documents.

Figure 2. A-Link and Pin Description



2.5.3 Programmer

2.5.3.1 E-PGM+ and E-PGM Serial

E-PGM+ and E-PGM Serial are standalone programmers and allow you to program on the device directly.

- Supports for all ABOV microcontroller devices
- A dedicated tool for mass production
- 40-pin Textool DIP socket for single-chip programming (E-PGM+ only)
- 10-pin connector for ISP mode
- USB host interface
- HEX downloads and controls

Figure 3. E-PGM+ (Single Writer) and Pin Descriptions



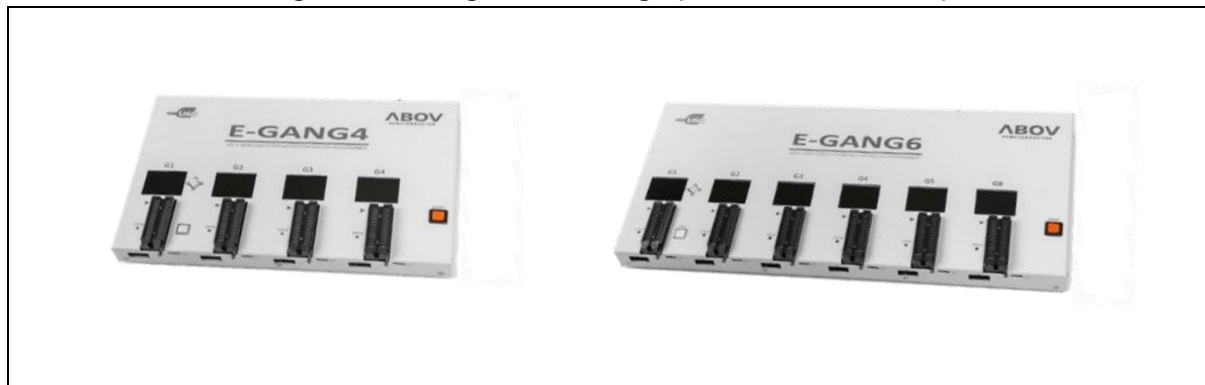
2.5.3.2 Gang Programmer

E-Gang4 and E-Gang6 allows a user to program on multiple devices at a time. They run not only in host-controlled mode but also in standalone mode without host control. USB interface is available, and it is easy to connect to the handler.

Table 9. Specification of E-Gang4 and E-Gang6

Gang Programmer	E-Gang4	E-Gang6
Dimension (x, y, h)	33.5 x 22.5 x 35 mm	148.2 x 22.5 x 35 mm
Weight	2.0 kg	2.8 kg
Input voltage	DC Adaptor 15 V/2 A	DC Adaptor 15 V/2 A
Operating temperature	-10°C to 40°C	-10°C to 40°C
Storage temperature	-30°C to 80°C	-30°C to 80°C
Waterproof	No	No

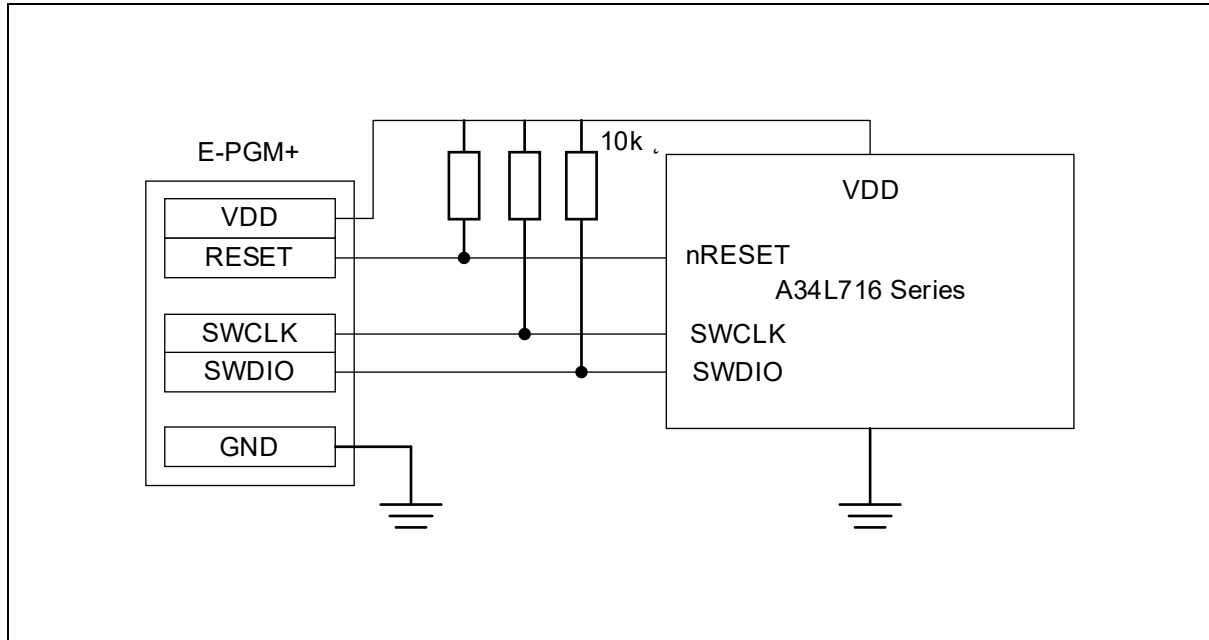
Figure 4. E-Gang4 and E-Gang6 (for Mass Production)



2.5.3.3 SWD Debug Mode and E-PGM+ Connection

Connections for the SWD debugger interface or E-PGM+ are described in Figure 5.

Figure 5. SWD Debugger Interface between A34L716 Series and E-PGM+



3. Pinouts and Pin Descriptions

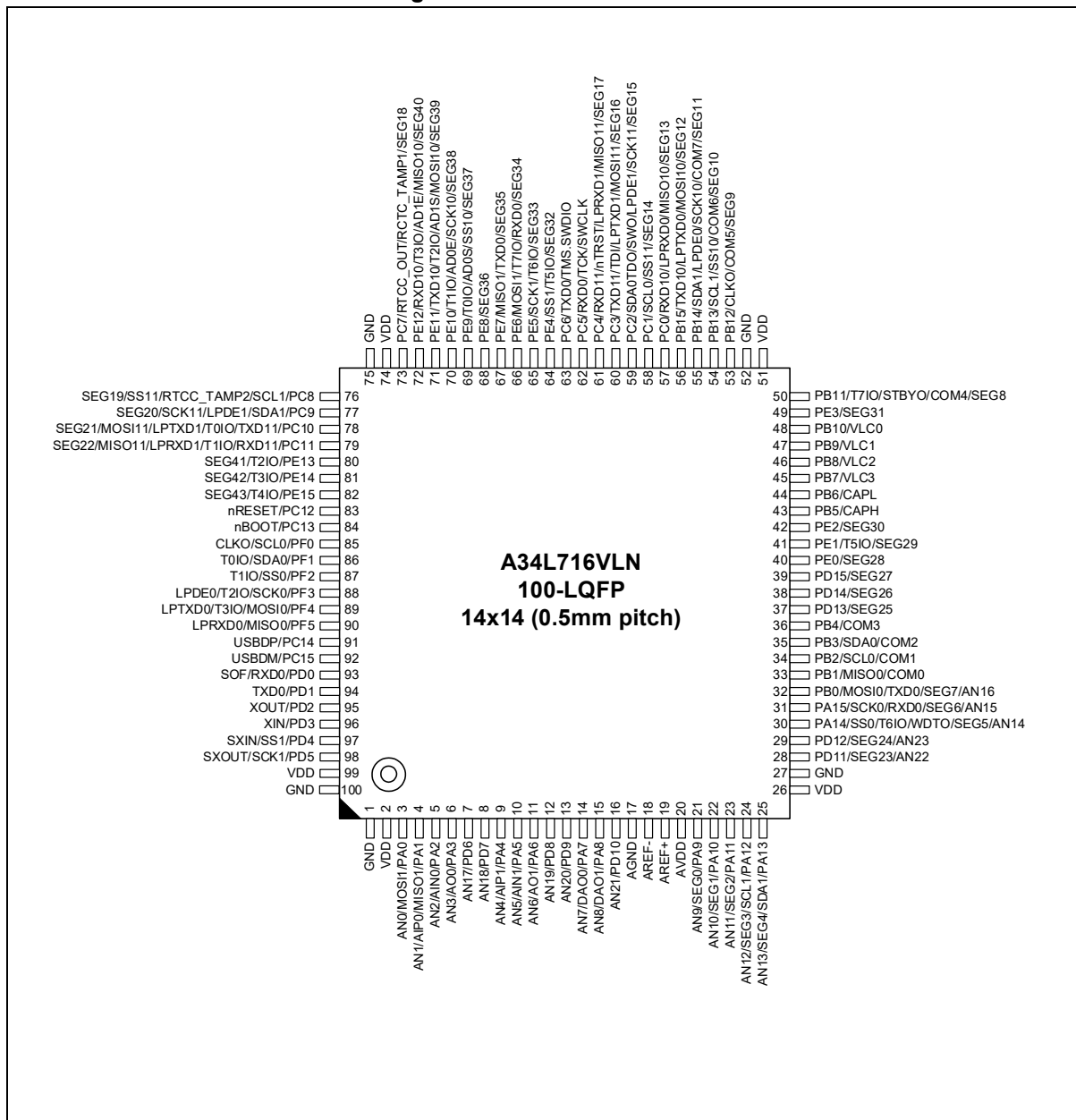
In this chapter, pinouts and pin descriptions of the A34L716 are described.

3.1 Pinouts

Figure 6, Figure 7, and Figure 8 show the top views of the packages.

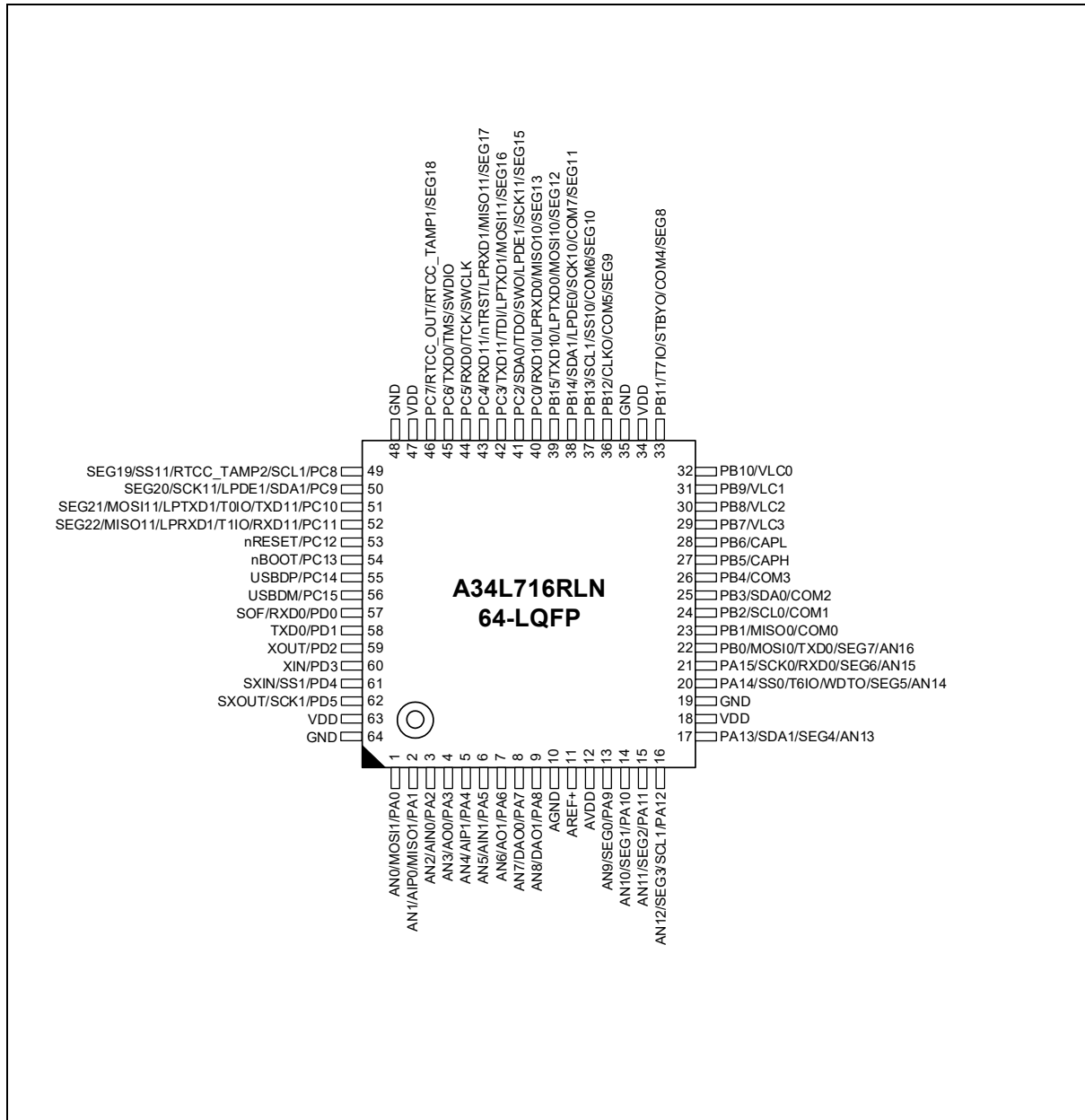
3.1.1 A34L716VLN (100-LQFP)

Figure 6. 100-LQFP Pinouts



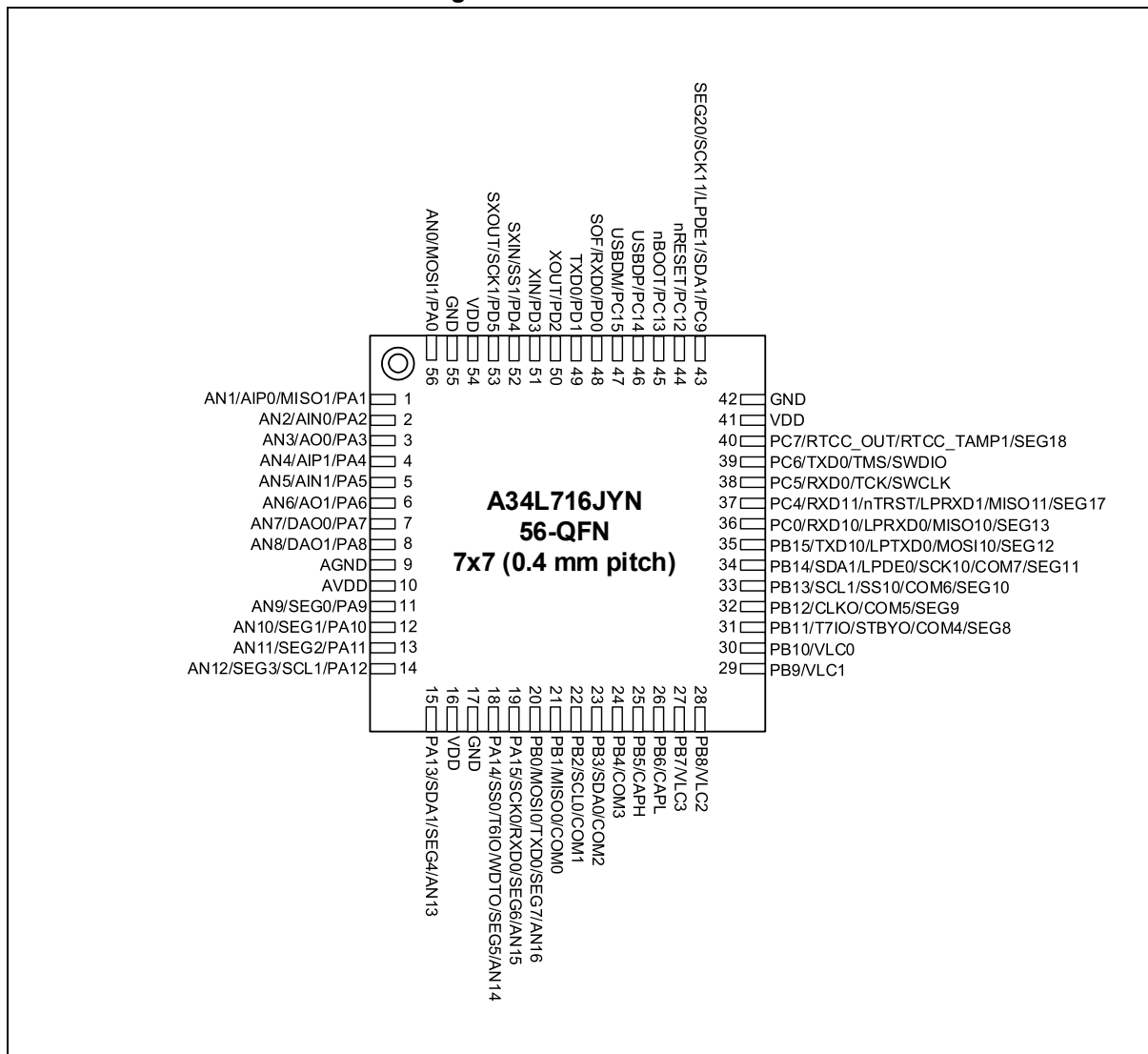
3.1.2 A34L716RLN (64-LQFP)

Figure 7. 64-LQFP Pinouts



3.1.3 A34L716JYN (56-QFN)

Figure 8. 56-QFN Pinouts



3.2 Pin Description

Table 10. Legend and Abbreviations used in Pin Description

Name	Abbreviation	Definition
Pin name	- The pin name is always the same. - Users can set a function on the pin using the alternative function.	
Pin type	I	Input
	O	Output
	I/O	Input/Output
	U	Pull-up
	D	Pull-down
	S	Schmitt-Trigger Input
	C	CMOS Input
	A	Analog
	P	Power
Pin function	Alternate functions	Functions selected through Pn_MR1/2 (PORT n mux1/2 select register) registers

NOTES

1. “*” means ‘selected pin function after reset condition’.
2. Unused pins are set to output from Firmware (low output is recommended).
3. Pin order may be changed with a revision notice.
4. PC13 (nBOOT), PC12 (nRESET), PC6 (SWDIO), PC5 (SWCLK)
5. Do not configure unused pins as floating inputs.
6. After a reset, the internal pull-up for the boot pin is enabled.
7. After a reset, the internal pull-up for the serial wire clock (SWCLK) and the serial wire data I/O (SWDIO) is enabled.
8. The SWCLK and SWDIO pins should not be switched to other functions while they are being used.

The pin configuration information in Table 11 contains two pairs of power/ground and other dedicated pins. These multi-function pins have up to five selections of functions, including GPIO. Configuration, including pin ordering, can be changed without notice.

Table 11. Pin Description

Pin Number			Pin Name	Type	Description	Remark
100-LQFP	64-LQFP	56-QFN				
1	-	-	GND	P	GND	
2	-	-	VDD	P	VDD	
3	1	56	PA0	IOUS	PORT A Bit 0 Input/Output	
			MOSI1	IO	SPI CH1 Master Out/Slave In Signal	
			AN0	IA	Analog Input 0	
4	2	1	PA1	IOUS	PORT A Bit 1 Input/Output	
			MISO1	IO	SPI CH1 Master In/Slave Out Signal	
			AN1/AIP0	IA	Analog Input 1/OPAMP Positive Input 0	
5	3	2	PA2	IOUS	PORT A Bit 2 Input/Output	
			AN2/AIN0	IA	Analog Input 2/OPAMP Negative Input 0	
6	4	3	PA3	IOUS	PORT A Bit 3 Input/Output	
			AN3/AO0	IA	Analog Input 3/OPAMP Output 0	
7	-	-	PD6	IOUS	PORT D Bit 6 Input/Output	
			AN17	IA	Analog Input 17	
8	-	-	PD7	IOUS	PORT D Bit 7 Input/Output	
			AN18	IA	Analog Input 18	
9	5	4	PA4	IOUS	PORT A Bit 4 Input/Output	
			AN4/AIP1	IA	Analog Input 4/OPAMP Positive Input 1	
10	6	5	PA5	IOUS	PORT A Bit 5 Input/Output	
			AN5/AIN1	IA	Analog Input 5/OPAMP Negative Input 1	
11	7	6	PA6	IOUS	PORT A Bit 6 Input/Output	
			AN6/AO1	IA	Analog Input 6/OPAMP Output 1	
12	-	-	PD8	IOUS	PORT D Bit 8 Input/Output	
			AN19	IA	Analog Input 19	
13	-	-	PD9	IOUS	PORT D Bit 9 Input/Output	
			AN20	IA	Analog Input 20	
14	8	7	PA7	IOUS	PORT A Bit 7 Input/Output	
			AN7/DAO0	IOA	Analog Input 7/Digital to analog output 0	
15	9	8	PA8	IOUS	PORT A Bit 8 Input/Output	
			AN8/DAO1	IOA	Analog Input 8/Digital to analog output 1	
16	-	-	PD10	IOUS	PORT D Bit 10 Input/Output	
			AN21	IA	Analog Input 21	

Table 11. Pin Description (continued)

Pin Number			Pin Name	Type	Description	Remark
100-LQFP	64-LQFP	56-QFN				
17	10	9	AGND	P	Analog Ground	
18	-	-	AREF-	P	Analog Reference Ground	
19	11	-	AREF+	P	Analog Reference VDD	
20	12	10	AVDD	P	Analog VDD	
21	13	11	PA9	IOUS	PORT A Bit 9 Input/Output	
			SEG0	OA	LCD Segment Signal Output	
			AN9	IA	Analog Input 9	
22	14	12	PA10	IOUS	PORT A Bit 10 Input/Output	
			SEG1	OA	LCD Segment Signal Output	
			AN10	IA	Analog Input 10	
23	15	13	PA11	IOUS	PORT A Bit 11 Input/Output	
			SEG2	OA	LCD Segment Signal Output	
			AN11	IA	Analog Input 11	
24	16	14	PA12	IOUS	PORT A Bit 12 Input/Output	
			SCL1	IO	I2C CH1 SCL Input/Output	
			SEG3	OA	LCD Segment Signal Output	
			AN12	IA	Analog Input 12	
25	17	15	PA13	IOUS	PORT A Bit 13 Input/Output	
			SDA1	IO	I2C CH1 SDA Input/Output	
			SEG4	OA	LCD Segment Signal Output	
			AN13	IA	Analog Input 13	
26	18	16	VDD	P	VDD	
27	19	17	GND	P	GND	
28	-	-	PD11	IOUS	PORT D Bit 11 Input/Output	
			SEG23	OA	LCD Segment Signal Output	
			AN22	IA	Analog Input 22	
29	-	-	PD12	IOUS	PORT D Bit 12 Input/Output	
			SEG24	OA	LCD Segment Signal Output	
			AN23	IA	Analog Input 23	
30	20	18	PA14	IOUS	PORT A Bit 14 Input/Output	
			SS0	IO	SPI CH0 Select Signal Input/Output	
			T6IO	IO	Timer 6 Input/Output	
			WDTO	O	WDT Output	
			SEG5	OA	LCD Segment Signal Output	
			AN14	IA	Analog Input 14	
31	21	19	PA15	IOUS	PORT A Bit 15 Input/Output	
			SCK0	IO	SPI CH0 Clock Input/Output	
			RXD0	I	UART CH0 RXD Input	
			SEG6	OA	LCD Segment Signal Output	
			AN15	IA	Analog Input 15	

Table 11. Pin Description (continued)

Pin Number			Pin Name	Type	Description	Remark
100-LQFP	64-LQFP	56-QFN				
32	22	20	PB0	IOUS	PORT B Bit 0 Input/Output	
			MOSI0	IO	SPI CH0 Master Out/Slave In Signal	
			TXD0	O	UART Channel 0 TXD Output	
			SEG7	OA	LCD Segment Signal Output	
			AN16	IA	Analog Input 16	
33	23	21	PB1	IOUS	PORT B Bit 1 Input/Output	
			MISO0	IO	SPI CH0 Master In/Slave Out Signal	
			COM0	OA	LCD Common Signal Output	
34	24	22	PB2	IOUS	PORT B Bit 2 Input/Output	
			SCL0	IO	I2C CH0 SCL Input/Output	
			COM1	OA	LCD Common Signal Output	
35	25	23	PB3	IOUS	PORT B Bit 3 Input/Output	
			SDA0	IO	I2C CH0 SDA Input/Output	
			COM2	OA	LCD Common Signal Output	
36	26	24	PB4	IOUS	PORT B Bit 4 Input/Output	
			COM3	OA	LCD Common Signal Output	
37	-	-	PD13	IOUS	PORT D Bit 13 Input/Output	
			SEG25	OA	LCD Segment Signal Output	
38	-	-	PD14	IOUS	PORT D Bit 14 Input/Output	
			SEG26	OA	LCD Segment Signal Output	
39	-	-	PD15	IOUS	PORT D Bit 15 Input/Output	
			SEG27	OA	LCD Segment Signal Output	
40	-	-	PE0	IOUS	PORT E Bit 0 Input/Output	
			SEG28	OA	LCD Segment Signal Output	
41	-	-	PE1	IOUS	PORT E Bit 1 Input/Output	
			T5IO	IO	Timer 5 Input/Output	
			SEG29	OA	LCD Segment Signal Output	
42	-	-	PE2	IOUS	PORT E Bit 2 Input/Output	
			SEG30	OA	LCD Segment Signal Output	
43	27	25	PB5	IOUS	PORT B Bit 5 Input/Output	
			CAPH	I	Capacitor terminal for voltage booster	
44	28	26	PB6	IOUS	PORT B Bit 6 Input/Output	
			CAPL	I	Capacitor terminal for voltage booster	
45	29	27	PB7	IOUS	PORT B Bit 7 Input/Output	
			VLC3	A/OA	LCD bias voltage input/output	

Table 11. Pin Description (continued)

Pin Number			Pin Name	Type	Description	Remark
100-LQFP	64-LQFP	56-QFN				
46	30	28	PB8	IOUS	PORT B Bit 8 Input/Output	
			VLC2	A/OA	LCD bias voltage input/output	
47	31	29	PB9	IOUS	PORT B Bit 9 Input/Output	
			VLC1	A/OA	LCD bias voltage input/output	
48	32	30	PB10	IOUS	PORT B Bit 10 Input/Output	
			VLC0	A/OA	LCD bias voltage input/output	
49	-	-	PE3	IOUS	PORT E Bit 3 Input/Output	
			SEG31	OA	LCD Segment Signal Output	
50	33	31	PB11	IOUS	PORT B Bit 11 Input/Output	
			T7IO	IO	Timer 7 Input/Output	
			STBYO	O	Power-down Mode Indication Signal	
			COM4/SEG8	OA	LCD Common Signal Output/ LCD Segment Signal Output	
51	34	-	VDD	P	VDD	
52	35	-	GND	P	Ground	
53	36	32	PB12	IOUS	PORT B Bit 12 Input/Output	
			CLKO	O	System Clock Output	
			COM5/SEG9	OA	LCD Common Signal Output/ LCD Segment Signal Output	
54	37	33	PB13	IOUS	PORT B Bit 13 Input/Output	
			SCL1	IO	I2C CH1 SCL Input/Output	
			SS10	I	SPI (USART) CH0 slave selects input.	
			COM6/SEG10	OA	LCD Common Signal Output/ LCD Segment Signal Output	
55	38	34	PB14	IOUS	PORT B Bit 14 Input/Output	
			SDA1	IO	I2C CH1 SDA Input/Output	
			LPDE0	O	LPUART CH0 DE Signal Output	
			SCK10	IO	SPI clock input/output	
			COM7/SEG11	OA	LCD Common Signal Output/ LCD Segment Signal Output	
56	39	35	PB15	IOUS	PORT B Bit 15 Input/Output	
			TXD10	O	UART (USART) CH0 data output	
			LPTXD0	O	LPUART CH0 Data Output	
			MOSI10	IO	SPI (USART) CH0 master output, slave input	
			SEG12	OA	LCD Segment Signal Output	

Table 11. Pin Description (continued)

Pin Number			Pin Name	Type	Description	Remark
100-LQFP	64-LQFP	56-QFN				
57	40	36	PC0	IOUS	PORT C Bit 0 Input/Output	
			RXD10	I	UART (USART) CH0 data input	
			LPRXD0	I	LPUART CH0 Data Input	
			MISO10	IO	SPI (USART) CH0 master input, slave output	
			SEG13	OA	LCD Segment Signal Output	
58	-	-	PC1	IOUS	PORT C Bit 1 Input/Output	
			SCL0	IO	I2C CH0 SCL Input/Output	
			SS11	I	SPI (USART) CH1 slave selects input.	
			SEG14	OA	LCD Segment Signal Output	
59	41	-	PC2	IOUS	PORT C Bit 2 Input/Output	
			SDA0	IO	I2C CH0 SDA Input/Output	
			LPDE1	O	LPUART CH1 DE Signal Output	
			SCK11	IO	SPI (USART) CH1 clock input/output	
			SEG15	OA	LCD Segment Signal Output	
			TDO/SWO*	O	JTAG TDO Output, Serial Wire Output	
60	42	-	PC3	IOUS	PORT C Bit 3 Input/Output	
			TXD11	O	UART (USART) CH1 data output	
			LPTXD1	O	LPUART CH1 Data Output	
			MOSI11	IO	SPI (USART) CH1 master output, slave input	
			SEG16	OA	LCD Segment Signal Output	
			TDI*	I	JTAG TDI Input	Internal pull-up enable
61	43	37	PC4	IOUS	PORT C Bit 4 Input/Output	
			RXD11	I	UART (USART) CH1 data input	
			LPRXD1	I	LPUART CH1 Data Input	
			MISO11	IO	SPI (USART) CH1 master input, slave output	
			SEG17	OA	LCD Segment Signal Output	
			nTRST*	I	JTAG nTRST Input	Internal pull-up enable
62	44	38	PC5	IOUS	PORT C Bit 5 Input/Output	
			RXD0	I	UART CH0 RXD Input	
			TCK/SWCLK*	I	JTAG TCK, SWD Clock Input	Internal pull-up enable

Table 11. Pin Description (continued)

Pin Number			Pin Name	Type	Description	Remark
100-LQFP	64-LQFP	56-QFN				
63	45	39	PC6	IOUS	PORT C Bit 6 Input/Output	
			TXD0	O	UART CH0 TXD Output	
			TMS/SWDIO*	I	JTAG TMS, SWD Data Input/Output	Internal pull-up enable
64	-	-	PE4	IOUS	PORT E Bit 4 Input/Output	
			SS1	IO	SPI CH1 Select Signal Input/Output	
			T5IO	IO	Timer 5 Input/Output	
			SEG32	OA	LCD Segment Signal Output	
65	-	-	PE5	IOUS	PORT E Bit 5 Input/Output	
			SCK1	IO	SPI CH1 Clock Input/Output	
			T6IO	IO	Timer 6 Input/Output	
			SEG33	OA	LCD Segment Signal Output	
66	-	-	PE6	IOUS	PORT E Bit 6 Input/Output	
			MOSI1	IO	SPI CH1 Master Out/Slave In Signal	
			T7IO	IO	Timer 7 Input/Output	
			RXD0	I	UART CH0 RXD Input	
			SEG34	OA	LCD Segment Signal Output	
67	-	-	PE7	IOUS	PORT E Bit 7 Input/Output	
			MISO1	IO	SPI CH1 Master input, slave output	
			TXD0	O	UART CH 0 TXD Output	
			SEG35	OA	LCD Segment Signal Output	
68	-	-	PE8	IOUS	PORT E Bit 8 Input/Output	
			SEG36	OA	LCD Segment Signal Output	
69	-	-	PE9	IOUS	PORT E Bit 9 Input/Output	
			T0IO	IO	Timer 0 Input/Output	
			AD0S	O	ADC0 Start of Conversion	
			SS10	I	SPI (USART) CH0 slave selects input.	
			SEG37	OA	LCD Segment Signal Output	
70	-	-	PE10	IOUS	PORT E Bit 10 Input/Output	
			T1IO	IO	Timer 1 Input/Output	
			AD0E	O	ADC0 End of Conversion	
			SCK10	I/O	SPI (USART) CH0 clock input/output	
			SEG38	OA	LCD Segment Signal Output	

Table 11. Pin Description (continued)

Pin Number			Pin Name	Type	Description	Remark
100-LQFP	64-LQFP	56-QFN				
71	-	-	PE11	IOUS	PORT E Bit 11 Input/Output	
			TXD10	O	UART (USART) CH0 data output	
			T2IO	IO	Timer 2 Input/Output	
			AD1S	O	ADC1 Start of Conversion	
			MOSI10	IO	SPI (USART) CH0 Master output, slave input	
			SEG39	OA	LCD Segment Signal Output	
72	-	-	PE12	IOUS	PORT E Bit 12 Input/Output	
			RXD10	I	UART (USART) CH0 data input	
			T3IO	IO	Timer 3 Input/Output	
			AD1E	O	ADC1 End of Conversion	
			MISO10	IO	SPI (USART) CH0 Master input, slave output	
			SEG40	OA	LCD Segment Signal Output	
73	46	40	PC7	IOUS	PORT C Bit 7 Input/Output	
			RTCC_OUT	O	RTCC Output	
			RTCC_TAMP1	I	RTCC TimeStamp Input 1	
			SEG18	OA	LCD Segment Signal Output	
74	47	41	VDD	P	VDD	
75	48	42	GND	P	Ground	
76	49	-	PC8	IOUS	PORT C Bit 8 Input/Output	
			SCL1	IO	I2C CH1 SCL Input/Output	
			RTCC_TAMP2	I	RTCC TimeStamp Input 2	
			SS11	I	SPI (USART) CH1 slave selects input.	
			SEG19	OA	LCD Segment Signal Output	
77	50	43	PC9	IOUS	PORT C Bit 9 Input/Output	
			SDA1	IO	I2C CH1 SDA Input/Output	
			LPDE1	O	LPUART CH1 DE Signal Output	
			SCK11	IO	SPI (USART) CH1 clock input/output	
			SEG20	OA	LCD Segment Signal Output	
78	51	-	PC10	IOUS	PORT C Bit 10 Input/Output	
			TXD11	O	UART (USART) CH1 data output	
			T0IO	IO	Timer 0 Input/Output	
			LPTXD1	O	LPUART CH1 Data Output	
			MOSI11	IO	SPI (USART) CH1 master output, slave input	
			SEG21	OA	LCD Segment Signal Output	

Table 11. Pin Description (continued)

Pin Number			Pin Name	Type	Description	Remark
100-LQFP	64-LQFP	56-QFN				
79	52	-	PC11	IOUS	PORT C Bit 11 Input/Output	
			RXD11	I	UART (USART) CH1 data input	
			T1IO	IO	Timer 1 Input/Output	
			LPRXD1	I	LPUART CH1 Data Input	
			MISO11	IO	SPI (USRAT) CH1 master input, slave output	
			SEG22	OA	LCD Segment Signal Output	
80	-	-	PE13	IOUS	PORT E Bit 13 Input/Output	
			T2IO	IO	Timer 2 Input/Output	
			SEG41	OA	LCD Segment Signal Output	
81	-	-	PE14	IOUS	PORT E Bit 14 Input/Output	
			T3IO	IO	Timer 3 Input/Output	
			SEG42	OA	LCD Segment Signal Output	
82	-	-	PE15	IOUS	PORT E Bit 15 Input/Output	
			T4IO	IO	Timer 4 Input/Output	
			SEG43	OA	LCD Segment Signal Output	
83	53	44	PC12	IOUS	PORT C Bit 12 Input/Output	
			nRESET	I	External Reset Input	Internal pull-up enable
84	54	45	PC13	IOUS	PORT C Bit 13 Input/Output	
			nBOOT	I	Boot Mode Selection Input	Internal pull-up enable
85	-	-	PF0	IOUS	PORT F Bit 0 Input/Output	
			SCL0	IO	I2C CH0 SCL Input/Output	
			CLKO	O	System Clock Output	
86	-	-	PF1	IOUS	PORT F Bit 1 Input/Output	
			SDA0	IO	I2C CH0 SDA Input/Output	
			T0IO	IO	Timer 0 Input/Output	
87	-	-	PF2	IOUS	PORT F Bit 2 Input/Output	
			SS0	I	SPI CH0 slave selects input.	
			T1IO	IO	Timer 1 Input/Output	
88	-	-	PF3	IOUS	PORT F Bit 3 Input/Output	
			SCK0	I/O	SPI CH0 clock input/output	
			T2IO	IO	Timer 2 Input/Output	
			LPDE0	O	LPUART CH0 DE Signal Output	

Table 11. Pin Description (continued)

Pin Number			Pin Name	Type	Description	Remark
100-LQFP	64-LQFP	56-QFN				
89	-	-	PF4	IOUS	PORT F Bit 4 Input/Output	
			MOSI0	IO	SPI CH0 Master output, slave input	
			T3IO	IO	Timer 3 Input/Output	
			LPTXD0	O	LPUART CH0 Data Output	
90	-	-	PF5	IOUS	PORT F Bit 5 Input/Output	
			MISO0	IO	SPI CH0 Master input, slave output	
			LPRXD0	I	LPUART CH0 Data Input	
91	55	46	PC14	IOUS	PORT C Bit 14 Input/Output	
			USBDP	IO	USB Data Line Plus	
92	56	47	PC15	IOUS	PORT C Bit 15 Input/Output	
			USBDM	IO	USB Data Line Minus	
93	57	48	PD0	IOUS	PORT D Bit 0 Input/Output	
			SOF	I	HSICMU External pin	
			RXD0	I	UART CH0 RXD Input	
94	58	49	PD1	IOUS	PORT D Bit 1 Input/Output	
			TXD0	O	UART CH0 TXD Output	
95	59	50	PD2	IOUS	PORT D Bit 2 Input/Output	
			XOUT	OA	External Crystal Oscillator Output	
96	60	51	PD3	IOUS	PORT D Bit 3 Input/Output	
			XIN	IA	External Crystal Oscillator Input	
97	61	52	PD4	IOUS	PORT D Bit 4 Input/Output	
			SS1	IO	SPI CH1 Select Signal Input/Output	
			SXIN	IA	Sub-Crystal Oscillator Input	
98	62	53	PD5	IOUS	PORT D Bit 5 Input/Output	
			SCK1	IO	SPI CH1 Clock Input/Output	
			SXOUT	OA	Sub-Crystal Oscillator Output	
99	63	54	VDD	P	VDD	
100	64	55	GND	P	Ground	

3.3 Alternate Function Pins

The GPIO pins have alternate functions, as described in Table 12.

Table 12. GPIO Alternate Functions

Pin Name	Alternative Function						
	AF0	AF1	AF2	AF3	AF4	AF5	AF7
PA0	PA0	MOSI1					AN0*
PA1	PA1	MISO1					AN1/AIP0*
PA2	PA2						AN2/AIN0*
PA3	PA3						AN3/AO0*
PA4	PA4						AN4/AIP1*
PA5	PA5						AN5/AIN1*
PA6	PA6						AN6/AO1*
PA7	PA7						AN7/DAO0*
PA8	PA8						AN8/DAO1*
PA9	PA9					SEG0	AN9*
PA10	PA10					SEG1	AN10*
PA11	PA11					SEG2	AN11*
PA12	PA12	SCL1				SEG3	AN12*
PA13	PA13	SDA1				SEG4	AN13*
PA14	PA14	SS0	T6IO	WDTO		SEG5	AN14*
PA15	PA15	SCK0		RXD0		SEG6	AN15*
PB0	PB0	MOSI0		TXD0		SEG7	AN16*
PB1	PB1	MISO0				COM0	*
PB2	PB2	SCL0				COM1	*
PB3	PB3	SDA0				COM2	*
PB4	PB4					COM3	*
PB5	PB5					CAPH	*
PB6	PB6					CAPL	*
PB7	PB7					VLC3	*
PB8	PB8					VLC2	*
PB9	PB9					VLC1	*
PB10	PB10					VLC0	*
PB11	PB11		T7IO	STBYO		COM4/SEG8	*
PB12	PB12			CLKO		COM5/SEG9	*
PB13	PB13	SCL1			SS10	COM6/SEG10	*
PB14	PB14	SDA1		LPDE0	SCK10	COM7/SEG11	*
PB15	PB15	TXD10		LPTXD0	MOSI10	SEG12	*
PC0	PC0	RXD10		LPRXD0	MISO10	SEG13	*
PC1	PC1	SCL0			SS11	SEG14	*
PC2	PC2	SDA0	TDO/SWO*	LPDE1	SCK11	SEG15	
PC3	PC3	TXD11	TDI*	LPTXD1	MOSI11	SEG16	
PC4	PC4	RXD11	nTRST*	LPRXD1	MISO11	SEG17	
PC5	PC5	RXD0	TCK/SWCLK*				
PC6	PC6	TXD0	TMS/SWDIO*				
PC7	PC7		RTCC_OUT	RTCC_TAMP1		SEG18	*
PC8	PC8	SCL1		RTCC_TAMP2	SS11	SEG19	*

Table 12. GPIO Alternate Functions (continued)

Pin Name	Alternative Function						
	AF0	AF1	AF2	AF3	AF4	AF5	AF7
PC9	PC9	SDA1		LPDE1	SCK11	SEG20	*
PC10	PC10	TXD11	T0IO	LPTXD1	MOSI11	SEG21	*
PC11	PC11	RXD11	T1IO	LPRXD1	MISO11	SEG22	*
PC12	PC12		nRESET*				
PC13	PC13		nBOOT*				
PC14	PC14				USBDP		*
PC15	PC15				USBDM		*
PD0	PD0	SOF		RXD0			*
PD1	PD1			TXD0			*
PD2	PD2						XOUT*
PD3	PD3						XIN*
PD4	PD4	SS1					SXIN*
PD5	PD5	SCK1					SXOUT*
PD6	PD6						AN17*
PD7	PD7						AN18*
PD8	PD8						AN19*
PD9	PD9						AN20*
PD10	PD10						AN21*
PD11	PD11					SEG23	AN22*
PD12	PD12					SEG24	AN23*
PD13	PD13					SEG25	*
PD14	PD14					SEG26	*
PD15	PD15					SEG27	*
PE0	PE0					SEG28	*
PE1	PE1		T5IO			SEG29	*
PE2	PE2					SEG30	*
PE3	PE3					SEG31	*
PE4	PE4	SS1	T5IO			SEG32	*
PE5	PE5	SCK1	T6IO			SEG33	*
PE6	PE6	MOSI1	T7IO	RXD0		SEG34	*
PE7	PE7	MISO1		TXD0		SEG35	*
PE8	PE8					SEG36	*
PE9	PE9		T0IO	AD0S	SS10	SEG37	*
PE10	PE10		T1IO	AD0E	SCK10	SEG38	*
PE11	PE11	TXD10	T2IO	AD1S	MOSI10	SEG39	*
PE12	PE12	RXD10	T3IO	AD1E	MISO10	SEG40	*
PE13	PE13		T2IO			SEG41	*
PE14	PE14		T3IO			SEG42	*
PE15	PE15		T4IO			SEG43	*
PF0	PF0	SCL0		CLKO			*
PF1	PF1	SDA0	T0IO				*
PF2	PF2	SS0	T1IO				*
PF3	PF3	SCK0	T2IO	LPDE0			*
PF4	PF4	MOSI0	T3IO	LPTXD0			*
PF5	PF5	MISO0		LPRXD0			*

4. Electrical Characteristics

4.1 Parameter Conditions

Unless otherwise specified, all voltages are referenced to GND.

4.1.1 Minimum and Maximum Values

Unless otherwise specified, our production tests guarantee the minimum and maximum values of the device under the worst-case conditions of ambient temperature, supply voltage, and frequency.

Data based on characterization results, design simulation, and/or technical characteristics are not tested in production but are indicated in the table footnotes.

4.1.2 Typical Value

Unless otherwise specified, normal data is under the conditions of $T_A = 25\text{ }^{\circ}\text{C}$ and $V_{DD} = AV_{DD} = 3.3\text{ V}$.

The normal data is provided only as a design guideline and has not been tested.

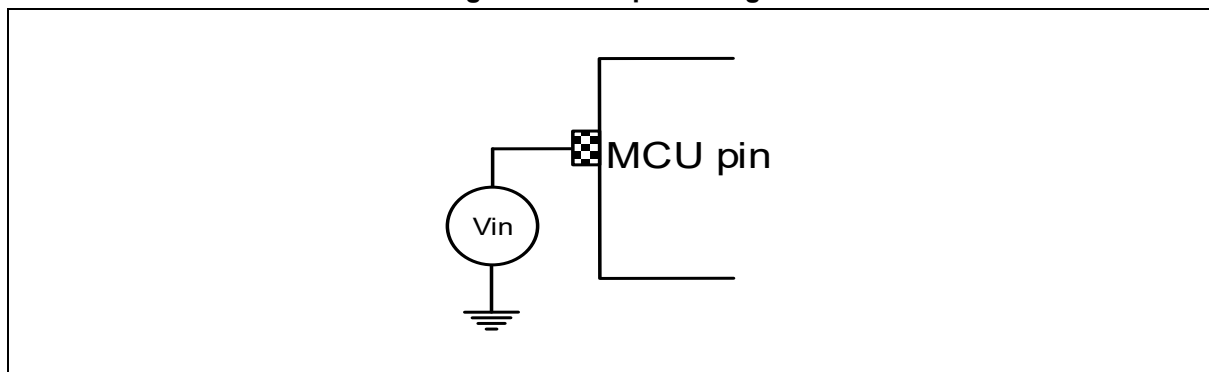
4.1.3 Typical Curves

Unless otherwise specified, all normal curves are provided only as a design guideline and are not tested.

4.1.4 Pin input Voltage

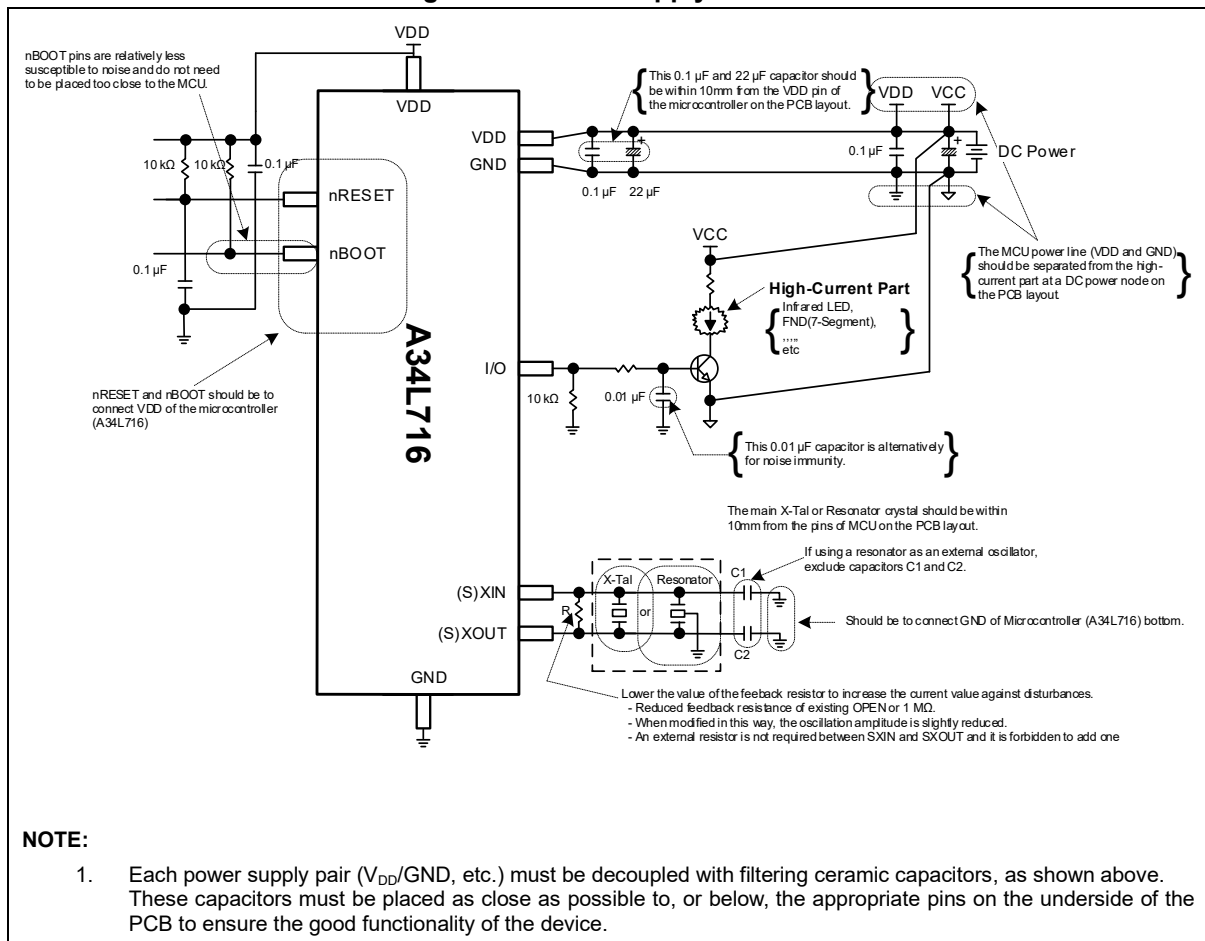
The input voltage measurement on the pin of the device is described in Figure 9

Figure 9. Pin Input Voltage



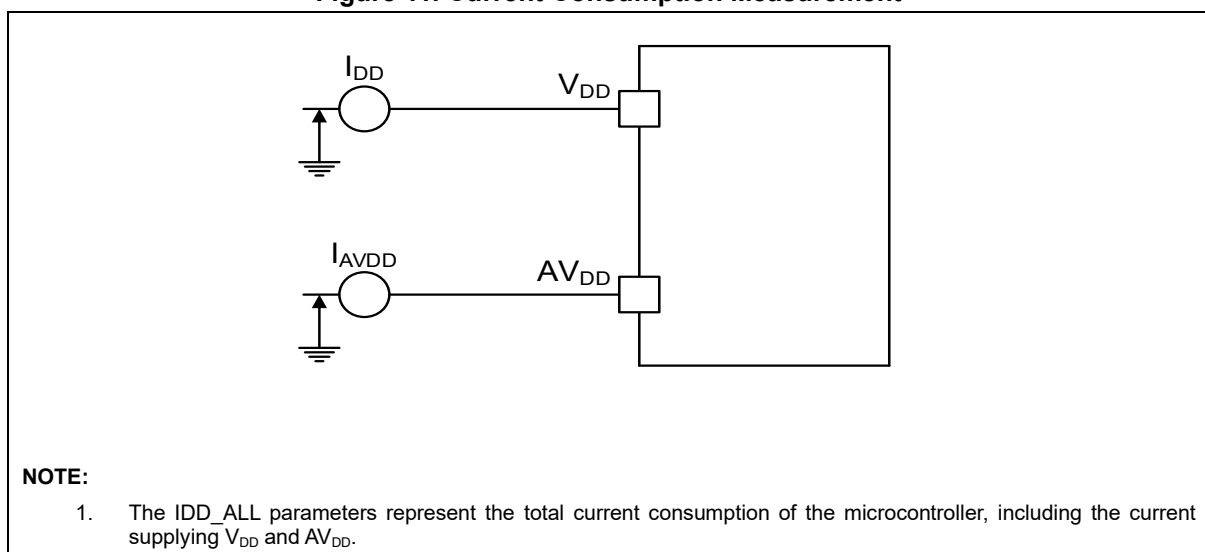
4.1.5 Power Supply Scheme

Figure 10. Power Supply Scheme



4.1.6 Current Consumption Measurement

Figure 11. Current Consumption Measurement



4.2 Absolute Maximum Ratings

Stresses beyond those listed in Table 13, Table 14, and Table 15, voltage characteristics beyond those listed in Table 13, current characteristics beyond those listed in Table 14, and thermal characteristics beyond those listed in Table 15 may cause permanent damage to the device.

This is a stress rating only, and the functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied.

Exposure to above maximum rating conditions for extended periods may affect device reliability.

Table 13. Voltage Characteristics

Symbol	Ratings	Min.	Max.	Unit
V_{DD-GND}	External main supply voltage (including V_{DD} , AV_{DD})	-0.3	4.2	V
$V_I^{(2)}$	Input voltage on I/O	-0.5	Max (V_{DD} , AV_{DD})+0.5	V
V_O	Output voltage on I/O	-0.5	Max (V_{DD} , AV_{DD})+0.5	V

NOTES:

1. All main power (V_{DD} , AV_{DD}) and ground (GND, AGND) pins must always be connected to the external power supply within the permitted range.
2. V_I maximum must always be respected.

Table 14. Current Characteristics

Symbol	Ratings	Max.	Unit
$\sum I_{VDD}$	Total current sum of all V_{DD} power lines (source) ⁽¹⁾	120	mA
$\sum I_{GND}$	Total current out of the sum of all GND ground lines (sink) ⁽¹⁾	120	mA
$I_{VDD(PIN)}$	Maximum current into each V_{DD} power pin (source) ⁽¹⁾	100	mA
$I_{GND(PIN)}$	Maximum current out of each GND ground pin (sink) ⁽¹⁾	-100	mA
$I_{IO(PIN)}$	Output current sink by any I/O	8	mA
	Output current sourced by any I/O and control pin	-8	mA
$\sum I_{IO(PIN)}$	Total output current sunk by the sum of all I/Os and control pins ⁽²⁾	120	mA
	Total output current sourced by the sum of all I/Os and control pins ⁽²⁾	-120	mA
I_{IH}	Input high leakage current	1	μA
I_{IL}	Input low leakage current	1	μA
P_T	Total Power Dissipation	400	mW

NOTES:

1. All main power (V_{DD} , AV_{DD}) and ground (GND, AGND) pins must always be connected to the external power supplies within the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.

Table 15. Thermal Characteristics

Symbol	Ratings	Value	Unit
T _{STG}	Storage temperature range	-55 to +125	°C
T _J	Maximum junction temperature	+105	°C

4.3 Operating Condition

4.3.1 General Operating Condition

Table 16. General Operating Condition

(Temperature: -40°C to +85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V _{DD}	Supply voltage	-	1.8	-	3.6	V
AV _{DD} ⁽²⁾	Analog supply voltage	ADC used	1.8	-	3.6	V
		DAC used	1.8	-	3.6	V
		OPAMP used	1.8	-	3.6	V
		VREFBUF used	2.4	-	3.6	V
		ADC, OPAMP, DAC, VREFBUF not used	1.8	-	3.6	V
FREQ	Operating frequency	HSE	1	-	16	MHz
		LSE	-	32.768	-	kHz
		HSI	31.52	32	32.48	MHz
		LSI40 kHz	28	40	52	kHz
V _{IN}	I/O input voltage	3.3 V I/O	-0.3	-	V _{DD}	V
T _A	Ambient temperature	-	-40	-	85	°C
T _J	Junction temperature range	-	-	-	105	°C

NOTES:

1. When RESET is released, functionality is guaranteed down to V_{LVR0} Min.
2. A_{VDD} must always be supplied at the exact same voltage level as V_{DD} without exception. (A_{VDD} = V_{DD})

4.3.2 Power-On Reset Characteristics

Table 17. POR Electrical Characteristics

(Temperature: -40°C to +85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V _{set}	POR set level	-	1.3	1.4	1.5	V
t _R	V _{DD} voltage rising time	-	0.02	-	20	ms/V
t _F	V _{DD} voltage falling time	-	0.4	-	20	ms/V
V _{reset}	POR reset level	-	1.00	1.2	1.4	V

4.3.3 Operating Condition at Power-up/Power-down

The parameters in Table 18. are derived from tests performed under the ambient temperature conditions summarized in Table 16.

Table 18. Operating Condition at Power-up/Power-down

(Temperature: -40°C to +85°C)

Symbol	Parameter	Conditions	Min.	Max.	Unit
T _{VDD}	V _{DD} rise time rate	-	0.02	20	ms/V
	V _{DD} fall time rate	-	0.4	20	ms/V

4.3.4 Embedded Reset and Power Control Block Characteristics (LVR, LVI)

The parameters in Table 19 and Table 20 are derived from tests performed under the ambient temperature conditions summarized in Table 16.

Table 19. Low-Voltage Reset Characteristics

(Temperature: -40°C to +85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I _{DD} (LVR_LVI)	LVR and LVD Consumption from V _{DD}	-		1	2	μA
V _{LVR0_R}	Detection level	Rising voltage	1.57	1.68	1.79	V
V _{LVR1_R}			1.93	2.08	2.23	
V _{LVR2_R}			2.19	2.36	2.53	
V _{LVR3_R}			2.49	2.69	2.89	
V _{LVR4_R}			2.7	2.92	3.14	
V _{LVR0_F}	Detection level	Falling voltage	1.47	1.58	1.69	V
V _{LVR1_F}			1.81	1.96	2.11	
V _{LVR2_F}			2.06	2.23	2.4	
V _{LVR3_F}			2.34	2.54	2.74	
V _{LVR4_F}			2.53	2.75	2.97	
-	Hysteresis	-	50	100	150	mV
-	Noise cancelling time	-	-	2	-	μs

Table 20. Low-Voltage Indicator Characteristics

(Temperature: -40°C to +85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V _{LVI0_R}	Detection level	Rising voltage	2.00	2.12	2.24	V
V _{LVI1_R}			2.16	2.29	2.42	
V _{LVI2_R}			2.31	2.45	2.59	
V _{LVI3_R}			2.45	2.60	2.75	
V _{LVI4_R}			2.58	2.73	2.88	
V _{LVI5_R}			2.73	2.90	3.06	
V _{LVI6_R}			2.80	2.97	3.14	
V _{LVI0_F}	Detection level	Falling voltage	1.96	2.07	2.15	V
V _{LVI1_F}			2.12	2.24	2.32	
V _{LVI2_F}			2.27	2.40	2.49	
V _{LVI3_F}			2.40	2.54	2.64	
V _{LVI4_F}			2.53	2.67	2.77	
V _{LVI5_F}			2.70	2.85	2.96	
V _{LVI6_F}			2.74	2.90	3.00	
-	Hysteresis	-	20	50	150	mV
-	Noise cancelling time	-	-	2	-	μs

4.3.5 Embedded Voltage Reference

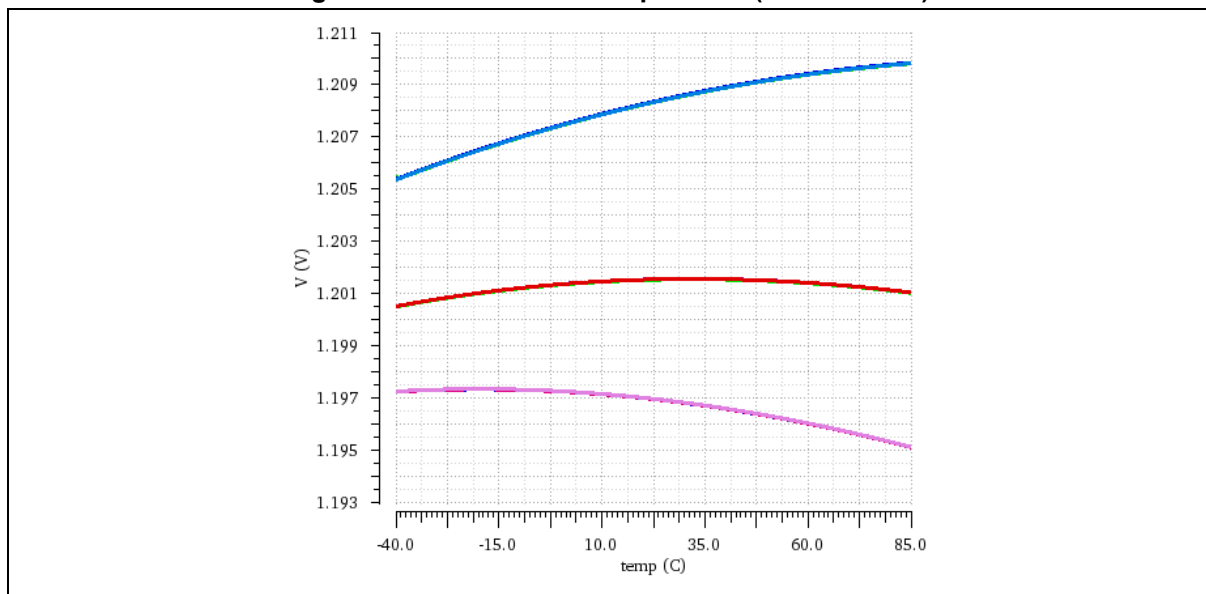
Table 21. Embedded Internal Voltage Reference

(Temperature: -40°C to +85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$AV_{DD}^{(3)}$	Analog Supply Voltage	VREF_SEL = 0	2.4	-	3.6	V
		VREF_SEL = 1	2.8	-	3.6	
V_{REFBUF_OUT}	Voltage reference output	VREF_SEL = 0	1.96	2	2.04	
		VREF_SEL = 1	2.45	2.5	2.55	
V_{REFINT}	Internal reference voltage	-40°C < T _A < +85°C	1.182	1.2	1.218	V
$I_{DD} (V_{REFINTBUF})$	V_{REFINT} buffer consumption from V _{DD} when converted by ADC	-	-	12.5	20	μA
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	$AV_{DD} = 3\text{ V}$	-	5	7.5	mV
T_{Coeff}	V_{REFINT} temperature coefficient	-40°C < T _A < +85°C	-	16	50	ppm/°C
$V_{DDCoeff}$	Average voltage coefficient	3.0 V < V _{DD} < 3.6 V	-	250	1200	ppm/V
C_L	Load Capacitor	-	0.5	1	1.5	μF
ESR	An Equivalent Serial Resistor of C _L	-	-	-	2	Ω
t_{START}	Start-up time of V _{REFBUF_OUT}	Internal mode	-	-	2	ms
		Bypass mode	-	-	2.5	
T_{Coeff}	V_{REFBUF_OUT} Temperature Coefficient	-	-	-	100	ppm/°C

NOTES:

1. The shortest sampling time is determined in the application by multiple iterations.
2. Guaranteed by design.
3. AV_{DD} must always be supplied at the exact same voltage level as V_{DD} without exception. ($AV_{DD} = V_{DD}$)

Figure 12. VREFINT vs. Temperature (-40°C ~ 85°C)

4.3.6 Supply Current Characteristics

Current consumption is a function of multiple parameters and factors, such as operating voltage, ambient temperature, I/O pin load, device software configuration, operating frequency, I/O pin switching speed, program location in memory, and binary code that was executed.

Current consumption is measured as described in Table 22.

4.3.6.1 Supply Current Consumption

Table 22. Supply Current Characteristics

(Temperature: -40°C to +85°C)

Symbol	Operation Mode	Condition					Voltage Scaling	Typ.	Max.	Unit
		LSI (40 kHz)	HSI (32 MHz)	HSE (8 MHz)	LSE (32.768 kHz)	f _{MCLK}				
I _{DD} (RUN)	Normal operation ⁽¹⁾	STOP	RUN	STOP	STOP	f _{HSI}	3 V	7.9	-	mA
		STOP	STOP	RUN	STOP	f _{HSE}	3 V	3.3	-	
		STOP	STOP	STOP	RUN	f _{LSE}	3 V	169	-	μA
		STOP	STOP	RUN	STOP	f _{PLL}	3 V	7.9	-	mA
I _{DD} (SLEEP)	SLEEP ⁽¹⁾	STOP	RUN	STOP	STOP	f _{HSI}	3 V	3.3	-	
		STOP	STOP	RUN	STOP	f _{HSE}	3 V	1.1	-	
		STOP	STOP	STOP	RUN	f _{LSE}	3 V	160	-	
		STOP	STOP	RUN	STOP	f _{PLL}	3 V	3.4	-	mA
I _{DD} (STOP 1)	DEEP-SLEEP ⁽¹⁾	VDC=STOP, RTCC(LSE)=ON					3 V	1.79	-	μA
		VDC=STOP, RTCC(LSI)=ON					3 V	1.79	-	
I _{DD} (STOP 2)	DEEP-SLEEP ⁽¹⁾	VDC=STOP, LVD=ON					3 V	1.6	-	
		VDC=STOP, LVD=OFF					3 V	1.4	-	

NOTE:

1. All peripherals are turned off.

4.3.6.2 I/O system Current Consumption

The current consumption in the I/O system is due to the two components, Static and Dynamic.

4.3.6.3 I/O static Current Consumption

All I/O pins used as inputs with Pull-ups cause the current consumption when the pins remain Low from the outside. This current consumption value can be calculated simply using the Pull-up/Pull-down resistor value provided in the I/O port characteristics.

To estimate the current consumption at the output pins, users need to consider external Pull-downs or external load.

Additional I/O current consumption can be caused due to the I/Os configured as inputs, if the medium voltage level is applied externally. This current is consumed by the input Schmitt trigger circuit used to tell the input value. Unless the application requires a specific configuration, users can prevent this supply current consumption by configuring the I/Os in an analog mode instead of using the Schmitt circuit. Specifically, input pins of the ADC, OPAMP, and DAC must be configured as analog inputs.

4.3.6.4 I/O Dynamic Current Consumption

The I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin.

4.3.7 External Clock Source Characteristics

4.3.7.1 High-speed External Clock Generated from a Crystal/Ceramic Resonator

A high-speed external clock (HSE) can be supplied with crystal/ceramic resonator oscillators in the range of 1 to 16 MHz. All information provided in this section is based on the design simulation results obtained by the typical external components specified in Table 23.

To minimize the outputs in the application, the resonator and load capacitor must be placed as close to the oscillator pin as possible.

For more information on the distortion and stabilization time, and the resonator characteristics (frequency, package, and accuracy), contact the manufacturer of the crystal resonator.

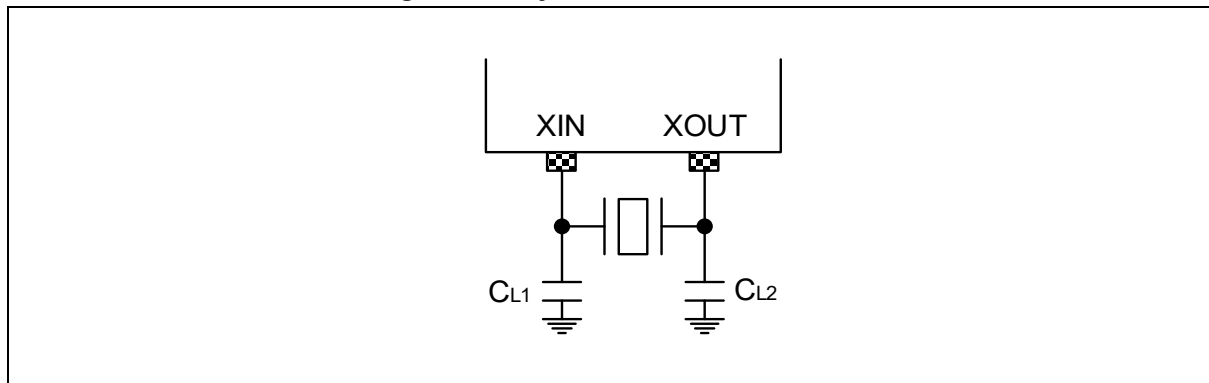
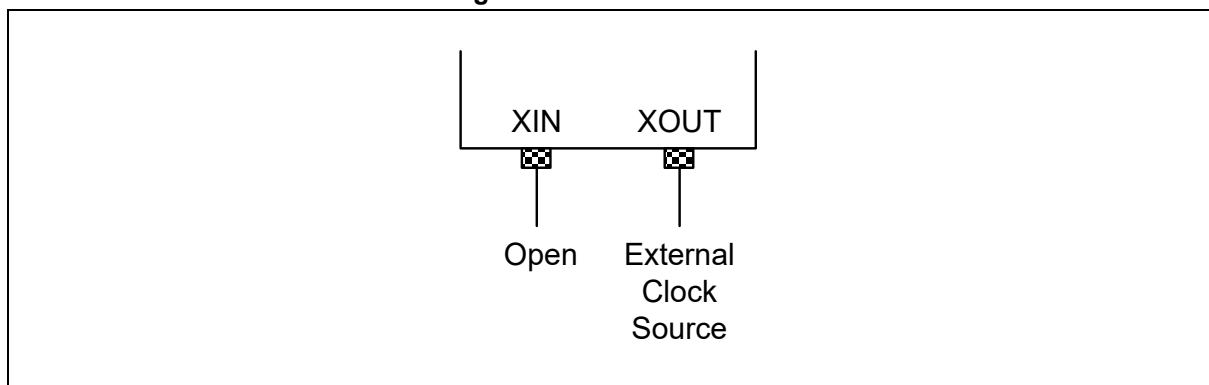
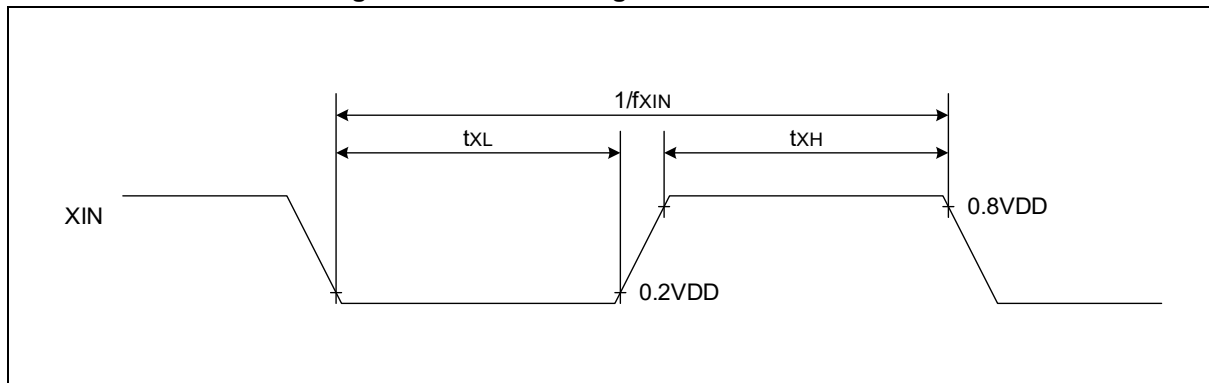
Table 23. HSE Oscillator Characteristics⁽¹⁾

(Temperature: -40°C to +85°C)

Symbol	Parameter	Conditions ⁽²⁾	Min.	Typ.	Max.	Unit
I _{DD(HSE)}	HSE current consumption	-	-	-	2.5	mA
f _{OSC_IN}	Oscillator frequency	-	1	8	16	MHz
f _{OUT}	Output Frequency	V _{DD} ≥ 1.8 V ⁽⁴⁾	1	-	4	MHz
		V _{DD} ≥ 2.0 V ⁽⁵⁾	1	-	8	
		V _{DD} ≥ 2.2 V ⁽⁶⁾	1	-	12	
		V _{DD} ≥ 2.4 V ⁽⁷⁾	1	-	16	
V _{IL}	Crystal input (low)	-	-	-	0.2V _{DD}	V
V _{IH}	Crystal input (high)	-	0.8V _{DD}	-	-	V
V _{OL}	Crystal out (low)	-	-	-	0.2V _{DD}	V
V _{OH}	Crystal out (high)	-	0.8V _{DD}	-	-	V
C _L	External Load Capacitor	1 MHz < f _{OUT} < 4 MHz	18	30	35	pF
		4 MHz < f _{OUT} < 12 MHz	10	22	30	pF
		12 MHz < f _{OUT} < 16 MHz	7	18	22	pF
R _F	Feedback resistor	-	0.7	1.0	1.3	MΩ
t _{SU(HSE)} ⁽³⁾	Startup time	-	-	1	-	ms

NOTES:

- Guaranteed by design.
- The crystal/ceramic resonator manufacturer gives resonator characteristics.
- t_{SU(HSE)} is the startup time measured from the moment it is enabled (by software) until it reaches a stabilized 8 MHz oscillation. This value is measured for a standard crystal resonator, and it can vary significantly with the crystal manufacturer:
- HSEISEL = 0x3, HSENFSEL = 0x0
- HSEISEL = 0x2, HSENFSEL = 0x1
- HSEISEL = 0x1, HSENFSEL = 0x2
- HSEISEL = 0x0, HSENFSEL = 0x3

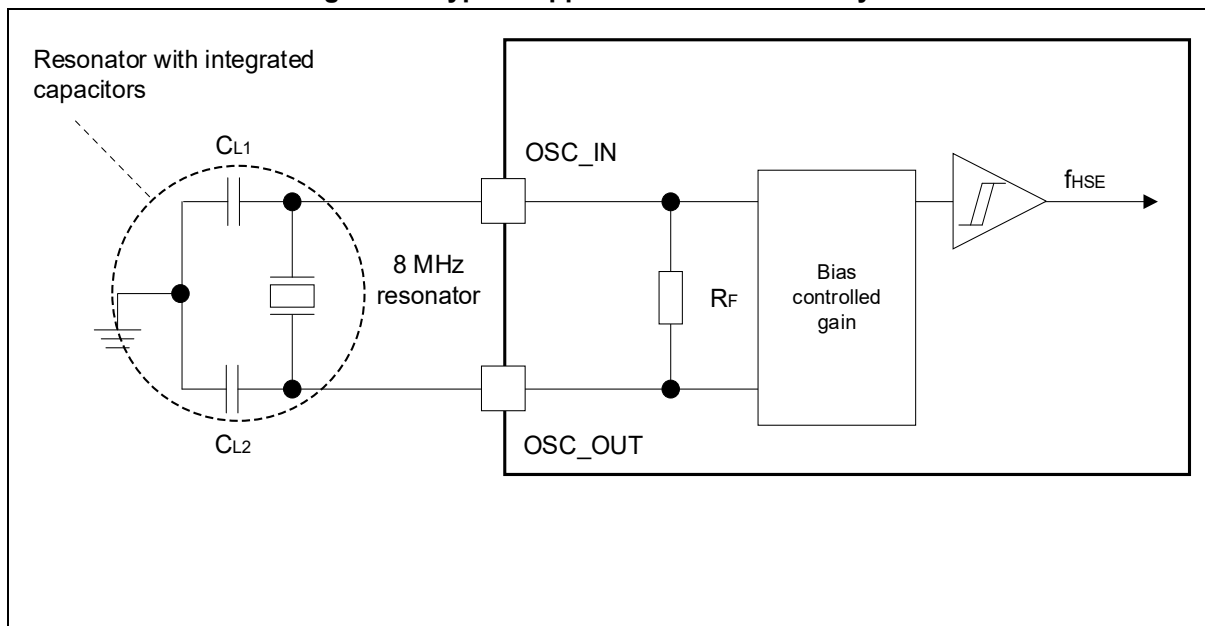
Figure 13. Crystal/Ceramic Oscillator**Figure 14. External Clock****Figure 15. Clock Timing Measurement at XIN**

It is recommended to use high-quality external ceramic capacitors designed for high-frequency applications and selected to match the requirements of the crystal or resonator.

The C_{L1} and C_{L2} are usually the same size. The crystal manufacturers typically specify the load capacitance, a series combination of the C_{L1} and C_{L2} . When adjusting the size of the C_{L1} and C_{L2} , the PCB and microcontroller's pin capacitances must be considered together. (10 pF can be used as a rough estimate of the combined pins and board capacitance.)

Figure 16 shows a circuit diagram of a typical application with an 8 MHz crystal.

Figure 16. Typical Application with 8 MHz Crystal



4.3.7.2 Low-speed External Clock Generated from a Crystal Resonator

A low-speed external clock (LSE) can be supplied with crystal resonator oscillators 32.768 kHz. All information provided in this section is based on the design simulation results obtained from the typical external components specified in Table 24.

To minimize the outputs in the application, the resonator and load capacitor must be placed as close to the oscillator pin as possible.

For more information on the distortion and stabilization time, and the resonator characteristics (frequency, package, and accuracy), contact the manufacturer of the crystal resonator.

Table 24. LSE Oscillator Characteristics (fLSE = 32.768 kHz) ⁽¹⁾

(Temperature: -40°C to +85°C)

Symbol	Parameter	Conditions ⁽²⁾	Min.	Typ.	Max.	Unit
I _{DD(LSE)}	LSE current consumption	-	-	0.3	1	μA
f _{OSC_IN}	Oscillator frequency	-	-	32.768	-	kHz
C _L	External Load Capacitor	-	5	10	15	pF
R _F	Feedback resistor	-	5	18	40	MΩ
t _{SU(LSE)} ⁽²⁾	Startup time	-	-	1	-	s

NOTES:

1. Guaranteed by design.
2. t_{SU(LSE)} is the startup time measured from the moment it is enabled (by software) until it reaches a stabilized 32.768 kHz oscillation. This value is measured for a standard crystal, and it can vary significantly with the crystal manufacturer.

Figure 17. Crystal Oscillator

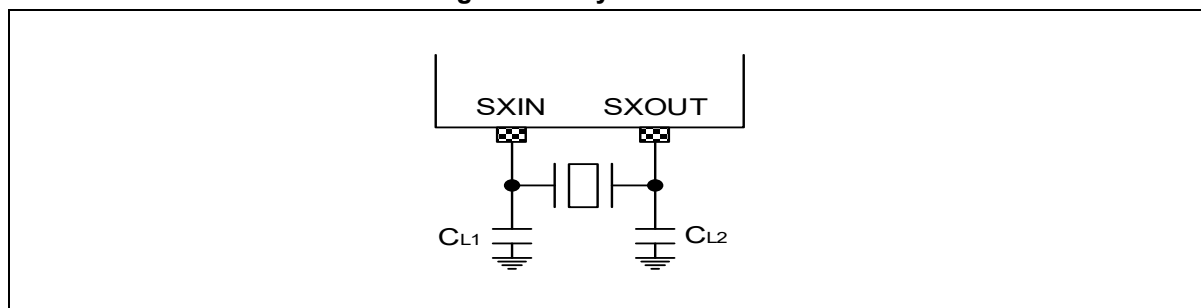
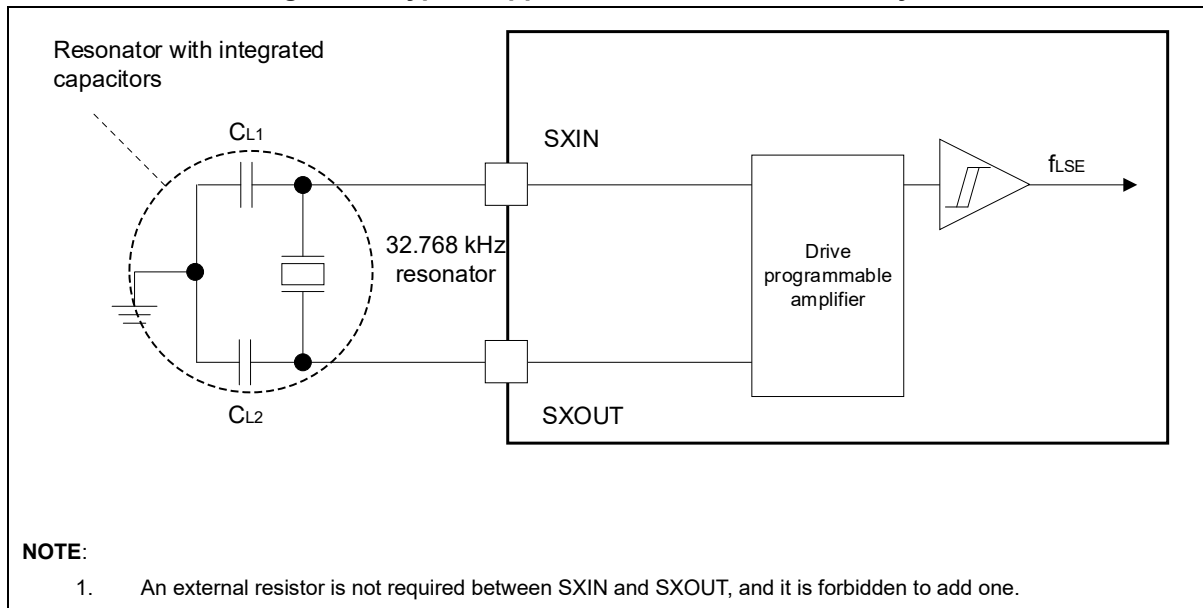
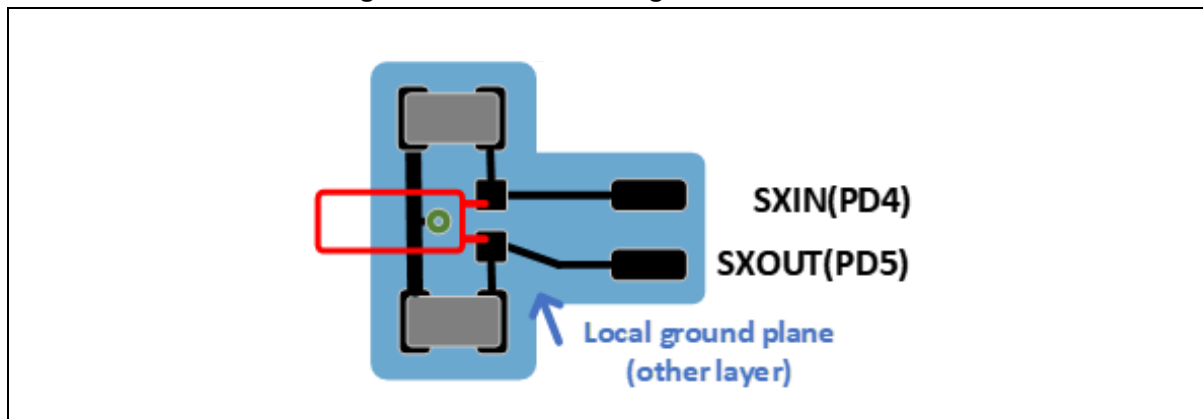


Figure 18. Typical Application with a 32.768 kHz Crystal**Figure 19. LSE PCB Design Considerations**

4.3.8 Internal Clock Source Characteristics

The parameters in Table 25 and Table 26 are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Table 16. The waveforms provided in this section are a characterization result that was not tested during production.

4.3.8.1 High-speed Internal RC Oscillator (HSI32)

Table 25. HSI32 Oscillator Characteristics ⁽¹⁾

(Temperature: -40°C to +85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f _{HSI32}	HSI32 Frequency	V _{DD} =3.0 V, T _A =30°C	31.52	32	32.48	MHz
f _E	Frequency error	TA = -40°C to + 85°C (HSICMU ON, SYNCSRC[1:0]=10 (SOSC)) ⁽²⁾	-0.5	-	0.5	%
		TA = -10°C to + 70°C (HSICMU OFF)	-3	-	3	
		TA = -20°C to + 85°C (HSICMU OFF)	-5	-	5	
t _{stab} (HSI32)	HSI32 oscillator stabilization time	-	-	-	30	μs
I _{DD} (HSI32)	HSI32 oscillator power consumption	-	-	300	350	μA

NOTES:

1. Guaranteed by characterization results and design.
2. The f_E (Frequency Error) value in HSICMU ON state excludes the deviation of the sub crystal (32.768 kHz).
3. HSICMU must be enabled to meet the ±0.5% specification requirement within the -40°C to 85°C range.
4. For detailed information on HSICMU settings, refer to the A34L716 User's Manual.

4.3.8.2 Low-speed Internal 40 kHz RC Oscillator (LSI)

Table 26. LSI Oscillator Characteristics

(Temperature: -40°C to +85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f _{OUT}	Output Frequency	After trim	28	40	52	kHz
t _{STAB} ⁽¹⁾	40 kHz oscillator stabilization time (after LSI40K enable)	5% of final frequency	-	30	250	μs
I _{LSI} ⁽¹⁾	40 kHz oscillator power consumption	Enable	-	150	250	nA
		Disable	-	2	40	

NOTE:

1. Guaranteed by design.

4.3.9 PLL Characteristics

The parameters in Table 27 are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Table 16.

Table 27. PLL Characteristics⁽¹⁾

(Temperature: -40°C to +85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _{DD} (PLL)	Operating current	-	-	1	-	mA
f _{OUT}	Output frequency	-	1	-	48	MHz
f _{VCO}	VCO frequency	-	60	-	192	MHz
f _{DUTY}	Duty	-	40	-	60	%
f _{PLLCLK}	Input frequency	-	2	8	16	MHz
t _{JITTER}	RMS Period Jitter	-	-	-	500	ps
t _{LOCK}	locking time	-	-	100	-	μs

NOTE:

1. Guaranteed by design.

4.3.10 Flash Memory Characteristics

Table 28. Code Flash Memory Characteristics

(Temperature: -40°C to +85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t _{PROG}	Program time	-	-	25	-	μs
t _{SER}	Page erase time	-	-	2	-	ms
t _{MER}	Macro erase time	-	-	8	-	ms
N _{FWE}	Endurance of write/erase	T _A =25°C, Page unit	10,000	-	-	times
t _{FRT}	Retention time	-	10	-	-	years

Table 29. Data Flash Memory Characteristics

(Temperature: -40°C to +85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t _{PROG}	Program time	-	-	25	-	μs
t _{SER}	Page erase time	-	-	2	-	ms
t _{MER}	Macro erase time	-	-	8	-	ms
N _{FWE}	Endurance of write/erase	T _A =25°C, Page unit	100,000	-	-	times
t _{FRT}	Retention time	-	10	-	-	years

4.3.11 I/O Port Characteristics

4.3.11.1 General Input/Output Characteristics

Unless otherwise specified, parameters in Table 30 are derived from tests performed under the conditions summarized in Table 16. All I/Os are designed to be compatible with CMOS and TTL.

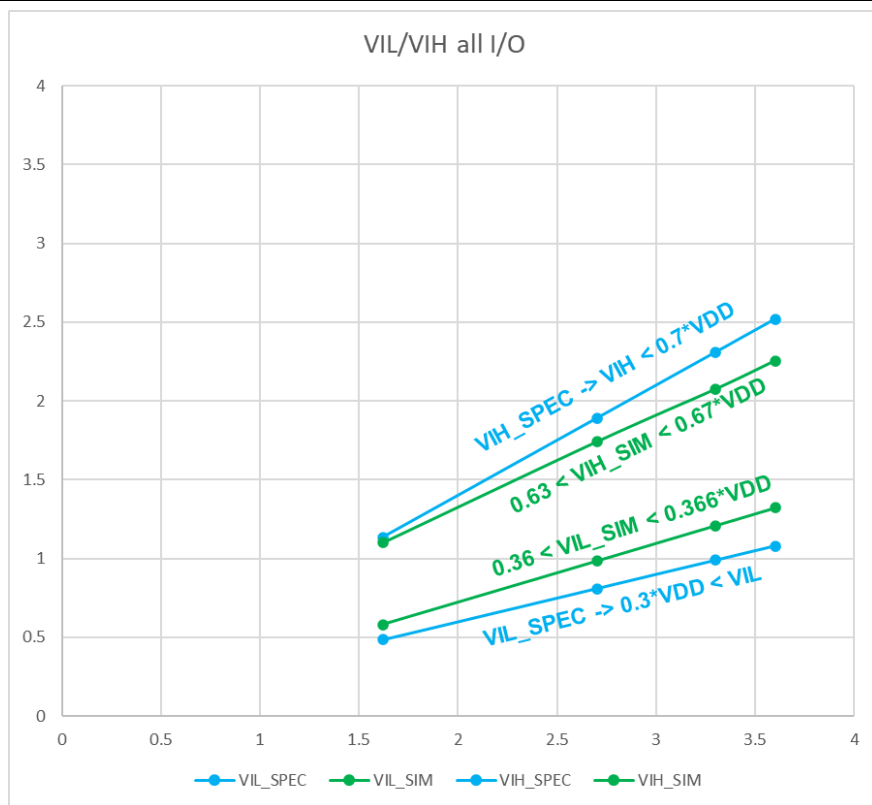
Table 30. I/O Static Characteristics

(Temperature: -40°C to +85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{IL}^{(1)(2)}$	I/O input low-level voltage	$1.8\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	-	-	$0.3 \times V_{DD}$	V
$V_{IH}^{(1)(2)}$	I/O input high-level voltage	$1.8\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	$0.7 \times V_{DD}$	-	-	V
$V_{HYS}^{(3)}$	Input hysteresis	$1.8\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	-	$0.25 \times V_{DD}$	-	mV
I_{leak}	Input leakage current ⁽³⁾	-	-	-	250	nA
R_{PU}	Weak pull-up equivalent resistor	$V_{IN} = G_{ND}$	40	50	60	kΩ
R_{PU}	Weak pulldown equivalent resistor	$V_{IN} = V_{DD}$	40	50	60	
C_{IO}	I/O pin capacitance	I/O pin capacitance	-	5	-	pF
F_{MAX}	Maximum frequency	$C=50\text{ pF}$, $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	-	-	32	MHz
T_R/T_F	Output rise and fall time	$C=50\text{ pF}$, $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	-	10	-	ns

NOTES:

1. Refer to Figure 20.
2. Guaranteed by test in production.
3. Guaranteed by design.

Figure 20. I/O Input Characteristics**NOTE:**

1. X-axis is V_{DD} , Y-axis is VIL/VIH Spec.

4.3.11.2 Output Driving Current

The GPIOs can typically sink or source ± 3 mA and up to ± 8 mA (VOL/VOH mitigation) of the current.

When users set the number of I/O pins that can drive the current in their applications, the number of pins must be limited to comply with the absolute maximum ratings set in section 4.2.

- The sum of the sink current across all I/Os of the GND and the microcontroller's maximum sink current consumption at the GND cannot exceed the absolute maximum ratings Σ IGND. (Refer to Table 13.)

4.3.11.3 Output Voltage Levels

Unless otherwise specified, parameters in Table 31 are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Table 16.

Table 31. Output Voltage Characteristics

(Temperature: -40°C to $+85^{\circ}\text{C}$)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OH}	Output high voltage	Normal GPIO, $V_{DD} > 2.7$ V $I_{OH1} = -3$ mA, $I_{OH2} = -8$ mA	$0.8 \times V_{DD}$	-	-	V
		LCD PAD, $V_{DD} > 2.7$ V $I_{OH1} = -3$ mA, $I_{OH2} = -5$ mA	$0.8 \times V_{DD}$	-	-	
V_{OL}	Output low voltage	Normal GPIO, $V_{DD} > 2.7$ V $I_{OL1} = 3$ mA, $I_{OL2} = 8$ mA	-	-	$0.2 \times V_{DD}$	
		LCD PAD, $V_{DD} > 2.7$ V $I_{OL1} = 3$ mA, $I_{OL2} = 5$ mA	-	-	$0.2 \times V_{DD}$	

NOTE:

- The drive strength of each pin can be selected through the Pn_STR register.

4.3.12 Analog-to-Digital Converter Characteristics

Table 32. ADC Electrical Characteristics

(Temperature: -40°C to +85°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$AV_{DD}^{(1)}$	Analog Power Supply	-	1.8	3.3	3.6	V
AREF+	Positive Reference Voltage	-	1.8	-	AV_{DD}	V
AREF-	Negative Reference Voltage	-	-	AGND	-	V
I_{AVDD}	AV_{DD} Current	Typ @ $AV_{DD} = 3.3$ V, 1 Msps	-	1	-	mA
I_{AREF+}	AREF+ Current	Typ @ $AV_{DD} = 3.3$ V, 1 Msps	-	0.4	-	mA
V_{AIN}	Conversion Voltage Range	-	0	-	AREF+	V
	Channel	-	-	24	-	ch
f_{ADC}	ADC Clock Frequency	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$, $AREF+ = AV_{DD}$	0.48	-	16	MHz
		$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$, $1.98\text{ V} \leq AREF+ < AV_{DD}$		-	8	
		$1.8\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$, $1.8\text{ V} \leq AREF+ < AV_{DD}$		-	4	
t_{CONV}	Total Conversion Time (including sampling time)	$f_{HCLK} = 32\text{ MHz}$ $f_{ADC} = 16\text{ MHz}$	0.93	-	17.31	μs
		-	15	-	277	$1/f_{ADC}$
TUE	Total unadjusted error	Single-ended	-	4.5	6.5	LSB
		Differential	-	4.5	6	
EO	Offset error	Single-ended	-	2.5	3.5	
		Differential	-	2.5	3.5	
EG	Gain error	Single-ended	-	3	5	
		Differential	-	3	4.5	
ED	Differential linearity error	Single-ended	-	1.5	2.0	
		Differential	-	1.2	1.5	
EL	Integral linearity error	Single-ended	-	2.0	4	
		Differential	-	1.5	3.5	

NOTE:

1. AV_{DD} must always be supplied at the exact same voltage level as V_{DD} without exception. ($AV_{DD} = V_{DD}$)

4.3.12.1 General PCB Design Guidelines

The power supplier must be separated, conforming to the scheme shown in Figure 10. The de-coupling capacitors across the V_{DD}/AV_{DD} are ceramic (good quality) capacitors and must be located as close as possible to the chip.

4.3.13 Digital-to-Analog Converter Characteristics

Table 33. DAC Electrical Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Analog Power Supply	$AV_{DD}^{(1)}$	-	1.8	-	3.6	V
Positive reference voltage	AREF+	-	1.8	-	AV_{DD}	V
Negative reference voltage	AREF-	-	-	AGND	-	-
Resistive load	R_L	Connected to GND	5	-	-	k Ω
Capacitive load	C_L	DAC output buffer on	-	-	50	pF
Output impedance	R_O	DAC output buffer off	13	16	-	k Ω
Power supply rejection ratio	PSRR	DAC output buffer on ($C_L = 50$ pF, $R_L = 5$ k Ω)	-	-80	-28	dB
AV_{DD} Current	I_{AVDD}	DAC output buffer on (No load, middle code)	-	315	500	μ A
		DAC output buffer off (No load, middle code)	-	-	0.2	
AREF+ Current	I_{AREF+}	DAC output buffer off (No load, middle code)	-	155	205	μ A
Conversion Voltage Range	V_{DAC_OUT}	DAC output buffer on	0.2	-	AREF+ -0.2	V
		DAC output buffer off	0	-	AREF+	
Setting time	$T_{setting}$	DAC output buffer on ($C_L = 50$ pF, $R_L = 5$ k Ω)	-	7	12	μ s
		DAC output buffer off ($C_L = 10$ pF)	-	1	2	
Wakeup time from off state	T_{wakeup}	DAC output buffer on ($C_L = 50$ pF, $R_L = 5$ k Ω)	-	6	10	μ s
		DAC output buffer off ($C_L = 10$ pF)	-	2	5	
DAC output for a small variation of the input code (1-LSB)	$T_{W_to_W}$	-	1	-	-	μ s
Differential nonlinearity	DNL	DAC output buffer on ($1.8V \leq AV_{DD} = AREF+ < 2.5V$)	-	-	± 6	LSB
		DAC output buffer off ($1.8V \leq AV_{DD} = AREF+ < 2.5V$)	-	-	± 6	
		DAC output buffer on ($2.5V \leq AV_{DD} \leq 3.6V$, $AREF+ = 2V$)	-	-	± 3	
		DAC output buffer off ($2.5V \leq AV_{DD} \leq 3.6V$, $AREF+ = 2V$)	-	-	± 3	

Table 33. DAC Electrical Characteristics (continued)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Integral nonlinearity	INL	DAC output buffer on ($1.8V \leq AV_{DD} = AREF + < 2.5V$)	-	-	± 8	LSB
		DAC output buffer off ($1.8V \leq AV_{DD} = AREF + < 2.5V$)	-	-	± 8	
		DAC output buffer on ($2.5V \leq AV_{DD} \leq 3.6V$, $AREF + = 2V$)	-	-	± 4	
		DAC output buffer off ($2.5V \leq AV_{DD} \leq 3.6V$, $AREF + = 2V$)	-	-	± 4	
Offset error at center code (0x800) after calibration	Offset	DAC output buffer on ($AREF + = 3.6V$)	-	-	± 5	LSB
		DAC output buffer on ($AREF + = 1.8V$)	-	-	± 7	
Offset error at one code (0x001)	Offset1	DAC output buffer off	-	-	± 5	LSB
Gain error	EGAIN	DAC output buffer on	-	-	± 0.5	%
		DAC output buffer off	-	-	± 0.5	
Total unadjusted error	TUE	DAC output buffer on	-	-	± 30	LSB
		DAC output buffer off	-	-	± 12	
Effective number of bits ⁽²⁾	ENOB	DAC output buffer on ($1.8V \leq AV_{DD} = AREF + < 2.5V$, BW 500 kHz)	-	10	-	bits
		DAC output buffer off ($1.8V \leq AV_{DD} = AREF + < 2.5V$, BW 500 kHz)	-	10.5	-	
		DAC output buffer on ($2.5V \leq AV_{DD} \leq 3.6V$, $AREF + = 2V$, BW 500 kHz)	-	10.5	-	
		DAC output buffer off ($2.5V \leq AV_{DD} \leq 3.6V$, $AREF + = 2V$, BW 500 kHz)	-	11	-	

NOTES:

1. AV_{DD} must always be supplied at the exact same voltage level as V_{DD} without exception. ($AV_{DD} = V_{DD}$)
2. Guaranteed by design.

4.3.14 Operational Amplifier Characteristics

Table 34. OPAMP Characteristics (Normal Mode)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Analog Power Supply	$AV_{DD}^{(1)}$	-	1.8	-	3.6	V
OPAMP current consumption	I_{OPAMP}	-	-	150	300	μA
Common mode input range	CMIR	-	0	-	AV_{DD}	V
Input offset voltage	V_{OFFSET}	-	-	-	0.5	mV
Input offset voltage drift	ΔV_{OFFSET}	-	-	± 1	-	$\mu V/^{\circ}C$
Input offset current	I_{IO}	-	-	10	-	pA
Input bias current	I_{IB}	-	-	10	-	pA
Output current load	I_{LOAD}	$AV_{DD} > 2 V$	-	-	500	μA
Resistive load	R_{LOAD}	$AV_{DD} < 2 V$	4	-	-	k Ω
Capacitive load	C_{LOAD}	-	-	-	50	pF
Common-mode rejection ratio	CMRR	$C_{LOAD}=50 pF$, $R_{LOAD}=5 k\Omega$	-	85	-	dB
Power supply rejection ratio	PSRR	$C_{LOAD}=50 pF$, $R_{LOAD}=5 k\Omega$	-	85	-	dB
Gain bandwidth product	GBW	$AV_{DD} \geq 2.4 V$	1800	3300	5800	kHz
Slew rate	SR	$AV_{DD} \geq 2.4 V$	-	1300	-	V/ms
Open loop gain	AO	$C_{LOAD}=50 pF$, $R_{LOAD}=5 k\Omega$	55	110	-	dB
High saturation voltage	$V_{OH(SAT)}$	$C_{LOAD}=50 pF$, $R_{LOAD}=5 k\Omega$	AV_{DD} -100	-	-	mV
Low saturation voltage	$V_{OL(SAT)}$	$C_{LOAD}=50 pF$, $R_{LOAD}=5 k\Omega$	-	-	100	mV
Phase margin	PM	$C_{LOAD}=50 pF$, $R_{LOAD}=5 k\Omega$	-	74	-	Degree
Wake up time from OFF state	T_{WAKEUP}	-	-	20	40	μs
Input bias current	I_{BIAS}	-	-	-	15	nA
Voltage noise density	V_{NOISE}	at 1 kHz	-	200	-	nV/ $\sqrt{Hz}$
		at 10 kHz	-	200	-	

NOTE:

1. AV_{DD} must always be supplied at the exact same voltage level as V_{DD} without exception. ($AV_{DD} = V_{DD}$)

Table 35. OPAMP Characteristics (Low-Power Mode)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Analog Power Supply	$AV_{DD}^{(1)}$	-	1.8	-	3.6	V
OPAMP current consumption	I_{OPAMP}	-	-	90	180	μA
Common mode input range	CMIR	-	0	-	AV_{DD}	V
Input offset voltage	V_{OFFSET}	-	-	-	0.5	mV
Input offset voltage drift	ΔV_{OFFSET}	-	-	± 1	-	$\mu V/^{\circ}C$
Output current load	I_{LOAD}	$AV_{DD} > 2 V$	-	-	100	μA
Resistive load	R_{LOAD}	$AV_{DD} < 2 V$	20	-	-	k Ω
Capacitive load	C_{LOAD}	-	-	-	50	pF
Common-mode rejection ratio	CMRR	$C_{LOAD}=50 pF$, $R_{LOAD}=5 k\Omega$	-	85	-	dB
Power supply rejection ratio	PSRR	$C_{LOAD}=50 pF$, $R_{LOAD}=5 k\Omega$	-	85	-	dB
Gain bandwidth product	GBW	$AV_{DD} \geq 2.4 V$	1100	2000	4000	kHz
Slew rate	SR	$AV_{DD} \geq 2.4 V$	-	800	-	V/ms
Open loop gain	AO	$C_{LOAD}=50 pF$, $R_{LOAD}=5 k\Omega$	100	120	130	dB
High saturation voltage	$V_{OH(SAT)}$	$C_{LOAD}=50 pF$, $R_{LOAD}=5 k\Omega$	AV_{DD} -100	-	-	mV
Low saturation voltage	$V_{OL(SAT)}$	$C_{LOAD}=50 pF$, $R_{LOAD}=5 k\Omega$	-	-	100	mV
Phase margin	PM	$C_{LOAD}=50 pF$, $R_{LOAD}=5 k\Omega$	-	80	-	Degree
Wake up time from OFF state	T_{WAKEUP}	-	-	50	100	μs
Input bias current	IBIAS	-	-	-	15	nA
Voltage noise density	VNOISE	at 1 kHz	-	200	-	nV/ $\sqrt{Hz}$
		at 10 kHz	-	200	-	

NOTE:

1. AV_{DD} must always be supplied at the exact same voltage level as V_{DD} without exception. ($AV_{DD} = V_{DD}$)

4.3.15 Communication Interfaces Characteristics

4.3.15.1 I2C Interface Characteristics

I2C interfaces comply with the I2C bus specifications and satisfy user timing requirements as shown below:

- Standard mode (Sm): up to 100 kbps bit rate
- Fast mode (Fm): up to 400 kbps bit rate

The I2C timing requirements are guaranteed by design when the peripherals around the I2C are correctly configured, and the I2C clock frequency is higher than the minimum value in Table 36.

Table 36. I2C Characteristics

(Temperature: -40°C to +85°C)

Parameter	Symbol	Standard		Fast		Units
		Min.	Max.	Min.	Max.	
Clock frequency	t _{SCL}	0	100	0	400	kHz
Clock high pulse width	t _{SCLH}	4.0	-	0.6	-	μs
clock low pulse width	t _{SCLL}	4.7	-	1.3	-	
Bus free time	t _{BF}	4.7	-	1.3	-	
Start condition setup time	t _{STSU}	4.7	-	0.6	-	
Start condition hold time	t _{STHD}	4.0	-	0.6	-	
Stop condition setup time	t _{SPSU}	4.0	-	0.6	-	
Stop condition hold time	t _{SPHD}	4.0	-	0.6	-	
Output valid from clock	t _{VD}	0	-	0	-	
Data input hold time	t _{DIH}	0	-	0	1.0	ns
Data input setup time	t _{DIS}	250	-	100	-	

4.3.15.2 SPI Interface Characteristics

Unless otherwise specified, parameters in Table 37 are derived from tests performed under the ambient temperature, f_{CLK} frequency, and supply voltage conditions summarized in Table 16.

- Capacitive load $C = 50 \text{ pF}$
- Measurement points are performed at the CMOS level: $0.5 \times V_{DD}$

For more information about I/O alternate function characteristics (SS, SCK, MOSI, and MISO for SPI), refer to section 4.3.11.

Table 37. SPI Characteristics

(Temperature: -40°C to $+85^{\circ}\text{C}$)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{SCK1}	SPI clock frequency with strength on	SPI0, SPI1 $V_{DD} \leq 1.8 \text{ V}$	-	-	10	MHz
f_{SCK2}		SPI0, SPI1 $V_{DD} \leq 3.3 \text{ V}$	-	-	10	MHz
f_{SCK4}	SPI clock frequency with strength off	SPI0, SPI1 $V_{DD} \leq 1.8 \text{ V}$	-	-	8	MHz
f_{SCK5}		SPI0, SPI1 $V_{DD} \leq 3.3 \text{ V}$	-	-	10	MHz
Duty	Duty cycle of SPI frequency (SCK)	Slave Mode	30	50	70	%
CCL	Capacitance load	-	-	-	50 ⁽¹⁾	pF

NOTE:

1. 3 MHz is expected when the capacitance load is 50 pF and V_{DD} is less than 1.8 V.

4.3.15.3 USB Interface Characteristics

Table 38. USB Characteristics

(Temperature: -40°C to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Operating supply voltage ⁽¹⁾	AV _{DD}	-	3	3.3	3.6	V
Differential input sensitivity	V _{DI}	-	0.2	-	-	
Differential common mode voltage	V _{CM}	-	0.8	-	2.5	
Low-level input voltage	V _{IL}	-	-	-	0.8	
High-level input voltage	V _{IH}	-	2.0	-	-	
Low-level output voltage	V _{OL}	RL = 1.5 kΩ to +3.6 V	-	-	0.3	
High-level output voltage	V _{OH}	RL = 15 kΩ to GND	2.8	-	3.6	
Power-down current	I _{PD}	@ SUSPEND, OEN='H'	-	-	10	μA
Transceiver capacitance	C _{IN}	Pin to GND	-	-	10	pF
Pull-down resistance on DP/DN	R _{PD}	Enable Internal Resistor	14.25	-	15.75	kΩ
Pull-up resistance on DP/DN	R _{PU}	Enable Internal Resistor	1.425	-	1.575	kΩ
Driver output impedance ⁽¹⁾	Z _{DRV}	Driving High or Low	28	-	44	Ω
Input impedance	Z _{INP}	Exclude pull-up/down	10	-	-	MΩ
Termination voltage for upstream port pull-up	V _{TERM}	-	3.0	-	3.6	V
Output Signal Crossover Voltage	V _{CRS}	-	1.3	-	2.0	V

NOTES:

1. No external termination series resistors are required on DP and DN pins, as the matching impedance is included in the embedded driver.
2. AV_{DD} must always be supplied at the exact same voltage level as V_{DD} without exception. (AV_{DD} = V_{DD})

4.3.16 LCD Driver Characteristics

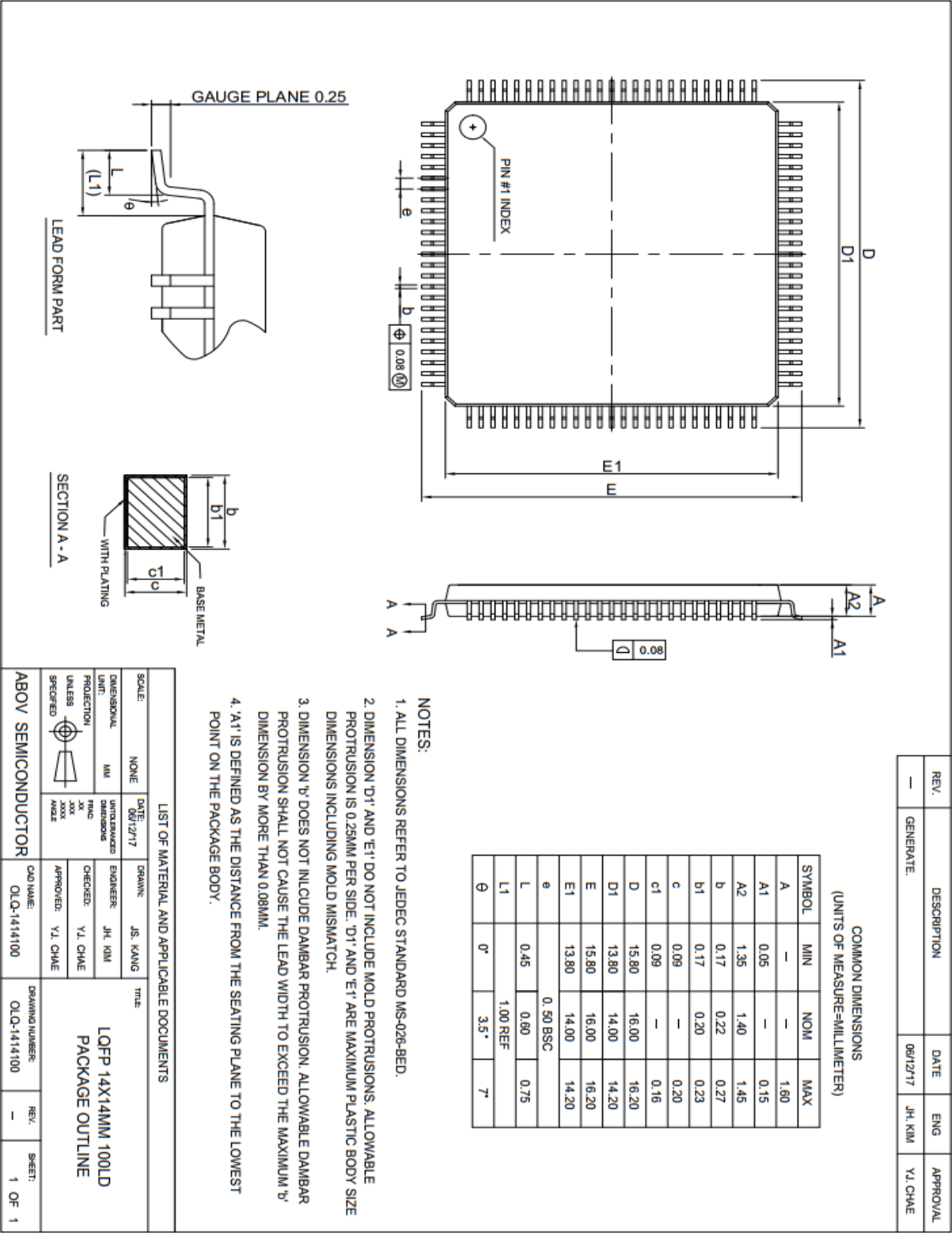
Table 39. LCD Driver Characteristics

Parameter	Symbol	Conditions	Min	Typ.	Max	Units
LCD voltage	VLC0	Voltage booster enabled, 1/4 bias	Typ. ×93%	3.07	Typ. ×107%	V
				3.17		
				3.26		
				3.36		
				3.46		
				3.55		
				3.65		
				3.74		
VLCD external capacitance	C _{VLC_EXT}	-	0.1	-	2	μF
LCD mid bias voltage (4-bias)	VLC0	Voltage booster enabled	-	4×V _{DD}	-	V
		Resistor mode	-	V _{DD}	-	
	VLC1	Voltage booster enabled	-	3×V _{DD}	-	
		Resistor mode	-	0.75×V _{DD}	-	
	VLC2	Voltage booster enabled	-	2×VLC3	-	
		Resistor mode	-	0.5×V _{DD}	-	
	VLC3	Voltage booster enabled	-	VLC3	-	
		Resistor mode	-	0.25×V _{DD}	-	
LCD bias dividing resistor	R _{LCD1}	-	-	10	-	kΩ
	R _{LCD2}	-	-	50	-	
	R _{LCD3}	-	-	100	-	
Operating current	I _{LCD}	Voltage booster enabled	-	3	6	μA
Power down current	I _{LCD_PD}	-	-	3	200	nA

5. Package Information

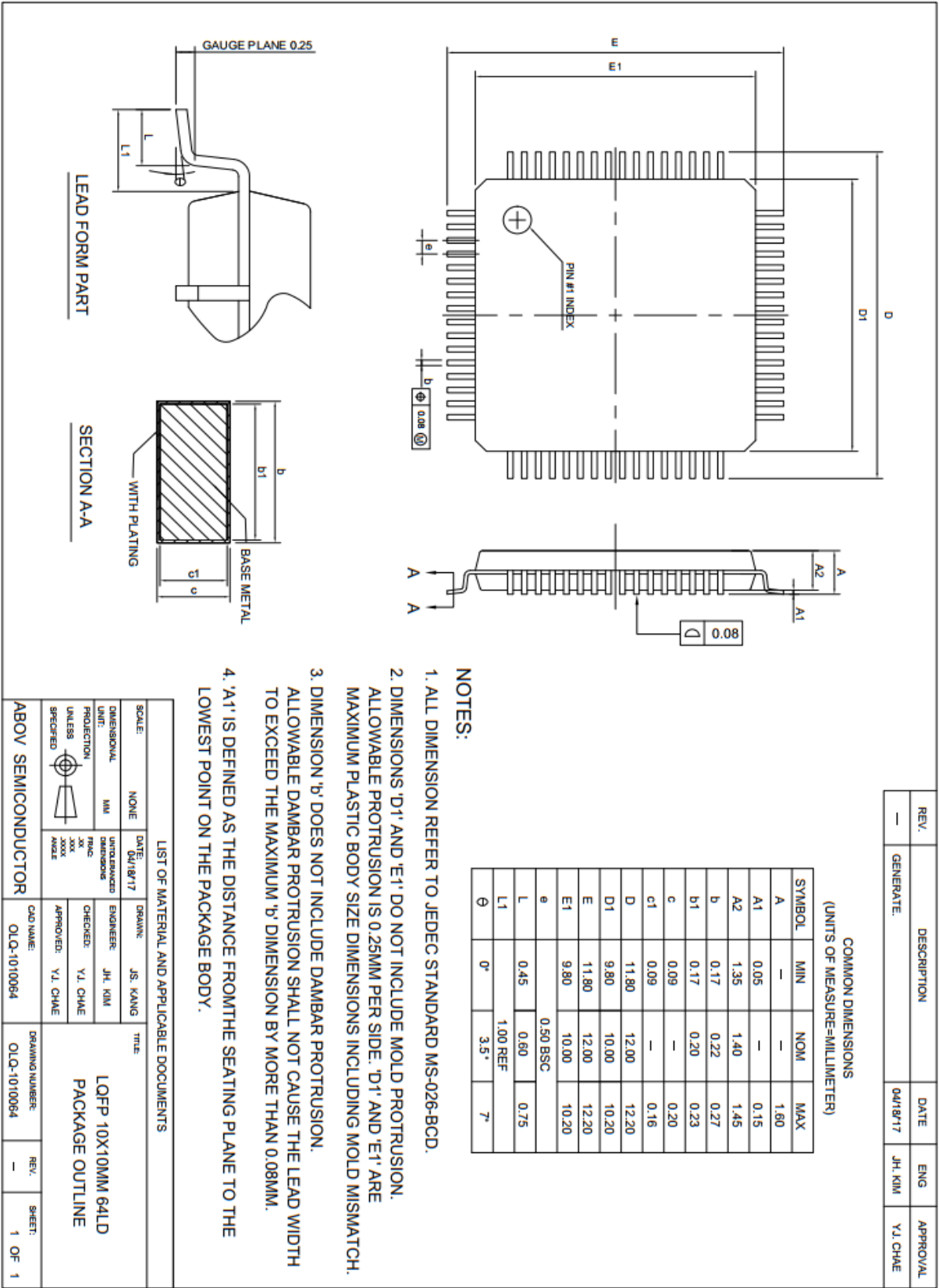
5.1 100-LQFP Package Information

Figure 21. Package Dimension (100-LQFP)



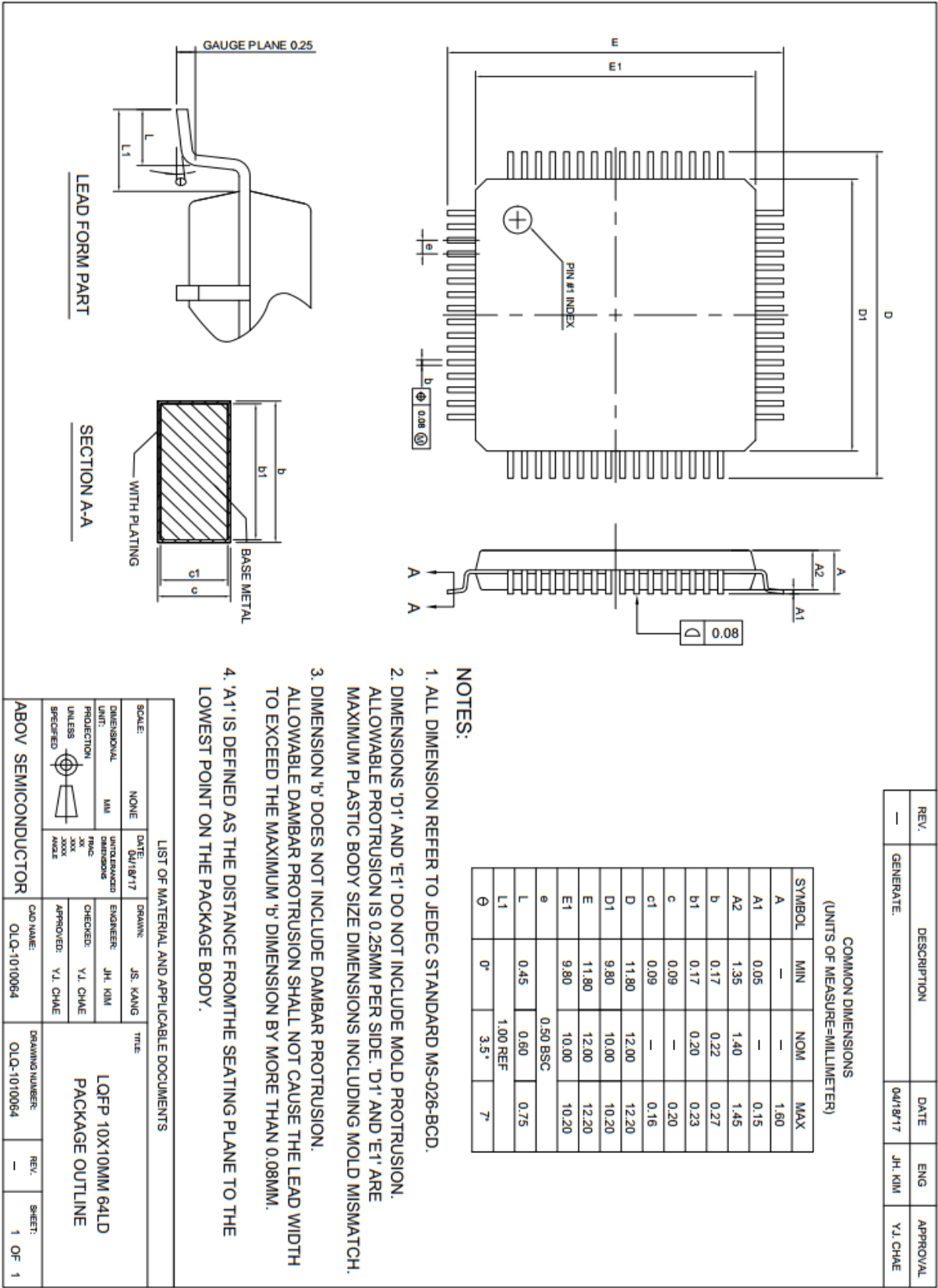
5.2 64-LQFP Package Information

Figure 22. Package Dimension (64-LQFP)



5.3 56-QFN Package Information

Figure 23. Package Dimension (56-QFN)



6. Ordering Information

Figure 24. A34L716 Device Numbering Nomenclature

A34L71 6 V L N (T)					
Device family name					
A34L71 = Arm Cortex-M4F based microcontroller					
Code memory size					
6 = 256 KB					
Pin count					
V = 100-pin					
R = 64-pin					
J = 56-pin					
Package type					
L = LQFP1 / 0.50 mm pin pitch					
M = LQFP2 / 0.62 mm pin pitch					
Y = QFN1					
Internal information					
N = Internal management code					
Packing					
None = Tray					
(T) = Tape & Reel					

NOTE:

- For a list of available options (memory, package, and so on) or further information on any aspect of this device, contact the nearest [ABOV sales office](#).

Revision History

Revision	Date	Notes
1.00	Sep. 20, 2024	Initial release.
1.01	Dec. 02, 2024	Updated the disclaimer.
1.02	Feb. 11, 2025	Updated the HSI spec and Table 24.
1.03	Apr. 17, 2025	Updated 64-LQFP pin map. Modified AVDD requirement description to clarify voltage constraint.

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