
**Cortex®-M0+ 32-Bit Microcontroller, 80 MHz, Up to 64 KB
Code Flash, 8 KB SRAM, 3-Phase PWM, 12-Bit ADC,
OPAMP for Motor Control Application**

DS Rev. 1.03

Features

Core

- Arm® 32-bit Cortex® -M0+ CPU
- Up to 80 MHz, 64 DMIPS
- Cache buffer (flash accelerator) support

Memories

- Up to 64 KB code flash (27 MHz flash access speed)
- Up to 8 KB SRAM

Reset and Power Management

- Power-on/power-down reset (POR/LVR/LVI)
- Low-power modes: SLEEP, DEEP-SLEEP

Clock Management

- High-Speed Internal (HSI) oscillator 32 MHz
 - $\pm 1\%$ @ -20°C to $+85^{\circ}\text{C}$
 - $\pm 1.5\%$ @ -40°C to 105°C
- Low-Speed Internal (LSI) oscillator 500 kHz
 - $\pm 30\%$
- High-Speed External (HSE) main oscillator
 - 4 MHz to 16 MHz
- Low-Speed External (LSE) sub-oscillator
 - 32.768 kHz
- Phase-Locked Loop (PLL) frequency generator
 - Up to 80 MHz

General-Purpose Input/Output

- Up to 44 I/O pins with interrupt capability
- All mappable on external interrupt vectors
- Multi-function pins capable of selection for up to 6 different functions, including GPIO

DMA Controller

- Four channels
- 8-/16-/32-bit data transfers
- Compatible with 8 different types of peripherals

ADC

- One independent ADC block
- 12 analog input channels
- Adjustable sample time and hold time
- Multiple operating modes:
 - Single conversion
 - Sequence conversion
 - Burst conversion
 - Multiple conversion
 - Inject conversion

Comparator

- One Comparator

Op-Amp

- Three operational amplifiers
- Compatible with ADC for joint operation

Internal Low-Dropout Regulator

16-Bit Timer

- Four channels
 - 4 input capture channels
 - 4 output channels
- Timer operating modes:
 - Periodic timer mode
 - One-shot mode
 - PWM mode
 - Capture mode
- 10-bit prescaler

WDT

- 32-bit down-count timer
- Reset and periodic interrupts
- Eight different prescalers

FRT

- 32-bit free-run timer

MPWM

- One MPWM generator
- Generating different waveforms through six channels with high- and low-signals of U, V, and W phases
- 16-bit up-/down-counters
- Six ADC trigger sources

Serial Interfaces

- UART
 - Two 16450 asynchronous serial communication ports
- SPI
 - One synchronous serial communication port
- I2C
 - One communication port

CRC Calculation Unit

- CRC operating modes:
 - CRC32 (0x04C1_1DB7)
 - CRC16-IBM (0x8005)
 - CRC16-CCITT (0x1021)
 - CRC8-CCITT (0x07)
- Support for byte reversal of input/output data
- Compatible with DMA

Development support

- Serial Wire Debug (SWD) interface

Package

- LQFP-48-7x7 (0.5 mm pitch)
- LQFP-32-7x7 (0.8 mm pitch)
- TSSOP-28-9.7x4.4 (0.65 mm pitch)

Operating Voltage

- 2.7 V to 5.5 V

Operating Temperature

- Commercial grade (-40°C to + 105°C)

Applications

- Refrigerator, washing machine, dryer, dishwasher, water purifier, blender
- Pump, Fan

Product Selection Table

Table 1. Device Summary

Part Number	Flash	SRAM	SPI	UART	I2C	MPWM	CMP	ADC	Op-Amp	TIMER	I/O Port	Package
A31M223CL2N	64 KB	8 KB	1	2	1	1	1	12	3	4	44	48-LQFP
A31M223KN2N*	64 KB	8 KB	1	2	1	1	1	10	2	4	30	32-LQFP
A31M223GR2N	64 KB	8 KB	1	2	1	1	1	10	2	4	26	28-TSSOP

* For available options or further information on the device with “*” marks, please contact the [ABOV sales office](#).

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1. Descriptions

1.1 General Information

The A31M22x series is a 32-bit microcontroller based on the high-performance Arm Cortex-M0+ core, with up to 64 KB of flash memory and 8 KB of SRAM. It is well-suited for a wide range of home appliances, such as refrigerators, washing machines, dryers, dishwashers, water purifiers, and blenders. It is also suitable for controlling pumps and fans, where both low-power consumption and high-performance are critical.

1.2 Product Category Definition

Table 2 provides an overview of the memory capacity for available devices in the A31M22x series.

This document provides an overview of the features supported by each device, including high-level information and brief explanations for each feature. Refer to Table 3 for the list of features supported by each product category.

Table 2. A31M22x Series Memory Capacity

Memory capacity		Category
Flash	RAM	
64 KB	8 KB	A31M223

1.3 Device Overview

Table 3 summarizes and lists the features specific to the device in the A31M22x series while considering the largest package.

Table 3. A31M22x Series Features

Peripheral		Description
Core	CPU	• Max. operating frequency: 80 MHz • 32-bit ARM Cortex-M0+ CPU • Register settings in CPU: - General purpose register: 32-bit Thumb-2 command - Main Stack Pointer (MSP) and Process Stack Pointer (PSP): R13 - Link Register (LR): R14 - Program Counter (PC): R15 • Data alignment in little endian • Von Neumann Architecture • AHB / APB
	Interrupt	• Nested-Vector Interrupt Controller (NVIC) • Max. 32 peripheral interrupts available • 2-bit width of group priority: 4 levels of priority
Memory	Code Flash	• Capacity: 64 KB • Large volume of embedded code flash • Max. 27 MHz Flash access speed • Erase unit: Page (512 bytes), sector (2 KB) or bulk (64 KB, chip) • Program unit: Word (4 bytes) • Read protection • Self-programming • CRC code generation and verification for the flash memory • Endurance: 10,000 cycles • Lifetime: 10 years (20 years for 100 cycles)
	Boot ROM	• Initiating the microcontroller's boot mode by receiving an external input signal at the nBOOT pin • UART boot mode • In-system programming - A user can store information in the internal Flash memory by using an application board to write data to the memory.

Table 3. A31M22x Series Features (continued)

Peripheral		Description
Memory	SRAM	- Capacity: 8 KB - Capable of functioning as a program's working area - High-speed execution for time-critical codes - Capability to remap into an interrupt vector area
System Control Unit (SCU)	Operating frequency	Up to 80 MHz
	Clock	- High-Speed Internal (HSI) oscillator 32 MHz ($\pm 1.0\%$ @ -20°C to $+85^{\circ}\text{C}$) 32 MHz ($\pm 1.5\%$ @ -40°C to $+105^{\circ}\text{C}$) - Low-Speed Internal (LSI) oscillator 500 kHz ($\pm 30\%$ @ -40°C to $+105^{\circ}\text{C}$) - High-Speed External (HSE) main oscillator: 4 MHz to 16 MHz - Low-Speed External (LSE) sub-oscillator: 32.768 kHz - Phase-Locked Loop (PLL) frequency generator: Capable of generating a high-speed clock (up to 80 MHz)
	Clock monitoring	- System Fail-Safe function by clock monitoring - High-Speed External (HSE) main oscillator - Low-Speed External (LSE) sub oscillator - Main system clock (MCLK)
	Operation mode	- RUN mode - SLEEP mode - DEEP-SLEEP (STOP) mode
	Reset	- nRESET Pin reset (PC10) - Core reset - Software reset - POR (Power-On Reset) - LVR (Low-Voltage Reset) - WDTR (Watch Dog Timer Reset) - Reset due to clock oscillating error
	VDC	Low-Dropout (LDO) regulator built in for low-voltage operation
	POR	POR generator: Capable of generating a reset signal by detecting an internal 1.4 V

Table 3. A31M22x Series Features (continued)

Peripheral		Description
System Control Unit (SCU)	LVDI	• 7 low-voltage detection levels • Supports interrupts • Supports wake-up from SLEEP mode
	Wake-up	• Wake-up by a General-Purpose Input / Output (GPIO) pin • Wake-up by a Free-Run Timer (FRT) • Wake-up by a Watchdog Timer (WDT) • Wake-up by a Low-Voltage Indicator (LVI)
General Purpose I/O (GPIO)		• Input / Output (I/O) port for general purpose • LQFP-48 - I/O pins: 44 • LQPF-32 - I/O pins: 30 • Selectable input and output configuration for each pin: - Push-pull output - Open drain output - Input • Pin configurations through multiplexer settings • Configurable as an external interrupt source with the following options: - Rising-edge (high-level) - Falling-edge (low-level) - Edge-triggered (both rising-edge and falling-edge) • Configurable pull-up/down resistors and debouncing • Adjustable drive strength • Configurable independently to be set or reset through its corresponding bit • Wake-up events triggered by external asynchronous inputs
Direct Memory Access (DMA) Controller		• 4-channel Direct Memory Access (DMA) supporting peripherals • 8-/16-/32-bit data transfers • Compatible with eight different types of peripherals • SPI, UART0, UART1, CRC, ADC

Table 3. A31M22x Series Features (continued)

Peripheral		Description
Timer	16-bit timer	• General-purpose 16-bit up-count timer • 4 channels - 4 (TnIO) input capture channels - 4 (TnIO) output channels • Timer operating modes - Periodic timer mode - One-shot mode - PWM mode - Capture mode • Interrupt events - Timer / counter match interrupt - Timer overflow interrupt • Free selectable clock sources: - PCLK configurable through the peripheral clock enable register1 (SCU_PCER1) - LSI, LSE, MCLK, HSI, HSE or PLL configurable through the miscellaneous clock control register 3 (SCU_MCCR3) • Timer signals output through TnIO pins • 10-bit prescaler
	Watchdog timer (WDT)	• 32-bit down-count timer • Reset and periodic interrupts • Free selectable clock sources: - LSI, LSE, MCLK, HSI, HSE or PLL configurable through the miscellaneous clock control register 1 (SCU_MCCR1) • Selectable eight different prescalers
	Free-run timer (FRT)	• 32-bit Free-run Timer - Timer for system time measurement - 32-bit up-count timer • Interrupt event - Period interrupt - Overflow interrupt

Table 3. A31M22x Series Features (continued)

Peripheral		Description
Serial interface	UART	• Two 16450 asynchronous serial communication ports • Configurable standard asynchronous communication bits (start, stop, and parity) • Flexible communication available through programming - 5- to 8-bit data transfers - Even / Odd / Non-parity generation and checking - 1-bit, 1.5-bit, or 2-bit stop bit generation and checking • 8-bit fraction controller and 16-bit baud rate generator
	SPI	• One synchronous serial communication port channel • Master / slave operation • Loop-back mode • Programmable and flexible communication - 8-bit / 9-bit / 16-bit / 17-bit data transmission / reception - SPI clock speed - Both Least Significant Bit (LSB)-first and Most Significant Bit (MSB)-first modes available
	I2C	• Standard I2C communication protocol • One channel support • Master and slave modes • 7-bit addressing for slave mode • Configurable SCL signal's high / low periods and SDA signal hold time
Motor Pulse-Width Modulation (MPWM)		• One MPWM generator • Generating different waveforms through six channels (high and low signals of U, V, and W phases) • 16-bit up / down counters • Six ADC trigger sources • Interrupt events - Bottom interrupts - Top (period) interrupts • Interval interrupt mode • Falling / rising dead time applicable • Protection and over-voltage detection support

Table 3. A31M22x Series Features (continued)

Peripheral	Description
12-bit A/D Converter (ADC)	• One independent ADC block • 12 analog input channels • Multiple operating modes: - Single conversion - Sequence conversion - Burst conversion - Multiple conversion - Inject conversion • Up to eight sequential conversions • Software triggers • Three internal trigger sources (MPWM and timers) • Adjustable sample time and hold time
Operational Amplifier (Op-Amp)	• 3 Op-Amps each with 2 input sources • Compatible with ADC for joint operation
Comparator (CMP)	• 1 internal comparator with 2 input sources • Various input and reference sources available
Cyclic Redundancy Check (CRC)	• CRC operating modes: - CRC32 (0x04C1_1DB7) - CRC16_IBM (0x8005) - CRC16_CCITT (0x1021) - CRC8_CCITT (0x07) • Support for byte reversal of input/output data • Compatible with DMA
Operating voltage	• 2.7 V to 5.5 V
Operating temperature	• Commercial grade (-40°C to +105°C)
Package	• Two types of package options - 48-LQFP-0707 (0.5 mm pitch) - 32-LQFP-0707 (0.8 mm pitch)

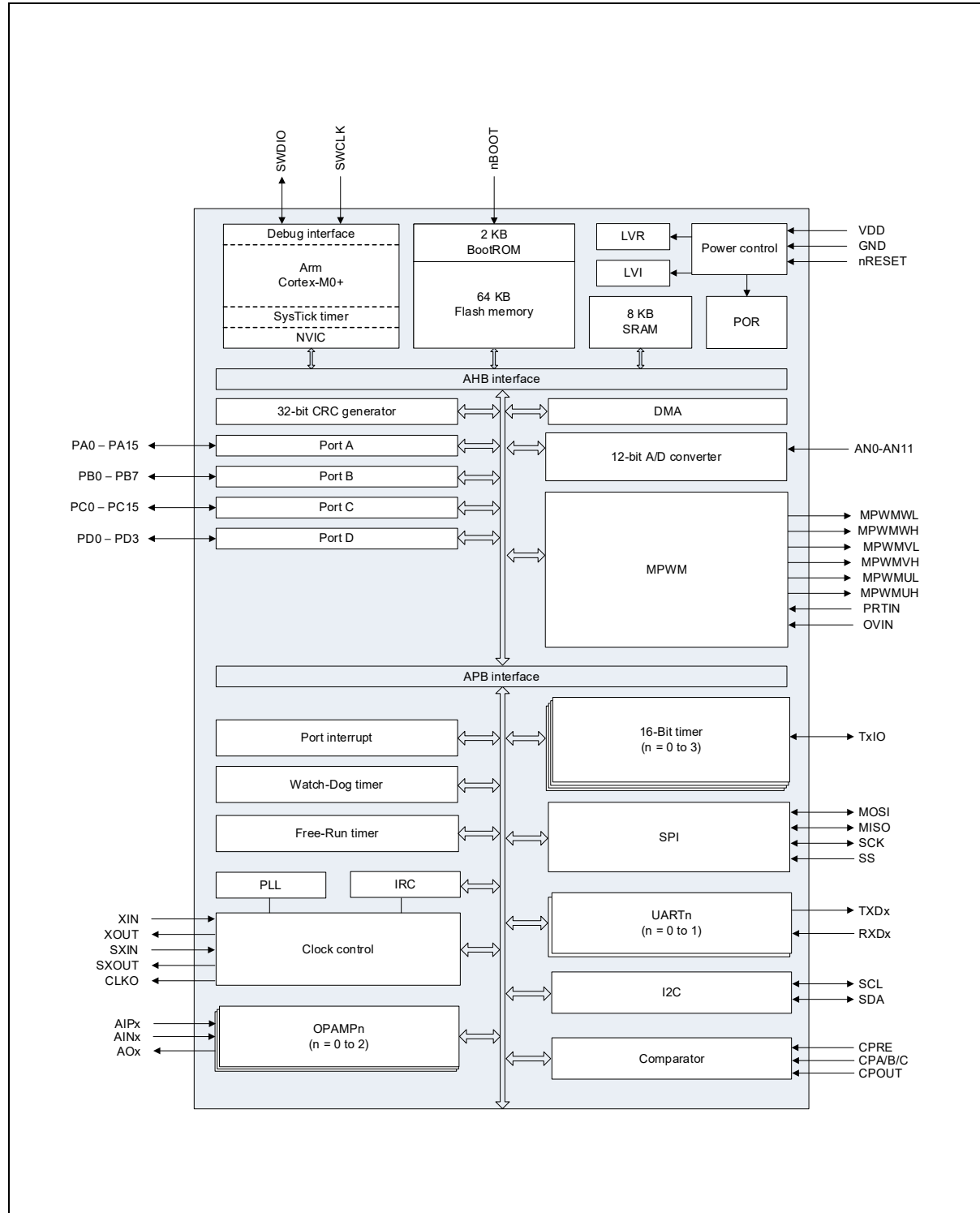
Table 4. Summary of A31M22x Peripherals

Peripheral		A31M223CL	A31M223KN	A31M223GR
Code flash memory		64 KB	64 KB	64 KB
SRAM		8 KB	8 KB	8 KB
Timers	MPWM	1 (16-bit)		
	General purpose	4 (16-bit)		
	SysTick timer	1		
	Watchdog timer	1		
	Free-run Timer	1		
Communication interfaces	SPI	1		1
	I2C	1		1
	UART	2		2
Direct Memory Access (DMA)		4		
GPIO		44	30	26
ADCs		2.0 Msps	2.0 Msps	2.0 Msps
Number of channels		12	10	10
Comparator		1	1	1
Op-Amp		3	2	2
Max. CPU frequency		80 MHz		
CRC		1		
Operating voltage		2.7 V to 5.5 V		
Operating temperature		Ambient operating temperature: 40°C to 105°C		
Packages		48-LQFP	32-LQFP	28-TSSOP

1.4 Block Diagram

Figure 1 shows a block diagram of the A31M22x series.

Figure 1. A31M22x Series Block Diagram



1.5 Functional Overview

The following sections provide overviews of the features of the A31M22x series microcontrollers.

1.5.1 Cortex-M0+ Core

The A31M22x series adopts the energy-efficient 32-bit microcontroller core, Cortex-M0+ of ARM as its CPU core. The Cortex-M0+ designed for low-power consumption uses the ARMv6-M Instruction set to improve performance and energy efficiency.

Refer to the technical reference manual “ARM DDI 0484C” for detailed information of Cortex-M0+.

1.5.2 Embedded SRAM

The A31M22x series has a block of 0-wait on-chip SRAM. The size of the SRAM is 8 KB and its base address is 0x2000_0000.

The SRAM memory area is commonly utilized for storing data and as a stack memory. Additionally, it can also be utilized for storing program code for faster execution or during flash erase/programming operations. This device does not support memory remap strategy. Therefore, it is necessary to perform a jump and return in order to execute the code stored in the SRAM memory area.

1.5.3 Boot Configuration

The A31M22x series offers one boot mode for programming the internal Flash memory. The boot mode can be entered by setting the nBOOT pin to ‘L’ during the system reset process (the normal state is ‘H’).

The boot mode supports the UART boot which uses the UART interface to transmit and receive boot data (TXD0/RXD0).

The pins for the boot mode are listed in Table 5.

Table 5. Boot Mode Pin List

Block	Pin Name	Pin Direction	Description
SYSTEM	nRESET / PC10	Input	Receive the reset signal.
	nBOOT / PC11	Input	Set the boot mode.
UART0	RXD0 / PC14	Input	Receive the UART boot data.
	TXD0 / PC15	Output	Transmit the UART boot data.

1.5.4 Power Supply

The device operates with a supply voltage of 2.7 V to 5.5 V (VDD). Additionally, the analog peripherals are powered through VDD, which is internally connected to AVDD within the microcontroller.

Table 6. Power Supply

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	VDD	2.7	5.5	V
	AVDD (Analog VDD)	2.7	5.5	V

During a power-up process, a reset plays an important role and affects the entire process of the system booting. The A31M22x series has two power-related reset options as described below:

POR_RST (Power-On Reset): Controls the voltage less than 1.4 V

LVD_RST (Low Voltage Detect Reset): Controls the voltage less than 2.12 V (default)

If the power level is higher than the POR and below the flash operating voltage (Min. 1.35 V), the Code Read operation may malfunction. To prevent this abnormal Code Read operation, the LVD_RST generates the SYSRESETn internal signal, and the microcontroller enters the reset mode to prevent the abnormal operation. The minimum level that can be set by the LVR is 1.6 V, which meets the flash minimum operating voltage.

1.5.5 Operation Mode

1.5.5.1 Transition of Operation Mode

INIT mode is an initial state of the chip when a reset is asserted. In RUN mode, the CPU operates at the maximum performance with the high-speed clock system.

SLEEP mode and DEEP-SLEEP mode can be used as low power consumption mode. In the low power consumption mode, power is effectively managed to reduce power consumption by halting the processor core and any unused peripherals.

1.5.5.2 RUN Mode

In RUN mode, the CPU and peripheral hardware operate with a high-speed clock. After a reset, the system will enter RUN mode if the INIT state is detected.

1.5.5.3 SLEEP Mode

Once the microcontroller enters SLEEP mode, the CPU becomes inactive. By setting the SCU_PER and SCU_PCER registers, users can determine which peripherals are to be inactive in SLEEP mode.

1.5.5.4 DEEP-SLEEP (STOP) Mode

When the core goes under stop state using WFI instruction, the microcontroller enters DEEP-SLEEP mode.

1.5.5.5 Reset Mode

The A31M22x series has two system reset options: a cold reset, which is effective during power up or down sequences, and a warm reset, which is triggered by multiple reset sources.

The reset features of A31M22x series are as follows:

- Power on reset (POR)
- Low Voltage Detect Reset (LVR)
- nRESET pin reset
- Watchdog Timer (WDT) reset
- Software reset
- Clock oscillating error reset
- CPU request reset

1.5.6 Clocks and Startup

The A31M22x series has two main operating clocks: HCLK, which generates clock signals for the CPU and AHB system, and PCLK, which generates clock signals for peripheral systems.

1.5.6.1 HCLK Clock

The Cortex-M0+ core requires two clocks: HCLK and FCLK. While the HCLK supplies the clock for both the CPU and AHB, the FCLK remains enabled unless the system enters DEEP-SLEEP mode. Conversely, during SLEEP mode, the HCLK can be disabled while the FCLK continues to function.

The buses and memories are clocked by the HCLK. As the bus clock frequency is limited to a maximum of 80 MHz, the HCLK frequency must not exceed 80 MHz.

1.5.6.2 PCLK Clock

The PCLK can be used as a clock source for any peripherals. The SCU_PCER registers determine whether the PCLK is enabled or disabled for each peripheral. If a peripheral block's PCLK input is not enabled, its registers cannot be read. Additionally, it is important to note that the PCLK stops operating in DEEP-SLEEP mode.

1.5.6.3 Clock Configuration Procedure

After power on, HSI (4 MHz, 32 MHz / 8) operates as a system clock by default. The HSI is enabled during the power up sequence, and the HSE is configured by user controls with the HSI system clock.

Before enabling the HSE block, the pin mux for XIN and XOUT must be configured. During this process, it is important to avoid affecting other bits of the PC_MR and PC_CR registers. After enabling the HSE block, it is necessary to wait for the crystal oscillation to be stabilized before proceeding.

The sub-oscillator, Low Speed External (LSE, operating at 32.768 kHz) clock, can be enabled using the SCU_CSCR register (Clock Source Control Register). Similar to the HSE, the LSE must be enabled after configuring the pin mux for SXIN and SXOUT and allowing sufficient time for the oscillation to be stabilized.

1.5.7 Interrupts and Events

1.5.7.1 Nested Vectored-Interrupt Controller (NVIC)

The A31M22x series includes up to 32 maskable interrupt channels that manage sixteen priority levels. The Nested Vector Interrupt Controller (NVIC) controls 16 interrupt lines of the Cortex-M0+.

The NVIC has the following advantages:

- Interrupt processing with reduced interrupt latency
- Direct transfer of Interrupt Vector Table (IVT) address to the core
- Fast interrupt processing capability
- Interrupts with higher priority are given precedence over those with lower priority, even if they occur after the lower-priority interrupts.
- Automatic saving of processor state
- Interrupt restoring without instructional overhead at the end of the interrupt

The NVIC hardware block provides flexible and efficient interrupt management with minimal interrupt latency.

1.5.7.2 Extended Interrupt (EXTI)

The Extended Interrupt feature enables the system to generate event requests or wake up from STOP mode. Each external line can be configured independently to detect trigger events such as rising or falling edges, or both edges, as well as level events such as Low or High.

1.5.8 General Purpose Input/Output (GPIO)

1.5.8.1 PCU Module

The A31M22x series has a Port Control Unit (PCU) module that controls the input and output (I/O) ports.

By setting the PCU registers, users can configure the functionality, input / output direction, pull-up / pull-down, and debouncing of the pins for their applications.

1.5.8.2 GPIO Module

Pins other than those specified as VDD, GND or certain purpose, can be used as General Purpose Input / Output (GPIO) pins.

The GPIO module controls the general I/O pins. Output pins can be configured to output high- or low-level signals by setting the corresponding bits of the GPIO control register. On the other hand, the input status of logic input pins can be monitored through the control registers.

1.5.9 Embedded Flash Memory

The flash memory controller serves as an interface between the core and the embedded flash memory and is responsible for managing the data stored on the flash memory.

The flash memory of A31M22x series has the following features:

- Code flash memory for 64 KB with write protection bits
- Erase units
 - Page (512 bytes)
 - Sector (2 KB)
 - Bulk (64 KB, chip)
- Program unit: Word (4 bytes)
- Zero wait (less than 27 MHz), 1- to 15-wait, and cache (flash acceleration) access
- Code flash read protection
- Code flash instruction cache

1.5.10 Direct Memory Access Controller (DMA)

The direct memory access (DMA) controller is used for high-speed data transfers between peripherals and memories. The DMA allows quick data transfers by copying or moving data between memory locations or between memory and peripherals, without involving the core.

The DMA has the following features:

- Four channels
- Only single-ended signaling
- 8-bit / 16-bit / 32-bit data transfers
- Multiple buffers of the same size
- DMA transfers are triggered by peripheral interrupts

1.5.11 Timers

1.5.11.1 16-Bit Timer

The A31M22x series has a TIMER module configured with four units. This 16-bit Timer supports four operating modes: Periodic Mode, PWM Mode, One-shot Mode, and Capture Mode.

Users can use a divided PCLK or an external clock as a clock source for the 16-bit Timer. An internal 10-bit prescaler allows to generate a variety of base clocks for the timer.

Interrupts can be triggered at regular intervals when the timer is used in Periodic Mode. Users can set the period and duty to form a PWM signal that is used in PWM Mode.

In One-shot Mode, the timer can generate one PWM waveform. The Capture Mode allows measuring the pulse intervals of an external input signal based on the predefined conditions. In addition, this timer can transmit signals to control other devices and is primarily used as a periodic tick timer or as a wake-up source.

1.5.11.2 Free-Run Timers (FRT)

The A31M22x series has one built-in 32-bit up count Free-run Timer (FRT). The FRT can operate with an overflow interrupt or a match interrupt based on its register settings and can remain active even in DEEP-SLEEP (STOP) mode.

1.5.11.3 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is used to detect errors in the microcontroller caused by external interference or unexpected logical conditions. These errors cause the application program to deviate from its normal sequence. If the microcontroller loses control, the WDT will reset the microcontroller, allowing it to return to normal operation.

The WDT of the A31M22x series is a 32-bit down counter. If the WDT is set as a reset source, the microcontroller restarts when the down counter reaches 0.

When it is not used to monitor the microcontroller, the WDT can be used as a cycle timer along with an interrupt.

1.5.11.4 SysTick Timer

Although the SysTick timer is primarily designed for real-time operating systems, it can also be utilized as a standard down-counter.

The SysTick timer has the following features:

- 24-bit down-counter
- Automatic refreshing
- Maskable system interrupt generation when counter reaches '0'
- Programmable clock source

1.5.12 Universal Asynchronous Receiver/Transmitter (UART)

The A31M22x series has a two-channel UART module. The built-in UART module allows users to specify settings for transmitting and receiving data and provides the ability to read the current status of the UART. By providing information about the current state of transmission and reception processes, including types and conditions, the UART module enables users to monitor potential errors such as parity, overrun, framing, or break interrupts during data reception.

The UART module includes a programmable baud-rate generator for each channel, which generates an internal clock for its corresponding UART unit. This is achieved by dividing a prescaled clock using a baud-rate divisor that ranges from 1 to 65535 and then dividing the result by 16.

Users can program interrupts that can control UART communication.

Furthermore, the built-in DMA allows the UART module to transfer data directly to or from memory without involving the CPU, reducing CPU usage and increasing the speed of data transfer.

1.5.13 Serial Peripheral Interface (SPI)

The A31M22x series has one built-in Serial Peripheral Interface (SPI) module. The SPI module is synchronized with a clock, and the specification of the transmission clock is adjustable.

The SPI module supports communication between one master and slaves. Slaves can be selected by the Slave Select (SS) signal.

The SPI module performs four-wire synchronous transfers via four signal terminals (SS, SCK, MOSI, and MISO). Its separate Transmit and Receive Buffers enable full-duplex communication, which is capable of reading and writing data simultaneously.

Specifically, the SPI module of the A31M22x series can enhance the Port Drive Strength, allowing the microcontroller to achieve SPI rates of up to 12 MHz.

1.5.14 Inter-Integrated Circuit (I2C) Interface

The I2C (Inter-integrated Circuit) interface built in A31M22x series is compliant with the standard I2C communication protocol. It is used for serial communication between internal and external devices via the I2C protocol.

Equipped with one unit, it supports both master and slave modes and is capable of transmitting and receiving data in bytes by using interrupts or polling.

The I2C interface of the A31M22x series operates in Standard mode (100 kHz) or Fast mode (400 kHz). In addition, it also supports General call.

The I2C interface facilitates communication with multiple peripherals that share the same bus type. To utilize I2C, it is recommended to configure the SCL and SDA pins as open-drain and attach external pull-up resistors to ensure that their output signals are maintained in the 'HIGH' state.

Table 7. Features of I2C

I2C Features	I2C
7-bit addressing mode	O
Standard mode (up to 100 kbit/s)	O
Fast mode (up to 400 kbit/s)	O
General call	O

1.5.15 Motor Pulse Width Modulation (MPWM)

The A31M22x series features two Motor Pulse Width Modulation (MPWM) modules. The MPWM in the A31M22x series operates total of two PWM modes as shown below to support various applications:

- Motor PWM mode for motor control
- Normal PWM mode for a variety of PWM applications

The MPWM module of the A31M22x series provides a range of PWM control functionalities in both Motor and Normal PWM modes, including up to 6 channels' outputs, dead-time management, up to 6 ADC triggers, a variety of interrupt event generations under different conditions, and protection events.

1.5.16 Analog-to-Digital Converter (ADC)

The A31M22x series features a 12-bit resolution Analog-to-Digital Converter (ADC) module. It consists of three independently controllable units and supports up to 12 different analog inputs.

The ADC module supports AD conversion of multiple channels in different modes, including single mode, sequential mode, multiple mode, inject mode and burst mode. It supports the sampling of voltage inputs from multiple channels at critical times, which is essential for various applications. This can be accomplished using the triggering functionality in conjunction with TIMER and MPWM.

Once the AD conversion is complete, the result is stored in 16-bit data registers with left alignment.

The ADC is mapped to the APB and capable of high-speed operation based on the internal clock source. In addition, it uses built-in DMA to reduce microcontroller core load while enabling fast data sampling.

The analog input monitoring and comparison capabilities of the ADC allow the applications to determine whether the input voltage is above or below the predefined level. In addition, it has the ability to use the Op-Amp's output signal as an input signal, which can be utilized for motor solutions.

1.5.17 Op-Amps

The A31M22x series features three Op-Amps each with two input and one output.

The Op-Amp of A31M22x series has the following features:

- Three Op-Amp units
- The Op-Amp 0/1/2 can utilize the external analog input signals PA4, PA7, and PC7 as its (+) input, respectively.
- The Op-Amp 0/1/2 can utilize the external analog input signals PA5, PA8, and PC8 as its (-) input, respectively.
- The output of each Op-Amp 0/1/2 is connected to the corresponding analog input of the ADC module, namely adc_ch17, adc_ch18, and adc_ch19, respectively.

1.5.18 Comparator (CMP)

The A31M22x series has one comparator. The comparator can output the result of comparing two analog voltages via an I/O pin or by generating interrupts.

The comparator of A31M22x series has the following features:

- One built-in comparator
- Support two input sources (CPn [n: A, B, C] and CPRE/Internal VDD 1.0 V)
- Control of the interrupt signal edges: either the falling or rising edge
- Noise filtering capability
- Four available hysteresis voltages (10 mV, 20 mV, 30 mV, and 40 mV)

1.5.19 Cyclic Redundancy Check Calculation Module (CRC)

The Cyclic Redundancy Check (CRC) module is used to calculate 32-bit, 16-bit IBM, 16-bit CCITT and 8-bit CCITT CRC codes from 8-bit or 32-bit data size. The user application can utilize CRC-based technologies to ensure the integrity of data transfers, storage, and flash memories in compliance with functional safety standards. With this module, you can verify the integrity of data transfers and flash memory.

Specifically, the CRC module of the A31M22x series supports DMA.

1.6 Development Tools

In this chapter, various development tools for the A31M22x series are introduced. ABOV provides software tools, debuggers, and programmers to assist users in achieving the desired results for their target applications. ABOV supports the complete development ecosystem for our customers.

1.6.1 Compiler

ABOV semiconductor does not provide any compiler for the A31M22x series. However, since the A31M22x series has the Arm's high-speed 32-bit Cortex-M0+ Core for its CPU, you can use all kinds of third party's standard compilers such as Keil C Compiler. These compilers' output debug information can be integrated with our A-Link and A-Link Pro. Please visit www.abovsemi.com for more information about the A-Link and A-Link Pro.

1.6.2 Debugger

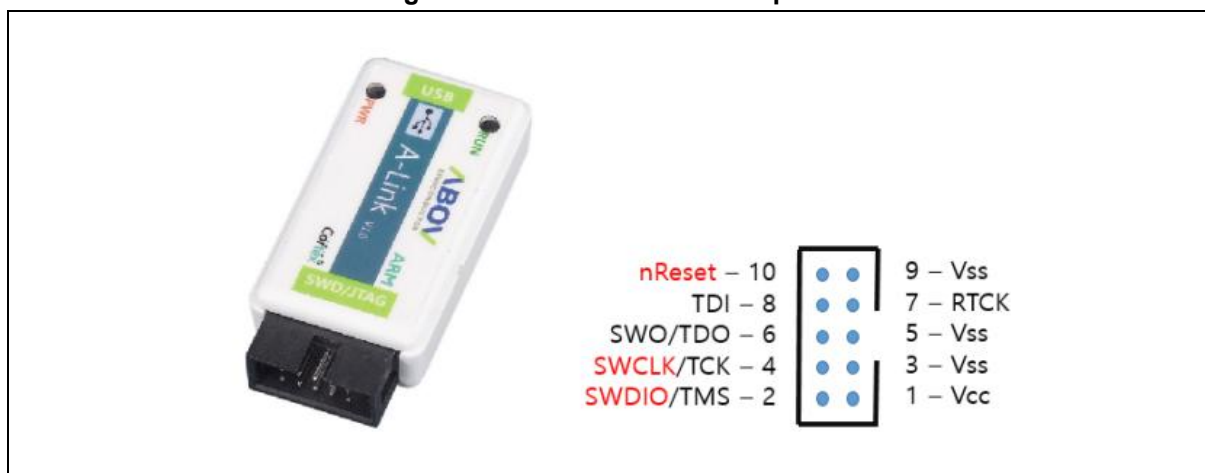
The A-Link and A-Link Pro can be used to emulate the A31M22x using the SWD interface. The A-Link and A-Link Pro use a two-wire interface to connect the PC to the microcontroller, which is connected to the user's system. The A-Link and A-Link Pro can read or change the value of microcontroller's internal memory and I/O peripherals. In addition, the A-Link and A-Link Pro control microcontroller's internal debugging logic. This means A-Link and A-Link Pro control emulation, step run, monitoring and many more functions regarding debugging.

The A-Link and A-Link Pro are compatible with Microsoft operating systems as shown below:

- Windows NT / 2000 / XP / Vista / 7 / 8 / 8.1 / 10 / 11 (32-bit, 64-bit)

Programming information using the A-Link and A-Link Pro is provided in Figure 2. For more detailed information about the A-Link and A-Link Pro, please visit www.abovsemi.com and download the debugger software and related documents.

Figure 2. A-Link and Pin Description



1.6.3 Programmer

1.6.3.1 E-PGM+ and E-PGM Serial

E-PGM+ and E-PGM Serial are standalone programmers which allow users to program directly on the device.

- Supports for all ABOV microcontroller devices
- A dedicated tool for mass production
- 40-pin Textool DIP socket for single-chip programming (E-PGM+ only)
- 10-pin connector for ISP mode
- USB host interface
- HEX downloads and controls

1.6.3.2 Gang Programmer

E-Gang4 and E-Gang6 are capable of programming multiple devices simultaneously and can operate in both PC-controlled and standalone modes without requiring a host computer connection. These programmers feature a USB interface for easy connection to a handler.

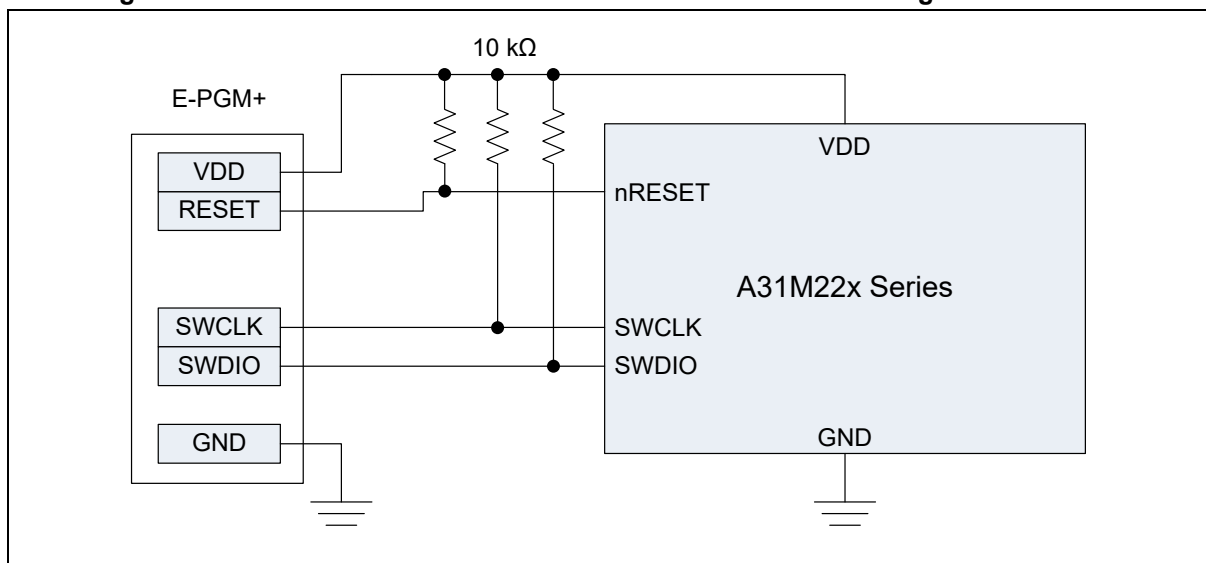
NOTE:

1. Please refer to [ABOV homepage](#) "Tools & Support > Programmer".

1.6.3.3 SWD Mode and E-PGM+ Connection

The connection between the A31M22x series and E-PGM+ using the SWD interface is illustrated in Figure 3.

Figure 3. Connection Between A31M22x Series and E-PGM+ Using SWD Interface



2. Pinouts and Pin Descriptions

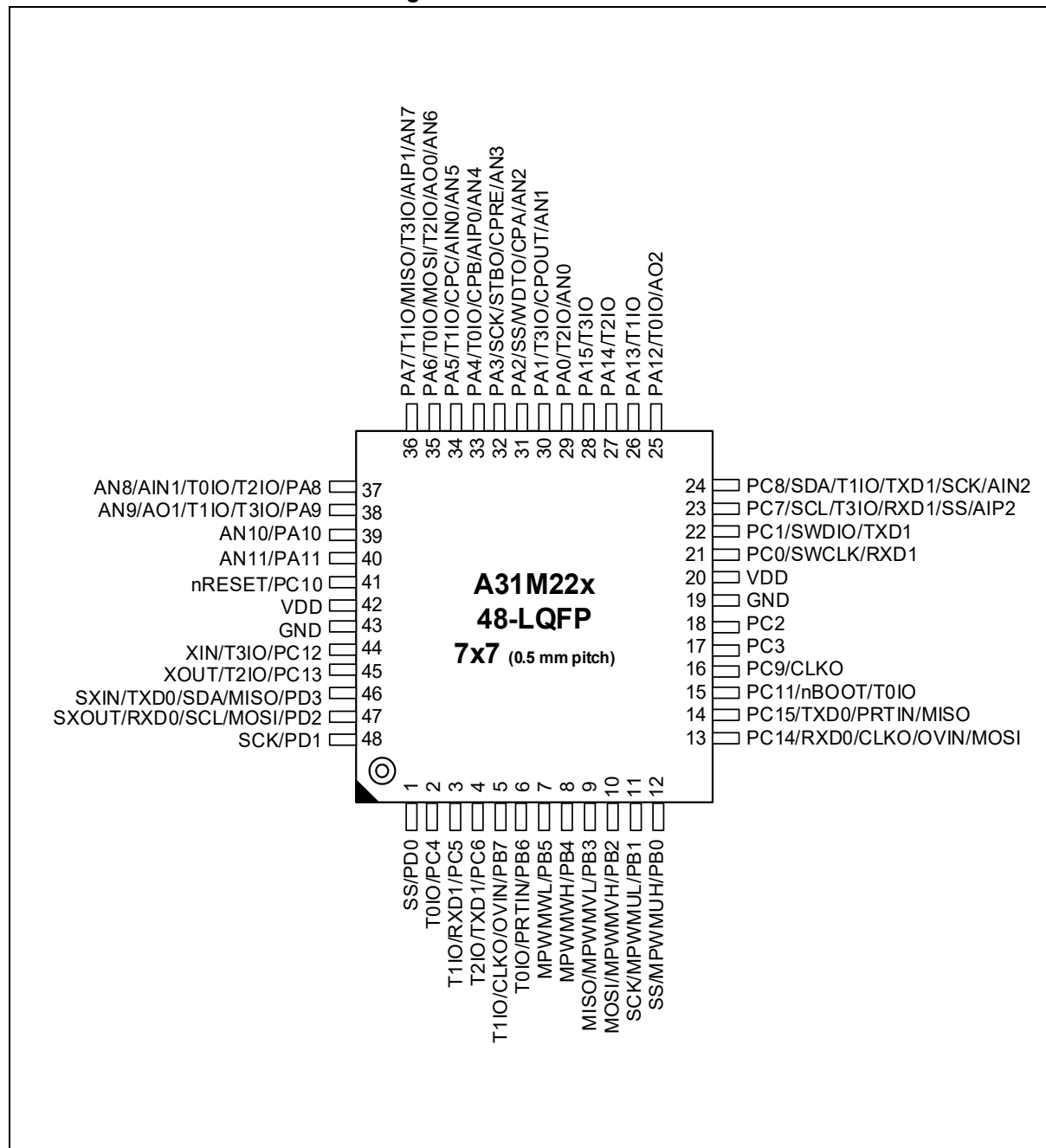
In this chapter, pinouts and pin descriptions of the A31M22x series are introduced.

2.1 Pinouts

Figure 4, Figure 5 and Figure 6 show the top views of the packages.

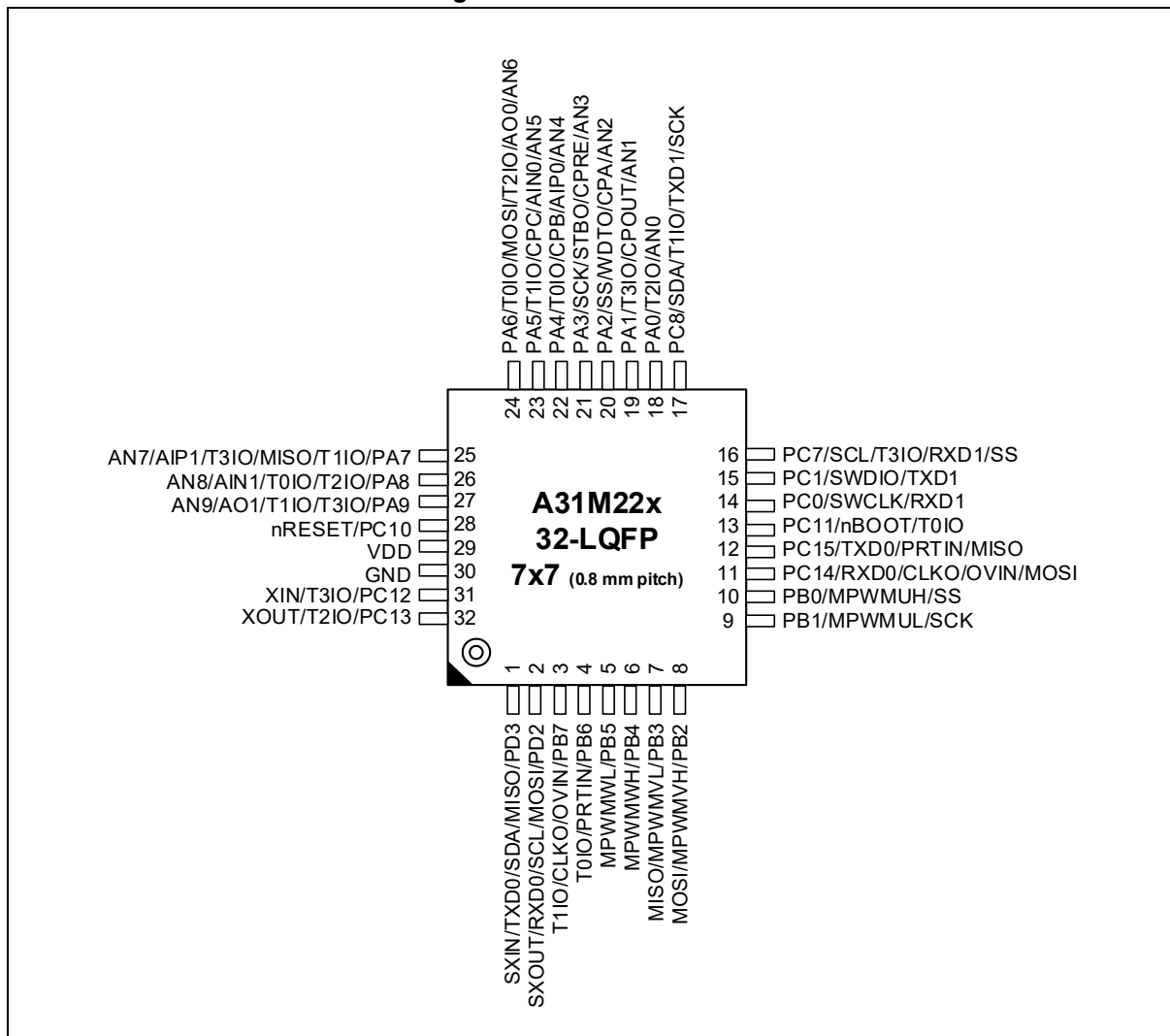
2.1.1 A31M223CL2N (48-LQFP)

Figure 4. 48-LQFP Pinouts



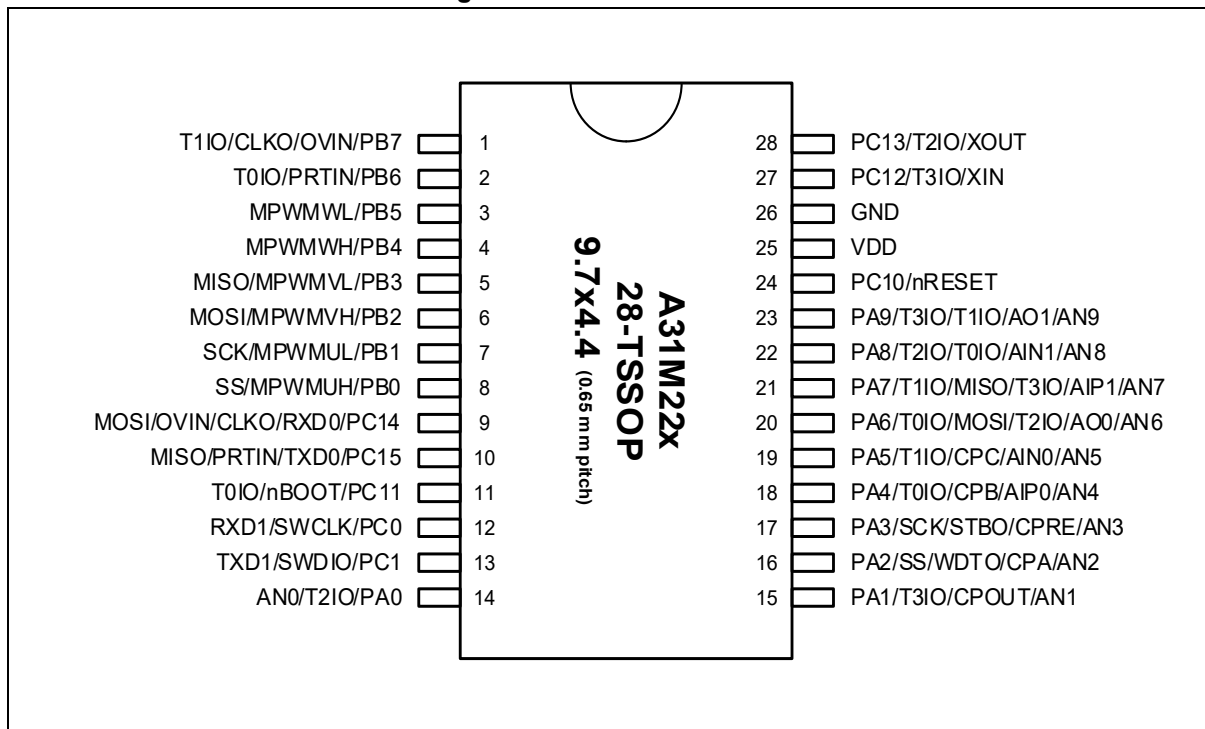
2.1.2 A31M222KN2N (32-LQFP)

Figure 5. 32-LQFP Pinouts



2.1.3 A31M223GR2N (28-TSSOP)

Figure 6. 28-TSSOP Pinouts



2.2 Pin Description

Table 8. Legend and Abbreviations Used in Pin Description

Name	Abbreviation	Definition
Pin name	- The pin name remains constant. - Users can assign a function to the pin using the alternate function.	
Pin type	I	Input
	O	Output
	I/O	Input/Output
	U	Pull-up
	D	Pull-down
	S	Schmitt-Trigger input
	C	CMOS input
	A	Analog
	P	Power

NOTES:

- After a reset, all the pins are configured to function defined by their initial values. The initial value of the pin depends on the package type. This configuration is in compliance with the 48-pin standard.
- Unused pins are set to output from Firmware (low output is recommended).
- PC11 (nBOOT), PC10 (nRESET), PC1 (SWDIO) and PC0 (SWCLK) are the default pull-up pins.
- Do not configure unused pins as floating inputs.
- After a reset, the internal pull-up for the boot pin is enabled.
- After a reset, the internal pull-up for the Serial Wire Clock (SWCLK) and the Serial Wire Data I/O (SWDIO) is enabled.
- The SWCLK and SWDIO pins should not be switched to other functions while they are being used.
- PC7 and PC8 pins are open-drain ports.
- When the PC12 (XIN), PC13 (XOUT), PD2(SXOUT), and PD3(SXIN) pins are configured for a function other than a clock, and if the clock is enabled by software, the other functions may not operate normally.

Pin configuration information in Table 9 contains two pairs of power/ground and other dedicated pins. These multi-function pins have up to six selections of functions including GPIO. Configuration including pin ordering can be changed without notice.

Table 9. Pin Description

Pin Number			Pin Name	Type	Function	Remark
48-LQFP	32-LQFP	28-TSSOP				
1	-	-	PD0	IOUDS	Port D bit 0 input / output	
			SS	IO	SPI channel slave select input / output	
2	-	-	PC4	IOUDS	Port C bit 4 input / output	
			T0IO	IO	Timer 0 input / output	
3	-	-	PC5	IOUDS	Port C bit 5 input / output	
			RXD1	I	UART RXD1 input	
			T1IO	IO	Timer 1 input / output	
4	-	-	PC6	IOUDS	Port C bit 6 input / output	
			TXD1	O	UART TXD1 output	
			T2IO	IO	Timer 2 input / output	
5	3	1	PB7	IOUDS	Port B bit 3 input / output	
			OVIN	I	PWM over-voltage input signal	
			CLKO	O	System clock output	
			T1IO	IO	Timer 1 input / output	
6	4	2	PB6	IOUDS	Port B bit 6 input / output	
			PRTIN	I	PWM protect input signal	
			T0IO	IO	Timer 0 input / output	
7	5	3	PB5	IOUDS	Port B bit 5 input / output	
			MPWMWL	O	MPWM WL output	
8	6	4	PB4	IOUDS	Port B bit 4 input / output	
			MPWMWH	O	MPWM WH output	
9	7	5	PB3	IOUDS	Port B bit 3 input / output	
			MPWMVL	O	MPWM VL output	
			MISO	IO	SPI channel master-in / slave-out	
10	8	6	PB2	IOUDS	Port B bit 2 input / output	
			MPWMVH	O	MPWM VH output	
			MOSI	IO	SPI channel master-out / slave-in	
11	9	7	PB1	IOUDS	Port B bit 1 input / output	
			MPWMUL	O	MPWM UL output	
			SCK	IO	SPI channel clock input / output	
12	10	8	PB0	IOUDS	Port B bit 0 input/output	
			MPWMUH	O	MPWM UH output	
			SS	IO	SPI channel slave select input / output	

Table 9. Pin Description (continued)

Pin Number			Pin Name	Type	Function	Remark
48-LQFP	32-LQFP	28-TSSOP				
13	11	9	PC14	IOUDS	Port C bit 14 input / output	
			RXD0	I	UART0 RXD0 input	
			CLKO	O	System clock output	
			OVIN	I	PWM over-voltage input signal	
			MOSI	IO	SPI channel master-out / slave-in	
14	12	10	PC15	IOUDS	Port C bit 15 input / output	
			TXD0	O	UART TXD0 output	
			PRTIN	I	PWM protect input signal	
			MISO	IO	SPI channel master-in / slave-out	
15	13	11	PC11	IOUDS	Port C bit 11 input / output	
			nBOOT ⁽¹⁾⁽³⁾⁽⁵⁾	IU	Boot mode selection input	Internal pull-up enable
			T0IO	IO	Timer 0 input / output	
16	-	-	PC9	IOUDS	Port C bit 9 input / output	
			CLKO	O	System clock output	
17	-	-	PC3	IOUDS	Port C bit 3 input / output	
18	-	-	PC	IOUDS	Port C bit 2 input / output	
19	-	-	GND	P	GND	
20	-	-	VDD	P	VDD	
21	14	12	PC0	IOUDS	Port C bit 0 input / output	
			SWCLK ⁽¹⁾⁽³⁾⁽⁵⁾⁽⁷⁾	I	SWD clock input	Internal pull-up enable
			RXD1	I	UART RXD1 input	
22	15	13	PC1	IOUDS	Port C bit 1 input / output	
			SWDIO ⁽¹⁾⁽³⁾⁽⁵⁾⁽⁷⁾	IO	SWD data input / output	Internal pull-up enable
			TXD1	O	UART TXD1 output	
23	16	-	PC7 ⁽⁸⁾	IOUDS	Port C bit 7 input / output	Open-drain port
			SCL	IO	I2C channel SCL input / output	
			T3IO	IO	Timer 3 input / output	
			RXD1	I	UART RXD1 input	
			SS	IO	SPI channel slave select input / output	
			AIP2	IA	Op-Amp positive input 2	

Table 9. Pin Description (continued)

Pin Number			Pin Name	Type	Function	Remark
48-LQFP	32-LQFP	28-TSSOP				
24	17	-	PC8 ⁽⁶⁾	IOUDS	Port C bit 8 input / output	Open-drain port
			SDA	IO	I2C channel SDA input / output	
			T1IO	IO	Timer 1 input / output	
			TXD1	O	UART TXD1 output	
			SCK	IO	SPI channel clock input / output	
			AIN2	IA	Op-Amp negative input 2	
25	-	-	PA12	IOUDS	Port A bit 12 input / output	
			T0IO	IO	Timer 0 input / output	
			AO2 ⁽¹⁾	OA	Op-Amp output 2	
26	-	-	PA13	IOUDS	Port C bit 13 input / output	
			T1IO	IO	Timer 1 input / output	
27	-	-	PA14	IOUDS	Port A bit 14 input / output	
			T2IO	IO	Timer 2 input / output	
28	-	-	PA15	IOUDS	Port A bit 15 input / output	
			T3IO	IO	Timer 3 input / output	
29	18	14	PA0	IOUDS	Port A bit 0 input / output	
			T2IO	IO	Timer 2 input / output	
			AN0 ⁽¹⁾	IA	Analog input 0	
30	19	15	PA1	IOUDS	Port A bit 1 input / output	
			T3IO	IO	Timer 3 input / output	
			CPOUT	O	Comparator output	
			AN1 ⁽¹⁾	IA	Analog input 1	
31	20	16	PA2	IOUDS	Port A bit 2 input / output	
			SS	IO	SPI channel slave select input / output	
			WDTO	O	Watchdog timer overflow output	
			AN2 ⁽¹⁾	IA	Analog input 2	
			CPA	IA	Comparator input A	
32	21	17	PA3	IOUDS	Port A bit 3 input / output	
			SCK	IO	SPI channel clock input / output	
			STBO	O	Deep sleep mode output	
			AN3 ⁽¹⁾	IA	Analog input 3	
			CPRE	IA	Comparator reference	
33	22	18	PA4	IOUDS	Port A bit 4 input / output	
			T0IO	IO	Timer 0 input / output	
			AN4 ⁽¹⁾	IA	Analog input 4	
			AIP0	IA	Op-Amp positive input 0	
			CPB	IA	Comparator input B	
34	23	19	PA5	IOUDS	Port A bit 5 input / output	
			T1IO	IO	Timer 1 input / output	
			AN5 ⁽¹⁾	IA	Analog input 5	
			AIN0	IA	Op-Amp negative input 0	
			CPC	IA	Comparator input C	

Table 9. Pin Description (continued)

Pin Number			Pin Name	Type	Function	Remark
48-LQFP	32-LQFP	28-TSSOP				
35	24	20	PA6	IOUDS	Port A bit 6 input / output	
			T0IO	IO	Timer 0 input / output	
			MOSI	IO	SPI channel master-out / slave-in	
			T2IO	IO	Timer 2 input / output	
			AN6 ⁽¹⁾	IA	Analog input 6	
			AO0	OA	Op-Amp output 0	
36	25	21	PA7	IOUDS	Port A bit 7 input / output	
			T1IO	IO	Timer 1 input/output	
			MISO	IO	SPI channel master-in / slave-out	
			T3IO	IO	Timer 3 input / output	
			AN7 ⁽¹⁾	IA	Analog input 7	
			AIP1	IA	Op-Amp positive input 1	
37	26	22	PA8	IODUS	Port A bit 8 input / output	
			T2IO	IO	Timer 2 input / output	
			T0IO	IO	Timer 0 input / output	
			AN8 ⁽¹⁾	IA	Analog input 8	
			AIN1	IA	Op-Amp negative input 1	
38	27	23	PA9	IODUS	Port A bit 9 input / output	
			T3IO	IO	Timer 3 input / output	
			T1IO	IO	Timer 1 input / output	
			AN9 ⁽¹⁾	IA	Analog input 9	
			AO1	OA	Op-Amp output 1	
39	-	-	PA10	IODUS	Port A bit 10 input / output	
			AN10 ⁽¹⁾	IA	Analog input 10	
40	-	-	PA11	IODUS	Port A bit 11 input / output	
			AN11 ⁽¹⁾	IA	Analog input 11	
41	28	24	PC10	IODUS	Port C bit 10 input / output	
			nRESET ⁽¹⁾⁽³⁾	IU	External reset input	Internal pull-up enable
42	29	25	VDD	P	VDD	
43	30	26	GND	P	GND	
44	31	27	PC12	IODUS	Port C bit 12 input / output	
			T3IO	IO	Timer 3 input / output	
			XIN ⁽⁹⁾	IA	External crystal oscillator input	
45	32	28	PC13	IODUS	Port C bit 13 input / output	
			T2IO	IO	Timer 2 input / output	
			XOUT ⁽⁹⁾	OA	External crystal oscillator output	
46	1	-	PD3	IODUS	Port D bit 3 input / output	
			MISO	IO	SPI channel master-in / slave-out	
			SDA	IO	I2C channel data input / output	
			TXD0	O	UART TXD0 output	
			SXIN ⁽⁹⁾	IA	External crystal sub oscillator input	

Table 9. Pin Description (continued)

Pin Number			Pin Name	Type	Function	Remark
48-LQFP	32-LQFP	28-TSSOP				
47	2	-	PD2	IODUS	Port D bit 2 input / output	
			MOSI	IO	SPI channel master-out / slave-in	
			SCL	IO	I2C channel clock input / output	
			RXD0	I	UART RXD0 input	
			SXOUT ⁽⁹⁾	OA	External crystal sub oscillator output	
48	-	-	PD1	IODUS	Port D bit 1 input / output	
			SCK	IO	SPI channel clock input / output	

NOTES:

1. I=Input, O=Output, U=Pull-up, D=Pull-down, S=Schmitt-Trigger Input Type, C=CMOS Input Type, A=Analog, P=Power
2. After a reset, all the pins are configured to function defined by their initial values. The initial value of the pin depends on the package type. This configuration is in compliance with the 48-pin standard.
3. PC11 (nBOOT), PC10 (nRESET), PC1 (SWDIO) and PC0 (SWCLK) are the default pull-up pins.
4. Do not configure unused pins as floating inputs.
5. After a reset, the internal pull-up for the boot pin is enabled.
6. After a reset, the internal pull-up for the serial wire clock (SWCLK) and the serial wire data I/O (SWDIO) is enabled.
7. The SWCLK and SWDIO pins should not be switched to other functions while they are being used.
8. PC7 and PC8 pins are open-drain ports.
9. When a function other than a clock is set through the PC12 (XIN), PC13 (XOUT), PD2(SXOUT) and PD3(SXIN) pins, other functions than the set clock will not operate normally if the clock is enabled by software.

2.3 Alternate Function Pins

The GPIO pins have alternate functions as described in Table 10.

Table 10. GPIO Alternate Functions

Pin Name	Alternate Function					
	AF0	AF1	AF2	AF3	AF4	AF5
PA0	PA0	T2IO				AN0*
PA1	PA1	T3IO			CPOUT	AN1*
PA2	PA2	SS	WDTO			AN2/CPA*
PA3	PA3	SCK	STBO			AN3/CPRE*
PA4	PA4			T0IO		AN4/AIP0/CPB*
PA5	PA5			T1IO		AN5/AIN0/CPC*
PA6	PA6	T0IO	MOSI	T2IO		AN6/AO0*
PA7	PA7	T1IO	MISO	T3IO		AN7/AIP1*
PA8	PA8	T2IO	T0IO			AN8/AIN1*
PA9	PA9	T3IO	T1IO			AN9/AO1*
PA10	PA10					AN10*
PA11	PA11					AN11*
PA12	PA12	T0IO				AO2*
PA13	PA13	T1IO				*
PA14	PA14	T2IO				*
PA15	PA15	T3IO				*
PB0	PB0	MPWMUH	SS			*
PB1	PB1	MPWMUL	SCK			*
PB2	PB2	MPWMVH	MOSI			*
PB3	PB3	MPWMVL	MISO			*
PB4	PB4	MPWMWH				*
PB5	PB5	MPWMWL				*
PB6	PB6	PRTIN		T0IO		*
PB7	PB7	OVIN	CLKO	T1IO		*

Table 10. GPIO Alternate Functions (continued)

Pin Name	Alternate Function					
	AF0	AF1	AF2	AF3	AF4	AF5
PC0	PC0	SWCLK*	RXD1			
PC1	PC1	SWDIO*	TXD1			
PC2	PC2					*
PC3	PC3					*
PC4	PC4		T0IO			*
PC5	PC5	RXD1	T1IO			*
PC6	PC6	TXD1	T2IO			*
PC7	PC7	SCL	T3IO	RXD1	SS	AIP2*
PC8	PC8	SDA	T1IO	TXD1	SCK	AIN2*
PC9	PC9	CLKO				*
PC10	PC10	nRESET*				
PC11	PC11	BOOT*	T0IO			
PC12	PC12	T3IO				XIN*
PC13	PC13	T2IO				XOUT*
PC14	PC14	RXD0	CLKO	OVIN	MOSI	*
PC15	PC15	TXD0		PRTIN	MISO	*
PD0	PD0	SS				*
PD1	PD1	SCK				*
PD2	PD2	MOSI	SCL		RXD0	SXOUT*
PD3	PD3	MISO	SDA		TXD0	SXIN*

NOTE:

1. The initial setting of each pin is marked by an asterisk (*). Unused pins are set to output from Firmware (Low output is recommended).

3. Electrical Characteristics

3.1 Parameter Conditions

Unless otherwise specified, all voltages are referenced to GND.

3.1.1 Minimum and Maximum Values

Unless otherwise specified, our production tests guarantee the minimum and maximum values of the device under the worst-case conditions of ambient temperature, supply voltage, and frequency.

Data based on characterization result, design simulation, and/or technical characteristics are not tested in production but indicated in the table footnotes.

3.1.2 Typical Value

Unless otherwise specified, typical data are based on the conditions of $T_A = 25^{\circ}\text{C}$ and $V_{DD} = AV_{DD} = 5.0\text{ V}$. The typical data are provided only as design recommendations and are not tested.

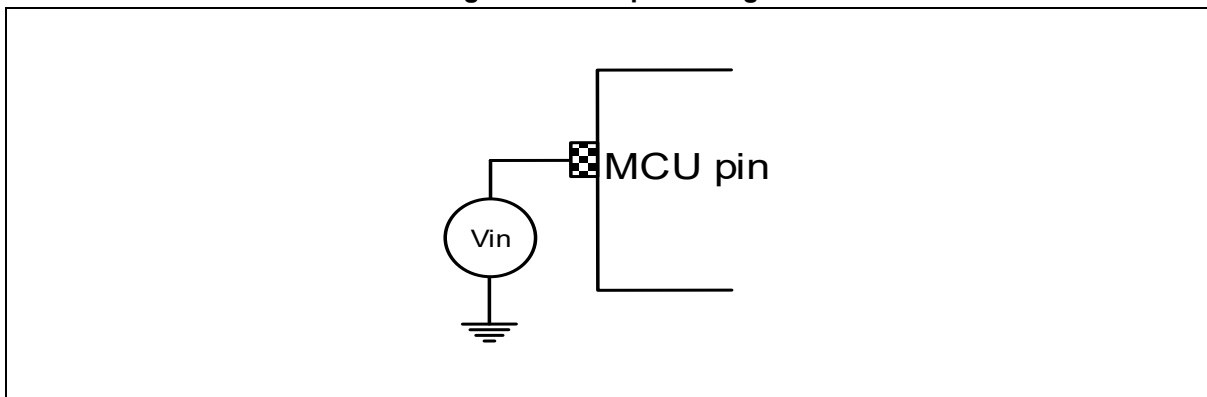
3.1.3 Typical Curves

Unless otherwise specified, all typical curves are provided only as design recommendations and are not tested.

3.1.4 Pin Input Voltage

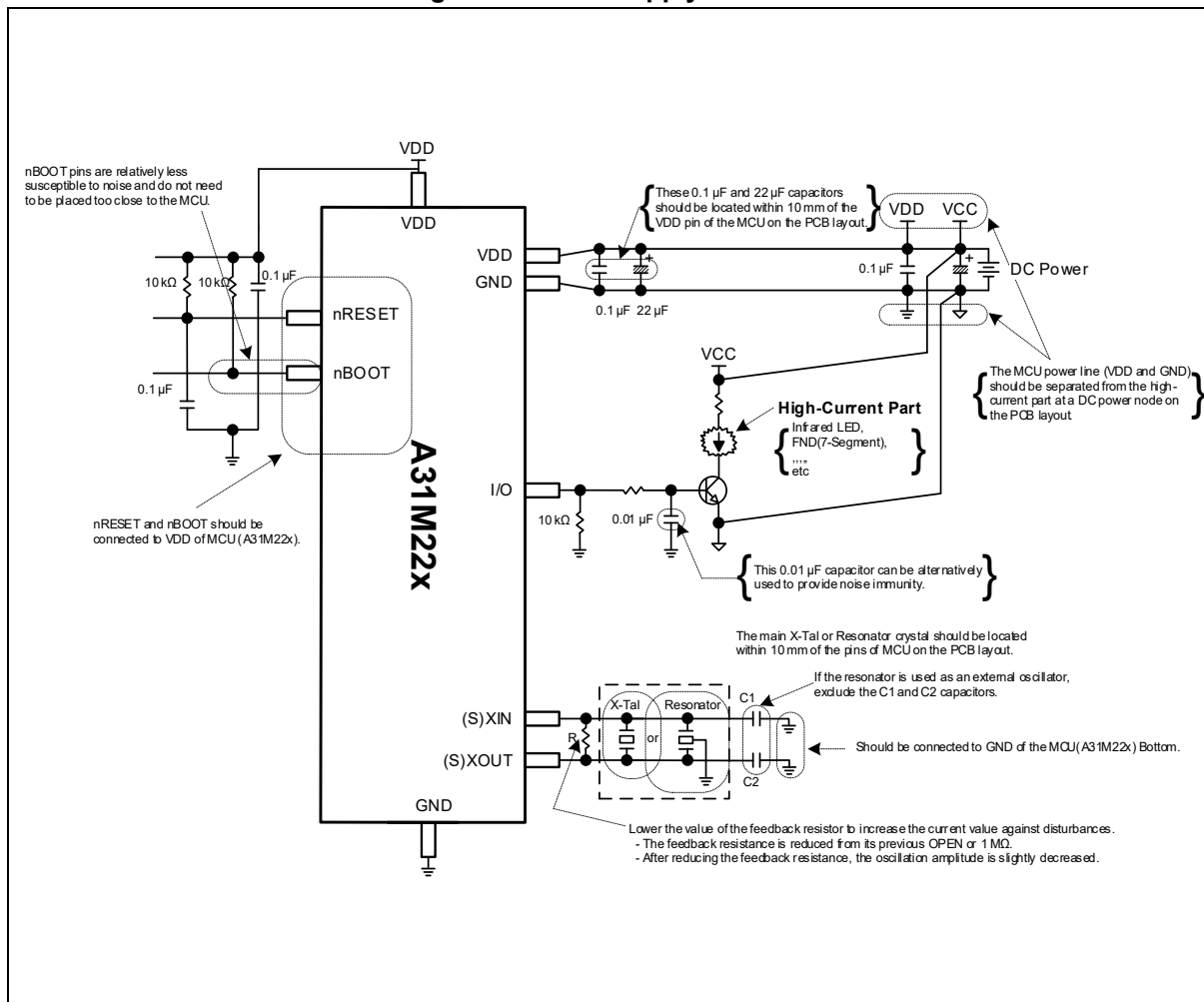
The input voltage measurement on a pin of the device is described in Figure 7.

Figure 7. Pin Input Voltage



3.1.5 Power Supply Scheme

Figure 8. Power Supply Scheme

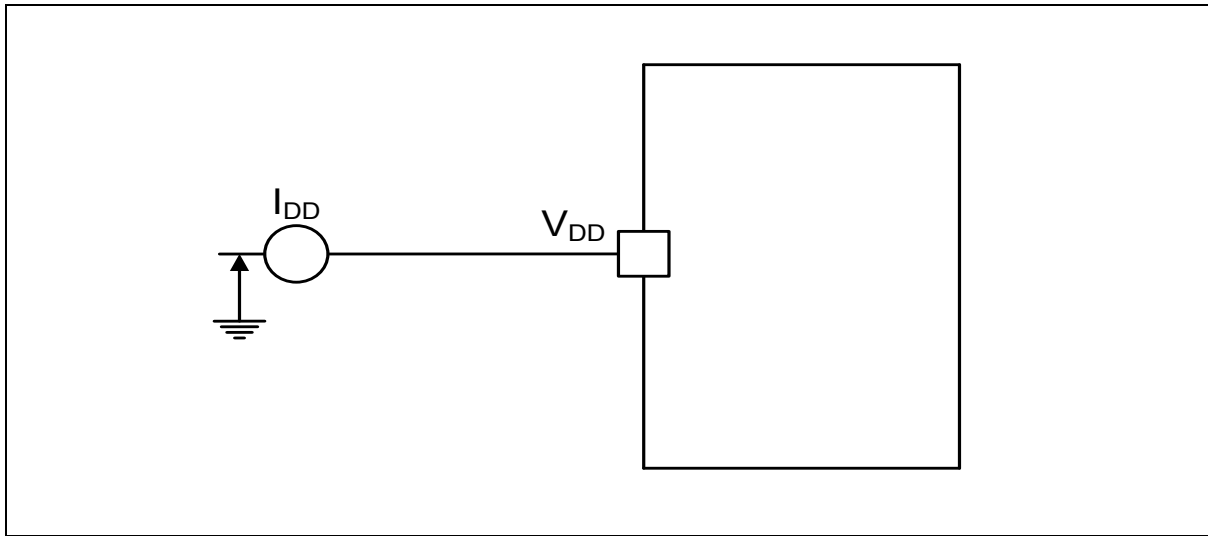


NOTE:

- Each power supply pair (VDD/GND etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

3.1.6 Current Consumption Measurement

Figure 9. Current Consumption Measurement



NOTE:

1. The I_{DD_ALL} parameter represents total microcontroller consumption including the current supplying V_{DD} .

3.2 Absolute Maximum Ratings

Exceeding stresses specified in the Table 11 for voltage characteristics, Table 12 for current characteristics, or Table 13 for thermal characteristics may result in permanent damage to the device. The values listed in the tables are stress ratings only, and do not imply that the device will function properly under these conditions. Prolonged exposure to these maximum rating conditions may impact on the reliability of the device. It is important to operate the device within its specified maximum ratings to ensure reliable performance.

Table 11. Voltage Characteristics

Symbol	Ratings	Min.	Max.	Unit
VDD - GND ⁽¹⁾	External main supply voltage (including VDD)	-0.5	6.0	V
VI ⁽²⁾	Input voltage on I/O	-0.3	Max. (VDD)+0.3	V
VO	Output voltage on I/O	-0.3	Max. (VDD)+0.3	V

NOTES:

1. All main power (VDD) and ground (GND) pins must always be connected to the external power supply, in the permitted range.
2. VI maximum must always be respected.

Table 12. Current Characteristics

Symbol	Ratings	Max.	Unit
$\sum I_{VDD}$	Total current into sum of all VDD power lines (source) ⁽¹⁾	120	mA
$\sum I_{GND}$	Total current out of sum of all GND ground lines (sink) ⁽¹⁾	120	mA
$I_{VDD(PIN)}$	Maximum current into each VDD power pin (source) ⁽¹⁾	100	mA
$I_{GND(PIN)}$	Maximum current out of each GND ground pin (sink) ⁽¹⁾	100	mA
$I_{IO(PIN)}$	Output current sunk by any I/O	5	mA
	Output current sourced by any I/O and control pin	5	mA
$\sum I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins ⁽²⁾	120	mA
	Total output current sourced by sum of all I/Os and control pins ⁽²⁾	120	mA
I_{IH}	Input high leakage current	1	μA
I_{IL}	Input low leakage current	1	μA
P_T	Total power dissipation	600	mW

NOTES:

1. All main power (VDD) and ground (GND) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP / TSSOP packages.

Table 13. Thermal Characteristics

Symbol	Ratings	Value	Unit
T _{OP}	Operating temperature	-40 to +105	°C
T _{STG}	Storage temperature range	-55 to +125	°C
T _J	Maximum junction temperature	+125	°C

3.3 Operating Condition

3.3.1 General Operating Condition

Table 14. General Operating Condition

(Temperature: -40°C to +105°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V _{DD}	Supply voltage	-	2.7 ⁽¹⁾	-	5.5	V
AV _{DD}	Analog supply voltage	ADC used	2.7	-	5.5	V
		CMP used	2.7	-	5.5	V
		Op-Amp used	2.7	-	5.5	V
		ADC, Op-Amp, CMP, not used	2.7	-	5.5	V
FREQ	Operating frequency	HSE	1	-	16	MHz
		LSE	-	32.768	-	kHz
		HSI	31.52	32	32.48	MHz
		LSI	350	500	650	kHz
		PLL	-	-	80	MHz
V _{IN}	I/O input voltage	5 V I/O	-0.3	-	V _{DD}	V
T _A	Ambient temperature	-	-40	-	105	°C
T _J	Junction temperature range	-	-	-	125	°C

NOTE:

1. When RESET is released, functionality is guaranteed down to V_{LVR5} Min.

3.3.2 Power on Reset Characteristics

Table 15. POR Electrical Characteristics

(Temperature: -40°C to +105°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I _{DD}	Operating current	-	-	0.062	0.2	μA
V _{set}	POR set level	-	1.2	1.4	1.6	V
t _R	VDD voltage rising time	-	20	-	20000	μs/V
t _F	VDD voltage falling time	-	400	-	20000	μs/V
V _{reset}	POR reset level	-	0.89	1.24	1.59	V

3.3.3 Operating Condition at Power-Up/Power-Down

The parameters listed in Table 16 are obtained through tests conducted under ambient temperature conditions, which are specified in Table 14.

Table 16. Operating Condition at Power-Up/Power-Down

(Temperature: -40°C to +105°C)

Symbol	Parameter	Condition	Min.	Max.	Unit
T_{VDD}	V_{DD} rise time rate	-	20	20000	$\mu\text{s/V}$
	V_{DD} fall time rate	-	400	20000	$\mu\text{s/V}$

3.3.4 Embedded Reset and Power Control Block Characteristics (LVR, LVI)

The parameters listed in Table 17 and Table 18 are obtained through tests conducted under ambient temperature conditions, which are specified in Table 14.

Table 17. Low Voltage Reset Characteristics

(Temperature: -40°C to +105°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V _{DD}	Operating voltage	-	0.8	5.0	5.5	V
V _{LVR5_F}	Detection level	Falling voltage	2.01	2.12	2.23	V
V _{LVR6_F}			2.19	2.30	2.42	
V _{LVR7_F}			2.35	2.47	2.59	
V _{LVR8_F}			2.54	2.67	2.80	
V _{LVR9_F}			2.89	3.04	3.19	
V _{LVR10_F}			3.02	3.18	3.34	
V _{LVR11_F}			3.41	3.59	3.77	
V _{LVR12_F}			3.53	3.72	3.91	
V _{LVR13_F}			3.83	4.03	4.23	
V _{LVR14_F}			3.99	4.20	4.41	
V _{LVR15_F}			4.26	4.48	4.70	
V _{LVR5_R}	Detection level	Rising voltage	2.09	2.20	2.31	V
V _{LVR6_R}			2.26	2.38	2.50	
V _{LVR7_R}			2.43	2.56	2.69	
V _{LVR8_R}			2.63	2.77	2.91	
V _{LVR9_R}			2.99	3.15	3.31	
V _{LVR10_R}			3.14	3.30	3.47	
V _{LVR11_R}			3.53	3.72	3.91	
V _{LVR12_R}			3.67	3.86	4.05	
V _{LVR13_R}			3.97	4.18	4.39	
V _{LVR14_R}			4.14	4.36	4.58	
V _{LVR15_R}			4.41	4.64	4.87	
-	Hysteresis	-	-	50	150	mV
-	Noise cancelling time	-	-	2	-	μs
I _{DD}	Operation current	-	-	3.5	5.5	μA
I _{DD, STOP}	Operation current (STOP)	-	-	2.5	3.0	nA

Table 18. Low Voltage Indicator Characteristics

(Temperature: -40°C to +105°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V _{DD}	Operating voltage	-	0.8	5.0	5.5	V
V _{LVI5_F}	Detection level	Falling voltage	2.01	2.12	2.23	V
V _{LVI6_F}			2.19	2.30	2.42	
V _{LVI7_F}			2.35	2.47	2.59	
V _{LVI8_F}			2.54	2.67	2.80	
V _{LVI9_F}			2.89	3.04	3.19	
V _{LVI10_F}			3.02	3.18	3.34	
V _{LVI11_F}			3.41	3.59	3.77	
V _{LVI12_F}			3.53	3.72	3.91	
V _{LVI13_F}			3.83	4.03	4.23	
V _{LVI14_F}			3.99	4.20	4.41	
V _{LVI15_F}			4.26	4.48	4.70	
V _{LVI5_R}	Detection level	Rising voltage	2.09	2.20	2.31	V
V _{LVI6_R}			2.26	2.38	2.50	
V _{LVI7_R}			2.43	2.56	2.69	
V _{LVI8_R}			2.63	2.77	2.91	
V _{LVI9_R}			2.99	3.15	3.31	
V _{LVI10_R}			3.14	3.30	3.47	
V _{LVI11_R}			3.53	3.72	3.91	
V _{LVI12_R}			3.67	3.86	4.05	
V _{LVI13_R}			3.97	4.18	4.39	
V _{LVI14_R}			4.14	4.36	4.58	
V _{LVI15_R}			4.41	4.64	4.87	
-	Hysteresis	-	-	50	150	mV
-	Noise cancelling time	-	-	2	-	μs
I _{DD}	Operation current	-	-	3.5	5.5	μA
I _{DD, STOP}	Operation current (STOP)	-	-	2.5	3.0	nA

3.3.5 Embedded Voltage Reference

Table 19. Embedded Internal Voltage Reference

(Temperature: -40°C to +105°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V _{REFINT}	Internal reference voltage	-40°C < T _A < +105°C	0.95	1.00	1.05	V
V _{CORE}	Logic power voltage		1.35	1.50	1.65	

3.3.6 Supply Current Characteristics

The amount of current consumed by the device is determined by various factors and parameters, including but not limited to the operating voltage, ambient temperature, load on I/O pins, software configuration, operating frequency, switching rate of I/O pins, location of the program in memory, and the binary code being executed.

The current consumption is measured under the conditions specified in Table 20.

3.3.6.1 Supply current consumption

Table 20. Supply Current Characteristics

(Temperature: -40°C to +105°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	unit
I _{DD1} (Run)	Supply current	f _{XIN} = 8 MHz	V _{DD} =5 V±10% All peripherals off	2.1	-	mA
		f _{HSI} = 32 MHz		5.7	-	mA
		f _{PLL} = 80 MHz		13.6	-	mA
		f _{LSI} = 500 kHz		348	-	µA
		f _{LSE} = 32.768 kHz		253	-	µA
I _{DD2} (Sleep)		f _{XIN} = 8 MHz	V _{DD} =5 V±10% All peripherals off	1.9	-	mA
		f _{HIRC} = 32 MHz		4.8	-	mA
		f _{PLL} = 80 MHz		11.7	-	mA
		f _{LIRC} = 500 kHz		347	-	µA
		f _{LSE} = 32.768 kHz		252	-	µA
I _{DD3} (Deep-Sleep)		All off	V _{DD} =5 V±10% All peripherals off	100	150	µA

NOTE:

1. In DEEP-SLEEP mode, all clocks are disabled.

3.3.6.2 I/O System Current Consumption

In the I/O system, current consumption can be separated into two components: Static and Dynamic.

3.3.6.3 I/O Static Current Consumption

When I/O pins configured as inputs with pull-up are externally held low, they generate a current consumption. This current consumption can be simply calculated using the values of the pull-up/pull-down resistors specified in the I/O port characteristics.

To estimate the current consumption for output pins, any external pull-down or load must also be taken into consideration.

The current consumption of I/O pins configured as inputs may increase when an intermediate voltage level is applied externally. This additional consumption is caused by the input schmitt trigger circuits that are used to detect the input value. Unless such a configuration is necessary for the application, this current consumption can be avoided by configuring these I/Os in analog mode. This is especially relevant for ADC, Op-Amp, and CMP input pins, which should be set up as analog inputs.

3.3.6.4 I/O Dynamic Current Consumption

Besides the internal peripheral current consumption, the application's I/Os also contribute to the overall current consumption. When an I/O pin switches, it draws current from the microcontroller's supply voltage to power the I/O pin circuitry and to charge/discharge any capacitive loads (either internal or external) connected to the pin.

3.3.7 External Clock Source Characteristics

3.3.7.1 High-Speed External Clock Generated from Crystal/Ceramic Resonator

The high-speed external (HSE) clock can be generated using a crystal/ceramic resonator oscillator with a frequency range of 1 to 16 MHz. The information provided in this paragraph is based on characterization results obtained using typical external components listed in Table 21.

To minimize output distortion and startup stabilization time, it is recommended to place the resonator and load capacitors as close as possible to the oscillator pins in the application.

For further information on the resonator characteristics such as frequency, package, and accuracy, it is advisable to refer to the crystal resonator manufacturer.

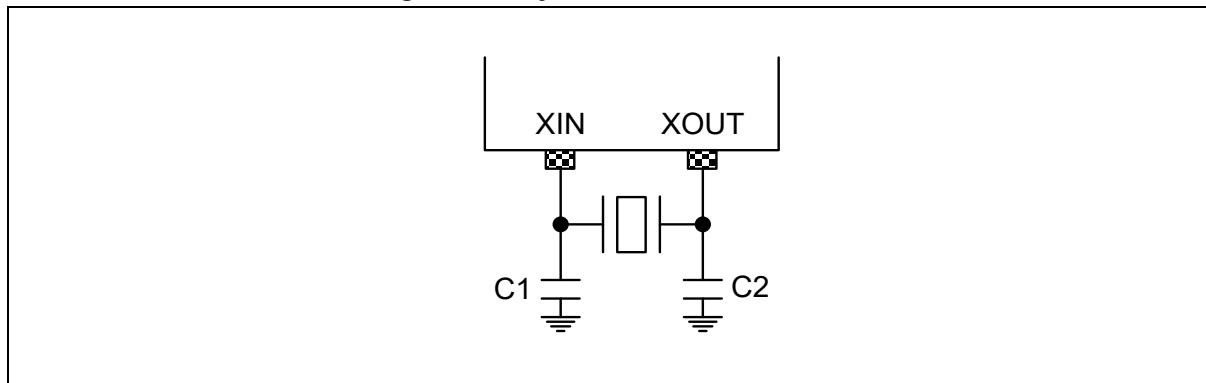
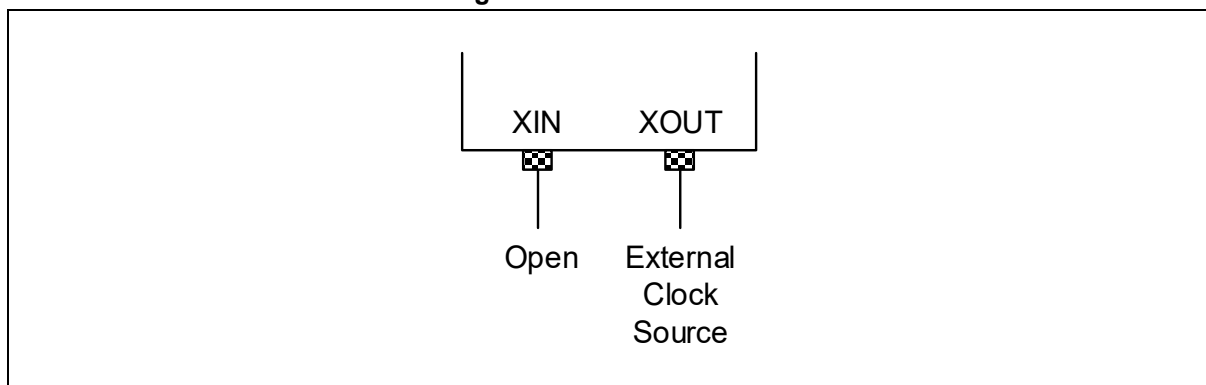
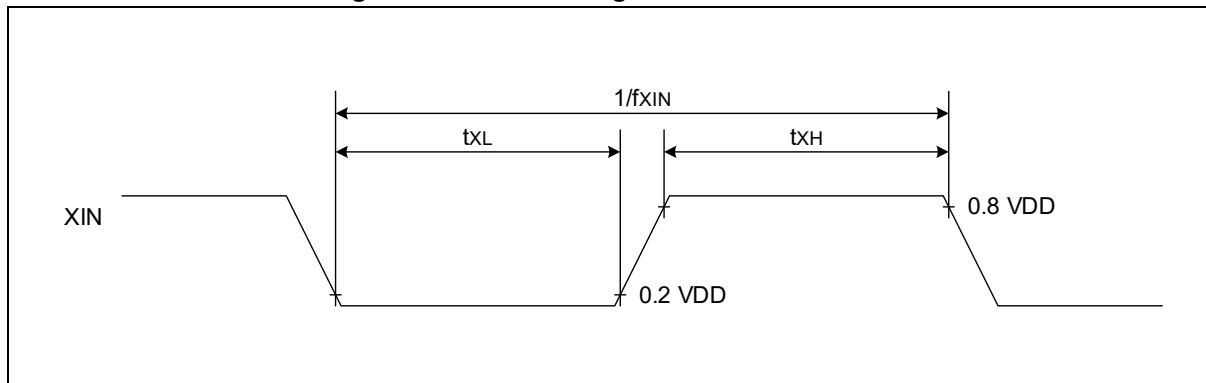
Table 21. HSE Oscillator Characteristics⁽¹⁾

(Temperature: -40°C to +105°C)

Symbol	Parameter	Condition ⁽²⁾	Min.	Typ.	Max.	Unit
V _{DD}	Operating voltage	-	1.8	5.0	5.5	V
I _{DD(HSE)}	HSE current consumption	-	-	-	2.5	mA
I _{STOP}	Power down current	-	-	0.2	30	nA
f _{OSC_IN}	Oscillator frequency	-	1	8	16	MHz
F _{out}	Output frequency	V _{DD} ≥ 1.8 V ⁽⁴⁾	1	-	4	MHz
		V _{DD} ≥ 2.0 V ⁽⁵⁾	1	-	8	
		V _{DD} ≥ 2.2 V ⁽⁶⁾	1	-	12	
		V _{DD} ≥ 2.4 V ⁽⁷⁾	1	-	16	
V _{IL}	Crystal input (low)	-	-	-	0.2×V _{DD}	V
V _{IH}	Crystal input (high)	-	0.8×V _{DD}	-	-	V
V _{OL}	Crystal out (low)	-	-	-	0.2×V _{DD}	V
V _{OH}	Crystal out (high)	-	0.8×V _{DD}	-	-	V
C _L	External load capacitor	1 MHz < f _{OUT} < 4 MHz	18	30	35	pf
		4 MHz < f _{OUT} < 12 MHz	10	22	30	pf
		12 MHz < f _{OUT} < 16 MHz	7	18	22	pf
R _F	Feedback resistor	V _{DD} = 5 V	0.76	1.0	1.3	MΩ
t _{SU(HSE)} ⁽³⁾	Startup time	-	-	1	-	ms

NOTES:

1. Guaranteed by design.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. t_{SU(HSE)} is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.
4. HSEISEL = 0x3, HSENFSEL = 0x0
5. HSEISEL = 0x2, HSENFSEL = 0x1
6. HSEISEL = 0x1, HSENFSEL = 0x2
7. HSEISEL = 0x0, HSENFSEL = 0x3

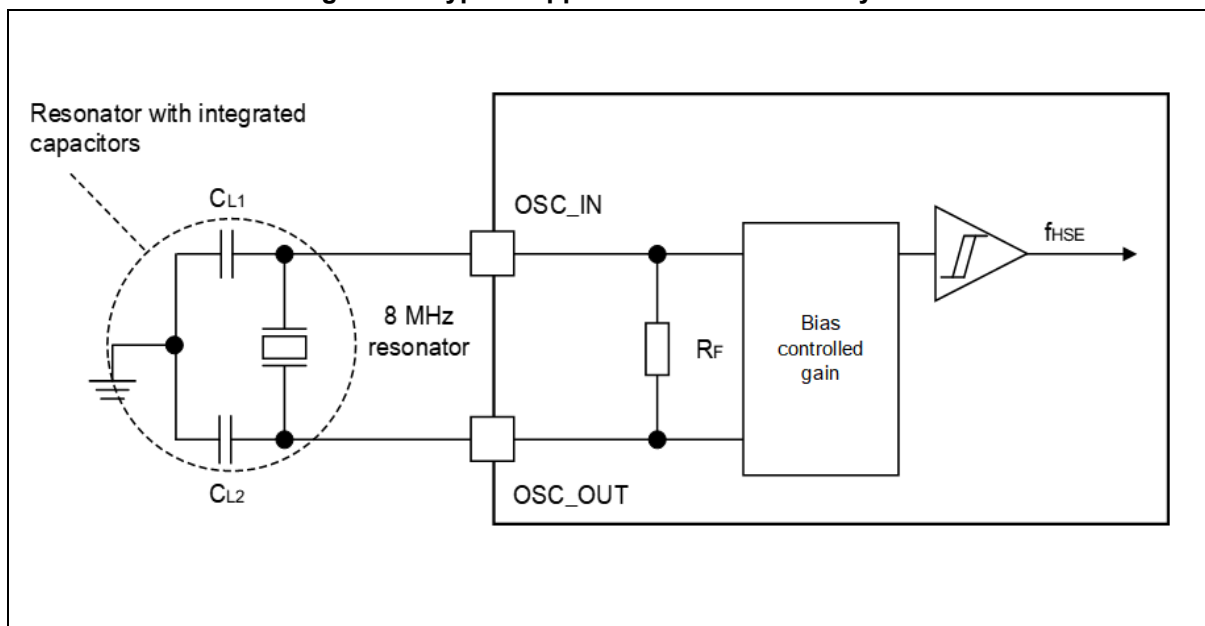
Figure 10. Crystal/Ceramic Oscillator**Figure 11. External Clock****Figure 12. Clock Timing Measurement at XIN**

It is recommended to use high-quality external ceramic capacitors designed for high-frequency applications and selected to match the requirements of the crystal or resonator. The capacitance of the CL1 and CL2 capacitors should be between 5 pF to 20 pF.

The CL1 and CL2 capacitors are usually of the same size, and the crystal manufacturer typically specifies a load capacitance, which is the series combination of both capacitors. However, the capacitance of the printed circuit board (PCB) and microcontroller pin should also be considered, which must be included in the calculation of the overall capacitance. A rough estimate of the combined pin and board capacitance is around 10 pF, which can be used to size CL1 and CL2 appropriately.

Figure 13 shows a circuit diagram of a typical application with an 8 MHz crystal.

Figure 13. Typical Application With 8 MHz Crystal



3.3.7.2 Low-Speed External Clock Generated from Crystal Resonator

The low-speed external (LSE) clock can be generated using a crystal/ceramic resonator oscillator with a 32.768 kHz. The information provided in this paragraph is based on characterization results obtained using typical external components listed in Table 22.

To minimize output distortion and startup stabilization time, it is recommended to place the resonator and load capacitors as close as possible to the oscillator pins in the application.

For further information on the resonator characteristics such as frequency, package, and accuracy, it is advisable to refer to the crystal resonator manufacturer.

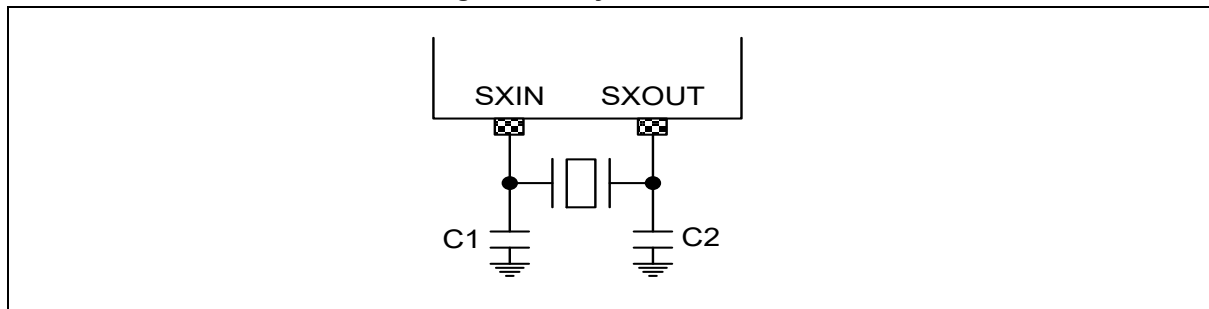
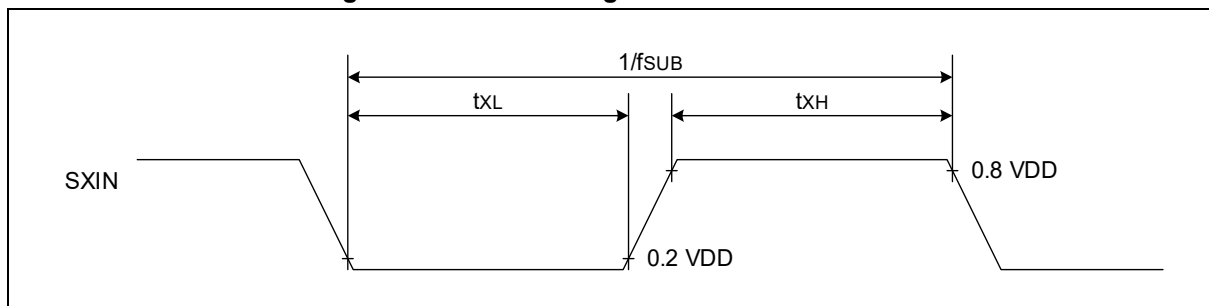
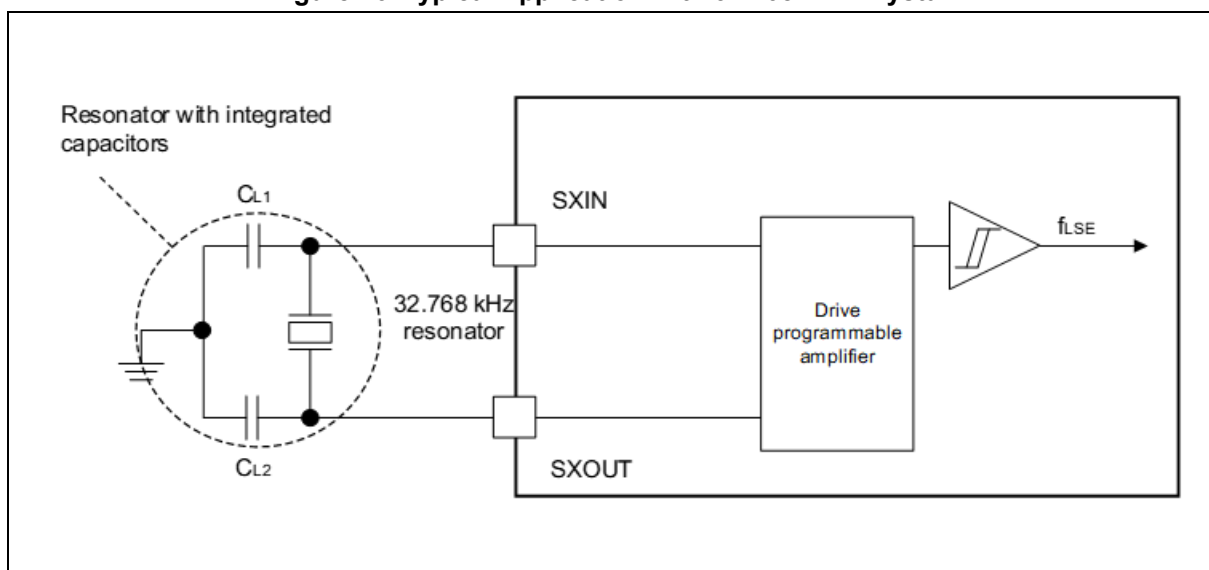
Table 22. LSE Oscillator Characteristics⁽¹⁾ (fLSE = 32.768 kHz)

(Temperature: -40°C to +105°C)

Symbol	Parameter	Condition ⁽²⁾	Min.	Typ.	Max.	Unit
V _{DD}	Operating voltage	-	2.7	5.0	5.5	V
I _{DD(LSE)}	LSE current consumption	-	-	2	7	μA
I _{STOP}	Power down current	-	-	0.3	25	nA
f _{OSC_IN}	Oscillator frequency	-	-	32.768	-	kHz
V _{IL}	Crystal input (low)	-	-	-	0.2 V _{DD}	V
V _{IH}	Crystal input (High)	-	0.8 V _{DD}	-	-	V
V _{OL}	Crystal out (low)	-	-	-	0.2 V _{DD}	V
V _{OH}	Crystal out (high)	-	0.8 V _{DD}	-	-	V
C _L	External load capacitor	-	5	15	35	pF
R _F	Feedback resistor	-	5	12	24	MΩ
t _{SU(LSE)} ⁽²⁾	Startup time	-	-	-	1	s

NOTES:

1. Guaranteed by design.
2. t_{SU(LSE)} is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 14. Crystal Oscillator**Figure 15. Clock Timing Measurement at SXIN****Figure 16. Typical Application with 32.768 kHz Crystal****NOTE:**

1. An external resistor is not required between SXIN and SXOUT and it is forbidden to add one.

3.3.8 Internal Clock Source Characteristics

The parameters listed in Table 23 and Table 24 are obtained through tests conducted under ambient temperature and supply voltage conditions, which are specified in Table 14.

3.3.8.1 High-Speed Internal (HSI32) RC Oscillator

Table 23. HSI32 Oscillator Characteristics⁽¹⁾

(Temperature: -40°C to +105°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V _{DD}	Operating voltage	-	2.7	-	5.5	V
f _{HSI32}	HSI32 frequency	-	31.52	32	32.48	MHz
f _E	Frequency error	@ -20°C to 85°C	-1.0	-	1.0	%
		@ -40°C to 105°C	-1.5	-	+1.5	%
DuCy (HSI32)	Duty cycle	-	45	-	55	%
ΔV _{DD} (HSI32)	HSI32 oscillator frequency drift over V _{DD}	V _{DD} =2.7 V to 5.5 V	-0.2	-	0.2	%
t _{su} (HSI32)	HSI32 oscillator start-up time	-	-	1	2	μs
t _{stab} (HSI32)	HSI32 oscillator stabilization time	-	-	4	10	μs
I _{DD} (HSI32)	HSI32 oscillator power consumption	-	-	330	-	μA

NOTE:

1. Guaranteed by characterization results and design.

3.3.8.2 Low-Speed Internal (LSI) 500 kHz RC Oscillator

Table 24. LSI Oscillator Characteristics

(Temperature: -40°C to +105°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Operating voltage	-	2.7	-	5.5	V
f_{OUT}	Output frequency	$V_{DD}=1.8$ to 5.5 V	350	500	650	kHz
$t_{VREG_SU}^{(1)}$	500 kHz oscillator VREG start-up time (after LSI 500K LDO enabled)	$V_{DD} = 5.0$ V $V_{DD} = 1.5$ V	-	25	40	μ s
$t_{STAB}^{(1)}$	500 kHz oscillator stabilization time (after LSI 500K enabled)	5% of target frequency	-	20	120	μ s
$I_{LIRC}^{(1)}$	500 kHz oscillator power consumption	The LSI oscillator is enabled. $V_{DD}=1.8$ to 5.5 V	-	1.5	4.9	μ A
		The LSI oscillator is disabled. $V_{DD}=1.8$ to 5.5 V	-	2.6	682	nA

NOTE:

1. Guaranteed by design.

3.3.9 PLL Characteristics

The parameters listed in Table 25 are obtained through tests conducted under ambient temperature and supply voltage conditions, which are specified in Table 14.

Table 25. PLL Characteristics⁽¹⁾

(Temperature: -40°C to +105°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V _{DD}	Operating voltage	-	2.7	-	5.5	V
I _{DD} (PLL)	PLL power consumption on V _{DD}	VCO freq = 160 MHz, F _{out} = 80 MHz	-	0.461	0.604	mA
f _{PLL_P_OUT}	PLL output clock	Voltage scaling range	-	-	80	MHz
f _{VCO_OUT}	PLL VCO output	VCO frequency range	9	-	351	MHz
f _{DUTY}	Duty	-	40	-	60	%
f _{PLLINCLK}	Input frequency	-	2	-	16	MHz
t _{JITTER}	P-P jitter	@ Lock state	-	-	500	ps
t _{LOCK}	PLL lock time	-	-	60	100	μs

NOTE:

1. Guaranteed by design.

3.3.10 Flash Memory Characteristics

Table 26. Flash Memory Characteristics

(Temperature: -40°C to +105°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
-	Max available clock frequency	0-wait	-	-	27	MHz
t _{RSTBUSY}	Reset cycle time	-	8	-	-	μs
t _{FRDBUSY}	Fuse program time	-	-	-	6	μs
t _{PGMBUSY}	Normal program time	-	-	-	25	μs
t _{BMPGMBUSY}	Burst program time	-	-	-	15	μs
t _{PERSBUSY}	Normal Page erase time	-	-	-	2	ms
t _{SERSBUSY}	Sector erase time	-	-	-	2	ms
t _{MERSBUSY}	Mat erase time	-	-	-	8	ms
Cycle	Number of code flash rewrites	Retained for 10 years T _A =25°C	10,000	-	-	times
Cycle	Number of code flash rewrites	Retained for 20 years T _A =85°C	100	-	-	times

3.3.11 I/O Port Characteristics

Table 27. DC Electrical Characteristics

(Temperature: -40°C to +105°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH1}	Input high voltage	PA[15:0], PB[7:0], PC[6:0], PC[15:9], PD[3:0]	$0.8 \times V_{DD}$	-	-	V
V_{IL1}	Input low voltage	PA[15:0], PB[7:0], PC[6:0], PC[15:9], PD[3:0]	-	-	$0.2 \times V_{DD}$	V
V_{IH2}	Open-drain input high voltage	PC[8:7]	$0.7 \times V_{DD}$	-	-	V
V_{IL2}	Open-drain input low voltage	PC[8:7]	-	-	$0.3 \times V_{DD}$	V
V_{OH1}	Output high voltage	$V_{DD}=4.5\text{ V}$, $I_{OH1} = -3\text{ mA}$	$0.8 \times V_{DD}$	-	-	V
V_{OL1}	Output low voltage	$V_{DD}=4.5\text{ V}$, $I_{OL1} = 3\text{ mA}$	-	-	$0.2 \times V_{DD}$	V
I_{OL1}	Output low current	$V_{DD}=5\text{ V}$, $V_{OL}=0.2 V_{DD}$	-	-	4	mA
I_{OH1}	Output high current	$V_{DD}=5\text{ V}$, $V_{OH}=0.8 V_{DD}$	-2.6	-	-	mA
I_{OL2}	Output low current	$V_{DD}=5\text{ V}$, $V_{OL}=0.2 V_{DD}$	-	-	10	mA
I_{OH2}	Output high current	$V_{DD}=5\text{ V}$, $V_{OH}=0.8 V_{DD}$	-7.5	-	-	mA
I_{IH}	Input high leakage current	All Input ports	-	-	1	μA
I_{IL}	Input low leakage current	All Input ports	-1	-	-	μA
R_{PU}	Pull-up resistor	$R_{MAX}: V_{DD} = 2.7\text{ V}$ $R_{MIN}: V_{DD} = 5\text{ V}$	30	-	70	k Ω

3.3.11.1 General Input/Output Characteristics

Unless otherwise specified, the parameters in Table 28 are obtained through tests conducted under the conditions, which are specified in Table 14. All I/Os conform to CMOS and TTL standards.

Table 28. I/O Static Characteristics

(Temperature: -40°C to +105°C)

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
$V_{IL1}^{(1)}$	I/O input low level voltage	5 V GPIO	$2.7\text{ V} < V_{DD} < 5.5\text{ V}$	-	-	$0.2 \times V_{DD}$	V
$V_{IH1}^{(1)}$	I/O input high level voltage	5 V GPIO	$2.7\text{ V} < V_{DD} < 5.5\text{ V}$	$0.8 \times V_{DD}$	-	-	V
$V_{IL2}^{(1)}$	Open-drain Input high voltage	5 V GPIO	$2.7\text{ V} < V_{DD} < 5.5\text{ V}$	-	-	$0.3 \times V_{DD}$	V
$V_{IH2}^{(1)}$	Open-drain Input low voltage	5 V GPIO	$2.7\text{ V} < V_{DD} < 5.5\text{ V}$	$0.7 \times V_{DD}$	-	-	V
$V_{HYS}^{(2)}$	Input hysteresis	5 V GPIO	$2.7\text{ V} < V_{DD} < 5.5\text{ V}$ $V_{DDTYPICAL} = 5\text{ V}$	-	1	-	V
I_{leak}	Input leakage current ⁽²⁾	5 V GPIO	$2.7 < V_{IN} \leq V_{DD} \times 1.1$	-	-	± 150	nA
R_{PU}	Weak pullup equivalent resistor	$V_{IN} = \text{GND}$		30	50	70	kΩ
R_{PD}	Weak pulldown equivalent resistor	$V_{IN} = V_{DD}$		30	50	70	
C_{IO}	I/O pin capacitance	I/O pin capacitance		-	5	-	pF

NOTES:

1. Data based on characterization results are not tested in production.
2. Guaranteed by design.

3.3.11.2 Output Driving Current

The GPIOs are capable of sinking or sourcing currents up to $\pm 8\text{ mA}$ and can also sink or source currents up to $\pm 20\text{ mA}$ when the V_{OL}/V_{OH} limits are relaxed.

To ensure compliance with the absolute maximum ratings specified in chapter 3.2, it is necessary to limit the number of I/O pins driving current in the user application.

- The total current sourced by all I/O pins on VDD and the maximum operating current of the microcontroller on VDD (during Run mode) must not exceed the absolute maximum rating ΣI_{VDD} specified in Table 12.
- The total current sunk by all I/O pins on GND and the maximum operating current of the microcontroller on GND (during Run mode) must not exceed the absolute maximum rating ΣI_{GND} specified in Table 12.

3.3.11.3 Output Voltage Levels

Unless otherwise specified, the parameters in Table 29 are obtained through tests conducted under ambient temperature and supply voltage conditions, which are specified in Table 14.

Table 29. Output Voltage Characteristics

(Temperature: -40°C to +105°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{OH1}	Output high level voltage for an I/O pin	$V_{DD} = 4.5\text{ V}$, $I_{OH1} = -3\text{ mA}$	$V_{DD}-1.0$	-	-	V
V_{OL1}	Output low level voltage for an I/O pin	$V_{DD} = 4.5\text{ V}$, $I_{OH1} = 3\text{ mA}$	-	-	1.0	
I_{OL1}	Output low level voltage for an I/O pin	$V_{DD} = 5\text{ V}$, $V_{OL} = 0.2 V_{DD}$	-	-	4	mA
I_{OH1}	Output high current	$V_{DD} = 5\text{ V}$, $V_{OH} = 0.8 V_{DD}$	-2.6	-	-	mA
I_{OL2}	Output low current	$V_{DD} = 5\text{ V}$, $V_{OL} = 0.2 V_{DD}$	-	-	10	mA
I_{OH2}	Output high current	$V_{DD} = 5\text{ V}$, $V_{OH} = 0.8 V_{DD}$	-7.5	-	-	mA

3.3.12 Analog-to-Digital Converter Characteristics

Table 30. ADC Electrical Characteristics

(Temperature: -40°C to +105°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	unit
AV _{DD}	Operating voltage	-	2.5	5	5.5	V
-	Resolution	-	-	-	12	bit
I _{DDA}	Operating current	AV _{DD} = 5.0 V @ f _{MCLK} = 42 MHz	-	3	-	mA
V _{AN}	Analog input range	-	GND	-	AV _{DD}	V
MCLK	Input clock frequency	@ AV _{DD} > 3.7 V	-	-	42	MHz
		@ AV _{DD} > 3.1 V	-	-	34	MHz
		@ AV _{DD} > 2.7 V	-	-	20	MHz
t _{CONV}	Conversion time	-	18×MCLK	-	48×MCLK	μs
F _{CONV}	Conversion frequency	@ AV _{DD} > 3.7 V	-	-	2.0	MHz
		@ AV _{DD} > 3.1 V	-	-	1.6	MHz
		@ AV _{DD} > 2.7 V	-	-	1.0	MHz
ACLK	Operating frequency	-	-	-	42	MHz
INL	DC accuracy	-	-	±2.5	±4	LSB
DNL		-	-	±1.5	±2	LSB
ZOE	Zero offset error	-	-	±2	±4	LSB
FSE	Full scale error	-	-	±2	±4	LSB

3.3.12.1 General PCB Design Guidelines

The power supply must be separated in accordance with the scheme shown in Figure 8. The decoupling capacitors across the VDD/AVDD are ceramic (good quality) capacitors and must be placed as close as possible to the chip.

3.3.13 Comparator Characteristics

Table 31. Comparator Characteristics

(Temperature: -40°C to +105°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V _{DD}	Operating voltage	-	2.7	-	5.5	V
T _A	Operating temperature	-	-40	25	105	°C
I _{DD}	Operating current	-	-	160	450	μA
V _{IVR}	Input voltage range	-	0	-	5.5	V
V _{IO}	Input offset voltage	-	-5	-	+5	mV
t _D	Propagation delay	Overdrive voltage 100 mV 50 pF load on	-	-	200	ns
V _{HYS}	Hysteresis	HYSTSEL[1:0] = '00'	8	10	16	mV
		HYSTSEL[1:0] = '01'	15	20	30	mV
		HYSTSEL[1:0] = '10'	20	30	45	mV
		HYSTSEL[1:0] = '11'	30	40	58	mV

3.3.14 Operational Amplifier Characteristics

Table 32. Op-Amp Characteristics

(Temperature: -40°C to +105°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{DD} (RMS)	Operating current	-	-	630	-	μA
G_E	Gain error	Gain= $\times 20$	-	-	3	%
F_{GB}	Gain bandwidth	CL=200 pF	-	5	-	MHz
A_V	Open loop voltage gain	-	-	100	-	dB
PM	Phase margin	CL=20 pF	-	80	-	Degree
V_{IO}	Input offset voltage	-	-	-	± 1.5	mV
V_I	Input voltage range	-	0	-	V_{DD}	V
V_O	Output voltage range	-	20 mV	-	$V_{DD}-20$ mV	V
CMRR	Common mode rejection ratio	-	-	100	-	dB
PSRR	Power supply rejection ratio	-	-	90	-	dB
SR	Slew rate	CL=200 pF	-	1	-	V/ μs
T_{PR}	Pulse response	-	-	-	1	μs

3.3.15 Communication Interfaces Characteristics

3.3.15.1 I2C Interface Characteristics

The I2C interface conforms to the timing requirements specified in the I2C-bus specification, in addition to the user timing requirements listed below:

- Standard mode (Sm): up to 100 kbps bit rate
- Fast mode (Fm): up to 400 kbps bit rate

The I2C timing requirements are guaranteed by design when the I2C peripheral is configured correctly and the I2C clock frequency is equal to or greater than the minimum value listed in the table below.

Table 33. I2C Characteristics

(Temperature: -40°C to +105°C)

Symbol	Parameter	Standard		Fast		Unit
		Min.	Max.	Min.	Max.	
t _{SCL}	Clock frequency	0	100	0	400	kHz
t _{SCLH}	Clock high pulse width	4.0	-	0.6	-	μs
t _{SCLL}	clock low pulse width	4.7	-	1.3	-	
t _{BF}	Bus free time	4.7	-	1.3	-	
t _{STSU}	Start condition setup time	4.7	-	0.6	-	
t _{STHD}	Start condition hold time	4.0	-	0.6	-	
t _{SPSU}	Stop condition setup time	4.0	-	0.6	-	
t _{SPHD}	Stop condition hold time	4.0	-	0.6	-	
t _{VD}	Output valid from clock	0	-	0	-	
t _{DIH}	Data input hold time	0	-	0	1.0	
t _{DIS}	Data input setup time	250	-	100	-	ns

3.3.15.2 SPI Interface Characteristics

Unless otherwise specified, the parameters in Table 34 are obtained through tests conducted under ambient temperature, f_{CLK} frequency and supply voltage conditions, which are specified in Table 14.

For more information about I/O alternate function characteristics (SS, SCK, MOSI, and MISO for SPI), refer to 3.3.11.

Table 34. SPI Characteristics

(Temperature: -40°C to +105°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{SCK1}	SPI clock frequency with strength on	$V_{DD} \leq 1.8\text{ V}$	-	-	12	MHz
f_{SCK2}		$V_{DD} \leq 3.3\text{ V}$	-	-	12	MHz
f_{SCK3}		$V_{DD} \leq 5.5\text{ V}$	-	-	12	MHz
f_{SCK4}	SPI clock frequency with strength off	$V_{DD} \leq 1.8\text{ V}$	-	-	5	MHz
f_{SCK5}		$V_{DD} \leq 3.3\text{ V}$	-	-	8	MHz
f_{SCK6}		$V_{DD} \leq 5.5\text{ V}$	-	-	10	MHz
Duty	Duty cycle of SPI frequency (SCK)	Slave mode	30	50	70	%

3.3.15.3 UART Interface Characteristics**Table 35. UART Characteristics**

(Temperature: -40°C to +105°C)

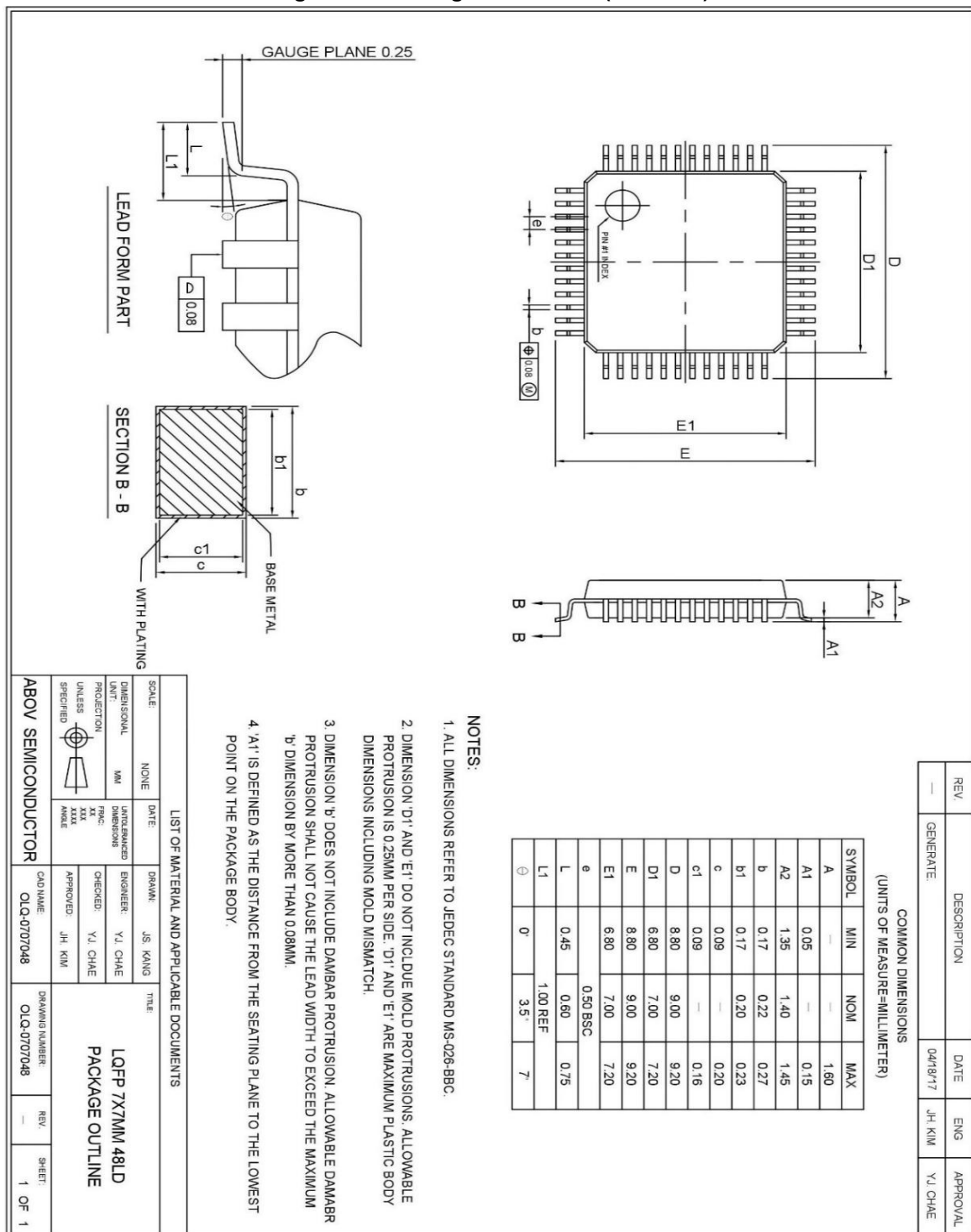
Symbol	Parameter	Typ.	Limit	Units
F_{max}	Maximum character transmission frequency	-	0.8	Mbits

4. Package Information

4.1 48-LQFP Package Information

LQFP-48 is a 48-pin, 7 x 7 mm quad flat package.

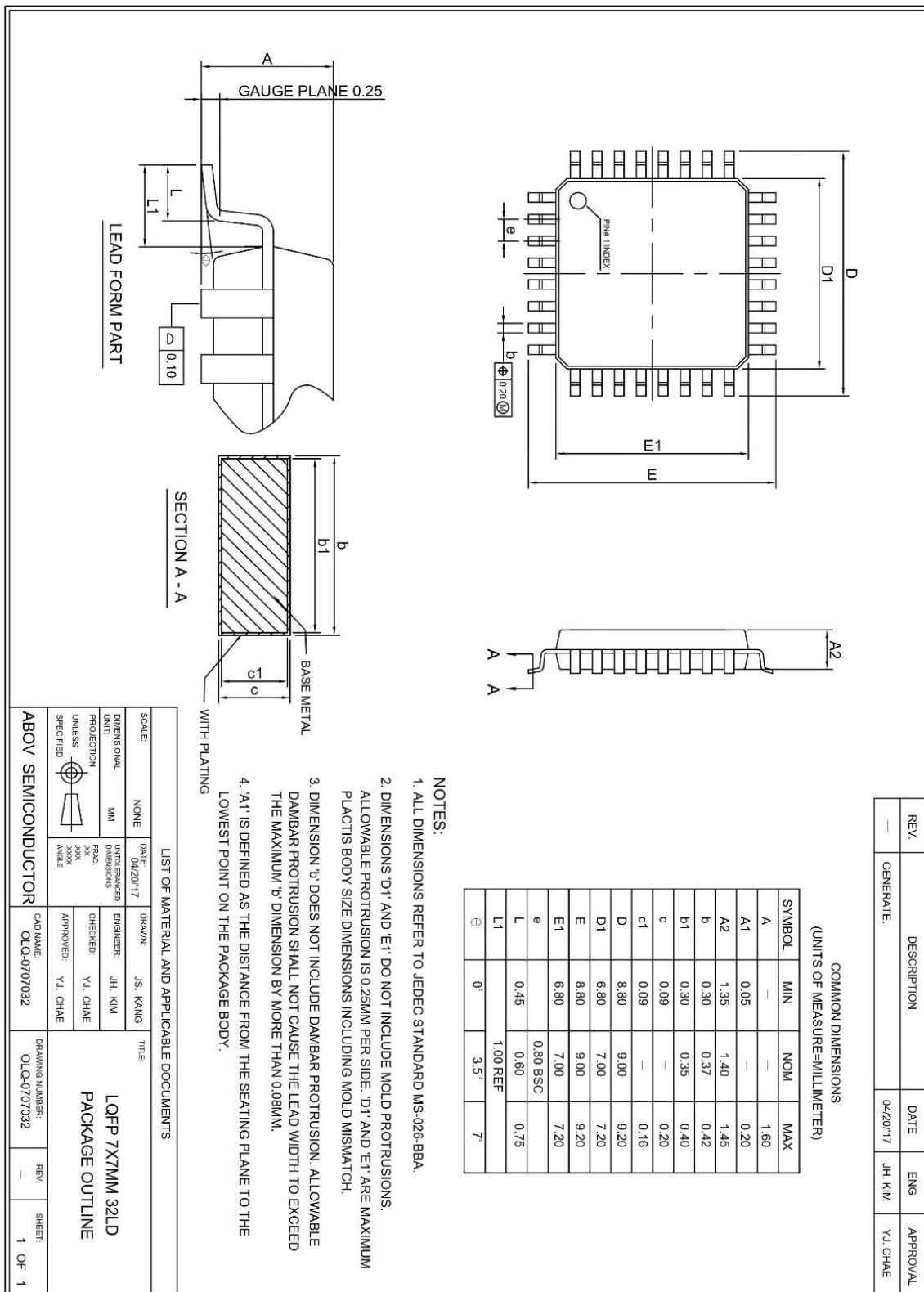
Figure 17. Package Dimension (48-LQFP)



4.2 32-LQFP Package Information

LQFP-32 is a 32-pin, 7 x 7 mm quad flat package.

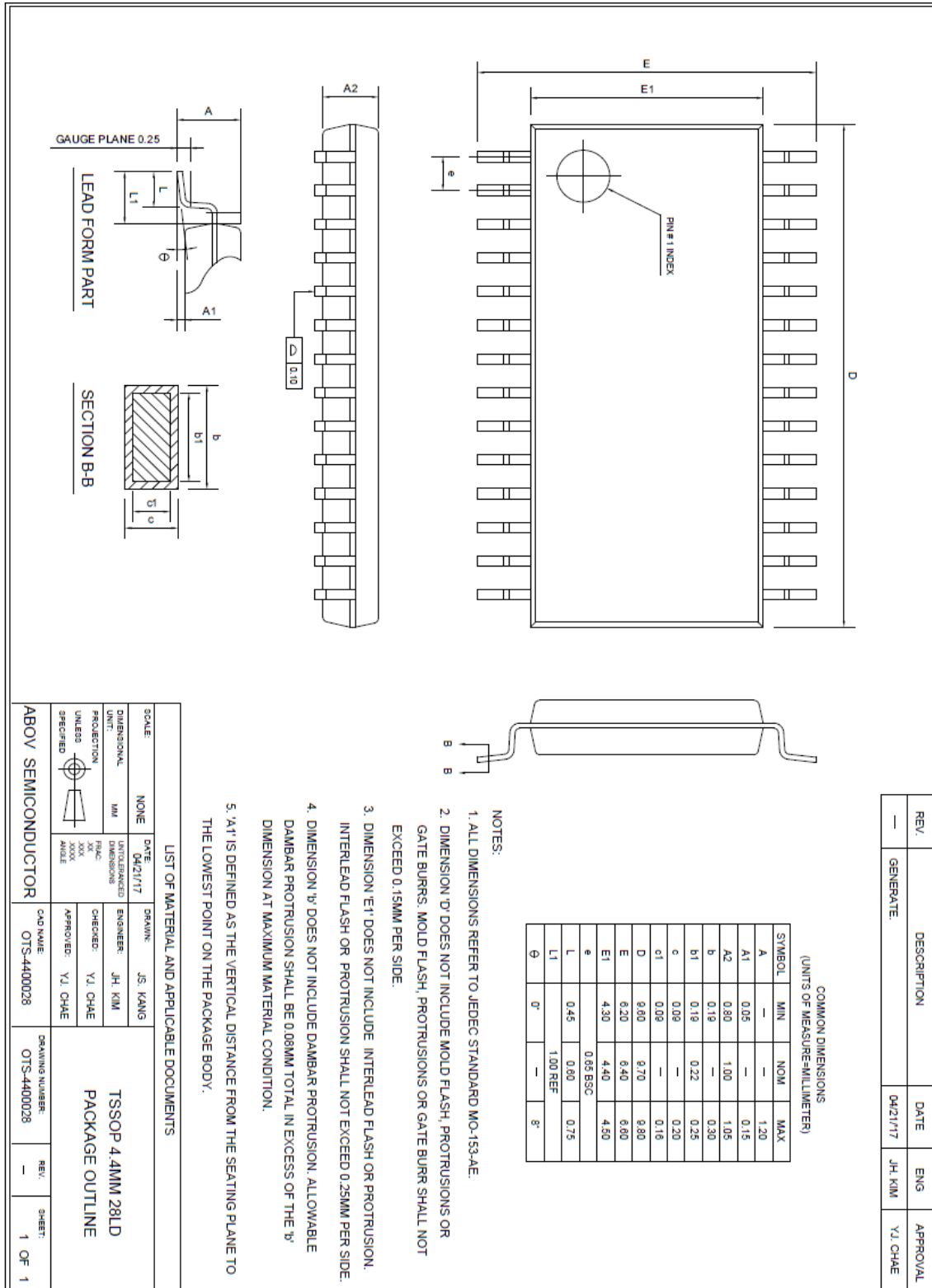
Figure 18. Package Dimension (32-LQFP)



4.3 28-TSSOP8 Package Information

TSSOP-28 is a 28-pin, 9.7 x 4.4 mm package.

Figure 19. Package Dimension (28-TSSOP)



NOTES:

1. ALL DIMENSIONS REFER TO JEDEC STANDARD MO-153-AE.
2. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURR SHALL NOT EXCEED 0.15MM PER SIDE.
3. DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25MM PER SIDE.
4. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. 'A1' IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE:	NONE	DATE:	04/21/17	DRAWN:	J.S. KANG	ENGINEER:	J.H. KIM	CHECKED:	Y.I. CHAE	APPROVED:	Y.I. CHAE	CAD NAME:	OTS-4400028	DRAWING NUMBER:	OTS-4400028	REV:	—	SHEET:	1 OF 1
DIMENSIONAL UNIT:	MM	UNITS/INCHES:		PROJECTION:	1st ANGLE	UNLESS SPECIFIED:													
TSSOP 4.4MM 28LD PACKAGE OUTLINE																			
ABOV SEMICONDUCTOR																			

5. Ordering Information

Figure 20. A31M22x Device Numbering Nomenclature

		A31M22 3 C L 2 N (T)					
Device family name							
A31M22 = Arm Cortex-M0+ based microcontroller							
Code memory size							
3	64 Kbytes						
2	32 Kbytes						
Pin count							
C	48 pins						
K	32 pins						
G	28 pins						
Package type							
L	LQFP1 (0.5 mm pin pitch)						
M	LQFP2 (0.65 mm pin pitch)						
N	LQFP3 (0.8 mm pin pitch)						
R	TSSOP (0.65 mm pin pitch)						
Temperature							
None	-40 to +85°C						
2	-40 to +105°C						
Bonding wire							
None	Au wire						
N	Pd-Cu wire						
Packing							
(T)	Tape & reel						
(W)	Wafer						
(C)	Chip carrier						

NOTE:

1. For a list of available options (memory, package, and so on) or for further information on any aspect of this device, contact the nearest ABOV sales office.

Revision History

Revision	Date	Notes
1.00	Apr. 17, 2023	Initial release
1.01	Aug. 18, 2023	Added 28-TSSOP package.
1.02	Nov. 08, 2024	Updated the disclaimer.
1.03	Sep. 25, 2025	Updated Table 26. Flash Memory Characteristics.

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