
Cortex®-M0+ based 32-bit General-Purpose Microcontroller,
48 MHz, Flash 256 KB, SRAM 32 KB, 12-bit 1 Msps ADC,
RTCC

DS Rev. 1.00

Features

Core

- Arm® Cortex®-M0+ core
- Up to 48 MHz clock speed

Memory

- 256 KB code Flash memory
 - Read protection for security
- 32 KB SRAM

Clock, Reset and Power Management

- Two main operating clocks: HCLK, PCLK
- Two system reset: cold reset, warm reset
- Low-Voltage Detection
 - Low Voltage Reset (LVR)
 - Low Voltage Indicator (LVI)
- Power management for power consumption
 - RUN, SLEEP, DEEP-SLEEP modes
- Clock monitoring function for system clock

Interrupt Management

- Nested Vectored Interrupt Controller (NVIC) with 29 interrupt sources

General-Purpose Input/Output

- Up to 50 I/O pins
- 50 mappable on external interrupt vectors
- Strength input/output

DMA Controller

- Four channels of Direct Memory Access
- 8/16/32-bit data transfers
- Conjunction with 19 internal peripherals

ADC

- One independent ADC block
- 10 analog input channels
- 7-bit prescaler
- 1 Msps conversion rate

Timer

- 16-bit timers: 6 channels
- 32-bit timers: 2 channels
- Timer operating modes
 - Timer/counter mode
 - One-shot mode
 - PWM mode
 - Capture mode
- 12-bit prescaler

Watchdog Timer

- 24-bit down-count timer
- Reset and periodic interrupts
- Four dividers selectable

Real Time Clock and Calendar

Communication Interfaces

- USART
 - Four Universal Synchronous Asynchronous Serial Receiver-Transceiver ports
- I2C
 - Three Inter-Integrated Circuit interface ports
- SPI
 - Two Serial Peripheral Interface port

CRC Calculation Unit

- CRC operating modes:
 - CRC-CCITT
 - CRC-16
 - Auto CRC/User-defined CRC
 - CRC and checksum

Operating Voltage

- 1.8 V to 5.5 V

Operating Temperature

- Commercial grade (–40°C to 85°C)

Temperature Sensor**Debug Interface**

- Serial Wire Debug (SWD) interface

Package

- 64-LQFP-1010 (0.50 mm pitch)
- 64-LQFP-1212 (0.65 mm pitch)
- 64-LQFP-1414 (0.80 mm pitch)
- 48-LQFP-0707 (0.50 mm pitch)
- 48-QFN-0606 (0.40 mm pitch)
- 32-QFN-0505 (0.50 mm pitch)

Product Selection Table**Table 1. Device Series Summary**

Base Product	Part Number	Flash	SRAM	USART	SPI	I2C	ADC	Timer	I/O Ports	Package
A31G346	A31G346RL	256 KB	32 KB	4	2	3	10	8	50	64-LQFP-1010
	A31G346RM*	256 KB	32 KB	4	2	3	10	8	50	64-LQFP-1212
	A31G346RN*	256 KB	32 KB	4	2	3	10	8	50	64-LQFP-1414
	A31G346CL*	256 KB	32 KB	4	1	3	7	8	39	48-LQFP-0707
	A31G346CU*	256 KB	32 KB	4	1	3	7	8	39	48-QFN-0606
	A31G346KU*	256 KB	32 KB	3	0	3	5	8	26	32-QFN-0505

* For available options or further information on the device with “*” marks, please contact the [ABOV sales office](#).

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1. Introduction

This document provides an overview of the features supported by the device, including high-level information and brief explanations for each feature.

Refer to Table 3 for the list of features supported by the device.

2. Description

The A31G346 is a 32-bit microcontroller based on the energy efficient Arm Cortex-M0+ core, with up to 256 KB of code Flash memory, and 32 KB of SRAM. The A31G346 operates at voltage range of 1.8 V to 5.5 V, providing a highly flexible and cost-effective solution for many embedded control applications.

The A31G346 features a variety of peripherals, including 16-bit and 32-bit timers, Real timer, and calendar, a 12-bit ADC, CRC generator, as well as USART, I2C, SPI, and DMA. In addition, this device is equipped with a POR, LVR, LVI, and an internal RC oscillator.

To further reduce power consumption, the A31G346 supports both SLEEP and DEEP-SLEEP modes.

2.1 Product Category Definition

Table 2 provides an overview of the memory capacity for the A31G346.

Table 2. A31G346 Memory Capacity

Memory Capacity		Category
Flash	RAM	
256 KB	32 KB	A31G346

2.2 Device Overview

Table 3 summarizes and lists the features specific to the device while considering the largest package.

Table 3. A31G346 Features

Item		Description
Core	CPU	• Max. operating frequency: 48 MHz • 32-bit Arm Cortex-M0+ CPU • Register settings in CPU: - General purpose register: 32-bit Thumb-2 instruction set - Main Stack Pointer (MSP) and Process Stack Pointer (PSP): R13 - Link Register (LR): R14 - Program Counter (PC): R15 • Data ordering format: Little-Endian • Von Neumann Architecture • AHB/APB
	Interrupt Controller	• NVIC (Nested-Vectored Interrupt Controller) • Up to 32 peripheral interrupts supported. • Assignable with four different priority levels
Memory	Code Flash	• Capacity: 256 KB • A high-capacity Code Flash memory built in • Max. 48 MHz Flash access speed - 0-wait: up to 20 MHz - 1-wait: up to 40 MHz - 2-wait: up to 48 MHz • Erase unit: Page (512-byte), Sector (2048-byte), Bulk (256 KB, full-chip) • Program unit: Word (4-byte) • Read protection • Self-programming • CRC code generation and verification for the Flash memory • Endurance: 10,000 cycles • Lifetime: 10 years
	Boot ROM	• It initiates the microcontroller's boot mode by receiving an external input signal at the BOOT pin. • UART boot mode • In-system programming - Users can program the internal Flash memory by using an application board to write data to the memory.
	SRAM	• Capacity: 32 KB • Usable as a program's work area • Part of the SRAM can be remapped into an interrupt vector area

Table 3. A31G346 Features (continued)

Item	Description
System Control Unit (SCU)	Operating Frequency • Up to 48 MHz
	Clock • High speed Internal oscillator (HSI) - 32 MHz ($\pm 1.5\%$ @ Ta = 0°C to +50°C) - 32 MHz ($\pm 3\%$ @ Ta = -40°C to +85°C) • Low speed Internal oscillator (LSI) - 40 kHz ($\pm 15\%$ @ Ta = -40°C to +85°C) • External Main Oscillator (HSE): 2 MHz to 16 MHz • External Sub-Oscillator (LSE): 32.768 kHz • Phase-locked loop (PLL): 48 MHz
	Clock Monitoring • System fail-safe function by clock monitoring - High frequency internal RC oscillator (HSI) - External main oscillator (HSE) - External sub oscillator (LSE) - Main system clock (MCLK)
	Operation Mode • RUN mode • SLEEP mode • DEEP-SLEEP (STOP) mode
	Reset • nRESET pin reset • Core reset • Software reset • POR (Power-On Reset) • LVR (Low-Voltage Reset) • WDTR (Watchdog Timer Reset) • MON (Clock monitoring reset)
	VDC • Low-dropout (LDO) regulator built in for low-voltage operation
	POR • The POR generator detects an internal 1.4 V and generates a reset signal
	LVI • 13 low-voltage detection levels • Supports interrupts • Supports wake-up from SLEEP mode and DEEP SLEEP modes
	Wake-up • Wake-up by an external interrupt (GPIO) pin • Wake-up by a Real Time Clock/Calendar (RTCC) • Wake-up by a Watchdog Timer (WDT) • Wake-up by a Low-Voltage Indicator (LVI) • Wake-up by a I2C • Wake-up by a USART • Wake-up by a T20

Table 3. A31G346 Features (continued)

Item		Description
	Wake-Up Timer (WUT)	• 16-bit down-count timer • Underflow interrupt • Stabilization time upon wake-up from deep sleep mode
	General-Purpose I/O (GPIO)	• Input/Output (I/O) port for general purpose • 64-LQFP-1010 - I/O pins: 50 • 64-LQFP-1212 - I/O pins: 50 • 64-LQFP-1414 - I/O pins: 50 • 48-LQFP-0707 - I/O pins: 39 • 48-QFN-0606 - I/O pins: 39 • 32-QFN-0505 - I/O pins: 26 • Each pin can be set for one of the following modes: - Push-pull output - Open drain output - Input • The use of each pin can be set by setting the register • Corresponding pin can be configured as an external interrupt source, either the level-trigger/edge-trigger interrupt or the rising-edge/ falling-edge/ both-edge interrupt • Pull-up or pull-down resistor, and debouncing can be set for each pin • Each pin bit can be individually set/reset • Wake-up events triggered by external asynchronous inputs
	Direct Memory Access (DMA) Controller	• 4-channel Direct Memory Access (DMA) supporting peripherals • 8-bit/16-bit/32-bit data transfers • Compatible with 19 different types of peripherals • SPI0, SPI1, USART10, USART11, USART12, USART13, I2C0, I2C1, I2C2, ADC

Table 3. A31G346 Features (continued)

Item		Description
General Purpose Timer	16-bit Timer	• General-purpose 16-bit up-count timer • 6 channels - Timer 1n capture port (T1nCAP) input channels - Timer 1n output port (T1nOUT) output channels • Timer operating modes - Timer/counter mode - Capture mode - PPG one-shot mode - PPG repeat mode • Interrupt events - Timer/counter match interrupt - Timer capture interrupt • Input clock selection - PCLK clock divided by prescaler is selectable - External clock is selectable • Timer signals can be generated through T1nOUT pins • 12-bit prescaler
	32-bit Timer	• General-purpose 32-bit up-count timer • 2 channels - Timer 2n capture port (T2nCAP) input channels - Timer 2n output port (T2nOUT) output channels • Timer operating modes - Timer/counter mode - Capture mode - PPG one-shot mode - PPG repeat mode • Interrupt events - Timer/counter match interrupt - Timer capture interrupt • Input clock selection - PCLK clock divided by prescaler is selectable - External clock is selectable (T20, T21) - LSE clock is selectable (T20) • Timer signals can be generated through T2nOUT pins • 12-bit prescaler
System Timer	WDT	• 24-bit down-count timer • Reset generation • Window match interrupt • Underflow interrupt • LSI or PCLK is selectable
	RTCC	• Calendar with 0.5 seconds, seconds, minutes, hours, day, week, month, and year up to 2099 • Time error correction function • Alarm function with interrupt • Wake-up possible from DEEP SLEEP mode

Table 3. A31G346 Features (continued)

Item		Description
Communication Interface	USART	• 4 channels for asynchronous, synchronous, and serial peripheral interfaces • Asynchronous/synchronous modes (UART) • 5- to 9-bit data transfers • Even/Odd/Non-parity generation and checking • 1-bit or 2-bit stop bit generation and checking • 12-bit baud rate generator • Receive time out function from start bit (Asynchronous only) • Receive character detection • Auto baud rate detection • 1-wire half-duplex communication • Local interconnection network (LIN) • Tx break transmit and Rx break detection • Serial peripheral interface (SPI) • Master/slave operation • Loop-back function • 8-bit data transmit/receive • Both least significant bit (LSB)-first and most significant bit (MSB)-first modes available
	SPI	• Two synchronous serial communication port channels • Master/slave operation • Loop-back mode • Programmable and flexible communication - 8-bit data transmit/receive - SPI clock speed - Both least significant bit (LSB)-first and most significant bit (MSB)-first modes available
	I2C	• Standard I2C communication protocol • Three channels supported • Master and slave modes supported for each channel • 7-bit addressing supported for slave mode • SCL signal's high/low periods and SDA signal's hold time settable
12-bit A/D Converter	ADC	• 10 analog input channels • Software and timer match signal triggers supported • Conversion modes and over sampling supported

Table 3. A31G346 Features (continued)

Item		Description
Cyclic Redundancy Check	CRC	• CRC operating modes: - CRC-CCITT (0x1021) - CRC-16 (0x8005) • Auto and user mode supported
Temperature Sensor	TS	• -40°C to +85°C wide range of operating temperature • A down counter at 20-bit intervals to count the frequency of the TS • A 24-bit data register to store the count value of the temperature sensor frequency
Operating Voltage		1.8 V to 5.5 V
Operating Temperature	Commercial Grade	-40°C to 85°C
Package		• Six types of package options - 64-LQFP-1010 (0.5 mm pitch) - 64-LQFP-1212 (0.65 mm pitch) - 64-LQFP-1414 (0.8 mm pitch) - 48-LQFP-0707 (0.5 mm pitch) - 48-QFN-0606 (0.4 mm pitch) - 32-QFN-0505 (0.5 mm pitch)

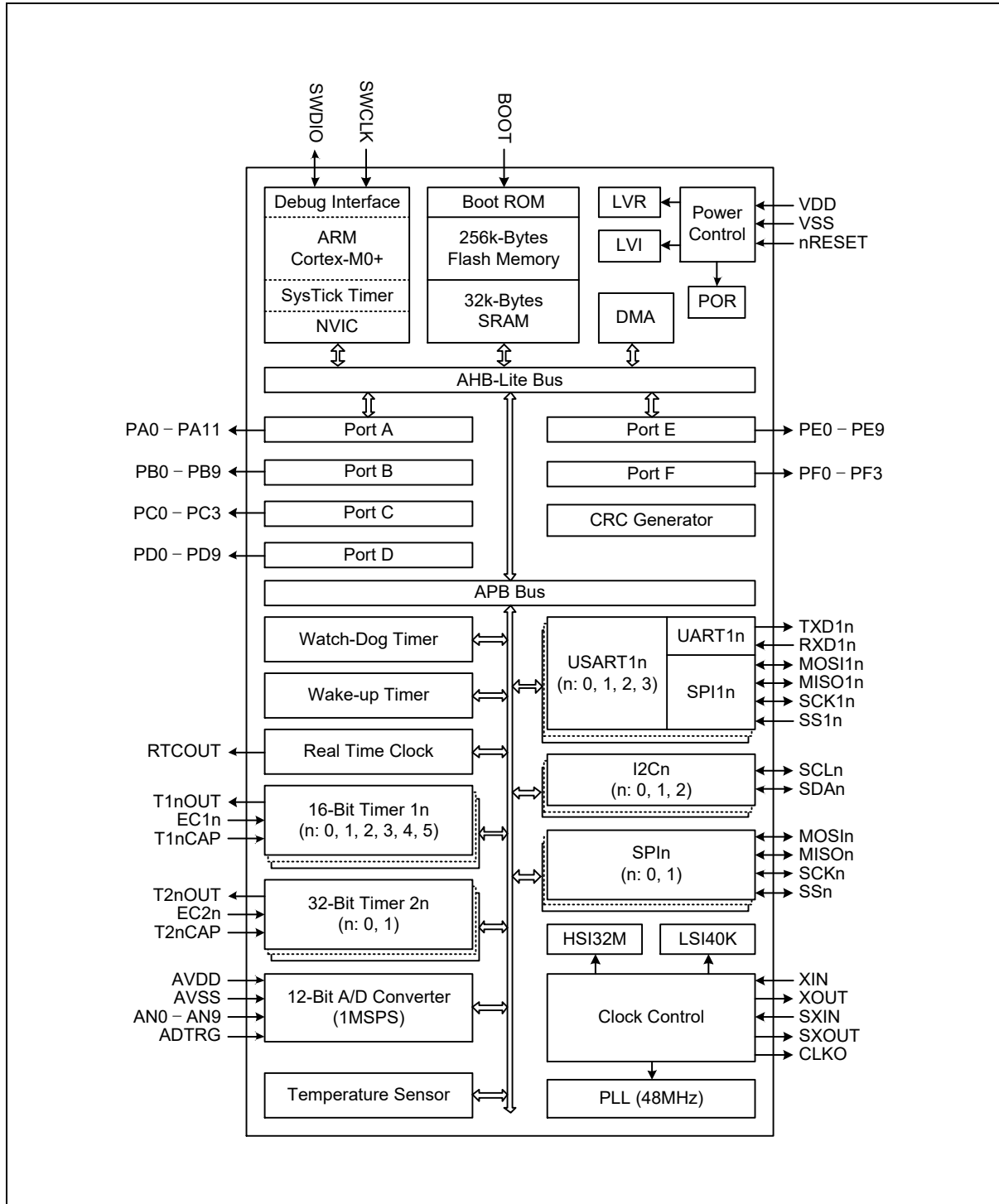
Table 4. Summary of A31G346 Peripherals

Peripheral		A31G346RL A31G346RM A31G346RN	A31G346CL	A31G346CU	A31G346KU
Code Flash Memory		256 KB	256 KB	256 KB	256 KB
SRAM		32 KB	32 KB	32 KB	32 KB
Timers	General Purpose	8	8	8	8
	SysTick	1	1	1	1
	Watchdog	1	1	1	1
	RTCC	1	1	1	1
Communication Interfaces	USART	4	4	4	3
	I2C	3	3	3	3
	SPI	2	1	1	0
Direct Memory Access (DMA)		4	4	4	4
GPIO		50	39	39	26
ADC Number of channels		1 Msps	1 Msps	1 Msps	1 Msps
		10	7	7	5
Max. Operating Frequency		48 MHz	48 MHz	48 MHz	48 MHz
CRC		1	1	1	1
Operating Voltage		1.8 V to 5.5 V			
Operating Temperature	Commercial	-40°C to 85°C			
Package		64-LQFP-1010 64-LQFP-1212 64-LQFP-1414	48LQFP-0707	48QFN-0606	32QFN-0505

2.3 Block Diagram

Figure 1 shows a block diagram of the A31G346.

Figure 1. A31G346 Block Diagram



2.4 Functional Overview

The following sections provide overviews of the features of the A31G346 microcontroller.

2.4.1 Cortex-M0+ Core

The A31G346 microcontroller uses the energy efficient Cortex-M0+ core from Arm, which is optimized for low-power consumption and features highly efficient 32-bit architecture. The Cortex-M0+ is based on the ARMv6-M Thumb instruction set and includes 16-bit instructions with Thumb-2 technology, allowing for improved performance and energy efficiency. It also includes a simple 24-bit system timer (SYSTICK) that can function as a real-time operating system or a counter. Additionally, the Cortex-M0+ features an integrated Nested Vectored Interrupt Controller (NVIC) for deterministic interrupt handling, hardware single-cycle multiplication for efficient computation, and supports SWD debugging features.

Refer to the technical reference manual **ARM DDI 0484C** for detailed information on Cortex-M0+.

2.4.2 On-Chip SRAM

The A31G346 has a block of 0-wait on-chip SRAM. The size of the SRAM is 32 KB, and its base address is 0x2000_0000. The SRAM memory area is commonly utilized for storing data and as a stack memory. Additionally, it can also be utilized for storing program code for faster execution or during Flash erasing/programming operations.

2.4.3 Boot Configuration

The A31G346 has a boot mode option to program internal Flash memory. Boot mode can be entered by setting BOOT pin to 'L' at reset timing (Normal state is 'H').

Boot mode supports the UART boot which uses the UART interface to transmit and receive boot data (TXD10/RXD10).

The pins for the boot mode are listed in Table 5.

Table 5. Boot Mode Pin List

Block	Pin Name	Pin Direction	Description
SYSTEM	nRESET	Input	Reset Input signal.
	BOOT/PD0	Input	Set the boot mode.
UART mode of USART10	RXD10/PA9	Input	Receive the UART boot data.
	TXD10/PA8	Output	Transmit the UART boot data.

2.4.4 Operating Voltage

The device operates with a supply voltage of a 1.8 V to 5.5 V (VDD).

During a power-up process, a reset plays an important role and affects the entire process of the system booting. The A31G346 has two power-related reset options as described below:

- POR_RST (Power-On Reset): Controls the voltage less than 1.4 V
- LVR_RST (Low-Voltage Reset): Controls the voltage less than 1.68 V (configuration option)

If the power level is higher than the POR and lower than the Flash operating voltage (min. 1.35 V), the Code Read operation may malfunction. To prevent this abnormal Code Read operation, the LVR_RST generates the nSYSRESET internal signal, and the microcontroller enters the reset mode to prevent the abnormal operation. To ensure stable operation, it is recommended to select a voltage level higher than the minimum level of 1.68 V that can be set by the LVR.

2.4.5 Operation Mode

2.4.5.1 Transition of Operation Mode

The INIT mode is the initial state of the chip when a reset is asserted. In RUN mode, the CPU operates at the maximum performance with the high-speed clock system. The SLEEP and DEEP-SLEEP modes are available as low-power consumption modes. During these modes, the processor core and any unused peripherals are halted to effectively manage power consumption.

2.4.5.2 RUN Mode

In RUN mode, the CPU and peripheral hardware operate with a high-speed clock. After a reset, the system will enter the RUN mode if the INIT state is detected.

2.4.5.3 SLEEP Mode

When the microcontroller enters the SLEEP mode, the CPU is halted while peripheral functions remain active. Users can determine which peripherals are active or inactive in the SLEEP mode by setting the corresponding function enable bit and clock enable bit in the SCU_PPCLKEN register.

2.4.5.4 DEEP-SLEEP Mode

In the DEEP-SLEEP mode, both the CPU and a selected system clock (MCLK) are halted to reduce power consumption. However, the Real time clock/calendar with a sub-clock and the watchdog timer with LSI can still operate in this mode.

2.4.5.5 Reset Mode

The A31G346 has two system reset types: a cold reset, which is effective during power up or down sequences, and a warm reset, which is triggered by multiple reset sources.

The reset features of the A31G346 are as follows:

- nRESET pin
- Watchdog Timer (WDT) reset
- Low-Voltage Reset (LVR)
- Monitor (MON) reset
- Software reset
- CPU request reset

2.4.6 Clocks and Startup

The A31G346 has two main operating clocks: HCLK, which generates clock signals for the CPU and AHB system, and PCLK, which generates clock signals for peripheral systems.

2.4.6.1 HCLK Clock

The Cortex-M0+ core requires two clocks: HCLK and FCLK. While the HCLK supplies the clock for both the CPU and AHB, the FCLK remains enabled unless the system enters the DEEP-SLEEP mode. Conversely, during the SLEEP mode, the HCLK can be disabled while the FCLK continues to function.

The buses and memories are clocked by the HCLK. As the bus clock frequency is limited to a maximum of 48 MHz, the HCLK frequency must not exceed 48 MHz.

2.4.6.2 PCLK Clock

The PCLK can be used as a clock source for any peripherals. The SCU_PPCLKEN registers determine whether the PCLK is enabled or disabled for each peripheral. If a peripheral block's PCLK input is not enabled, its registers cannot be read. Additionally, it is important to note that the PCLK stops operating in the DEEP-SLEEP mode.

2.4.6.3 Clock Configuration Procedure

Initially, after power on, the HSI (2 MHz) is enabled as a system clock source by default in the system operation sequence. The HSI operates as a system clock until users configure other clock sources according to their needs.

To enable the HSE and LSE clocks, users can set the HSEEN and LSEEN bits in the SCU_CLKSRCR register. However, before enabling the HSE and LSE blocks, users must first configure the pin mux settings for the XIN/XOUT and SXIN/SXOUT functions. Note that PF0/PF1 and PF2/PF3 pins are shared between these functions, and thus the PF_MOD and PF_AFSR1 registers must be configured correctly.

Once the HSE and LSE clocks are enabled, users can verify the stability of the crystal oscillation by using the clock monitoring control register, SCU_CMONCR. However, it is important to wait at least 10 ms to ensure that the crystal oscillation is stable before changing the system clock.

2.4.7 Nested Vectored Interrupt Controller (NVIC)

The A31G346 incorporates the Nested Vector Interrupt Controller (NVIC), which can manage up to 32 maskable interrupt channels with four priority levels. The NVIC in the Cortex-M0+ processor handles and prioritizes interrupts internally within the processor. Software can set the priority of each interrupt, and external interrupt signals are connected to the NVIC, which prioritizes them. The NVIC enables efficient processing of late-arriving interrupts and achieves low-latency interrupt processing. Access to all NVIC registers is only possible through word transfers.

The NVIC has the following advantages:

- Interrupt processing with reduced interrupt latency
- Direct transfer of Interrupt Vector Table (IVT) address to the core
- Fast interrupt processing capability
- Interrupts with higher priority are given precedence over those with lower priority, even if they occur after the lower-priority interrupts.
- Tail Chaining
- Automatic saving of processor state
- Interrupt restoring without instructional overhead at the end of the interrupt

The NVIC hardware block provides flexible and efficient interrupt management with minimal interrupt latency.

2.4.8 Port Control Unit (PCU)

The A31G346 has a Port Control Unit (PCU) module that controls the input and output (I/O) ports. By setting the PCU registers, users can configure the functionality, input/output direction, pull-up/pull-down, and debouncing of the pins for their applications.

2.4.9 General-Purpose Input/Output (GPIO)

Pins other than those specified as VDD, GND or certain purpose, can be used as General-Purpose Input/Output (GPIO) pins.

The GPIO module controls the general I/O pins. Output pins can be configured to output high-level or low-level signals by setting the corresponding bits of the GPIO control register. On the other hand, the input status of logic input pins can be monitored through the control registers.

2.4.10 Embedded Flash Memory

The Flash memory controller serves as an interface between the core and the embedded Flash memory and is responsible for managing the data stored on the Flash memory.

Self-programming is available and ISP and SWD programming is also supported in boot or debugging mode.

The Flash memory of the A31G346 has the following features:

- Code Flash memory for 256 KB with write protection bits
- Erase units
 - Page (512 bytes)
 - Sector (2048 bytes)
 - Bulk (256 KB, full-chip)
- Program unit:
 - Word (4 bytes)
- Code Flash read protection

2.4.11 Direct Memory Access (DMA) Controller

The Direct Memory Access (DMA) controller is used for high-speed data transfers between peripherals and memories. The DMA allows quick data transfers by copying or moving data between memory and peripherals, without involving the core.

- Four channels of direct memory access
- 8-/ 16-/ 32-bit data transfers
- Memory to peripheral transmission
- Peripheral to memory transmission
- DMA transfers are triggered by peripheral interrupts

2.4.12 16-Bit and 32-Bit Timers

The A31G346 includes six 16-bit and two 32-bit Timers that offer four operating modes: Periodic Mode, PWM Mode, One-shot Mode, and Capture Mode.

Users can select an input clock source for the 16-bit and 32-bit Timers, either a divided PCLK or an external clock. Especially for the 32-bit timer 20, LSE can be selected as an input clock source. An internal 12-bit prescaler allows to generate a variety of base clocks for the timers.

When the timer operates in Periodic Mode, interrupts can be triggered at regular intervals. In PWM Mode, users can set the period and duty to generate a PWM signal. In One-shot mode, the timer can generate one PWM waveform. In Capture Mode, the timer can measure pulse intervals of an external input signal based on the predefined conditions. In addition, the timer can transmit signals to control other devices and is primarily used as a periodic tick timer or as a wake-up source.

2.4.13 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is used to detect errors in the microcontroller caused by external interference or unexpected logical conditions. These errors cause the application program to deviate from its normal sequence. If the microcontroller loses control, the WDT will reset the microcontroller, allowing it to return to normal operation.

The WDT of the A31G346 is a 24-bit down counter. If the WDT is set as a reset source, the microcontroller restarts when the down counter reaches 0.

When it is not used to monitor the microcontroller, the WDT can be used as a cycle timer along with an interrupt.

2.4.14 Real Time Clock and Calendar (RTCC)

A real time clock and a calendar can run in SLEEP and DEEP SLEEP modes. The RTCC is not reset by a system reset except in the event of a power-on reset. The internal structure of the RTCC is implemented with the clock source select circuit, second/minute/hour/week/month/year counter circuits, alarm circuit, output select circuit, and error correction circuit.

The RTCC is an independent BCD counter. The main operations of the RTCC include the following:

- Calendar counting 0.5 seconds, seconds, minutes, hours, days, weeks, months, and years up to 2099
- Time error correction function
- Alarm function with interrupt
- Wake-up possibility from DEEP SLEEP mode

2.4.15 Universal Synchronous and Asynchronous Receiver Transmitter (USART)

The A31G346 has a four-channel USART module. The USART module supports UART and SPI modes and features as follows:

- Full duplex operation with independent serial receive and transmit registers
- Asynchronous or synchronous communication
- Baud rate generator
- Supports serial frames with 5- to 9-bit data transfer length and 1 or 2 stop bits generation and checking
- Even/Odd/Non-parity generation and checking-
- Receive character detection and receive time-out function
- Local Interconnection Network (LIN)
- Data over-run detection
- Framing error detection
- Supports three types of interrupts: TX completion, TX data register empty and RX completion
- Double speed asynchronous communication mode
- Up to 8 MHz data transfer in SPI mode

2.4.16 Serial Peripheral Interface (SPI)

The A31G346 has two built-in Serial Peripheral Interface (SPI) modules, which are clock-synchronized, and allow for customizable transmission clock specifications.

The SPI modules facilitate communications between one master and multiple slaves, which can be chosen using the Slave Select (SS) signal. Using four signal terminals (SS, SCK, MOSI, and MISO), the SPI module enables three or four-wire synchronous transfers. Its Transmit and Receive Buffers are separate, which enables full-duplex communication and simultaneous reading and writing of data.

2.4.17 Inter-Integrated Circuit (I2C) Interface

The Inter-Integrated Circuit (I2C) interface built in the A31G346 is compliant with the standard I2C communication protocol. It is used for serial communication between internal and external devices via the I2C protocol.

The built-in I2C interface, equipped with three units, supports both master and slave modes and is capable of transmitting and receiving data in bytes by using interrupts or polling.

The I2C of the A31G346 operates in Standard mode (100 kHz), Fast mode (400 kHz), or Fast Plus mode (1 MHz). In addition, it also supports General call.

The I2C interface facilitates communication with multiple peripherals that share the same bus type. To utilize I2C, it is recommended to configure the SCL and SDA pins as open-drain and attach external pull-up resistors to ensure that their output signals are maintained in a high-level.

Table 6. Features of I2Cn (n = 0 to 2)

I2C Features	I2C0	I2C1	I2C2
7-bit addressing mode	O	O	O
Standard mode (up to 100 kbit/s)	O	O	O
Fast mode (up to 400 kbit/s)	O	O	O
Fast Plus mode (up to 1,000 kbit/s)	O	O	O
General call	O	O	O

2.4.18 Analog-to-Digital Converter (ADC)

The A31G346 is equipped with a 12-bit Analog-to-Digital Converter (ADC) module that supports up to 10 analog inputs. It can convert analog signals to digital signals at a conversion rate of up to 1 Msps. 13-channel analog MUX provides various combinations of data from external and internal analog signals. The A/D module supports single, sequential, and continuous conversion modes.

2.4.19 Cyclic Redundancy Check (CRC) Calculation Module

The A31G346 has a built-in Cyclic Redundancy Check (CRC) module capable of computing 16-bit CRC codes from data streams and Flash memories. CRC-based techniques are commonly used to ensure the integrity of data transmission or storage and can also be used to verify the integrity of Flash memory in compliance with functional safety standards. By computing a signature of the software during runtime and comparing it with a reference signature, the CRC module can help detect any changes made to the software.

The CRC module in the A31G346 offers the following features:

- Auto CRC and user CRC mode
- Supports CRC-CCITT ($G1(x) = x^{16} + x^{12} + x^5 + 1$)
- Supports CRC-16 ($G2(x) = x^{16} + x^{15} + x^2 + 1$)
- CRC and checksum mode
- CRC/checksum start address auto increment (user mode only)

2.4.20 Temperature Sensor (TS)

The temperature sensor consists of a ring-oscillator. Its frequency varies with temperature. It can be used to measure the junction temperature of the device.

2.5 Development Tools

In this chapter, various development tools for the A31G346 are described. ABOV provides software tools, debuggers, and programmers to assist users in achieving the desired results for their target applications. ABOV supports the complete development ecosystem for our customers.

2.5.1 Compiler

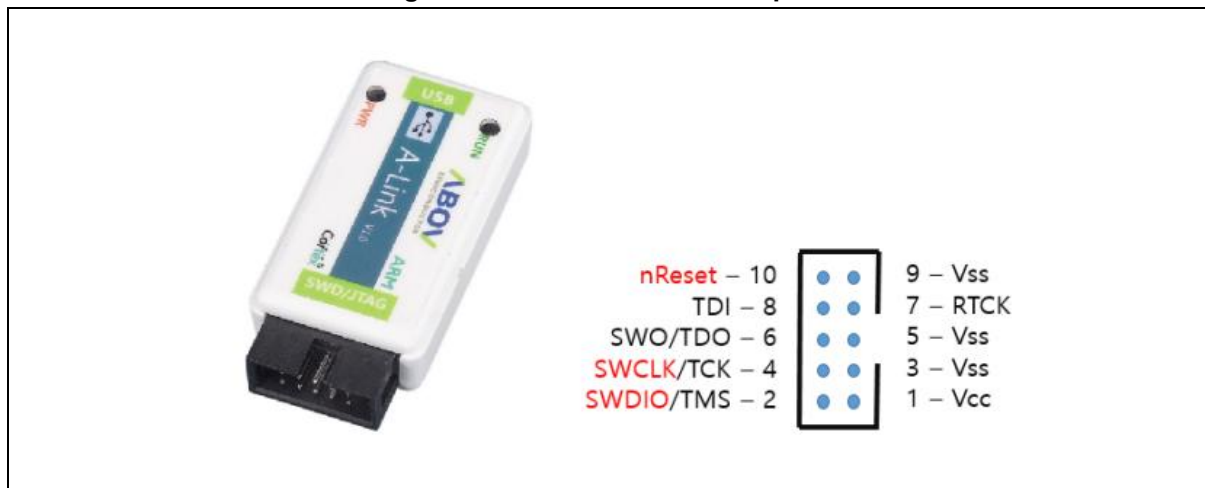
Since the A31G346 has the Arm Cortex-M0+ core, any third-party compiler, such as Keil, IAR and GCC cross-C compiler supporting Cortex-M0+, is available.

2.5.2 Debugger

A-Link and A-Link Pro can be used to emulate the A31G346 microcontroller using the SWD interface and have a two-wire interface to connect to the microcontroller on the user system. A-Link and A-Link Pro provide extensive debugging capabilities for the microcontroller, including the ability to read or write the value of the microcontroller's internal memory and I/O peripherals, as well as control its internal debugging logic. A-Link and A-Link Pro are debug interfaces with third-party compilers, providing an excellent combination of debugging environments.

The figure below shows the pinout for programming with the A-Link and A-Link Pro. For more detailed information about the A-Link and A-Link Pro, please visit www.abovsemi.com and download related software and documents.

Figure 2. A-Link and Pin Description



2.5.3 Programmer

2.5.3.1 E-PGM+ and E-PGM Serial

E-PGM+ and E-PGM Serial are standalone programmers, which allow users to program directly on the device.

- Supports for all ABOV microcontrollers
- Dedicated tool for mass production
- 40-pin Textool DIP socket for single chip programming (E-PGM+ only)
- 10-pin connector for ISP mode
- USB host interface
- HEX downloads and controls

2.5.3.2 Gang Programmer

E-Gang4 and E-Gang6 can program multiple devices simultaneously and operate in host-controlled and standalone modes without requiring a host computer connection. These programmers feature a USB interface for easy connection to a handler.

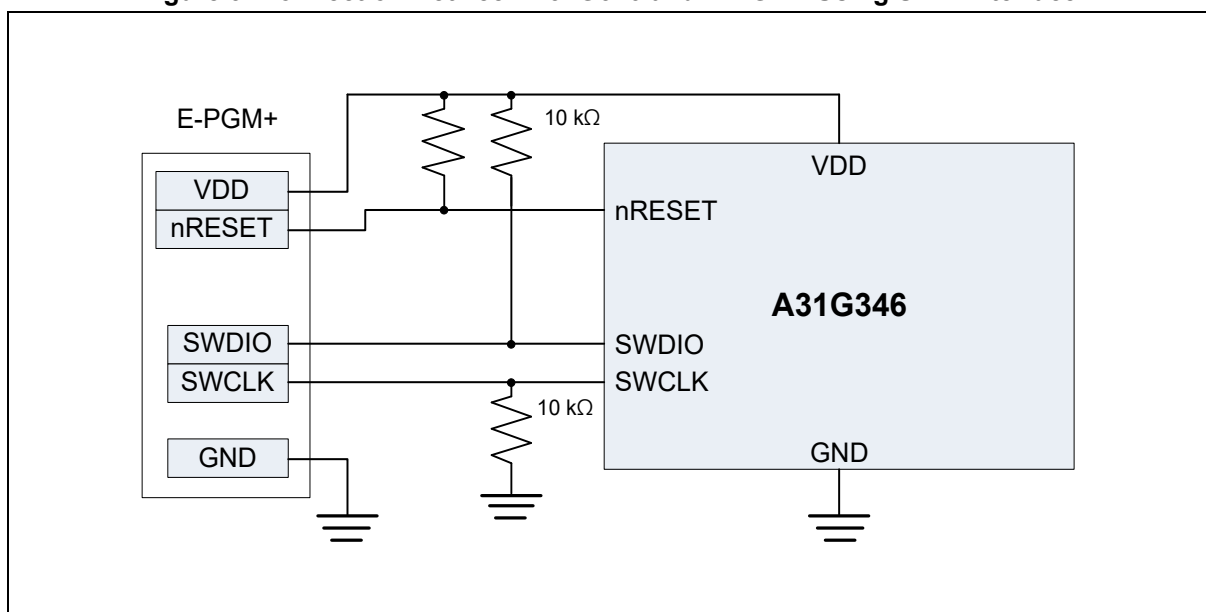
NOTE:

1. Visit the [ABOV homepage](#) and refer to the "Tools & Support > Programmer" menu.

2.5.3.3 SWD Mode and E-PGM+ Connections

The connection between the A31G346 and E-PGM+ using the SWD interface is illustrated in Figure 3.

Figure 3. Connection Between A31G346 and E-PGM+ Using SWD Interface



3. Pinouts and Pin Descriptions

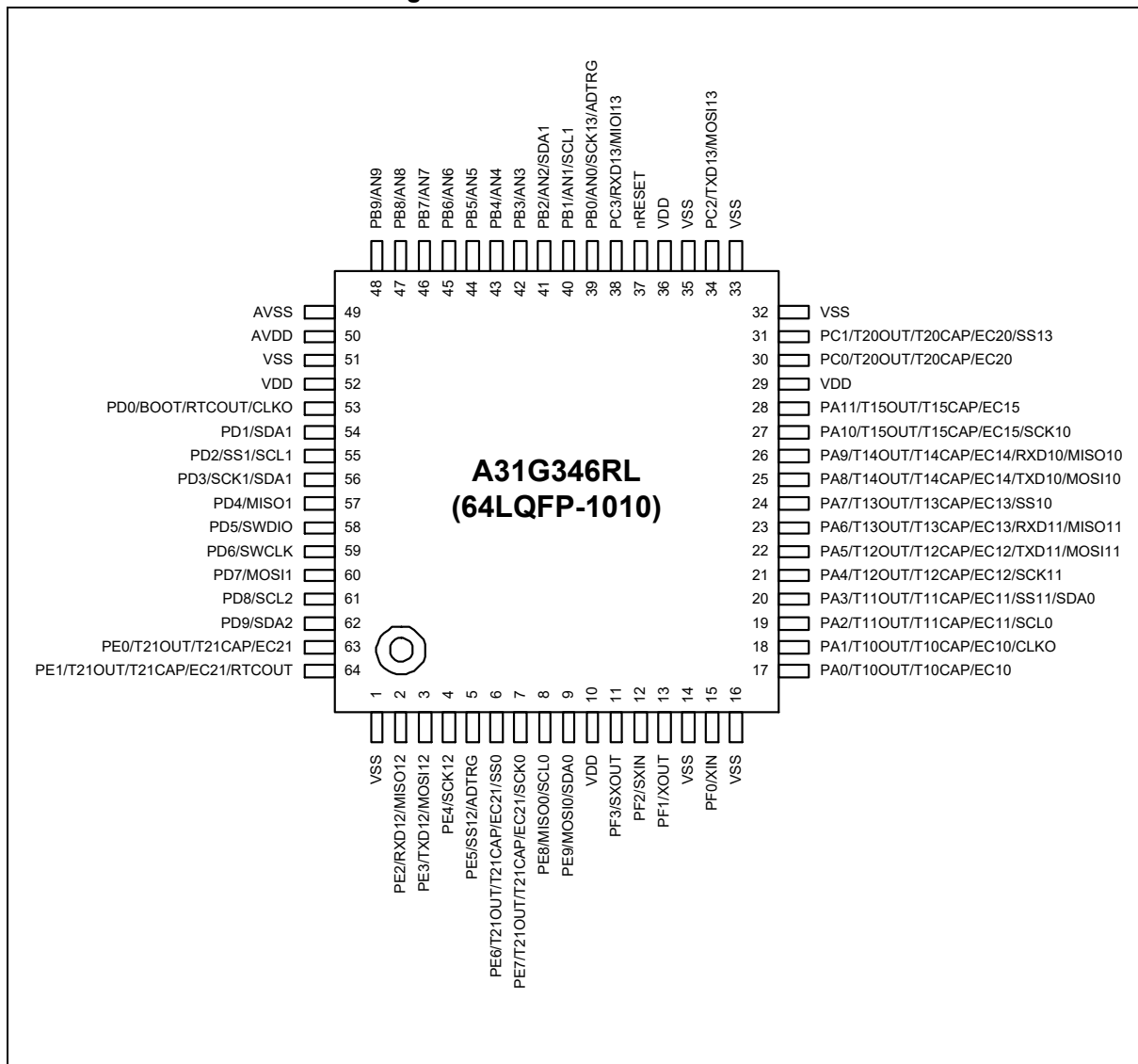
In this chapter, pinouts, and pin descriptions of the A31G346 are described.

3.1 Pinouts

Figure 4, Figure 5, Figure 6, Figure 7, Figure 8, and Figure 9 show the top view of the packages.

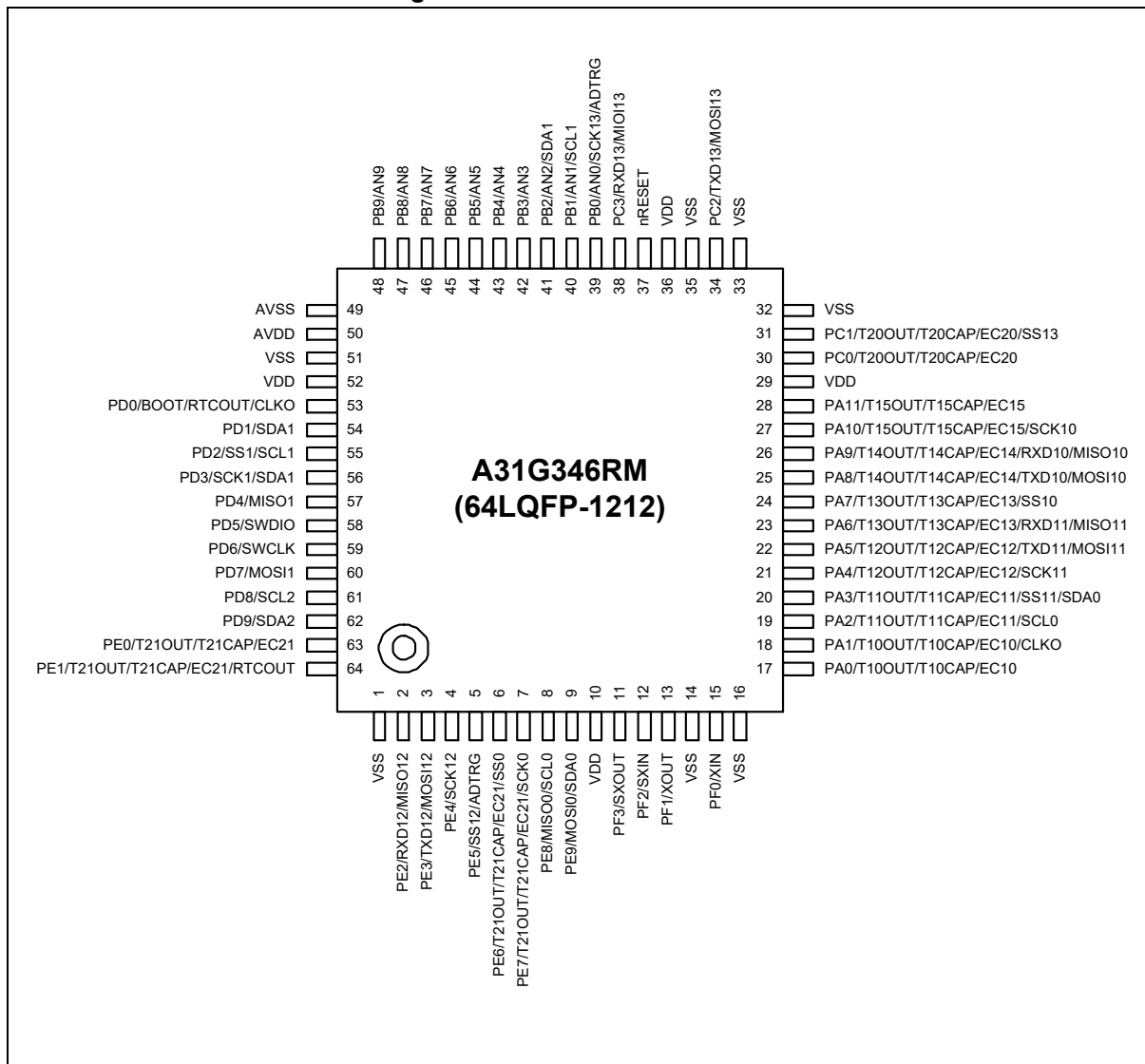
3.1.1 A31G346RL (64-LQFP-1010)

Figure 4. 64-LQFP-1010 Pinouts



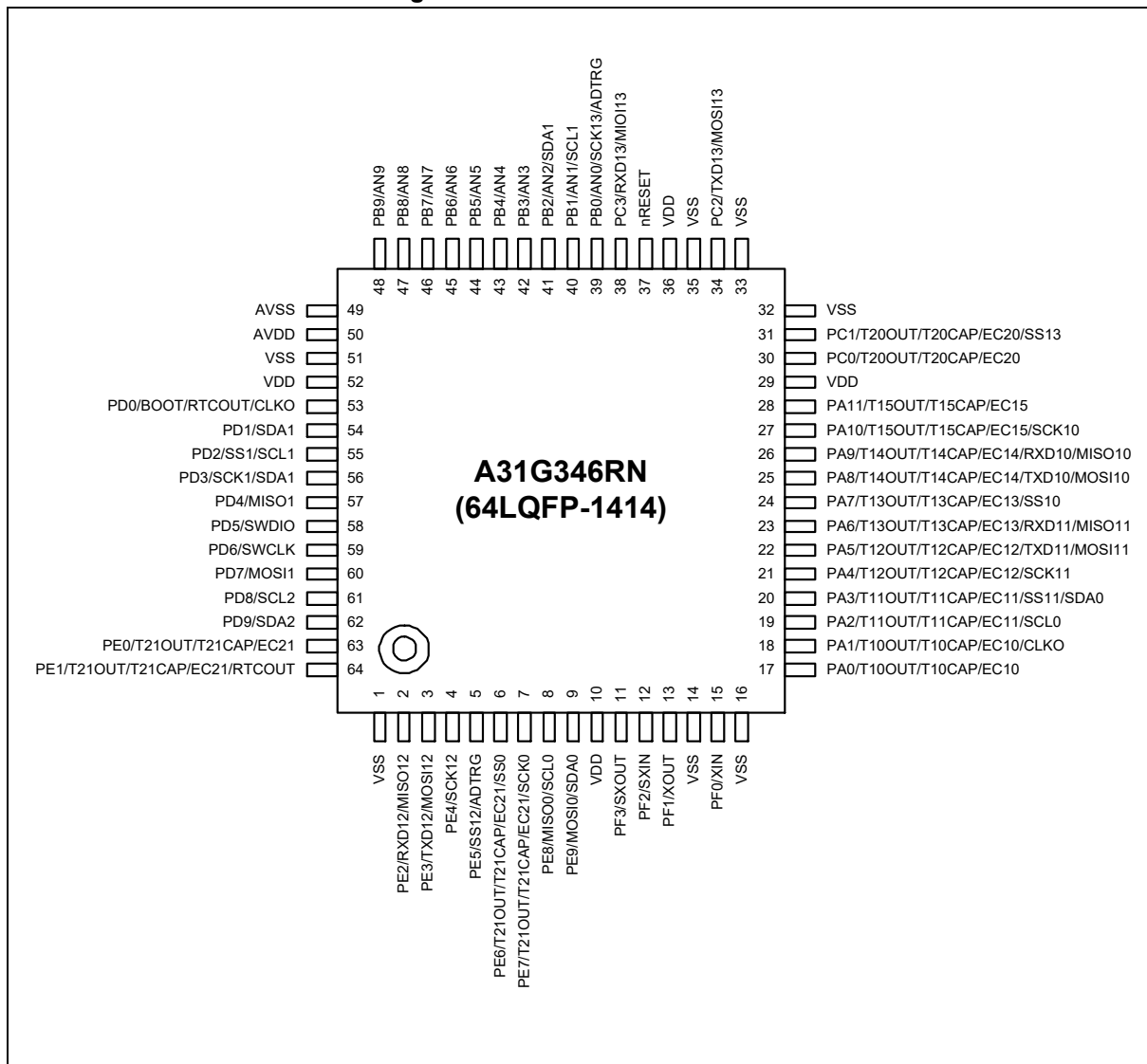
3.1.2 A31G346RM (64-LQFP-1212)

Figure 5. 64-LQFP-1212 Pinouts



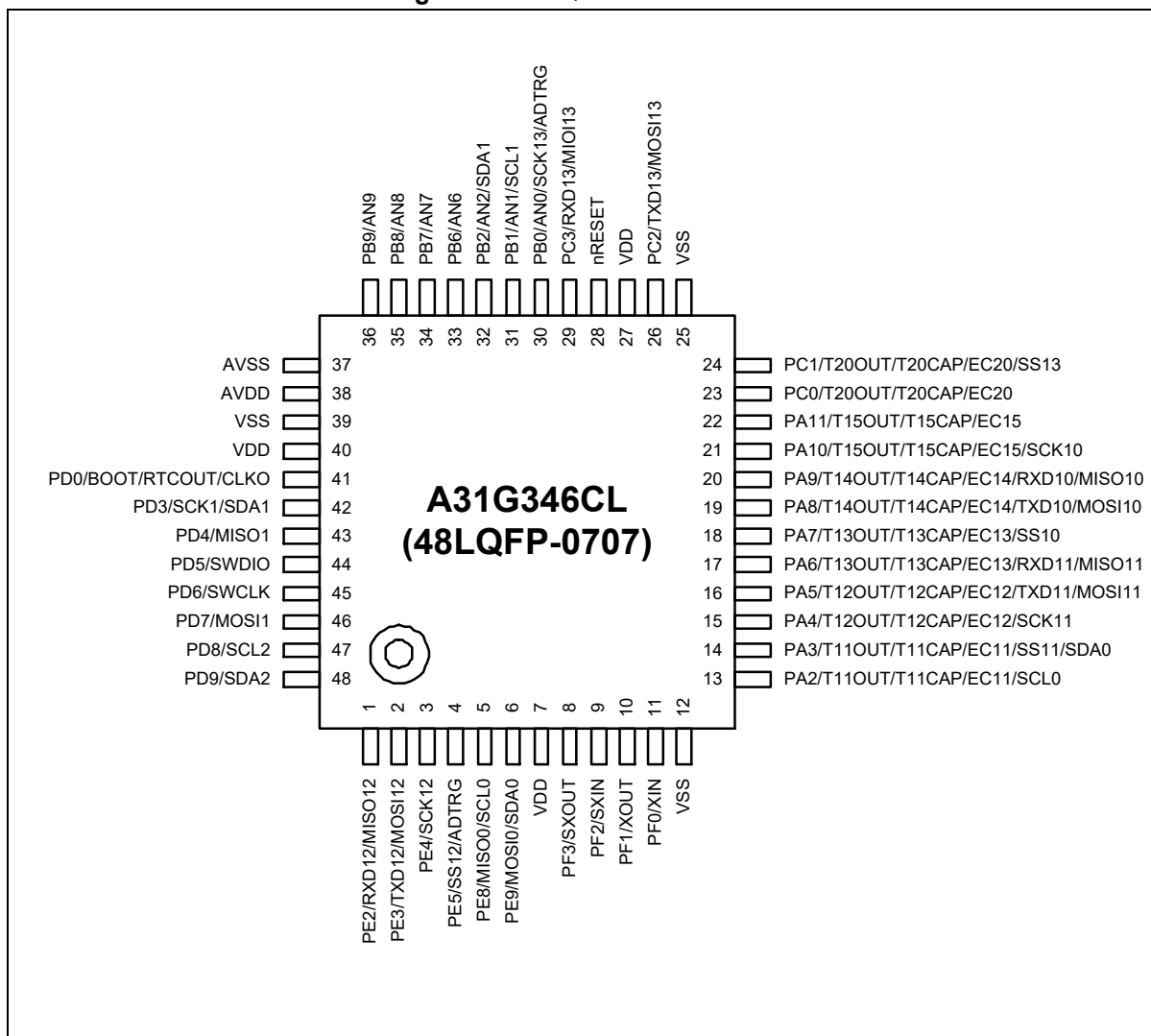
3.1.3 A31G346RN (64-LQFP-1414)

Figure 6. 64-LQFP-1414 Pinouts



3.1.4 A31G346CL (48-LQFP-0707)

Figure 7. 48-LQFP-0707 Pinouts

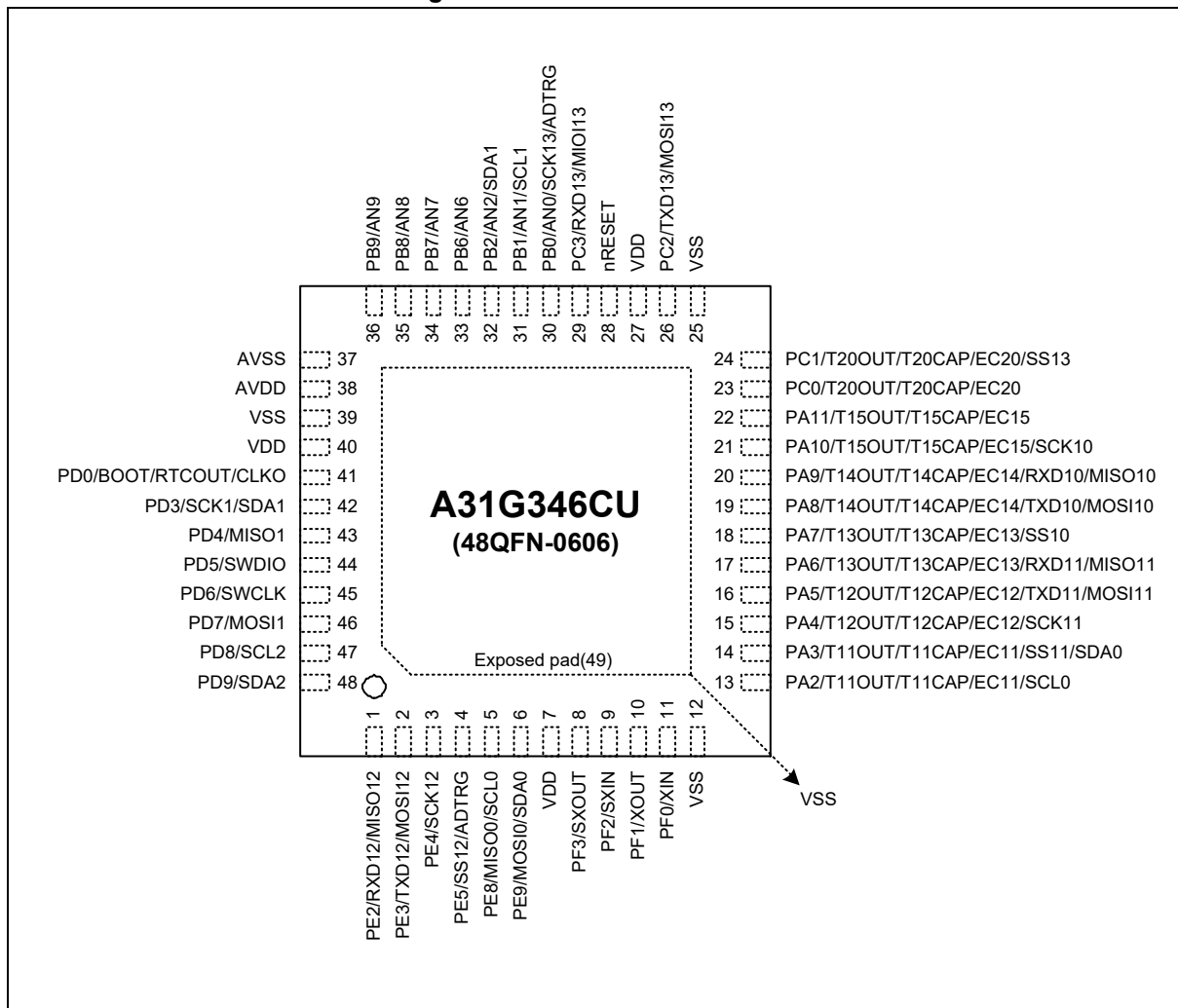


NOTE:

1. When using the 48-LQFP package, each of the PA[1:0], PB[5:3], PD[2:1], and PE[7:6, 1:0] pins should be configured as either a push-pull output or an input with a pull-up or pull-down resistor by software control using the appropriate registers or configuration settings.

3.1.5 A31G346CU (48-QFN-0606)

Figure 8. 48-QFN-0606 Pinouts

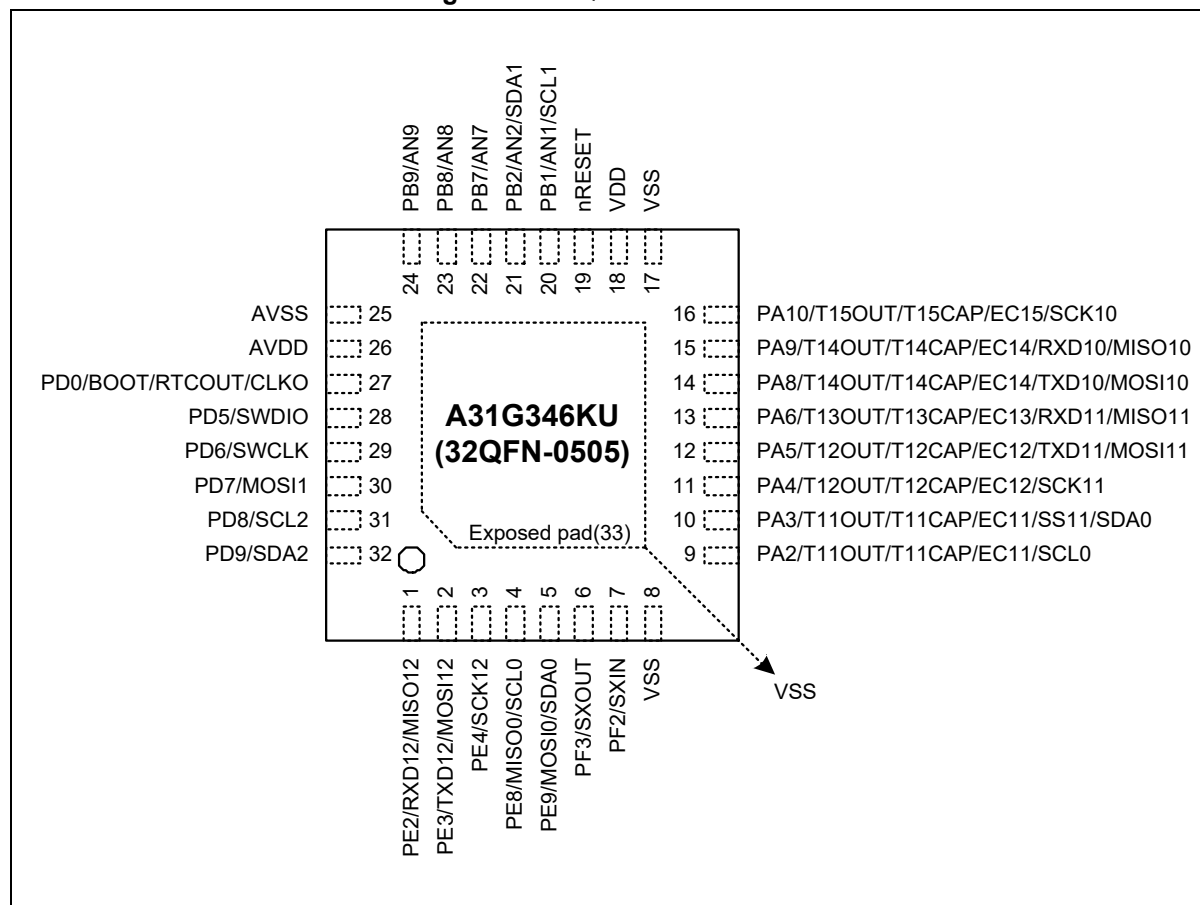


NOTE:

1. When using the 48-QFN package, each of the PA[1:0], PB[5:3], PD[2:1], and PE[7:6, 1:0] pins should be configured as either a push-pull output or an input with a pull-up or pull-down resistor by software control using the appropriate registers or configuration settings.

3.1.6 A31G346KU (32-QFN-0505)

Figure 9. 32-QFN-0505 Pinouts



NOTE:

1. When using the 32-QFN package, each of the PA[11, 7, 1:0], PB[6:3, 0], PC[3:0], PD[4:1], PE[7:5, 1:0], and PF[1:0] pins should be configured as either a push-pull output or an input with a pull-up or pull-down resistor by software control using the appropriate registers or configuration settings.

3.2 Pin Description

Table 7. Legend and Abbreviation Used in Pin Description

Name	Abbreviation	Definition
Pin name	The pin name remains constant.	
Pin type	I	Input
	O	Output
	I/O	Input/Output
	U	Pull-up
	D	Pull-down
	S	Schmitt-Trigger input
	C	CMOS input
	A	Analog
	P	Power

Pin configuration information in Table 8 contains two pairs of power/ground and other dedicated pins. These multi-function pins have up to eight selections of functions including GPIO.

Table 8. Pin Description

Pin Number			Pin Name	Type	Description	Remark
64-Pin	48-Pin	32-Pin				
1			VSS	P	Ground	
2	1	1	PE2 ⁽¹⁾	IOUDS	Port E bit 2 input/output	
			RXD12	I	UART data input	
			MISO12	IO	SPI master in slave out	
3	2	2	PE3 ⁽¹⁾	IOUDS	Port E bit 3 input/output	
			TXD12	O	UART data output	
			MOSI12	IO	SPI master out slave in	
4	3	3	PE4 ⁽¹⁾	IOUDS	Port E bit 4 input/output	
			SCK12	IO	SPI clock input/output	
5	4		PE5 ⁽¹⁾	IOUDS	Port E bit 5 input/output	
			SS12	I	SPI slave select input	
			ADTRG	I	ADC trigger input	
6			PE6 ⁽¹⁾	IOUDS	Port E bit 6 input/output	
			T21OUT	O	Timer 21 pulse output	
			T21CAP	I	Timer 21 capture input	
			EC21	I	Timer 21 event count input	
			SS0	I	SPI slave select input	
7			PE7 ⁽¹⁾	IOUDS	Port E bit 7 input/output	
			T21OUT	O	Timer 21 pulse output	
			T21CAP	I	Timer 21 capture input	
			EC21	I	Timer 21 event count input	
			SCK0	IO	SPI clock input/output	
8	5	4	PE8 ⁽¹⁾	IOUDS	Port E bit 8 input/output	
			MISO0	IO	SPI master in slave out	
			SCL0	IO	I2C clock input/output	
9	6	5	PE9 ⁽¹⁾	IOUDS	Port E bit 9 input/output	
			MOSI0	IO	SPI master out slave in	
			SDA0	IO	I2C data input/output	
10	7		VDD	P	VDD	
11	8	6	PF3 ⁽¹⁾	IOUDS	Port F bit 3 input/output	
			SXOUT	OA	Sub-oscillator output	
12	9	7	PF2 ⁽¹⁾	IOUDS	Port F bit 2 input/output	
			SXIN	IA	Sub-oscillator input	
13	10		PF1 ⁽¹⁾	IOUDS	Port F bit 1 input/output	
			XOUT	OA	Main oscillator output	
14			VSS	P	Ground	
15	11		PF0 ⁽¹⁾	IOUDS	Port F bit 0 input/output	
			XIN	IA	Main oscillator input	
16	12	8	VSS	P	Ground	

Table 8. Pin Description (continued)

Pin Number			Pin Name	Type	Description	Remark
64-pin	48-pin	32-pin				
17			PA0 ⁽¹⁾	IOUDS	Port A bit 0 input/output	
			T10OUT	O	Timer 10 pulse output	
			T10CAP	I	Timer 10 capture input	
			EC10	I	Timer 10 event count input	
18			PA1 ⁽¹⁾	IOUDS	Port A bit 1 input/output	
			T10OUT	O	Timer 10 pulse output	
			T10CAP	I	Timer 10 capture input	
			EC10	I	Timer 10 event count input	
			CLKO	O	System clock output	
19	13	9	PA2 ⁽¹⁾	IOUDS	Port A bit 2 input/output	
			T11OUT	O	Timer 11 pulse output	
			T11CAP	I	Timer 11 capture input	
			EC11	I	Timer 11 event count input	
			SCL0	IO	I2C clock input/output	
20	14	10	PA3 ⁽¹⁾	IOUDS	Port A bit 3 input/output	
			T11OUT	O	Timer 11 pulse output	
			T11CAP	I	Timer 11 capture input	
			EC11	I	Timer 11 event count input	
			SS11	I	SPI slave select input	
			SDA0	IO	I2C data input/output	
21	15	11	PA4 ⁽¹⁾	IOUDS	Port A bit 4 input/output	
			T12OUT	O	Timer 12 pulse output	
			T12CAP	I	Timer 12 capture input	
			EC12	I	Timer 12 event count input	
			SCK11	IO	SPI clock input/output	
22	16	12	PA5 ⁽¹⁾	IOUDS	Port A bit 5 input/output	
			T12OUT	O	Timer 12 pulse output	
			T12CAP	I	Timer 12 capture input	
			EC12	I	Timer 12 event count input	
			TXD11	O	UART data output	
			MOSI11	IO	SPI master out slave in	
23	17	13	PA6 ⁽¹⁾	IOUDS	Port A bit 6 input/output	
			T13OUT	O	Timer 13 pulse output	
			T13CAP	I	Timer 13 capture input	
			EC13	I	Timer 13 event count input	
			RXD11	I	UART data input	
			MISO11	IO	SPI master in slave out	
24	18		PA7 ⁽¹⁾	IOUDS	Port A bit 7 input/output	
			T13OUT	O	Timer 13 pulse output	
			T13CAP	I	Timer 13 capture input	
			EC13	I	Timer 13 event count input	
			SS10	I	SPI slave select input	

Table 8. Pin Description (continued)

Pin Number			Pin Name	Type	Description	Remark
64-pin	48-pin	32-pin				
25	19	14	PA8 ⁽¹⁾	IOUDS	Port A bit 8 input/output	
			T14OUT	O	Timer 14 pulse output	
			T14CAP	I	Timer 14 capture input	
			EC14	I	Timer 14 event count input	
			TXD10	O	UART data output	
			MOSI10	IO	SPI master out slave in	
26	20	15	PA9 ⁽¹⁾	IOUDS	Port A bit 9 input/output	
			T14OUT	O	Timer 14 pulse output	
			T14CAP	I	Timer 14 capture input	
			EC14	I	Timer 14 event count input	
			RXD10	I	UART data input	
			MISO10	IO	SPI master in slave out	
27	21	16	PA10 ⁽¹⁾	IOUDS	Port A bit 10 input/output	
			T15OUT	O	Timer 15 pulse output	
			T15CAP	I	Timer 15 capture input	
			EC15	I	Timer 15 event count input	
			SCK10	IO	SPI clock input/output	
28	22		PA11 ⁽¹⁾	IOUDS	Port A bit 11 input/output	
			T15OUT	O	Timer 15 pulse output	
			T15CAP	I	Timer 15 capture input	
			EC15	I	Timer 15 event count input	
29			VDD	P	VDD	
30	23		PC0 ⁽¹⁾	IOUDS	Port C bit 0 input/output	
			T20OUT	O	Timer 20 pulse output	
			T20CAP	I	Timer 20 capture input	
			EC20	I	Timer 20 event count input	
31	24		PC1 ⁽¹⁾	IOUDS	Port C bit 1 input/output	
			T20OUT	O	Timer 20 pulse output	
			T20CAP	I	Timer 20 capture input	
			EC20	I	Timer 20 event count input	
			SS13	I	SPI slave select input	
32			VSS	P	Ground	
33	25	17	VSS	P	VDD	
34	26		PC2 ⁽¹⁾	IOUDS	Port C bit 2 input/output	
			TXD13	O	UART data output	
			MOSI13	IO	SPI master out slave in	
35			VSS	P	Ground	
36	27	18	VDD	P	VDD	
37	28	19	nRESET	IU	External reset input	Always pull-up
38	29		PC3 ⁽¹⁾	IOUDS	Port C bit 3 input/output	
			RXD13	I	UART data input	
			MISO13	IO	SPI master in slave out	

Table 8. Pin Description (continued)

Pin Number			Pin Name	Type	Description	Remark
64-pin	48-pin	32-pin				
39	30		PB0 ⁽¹⁾	IOUDS	Port B bit 0 input/output	
			AN0	IA	A/D converter analog input channel	
			SCK13	IO	SPI clock input/output	
			ADTRG	I	ADC trigger input	
40	31	20	PB1 ⁽¹⁾	IOUDS	Port B bit 1 input/output	
			AN1	IA	A/D converter analog input channel	
			SCL1	IO	I2C clock input/output	
41	32	21	PB2 ⁽¹⁾	IOUDS	Port B bit 2 input/output	
			AN2	IA	A/D converter analog input channel	
			SDA1	IO	I2C data input/output	
42			PB3 ⁽¹⁾	IOUDS	Port B bit 3 input/output	
			AN3	IA	A/D converter analog input channel	
43			PB4 ⁽¹⁾	IOUDS	Port B bit 4 input/output	
			AN4	IA	A/D converter analog input channel	
44			PB5 ⁽¹⁾	IOUDS	Port B bit 5 input/output	
			AN5	IA	A/D converter analog input channel	
45	33		PB6 ⁽¹⁾	IOUDS	Port B bit 6 input/output	
			AN6	IA	A/D converter analog input channel	
46	34	22	PB7 ⁽¹⁾	IOUDS	Port B bit 7 input/output	
			AN7	IA	A/D converter analog input channel	
47	35	23	PB8 ⁽¹⁾	IOUDS	Port B bit 8 input/output	
			AN8	IA	A/D converter analog input channel	
48	36	24	PB9 ⁽¹⁾	IOUDS	Port B bit 9 input/output	
			AN9	IA	A/D converter analog input channel	
49	37	25	AVSS	AP	Analog ground	
50	38	26	AVDD	AP	AVDD	
51	39		VSS	P	Ground	
52	40		VDD	P	VDD	
53	41	27	PD0	IOUDS	Port D bit 0 input/output	
			BOOT ⁽¹⁾⁽⁵⁾	IU	Boot mode input	Pull-up when reset
			RTCOUT	O	Real time clock output	
			CLKO	O	System clock output	
54			PD1 ⁽¹⁾	IOUDS	Port D bit 1 input/output	
			SDA1	IO	I2C data input/output	
55			PD2 ⁽¹⁾	IOUDS	Port D bit 2 input/output	
			SS1	I	SPI slave select input	
			SCL1	IO	I2C clock input/output	
56	42		PD3 ⁽¹⁾	IOUDS	Port D bit 3 input/output	
			SCK1	IO	SPI clock input/output	
			SDA1	IO	I2C data input/output	

Table 8. Pin Description (continued)

Pin Number			Pin Name	Type	Description	Remark
64-pin	48-pin	32-pin				
57	43		PD4 ⁽¹⁾	IOUDS	Port D bit 4 input/output	
			MISO1	IO	SPI master in slave out	
58	44	28	PD5	IOUDS	Port D bit 5 input/output	
			SWDIO ⁽¹⁾⁽³⁾⁽⁴⁾	IO	SWD data input/output	Pull-up when reset
59	45	29	PD6	IOUDS	Port D bit 6 input/output	
			SWCLK ⁽¹⁾⁽³⁾⁽⁴⁾	I	SWD clock input	Pull-down when reset
60	46	30	PD7 ⁽¹⁾	IOUDS	Port D bit 7 input/output	
			MOSI1	IO	SPI master out slave in	
61	47	31	PD8 ⁽¹⁾	IOUDS	Port D bit 8 input/output	
			SCL2	IO	I2C clock input/output	
62	48	32	PD9 ⁽¹⁾	IOUDS	Port D bit 9 input/output	
			SDA2	IO	I2C data input/output	
63			PE0 ⁽¹⁾	IOUDS	Port E bit 0 input/output	
			T21OUT	O	Timer 21 pulse output	
			T21CAP	I	Timer 21 capture input	
			EC21	I	Timer 21 event count input	
64			PE1 ⁽¹⁾	IOUDS	Port E bit 1 input/output	
			T21OUT	O	Timer 21 pulse output	
			T21CAP	I	Timer 21 capture input	
			EC21	I	Timer 21 event count input	
			RTCOUT	O	Real time clock output	

NOTES:

1. After a reset, all the pins are configured to function defined by their initial values. The initial value of the pin depends on the reset value. This configuration is in compliance with the 64-pin standard.
2. Do not configure unused pins as floating inputs.
3. After a reset, the alternate functions of the PD5 and PD6 pins are set as SWDIO and SWCLK, respectively, and the internal pull-down on SWCLK and the internal pull-up on SWDIO are enabled.
4. The SWCLK and SWDIO pins should not be switched to other functions while they are being used.
5. After reset, the PD0 pin is configured as BOOT alternate function and the internal pull-up is activated.

3.3 Alternate Function Pins

The GPIO pins have alternate functions as described in Table 9.

Table 9. GPIO Alternate Functions

Pin Name	Alternate Function				
	AF0	AF1	AF2	AF3	AF4
PA0	T10OUT	T10CAP	–	–	EC10
PA1	T10OUT	T10CAP	CLKO	–	EC10
PA2	T11OUT	T11CAP	SCL0	–	EC11
PA3	T11OUT	T11CAP	SDA0	SS11	EC11
PA4	T12OUT	T12CAP	–	SCK11	EC12
PA5	T12OUT	T12CAP	TXD11	MOSI11	EC12
PA6	T13OUT	T13CAP	RXD11	MISO11	EC13
PA7	T13OUT	T13CAP	–	SS10	EC13
PA8	T14OUT	T14CAP	TXD10	MOSI10	EC14
PA9	T14OUT	T14CAP	RXD10	MISO10	EC14
PA10	T15OUT	T15CAP	–	SCK10	EC15
PA11	T15OUT	T15CAP	–	–	EC15
PB0	AN0	–	–	SCK13	ADTRG
PB1	AN1	–	SCL1	–	–
PB2	AN2	–	SDA1	–	–
PB3	AN3	–	–	–	–
PB4	AN4	–	–	–	–
PB5	AN5	–	–	–	–
PB6	AN6	–	–	–	–
PB7	AN7	–	–	–	–
PB8	AN8	–	–	–	–
PB9	AN9	–	–	–	–
PC0	T20OUT	T20CAP	–	–	EC20
PC1	T20OUT	T20CAP	–	SS13	EC20
PC2	–	–	TXD13	MOSI13	–
PC3	–	–	RXD13	MISO13	–

Table 9. GPIO alternate functions (continued)

Pin Name	Alternate Function				
	AF0	AF1	AF2	AF3	AF4
PD0	BOOT	RTCOUT	–	–	CLKO
PD1	–	–	SDA1	–	–
PD2	–	–	SCL1	SS1	–
PD3	–	–	SDA1	SCK1	–
PD4	–	–	–	MISO1	–
PD5	SWDIO	–	–	–	–
PD6	SWCLK	–	–	–	–
PD7	–	–	–	MOSI1	–
PD8	–	–	SCL2	–	–
PD9	–	–	SDA2	–	–
PE0	T21OUT	T21CAP	–	–	EC21
PE1	T21OUT	T21CAP	–	RTCOUT	EC21
PE2	–	–	RXD12	MISO12	–
PE3	–	–	TXD12	MOSI12	–
PE4	–	–	–	SCK12	–
PE5	–	–	–	SS12	ADTRG
PE6	T21OUT	T21CAP	–	SS0	EC21
PE7	T21OUT	T21CAP	–	SCK0	EC21
PE8	–	–	SCL0	MISO0	–
PE9	–	–	SDA0	MOSI0	–
PF0	XIN	–	–	–	–
PF1	XOUT	–	–	–	–
PF2	SXIN	–	–	–	–
PF3	SXOUT	–	–	–	–

4. Electrical Characteristics

4.1 Parameter Conditions

Unless otherwise specified, all voltages are referenced to V_{SS} .

4.1.1 Minimum and Maximum Values

Unless otherwise specified, our production tests guarantee the minimum and maximum values of the device under the worst-case conditions of ambient temperature, supply voltage, and frequency

Data based on characterization results, design simulations, and/or technical characteristics are not tested in production but are indicated in the table footnotes.

4.1.2 Typical Values

Unless otherwise specified, typical data are based on the conditions of $T_A = 25^{\circ}\text{C}$ and $V_{DD} = 5.0\text{V}$. The typical data are provided only as design recommendations and are not tested.

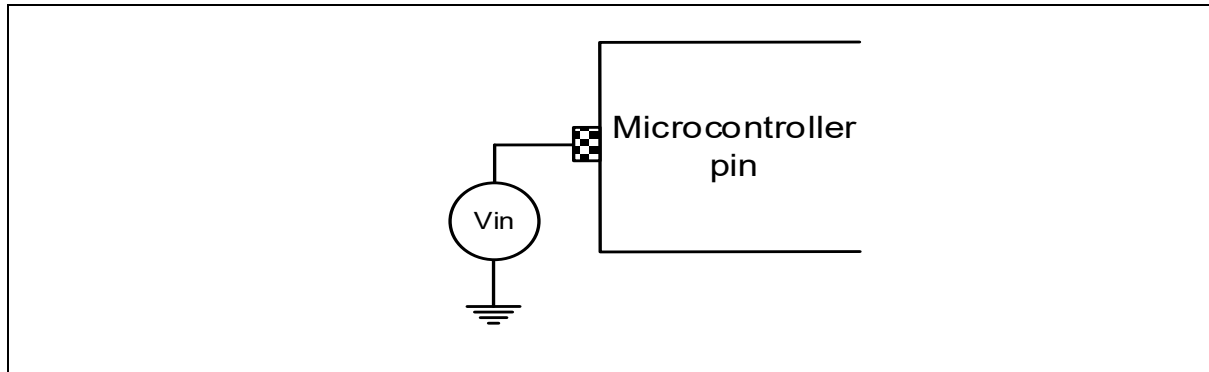
4.1.3 Typical Curves

Unless otherwise specified, all typical curves are provided only as design recommendations and are not tested.

4.1.4 Pin Input Voltage

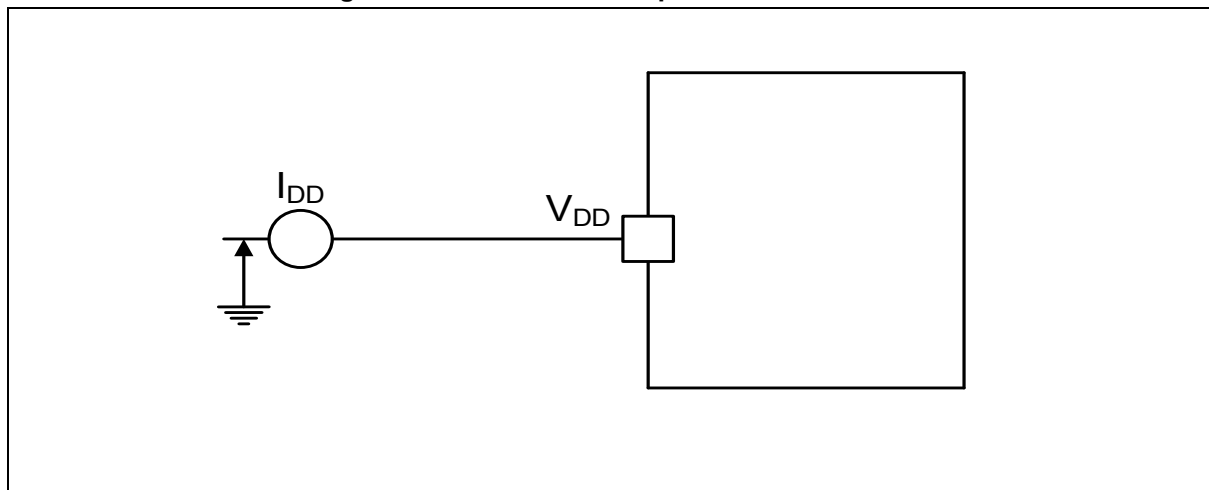
The input voltage measurement on a pin of the device is described in Figure 10.

Figure 10. Pin Input Voltage



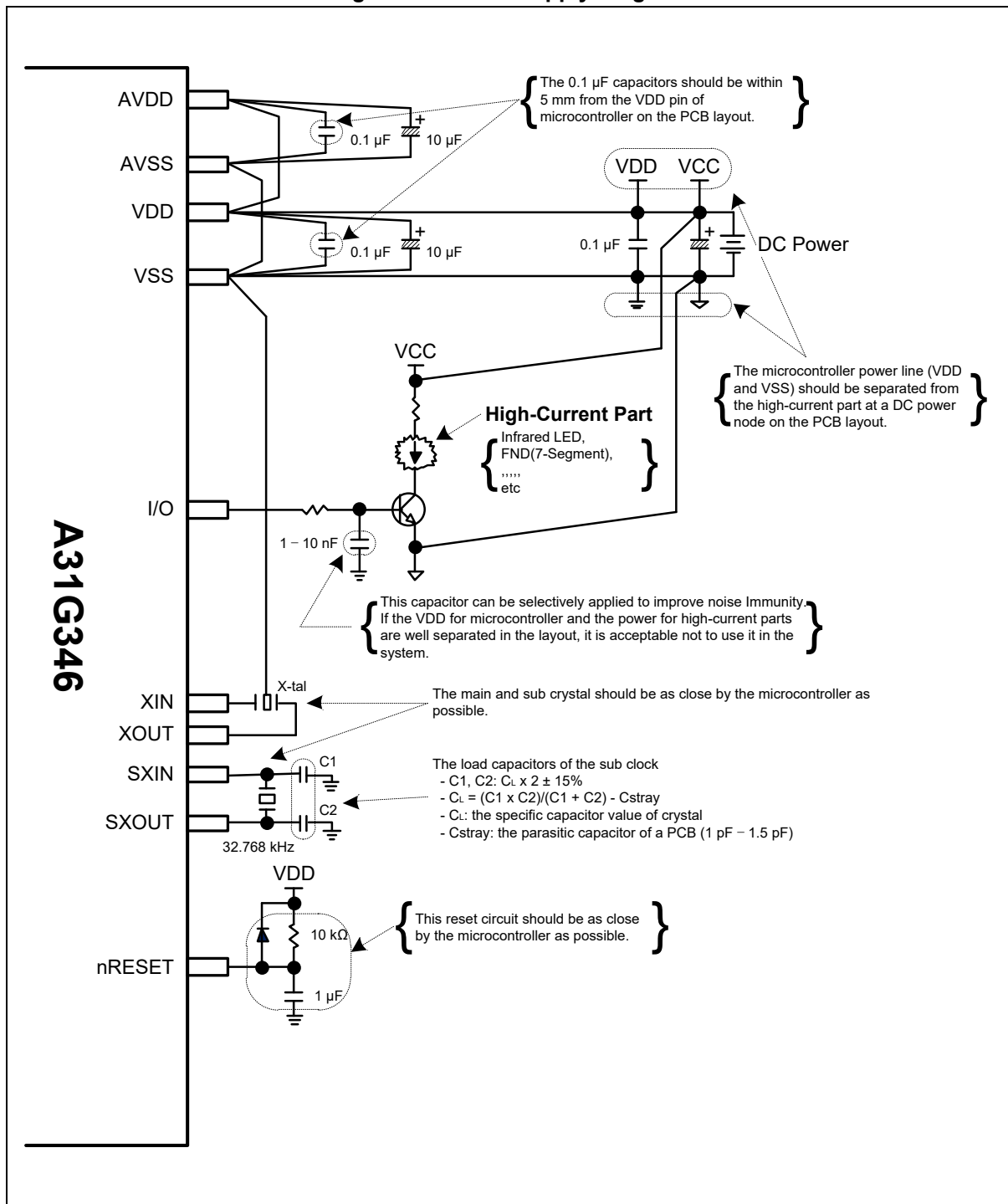
4.1.5 Current Consumption Measurement

Figure 11. Current Consumption Measurement



4.1.6 Power Supply Diagram

Figure 12. Power Supply Diagram



NOTE:

- Each power supply pair (VDD/VSS etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

4.2 Absolute Maximum Ratings

Exceeding stresses specified in Table 10 for voltage characteristics, Table 10 for current characteristics, or Table 11 for thermal characteristics may result in permanent damage to the device.

The values listed in the tables are stress ratings only and do not imply that the device will function correctly under these conditions. Prolonged exposure to these maximum rating conditions may impact on the device's reliability.

It is important to operate the device within its specified maximum ratings to ensure reliable performance.

Table 10. Voltage Characteristics

Symbol	Description	Min.	Max.	Unit
$V_{DD} - V_{SS}^{(1)}$	External main supply voltage (including V_{DD})	-0.3	6.5	V
V_I	Input voltage on I/O	-0.3	Max. (V_{DD}) + 0.3	V
V_O	Output voltage on I/O	-0.3	Max. (V_{DD}) + 0.3	V

NOTES:

1. All main power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external power supply, in the permitted range.
2. V_I maximum must always be respected.

Table 11. Current Characteristics

Symbol	Description	Max.	Unit
ΣI_{VDD}	Total current flowing into all V_{DD} power lines (source) ⁽¹⁾	120	mA
ΣI_{VSS}	Total current flowing out of all V_{SS} ground lines (sink) ⁽²⁾	120	mA
I_{OH}	Maximum out current sourced by any I/O and control pin	-25	mA
$\Sigma I_{OH(PIN)}$	Total output current sourced by sum of all I/Os and control pins ⁽²⁾	-100	mA
$I_{OL(PIN)}$	Maximum output current sunk by any I/O and control pin	25	mA
$\Sigma I_{OL(PIN)}$	Total output current sunk by sum of all I/Os and control pins ⁽²⁾	100	mA
P_T	Total power dissipation	300	mW

NOTES:

1. All main power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.

Table 12. Thermal Characteristics

Symbol	Description	Value	Unit
T_{OP}	Operating temperature (commercial grade)	-40 to 85	°C
T_{STG}	Storage temperature range	-65 to 125	°C
T_J	Maximum junction temperature	125	°C

4.3 Operating Conditions

4.3.1 Recommended Operating Conditions

Table 13. Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V _{DD}	Supply voltage	-	1.8 ⁽¹⁾	–	5.5	V
FREQ	Operating frequency	HSI @ 1.8 ≤ VDD ≤ 5.5	2.0	–	32	MHz
		LSI @ 1.8 ≤ VDD ≤ 5.5	–	40	–	kHz
		External clock @ 3.0 ≤ VDD ≤ 5.5	2.0	–	48	MHz
		Main oscillator (ceramic) @ 2.0 ≤ VDD ≤ 5.5	2.0	–	4.2	MHz
		Main oscillator (crystal) @ 2.7 ≤ VDD ≤ 5.5	2.0	–	16	MHz
		PLL @ 1.8 ≤ VDD ≤ 5.5	4.0	–	48	MHz
		Sub-oscillator @ 2.7 ≤ VDD ≤ 5.5	32	–	38	kHz
V _{IN}	I/O input voltage	–	–0.3	–	V _{DD}	V
T _A	Ambient temperature	Commercial @ 1.8 ≤ VDD ≤ 5.5	–40	–	85	°C
T _J	Junction temperature	-	–40	–	105	°C

NOTE:

1. When RESET is released, functionality is guaranteed down to VLVR Min.

4.3.2 Power-On Reset Characteristics

Table 14. Power-On Reset Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I _{DD}	Operating current	–	–	0.1	–	μA
V _{set}	POR setting level	–	–	1.4	–	V
t _R	V _{DD} voltage rising time	0.2 V to 2.0 V	0.01	–	20	ms/V
t _F	V _{DD} voltage falling time	0.2 V to 2.0 V	0.01	–	20	ms/V
V _{reset}	POR reset level	–	–	1.0	–	V
ΔV	Hysteresis voltage	–	–	0.2	–	V

4.3.3 Reset and Power Control Block Characteristics (LVR and LVI)

The parameters listed in Table 15 and Table 16 are obtained through tests conducted under ambient temperature conditions, which are specified in Table 13.

Table 15. Low Voltage Reset Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
$V_{LVR\_R}^{(1)}$	LVR Rising edge threshold	LVRVS[3:0]	1111	–	1.68	1.79	V
$V_{LVR\_F}^{(1)}$	LVR falling edge threshold	LVRVS[3:0]	1100	1.80	1.93	2.06	
			1011	1.86	2.00	2.14	
			1010	1.98	2.13	2.28	
			1001	2.15	2.31	2.47	
			1000	2.31	2.48	2.65	
			0111	2.49	2.68	2.87	
			0110	2.84	3.05	3.26	
			0101	2.97	3.19	3.41	
			0100	3.35	3.60	3.85	
			0011	3.48	3.74	4.00	
			0010	3.76	4.04	4.32	
			0001	3.93	4.22	4.51	
			0000	4.19	4.50	4.81	
ΔV	Hysteresis	–		–	100	200	mV
t_{LVRW}	Minimum pulse width	–		100	–	–	μs
–	Noise cancelling time	–		–	2	–	μs
I_{LVR}	LVR current	Enable	$V_{DD} = 5 V$	–	3.5	5.0	μA
		Disable		–	–	0.1	

NOTE:

1. The LVR threshold is selected by LVRVS[3:0] bits of CONF_LVRCNFIG register in the Configure Option Area.

Table 16. Low Voltage Indicator Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
$V_{LVI\_F^{(1)(2)}}$	Detection level	Falling edge voltage		1.80	1.93	2.06	V
				1.86	2.00	2.14	
				1.98	2.13	2.28	
				2.15	2.31	2.47	
				2.31	2.48	2.65	
				2.49	2.68	2.87	
				2.84	3.05	3.26	
				2.97	3.19	3.41	
				3.35	3.60	3.85	
				3.48	3.74	4.00	
				3.76	4.04	4.32	
				3.93	4.22	4.51	
				4.19	4.50	4.81	
ΔV	Hysteresis	–		–	100	200	mV
t_{LVRW}	Minimum pulse width	–		100	–	–	μs
–	Noise cancelling time	–		–	2	–	μs
I_{LVI}	LVI current	Enable	$V_{DD} = 5 V$	–	3.5	5.0	μA
		Disable		–	–	0.1	

NOTES:

1. The LVI level can be selected by the SCU_LVICR.LVIVS[3:0] bits.
2. Refer to the low voltage indicator control register of chapter 4.8.25 in the user's manual.

4.3.4 Current Consumption Characteristics

The amount of current consumed by the device is determined by various factors and parameters, including but not limited to the operating voltage, ambient temperature, load on I/O pins, software configuration, operating frequency, switching rate of I/O pins, location of the program in memory, and the binary code being executed.

The current consumption is measured under the conditions specified in Table 17.

4.3.4.1 Supply Voltage and Current Consumption

Table 17. Supply Voltage and Current Characteristics

Symbol	Parameter	Condition		Typ.	Max.	Unit
I _{DD1} (Main RUN)	Supply current	f _{HSI} = 32 MHz	V _{DD} = 5V ± 10%	4.5	9.0	mA
		f _{HSI} = 16 MHz	V _{DD} = 5V ± 10%	3.0	6.0	
		f _{HSI} = 8 MHz	V _{DD} = 5V ± 10%	1.9	3.8	
		f _{HSE} = 16 MHz	V _{DD} = 5V ± 10%	3.5	7.0	
			V _{DD} = 3V ± 10%	2.7	5.4	
		f _{HSE} = 8 MHz	V _{DD} = 5V ± 10%	2.2	4.4	
		f _{PLL} = 48 MHz	V _{DD} = 5V ± 10%	6.0	12.0	
I _{DD2} (Main SLEEP)		f _{HSI} = 32 MHz	V _{DD} = 5V ± 10%	2.3	4.6	mA
		f _{HSI} = 16 MHz	V _{DD} = 5V ± 10%	1.5	3.0	
		f _{HSI} = 8 MHz	V _{DD} = 5V ± 10%	1.2	2.4	
		f _{HSE} = 16 MHz	V _{DD} = 5V ± 10%	2.0	4.0	
			V _{DD} = 3V ± 10%	1.3	2.6	
		f _{HSE} = 8 MHz	V _{DD} = 5V ± 10%	1.4	2.8	
		f _{PLL} = 48 MHz	V _{DD} = 5V ± 10%	3.5	7.0	
I _{DD3} (Sub-RUN)	f _{LSE} = 32.768 kHz or f _{LSI} = 40 kHz		200	400	μA	
I _{DD4} (Sub-SLEEP)	V _{DD} = 3V/5V ± 10%, T _A = 25°C		6.0	12.0	μA	
I _{DD5} (DEEP-SLEEP)	RTCC/f _{LSE} off	V _{DD} = 5V ± 10%, T _A = 25°C	1.5	5.0	μA	
	RTCC/f _{LSE} on		3.5	8.0		

NOTES:

- Where the f_{HSE} is an external main oscillator, the f_{LSE} is an external sub-oscillator, and the f_{HSI} is a high frequency internal RC oscillator, the f_{LSI} is a low-speed internal RC oscillator, and the f_x is the selected system clock.
- All supply current items do not include the current of the low-speed internal RC (LSI) oscillator and peripheral blocks. However, they include the current of the Power-on Reset (POR) block.
- Each current consumption is measured as 0-wait for 20 MHz or less, 1-wait for 32 MHz, and 2-wait for 48 MHz.

4.3.4.2 I/O System Current Consumption

In the I/O system, current consumption can be separated into two components: Static and Dynamic.

4.3.4.3 I/O Static Current Consumption

When I/O pins configured as inputs with pull-up are externally held low, they generate a current consumption. This current consumption can be simply calculated using the values of the pull-up/pull-down resistors specified in the I/O port characteristics.

To estimate the current consumption for output pins, any external pull-down or load must also be taken into consideration.

The current consumption of I/O pins configured as inputs may increase when an intermediate voltage level is applied externally. Therefore, it is recommended to avoid applying an intermediate voltage level if there is no specific need for this configuration.

4.3.4.4 I/O Dynamic Current Consumption

Besides the internal peripheral current consumption, the application's I/Os also contribute to the overall current consumption. When an I/O pin switches, it draws current from the microcontroller's supply voltage to power the I/O pin circuitry and to charge/discharge any capacitive loads (either internal or external) connected to the pin.

4.3.5 External Clock Source Characteristics

4.3.5.1 External Main Oscillator

The external main oscillator (HSE) clock can be generated using a crystal/ceramic resonator oscillator with a frequency range of 2 to 16 MHz. The information provided in this paragraph is based on characterization results obtained using typical external components listed in Table 18.

To minimize output distortion and startup stabilization time, it is recommended to place the resonator and load capacitors as close as possible to the oscillator pins in the application.

For further information on the resonator characteristics such as frequency, package, and accuracy, it is advisable to refer to the crystal resonator manufacturer.

Table 18. External Main Oscillator Characteristics ⁽¹⁾

Symbol	Parameter	Condition ⁽²⁾	Min.	Typ.	Max.	Unit
f_{HSE}	HSE crystal frequency	$V_{DD} = 2.7 \text{ V to } 5.5 \text{ V}$	2.0	–	16.0	MHz
	HSE ceramic oscillator frequency	$V_{DD} = 2.0 \text{ V to } 5.5 \text{ V}$	2.0	–	4.2	
		$V_{DD} = 2.7 \text{ V to } 5.5 \text{ V}$	2.0	–	16.0	
f_{OSC_IN}	XIN input frequency	$V_{DD} = 3.0 \text{ V to } 5.5 \text{ V}$	2.0	–	48.0	MHz
	External clock duty ratio	–	–	50	–	%
R_F	Feedback resistor	$XIN = V_{DD}$, $XOUT = V_{SS}$, $T_A = 25^\circ\text{C}$, $V_{DD} = 5 \text{ V}$	0.7	1.0	1.3	MΩ
$t_{SU(HSE)}^{(3)}$	HSE crystal startup time	$V_{DD} = 2.7 \text{ V to } 5.5 \text{ V}$, $f_{HSE} \geq 2 \text{ MHz}$	–	–	60	ms
	HSE ceramic oscillator startup time	$V_{DD} = 2.0 \text{ V to } 5.5 \text{ V}$, $4.2 \text{ MHz} \geq f_{HSE} \geq 2 \text{ MHz}$	–	–	10	
$t_{XH/XL}$	Duration of high or low state of XIN input	$f_{OSC\_IN} = 2.0 \text{ to } 48 \text{ MHz}$	10.4	–	250	ns

NOTES:

1. Guaranteed by design.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 2 MHz oscillation is reached. This value is measured for a standard crystal resonator, and it can vary significantly with the crystal manufacturer.

Figure 13. Crystal/Ceramic Oscillator

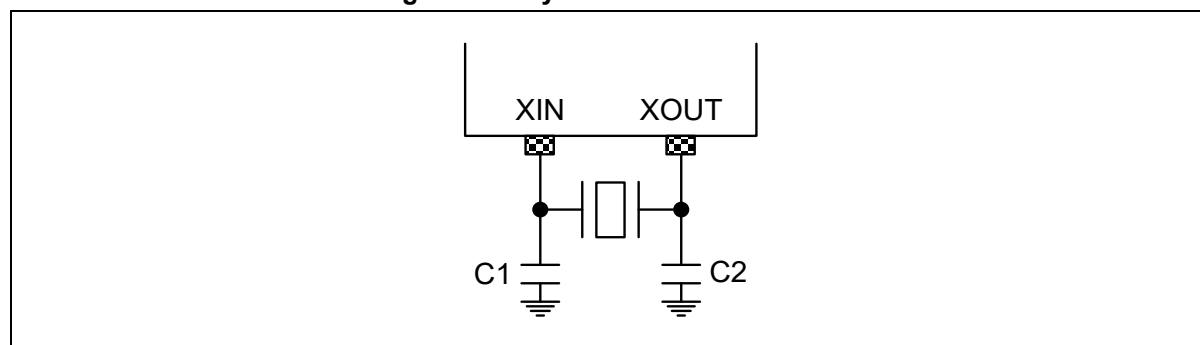
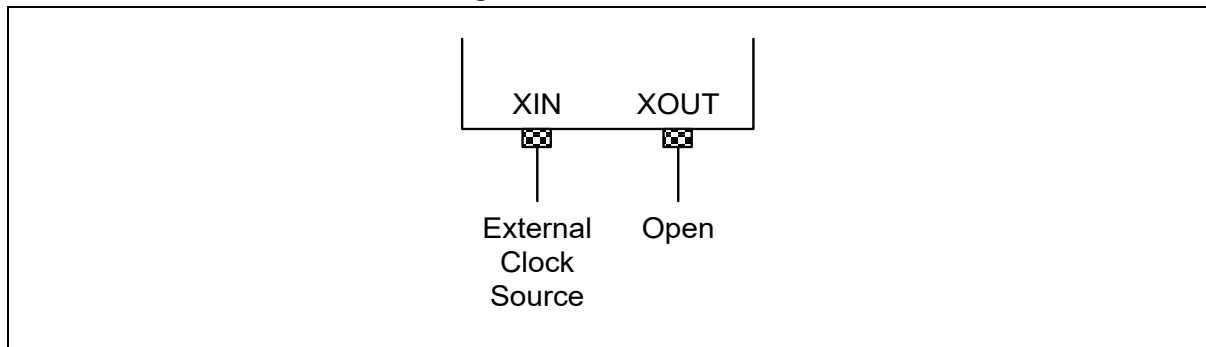
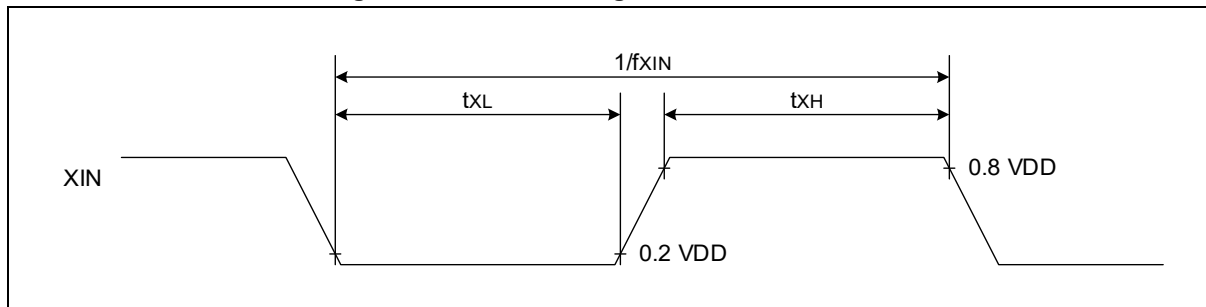
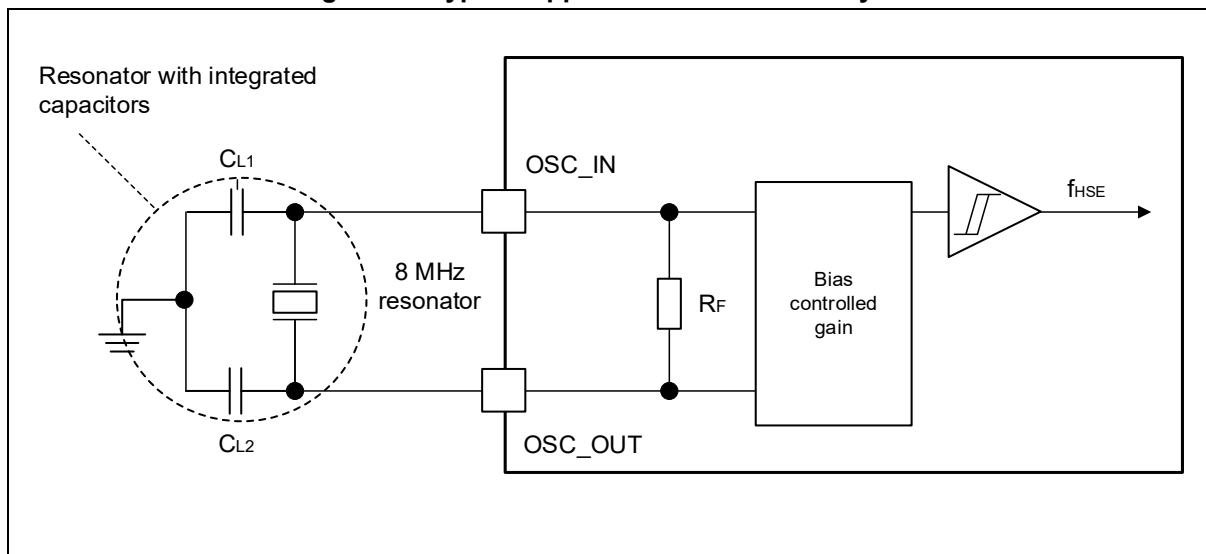


Figure 14. External Clock**Figure 15. Clock Timing Measurement at XIN**

It is recommended to use high-quality external ceramic capacitors designed for high-frequency applications and selected to match the requirements of the crystal or resonator. The CL1 and CL2 capacitors are usually of the same size, and the crystal manufacturer typically specifies a load capacitance, which is the series combination of both capacitors. The capacitance values of the CL1 and CL2 capacitors should be set by considering the parasitic capacitance of the printed circuit board (PCB) and microcontroller pins, which is approximately twice the specified load capacitance of the crystal.

Figure 16 shows a circuit diagram of a typical application with an 8 MHz crystal.

Figure 16. Typical Application With 8 MHz Crystal

4.3.5.2 External Sub-Oscillator

The external sub-oscillator (LSE) clock can be generated using a crystal/ceramic resonator oscillator with a frequency of 32.768 kHz. The information provided in this paragraph is based on characterization results obtained using typical external components listed in Table 19.

To minimize output distortion and startup stabilization time, it is recommended to place the resonator and load capacitors as close as possible to the oscillator pins in the application.

For further information on the resonator characteristics such as frequency, package, and accuracy, it is advisable to refer to the crystal resonator manufacturer.

Table 19. External Sub-Oscillator Characteristics ⁽¹⁾

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{LSE}	LSE oscillator frequency	2.7 V to 5.5 V	32	32.768	38	kHz
f_{OSC_SXIN}	SXIN input frequency	2.7 V to 5.5 V	32	–	38	kHz
R_F	Feedback resistor	$T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{ V}$	6.5	13	26	$\text{M}\Omega$
$t_{SU(LSE)}^{(2)}$	LSE crystal startup time	–	–	–	10	s
		$V_{DD} = 3\text{ V}$, $T_A = 25^\circ\text{C}$		0.7	1.5	
$t_{XH/XL}$	Duration of high or low state of SXIN input	–	13	–	15	μs

NOTES:

1. Guaranteed by design.
2. t_{SU} (LSI) is the startup time measured from the moment it is enabled (by software) until it reaches a stabilized 32.768 kHz oscillation. This value is measured using a standard crystal resonator and can vary significantly depending on the crystal manufacturer.

Figure 17. Crystal Oscillator

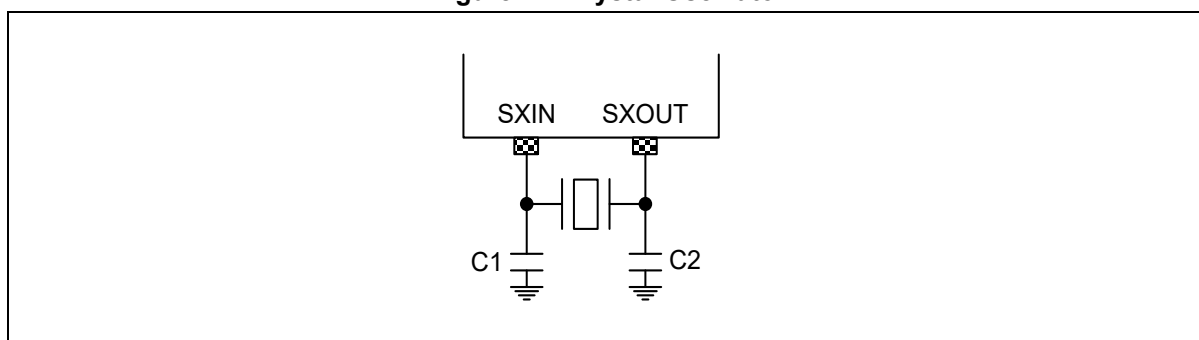


Figure 18. External Clock

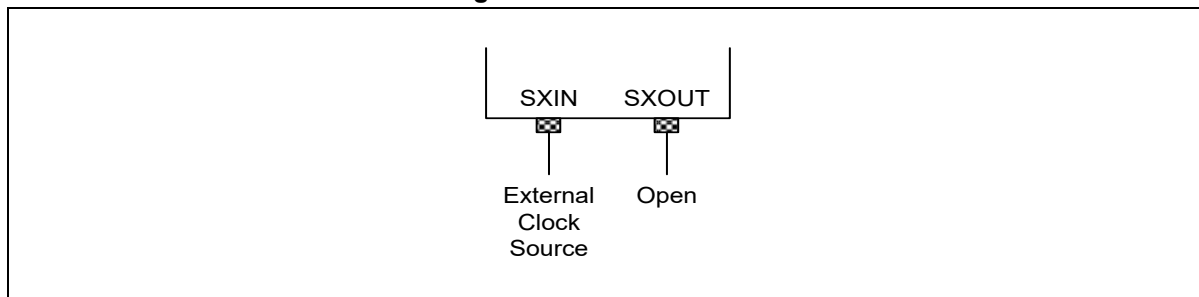
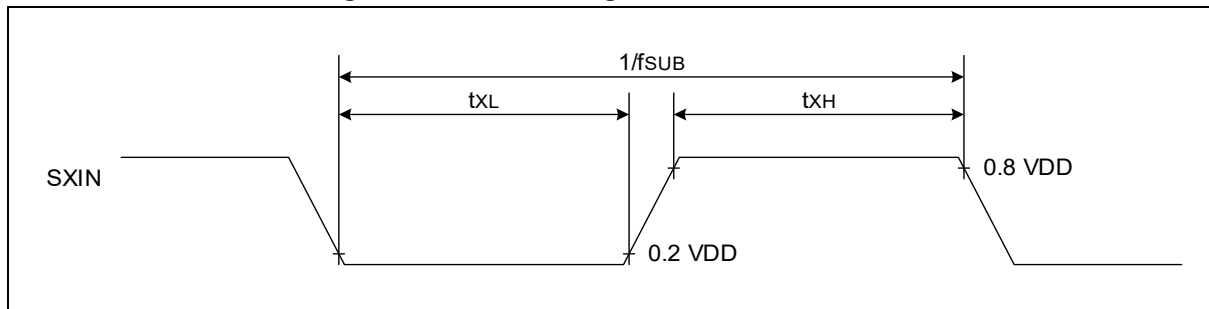
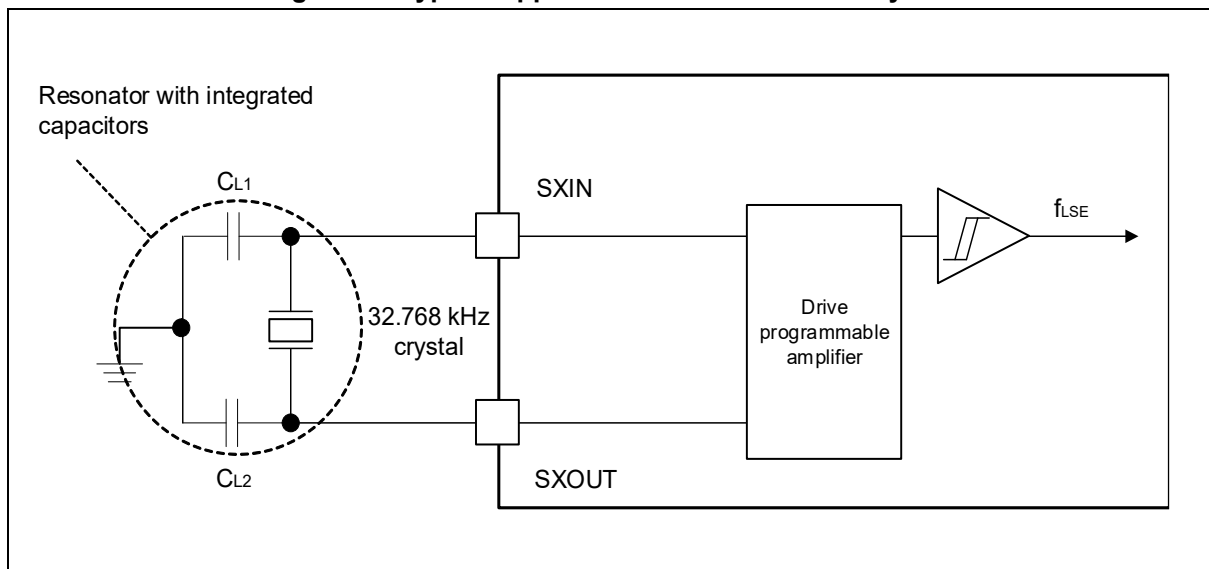


Figure 19. Clock Timing Measurement at SXIN**Figure 20. Typical Application With 32.768 kHz Crystal****NOTE:**

1. An external resistor is not required between SXIN and SXOUT and it is forbidden to add one.

4.3.6 Internal Clock Source Characteristics

The parameters listed in Table 20 and Table 21 are obtained through tests conducted under ambient temperature and supply voltage conditions, which are specified in Table 13.

4.3.6.1 High-Speed Internal RC Oscillator

Table 20. High-Speed Internal RC Oscillator Characteristics

Symbol	Parameter	Condition ⁽²⁾	Min.	Typ.	Max.	Unit
V _{DD}	Operating voltage	–	1.8	–	5.5	V
f _{HSI}	HSI frequency	–	–	32	–	MHz
ACC _{HSI} ⁽¹⁾	Accuracy	T _A = 0°C to 50°C	–	–	±1.5	%
		T _A = –40°C to 85°C (commercial)	–	–	±3.0	
DuCy	Duty cycle	–	40	50	60	%
t _{STAB(HSI)}	HSI oscillator stabilization time	–	–	–	2	μs
I _{HSI}	HSI oscillator power consumption	HSI oscillator is enabled.	–	500	700	μA
		HSI oscillator is disabled.	–	–	0.1	

NOTE:

1. Guaranteed by design, but it may require on-board programming after the SMT process. Calibration of the HSI at high temperatures can result in frequency shifts, so it is important to ensure sufficient calibration time for cooling to near room temperature after the SMT process.

4.3.6.2 Low-Speed Internal RC Oscillator

Table 21. Low-Speed Internal RC Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f _{LSI}	LSI frequency	–	34	40	46	kHz
t _{STAB(LSI)}	LSI stabilization time	–	–	100	1000	μs
I _{LSI}	LSI power consumption	LSI is enabled.	–	2	4	μA
		LSI is disabled.	–	–	0.1	

4.3.7 PLL Electrical Characteristics

Table 22. PLL Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{PLLIN}	Input Frequency Range	—	1	2	3	MHz
f_{VCO}	VCO Frequency Range	—	60	—	96	MHz
f_{PLL}	Output Frequency Range	—	4	—	48	MHz
T_{OD}	Clock Duty Ratio	—	40	50	60	%
t_{LOCK}	Locking Time	—	—	—	200	μ s
I_{PLL}	PLL Current	PLL is enabled.	—	300	500	μ A
		PLL is disabled.	—	—	0.1	μ A

4.3.8 Flash Memory Characteristics

Table 23. Flash Memory Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
t _{FW}	Write time	Flash write mode		–	25	–	μs
t _{FSE}	Page/Sector erase time	–		–	2	–	ms
t _{FCE}	Chip erase time	–		–	8	–	ms
V _{PGM}	Programming voltage	During erase/write		1.8	–	5.5	V
f _{HCLK}	System clock frequency	–		2.0	–	–	MHz
N _{FWE}	Endurance of code Flash memory (write/erase operation)	Page 0 to 511 Configuration option page 1	T _A = 25°C Page unit	10,000	–	–	cycles
		Configuration option page 2/3/4/5		100,000	–	–	
t _{FRT}	Retention time	–		10	–	–	years

4.3.9 I/O Port Characteristics

The parameters listed in Table 24 are obtained through tests conducted under ambient temperature and supply voltage conditions, which are specified in Table 13.

Table 24. DC Electrical Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
V _{IH}	Input high voltage	All input ports, nRESET		0.8 × V _{DD}	–	V _{DD}	V
V _{IL}	Input low voltage	All input ports, nRESET		–	–	0.2 × V _{DD}	V
V _{OH}	Output high voltage	V _{DD} = 4.5 V, I _{OH} = –10 mA, All output ports, T _A = 25°C		V _{DD} – 1.3	–	–	V
V _{OL}	Output low voltage	V _{DD} = 4.5 V, I _{OL} = 15 mA, All output ports, T _A = 25°C		–	–	1.3	V
I _{IH}	Input high leakage current	All input ports		–	–	1	μA
I _{IL}	Input low leakage current	All input ports		–1	–	–	μA
R _{PU}	Pull-up resistor	V _I = 0 V, T _A = 25°C All input ports	V _{DD} = 5 V	25	50	100	kΩ
			V _{DD} = 3 V	50	100	200	
		V _I = 0 V, T _A = 25°C nRESET	V _{DD} = 5 V	150	250	400	
			V _{DD} = 3 V				
R _{PD}	Pull-down resistor	V _I = V _{DD} , T _A = 25°C All input ports	V _{DD} = 5 V	25	50	100	kΩ
			V _{DD} = 3 V	50	100	200	
C _{IO}	I/O pin capacitance	F = 1 MHz. Unmeasured pins are connected to V _{SS} .		–	–	10	pF

4.3.9.1 Output Driving Current

The GPIOs are capable of sinking or sourcing currents within the range specified by I_{OL} and I_{OH} .

To ensure compliance with the absolute maximum ratings specified in chapter 4.2, it is necessary to limit the number of I/O pins driving current in the user application.

- The total current sourced by all I/O pins on V_{DD} and the maximum operating current of the microcontroller on V_{DD} (during RUN mode) must not exceed the absolute maximum rating ΣI_{VDD} specified in Table 11.
- The total current sunk by all I/O pins on GND and the maximum operating current of the microcontroller on GND (during RUN mode) must not exceed the absolute maximum rating ΣI_{VSS} specified in Table 11.

4.3.9.2 Output Voltage Characteristics

Unless otherwise specified, the parameters in Table 25 are obtained through tests conducted under ambient temperature and supply voltage conditions, which are specified in Table 13.

Table 25. Output Voltage Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V _{OH}	Output high level voltage for an I/O pin	VDD = 4.5 V, IOH = -10 mA	VDD - 1.3	-	-	V
V _{OL}	Output low level voltage for an I/O pin	VDD = 4.5 V, IOL = 15 mA	-	-	1.3	V

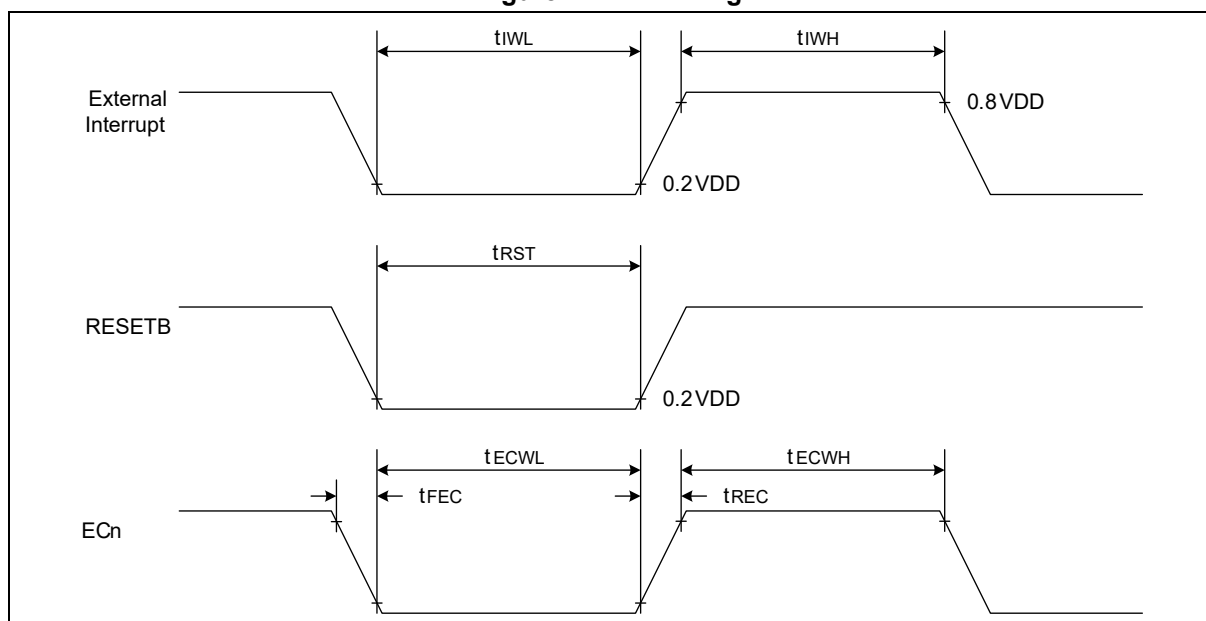
4.3.9.3 AC Characteristics

Unless otherwise specified, the parameters in Table 26 are obtained through tests conducted under ambient temperature and supply voltage conditions, which are specified in Table 13.

Table 26. AC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{RST}	RESETB input low width	$V_{DD} = 5\text{ V}$	10	—	—	μs
t_{IWH}, t_{IWL}	Interrupt input high, low width	$V_{DD} = 5\text{ V}$, all interrupts	100	—	—	ns
t_{ECWH}, t_{ECWL}	External counter input high, low pulse width	$V_{DD} = 5\text{ V}$, all external counter inputs	100	—	—	ns
t_{REC}, t_{FEC}	External counter transition time	$V_{DD} = 5\text{ V}$, all external counter inputs	—	—	20	ns
f_{IO1}	I/O frequency	$V_{DD} = 5.0\text{ V}$, $C_L = 30\text{ pF}$ All except f_{IO2}	—	—	6	MHz
f_{IO2}		$V_{DD} = 2.7\text{ V}$, $C_L = 30\text{ pF}$, SPI pins	—	—	8	MHz

Figure 21. AC Timing



4.3.10 Analog-to-Digital Converter Characteristics

Unless otherwise specified, the parameters in Table 27 are obtained through tests conducted under ambient temperature and supply voltage conditions, which are specified in Table 13.

Table 27. ADC Electrical Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
V _{DD}	Operating voltage	—		2.7	—	5.5	V
—	Resolution	—		—	12	—	bit
V _{AN}	Analog input voltage	—		AV _{SS}	—	AV _{DD}	V
AV _{DD}	Analog voltage	—		V _{DD} -0.3	V _{DD}	V _{DD} +0.3	V
V _{ADCBUF}	Band Gap Reference Buffer Voltage	—		900	950	1000	mV
I _{ADC}	ADC current	ADC is enabled.	AV _{DD} = 5.0 V f _{ADC} = 20 MHz	—	1.6	—	mA
		ADC is disabled.		—	—	0.1	μA
I _{AN}	ADC input leakage current	AV _{DD} = 5.0 V		—	—	2	μA
t _{CONV}	Conversion time	2.7 V < AV _{DD}		1	—	—	μs
f _{ADC}	Operating frequency	—		—	—	20	MHz
INL	Integral non-linearity	—		—	±4	±9	LSB
DNL	Differential non-linearity			—	±2	±6	
ZOE ⁽¹⁾	Zero-offset error			—	±3	—	
FSE ⁽²⁾	Full-scale error			—	±3	—	

NOTES:

1. The zero offset error is the discrepancy between the value of 0x000 and the converted output value when a zero-input voltage (AV_{SS}) is applied.
2. The full-scale error is the discrepancy between the value of 0xFFFF and the converted output value when the full-scale voltage (AV_{DD}) is applied.
3. T_A = 25°C

4.3.10.1 General PCB Design Guidelines

The power supply must be separated in accordance with the scheme shown in Figure 12. The decoupling capacitors across the V_{DD}/AV_{DD} are ceramic (good quality) capacitors and must be placed as close as possible to the chip.

4.3.11 Temperature Sensor Characteristics

Table 28. Temperature Sensor Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T_{LIN}	Temperature Linearity	–	–	± 10	–	$^{\circ}\text{C}$
ΔF	Frequency Variation	$(F(T2) - F(T1)) \div (T2 - T1)$	1.6	3.6	6.5	$\text{kHz}/^{\circ}\text{C}$
–	Frequency Deviation	$\Delta F \div F(30)$	0.3	0.45	0.6	%
I_{TS}	Sensor Current	Enable	$V_{DD} = 5.0 \text{ V}$	10	20	μA
		Disable		–	10	nA
t_{START}	Startup Time	–	–	–	500	μs

NOTE:

1. $\text{Temperature} = \{(F(T) - F(30)) \div \Delta F\} + 30 [^{\circ}\text{C}]$
 Where $T1 = 30^{\circ}\text{C}$, $T2 = 85^{\circ}\text{C}$
 - A. $F(T1)$ [kHz] is the temperature sensor output frequency acquired at 30°C .
 - B. $F(T2)$ [kHz] is the temperature sensor output frequency acquired at 85°C .
 - C. $F(T)$ [kHz] is the temperature sensor output frequency acquired at an arbitrary temperature.

4.3.12 Communication Interface Characteristics

4.3.12.1 I2C Interface Characteristics

The I2C interface conforms to the timing requirements specified in the I2C-bus specification, in addition to the user timing requirements listed below:

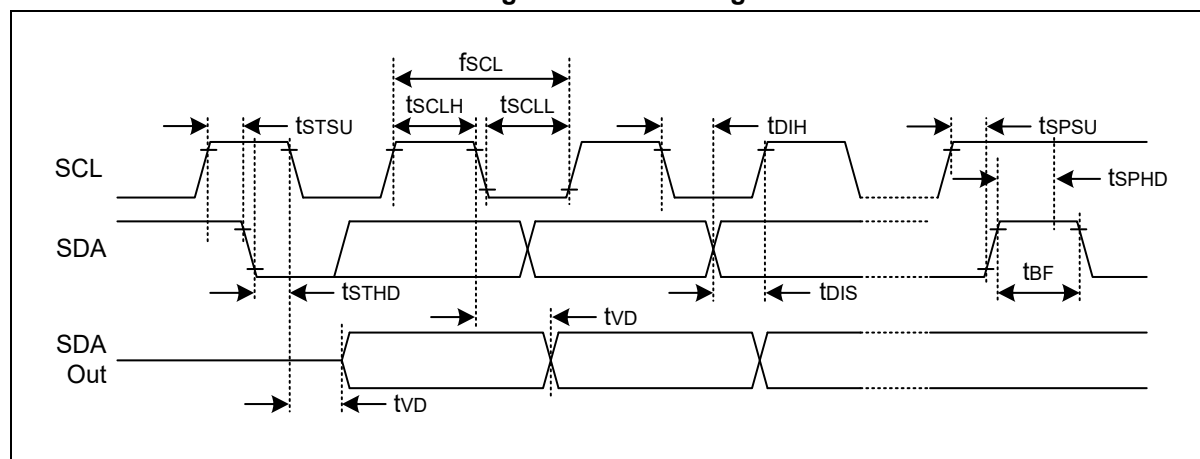
- Standard mode (Sm): up to 100 kbps bit rate
- Fast mode (Fm): up to 400 kbps bit rate
- Fast mode plus (Fm+): up to 1 Mbps bit rate

The I2C timing requirements are guaranteed by design when the I2C peripheral is configured correctly and the I2C clock frequency is equal to or greater than the minimum value listed in the table below.

Table 29. I2C Characteristics

Symbol	Parameter	Standard mode		Fast mode		Fast mode plus		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
–	I2C Operating voltage	$V_{DD} \geq 1.8\text{ V}$		$V_{DD} \geq 2.0\text{ V}$		$V_{DD} \geq 2.7\text{ V}$		V
f_{SCL}	Clock frequency	0	100	0	400	0	1,000	kHz
t_{SCLH}	Clock high pulse width	4.0	–	0.6	–	0.26	–	μs
t_{SCLL}	Clock low pulse width	4.7	–	1.3	–	0.5	–	
t_{BF}	Bus free time	4.7	–	1.3	–	0.5	–	
t_{STSU}	Start condition setup time	4.7	–	0.6	–	0.26	–	
t_{STHD}	Start condition hold time	4.0	–	0.6	–	0.26	–	
t_{SPSU}	Stop condition setup time	4.0	–	0.6	–	0.26	–	
t_{SPHD}	Stop condition hold time	4.0	–	0.6	–	0.26	–	
t_{VD}	Output valid from clock	0	–	0	–	0	–	
t_{DIH}	Data input hold time	0	–	0	1.0	0	0.45	
t_{DIS}	Data input setup time	250	–	100	–	50	–	ns

Figure 22. I2C Timing



4.3.12.2 SPI Interface Characteristics

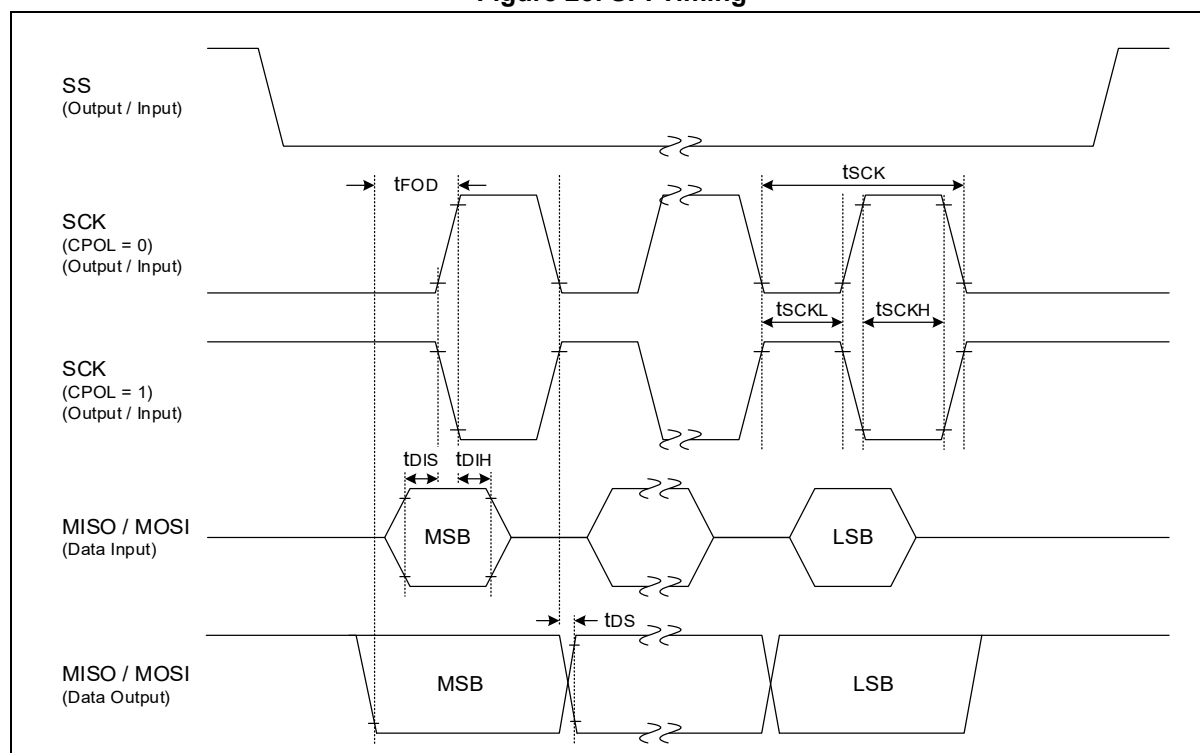
Unless otherwise specified, the parameters in Table 30 are obtained through tests conducted under ambient temperature, f_{PCLK} frequency and supply voltage conditions, which are specified in Table 13.

For more information about I/O alternate function characteristics (SS, SCK, MOSI, and MISO for SPI), refer to 4.3.9.

Table 30. SPI Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
f _{SCK}	SPI clock frequency	VDD ≥ 2.7 V	Internal SCK source	–	–	8	MHz
			External SCK source				
		VDD ≥ 1.8 V	Internal SCK source	–	–	4	
			External SCK source				
t _{SCKH} , t _{SCKL}	Input/output clock high, low pulse width	Internal/External SCK source		0.8 × Typ.	t _{SCK} /2	1.2 × Typ.	ns
t _{FOD}	First output clock delay time	Internal/External SCK source, CPHA = 0		0.4 x t _{SCK}	–	–	ns
t _{DS}	Output clock delay time	–		–	–	25	ns
t _{DIS}	Input setup time			17	–	–	ns
t _{DIH}	Input hold time			20	–	–	ns
Duty	Duty cycle of SPI frequency (SCK)	Slave mode		40	50	60	%

Figure 23. SPI Timing



4.3.12.3 UART Interface Characteristics

Unless otherwise specified, the parameters in Table 31 are obtained through tests conducted under ambient temperature, f_{CLK} frequency and supply voltage conditions, which are specified in Table 13.

Table 31. UART Characteristic

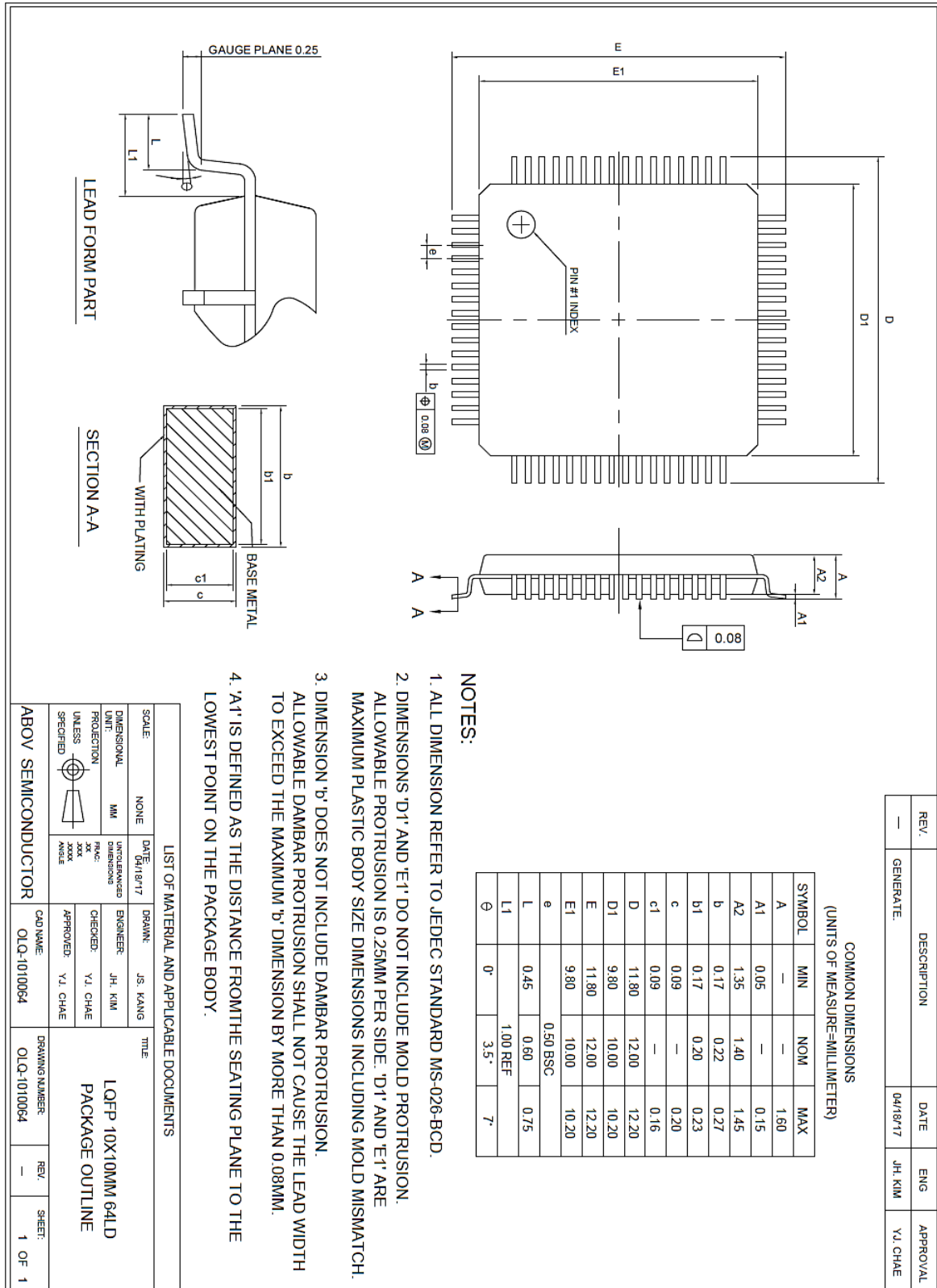
Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{max}	Maximum character transmission frequency	–	–	0.32	Mbits

5. Package Information

5.1 64-LQFP-1010 Package Information

64-LQFP is a 64-pin, 10 x 10 mm Quad Flat Package.

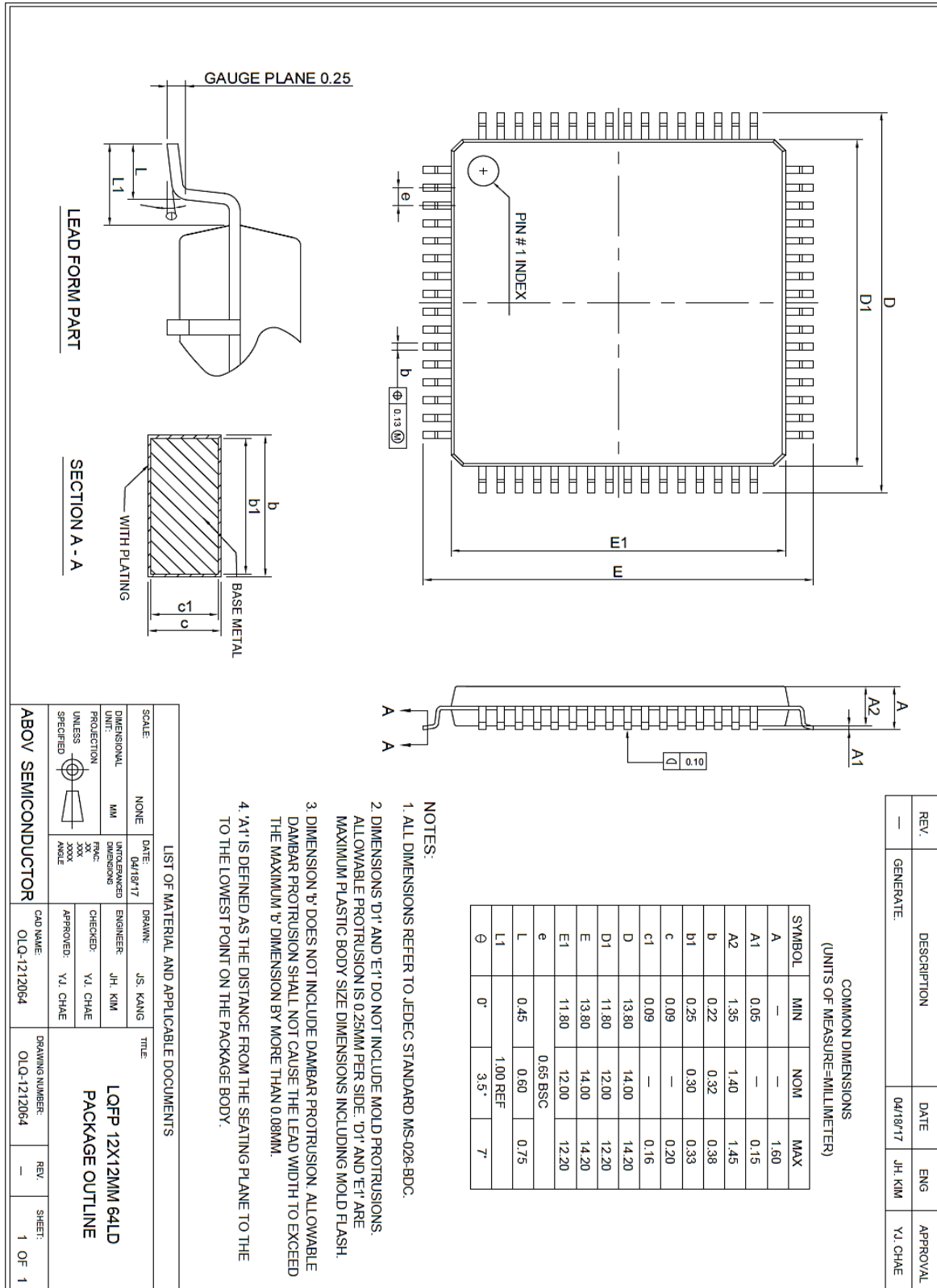
Figure 24. 64-LQFP-1010 Package Dimension



5.2 64-LQFP-1212 Package Information

64-LQFP is a 64-pin, 12 x 12 mm Quad Flat Package.

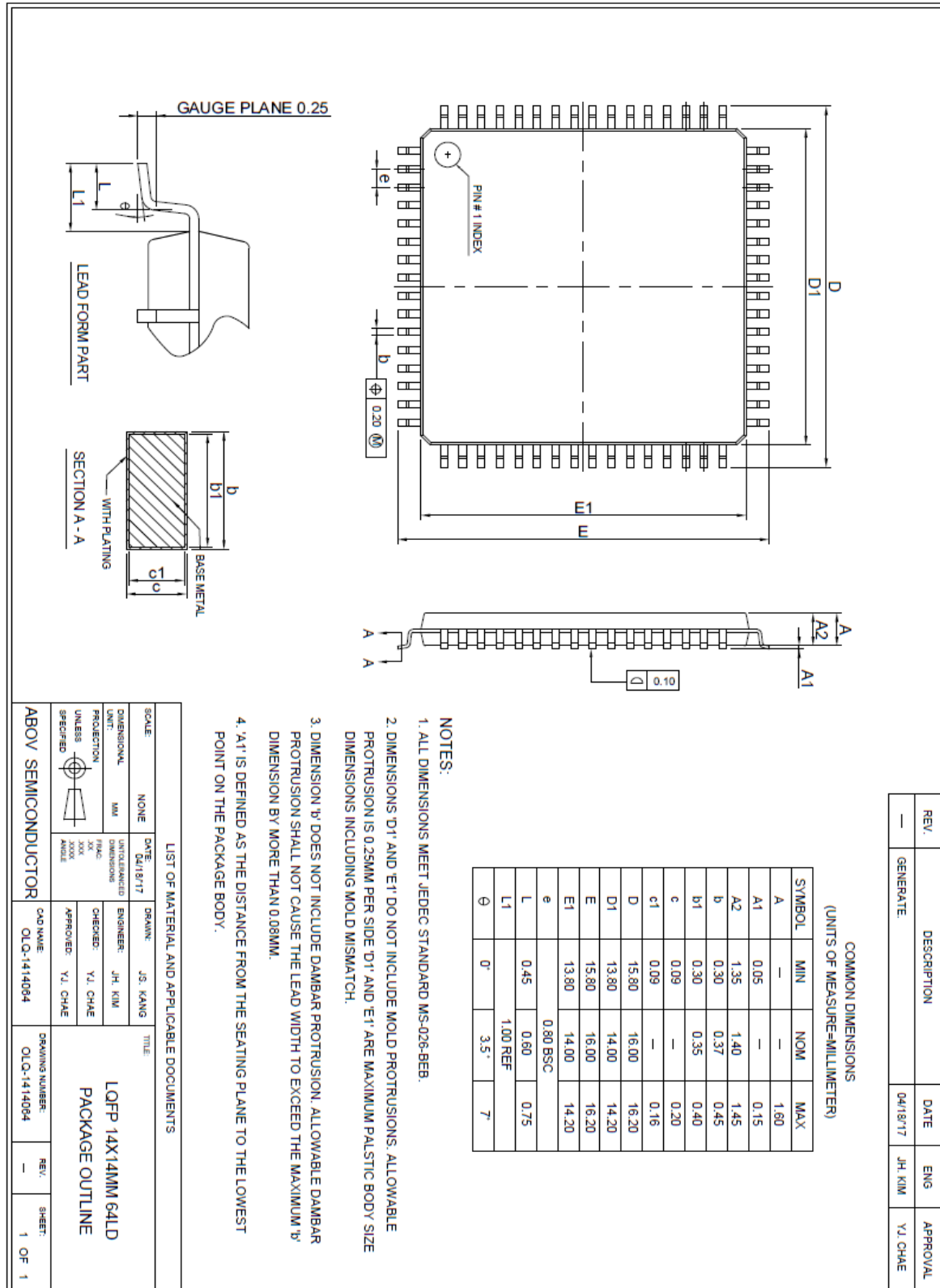
Figure 25. 64-LQFP-1212 Package Dimension



5.3 64-LQFP-1414 Package Information

64-LQFP is a 64-pin, 14 x 14 mm Quad Flat Package.

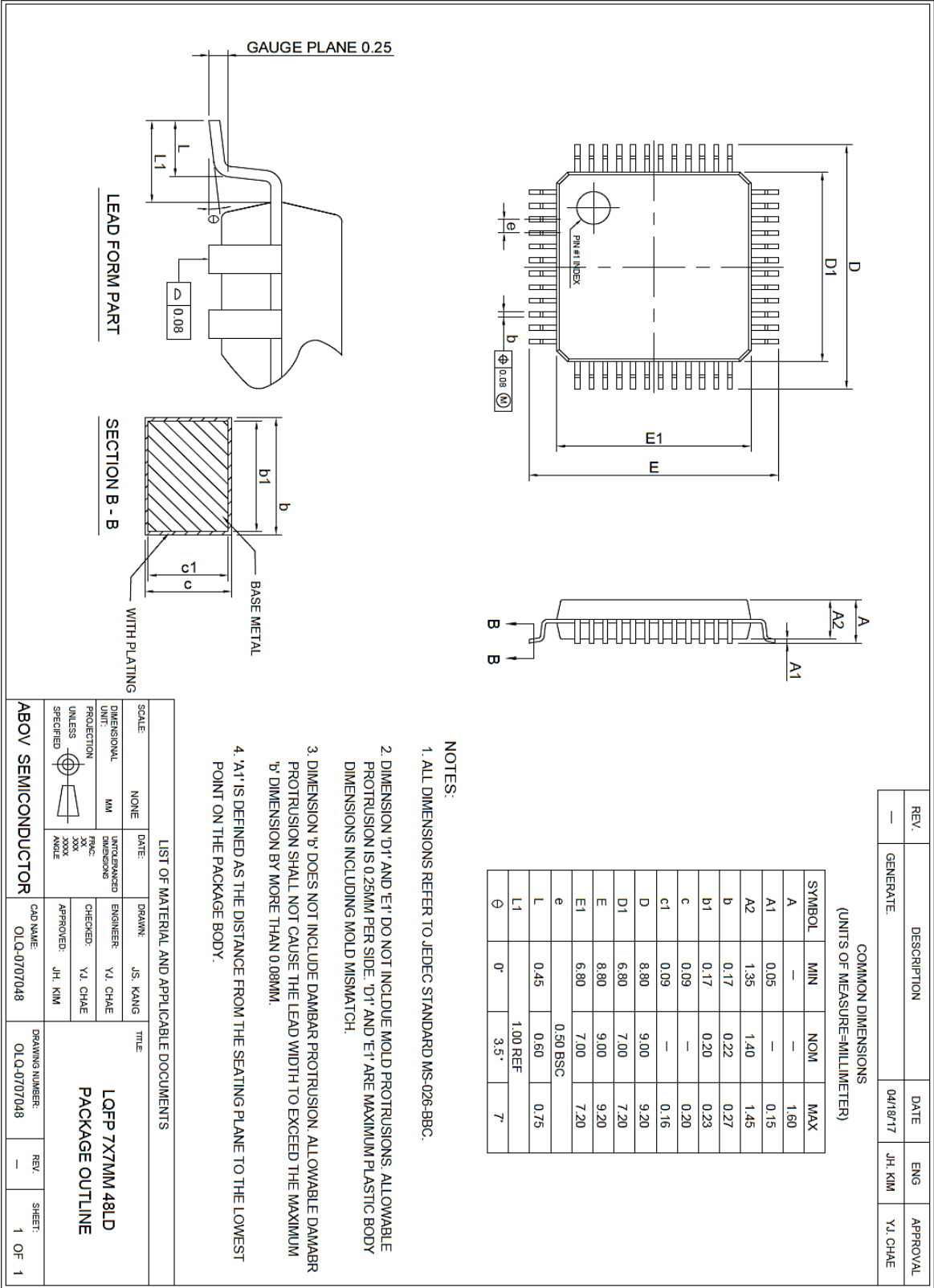
Figure 26. 64-LQFP-1414 Package Dimension



5.4 48-LQFP-0707 Package Information

48-LQFP is a 48-pin, 7 x 7 mm Quad Flat Package.

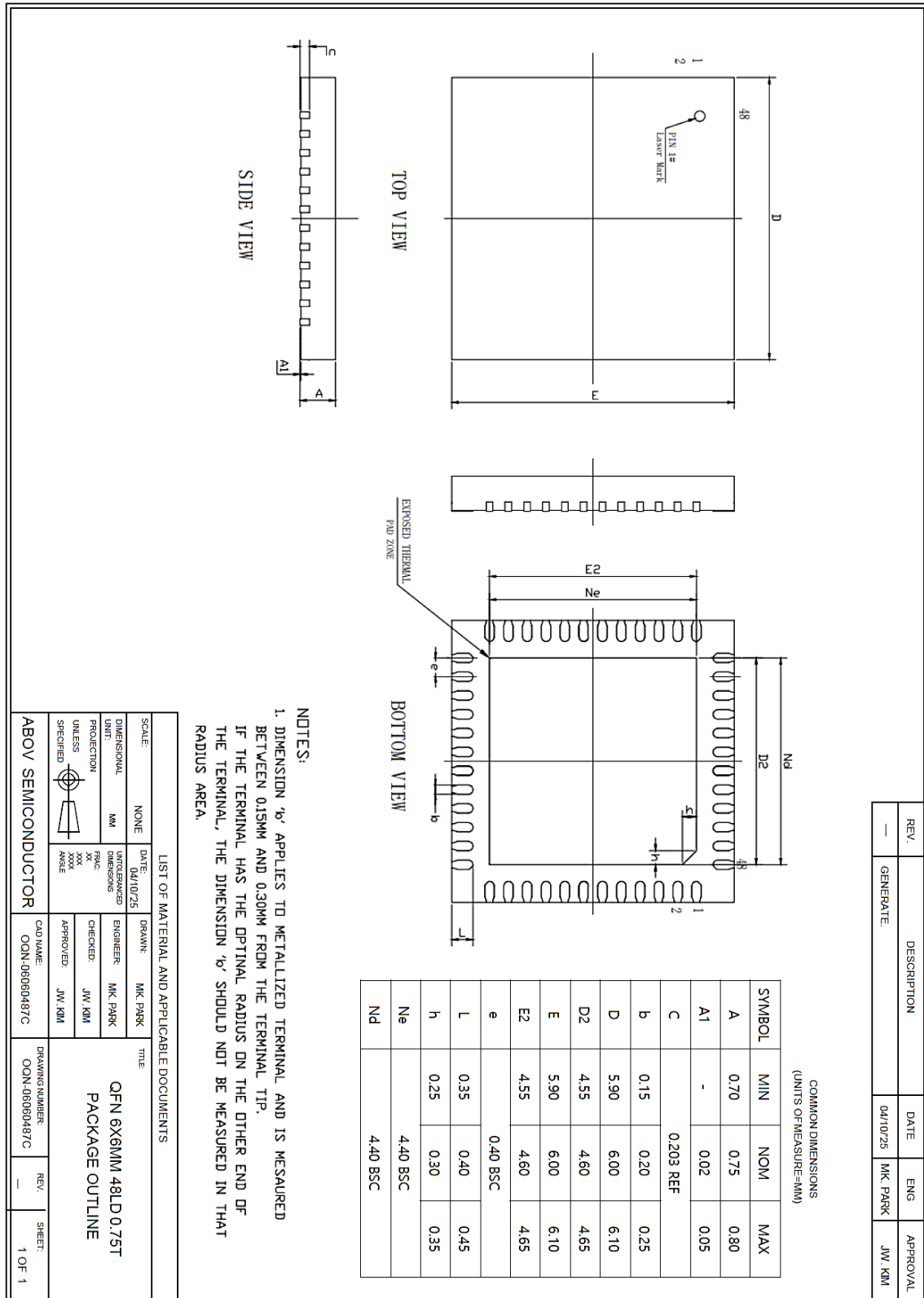
Figure 27. 48-LQFP-0707 Package Dimension



5.5 48-QFN-0606 Package Information

48-QFN is a 48-pin, 6 x 6 mm Quad Flat No-lead package.

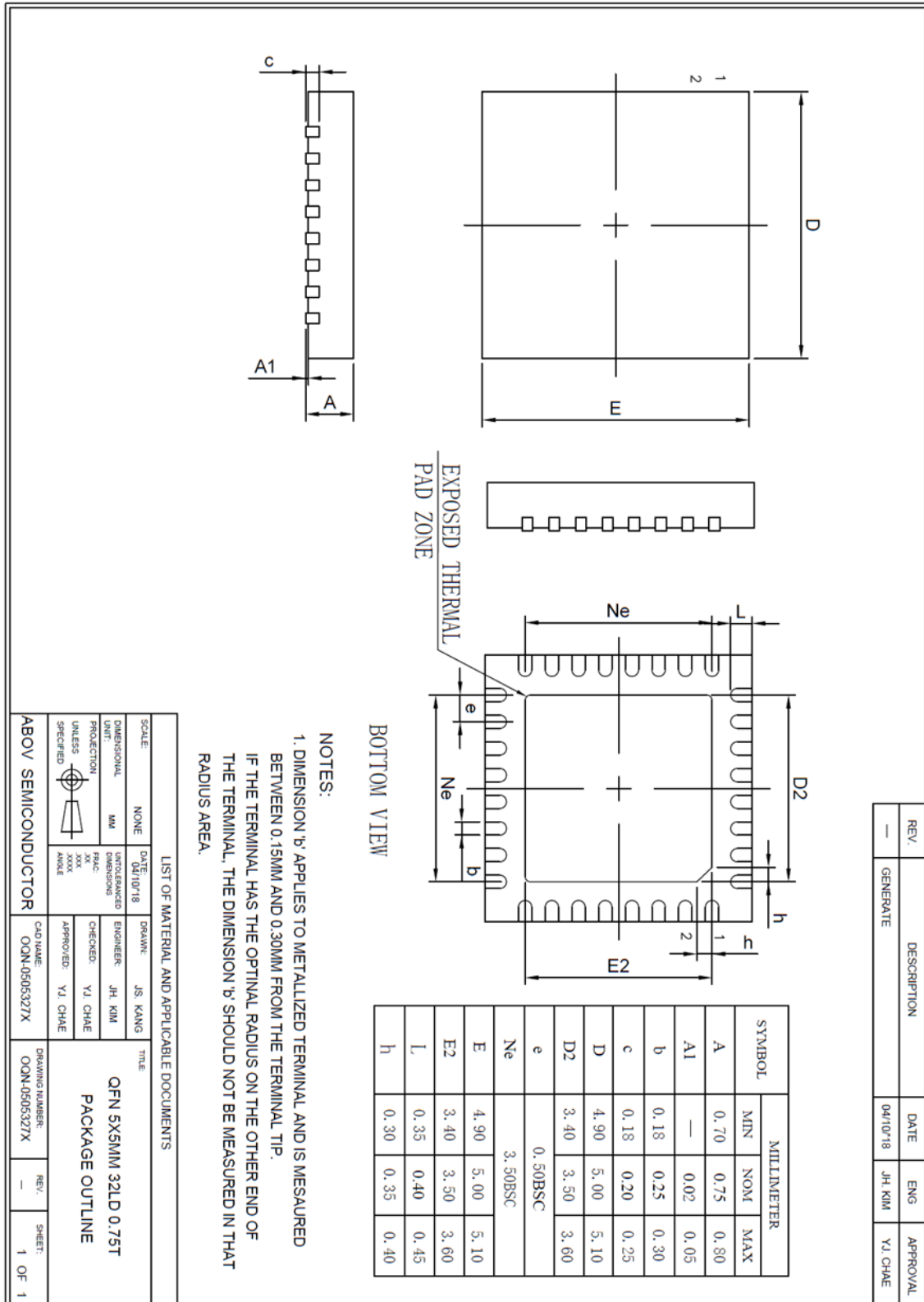
Figure 28. 48-QFN-0606 Package Dimension



5.6 32-QFN-0505 Package Information

32-QFN is a 32-pin, 5 x 5 mm Quad Flat No-lead package.

Figure 29. 32-QFN-0505 Package Dimension



6. Ordering Information

Figure 30. Device Nomenclature - Part Number Decoder

A31G34		6	R	L	N	(T)
Device family name						
A31G34 = Arm Cortex-M0+ based microcontroller						
Code memory size						
6	256 Kbytes					
Pin count						
R	64 pins					
C	48 pins					
K	32 pins					
Package type						
L	LQFP (0.5 mm pin pitch)					
M	LQFP (0.65 mm pin pitch)					
N	LQFP (0.8 mm pin pitch)					
U	QFN					
Temperature						
None	–40 to 85°C (commercial grade)					
Bonding wire						
None	Au wire					
N	Pd-Cu wire					
Packing						
(T)	Tape & reel					
(W)	Wafer					
(C)	Chip carrier					

NOTE:

- For a list of available options (memory, package, and so on) or for further information on any aspect of this device, contact the nearest [ABOV sales office](#)

Revision History

Revision	Date	Notes
1.00	Sep. 16, 2025	Initial release

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