A31G324, A31G323
Data Sheet

32-bit Cortex-M0+ based General Purpose Microcontroller

Version 1.05

Features

Core

- High performance Cortex-M0+ core

Memories

- 128/64KB code flash memory
- 16KB SRAM

Clock, reset and power management

- Two main operating clocks: HCLK, PCLK
  - — Real time clock and calendar
- Two system reset: cold reset, warm reset
  - — Cold reset source: POR
  - — Warm reset sources: nRESET pin, WDT reset, LVR reset, MON reset, S/W reset, CPU request reset

  Power management mode

  : RUN, SLEEP, DEEP SLEEP, BAKUP POWER

Interrupt management

- Nested vector interrupt controller (NVIC) with 32 interrupt sources

Timers

- Watchdog Timer, Watch Timer
- 16-bit 4ch general purpose timers
  - — Periodic, one-shot, PWM, capture mode
- 32-bit 2ch general purpose timers
  - — Periodic, one-shot, PWM, capture mode
- 16-bit 1ch timer for 3-phase PWM output
- 16-bit 1ch timer for 3ch input capture

Communication interfaces

- External communication ports
  - — 4 USART (UART + SPI),
  - — 2 I2Cs, 2 SPIs
  - — Full-Speed USB, External Bus Interface.
- Supports USART (UART + SPI) ISP

1Msps 12-bit ADC

- 16-channels inputs

10-bit DAC

Comparator

- 2-channels, Internal Reference Voltage

CRC generator

- CRC-CCITT, CRC-16

Temperature Sensor

Development support

- SWD debug interface

Four types of package options

- LQFP 64 (10 x 10, 0.5mm pitch)
- LQFP 48 (7 x 7, 0.5mm pitch)
- QFN 48 (5 x 5, 0.55T)

Operating temperature

- Commercial grade (-40℃ to +85℃)

Product selection table

Table 1. GPIO Alternative Function

Part number	Flash	SRAM	SPI	USART	I2C	TIMER	PWM	ADC	I/O Ports	Package
A31G324RLN	128KB	16KB	2	4	2	6(16-bit)/2(32-bit)	8	16	51	LQFP 64
A31G324CLN*	128KB	16KB	2	3	2	6(16-bit)/2(32-bit)	8	10	37	LQFP 48
A31G324CUN*	128KB	16KB	2	3	2	6(16-bit)/2(32-bit)	8	10	37	QFN 48
A31G323RLN*	64KB	16KB	2	4	2	6(16-bit)/2(32-bit)	8	16	51	LQFP 64
A31G323CLN*	64KB	16KB	2	3	2	6(16-bit)/2(32-bit)	8	10	37	LQFP 48
A31G323CUN*	64KB	16KB	2	3	2	6(16-bit)/2(32-bit)	8	10	37	QFN 48

For available options or further information on the devices with "*" marks, please contact the ABOV sales offices.

Reference document

- Document 'DDI 0484C' is provided by ARM and contains information of Cortex-M0+.
- A31G32x User's Manual is provided by ABOV and available at www.abovsemi.com.

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1 Description

A31G32x lines are 32-bit general purpose microcontrollers with up to 128 Kbytes of flash memory. They are powerful microcontrollers which provide effective solutions to various electrical appliances which require both low power consumption and high performance.

1.1 Device overview

In this section, features of A31G32x and peripheral counts are introduced.

Table 2. A31G324 and A31G323 Device Features and Peripheral Counts

Peripherals		Description
Core	CPU	High Performance Low-Power Cortex-M0+ Core 32-bit ARM Cortex-M0+ CPU
	Interrupt	NVIC (Nested-Vectored Interrupt Controller) Up to 32 peripheral interrupts supported.
Memory	Code flash	A31G324: 128Kbytes code flash memory A31G323: 64Kbytes code flash memory Flash access wait 0 clock wait: up to 20MHz 1 clock wait: up to 40MHz 2 clock wait: up to 48MHz
	SRAM	16 Kbytes SRAM (0 wait)
	Endurance	10,000 times at room temperature Retention for 10 years
System Control Unit (SCU)	Operating frequency	Up to 48 MHz
	Clock	High speed internal oscillator (HSI) 48MHz (±3% @-40℃ to +85℃) Low speed internal oscillator (LSI) 750KHz (±20% @-40℃ to +85℃) 40KHz (±50% @-40℃ to +85℃) External main oscillator (HSE): 2MHz to 16MHz External sub-oscillator (LSE): 32.768KHz Phase-locked loop (PLL) frequency generator generates a high-speed clock (up to 144MHz)
	Clock monitoring	System Fail-Safe function by Clock Monitoring External main oscillator(HSE) External sub oscillator(LSE) Main system clock (MCLK)

Table 2. A31G324 and A31G323 Device Features and Peripheral Counts (continued)

Peripherals		Description
	Operating mode	RUN mode SLEEP mode STOP mode STANDBY mode Backup Power mode
	Reset	nRESET pin reset Core reset Software reset POR (Power On Reset) LVR (Low Voltage Reset) WDTR (Watch Dog Timer Reset) Reset due to clock oscillating error
General Purpose I/O (GPIO)		51 Ports (PA[15:0], PB[15:0], PC[15:0], PF[2:0]): 64-Pin 37 Ports (PA[15:0], PB[15:0], PC[15:13], PF[1:0]): 48-Pin
Direct Memory Access Controller (DMA)		4-ch direct memory access (DMA) support peripherals SPI20, SPI21, USART10, USART11, USART12, USART13, CRC, ADC
Watch Timer (WT)		14-bit divider with extended 12-bit counter 1-ch
Watchdog Timer (WDT)		24-bit down counter timer: 1-ch Reset and periodic interrupts are supported
TIMER	Timer1x	16bit: 4-ch Periodic timer mode, One-shot timer mode, PWM pulse mode, Capture mode
	Timer2x	32bit : 2-ch Periodic timer mode, One-shot timer mode, PWM pulse mode, Capture mode
	Timer40	16bit : 1-ch Periodic timer mode, One-shot timer mode, PWM pulse mode, 3-Phase Capture mode
PWM	Timer30	16bit : 6-ch Periodic timer mode, Back-to-Back mode, Capture mode

Table 2. A31G324 and A31G323 Device Features and Peripheral Counts (continued)

Peripherals		Description
Communication function	USART	4-ch
	SPI	2-ch
	I2C	2-ch
	USB	Full speed 2.0 device
ADC		12-bit ADC : 1Msps 64-pin : 16-ch 48-pin : 10-ch
DAC		10-bit DAC 1-ch PA4, PA5: output pin
External Bus Interface (EBI)		20-bit address size, 16-bit multiplexed address/data bus
CRC calculator (CRC)		CRC-CCITT, CRC-16
Comparator		8-ch reference input 2-ch output comparator Window mode
Operating Voltage		1.8V to 5.5V
Operating temperature		Commercial grade (-40℃ to +85℃)
Package		Three types of package options 48-pin QFN 48-pin LQFP 64-pin LQFP

1.2 Block diagram

In this section, A31G32x devices with peripherals are described in block diagram.

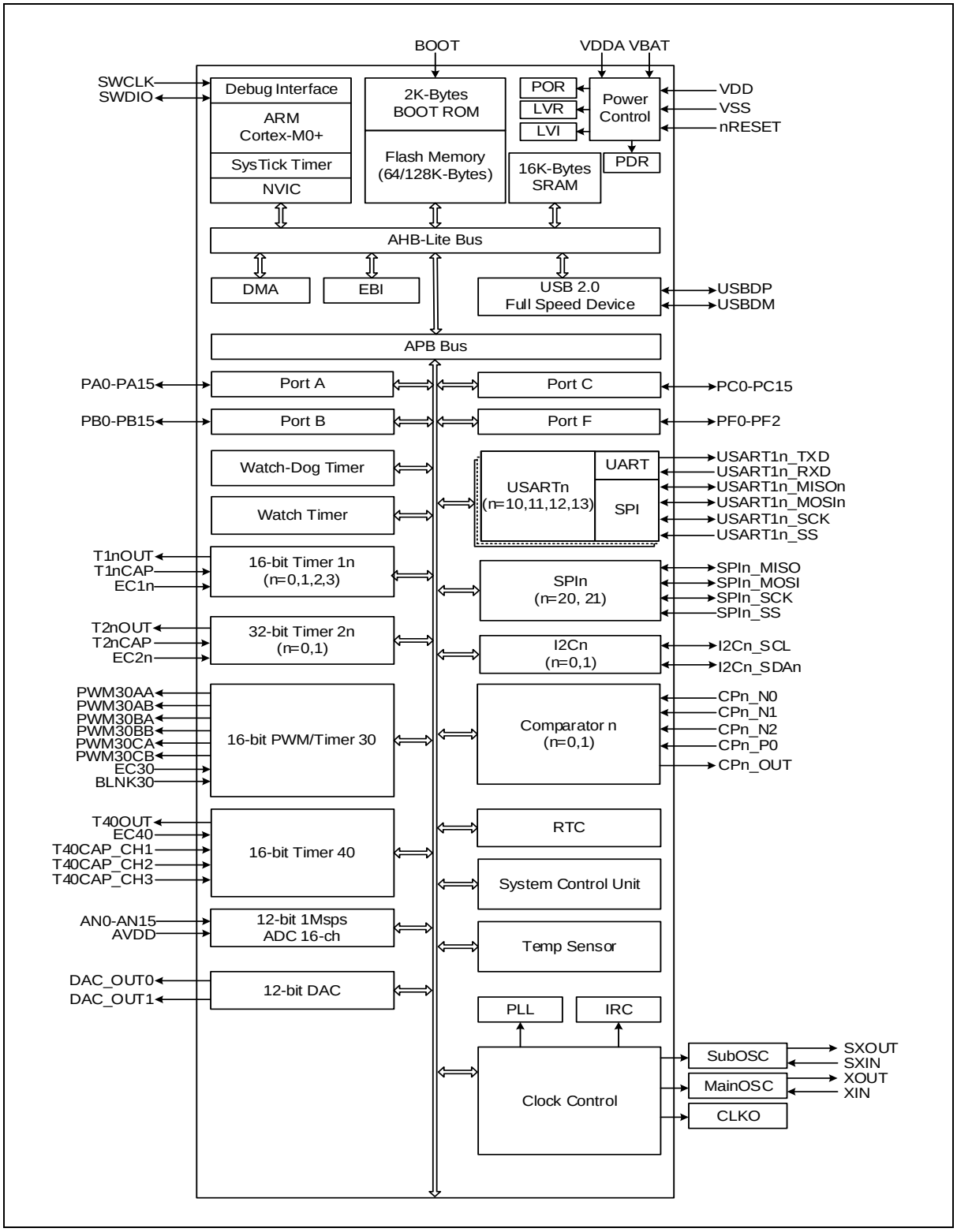


Figure 1. A31G32x Block diagram

2. Pinouts and pin descriptions

In this chapter, A31G32x devices' pinouts and pin descriptions are introduced.

2.1 Pinouts

2.1.1 A31G323RLN, A31G324RLN (64 LQFP)

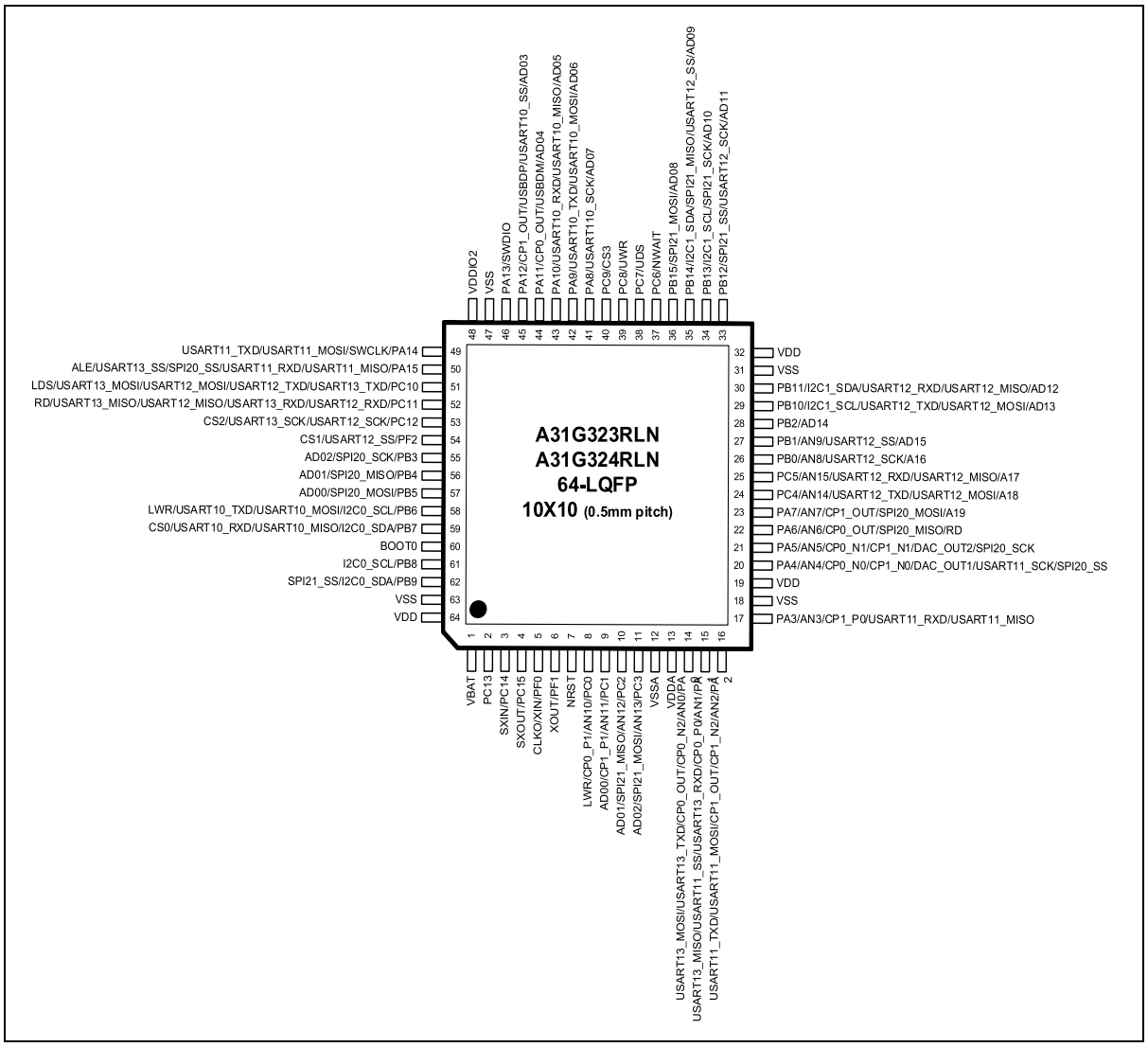


Figure 2. LQFP 64 Pinouts

2.1.2 A31G323CLN, A31G324CLN (48 LQFP)

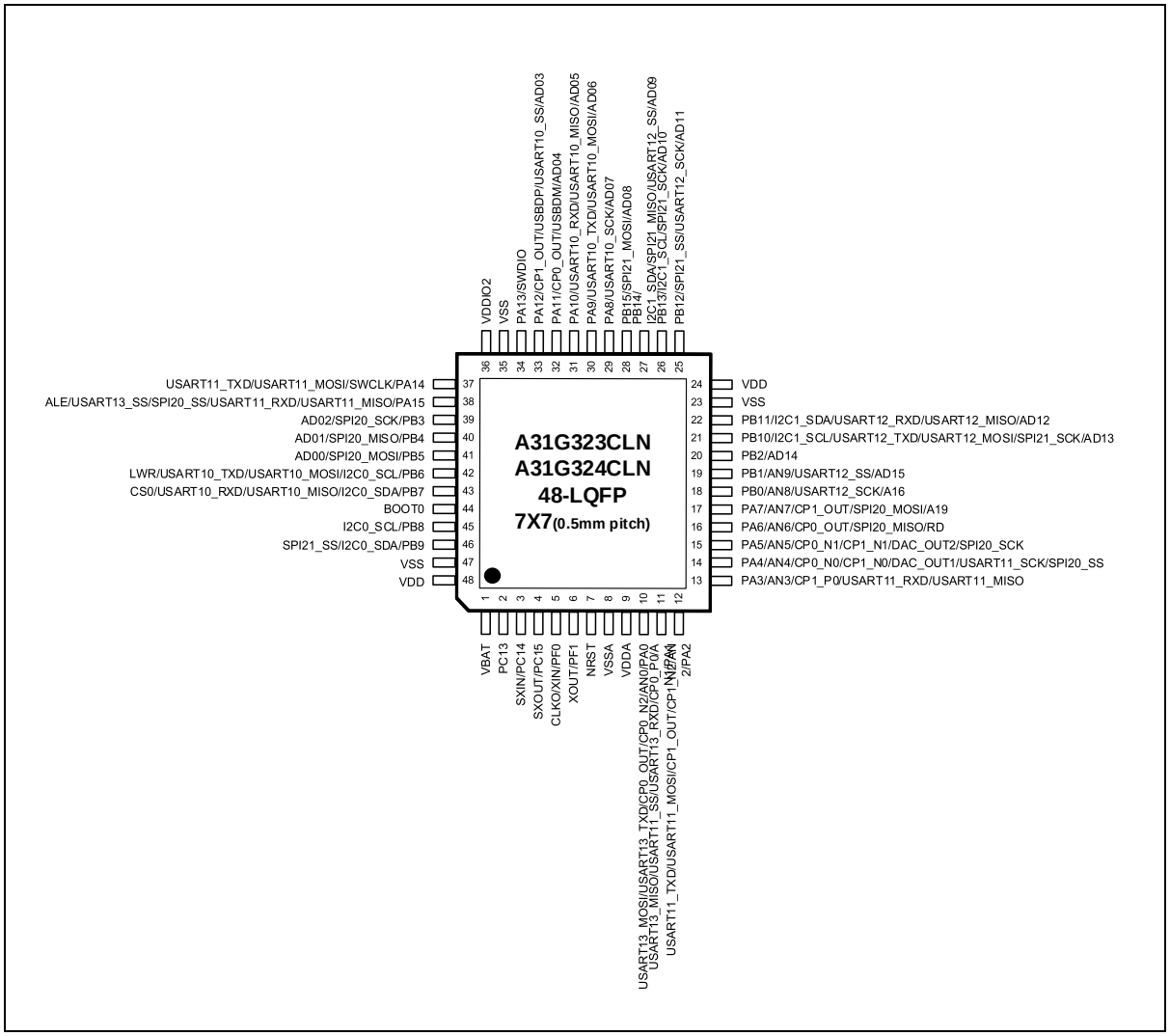
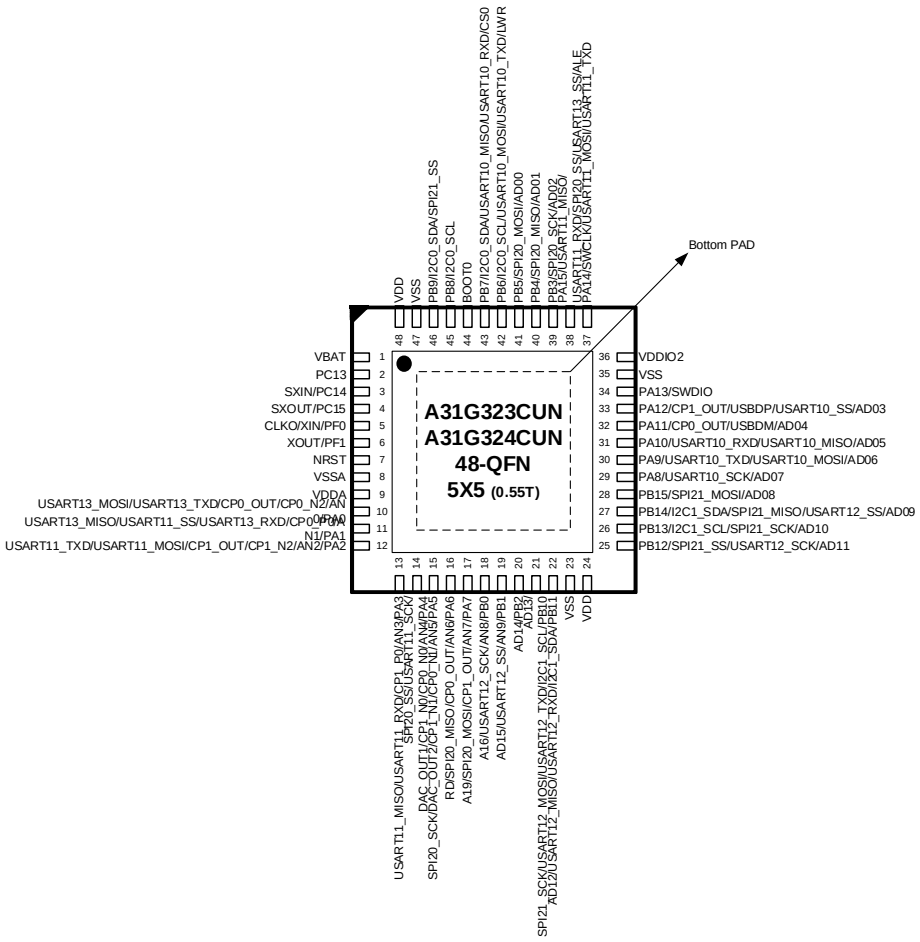


Figure 3. LQFP 48 Pinouts

2.1.3 A31G323CUN, A31G324CUN (48 QFN)



NOTE) Bottom PAD is Floating. (Connectable to VSS)

Figure 4. QFN 48 Pinouts

2.2 Pin description

Pin configuration information in Table 3 contains two pairs of power/ground and other dedicated pins. These multi-function pins have up to ten selections of functions including GPIO. Configuration including pin ordering can be changed without notice.

Table 3. Pin Description

Pin no.		Pin name	Type	Description	Remark
64-pin	48-pin				
1	1	VBAT	P	Backup Power Supply	
2	2	PC13*	IOUDS	PORT C Bit 13 Input/Output	
		RTC_TAMP1	I	RTC TimeStamp Input	
		RTC_OUT	O	RTC Output	
3	3	PC14*	IOUDS	PORT C Bit 14 Input/Output	
		SXIN	I	Sub Oscillator Input	
4	4	PC15*	IOUDS	PORT C Bit 15 Input/Output	
		SXOUT	O	Sub Oscillator Output	
5	5	PF0*	IOUDS	PORT F Bit 0 Input/Output	
		XIN	I	Main Oscillator Input	
		CLKO	O	Clock Output	
6	6	PF1*	IOUDS	PORT F Bit 1 Input/Output	
		XOUT	O	Main Oscillator Output	
7	7	nReset	IU	Reset Pin	Pull-up
8	—	PC0*	IOUDS	PORT C Bit 0 Input/Output	
		AN10	IA	ADC Input 10	
		LWR	O	EBI Lower byte write signal	
		CP0_P1	IA	Comparator 0 Positive 1 Input	
9	—	PC1*	IOUDS	PORT C Bit 1 Input/Output	
		AN11	IA	ADC Input 11	
		AD00	I/O	EBI Address/Data bus bit 0	
		CP1_P1	IA	Comparator 1 Positive 1 Input	
10	—	PC2*	IOUDS	PORT C Bit 2 Input/Output	
		SPI21_MISO	I/O	SPI Channel 21 Master Input/Slave Output	
		AN12	IA	ADC Input 12	
		AD01	I/O	EBI Address/Data bus bit 1	
11	—	PC3*	IOUDS	PORT C Bit 3 Input/Output	
		SPI21_MOSI	I/O	SPI Channel 21 Master Out / Slave In	
		AN13	IA	ADC Input 13	
		AD02	I/O	EBI Address/Data bus bit 2	
		EC13	I	Timer 13 Event Count Input	
		T13CAP	I	Timer 13 Capture Input	
		T13OUT	O	Timer 13 Output	
12	8	AVSS	P	Power supply for ADC, DAC, Comparator	

Table 3. Pin Description(continued)

Pin no.		Pin name	Type	Description	Remark
64-pin	48-pin				
13	9	AVDD	P	Power supply for ADC, DAC, Comparator	
14	10	PA0*	IOUDS	PORT A Bit 0 Input/Output	
		CP0_OUT	O	Comparator 0 Output	
		USART13_TXD	O	USART Channel 13 TXD Output	
		USART13_MOSI	I/O	USART Channel 13 Master Out / Slave In	
		AN0	IA	ADC Input 0	
		CP0_N2	IA	Comparator 0 Negative 2 Input	
		RTC_TAMP2	I	RTC TimeStamp Input	
		EC20	I	Timer 20 External Clock Input	
15	11	PA1*	IOUDS	PORT A Bit 1 Input/Output	
		USART11_SS	I/O	USART Channel 11 Slave Select Signal	
		USART13_RXD	I	USART Channel 13 RXD Input	
		USART13_MISO	I/O	USART Channel 13 Master Input/Slave Output	
		AN1	IA	ADC Input 1	
		CP0_P0	IA	Comparator 0 Positive 0 Input	
		T20OUT	O	Timer 20 Output	
		T20CAP	I	Timer 20 Capture Input	
		T13OUT	O	Timer 13 Output	
		T13CAP	I	Timer 13 Capture Input	
		EC13	I	Timer 13 External Clock Input	
16	12	PA2*	IOUDS	PORT A Bit 2 Input/Output	
		USART11_TXD	O	USART Channel 11 TXD Output	
		USART11_MOSI	I/O	USART Channel 11 Master Output/Slave Input	
		CP1_OUT	O	Comparator 1 Output	
		AN2	IA	ADC Input 2	
		CP1_N2	IA	Comparator 1 Negative 2 Input	
		T20OUT	O	Timer 20 Output	
		T20CAP	I	Timer 20 Capture Input	
		T10OUT	O	Timer 10 Output	
		T10CAP	I	Timer 10 Capture Input	
		EC10	I	Timer 10 External Clock Input	
17	13	PA3*	IOUDS	PORT A Bit 3 Input/Output	
		USART11_RXD	I	USART Channel 11 RXD Input	
		USART11_MISO	I/O	USART Channel 11 Master Input/Slave Output	
		AN3	IA	ADC Input 3	
		CP1_P0	IA	Comparator 1 Positive 0 Input	
		T20OUT	O	Timer 20 Output	
		T20CAP	I	Timer 20 Capture Input	
		T10OUT	O	Timer 10 Output	
		T10CAP	I	Timer 10 Capture Input	
		EC10	I	Timer 10 External Clock Input	

Table 3. Pin Description(continued)

Pin no.		Pin name	Type	Description	Remark
64-pin	48-pin				
18	—	VSS	P	VSS	
19	—	VDD	P	VDD	
20	14	PA4*	IOUDS	PORT A Bit 4 Input/Output	
		SPI20_SS	I/O	SPI Channel 20 Slave Select Signal	
		CP0_N0	IA	Comparator 0 Negative 0 Input	
		CP1_N0	IA	Comparator 1 Negative 0 Input	
		AN4	IA	ADC Input 4	
		USART11_SCK	I/O	USART Channel 11 Clock Input/Output	
		DAC_OUT1	O	DAC Output	
21	15	PA5*	IOUDS	PORT A Bit 5 Input/Output	
		SPI20_SCK	I/O	SPI Channel 20 Clock Input/Output	
		CP0_N1	IA	Comparator 0 Negative 1 Input	
		CP1_N1	IA	Comparator 1 Negative 1 Input	
		AN5	IA	ADC Input 5	
		EC20	I	Timer 20 External Clock Input	
		DAC_OUT2	O	DAC Output	
22	16	PA6*	IOUDS	PORT A Bit 6 Input/Output	
		SPI20_MISO	I/O	SPI Channel 20 Master-Input/Slave-Output	
		CP0_OUT	O	Comparator 0 Output	
		AN6	IA	ADC Input 6	
		BLNK30	I	External Sync Signal Input for T30 PWM	
		T40OUT	O	Timer 40 Output	
		T40CAP_CH1	I	Timer 40 CH1 Capture Input	
		T11OUT	O	Timer 11 Output	
		T11CAP	I	Timer 11 Capture Input	
		EC11	I	Timer 11 External Clock Input	
		RD	O	EBI Read signal	
23	17	PA7*	IOUDS	PORT A Bit 7 Input/Output	
		SPI20_MOSI	I/O	SPI Channel 20 Master Out / Slave In	
		CP1_OUT	O	Comparator 1 Output	
		AN7	IA	ADC Input 7	
		PWM30AB	O	Timer 30 PWM Output	
		T40OUT	O	Timer 40 Output	
		T40CAP_CH2	I	Timer 40 CH2 Capture Input	
		T12OUT	O	Timer 12 Output	
		T12CAP	I	Timer 12 Capture Input	
		EC12	I	Timer 12 External Clock Input	
		A19	O	EBI Address 19 bus signal	

Table 3. Pin Description(continued)

Pin no.		Pin name	Type	Description	Remark
64-pin	48-pin				
24	—	PC4*	IOUDS	PORT C Bit 4 Input/Output	
		USART12_TXD	O	USART Channel 12 TXD Input	
		USART12_MOSI	I/O	USART Channel 12 Master Output/Slave Input	
		AN14	IA	ADC Input 14	
		EC40	I	Timer 40 External Clock Input	
		A18	O	EBI Address 18 bus signal	
25	—	PC5*	IOUDS	PORT C Bit 5 Input/Output	
		USART12_RXD	I	USART Channel 12 RXD Input	
		USART12_MISO	I/O	USART Channel 12 Master Input/Slave Output	
		AN15	IA	ADC Input 15	
		T21CAP	I	Timer 21 Capture Input	
		T21OUT	O	Timer 21 Output	
		A17	O	EBI Address 17 bus signal	
26	18	PB0*	IOUDS	PORT B Bit 0 Input/Output	
		AN8	IA	ADC Input 8	
		PWM30BB	O	Timer 30 PWM Output	
		T21CAP	I	Timer 21 Capture Input	
		T21OUT	O	Timer 21 Output	
		T40OUT	O	Timer 40 Output	
		T40CAP_CH3	I	Timer 40 CH3 Capture Input	
		USART12_SCK	I/O	USART Channel 12 Clock Input/Output	
		A16	O	EBI Address 16 bus signal	
27	19	PB1*	IOUDS	PORT B Bit 1 Input/Output	
		AN9	IA	ADC Input 9	
		PWM30CB	O	Timer 30 PWM Output	
		USART12_SS	I/O	USART Channel 12 Slave Select Signal	
		T13OUT	O	Timer 13 Output	
		T13CAP	I	Timer 13 Capture Input	
		EC13	I	Timer 13 External Clock Input	
		AD15	I/O	EBI Address or Data 15 bus signal	
28	20	PB2*	IOUDS	PORT B Bit 2 Input/Output	
		T13OUT	O	Timer 13 Output	
		T13CAP	I	Timer 13 Capture Input	
		EC13	I	Timer 13 External Clock Input	
		AD14	I/O	EBI Address or Data 14 bus signal	

Table 3. Pin Description(continued)

Pin no.		Pin name	Type	Description	Remark
64-pin	48-pin				
29	21	PB10*	IOUDS	PORT B Bit 10 Input/Output	
		SPI21_SCK	I/O	SPI Channel 21 Clock Input/Output	
		I2C1_SCL	I/O	I2C Channel 1 SCL In/Output	
		USART12_TXD	O	USART Channel 12 TXD Input	
		USART12_MOSI	I/O	USART Channel 12 Master Output/Slave Input	
		T20OUT	O	Timer 20 Output	
		T20CAP	I	Timer 20 Capture Input	
		AD13	I/O	EBI Address or Data 13 bus signal	
30	22	PB11*	IOUDS	PORT B Bit 11 Input/Output	
		USART12_RXD	I	USART Channel 12 RXD Input	
		USART12_MISO	I/O	USART Channel 12 Master Input/Slave Output	
		I2C1_SDA	I/O	I2C Channel 1 SDA In/Output	
		T20OUT	O	Timer 20 Output	
		T20CAP	I	Timer 20 Capture Input	
		AD12	I/O	EBI Address or Data 12 bus signal	
31	23	VSS	P	VSS	
32	24	VDD	P	VDD	
33	25	PB12*	IOUDS	PORT B Bit 12 Input/Output	
		SPI21_SS	I/O	SPI Channel 21 Slave Select Signal	
		BLNK30	I	External Sync Signal Input for T30 PWM	
		USART12_SCK	I/O	USART Channel 12 Clock Input/Output	
		EC13	I	Timer 13 External Clock Input	
		T13CAP	I	Timer 13 Capture Input	
		T13OUT	O	Timer 13 Output	
		AD11	I/O	EBI Address or Data 11 bus signal	
34	26	PB13*	IOUDS	PORT B Bit 13 Input/Output	
		SPI21_SCK	I/O	SPI Channel 21 Clock Input/Output	
		I2C1_SCL	I/O	I2C Channel 1 SCL In/Output	
		PWM30AB	O	Timer 30 PWM Output	
		AD10	I/O	EBI Address or Data 10 bus signal	
35	27	PB14*	IOUDS	PORT B Bit 14 Input/Output	
		SPI21_MISO	I/O	SPI Channel 21 Master-Input/Slave-Output	
		I2C1_SDA	I/O	I2C Channel 1 SDA In/Output	
		PWM30BB	O	Timer 30 PWM Output	
		T10OUT	O	Timer 10 Output	
		T10CAP	I	Timer 10 Capture Input	
		EC10	I	Timer 10 External Clock Input	
		USART12_SS	I/O	USART Channel 12 Slave Select Signal	
		AD09	I/O	EBI Address or Data 9 bus signal	

Table 3. Pin Description(continued)

Pin no.		Pin name	Type	Description	Remark
64-pin	48-pin				
36	28	PB15*	IOUDS	PORT B Bit 15 Input/Output	
		SPI21_MOSI	I/O	SPI Channel 21 Master Out / Slave In	
		PWM30CB	O	Timer 30 PWM Output	
		T10OUT	O	Timer 10 Output	
		T10CAP	I	Timer 10 Capture Input	
		EC10	I	Timer 10 External Clock Input	
		T21CAP	I	Timer 21 Capture Input	
		T21OUT	O	Timer 21 Output	
		AD08	I/O	EBI Address or Data 8 bus signal	
37	—	PC6*	IOUDS	PORT C Bit 6 Input/Output	
		T21CAP	I	Timer 21 Capture Input	
		T21OUT	O	Timer 21 Output	
		T40OUT	O	Timer 40 Output	
		T40CAP_CH1	I	Timer 40 CH1 Capture Input	
		nWAIT	O	EBI External Wait signal	
38	—	PC7*	IOUDS	PORT C Bit 7 Input/Output	
		T40OUT	O	Timer 40 Output	
		T40CAP_CH2	I	Timer 40 CH2 Capture Input	
		UDS	O	EBI Upper Data select signal	
39	—	PC8*	IOUDS	PORT C Bit 8 Input/Output	
		T40OUT	O	Timer 40 Output	
		T40CAP_CH3	I	Timer 40 CH3 Capture Input	
		UWR	O	EBI Upper Byte write signal	
40	—	PC9*	IOUDS	PORT C Bit 9 Input/Output	
		EC40	I	Timer 40 External Clock Input	
		CS3	O	EBI memory selection signal 3	
41	29	PA8*	IOUDS	PORT A Bit 8 Input/Output	
		USART10_SCK	I/O	USART Channel 10 Clock Input/Output	
		PWM30AA	O	Timer 30 PWM Output	
		AD07	I/O	EBI Address or Data 7 bus signal	
42	30	PA9*	IOUDS	PORT A Bit 9 Input/Output	
		USART10_TXD	O	USART Channel 10 TXD Input	
		USART10_MOSI	I/O	USART Channel 10 Master Output/Slave Input	
		PWM30BA	O	Timer 30 PWM Output	
		AD06	I/O	EBI Address or Data 6 bus signal	
43	31	PA10*	IOUDS	PORT A Bit 10 Input/Output	
		USART10_RXD	I	USART Channel 10 RXD Input	
		USART10_MISO	I/O	USART Channel 10 Master Input/Slave Output	
		PWM30CA	O	Timer 30 PWM Output	
		EC21	I	Timer 21 External Clock Input	
		AD05	I/O	EBI Address or Data 5 bus signal	

Table 3. Pin Description(continued)

Pin no.		Pin name	Type	Description	Remark
64-pin	48-pin				
44	32	PA11*	IOUDS	PORT A Bit 11 Input/Output	
		CP0_OUT	O	Comparator 0 Output	
		USBDM	I/O	USB Data Line Minus	
		AD04	I/O	EBI Address or Data 4 bus signal	
45	33	PA12*	IOUDS	PORT A Bit 12 Input/Output	
		CP1_OUT	O	Comparator 2 Output	
		USBDP	I/O	USB Data Line Plus	
		EC30	I	Timer 30 External Clock Input	
		USART10_SS	I/O	USART Channel 10 Slave Select Signal	
		T30CAP	I	Timer 30 Capture Input	
		AD03	I/O	EBI Address or Data 3 bus signal	
46	34	PA13	IOUDS	PORT A Bit 13 Input/Output	
		SWDIO*	I/OU	SWD Data Input/Output	Pull-up
47	35	VSS	P	VSS	
48	36	VDDIO2	P	VDD	
49	37	PA14	IOUDS	PORT A Bit 14 Input/Output	
		USART11_TXD	O	USART Channel 11 TXD Output	
		USART11_MOSI	I/O	USART Channel 11 Master Output/Slave Input	
		SWCLK*	IU	SWD Clock Input	Pull-up
50	38	PA15*	IOUDS	PORT A Bit 15 Input/Output	
		USART13_SS	I/O	USART Channel 13 Slave Select Signal	
		USART11_RXD	I	USART Channel 11 RXD Input	
		USART11_MISO	I/O	USART Channel 11 Master Input/Slave Output	
		SPI20_SS	I/O	SPI Channel 20 Slave Select Signal	
		EC21	I	Timer 21 External Clock Input	
		ALE	O	EBI Address Latch signal	
51	—	PC10*	IOUDS	PORT C Bit 10 Input/Output	
		USART12_TXD	O	USART Channel 12 TXD Output	
		USART12_MOSI	I/O	USART Channel 12 Master Output/Slave Input	
		USART13_TXD	O	USART Channel 13 TXD Output	
		USART13_MOSI	I/O	USART Channel 13 Master Output/Slave Input	
		LDS	O	EBI Lower Data select signal	
52	—	PC11*	IOUDS	PORT C Bit 11 Input/Output	
		USART12_RXD	I	USART Channel 12 RXD Input	
		USART12_MISO	I/O	USART Channel 12 Master Input/Slave Output	
		USART13_RXD	I	USART Channel 13 RXD Input	
		USART13_MISO	I/O	USART Channel 13 Master Input/Slave Output	
		EC21	I	Timer 21 External Clock Input	
		RD	O	EBI Read signal	

Table 3. Pin Description(continued)

Pin no.		Pin name	Type	Description	Remark
64-pin	48-pin				
53	—	PC12*	IOUDS	PORT C Bit 12 Input/Output	
		USART12_SCK	I/O	USART Channel 12 Clock Input/Output	
		USART13_SCK	I/O	USART Channel 13 Clock Input/Output	
		CS2	O	EBI memory selection signal 2	
54	—	PF2*	IOUDS	PORT F Bit 2 Input/Output	
		USART12_SS	I/O	USART Channel 12 Slave Select Signal	
		EC40	I	Timer 40 External Clock Input	
		T21CAP	I	Timer 21 Capture Input	
		T21OUT	O	Timer 21 Output	
		CS1	O	EBI memory selection signal 1	
55	39	PB3*	IOUDS	PORT B Bit 3 Input/Output	
		SPI20_SCK	I/O	SPI Channel 20 Clock Input/Output	
		T20OUT	O	Timer 20 Output	
		T20CAP	I	Timer 20 Capture Input	
		AD02	I/O	EBI Address or Data 2 bus signal	
56	40	PB4*	IOUDS	PORT B Bit 4 Input/Output	
		SPI20_MISO	I/O	SPI Channel 20 Master-Input/Slave-Output	
		T40OUT	O	Timer 40 Output	
		T40CAP_CH1	I	Timer 40 CH1 Capture Input	
		AD01	I/O	EBI Address or Data 1 bus signal	
57	41	PB5*	IOUDS	PORT B Bit 5 Input/Output	
		SPI20_MOSI	I/O	SPI Channel 20 Master Out / Slave In	
		T40OUT	O	Timer 40 Output	
		T40CAP_CH2	I	Timer 40 CH2 Capture Input	
		T21CAP	I	Timer 21 Capture Input	
		T21OUT	O	Timer 21 Output	
		AD00	I/O	EBI Address or Data 0 bus signal	
58	42	PB6*	IOUDS	PORT B Bit 6 Input/Output	
		I2C0_SCL	O	I2C Channel 0 SCL In/Output	
		USART10_TXD	O	USART Channel 10 TXD Output	
		USART10_MOSI	I/O	USART Channel 10 Master Output/Slave Input	
		T11OUT	O	Timer 11 Output	
		T11CAP	I	Timer 11 Capture Input	
		EC11	I	Timer 11 External Clock Input	
		T40CAP_CH3	I	Timer 40 CH3 Capture Input	
		T40OUT	O	Timer 40 Output	
		LWR	O	EBI Lower Byte Write signal	

Table 3. Pin Description(continued)

Pin no.		Pin name	Type	Description	Remark
64-pin	48-pin				
59	43	PB7*	IOUDS	PORT B Bit 7 Input/Output	
		I2C0_SDA	I/O	I2C Channel 0 SDA In/Output	
		USART10_RXD	I	USART Channel 10 RXD Input	
		USART10_MISO	I/O	USART Channel 10 Master Input/Slave Output	
		T12OUT	O	Timer 12 Output	
		T12CAP	I	Timer 12 Capture Input	
		EC12	I	Timer 12 External Clock Input	
		CS0	O	EBI memory selection signal 0	
60	44	BOOT0	IU	Boot Mode Selection Input	Pull-up
61	45	PB8*	IOUDS	PORT B Bit 8 Input/Output	Pull-up
		I2C0_SCL	I/O	I2C Channel 0 SCL In/Output	
		T11OUT	O	Timer 11 Output	
		T11CAP	I	Timer 11 Capture Input	
		EC11	I	Timer 11 External Clock Input	
62	46	PB9*	IOUDS	PORT B Bit 9 Input/Output	Pull-up
		SPI21_SS	I/O	SPI Channel 21 Slave Select Signal	
		I2C0_SDA	I/O	I2C Channel 0 SDA In/Output	
		T12OUT	O	Timer 12 Output	
		T12CAP	I	Timer 12 Capture Input	
		EC12	I	Timer 12 External Clock Input	
63	47	VSS	P	VSS	
64	48	VDD	P	VDD	

NOTES:

1. I=Input, O=Output, U=Pull-up, D=Pull-down, S=Schmitt-Trigger Input Type, C=CMOS Input Type, A=Analog, P=Power
2. The * means ‘selected pin function after reset condition’.
3. Pin order may be changed with revision notice.
4. BOOT0, nRESET, PA13 (SWDIO), PA14 (SWCLK), PB8, and PB9 are the default pull-up pins.

3. System and memory overview

3.1 System architecture

Main system of A31G32x series consists of the followings:

- ARM® Cortex® -M0+ core
- General purpose DMA
- Internal SRAM
- Internal Flash memory
- Two AHB buses

3.1.1 Cortex-M0+ Core

The ARM® Cortex®-M0+ processor is the most energy-efficient ARM processor available. It builds on the very successful Cortex-M0+ processor, retaining full instruction set and tool compatibility, while further reducing energy consumption and increasing performance. Document “DDI 0484C” from ARM provides detail information of Cortex-M0+.

3.1.2 Interrupt controller

Table 4. Interrupt Vector Map

Priority	Vector Address	Interrupt Source
-16	0x0000_0000	Stack Pointer
-15	0x0000_0004	Reset Address
-14	0x0000_0008	NMI Handler
-13	0x0000_000C	Hard Fault Handler
-12	0x0000_0010	Reserved
-11	0x0000_0014	
-10	0x0000_0018	
-9	0x0000_001C	
-8	0x0000_0020	
-7	0x0000_0024	
-6	0x0000_0028	
-5	0x0000_002C	SVCall Handler
-4	0x0000_0030	Reserved
-3	0x0000_0034	
-2	0x0000_0038	PenSV Handler
-1	0x0000_003C	SysTick Handler

Table 4. Interrupt Vector Map (continued)

Priority	Vector Address	Interrupt Source
0	0x0000_0040	LVR
1	0x0000_0044	SYSCLKFAIL
2	0x0000_0048	WDT
3	0x0000_004C	GPIOA, GPIOB
4	0x0000_0050	GPIOC, GPIOF
5	0x0000_0054	Reserved
6	0x0000_0058	Reserved
7	0x0000_005C	TIMER10
8	0x0000_0060	TIMER11
9	0x0000_0064	TIMER12
10	0x0000_0068	I2C0
11	0x0000_006C	USART10
12	0x0000_0070	WT
13	0x0000_0074	TIMER30
14	0x0000_0078	I2C1
15	0x0000_007C	TIMER20
16	0x0000_0080	TIMER21
17	0x0000_0084	USART11
18	0x0000_0088	ADC
19	0x0000_008C	SPI20
20	0x0000_0090	SPI21
21	0x0000_0094	TIMER13
22	0x0000_0098	TIMER40
23	0x0000_009C	RTC
24	0x0000_00A0	Reserved
25	0x0000_00A4	Reserved
26	0x0000_00A8	USART12
27	0x0000_00AC	USART13
28	0x0000_00B0	TEMP-Sensor
29	0x0000_00B4	COMP
30	0x0000_00B8	USB
31	0x0000_00BC	CRC

NOTES:

1. Each interrupt has an associated priority-level register. Each of them is 2 bits wide, occupying the two MSBs of the Interrupt Priority Level Registers.

Each Interrupt Priority Level Register occupies 1 byte (8 bits).NVIC registers in the Cortex-M0+ processor can only be accessed using word-size transfers, so for each access, four Interrupt Priority Level Registers are accessed at the same time.
** __NVIC_PRIO_BITS = 2

2. Figure 5 is a caution when using Peripheral Interrupts. Interrupt don't work if only peripheral interrupts are enabled. Enable the function in core to enable interrupt.
   * __enable_irq > NVCI_EnableIRQ(Peripheral) > Each Peripheral Interrupt

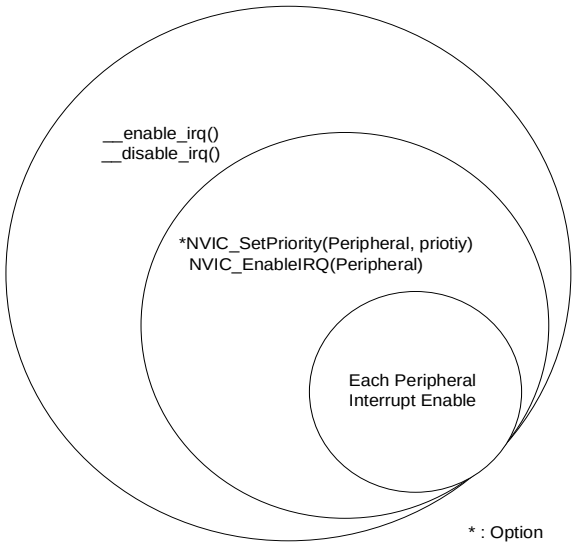


Figure 5. Interrupt Block Diagram

3.2 Memory organization

Program memory, data memory, registers and I/O ports are organized in the same address space.

3.2.1 Register boundary address

Table 5 gives the boundary addresses of peripherals in A31G32x series.

Table 5. A31G32x Memory Boundary Addresses

Boundary address	Memory area
0x4000_0000	SCU
0x4000_5100	LVI/LVR
0x4000_1000/1100/1200/1500	PCU A/B/C/F
0x4000_0100	Flash controller
0x2000_0000	Internal SRAM
0x4000_0400/0410/0420/0430	DMACH0/1/2/3
0x4000_6200	Static memory controller
0x4000_1A00	WDT
0x4000_2000	WT
0x4000_2100/2200/2300/2700	Timer 10/11/12/13
0x4000_2500/2600	Timer 20/21
0x4000_2400/2800	Timer 30/40
0x4000_3800/3900/3A00/3B00	USART 10/11/12/13
0x4000_4800/4900	I2C 0/1
0x4000_4C00/4D00	SPI 20/21
0x4000_3000	12-bit ADC
0x4000_3500	10-bit DAC
0x4000_3420	Comparator
0x4000_0300	CRC
0x5000_0000	USB
0x4000_6100	RTC
0x4000_6300	Temp sensor

3.2.2 Memory map

Figure 6 shows addressable memory space in memory map.

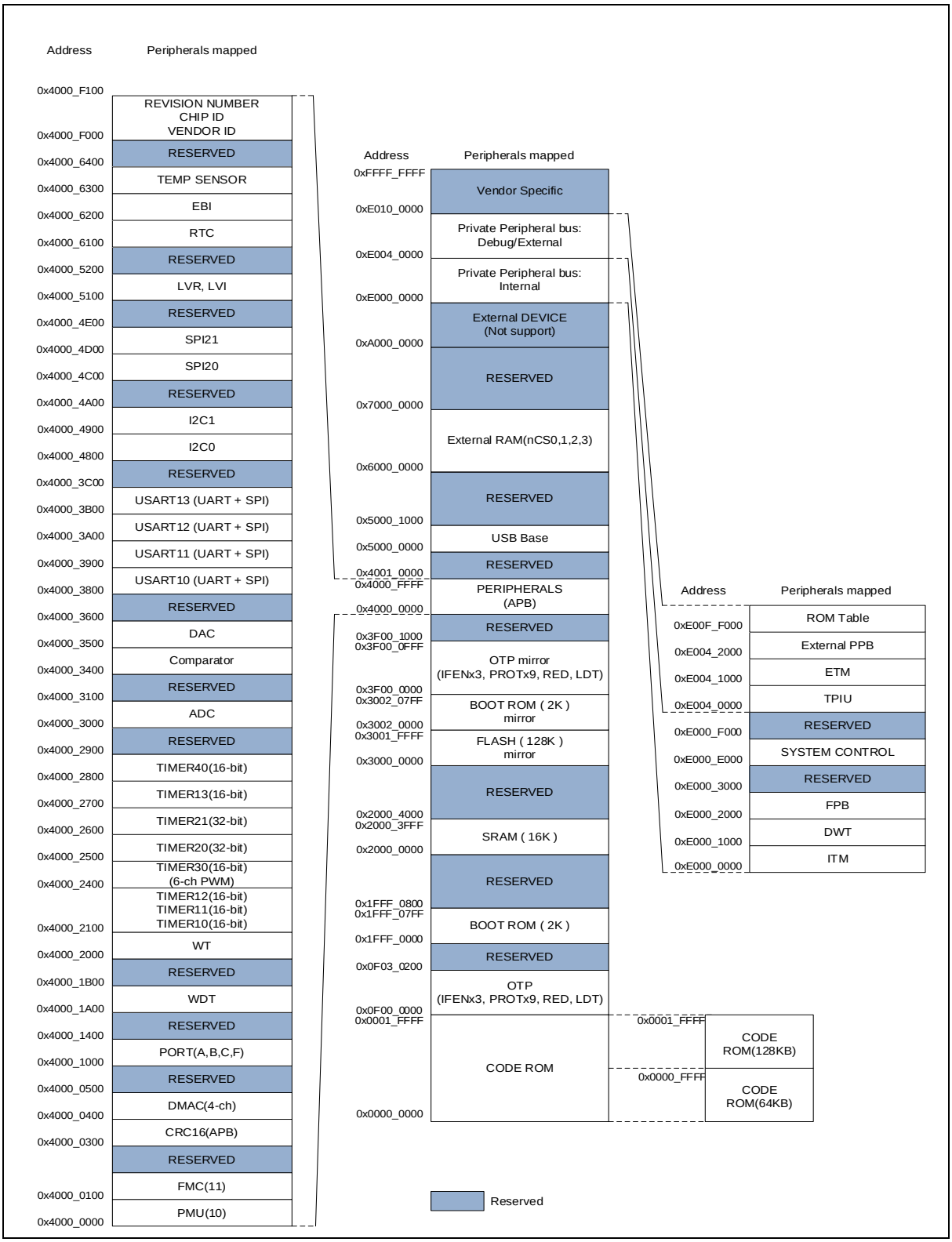


Figure 6. Memory Map

3.2.3 Embedded SRAM

A31G32x series have a block of 0-wait on-chip SRAM. The size of SRAM is 16KB and its base address is 0x2000_0000.

SRAM memory area is usually used for data memory and stack memory. Sometimes the code is dumped into the SRAM memory for fast operation or flash erase/programming operation. This device does not support memory remap strategy. So jump and return are required to perform the code in SRAM memory area.

3.2.4 Flash memory overview

A31G32x series provides internal 128KB code flash memory and its controller. This is enough to control the general system. Self-programming is available and ISP and SWD programming is also supported in boot or debugging mode.

Instruction and data cache buffer are present and overcome the low bandwidth flash memory. CPU can access flash memory with one wait state up to 48MHz bus frequency.

3.2.5 Boot mode

Boot mode pins

A31G32x series has a boot mode option to program internal flash memory. Boot mode can be entered by setting BOOT pin to 'L' at reset timing (Normal state is 'H').

Boot mode supports both of UART boot and I2C boot:

- UART boot uses USART10_TXD/USART10_RXD port or USART11_TXD/USART11_RXD.
- I2C boot uses I2C0_SCL/I2C0_SDA1 port.

The pins for boot mode are listed in Table 6.

Table 6. Boot Mode Pin List

Block	Pin Name	Dir	Description
SYSTEM	nRESET	I	Reset Input signal
	nBOOT	I	'Low' to enter Boot mode
UART mode of USART10	USART10_RXD/PA10	I	USART10 Boot Receive Data
	USART10_TXD/PA9	O	USART10 Boot Transmit Data
UART mode of USART11	USART11_RXD/PA15	I	USART11 Boot Receive Data
	USART11_TXD/PA14	O	USART11 Boot Transmit Data
I2C	I2C0_SDA/PB7	I / O	I2C0 Boot Data Input/Output
	I2C0_SCL/PB6	I	I2C0 Boot Clock Input

Boot mode connections

User can design a target board using any of boot mode ports such as I2C or UART mode of USART10, USART11. Sample connection diagrams of boot mode are introduced in the following figures:

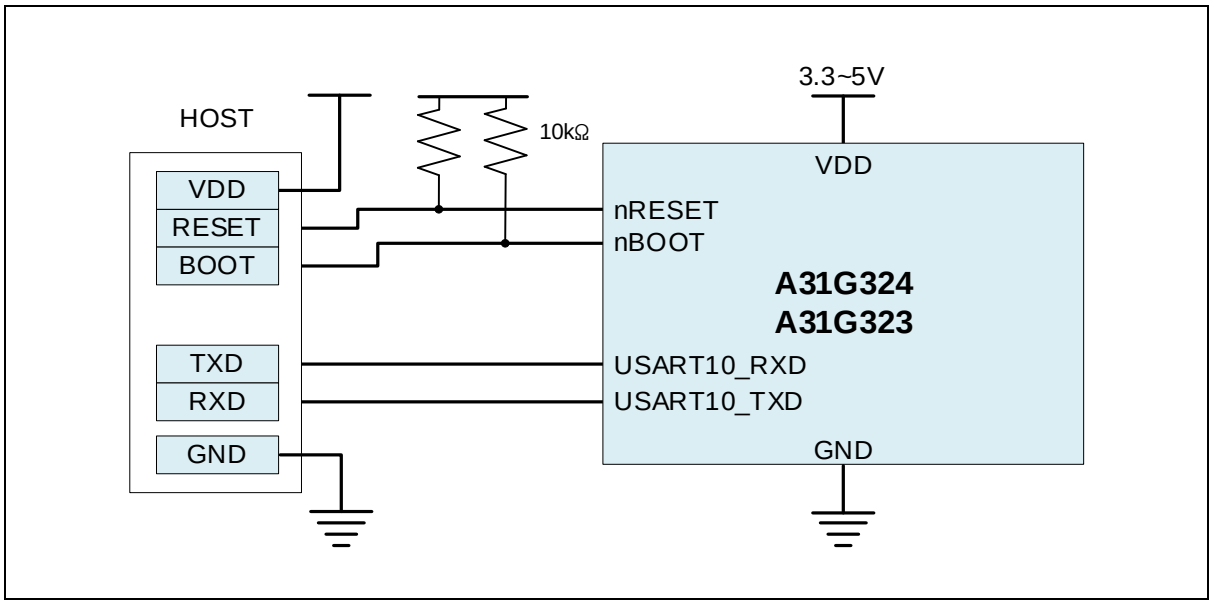


Figure 7. Connection Diagram of UART10 Boot

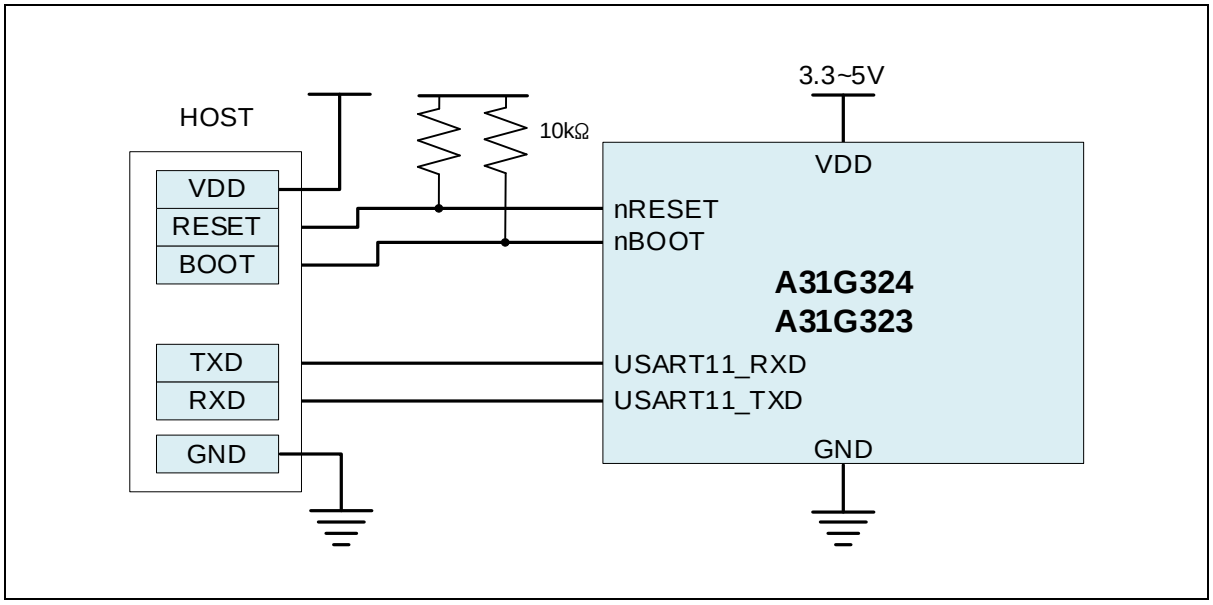


Figure 8. Connection Diagram of UART11 Boot

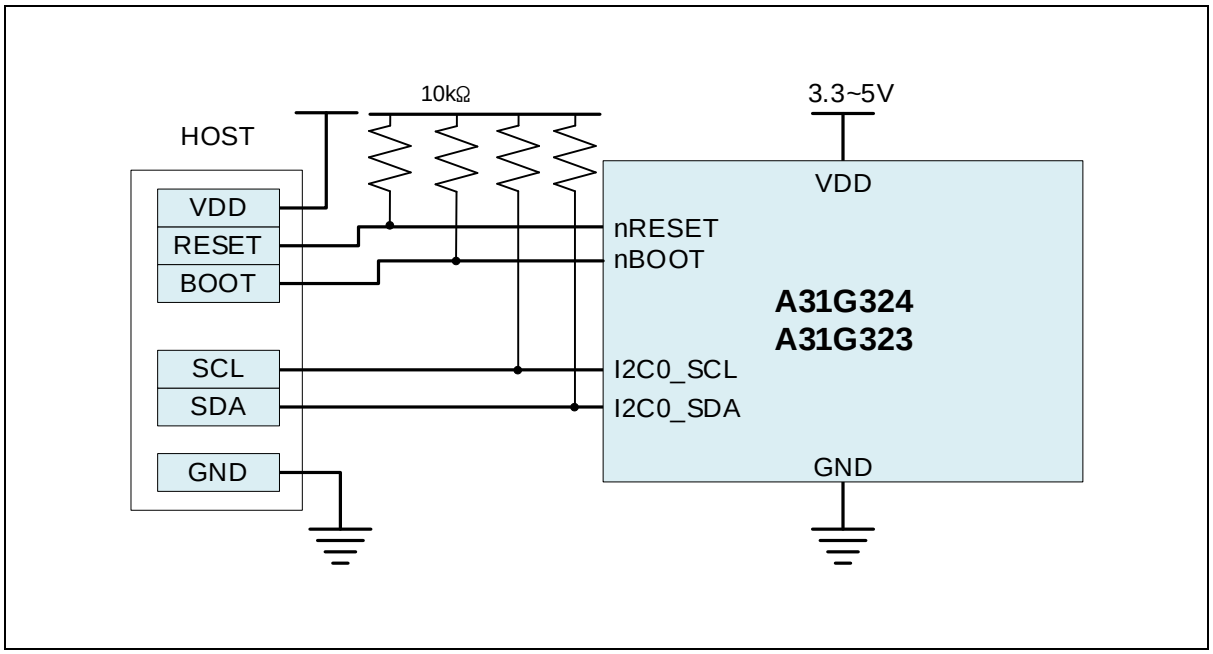
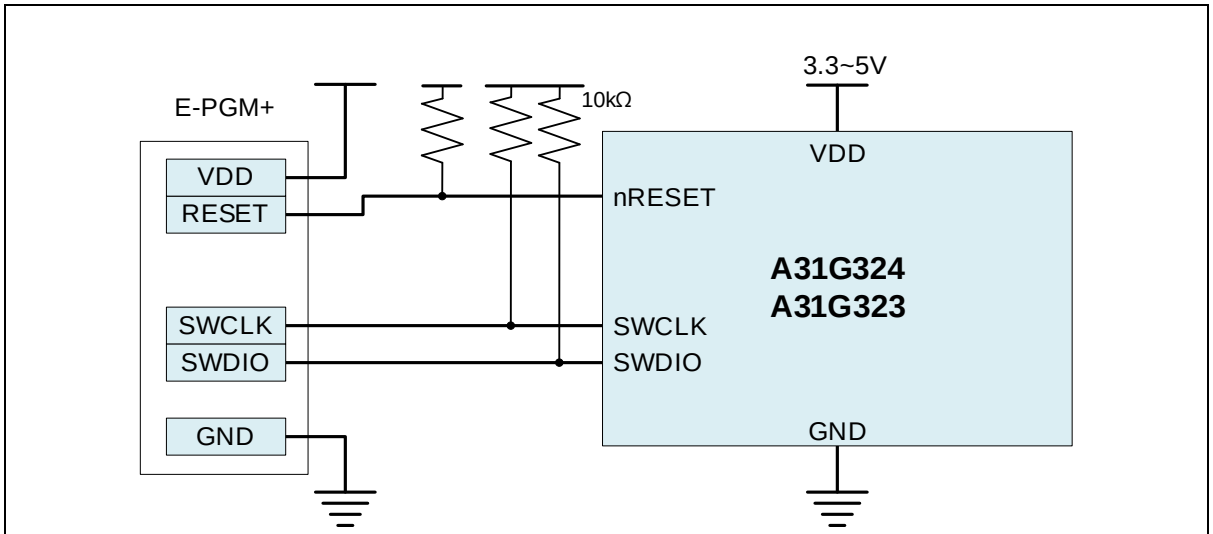


Figure 9. Connection Diagram of I2C Boot

SWD mode connections

A user can use SWD mode for writing with E-PGM+. This mode can be used for writing & debugging.



NOTES:

1. A31G32x series should not be connected to SWD mode in Boot Mode.
2. SWCLK Pin is used in Boot Mode as USART11_TXD.

Figure 10. Connection Diagram of E-PGM+ and SWD Port

4. System control unit

A31G32x series have a built-in intelligent power control block which manages system analog blocks and operating modes. System control unit (SCU) block controls an internal reset and clock signals to maintain optimize system performance and power dissipation.

Four pins in Table 7 are assigned for SCU block.

Table 7. SCU Pins

Pin name	Type	Description
nRESET	I	External Reset Input
XIN/XOUT	OSC	External Crystal Oscillator
SXIN/SXOUT	OSC	External sub-Crystal Oscillator
CLKO	O	Clock Output Monitoring Signal

4.1 SCU block diagram

In this subsection, SCU block diagram is introduced in Figure 11.

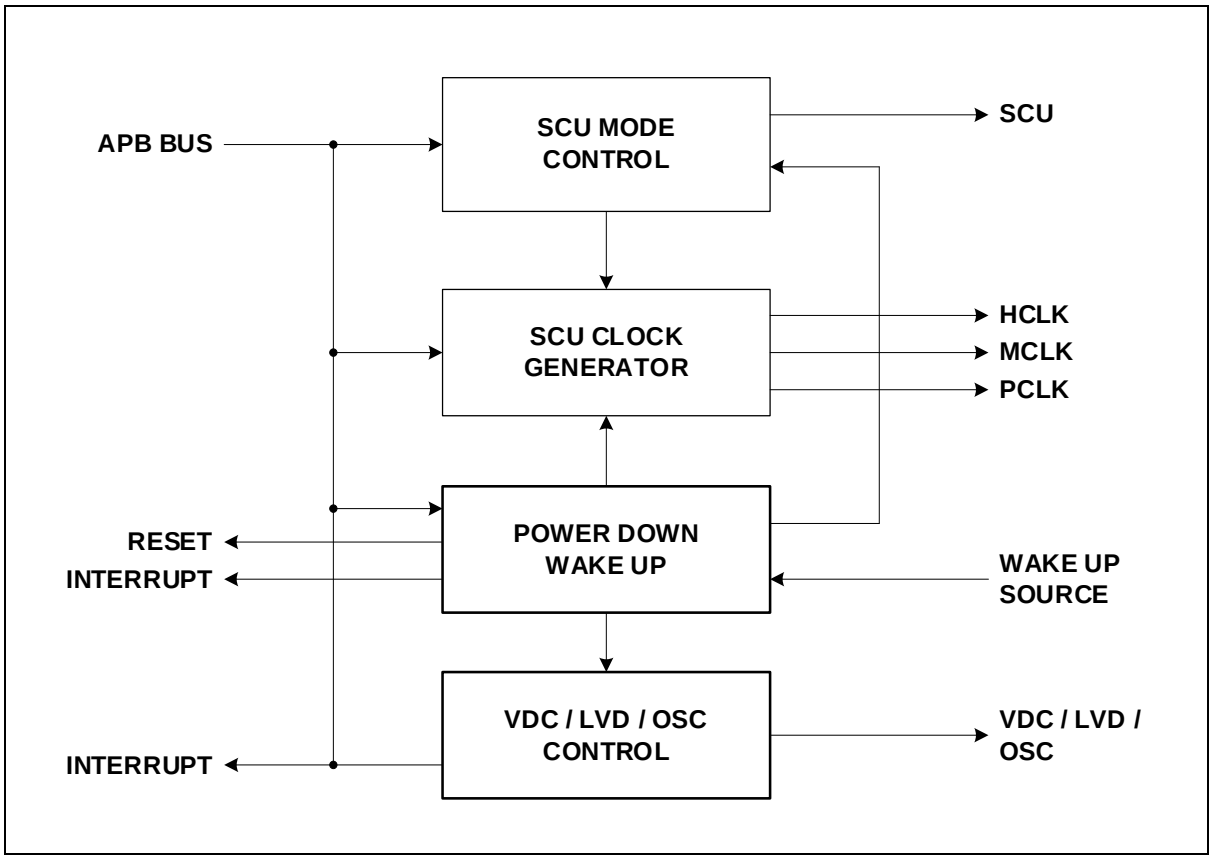


Figure 11. SCU Block diagram

4.2 Clock system

A31G32x series have two main operating clocks. One is HCLK which produces a clock signal both for CPU and AHB bus system. The other is PCLK which produces a clock signal for peripheral systems.

A user can keep the clock system variation under software control. Through Figure 12 and Table 8, users learn about the clock system of A31G32x devices and clock sources.

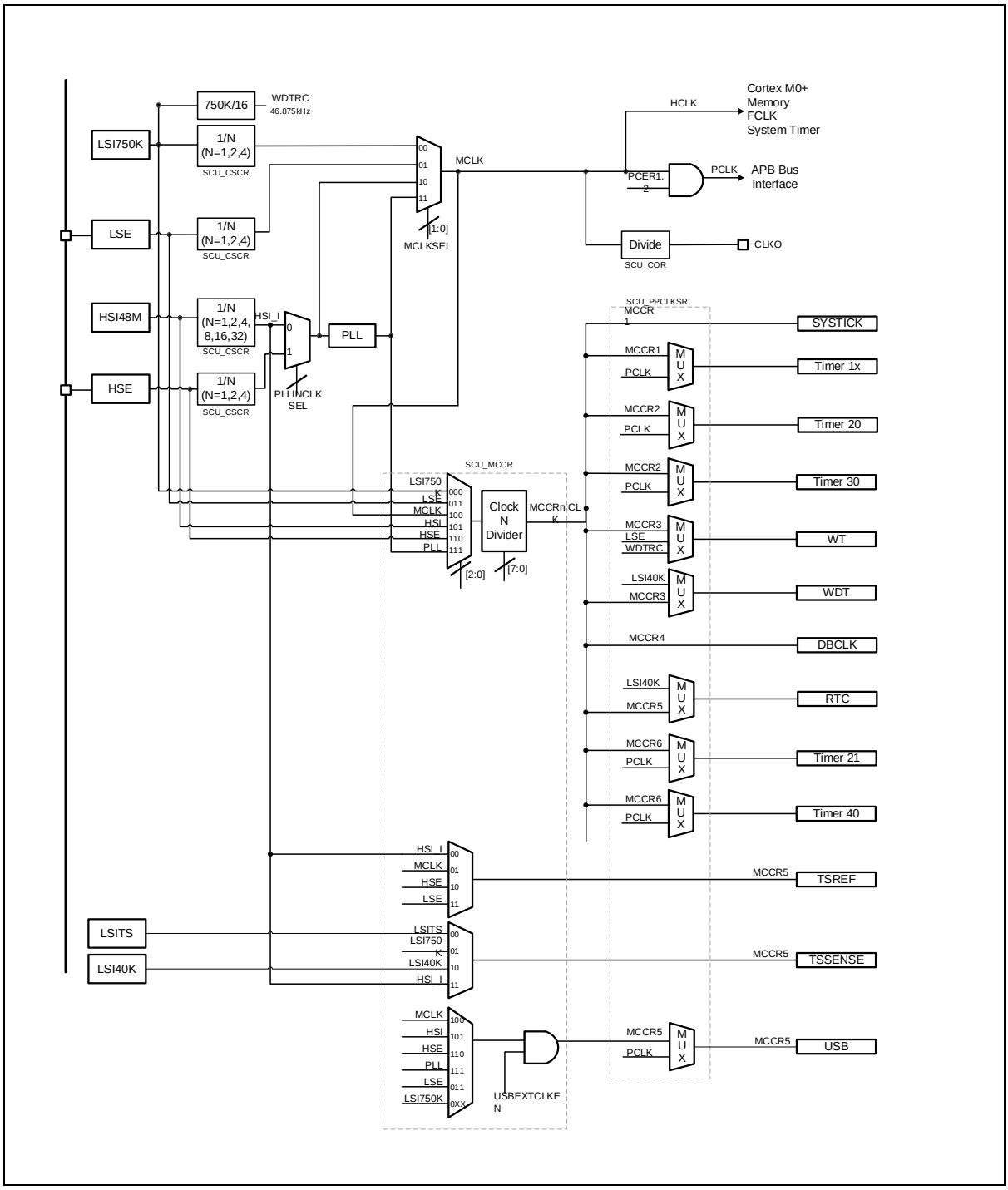


Figure 12. Clock Tree Configuration

All multiplexers switching clock sources have a glitch-free circuit in each. So a clock can be switched without glitch risks. When a user tries to change a clock mux control, both of clock sources must be alive. If one of them is not alive, clock change operation is stopped and system will be halted and not be recovered.

Table 8. Clock Sources

Clock name	Frequency	Description
HSE	2-16 MHz	High Speed External Oscillator
LSE	32.768 kHz	Low Speed External Oscillator
HSI	48 MHz	High Speed Internal OSC
LSI750K	750 kHz	Low Speed Internal OSC
LSI40K	40 kHz	Low Speed Internal OSC
LSITS	—	Internal OSC for temp sensor

4.2.1 HCLK clock domain

HCLK clock feeds the clock to the CPU and the AHB bus. Cortex-M0+ CPU requires 2 clocks related with FCLK and HCLK. FCLK is free running clock and it is always running except in power down mode. HCLK can be stopped in SLEEP mode and power down mode.

BUS system and memory systems are operated by MCLK clock. Maximum bus operating clock speed is 48MHz.

4.2.2 PCLK clock domain

PCLK is the master clock of all peripherals. Each peripheral clock is enabled by SCU_PCER1, and SCU_PCER2 registers can be used by each peripheral. Before enabling the PCLK input clock of each block, it can't be accessible even reading its registers. It can be stopped in power down mode.

4.2.3 Clock configuration procedure

After powering up, the default system clock is fed by LSI750K (750KHz) clock. By default LSI750K is enabled at power up sequence. The other clock sources will be enabled by user controls with the LSI750K system clock.

HSI48M (48MHz) clock can be enabled by SCU_CSCR register.

HSE (2-16MHz) clock can be enabled by SCU_CSCR register. Prior to enable the HSE block, the pin mux configuration should be set for XIN, XOUT function. PF0 and PF1 pins are shared with HSE's XIN and XOUT function – PF_MOD and PF_AFSR0 registers should be configured properly. After enabling the HSE block, you must wait for more than 2ms time to ensure stable operation of crystal oscillation.

LSE (32.768KHz) clock can be enabled by SCU_CSCR register. Prior to enable the LSE block, the pin mux configuration should be set for SXIN, SXOUT function. PC14 and PC15 pins are shared with LSE's SXIN and SXOUT function – PC_MOD and PC_AFSR1 registers should be configured properly.

After enabling the LSE block, you must wait for more than 2s time to ensure stable operation of crystal oscillation. You can change an MCLK by using the SCU_SCCR register.

You can find an example flow chart configuring the system clock in Figure 13.

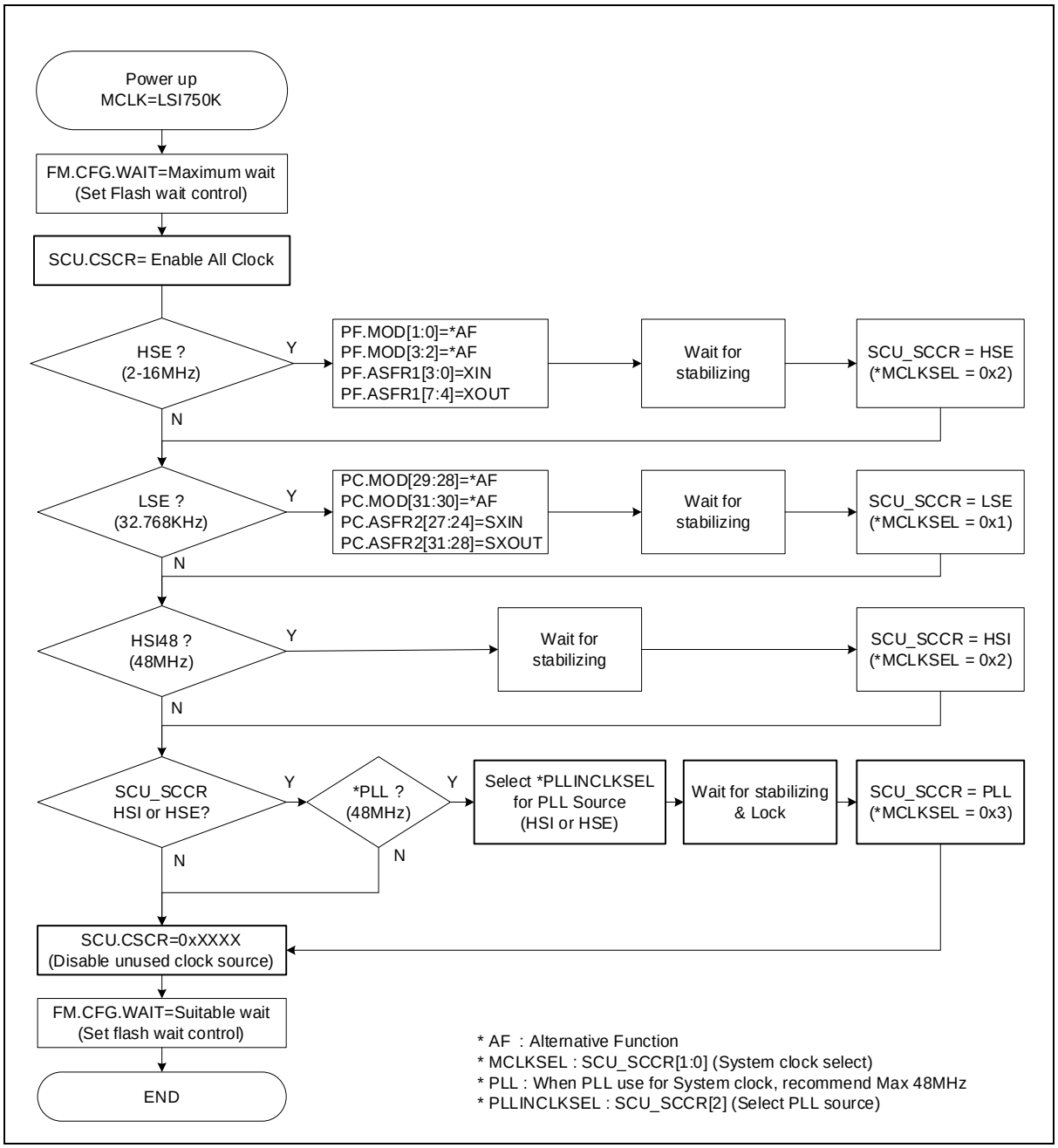


Figure 13. Clock Change Procedure

When you speed up the system clock to the maximum operating frequency, you should check flash wait control configuration. Flash read access time is one of limitation factor for performance. The wait control recommendation is suggested in Table 9.

Table 9. Flash Wait Control Recommendation

FM.CFG.WAIT	FLASH Access Wait	Available Max System clock frequency
00	0 clock wait	~20MHz
01	1 clock wait	~40MHz
10	2 clock wait	~48MHz

Figure 14 shows how to set the peripheral clock. Selecting a peripheral clock is a typical method of MCCRn and PCLK. Exceptionally WT, WDT, RTC use other clocks besides MCCRn and PCLK. (n = 1, 2, 3, 4, 5 and 6).

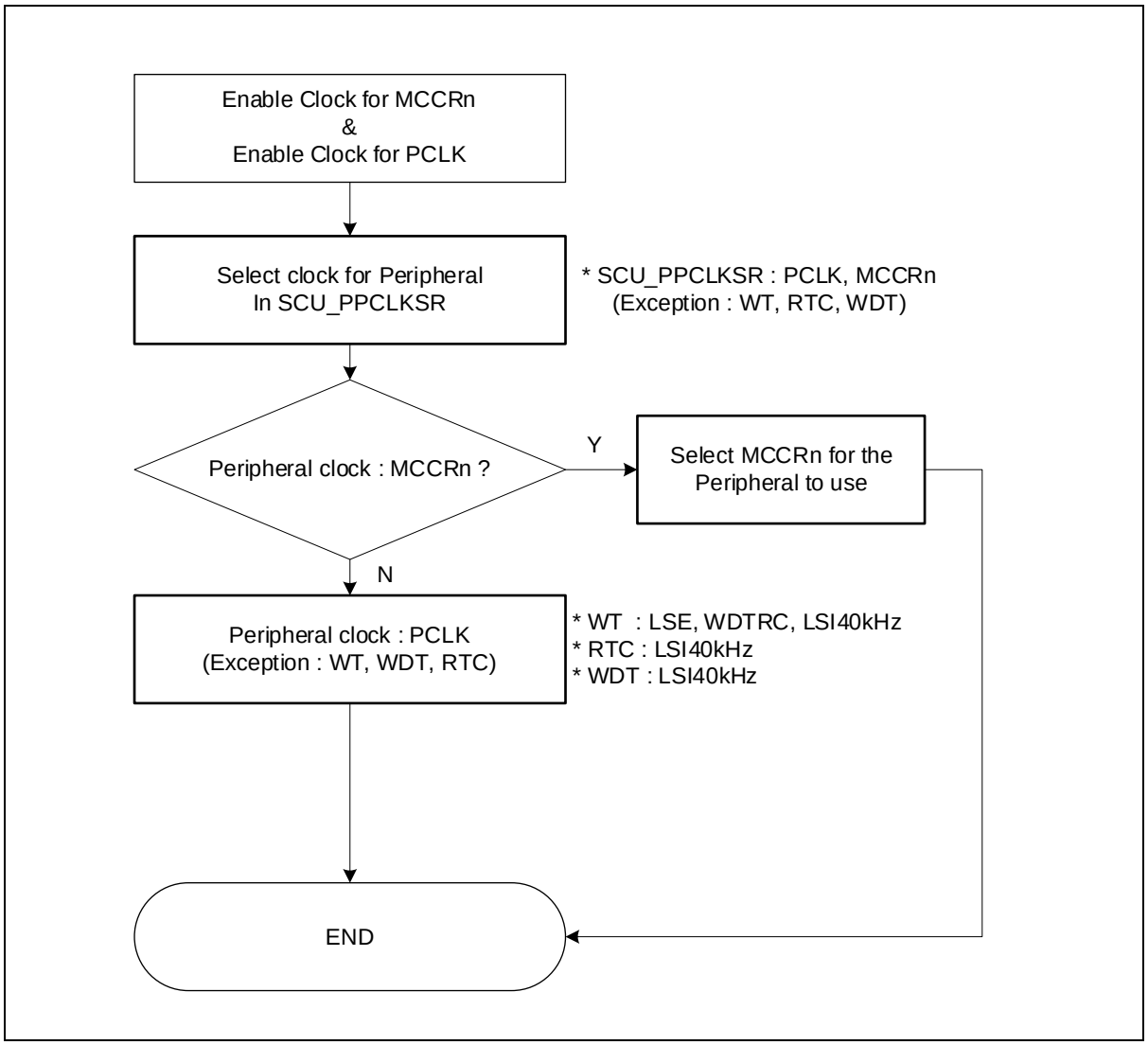


Figure 14. Peripheral Clock Select (n: 1, 2, 3, 4, 5, and 6)

Table 10. Peripheral Clock Select

Peripheral	Clock Selection		
	MCCRn	**PCLK**	**Another**
Systick	MCCR1	N/A	N/A
Timer1n		O	N/A
Timer20	MCCR2	O	N/A
Timer30		O	N/A
WT	MCCR3	N/A	WDTRC, LSE, LSI40kHz
WDT		N/A	LSI40kHz
DBCLK	MCCR4	N/A	N/A
RTC	MCCR5	N/A	LSI40kHz
TSREF		N/A	N/A
TSSENSE		N/A	N/A
USB		O	N/A
Timer40	MCCR6	O	N/A
Timer21		O	N/A

4.3 Power domain

A31G32x series have two VDCs supplying internal 1.5V power to digital circuit: one for VDD15 domain and one for backup domain.

VDD is the main power supply and VBAT is the backup power supply. A power supply switch determines which power is to be supplied (VPWRSW). In initial state, this switch selects VDD as power supply, so it isn't booted by VBAT but is booted only by VDD. To retain the contents of the backup domain when VDD is off during operation, the power supply switch selects VBAT and uses the optional STANDBY voltage provided by the battery or other source.

To improve conversion accuracy and to extend the supply flexibility, the ADC, the DAC and Comparator have an independent power supply VDDA and VSSA which can be separately filtered and shielded from noise on the PCB. The VDDA supply voltage must be greater or equal to VDD.

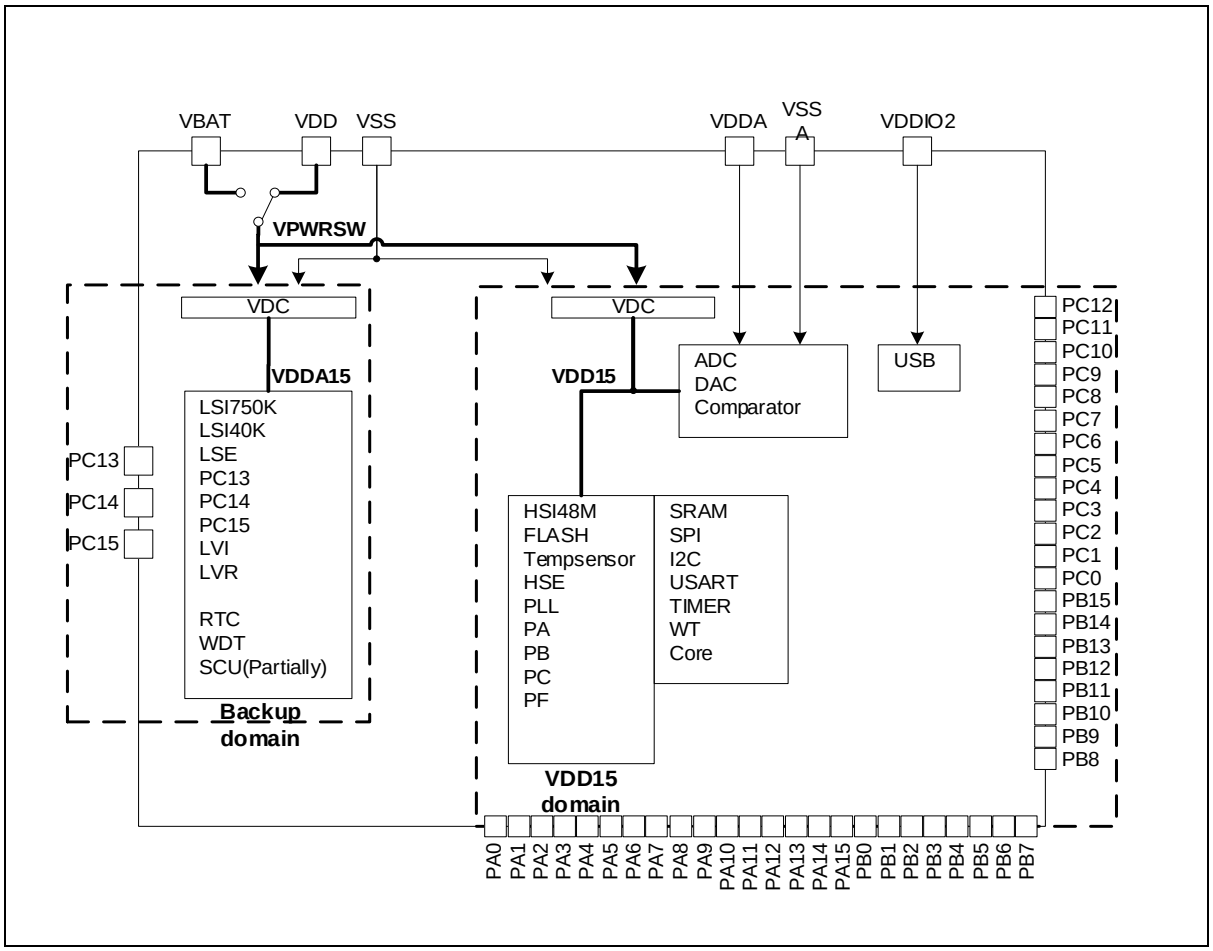


Figure 15. Power Domain Diagram

Another regulator VDC33 is embedded to supply 3.3V power to a USB. When power to the USB is supplied from outside, output of the VDC33 must be floating. VDD33_PD of SCU_VDCCON register must be set to 1 to make it floating.

4.4 Reset

A31G32x series have two system reset options. One is to cold reset that is effective during power up or down sequence. The other is warm reset which is generated by several reset sources. A reset event makes a chip to turn to an initial state. Reset sources of the cold reset and the warm reset are listed in Table 11.

Table 11. Reset Sources of Cold Reset and Warm Reset

	Cold reset	Warm reset
Reset sources	VPWRSW POR VDD15 POR LVR reset	nRESET Pin WDT reset MCLK Fail reset HSE Fail reset S/W reset CPU request reset

4.4.1 Cold reset

Cold reset is an important feature of a chip when power is up. This characteristic will affect overall system boot.

Internal VDC is enabled when VDD power is turn on. Internal POR trigger level is 1.2V of VDD voltage out level. At this time, boot operation is started. The LSI750K clock is enabled and counts 2.73msec time for internal VDC level stabilizing. In this time, VDD voltage level should be over than initial LVR level (1.63V). After 2.73msec counting, the cold reset is released and counts 0.27msec time for warm reset synchronizing. After releasing both cold and warm reset, BOOTROM and CPU are running.

Figure 16 shows power up sequence and internal reset waveforms.

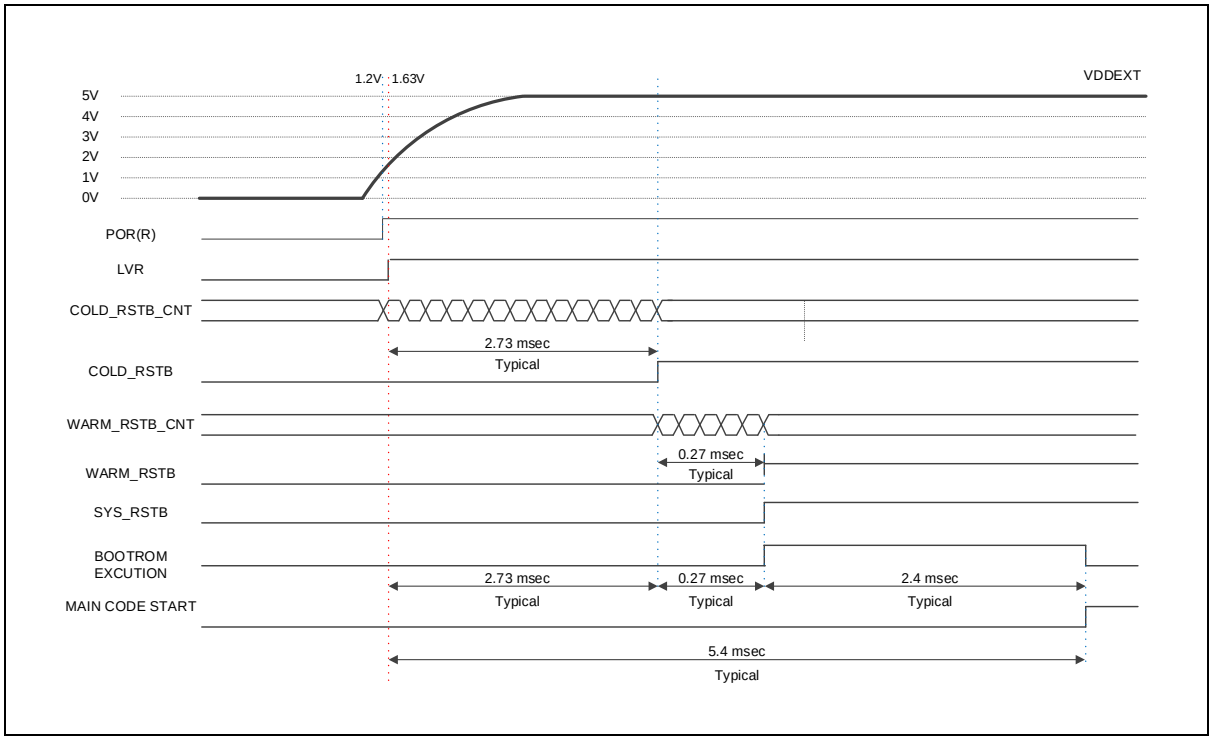


Figure 16. Power up Procedure

The VDD15 POR in the cold reset source senses the VDC output voltage in the VDD15 domain and generates a reset signal. The VDD15 POR reset signal initializes only the VDD15 domain. The backup domain is initialized only by VPWRSW POR or LVR reset.

In STANDBY mode and BACKUP POWER mode, VDD15 domain VDC is turned off and VDD15 POR occurs. Because core exists in VDD15 domain, wakeup in STANDBY mode or BACKUP POWER mode will execute BOOTROM and jump to start address.

4.4.2 Warm reset

Warm reset event has several reset sources and some parts of chip returns to an initial state when the warm reset condition is occurred.

The warm reset source is controlled by SCU_RSER register and the status is appeared in SCU_RSSR register. The reset for each peripheral blocks is controlled by SCU_PRER register. The reset can be masked independently.

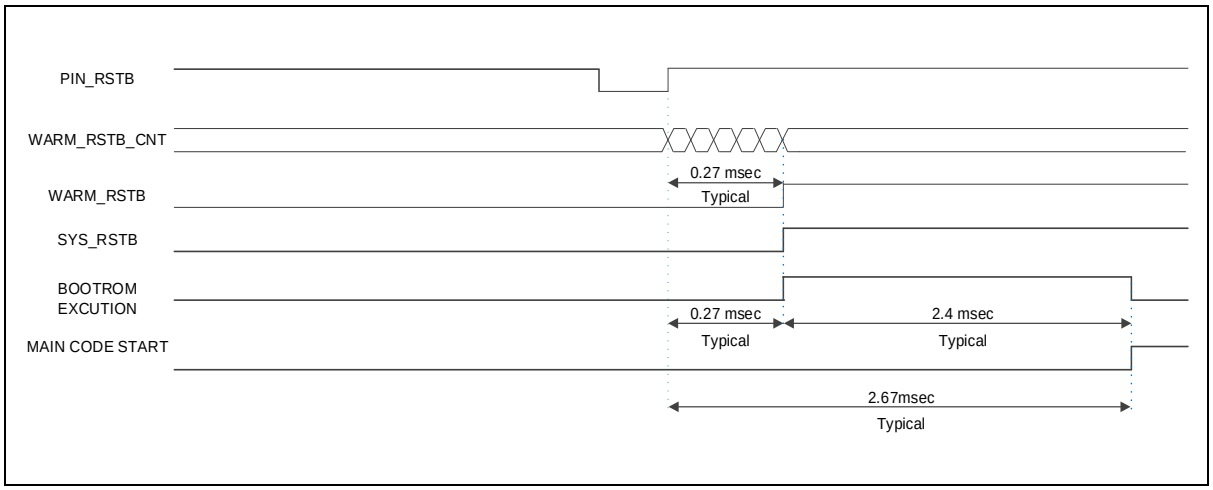


Figure 17. Warm Reset Diagram

4.4.3 LVR reset

Voltage level of LVR is set by low voltage reset configuration register (SCULV_LVRCNFG). Reset status of the LVR is shown in SCU_RSSR register. The LVR reset is controlled by SCULV_LVRCR register, which is cleared to “0x00” by VPWRSW POR reset.

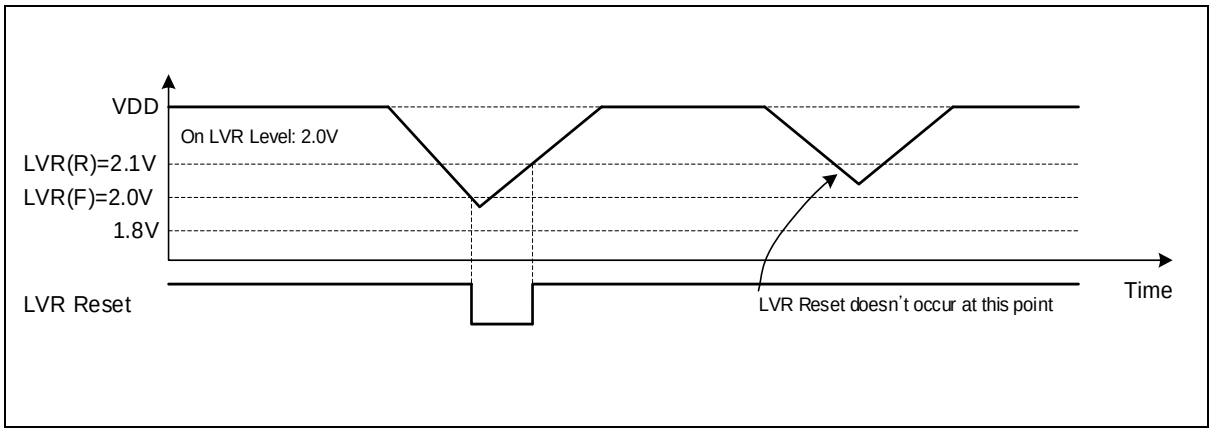
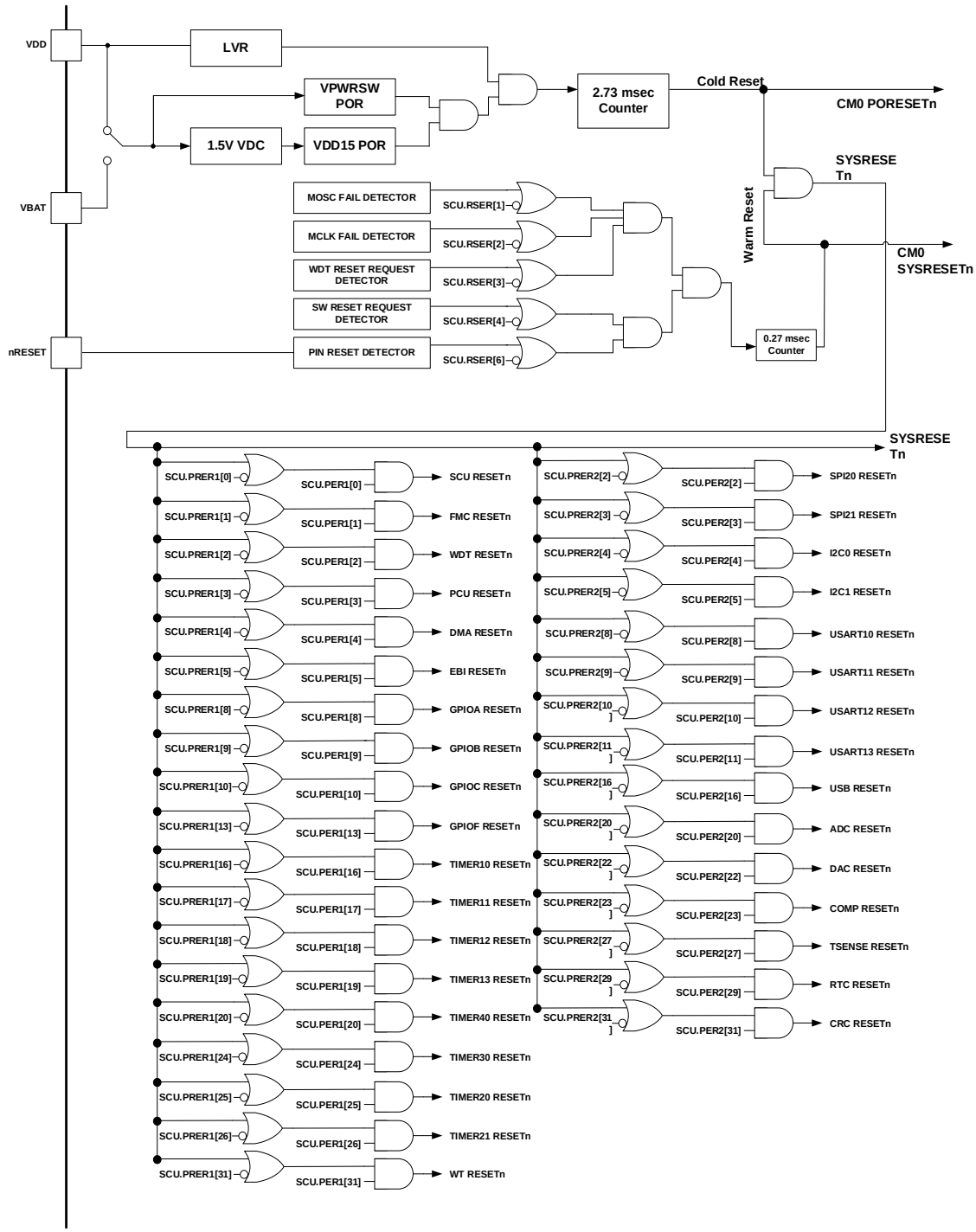


Figure 18. LVR Reset Timing Diagram

4.4.4 Reset tree



NOTES:

1. When cold reset occurs, WDT and RTC are no reset in STANDBY mode or BACKUP POWER mode.
2. WDT and RTC are reset, only by LVR reset and VPWRSW POR.

Figure 19. Reset Tree Configuration

4.5 Operation mode

INIT mode is an initial state of the chip when a reset is asserted. In RUN mode, CPU shows the maximum performance with high-speed clock system. SLEEP mode and three Power Down modes (STOP, STANDBY, and BACKUP POWER) can be used as a low power consumption mode. In the low power consumption mode, power is effectively managed to reduce power consumption by halting processor core and unused peripherals. Figure 20 describes transition between the operation modes.

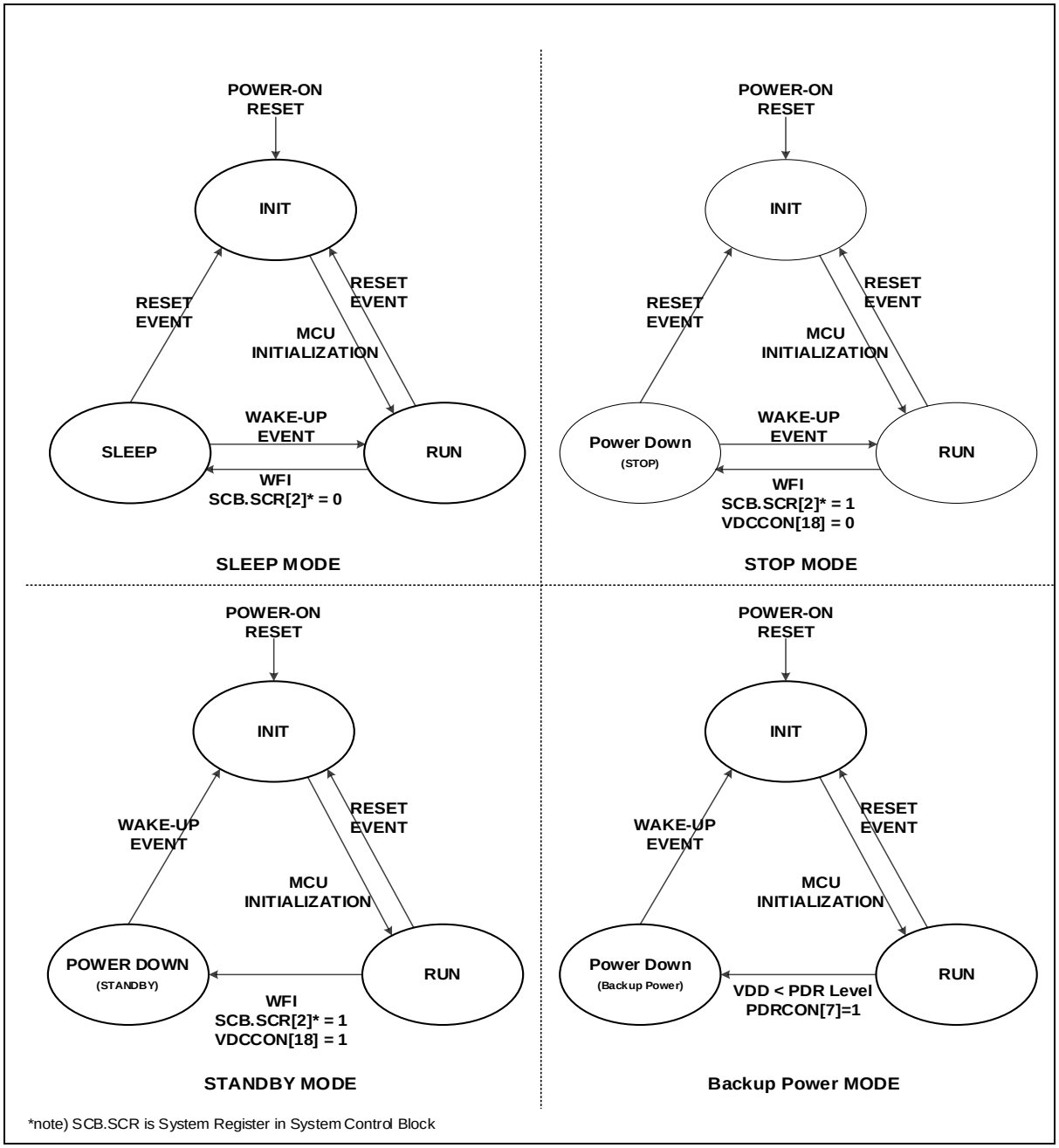


Figure 20. Transition between Operation Modes

Table 12. Operation Mode

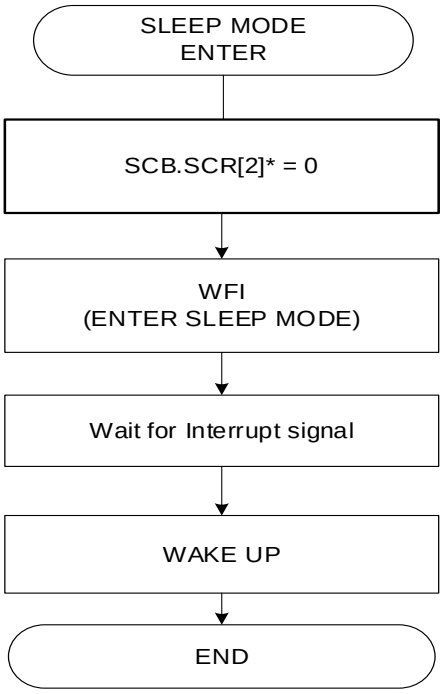
MODE	Condition	After Wake up Event	After Reset Event
RUN	POWER ON	N/A	INIT
SLEEP	WFI (Wait for Interrupt): SCB.SCR[2]*=0	RUN	INIT
STOP	WFI (Wait for Interrupt): SCB.SCR[2]*=1	RUN	INIT
STANDBY	WFI (Wait for Interrupt): SCB.SCR[2]*=1, VDDCON[18]=1	INIT	INIT
BACKUP POWER	VDD<PDR Level: PDRCON[7]=1	INIT	INIT

4.5.1 RUN mode

In RUM mode, CPU and the peripheral hardware operate with a high-speed clock. After a reset followed by INIT state, the system enters in the RUN mode.

4.5.2 SLEEP mode

Only CPU is stopped in this mode. Each peripheral function can be enabled by the function enable and clock enable bit in the PER and PCER register.



NOTE: SCB.SCR is System Control Register in System Control Block

Figure 21. SLEEP Mode Operation Sequence

4.5.3 Power-down mode

The A31G32x series have three power down modes: STOP mode, STANDBY mode, and BACKUP POWER mode.

In STOP mode, 1.5V VDC is off and backup domain VDC is supplied to 1.5V domain. All peripherals in the 1.5V domain are switched to STOP state and CPU goes under deepsleep state. In STANDBY mode, 1.5V VDC is off and power is not supplied to 1.5V domain. Therefore, all peripherals of the 1.5V domain are initialized by VDD15 POR. In BACKUP POWER mode, VDD is turned off and the power switch selects VBAT instead of VDD. 1.5V VDC is off and no power is supplied and initialized by VDD15 POR.

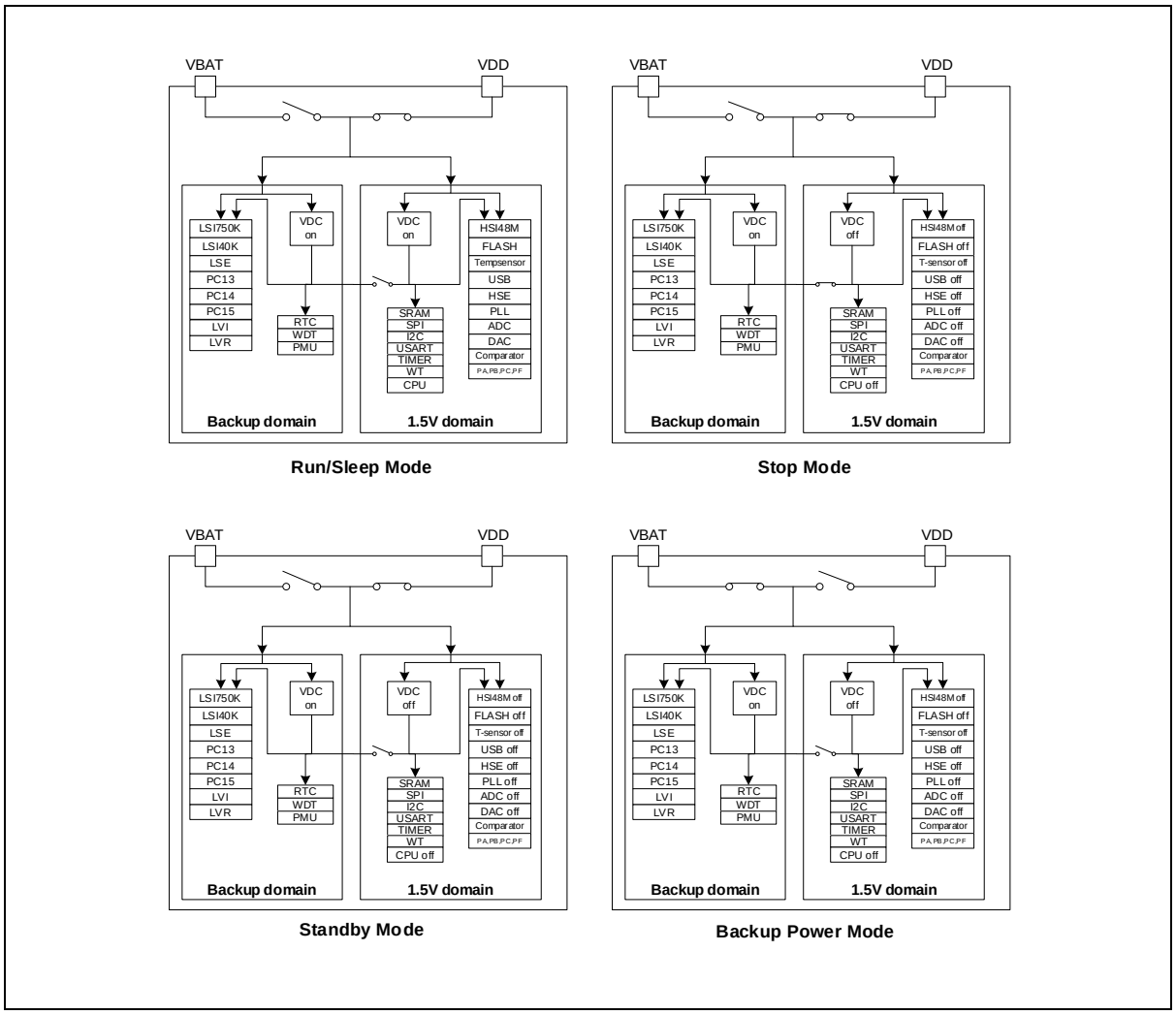


Figure 22. Power down Mode Block Diagram

LVI operates in STOP mode and STANDBY mode but is ignored in BACKUP POWER mode. LVR operation is not recommended in STOP mode and STANDBY mode. To use it, set BGRAON = 1 in SCU_SMR. LVR is not supported in BACKUP POWER mode. LVI and LVR are set using the SCULV_LVRCNFIG, SCULV_LVRCR and SCULV_LVICR registers. Initially the LVR is on. When LVR occurs, both backup domain and 1.5V domain are reset.

In power down mode, LSE, and LSI40K can operate in backup domain. To operate the LSE in power down mode, set SCU_CSCR [14] = 1. LSI40K does not turn off automatically in power down mode, so if you want LSI40K not to work in power down mode, you have to turn it off before entering power down mode.

Table 13. Oscillator Control in Power down Mode

	Operation enable	Power down operation
LSE	SCU_CSCR[15] = 1	If SCU_CSCR[14] = 1, RUN mode state is maintained If SCU_CSCR[14] = 0, turned off.
LSI40K	SCU_MCCR3[11] = 1	RUN mode state is maintained.

Table 14 lists peripheral's operation in each power down mode.

Table 14. Peripheral Operation in Power down Mode

Mode	Stop mode	Standby mode	Backup power mode
HSI48M	Stop	Power off	Power off
FLASH	Stop	Power off	Power off
Tempsensor	Stop	Power off	Power off
USB	Stop	Power off	Power off
HSE	Stop	Power off	Power off
PLL	Stop	Power off	Power off
ADC	Stop	Power off	Power off
DAC	Stop	Power off	Power off
Comparator	Operates	Power off	Power off
CPU	Deepsleep	Power off	Power off
SRAM	Retain	Power off	Power off
SPI20,21	Stop	Power off	Power off
I2C0,1	Operates only slave mode	Power off	Power off
USART10,11,12,13	Operates as only wakeup source	Power off	Power off
TIMER10,11,12,13 TIMER20,21,30,40	Operates only when the TIMER clock is oscillates	Power off	Power off

Table 14. Peripheral Operation in Power down Mode (continued)

Mode	Stop mode	Standby mode	Backup power mode
WT	Operates only when the WT clock is oscillates	Power off	Power off
PA,PB,PC,PF (except PC13, PC14, PC15)	Retain	Power off	Power off
PC13	Retain	GPIO or wakeup Pin	GPIO or wakeup Pin
PC14	Retain	GPIO or SXIN	GPIO or SXIN
PC15	Retain	GPIO or SXOUT	GPIO or SXOUT
LSI750K	Off	Off	Off
LSI40K	Operates	Operates	Operates
LSE	Operates	Operates	Operates
LVI	Operates	Operates	Discard
LVR	Operates	Operates	No support
RTC	Operates only when the RTC clock is oscillates	Operates only when the RTC clock is oscillates	Operates only when the RTC clock is oscillates
WDT	Operates only when the WDT clock is oscillates	Operates only when the WDT clock is oscillates	Operates only when the WDT clock is oscillates
SCU(Partially)	Operates	Operates	Operates

4.5.4 STOP mode

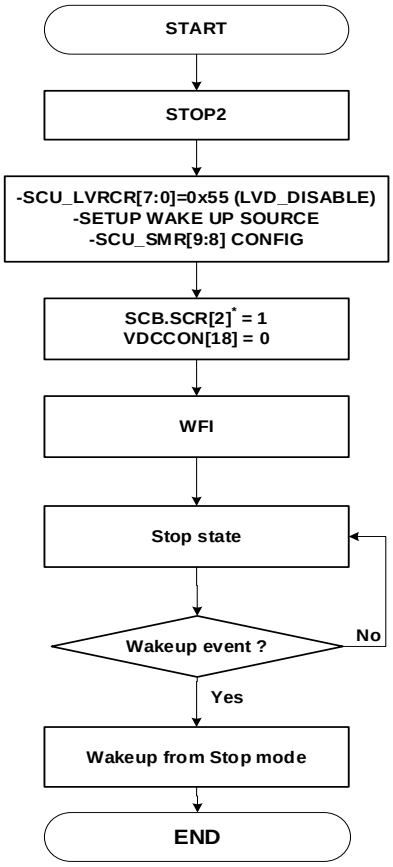
When the core goes under deepsleep state using WFI instruction, the chip enters in STOP mode. In STOP mode, all peripherals of 1.5V domain are stopped. Once power is supplied, internal SRAM and registers maintain their values.

The backup domain operates regardless of the STOP mode. To wake up in STOP mode, an interrupt request must be generated and can be selected in the SCU_WUER register. Stabilization time is 2.73ms after wakeup event occurs.

When entering in STOP mode, HSE is selected as the PLL input clock. These are maintained after wakeup.

Table 15. STOP Mode Configuration

Mode	Condition	Wakeup source
STOP	WFI SCB.SCR[2]* = 1 VDCCON[18] = 0	Source included in WUER



NOTES:

1. SCB.SCR is System Control Register in System Control Block.

Figure 23. STOP Mode Sequence

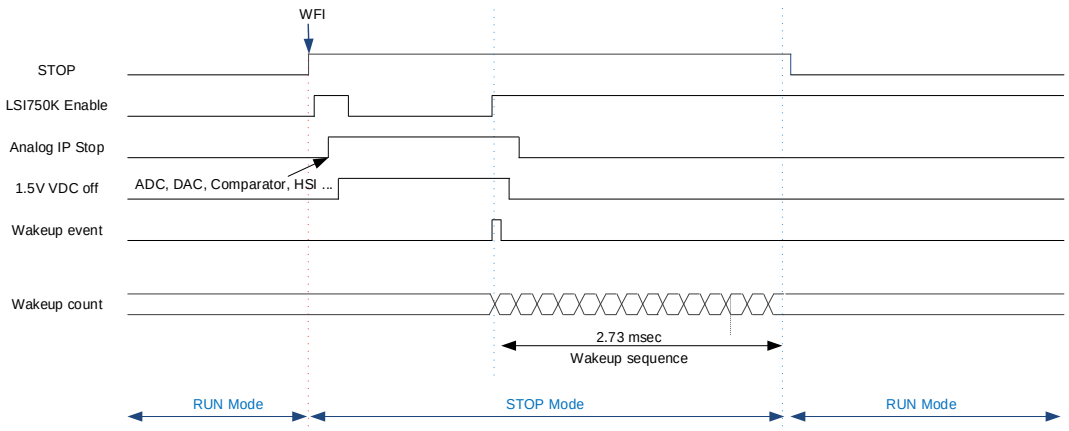


Figure 24. STOP Mode Timing Diagram

4.5.5 STANDBY mode

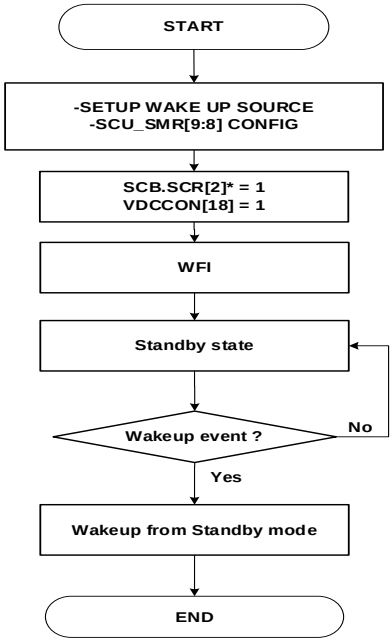
When the core goes under deepsleep state using WFI instruction with VDCCON[18] = 1, the chip enters in STANDBY mode. In STANDBY mode, VDC is turned off in 1.5V domain and all peripherals of 1.5V domain are in power off state. Therefore, the 1.5V domain is initialized as a whole by the VDD15 POR in STANDBY mode. The backup domain operates regardless of the STANDBY mode.

When selected in the SCU_WUER register, the LVI, WDT, and RTC interrupt flags in the backup domain can be used to wake up in STANDBY mode. If you set PC13 as wakeup pin by setting the RTCPFCR register, the chip can wake up from STANDBY mode with rising edge of PC13. When a pin reset occurs in STANDBY mode, the chip exits STANDBY mode. Pin reset can be enabled in SCU_RSER. Stabilization time is 2.73ms after wakeup event occurs.

When entering in STANDBY mode, HSE is selected as the PLL input clock. These are maintained after wake-up.

Table 16. STANDBY Mode Configuration

Mode	Condition	Wakeup source
STANDBY	WFI SCB.SCR[2]* = 1 VDCCON[18] = 1	RTC WDT PC13 (Wakeup pin) Pin reset



NOTES:

1. SCB.SCR is System Control Register in System Control Block

Figure 25. STANDBY Mode Sequence

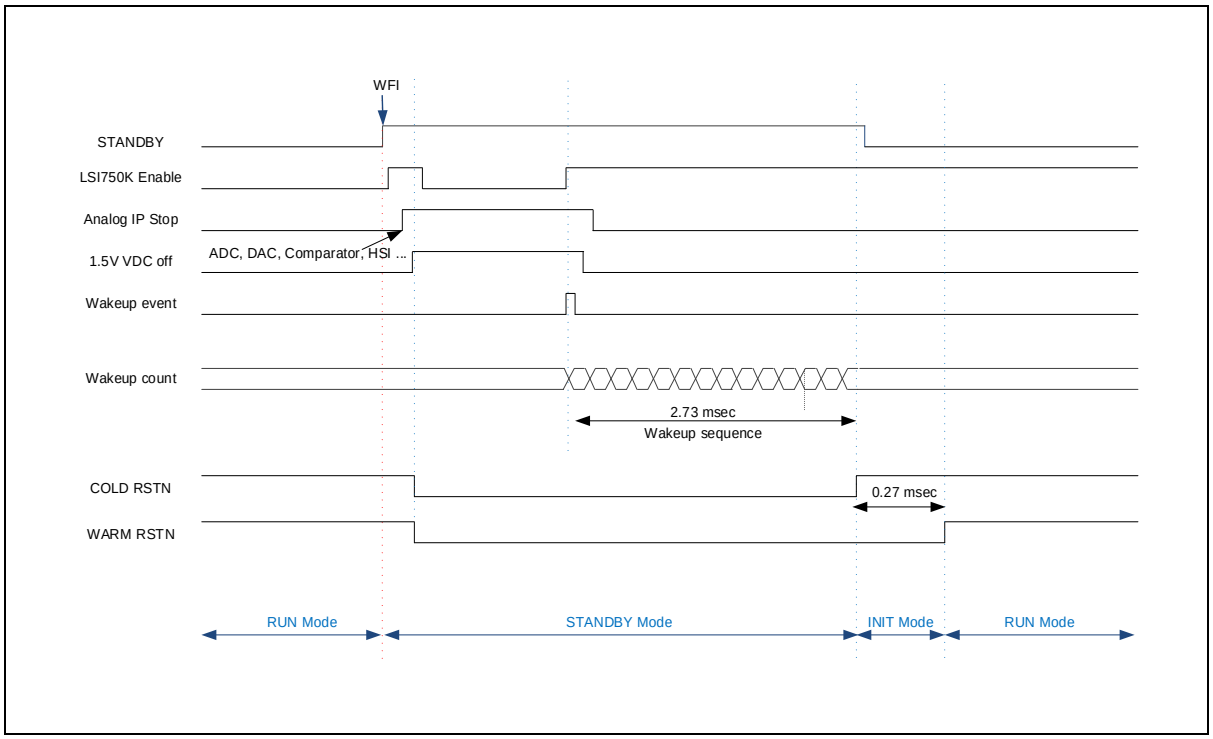


Figure 26. STANDBY Mode Timing Diagram

4.5.6 BACKUP POWER mode

By connecting the VBAT pin to an optional standby voltage from a battery or other source, you can maintain the contents of the backup register and power the entire backup domain when VDD is turned off.

BACKUP POWER mode can be entered from all operation modes (RUN, SLEEP and STOP, STANDBY). If a PDR reset occurs when Power down reset (PDR) is enabled through the PDRCON register, the chip enters in BACKUP POWER mode. In BACKUP POWER mode, 1.5V VDC is turned off and all peripherals are in power off state. If VDD rises again and becomes higher than PDR, it exits BACKUP POWER mode and 1.5V domain restarts in initial state. For more information about BACKUP POWER mode, please refer to 4.3 Power domain.

Table 17. BACKUP POWER Mode Configuration

Mode	Condition	Wakeup source
BACKUP POWER	PDRCON[7] = 1	(VDD rising) > PDR

NOTE: It is recommended that VBAT is higher than PDR voltage.

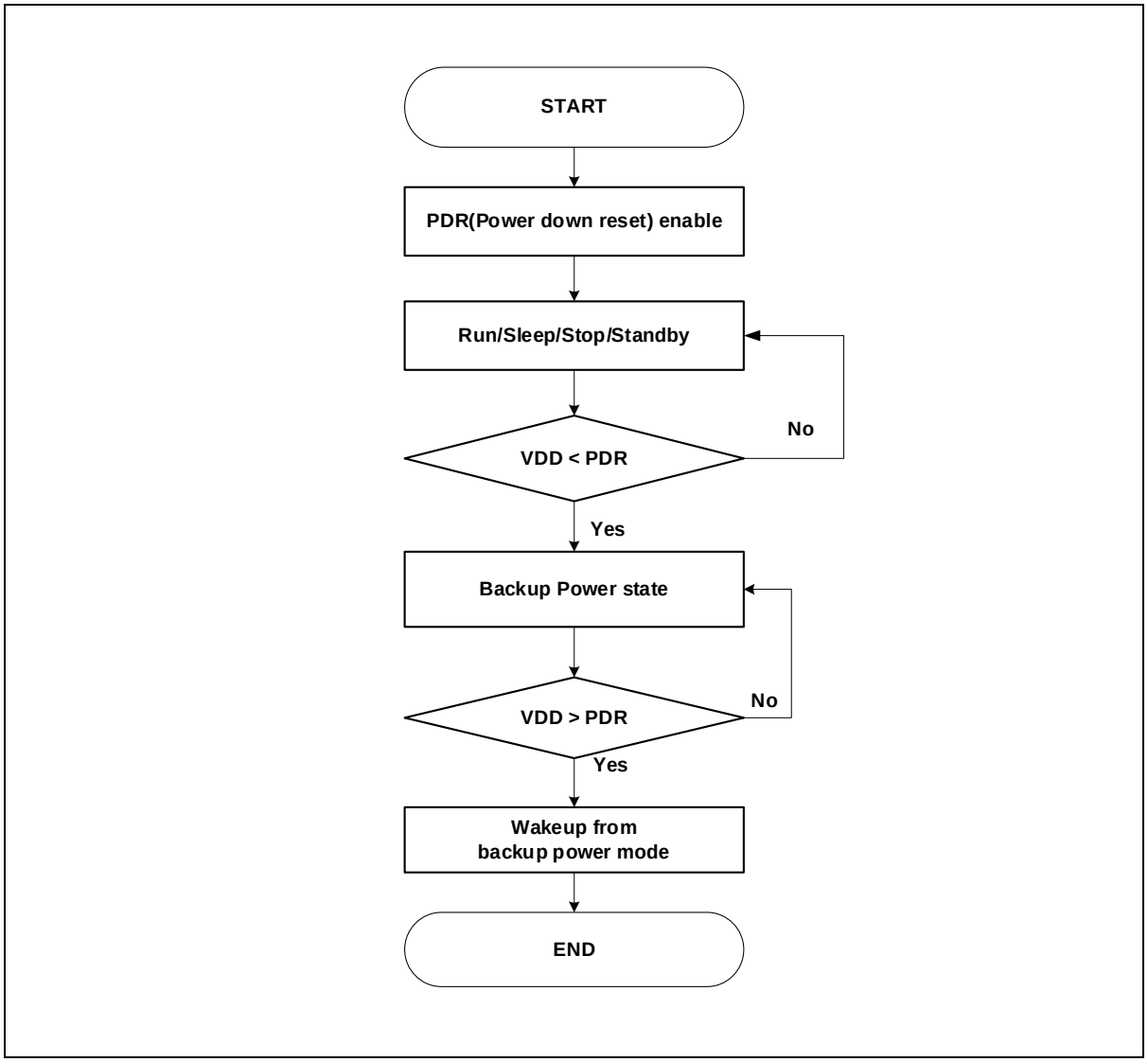


Figure 27. BACKUP POWER Mode Sequence

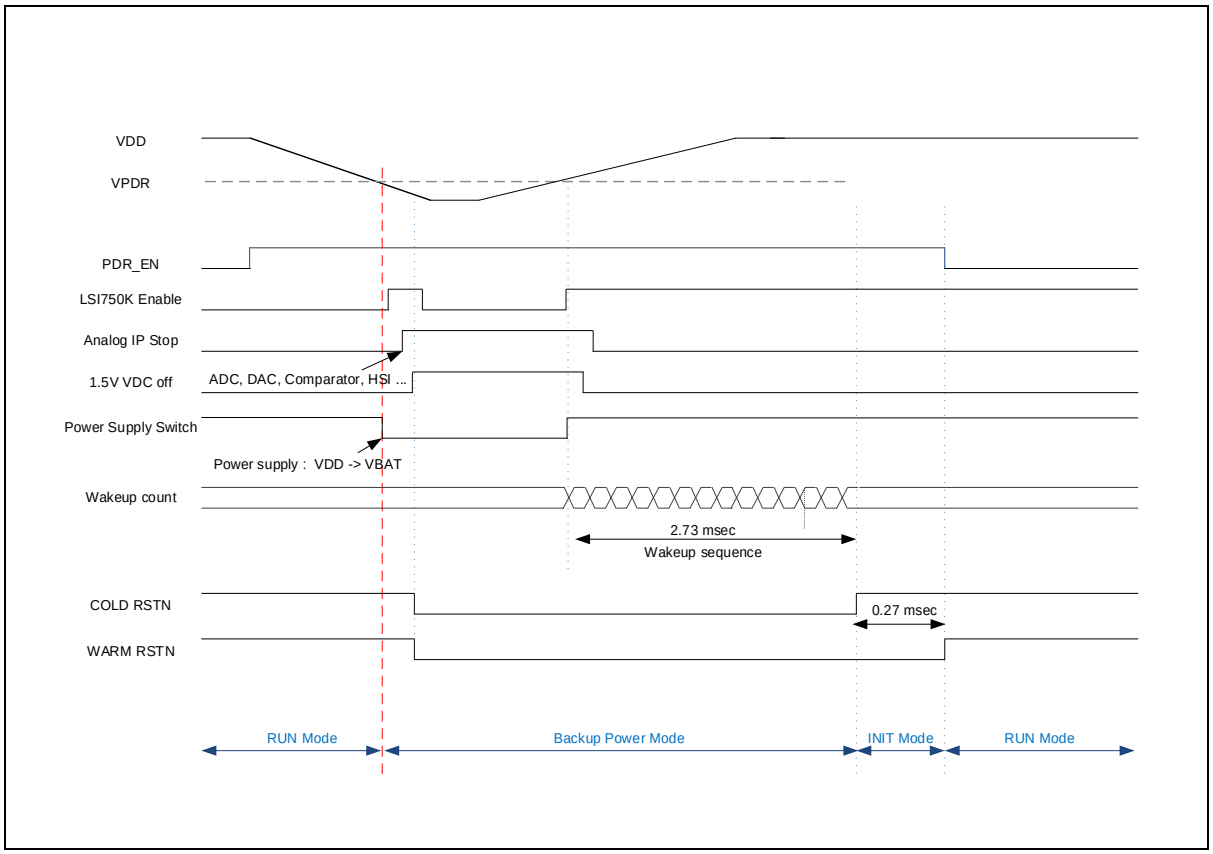


Figure 28. BACKUP POWER Mode Timing Diagram

5. PCU and GPIO

Port Control Unit (PCU) configures and controls external I/Os as listed in the followings:

- External signal directions of each pins
- Interrupt trigger mode for each pins
- Internal pull-up/down register control and open drain control

General Purpose Input/Output (GPIO) is corresponding to the most pins except dedicated-function pins. GPIO ports are controlled by GPIO block as listed in the followings:

- Output signal level (H/L) select
- External interrupt interface
- Pull up/down enable or disable

Four pins in Table 18 are assigned for PCU and GPIO blocks.

Table 18. PCU and GPIO pins

Pin name	Type	Description
PA	IO	PA0 to PA15
PB	IO	PB0 to PB15
PC	IO	PC0 to PC15
PF	IO	PF0 to PF2

5.1 PCU and GPIO Block diagram

Figure 29 describes PCU in block diagram.

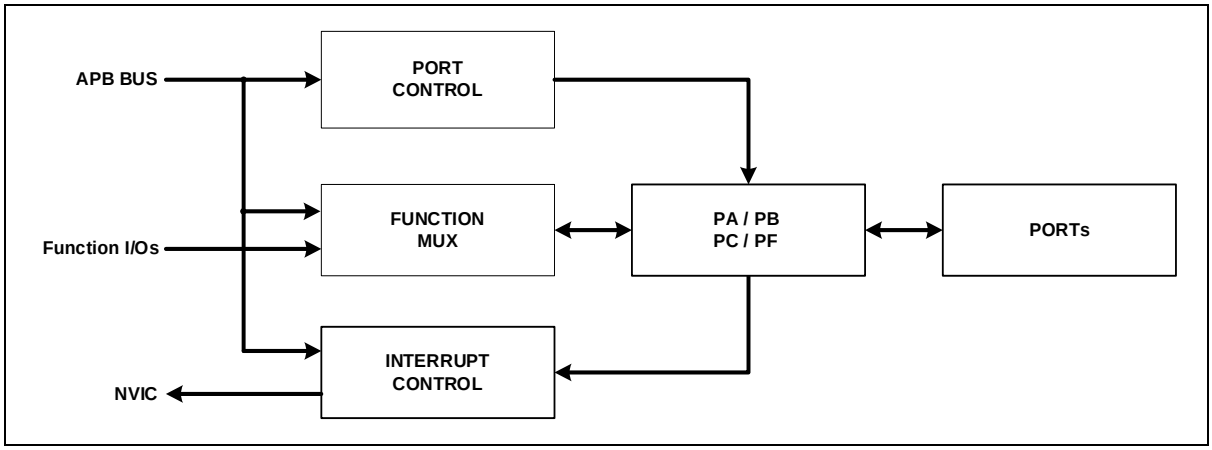


Figure 29. PCU Block Diagram

Figure 30 and Figure 31 describes GPIO in block diagram, and Figure 32 introduces external interrupt I/O pins.

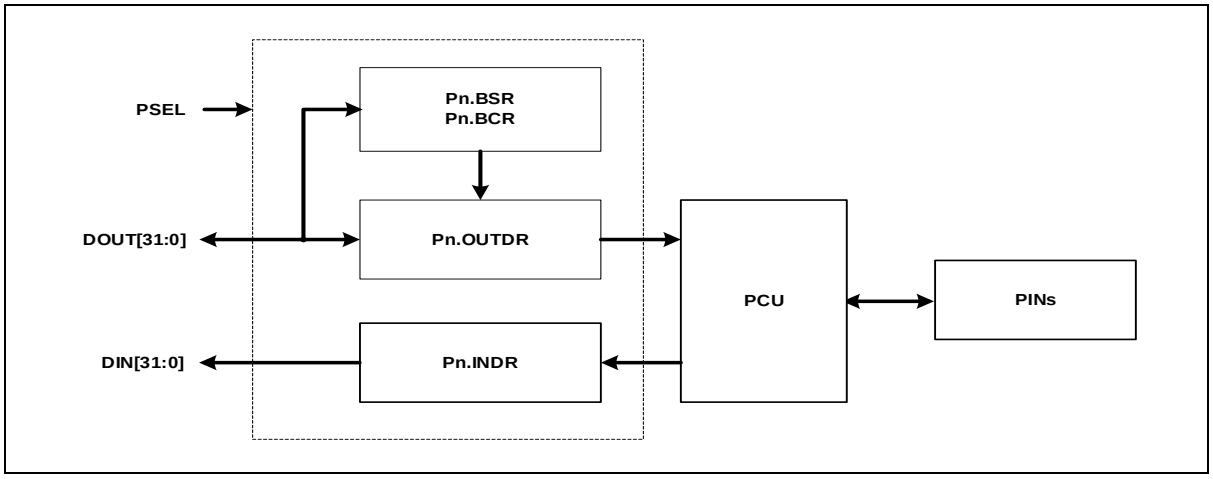


Figure 30. GPIO Block Diagram(Except PC13, PC14, PC15)

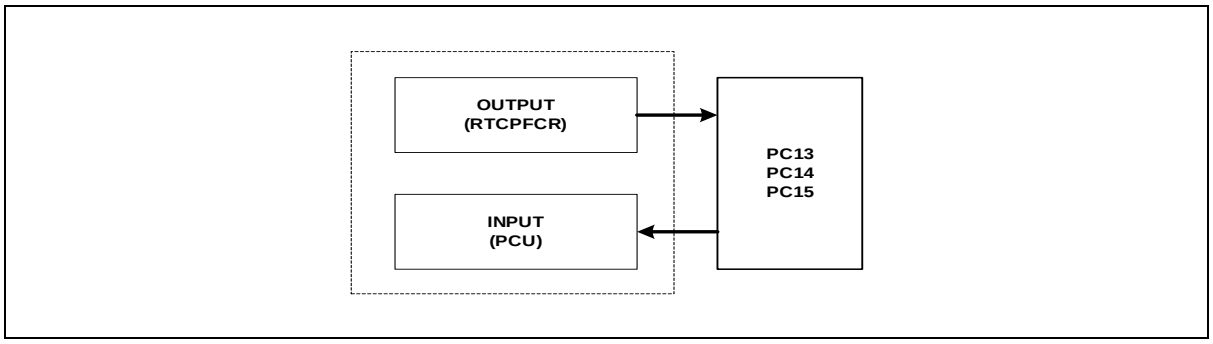


Figure 31. PC13, PC14, PC15 Block Diagram

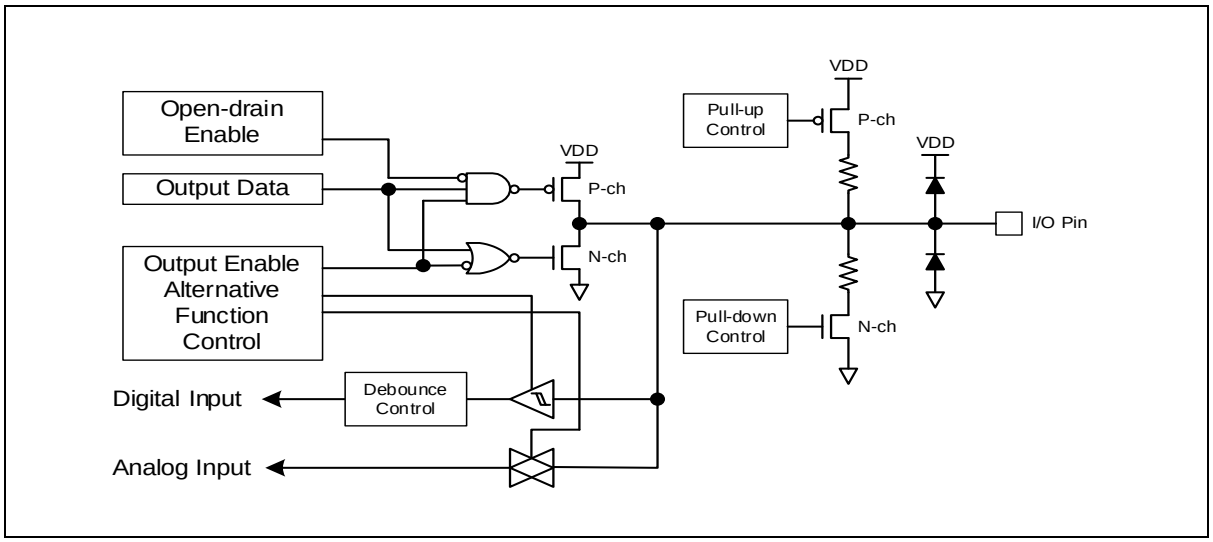


Figure 32. I/O Port Block Diagram (External Interrupt I/O Pins)

5.2 Pin multiplexing

GPIO pins have alternative function pins. Table 19 shows pin multiplexing information.

Table 19. GPIO Alternative Function

Pin name	Alternative function										
	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10
PA0	USART13_TXD	USART13_MOSI		CP0_OUT	EC20			RTC_TAMP2			AN0 CP0_N2
PA1	USART13_RXD	USART13_MISO	USART11_SS		EC13	T13CAP	T13OUT	T20CAP	T20OUT		AN1 CP0_P0
PA2	USART11_TXD		USART11_MOSI	CP1_OUT	EC10	T10CAP	T10OUT	T20CAP	T20OUT		AN2 CP1_N2
PA3	USART11_RXD		USART11_MISO		EC10	T10CAP	T10OUT	T20CAP	T20OUT		AN3 CP1_P0
PA4	SPI20_SS		USART11_SCK								AN4 CP0_N0 CP1_N0 DAC_OUT1
PA5	SPI20_SCK				EC20						AN5 CP0_N1 CP1_N1 DAC_OUT2
PA6	SPI20_MISO	CP0_OUT		BLNK30	EC11	T11CAP	T11OUT	T40CAP_CH1	T40OUT	RD	AN6
PA7	SPI20_MOSI	CP1_OUT		PWM30AB	EC12	T12CAP	T12OUT	T40CAP_CH2	T40OUT	A19	AN7
PA8		USART10_SCK		PWM30AA						AD07	
PA9	USART10_TXD	USART10_MOSI		PWM30BA						AD06	
PA10	USART10_RXD	USART10_MISO		PWM30CA	EC21					AD05	
PA11	CP0_OUT									AD04	USBDM
PA12	CP1_OUT	USART10_SS		EC30	T30CAP					AD03	USBDP
PA13		SWDIO									
PA14	USART11_TXD	SWCLK	USART11_MOSI								
PA15	USART11_RXD	USART13_SS	USART11_MISO	SPI20_SS	EC21					ALE	
PB0		USART12_SCK		PWM30BB		T21CAP	T21OUT	T40CAP_CH3	T40OUT	A16	AN8
PB1		USART12_SS		PWM30CB	EC13	T13CAP	T13OUT			AD15	AN9
PB2					EC13	T13CAP	T13OUT			AD14	
PB3				SPI20_SCK		T20CAP	T20OUT			AD02	
PB4				SPI20_MISO				T40CAP_CH1	T40OUT	AD01	
PB5				SPI20_MOSI		T21CAP	T21OUT	T40CAP_CH2	T40OUT	AD00	
PB6	USART10_TXD	USART10_MOSI	I2C0_SCL		EC11	T11CAP	T11OUT	T40CAP_CH3	T40OUT	LWR	
PB7	USART10_RXD	USART10_MISO	I2C0_SDA		EC12	T12CAP	T12OUT			CS0	

Table 19. GPIO Alternative Function (continued)

Pin name	Alternative function										
	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10
PB8		I2C0_SCL			EC11	T11CAP	T11OUT				
PB9		I2C0_SDA		SPI21_SS	EC12	T12CAP	T12OUT				
PB10	USART12_TXD	USART12_MOSI	I2C1_SCL	SPI21_SCK		T20CAP	T20OUT			AD13	
PB11	USART12_RXD	USART12_MISO	I2C1_SDA			T20CAP	T20OUT			AD12	
PB12	SPI21_SS	USART12_SCK		BLNK30	EC13	T13CAP	T13OUT			AD11	
PB13	SPI21_SCK		I2C1_SCL	PWM30AB						AD10	
PB14	SPI21_MISO	USART12_SS	I2C1_SDA	PWM30BB	EC10	T10CAP	T10OUT			AD09	
PB15	SPI21_MOSI			PWM30CB	EC10	T10CAP	T10OUT	T21CAP	T21OUT	AD08	
PC0										LWR	AN10 CP0_P1
PC1										AD00	AN11 CP1_P1
PC2	SPI21_MISO									AD01	AN12
PC3	SPI21_MOSI				EC13	T13CAP	T13OUT			AD02	AN13
PC4	USART12_TXD	USART12_MOSI						EC40		A18	AN14
PC5	USART12_RXD	USART12_MISO				T21CAP	T21OUT			A17	AN15
PC6						T21CAP	T21OUT	T40CAP_CH1	T40OUT	NWAIT	
PC7								T40CAP_CH2	T40OUT	UDS	
PC8								T40CAP_CH3	T40OUT	UWR	
PC9								EC40		CS3	
PC10	USART13_TXD	USART13_MOSI	USART12_TXD	USART12_MOSI						LDS	
PC11	USART13_RXD	USART13_MISO	USART12_RXD	USART12_MISO	EC21					RD	
PC12		USART13_SCK		USART12_SCK						CS2	
PC13								RTC_TAMP1			
PC14											SXIN
PC15											SXOUT
PF0		CLKO									XIN
PF1											XOUT
PF2				USART12_SS		T21CAP	T21OUT	EC40		CS1	

NOTES:

1. On connection with debugger host, SWCLK and SWDIO pins are always for SW-DP pins.
   So, the corresponding bits of PB_MOD/PB_TYP/PB_AFSR1/PB_PUPD registers may not be written by software.
2. RTCOUT must be set in PC13MODE in the RTCPFCR register.

6. Flash memory controller

Flash Memory Controller is an internal flash memory interface controller, and includes following features as shown below:

- 128 or 64KB Flash code memory
- Wait, 1-wait, 2-wait(default)
- Read protection support
- Self-Program support
- User option area
- 3-page (each 512 Bytes)
- Erase, Program in user mode

Table 20. Flash Memory Controller Features

Item	Description	
Size	64KB	128KB
Start Address	0x0000_0000	0x0000_0000
End Address	0x0001_0000	0x0002_0000
Page Size	512-byte	512-byte
Total Page Count	128 pages	256 pages
PGM Unit	32-bit	32-bit
Erase Unit	512-byte/ 1KB/ 4KB/ bulk	512-byte/ 1KB/ 4KB/ bulk

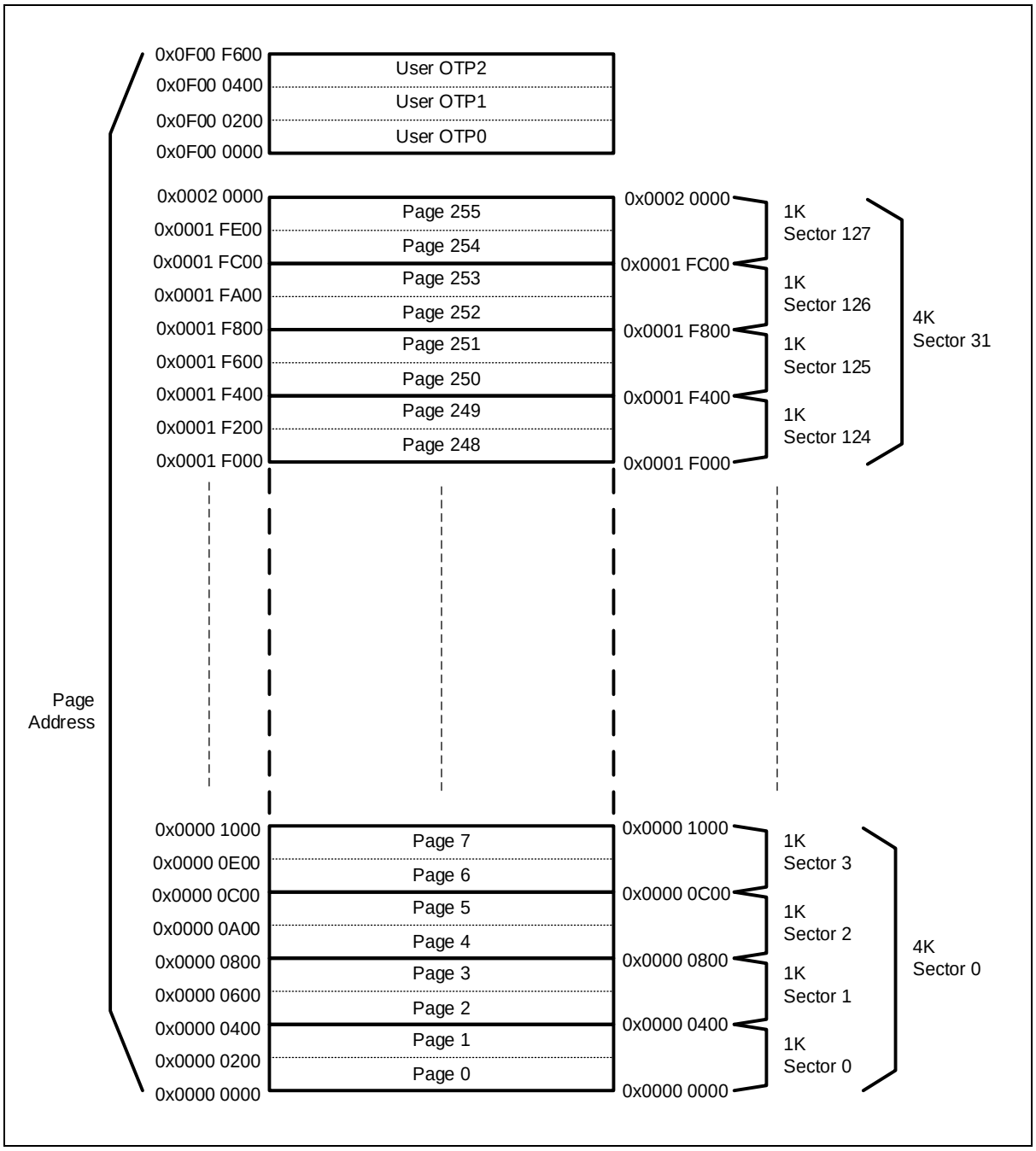


Figure 33. Flash Memory Map (128 KB Code Flash)

7. Direct Memory Access Controller (DMAC)

The direct memory access (DMA) controller is used for high-speed data transfers between peripherals and memories. DMA enables quick data transfers having memory to memory copying or moving of data within memory.

- 4 channels
- Single transfer only
- Support 8/16/32-bit data size
- Support multiple buffer with same size
- Interrupt condition is transferred through a peripheral interrupt.

7.1 Block diagram

In this section, DMAC block diagram is introduced in Figure 34.

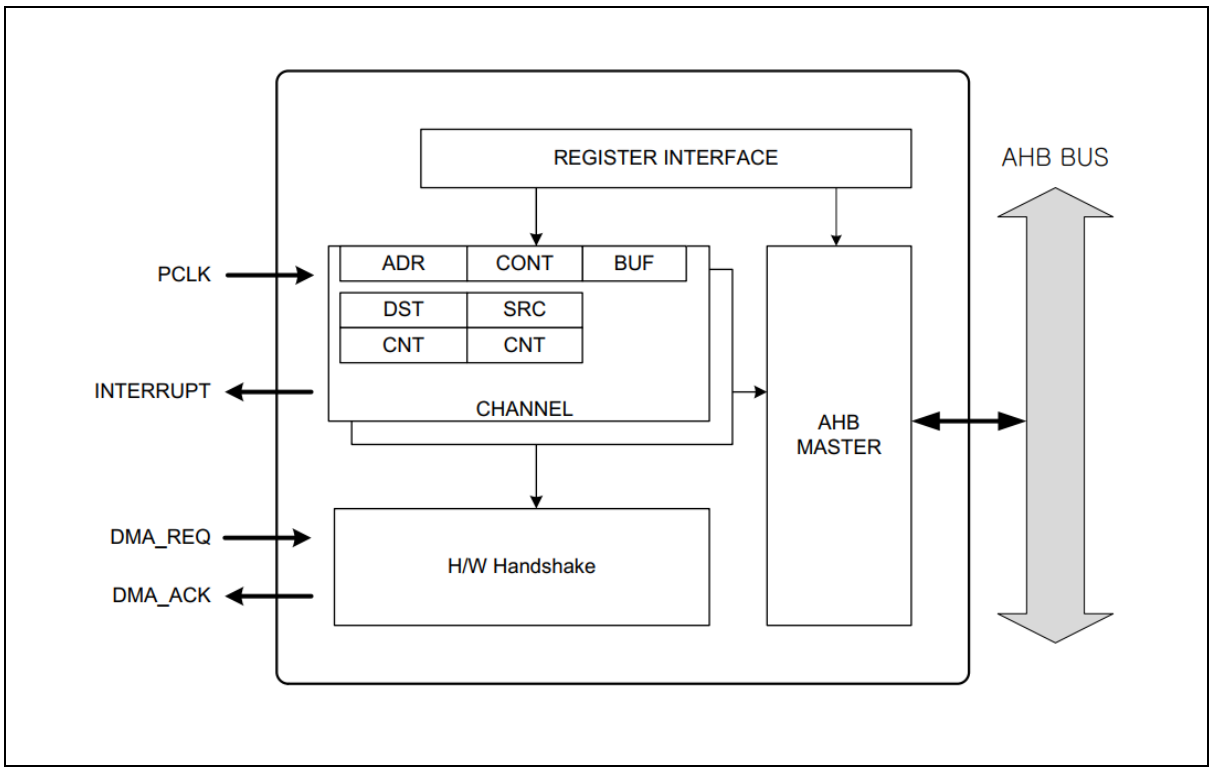


Figure 34. DMAC Block Diagram

8. Static memory controller (EBI)

Static memory controller is used for external bus interfaces to control external memory I/Os. External memory area is divided to 4 sections. 1MByte memory area is allocated for each section respectively. Memory devices (SRAM, ROM and Flash) or I/O devices can be mapped to the memory section. Bus configurations such as bus width of external device and the number of wait are configurable in each section; a user can attach many kinds of memories or I/O devices.

Table 21 introduces pins assigned for static memory controller.

Table 21. Pin Assignment of Static Memory Controller

Pin name	Type	Description
nCS[3:0]	O	Select memory region from 0 to 3.
nRD	O	Perform read operation from external memory.
nUWR	O	Upper byte write signal. When 16-bit bank is organized using 8bit memory, this pin indicates that D[15:8] is being written to external memory
nLWR/nWE	O	Lower byte write signal. It is used in various ways according to the memory and bank organization. When 8-bit or 16-bit bank is organized using 8-bit memory, this pin indicates that lower byte, D[7:0] is being written to external memory.
nUDS	O	Upper Data Select signal. It is used in various ways according to the memory and bank organization. When 16-bit bank is organized using 16-bit memory, this pin indicates that upper byte is being selected.
nLDS	O	Lower Data Select signal. It is used in various ways according to the memory and bank organization. When 16-bit bank is organized using 16-bit memory, this pin indicates that lower byte is being selected.
nWAIT	I	This pin is an external wait signal pin. If value of this pin becomes “L”, wait is added as much as nWAIT maintains “L”.
ALE	O	Address Latch Enable In the case of muxed Address/Data access, external address buffer for A[15:0] must be used. Address buffer latch AD[15:0] signals when ALE is high.
A[19:16]	O	Upper Address bus for external memory devices
AD[15:0]	I/O	Address or Data input/output bus for external memory devices

8.1 Block diagram

In this section, static memory controller is described in Figure 35.

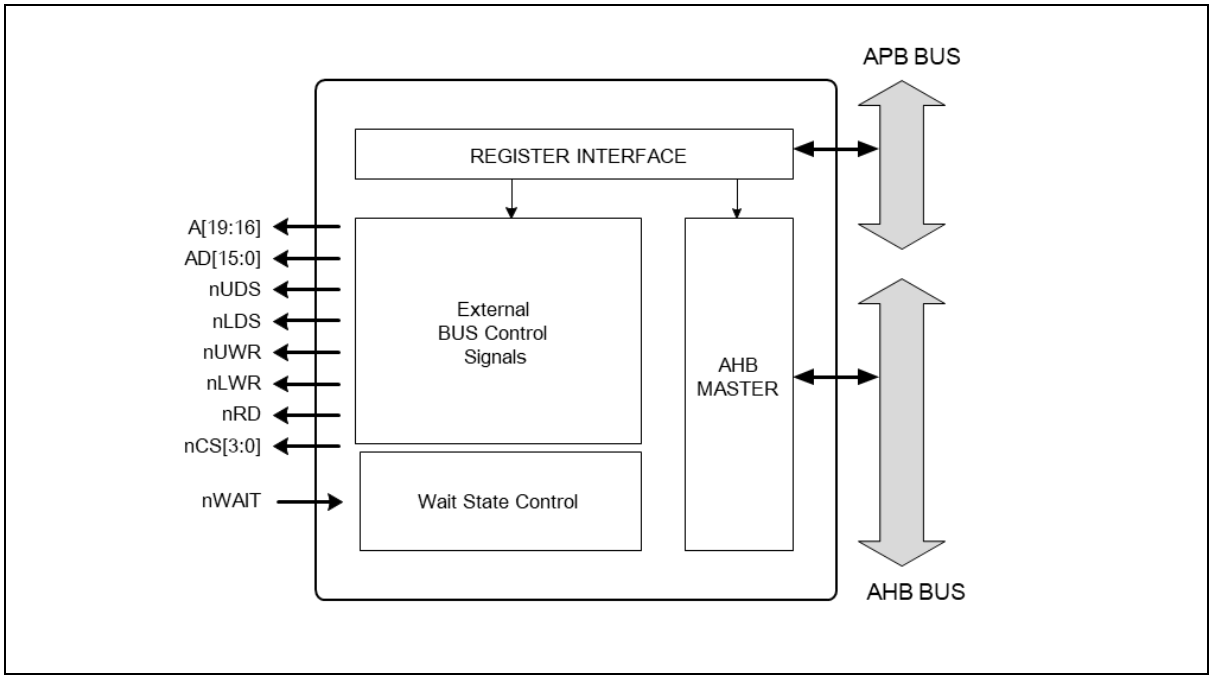


Figure 35. Static Memory Controller Block Diagram

9. Watchdog timer (WDT)

Watchdog timer (WDT) rapidly detects CPU's malfunction such as endless looping caused by noise, and resumes the CPU to the normal state. WDT signal for malfunction detection can be used as either a CPU reset or an interrupt request. When WDT is not being used for malfunction detection, it can be used as a timer generating an interrupt at fixed intervals.

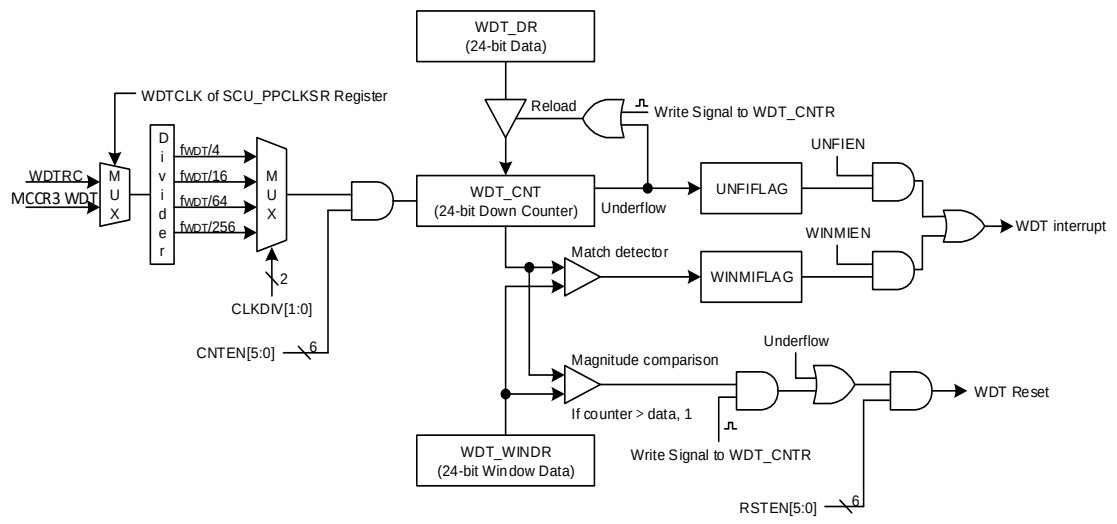
When WDT_CNT value is reached to WDT_WINDR value, a watchdog interrupt can be generated. The underflow time of WDT can be set by WDT_DR. If the underflow occurs, an internal reset is generated. WDT operates on the WDTRC embedded RC oscillator clock.

WDT of A31G32x series features followings:

- 24-bit down counter (WDT_CNT)
- Select reset or periodic interrupt
- Count clock selection
- Watchdog overflow output signal
- Counter window function

9.1 WDT block diagram

In this section, WDT block diagram is introduced in Figure 36.



NOTE: If a reload signal is generated, the WDT_DR value is reloaded to WDT_CNT register after 1 clock delay with the clock which is selected by the CLKDIV bits.

Figure 36. WDT Block Diagram

10. Watch timer

Watch timer (WT) has functions for RTC (Real Time Clock) operation. It is generally used for RTC design. WT consists of a clock source select circuit, a timer counter circuit, an output select circuit and watch timer control registers.

Prior to operate WT, a user needs to determine an input clock source and output interval, and to set WTEN as '1' in watch timer control register (WT_CR). It is able to execute simultaneously or individually. To stop or reset WT, clear the WTEN bit in WT_CR register.

Watch timer counter circuit corporates a 26-bit counter. Low 14 bits of the counter form a binary counter and high 12 bits form an auto reload counter in order to raise resolution. In WTCLR, it can control WT clear and set interval value at write time, and it can read 12-bit WT counter value at read time.

10.1 WT block diagram

As shown in Figure 37, WT of A31G32x series have the following blocks:

- 14-bit divider
- 12-bit up-counter
- RTC function

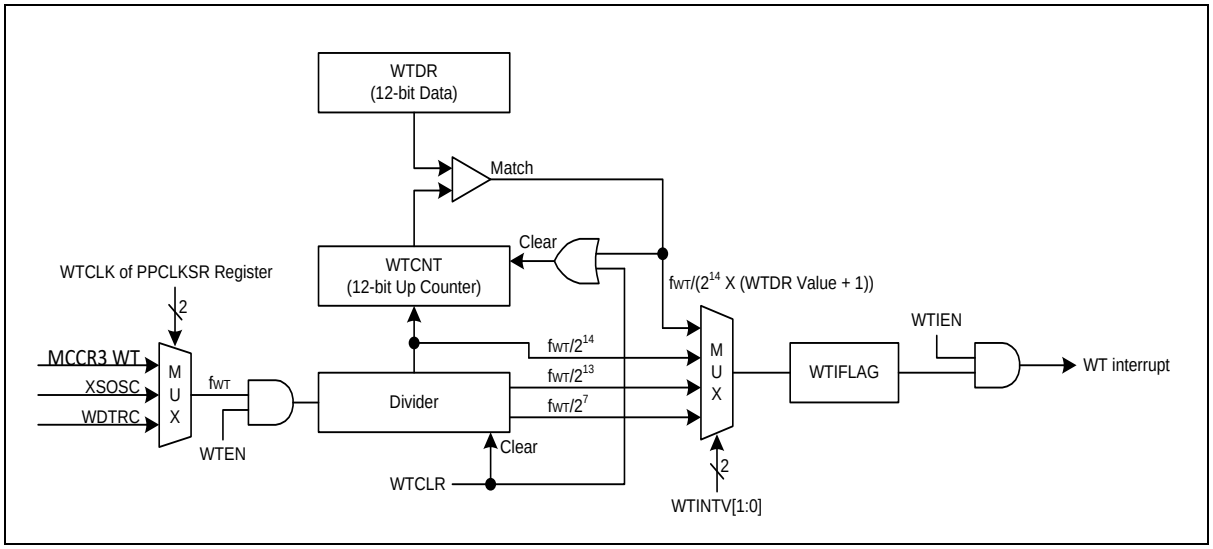


Figure 37. Watch Timer Block Diagram

11. 16-bit timer

16-bit timer block comprises 4 channels of 16-bit general purpose timers. Each channel has an independent 16-bit counter and a dedicated prescaler that feeds a counting clock. 16-bit timer supports periodic timer, PWM pulse, one-shot and capture mode. In addition, one more optional free-run timer is provided. Main purpose of 16-bit timer is a periodical tick timer.

16-bit timer of A31G32x series features the followings:

- 16-bit up-counter
- Periodic timer mode
- One-shot timer mode
- PWM pulse mode
- Capture mode
- 12-bit prescaler
- Synchronous start and clear function

Table 22 introduces pins assigned for 16-bit timer.

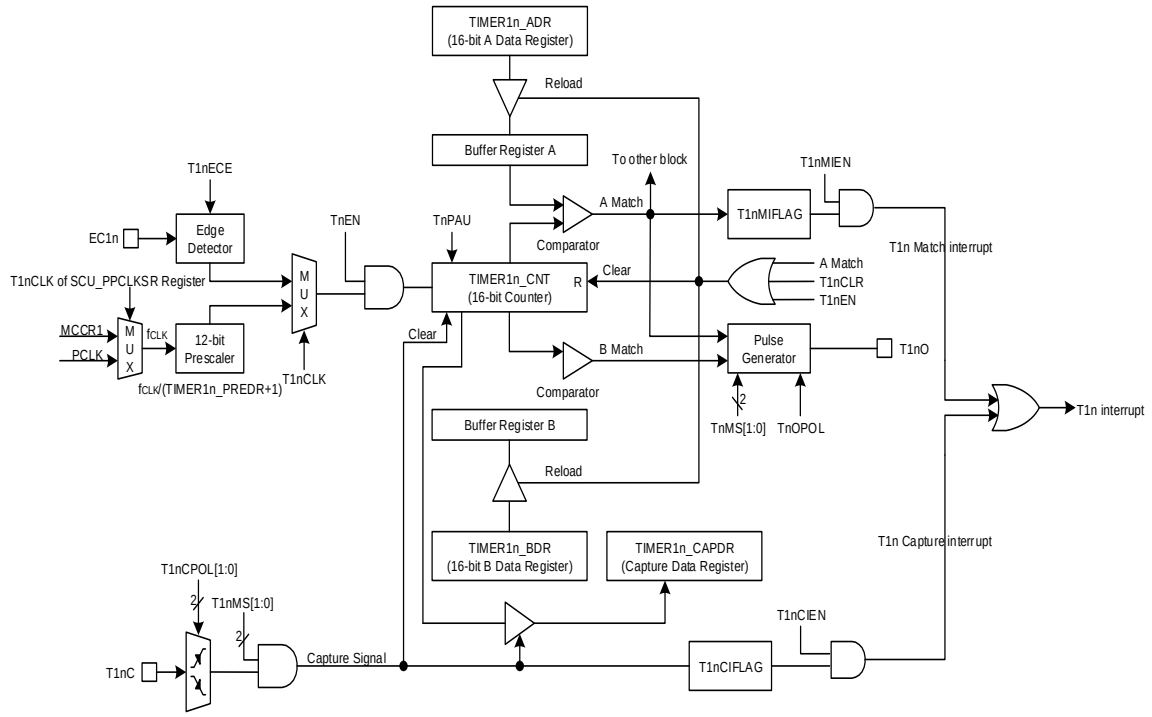
Table 22. Pin Assignment of 16-bit Timer: External Pins

Pin name	Type	Description
EC1n	I	Timer 1n External Clock input
T1nCAP	I	Timer 1n Capture input
T1nOUT	O	Timer 1n Output

NOTE: n = 0, 1, 2, and 3

11.1 16-bit timer block diagram

In this section, 16-bit timer is described in a block diagram in Figure 38.



NOTES:

1. The TnEN is automatically cleared to logic “0” after one pulse is generated at a PPG one-shot mode.
2. After the TnEN bit is set, the counting of TIMERn_CNT may be delayed 2 clocks or more.

Figure 38. 16-bit Timer Block Diagram

12. 32-bit timer

32-bit timer block comprises 2 channels of 32-bit general purpose timers. Each channel has an independent 32-bit counter and a dedicated prescaler that feeds a counting clock. 32-bit timer supports periodic timer, PWM pulse, one-shot and capture mode. In addition, one more optional free-run timer is provided. Main purpose of 32-bit timer is a periodical tick timer.

32-bit timer of A31G32x series features the followings:

- 32-bit up-counter
- Periodic timer mode
- One-shot timer mode
- PWM pulse mode
- Capture mode
- 12-bit prescaler
- Synchronous start and clear function

Table 23 introduces pins assigned for 32-bit timer.

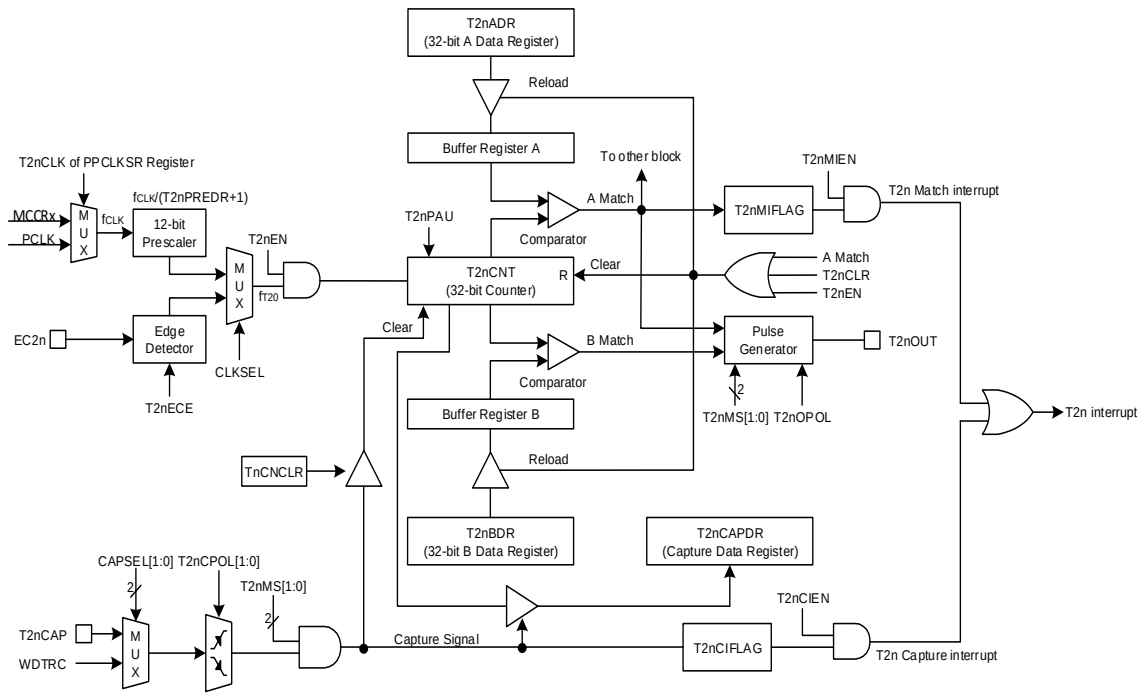
Table 23. Pin Assignment of 32-bit Timer: External Pins

Pin name	Type	Description
EC2n	I	Timer 2n external clock input
T2nCAP	I	Timer 2n capture input
T2nOUT	O	Timer/PWM/one-shot output

NOTE: n = 0 or 1

12.1 32-bit timer block diagram

In this section, 32-bit timer is described in a block diagram in Figure 39.



NOTES:

1. The T20EN is automatically cleared to logic “0” after one pulse is generated at a PPG one-shot mode.
2. After the T20EN bit is set, the counting of TIMER20_CNT may be delayed 2 clocks or more.

Figure 39. 16-bit Timer Block Diagram

13. Timer counter 30

Timer counter 30 of A31G24x series consist of a multiplexer, a comparator, 16-bit sized timer data registers A/B/C, and many other registers used for its operation. Main features are listed in the followings:

- 16-bit up/down-counter
- Periodic timer mode
- Back-to-Back mode
- Capture mode
- 12-bit prescaler

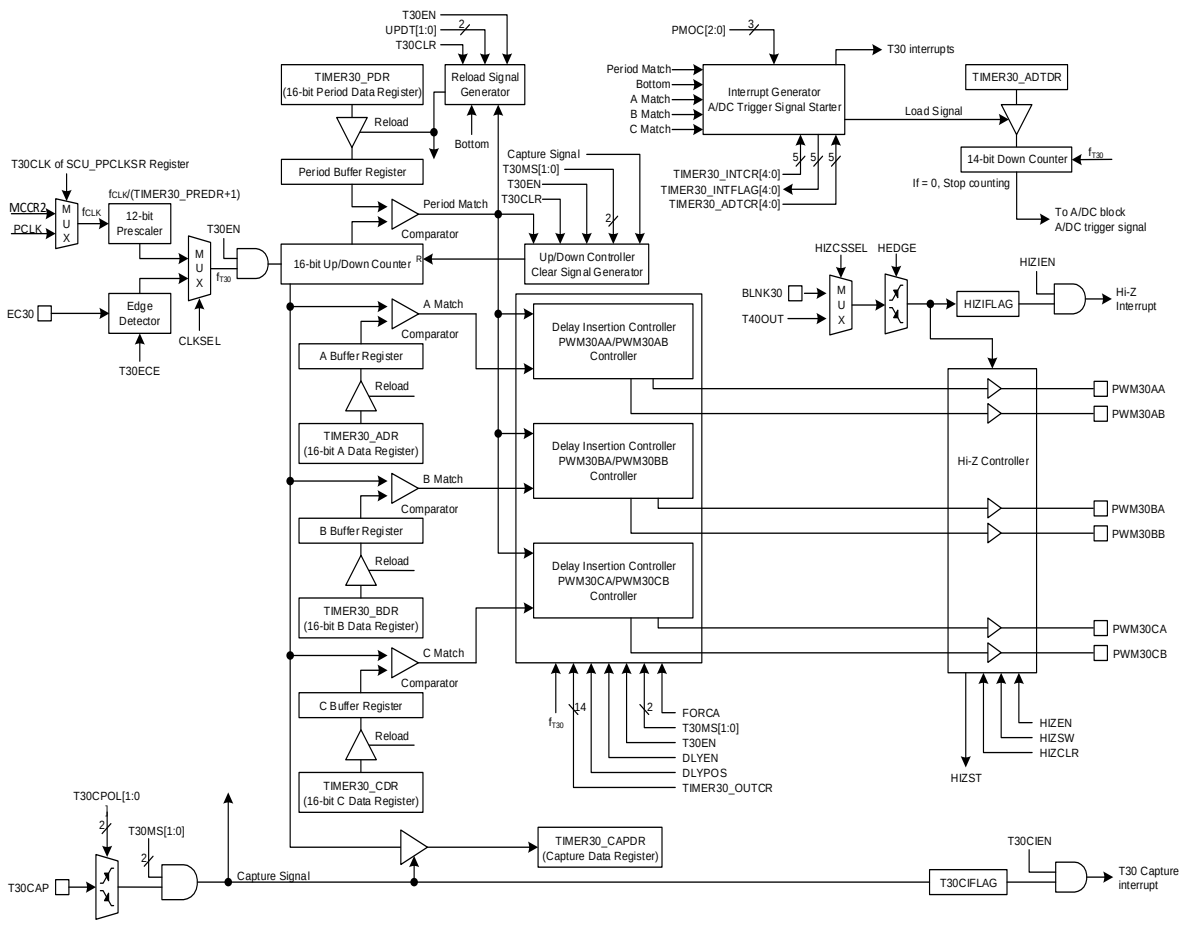
Table 24 introduces pins assigned for the timer counter 30.

Table 24. Pin Assignment of Timer Counter 30: External Pins

Pin name	Type	Description
EC30	I	External clock input
T30CAP	I	Capture input
BLNK30	I	External sync signal input
T40OUT	I	Internal sync signal Input (Timer40 Out)
PWM30AA	O	PWM output
PWM30AB	O	PWM output
PWM30BA	O	PWM output
PWM30BB	O	PWM output
PWM30CA	O	PWM output
PWM30CB	O	PWM output

13.1 Timer counter 30 block diagram

In this section, timer counter 30 is introduced in a block diagram.



NOTES:

1. The Period/A/B/C match interrupts except for Bottom can occur in the interval mode.
2. The Period match interrupt only can occur in the capture mode.
3. The 16-bit up/down counter in the capture mode is cleared to “0x0000” after the counter value is loaded to the TIMER30_CAPDR register at valid edge.
4. The HIZSW (high-impedance output software setting) bit can be used for debugging mode. That is, All T30PWM outputs can be high-impedance state with setting the HIZSW bit to ‘1’ by the UI of debugger.
5. After the T30EN bit is set, the counting of TIMER30_CNT may be delayed 2 clocks or more.

Figure 40. Timer Counter 30 Block Diagram

14. Timer counter 40

Timer counter 40 block comprises a single channel 16-bit general purpose timer. This has an independent 32-bit counter and a dedicated prescaler feeds counting clock. It supports periodic timer, PWM pulse, one-shot timer and capture mode. In addition, optional free-run timer is provided.

Main purpose of the timer counter 40 is a periodical tick timer, and main features are listed in the followings:

- 16-bit up-counter
- Periodic timer mode
- One-shot timer mode
- PWM pulse mode
- 3-Channel XOR Capture mode
- 12-bit prescaler
- Synchronous start and clear function

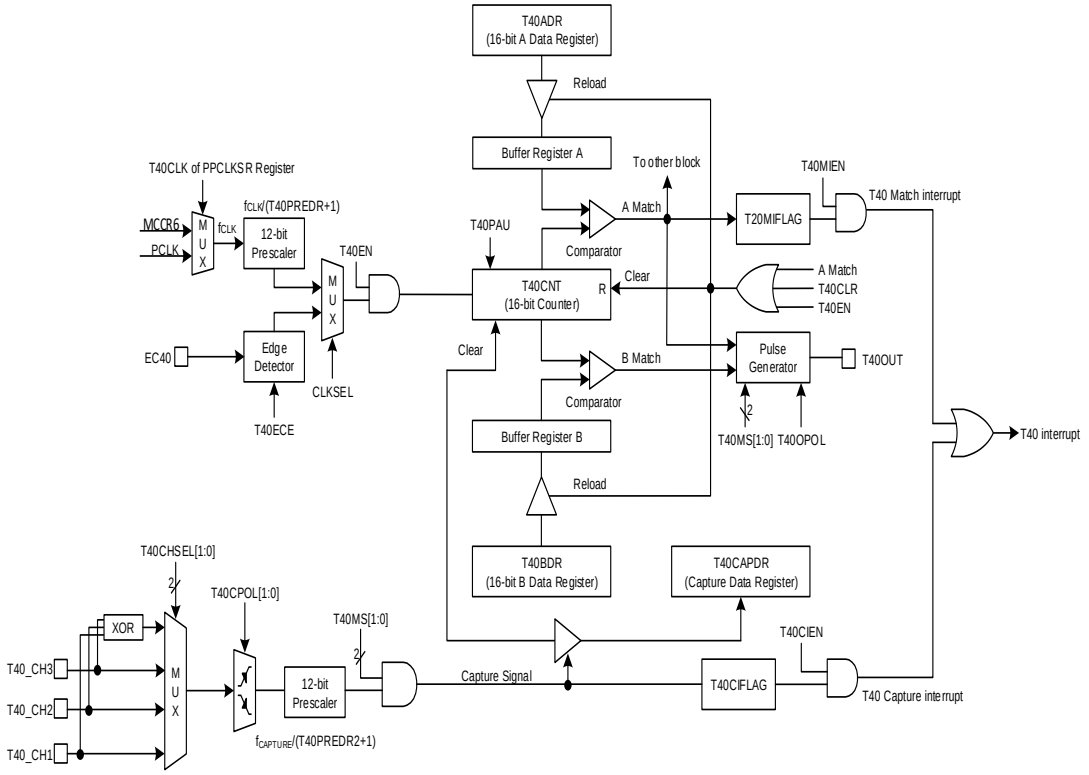
Table 25 introduces pins assigned for the timer counter 40.

Table 25. Pin Assignment of Timer Counter 40: External Pins

Pin name	Type	Description
EC40	I	External clock input
T40_CH1	I	Capture input
T40_CH2	I	Capture input
T40_CH3	I	Capture input
T40OUT	O	Timer/PWM/one-shot output

14.1 Timer counter 40 block diagram

In this section, timer counter 40 is introduced in a block diagram.



NOTES:

1. The T40EN is automatically cleared to logic “0” after one pulse is generated at a PPG one-shot mode.
2. After the T40EN bit is set, the counting of TIMER40_CNT may be delayed 2 clocks or more.

Figure 41. Timer Counter 40 Block Diagram

15. Universal synchronous/asynchronous receiver/transmitter

Universal Synchronous and Asynchronous serial Receiver and Transmitter (USART) is a highly flexible serial communication device. The main features are listed below:

- Full Duplex Operation. (Independent Serial Receive and Transmit Registers)
- Asynchronous or Synchronous Operation.
- Baud Rate Generator.
- Supports Serial Frames with 5,6,7,8, or 9 Data bits and 1 or 2 Stop bits.
- Odd or Even Parity Generation and Parity Check are Supported by Hardware.
- Data OverRun Detection.
- Framing Error Detection.
- Three Separate Interrupts on TX Completion, TX Data Register Empty and RX Completion.
- Double Speed Asynchronous communication mode.

Additional features are:

- 0% Error Baud Rate by floating point count register.
- Supports receive time out interrupt.
- Supports direct memory access and interrupt.

Table 26 introduces pins assigned for the USART.

Table 26. Pin Assignment of USART: External Pins

Pin name	Type	Description
TXD	O	UART Channel n transmit output
RXD	I	UART Channel n receive input
SS	I/O	SPIn Slave select input / output
SCK	I/O	SPIn Serial clock input / output
MOSI	I/O	SPIn Serial data (Master output, Slave input)
MISO	I/O	SPIn Serial data (Master input, Slave output)

NOTE: n = 10, 11, 12 and 13

15.1 USART block diagram

In this section, USART and SPIN are introduced in block diagrams.

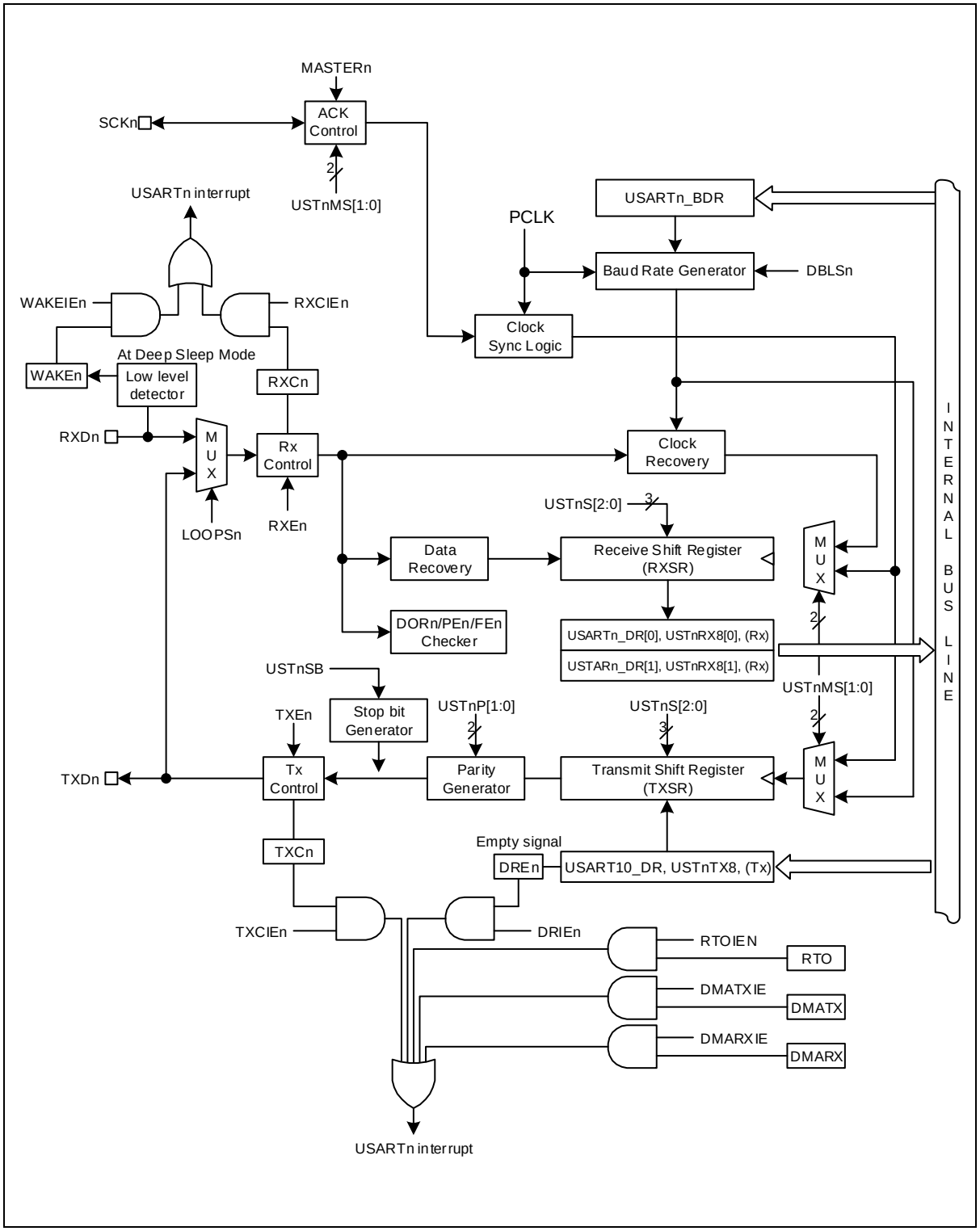


Figure 42. UART Block Diagram (n = 10, 11, 12, and 13)

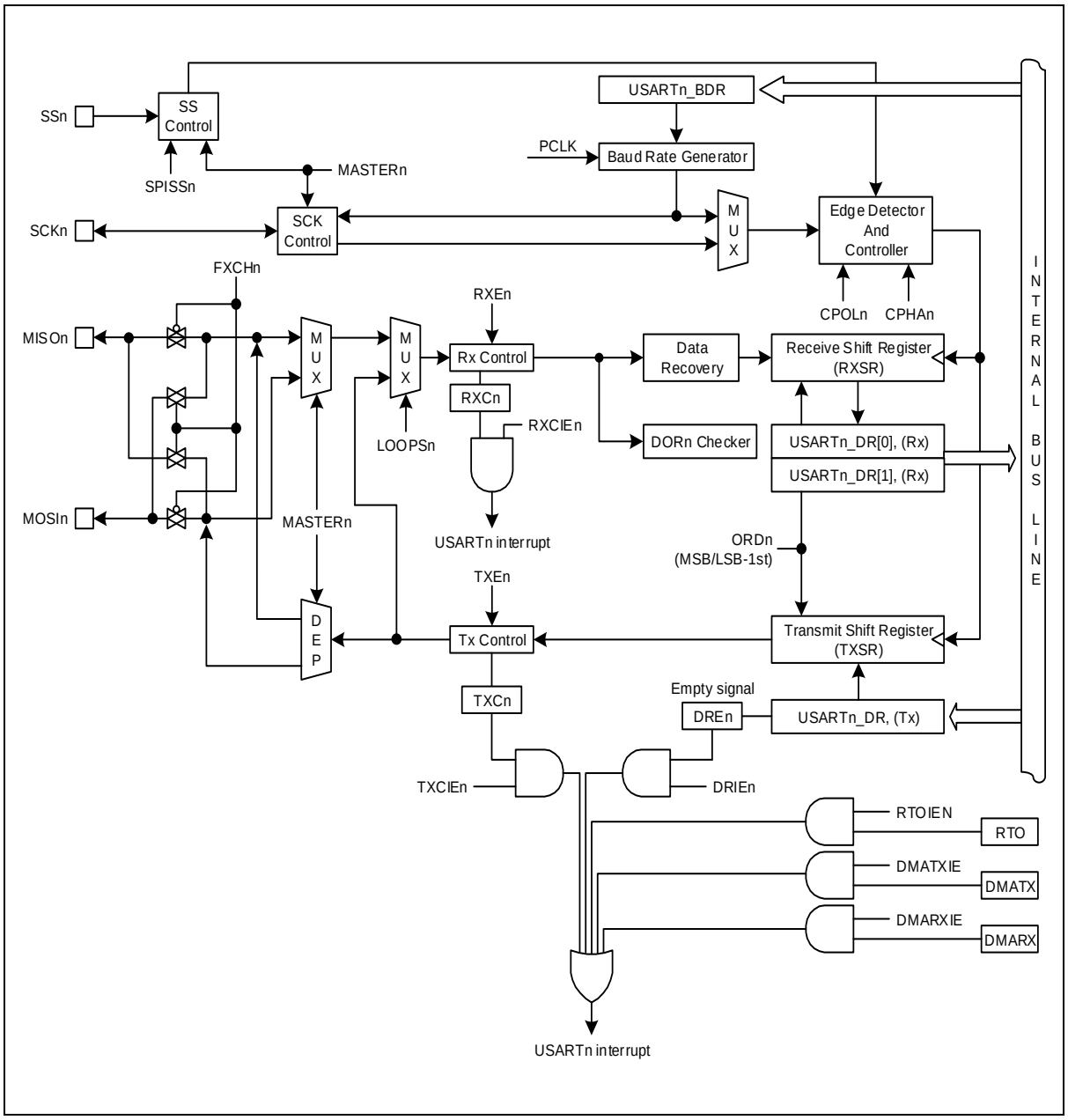


Figure 43. SPIN Block Diagram (n = 10, 11, 12, and 13)

16. I2C interface

I2C is one of industrial standard serial communication protocols, and which uses 2 bus lines such as Serial Data Line (SDAn) and Serial Clock Line (SCLn) to exchange data. Because both SDAn and SCLn lines are open-drain output, each line needs pull-up resistor respectively.

I2C features the followings (n = 0 and 1):

- Compatible with I2C bus standard.
- Multi-master operation.
- Up to 1MHz data transfer read speed.
- 7-bit address.
- Support two slave address.
- Both master and slave operation.
- Bus busy detection

Table 27 introduces pins assigned for I2C interface.

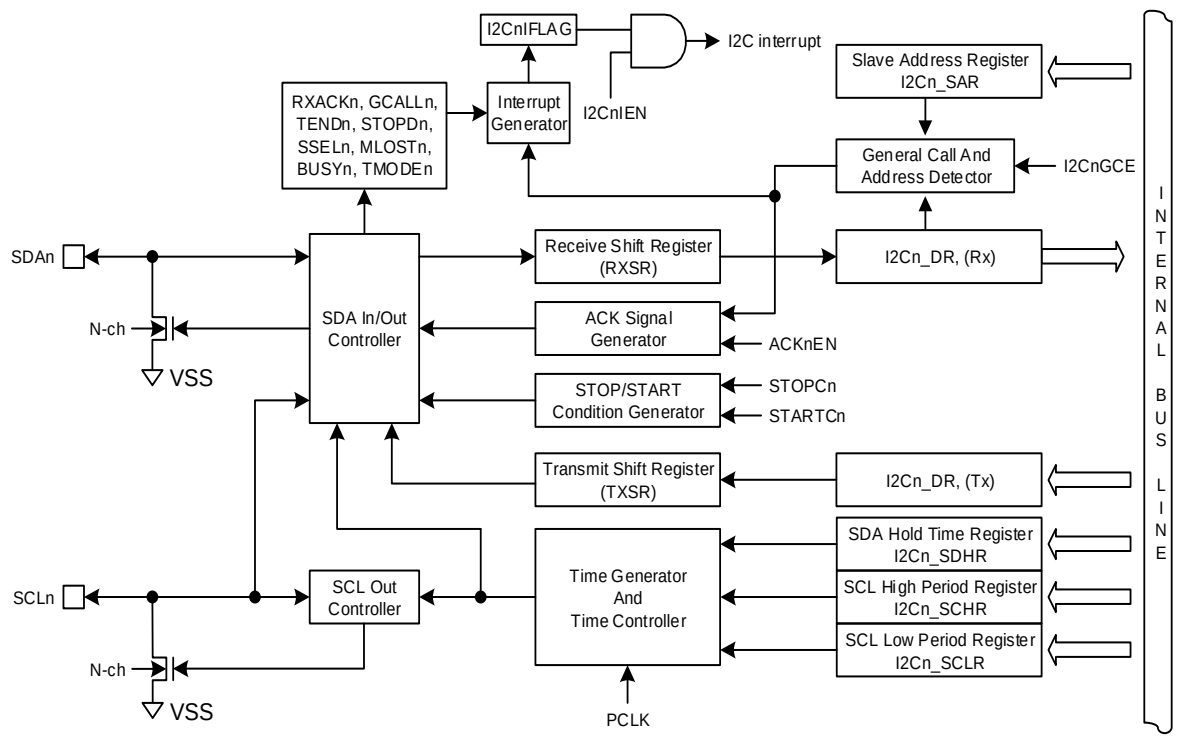
Table 27. Pin Assignment of I2C: External Pins

Pin name	Type	Description
SCL0	I/O	I2C channel 0 Serial clock bus line (open-drain)
SDA0	I/O	I2C channel 0 Serial data bus line (open-drain)
SCL1	I/O	I2C channel 1 Serial clock bus line (open-drain)
SDA1	I/O	I2C channel 1 Serial data bus line (open-drain)

NOTE: n = 0 and 1

16.1 I2C block diagram

In this section, I2C interface block is described in a block diagram.



NOTE: When the corresponding port of I2C is a sub-function for SCL/SDA pin, the SCL/SDA pins are automatically set to the N-channel open-drain outputs and the input latch is read in the case of reading the pins. The corresponding pull-up resistor is determined by the control register.

Figure 44. I2C Block Diagram

17. Serial peripheral interface (SPI)

A channel serial interface is provided for synchronous serial communications with external peripherals. SPI block support both of master and slave mode. Four signals will be used for SPI communication such as SS, SCK, MOSI, and MISO.

SPI of A31G32x series features the followings:

- Master or Slave operation.
- Programmable clock polarity and phase.
- 8, 9, 16, 17-bit wide transmit/receive register.
- 8, 9, 16, 17-bit wide data frame.
- Loop-back mode.
- Programmable start, burst, and stop delay time.
- DMA transfer operation.

Table 28 introduces pins assigned for SPI.

Table 28. Pin Assignment of SPI: External Pins

Pin name	Type	Description
SSn	I/O	SPIn Slave select input / output
SCKn	I/O	SPIn Serial clock input / output
MOSIn	I/O	SPIn Serial data (Master output, Slave input)
MISOn	I/O	SPIn Serial data (Master input, Slave output)

NOTE: n = 20 and 21

17.1 SPI block diagram

In this section, SPI is described in a block diagram in Figure 45.

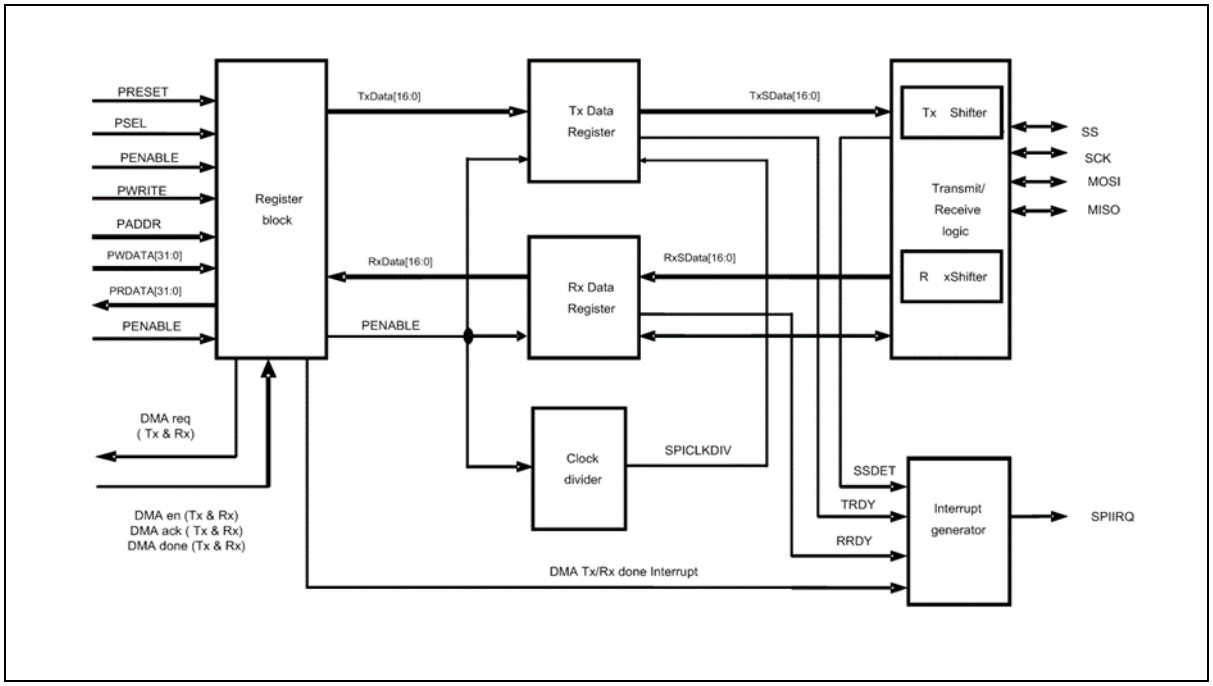


Figure 45. SPI Block Diagram

18. 12-bit ADC

ADC block of A31G32x series consists of an independent ADC unit featuring the followings:

- 16 Channel Analog Input
- Single mode and Continuous conversion mode
- Maximum 8 sequential conversion support
- Software trigger support
- Three internal trigger source (PWM, TIMER) Support
- Adjustable sample and hold time

Table 29 introduces pins assigned for ADC.

Table 29. Pin Assignment of ADC: External Signal

Pin name	Type	Description
AVDD	P	Analog Power(3.0V to VDD)
AVSS	P	Analog GND
AN0	A	ADC Input 0
AN1	A	ADC Input 1
AN2	A	ADC Input 2
AN3	A	ADC Input 3
AN4	A	ADC Input 4
AN5	A	ADC Input 5
AN6	A	ADC Input 6
AN7	A	ADC Input 7
AN8	A	ADC Input 8
AN9	A	ADC Input 9
AN10	A	ADC Input 10
AN11	A	ADC Input 11
AN12	A	ADC Input 12
AN13	A	ADC Input 13
AN14	A	ADC Input 14
AN15	A	ADC Input 15

18.1 12-bit ADC block diagram

In this section, 12-bit ADC is described in a block diagram in Figure 46.

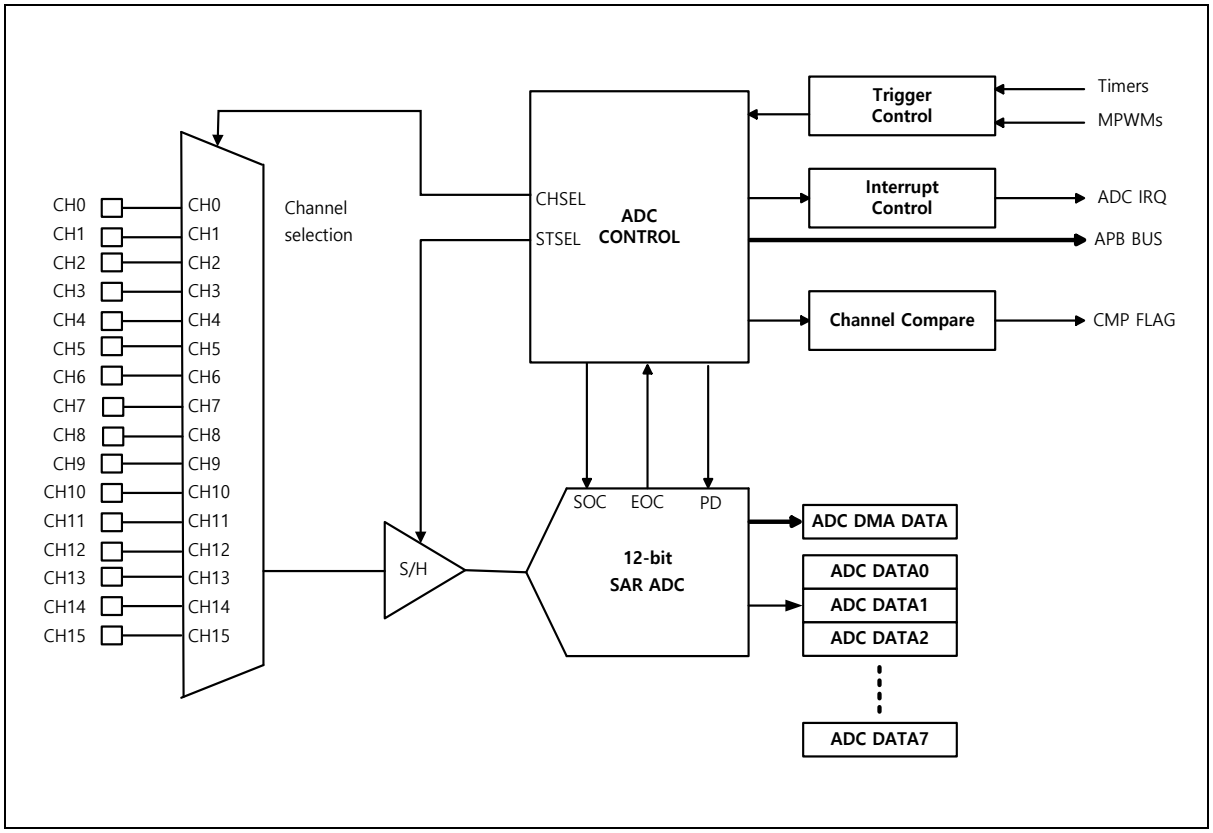


Figure 46. 12-bit ADC Block Diagram

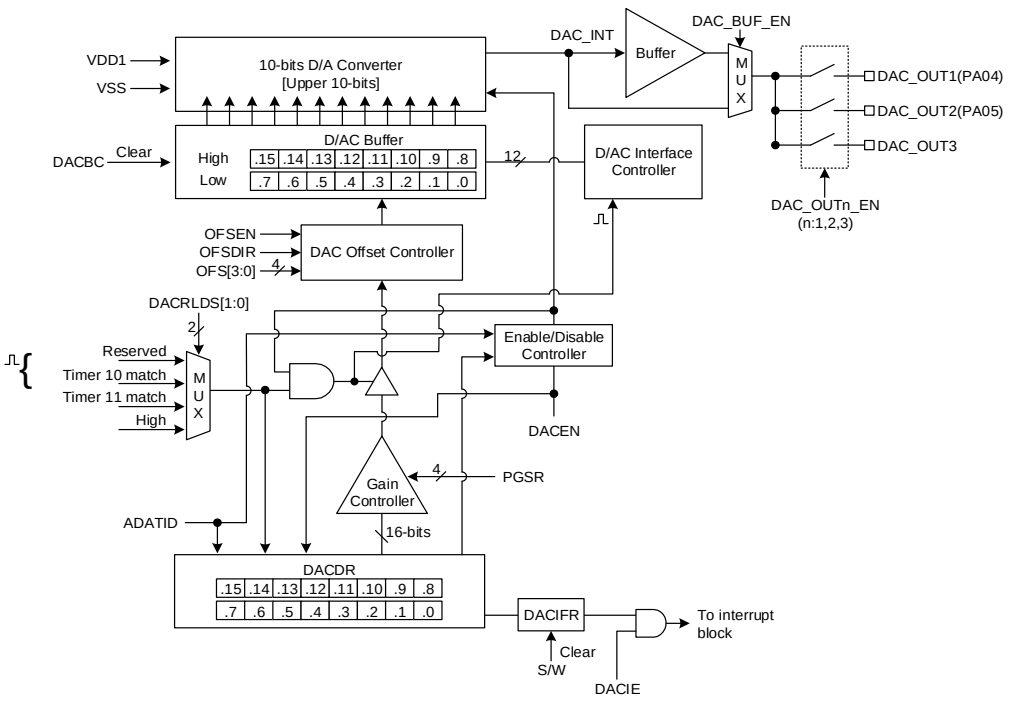
19. 10-bit DAC

Digital-to-analog (D/A) converter uses successive approximation logic to convert 10-bit digital value to an analog output level.

DAC module has six registers which are the DAC control register (DACCR), DAC data high register (DACDRH), DAC data low register (DACDRL), DAC buffer high register (DACBRH), DAC buffer low register (DACBRL) and programmable gain selection register (PGSR).

19.1 10-bit DAC block diagram and analog power pin

In Figure 47, 10-bit DAC is described in a block diagram.



NOTES:

1. Gain controller converts data in the sequence listed below:
   A. Get the DACDR[15:6] value.
   B. Adjust the data by selection gain.
   C. Write the data to the D/AC buffer.
2. DAC interface block doesn't work when DACRLDS bits of the DACCR register are set to "00b".

Figure 47. 10-bit DAC Block Diagram

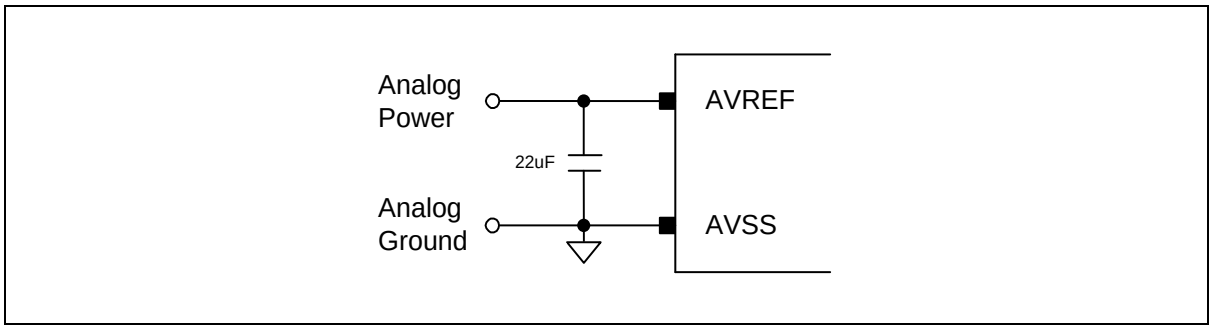


Figure 48. Analog Power (AVREF) Pin with a Capacitor

20. Comparator

Comparator of A31G32x series compares one analogue voltage level with external reference voltage, or internal reference voltage output voltage.

The comparator features the followings:

- 2 Comparators
- Internal BGR reference for comparator
- Comparator output de-bounce function
- Level and edge interrupt mode support for comparator

20.1 Comparator block diagram

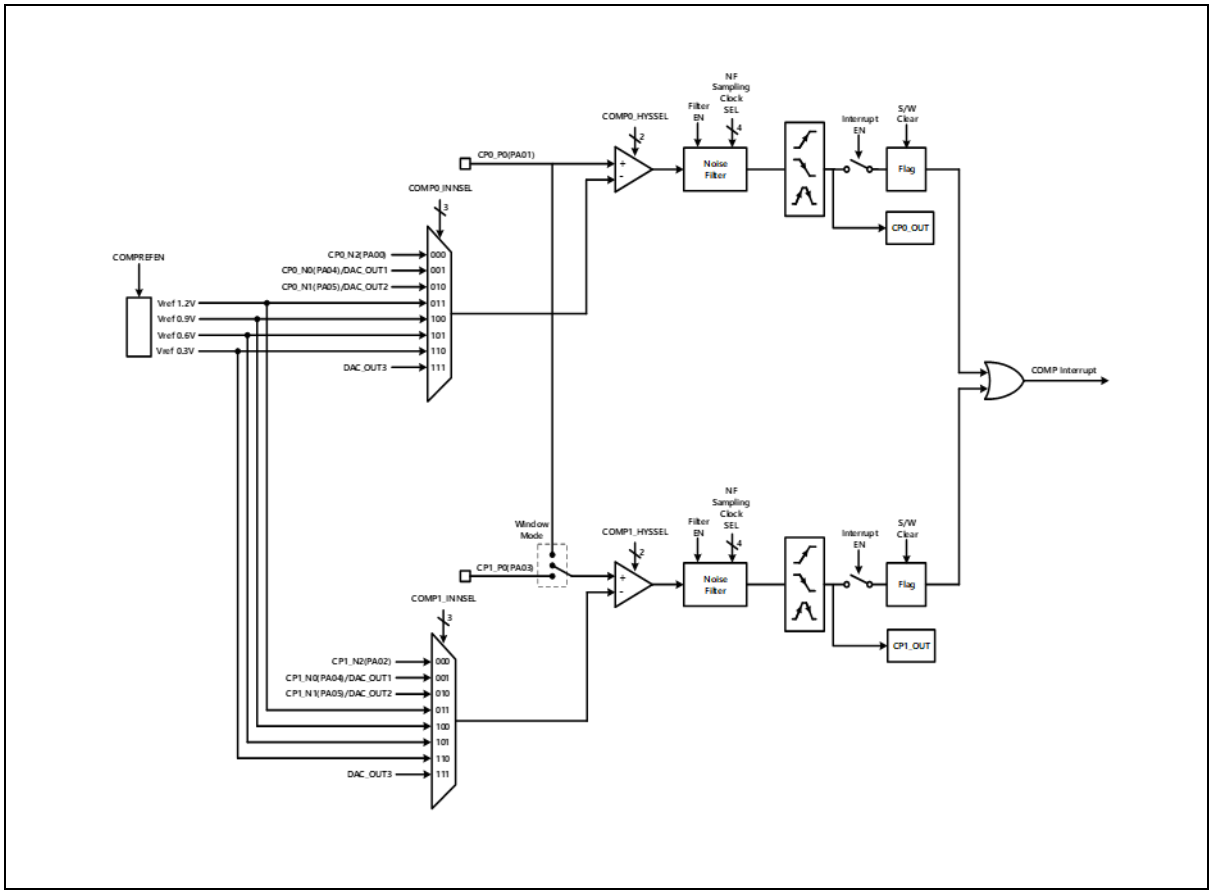


Figure 49. Comparator Block Diagram

21. Cyclic redundancy check and checksum (CRC checksum)

Cyclic redundancy check (CRC) generator is used to get a 16-bit CRC code from Flash ROM and a generator polynomial. Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the functional safety standards, they offer a means of verifying the Flash memory integrity. CRC generator helps compute a signature of the software during runtime, to be compared with a reference signature.

CRC generator of A31G32x series features the followings:

- Auto CRC (DMA) and User CRC Mode.
- Polynomial:
  - CRC-CCITT ($G_1(x) = x^{16} + x^{12} + x^5 + 1$)
  - CRC-16 ($G_2(x) = x^{16} + x^{15} + x^2 + 1$)
- CRC Mode and Checksum Mode.

21.1 CRC and checksum block diagram

Figure 50 describes the CRC and checksum in a block diagram.

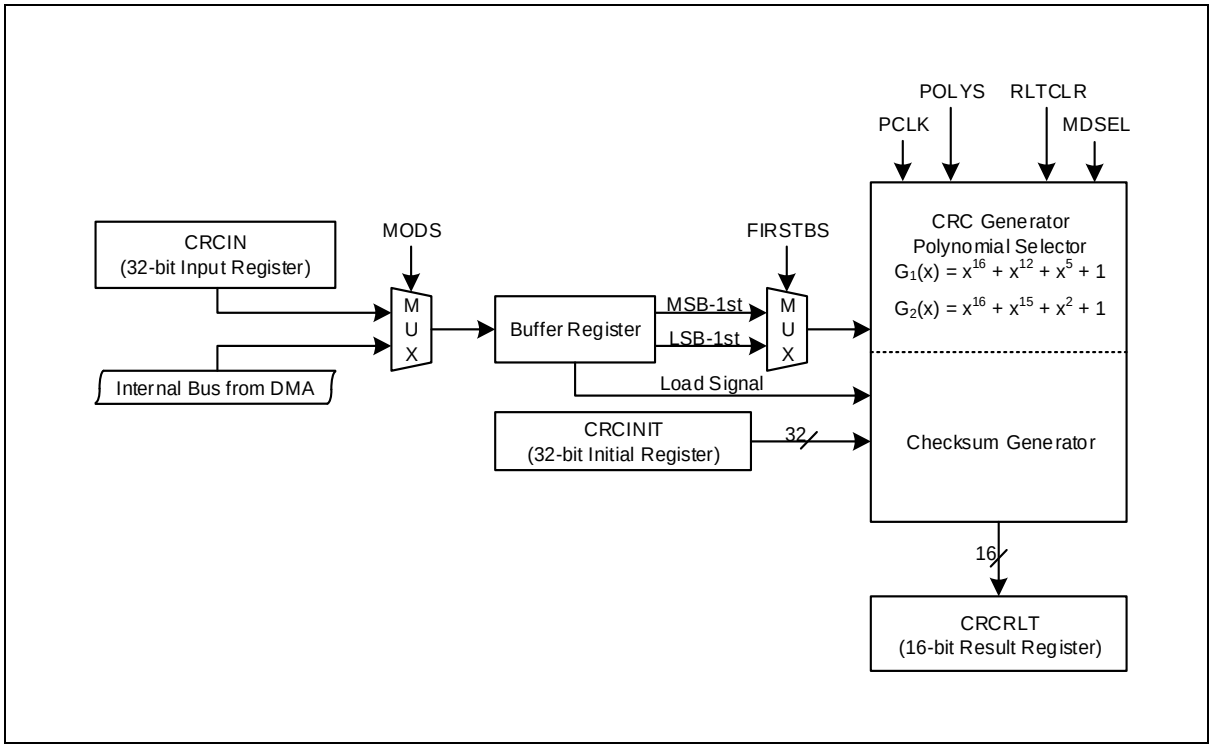


Figure 50. CRC and Checksum Block Diagram

22. USB full speed device interface

USB block of A31G24x series controls USB 2.0 full speed interface. The USB block features the followings:

- Support for the following speeds:
  - Full-Speed (FS, 12-Mbps)
  - Low-Speed (LS, 1.5-Mbps)
- USB 2.0 full-speed
- Configurable number of endpoints from 1 to 4
- 2 KB dynamic FIFO support.
- Control/bulk/interrupt transfer support.

22.1 USB block diagram

Figure 51 describes the USB interface block of A31G32x series in a block diagram.

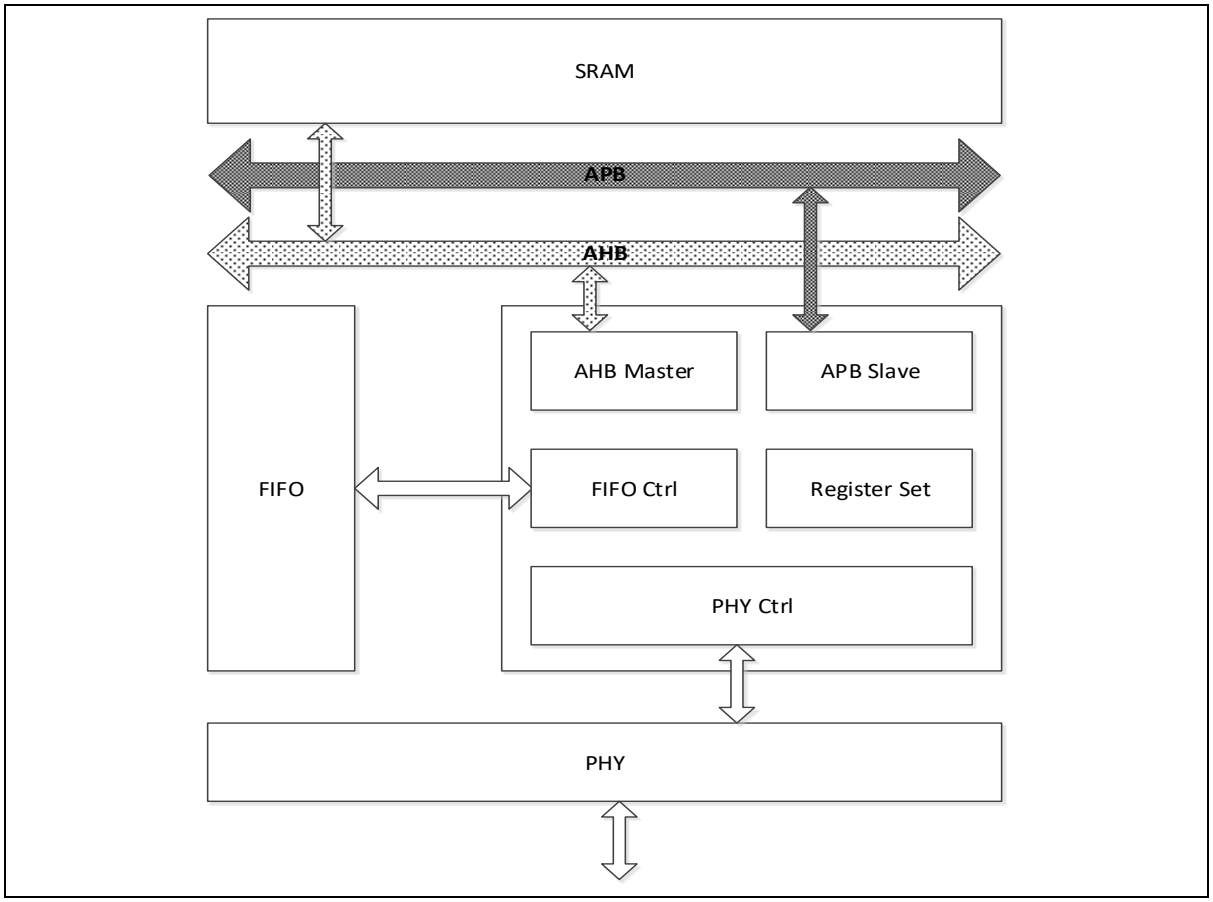


Figure 51. USB Interface Block Diagram

23. Real-time clock (RTC)

Real-time clock (RTC) of A31G32x series provides an automatic wakeup function to manage all low-power modes.

The RTC is an independent BCD timer/counter. It provides a time-of-day clock/calendar with programmable alarm interrupt. In addition, it includes a periodic programmable wakeup flag with interrupt capability. Eight RTC counters contain the sub-seconds, seconds, minutes, hours, week, day, month, and year expressed in binary coded decimal format (BCD). Compensations for 28-, 29- (leap year), 30-, and 31-day months are performed automatically. An error correction is available to compensate for variations in crystal oscillator accuracy.

In any mode of operation, the sub-second counter is never accessible. In normal operating mode, seven RTC counters are protected from read and write access. Read and write operation is possible only in RW mode. As long as the supply voltage remains in the operating range, the RTC never stops, regardless of the device status (run mode, low-power mode or under reset).

The RTC features the followings:

- LSI40KHz and MCCR5 clock as RTC clock (fRTC)
- Counters of year, month, week, day, hour, minute, and second (up to 99 years)
- Constant-period matching interrupt function (period: 0.5 seconds, 1 second, 1 minute, 1 hour, 1 day, 1 month)
- Alarm interrupt function (alarm: week, hour, minute)
- Timestamp interrupt and function
- Pin output of 1Hz clock
- Error correction by 1.53ppm resolution when using 32768Hz LSE
- Backup power mode operation support
- Four 32-bit backup registers (BKUR1~4) implemented in the RTC domain (remaining powered-on by VBAT when the VDD power is switched off)

Internal clock frequency for the RTC clock is detailed in electrical characteristic.

23.1 RTC block diagram

In this section, RTC block diagram is introduced in Figure 52.

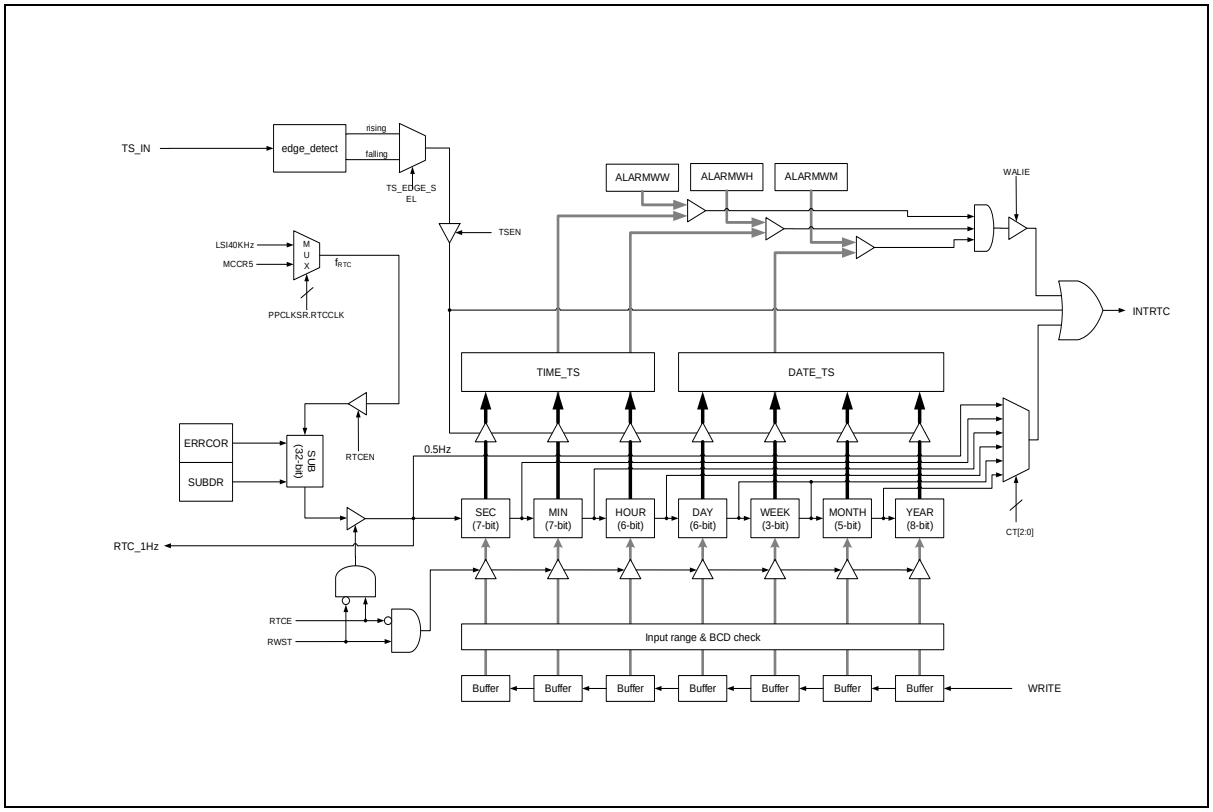


Figure 52. RTC Block Diagram

24. Temp sensor

Temp sensor is to use the internal oscillator LSITS by default, which has a large temperature variation. The temperature-dependent LSITS frequency can be calculated based on a precisely trimmed internal oscillator or an external clock. Reference clock and sense clock of the temp sensor can be changed by configuring TSENSECON register. When selecting the clock, frequency of the reference clock must be faster than the sense clock frequency. In SCU, each clock must be activated by configuring corresponding register. If value of TSREFCNT using REF clock matches the TSREFPERIOD set by the user, a match flag is generated and frequency of the sense clock is calculated by reading the value of TSSENSECNT at this time. Match flags can be used as interrupt sources.

Note) In order to use the sensor properly, it should be set **the reference clock of temperature sensor is minimum 8MHz.**

Glossary for this chapter

- HSI_I: HSI clock set by CSCR
- MCLK: System clock set by SCCR
- LSE: External sub oscillator
- LSITS: Internal temp sense oscillator
- LSI750KHz: Internal 750KHz oscillator
- LSI40KHz: Internal 40KHz oscillator

24.1 Temp sensor block diagram

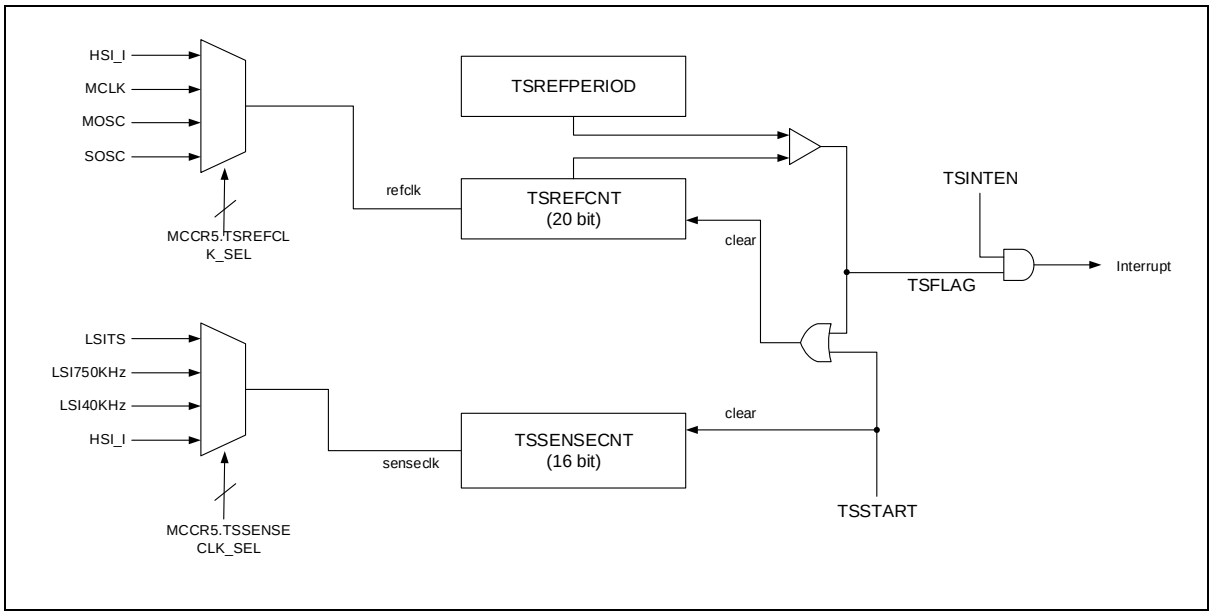


Figure 53. Temp Sensor Block Diagram

25. Electrical characteristics

25.1 Absolute maximum ratings

Absolute maximum ratings are limiting values of operating and environmental conditions which should not be exceeded under the worst possible conditions.

Table 30. Absolute maximum rating

Parameter	Symbol	Ratings	Unit	Note
Supply Voltage	VDD	-0.3 – +6.5	V	—
Normal Pin	V_I	-0.3 – VDD+0.3	V	Voltage on any pin with respect to VSS
	V_O	-0.3 – VDD+0.3	V	
	I_{OH}	25	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	ΣI_{OH}	100	mA	Maximum current (ΣI_{OH})
	I_{OL}	22	mA	Maximum current sunk by (I_{OL} per I/O pin)
	ΣI_{OL}	88	mA	Maximum current (ΣI_{OL})
Total Power Dissipation	T_P	300	mW	—
Storage Temperature	T_{STG}	-55 – +125	℃	—

25.2 Recommended operating conditions

Table 31. Recommended Operating Condition

(Temperature: -40℃ to +85℃)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Supply Voltage	VDD	—	1.8	—	5.5	V
		Use USB function	3.0	—	5.5	V
Operating Frequency	FREQ	HSE	2	—	16	MHz
		LSE	—	32.768	—	KHz
		HSI	46.56	48	49.44	MHz
		LSI750kHz	600	750	900	KHz
		LSI40kHz	22.8	40	62.6	KHz
Operating Temperature	Top	Top	-40	—	+85	℃

NOTE: AVDD must always be equal to or greater than VDDEXT

25.3 ADC characteristics

Table 32. ADC Electrical Characteristics

(Temperature: -40℃ to +85℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Operating voltage	AVDD		2.7	5	5.5	V
Resolution					12	Bit
Operating current	IDDA	AVDD = 5.0V @f_{MCLK} = 24MHz		1.6		mA
Analog input range	V_{AN}		VSS		AVDD	V
Conversion rate	F_{CONV}	@AVDD > 3.6V		—	1.5	MHz
		@AVDD > 3.0V			1	MHz
		@AVDD > 2.7V			0.5	MHz
Operating frequency	ACLK				25	MHz
DC accuracy	INL	AVDD = 5.0V		±3	±6	LSB
	DNL	AVDD = 5.0V		±2	±3	LSB
Error Of Bottom	EOB			±4		LSB
Error Of Top	EOT			±4		LSB

NOTE) AVDD must always be equal to or greater than VDDEXT

25.4 DAC characteristics

Table 33. DAC Electrical Characteristics

(Temperature: -40℃ to +85℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Operating voltage	AVDD		2.7	5	5.5	V
Resolution	-	-	-	10		BIT
Load Resistance with Buffer	R_{LOAD}	Load connected to VSS	5	-	-	kΩ
		Load connected to VAVDD	25	-	-	kΩ
Output Impedance Without Buffer	R_O		-	-	130	kΩ
DAC Output Voltage	D_{AOUT}		0.2	-	AVDD - 0.2	V
Operating Current	$I_{AVDD,rms}$	No load, middle code(0x200)	-	1.48	0.95	mA
DNL	-	No R-Load, DAC Output	-	±1	±2	LSB
	-	R-Load=5kΩ, C-Load=50pF, DAC Output	-	±2	±8	
INL	-	No R-Load, DAC Output	-	±3	±5	LSB
	-	R-Load=5kΩ, C-Load=50pF, DAC Output	-	±4	±8	
Offset	-	Offset Error is difference between measured value at Code (0x200) and the ideal value(AVDD/2)	-	-	8	LSB
Gain Error	-		-	1.0	-	%
Conversion Time	$t_{SETTLINB}$		-	2	4	us
Stop Current			-	2	400	nA

NOTE

1. AVDD must always be equal to or greater than VDDEXT
2. Data based on characterization results, not tested in production

25.5 Power on reset characteristics

Table 34. POR Electrical Characteristics

(Temperature: -40℃ to +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
POR set level	V_{set}	—	1.05	1.2	1.35	V
POR reset level	V_{reset}	—	0.9	1.1	1.3	V
VDD rise time rate	T_{rVDD}	—	0.02	-	20	ms/V
VDD fall time rate	T_{fVDD}	—	0.4	-	20	ms/V

25.6 Low voltage reset/indicator characteristics

Table 35. Low Voltage Reset/Indicator Characteristics

(Temperature: -40℃ to +85℃)

Parameter	Symbol		Conditions	Min	Typ	Max	Units
Operating voltage	VDD			1.5	5	5.5	V
Detection level	V_{LVR}	Level0	Rising voltage	1.56	1.68	1.80	V
			Falling voltage	-	1.63	1.74	
		Level1	Rising voltage	1.65	1.77	1.89	
			Falling voltage	1.60	1.72	1.84	
		Level2	Rising voltage	1.74	1.87	2.00	
			Falling voltage	1.70	1.82	1.94	
		Level3	Rising voltage	1.85	1.99	2.13	
			Falling voltage	1.81	1.94	2.07	
		Level4	Rising voltage	1.95	2.09	2.23	
			Falling voltage	1.89	2.03	2.17	
		Level5	Rising voltage	2.07	2.22	2.37	
			Falling voltage	2.01	2.16	2.31	
		Level6	Rising voltage	2.23	2.40	2.57	
			Falling voltage	2.19	2.35	2.51	
		Level7	Rising voltage	2.41	2.59	2.77	
			Falling voltage	2.35	2.52	2.69	
		Level8	Rising voltage	2.61	2.80	2.99	
			Falling voltage	2.53	2.72	2.91	
		Level9	Rising voltage	2.96	3.18	3.40	
			Falling voltage	2.89	3.10	3.31	
		Level10	Rising voltage	3.10	3.33	3.56	
			Falling voltage	3.02	3.24	3.46	
		Level11	Rising voltage	3.50	3.76	4.02	
			Falling voltage	3.41	3.66	3.91	
		Level12	Rising voltage	3.63	3.90	4.17	
			Falling voltage	3.53	3.79	4.05	
		Level13	Rising voltage	3.93	4.22	4.51	
			Falling voltage	3.83	4.11	4.39	
		Level14	Rising voltage	4.09	4.40	4.71	
			Falling voltage	3.99	4.28	4.57	
		Level15	Rising voltage	4.37	4.69	5.01	
			Falling voltage	4.26	4.57	4.88	
Hysteresis	—			—	100	200	mV
Noise cancelling time	—			—	2	-	us
Operation current	I_{DD}			—	3.5	5	uA
Operation current(STOP)	$I_{DD, STOP}$			—	2.5	3	nA

25.7 High frequency internal RC oscillator characteristics

Table 36. High Frequency Internal RC Oscillator Characteristics

(Temperature: -40℃ to +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating current	I_{HIRC}	Enable	—	350	450	uA
		Disable	—	0.6	70	nA
Frequency	f_{HIRC}	VDD = 1.8V to 5.5V T_A = – 40°C to +85℃	46.56	48	49.44	MHz
		VDD = 1.8V to 5.5V T_A = 0°C to +50℃	47.28	48	48.72	MHz

25.8 Low frequency internal RC oscillator characteristics

Table 37. Low Frequency (750KHz) Internal RC Oscillator Characteristics

(Temperature: -40℃ to +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating voltage	VDD		1.8	5	5.5	V
Operating current	I_{LIRC}	Enable	—	1.5	2	uA
		Disable	—	1	20	nA
Frequency	f_{LIRC}	VDD = 1.8V to 5.5V	600	750	900	kHz
Stabilization time	t_{LFS}	—	—	100		us

Table 38. Low Frequency (40KHz) Internal RC Oscillator Characteristics

(Temperature: -40℃ to +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating voltage	VDD		1.8	5	5.5	V
Operating current	I_{LIRC}	Enable	—	305	588.2	nA
		Disable	—	—	1	nA
Frequency	f_{LIRC}	VDD = 1.8V to 5.5V	22.8	40	62.6	KHz
Stabilization time	t_{LFS}	—	—	100		us

25.9 DC electrical characteristics

Table 39. DC Electrical Characteristics

(Temperature: -40℃ to +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input high voltage	V_{IH}	PA,PB,PC,PF, nRESET, nBOOT	0.8VDD	—	VDD	V
Input low voltage	V_{IL}	PA,PB,PC,PF, nRESET, nBOOT	—	—	0.2VDD	V
Input hysteresis	△V	All input pins, nRESET, nBOOT VDD=3V	100	200	—	mV
Output high voltage	V_{OH1}	VDD=5V, I_{OH1} = – 2.64mA; PA[15:11],PA[4:0],PB[12:6], PB[2],PC[12:4],PC[1:0], PF[2:0]	0.8VDD	—	—	V
	V_{OH2}	VDD=5V, I_{OH2} = – 4mA; PA[10:5], PB[15:13, 5:3, 1:0], PC[3:2]	0.8VDD	—	—	V
	V_{OH3}	VDD=5V, I_{OH3} = – 1mA; PC[15:13]	VDD-0.5	—	—	V
Output low voltage	V_{OL1}	VDD=5V, I_{OL1}=3.6mA; PA[15:11],PA[4:0],PB[12:6], PB[2],PC[15:4],PC[1:0],PF[2:0]	—	—	0.2VDD	V
Output low voltage	V_{OL2}	VDD=5V, I_{OL2}=3.6mA; PA[10:5], PB[15:13, 5:3, 1:0], PC[3:2]	—	—	0.2VDD	V
Input high leakage current	I_{IH}	All Input ports	—	—	1	uA
Input low leakage current	I_{IL}	All Input ports	– 1	—	—	uA
Pull-up resistor	R_{PU}	V_I=0V, T_A=25°C, VDD=5V PA,PB,PC,PF	25	50	100	KΩ
		V_I=0V, T_A=25°C, VDD=5V nRESET, nBOOT	150	250	400	
Pull-down resistor	R_{PD}	V_I=VDD, T_A=25°C, VDD=5V PA,PB,PC,PF	25	50	100	KΩ

25.10 Supply current characteristics

Table 40. Supply Current Characteristics

(Temperature: -40 to +85℃)

Parameter	Symbol	Conditions		Typ	Max	Units
Supply current	I_{DD1} (Run)	f_{XIN} = 8MHz	VDD=5V±10% All peripherals off	3	—	mA
		f_{HIRC} = 12MHz		2.5	—	
		f_{HIRC} = 48MHz		8	—	
		F_{LIRC} = 750KHz		250	—	uA
		F_{LSE} = 32.768KHz		1	—	
	I_{DD2} (Sleep)	f_{XIN} = 8MHz	VDD=5V±10% All peripherals off	2.5	—	mA
		f_{HIRC} = 12MHz		2	—	
		f_{HIRC} = 48MHz		6	—	
		F_{LIRC} = 750KHz		250	—	uA
		F_{LSE} = 32.768KHz		1	—	
	I_{DD3} (Stop)	All Oscillators Off	VDD=5V±10%	2	—	uA
		Only LSE on		3.5	—	
		Only LSI40K on		3.5	—	
		Only LVR on		6	—	
	I_{DD4} (Standby)	All Oscillators Off	VDD=5V±10%	1.5	—	uA
		Only LSE on		2	—	
		Only LSI40K on		2	—	
		Only LVR on		5	—	
	I_{DD5} (Backup power)	All Oscillators Off	VDD=5V±10%	1.3	—	uA
		Only LSE on		1.6	—	
		Only LSE + RTC on		1.7	—	
		Only LSI40K on		1.5	—	

NOTES:

1. Where the f_{XIN} is an external main oscillator, the f_{SUB} is an external sub oscillator, the f_{HIRC} is a high frequency internal RC oscillator, and the f_x is the selected system clock.
2. All supply current items don't include the current of a low frequency internal RC oscillator and a peripheral block.
3. All supply current items include the current of the power-on reset (POR) block.

25.11 AC characteristics

Table 41. AC Characteristics

(Temperature: -40℃ to +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
RESETB input low width	t_{RST}	VDD = 5V	10	—	—	us
Interrupt input high low width	t_{IWH}, t_{IWL}	All interrupts, VDD = 5V	100	—	—	ns
External counter input high low pulse width	t_{ECWH}, t_{ECWL}	VDD = 5V All external counter input	100	—	—	
External counter transition time	t_{REC}, t_{FEC}	Ecn, VDD = 5V All external counter input	—	—	20	

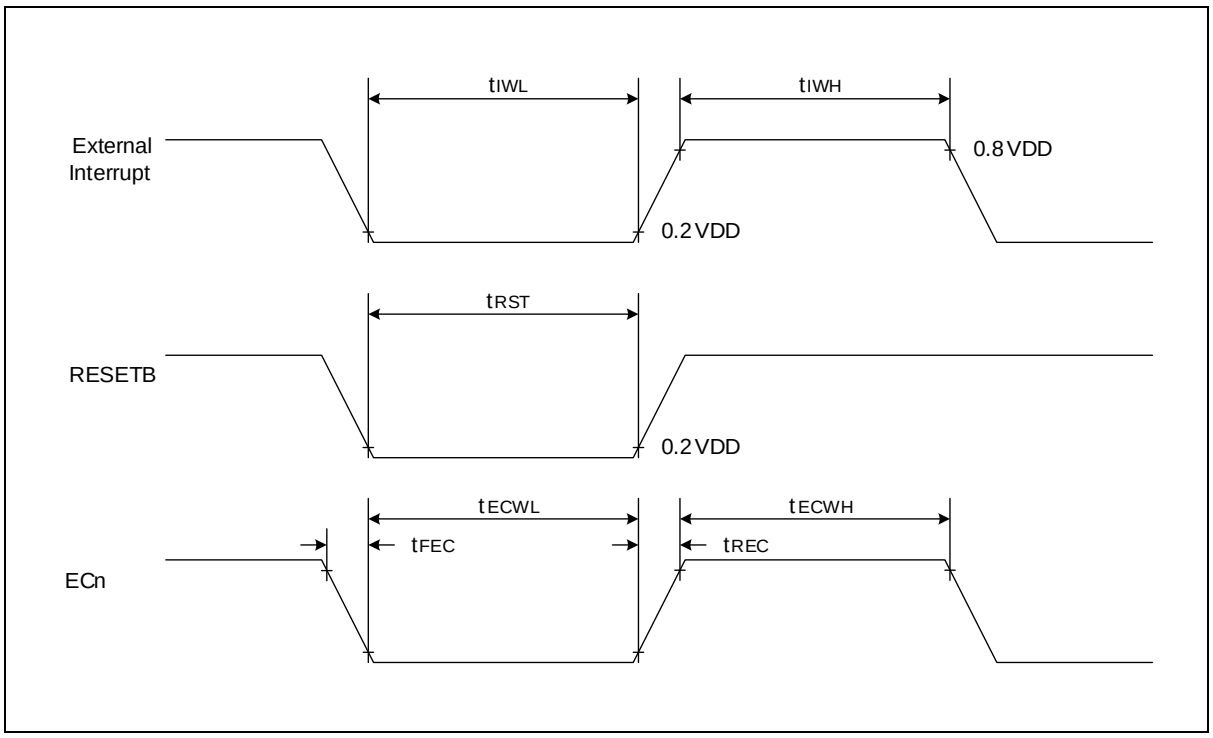


Figure 54. AC Timing

25.12 USART SPI characteristics

Table 42. SPI Characteristics with High Voltage

(Temperature: -40℃ to +85℃, VDD = 3V to 5.5V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SPI Clock frequency	f_{SCK} $1/f_{c(SCK)}$	Master mode	—	—	12	MHz
		Slave mode	—	—	6	
Output clock pulse period	t_{SCK}	Internal SCK source	80	—	—	ns
Input clock pulse period		External SCK source	80	—	—	
Output clock high, low pulse width	t_{SCKH}, t_{SCKL}	Internal SCK source	16	—	—	
Input clock high, low pulse width		External SCK source	16	—	—	
First output clock delay time	t_{FOD}	Internal/external SCK source	40	—	—	
Output clock delay time	t_{DS}	—	—	—	25	
Input setup time	t_{DIS}	—	36`	—	—	
Input hold time	t_{DIH}	—	36	—	—	

Note) The speed of support for SPI clock frequency depends on the VDD value.

Table 43. SPI Characteristics with Low Voltage

(Temperature: -40℃ to +85℃, VDD = 1.8V to 3V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SPI Clock frequency	f_{SCK} $1/f_{c(SCK)}$	Master mode	—	—	6	MHz
		Slave mode	—	—	6	
Output clock pulse period	t_{SCK}	Internal SCK source	160	—	—	ns
Input clock pulse period		External SCK source	160	—	—	
Output clock high, low pulse width	t_{SCKH}, t_{SCKL}	Internal SCK source	32	—	—	
Input clock high, low pulse width		External SCK source	32	—	—	
First output clock delay time	t_{FOD}	Internal/external SCK source	80	—	—	
Output clock delay time	t_{DS}	—	—	—	50	
Input setup time	t_{DIS}	—	72	—	—	
Input hold time	t_{DIH}	—	72	—	—	

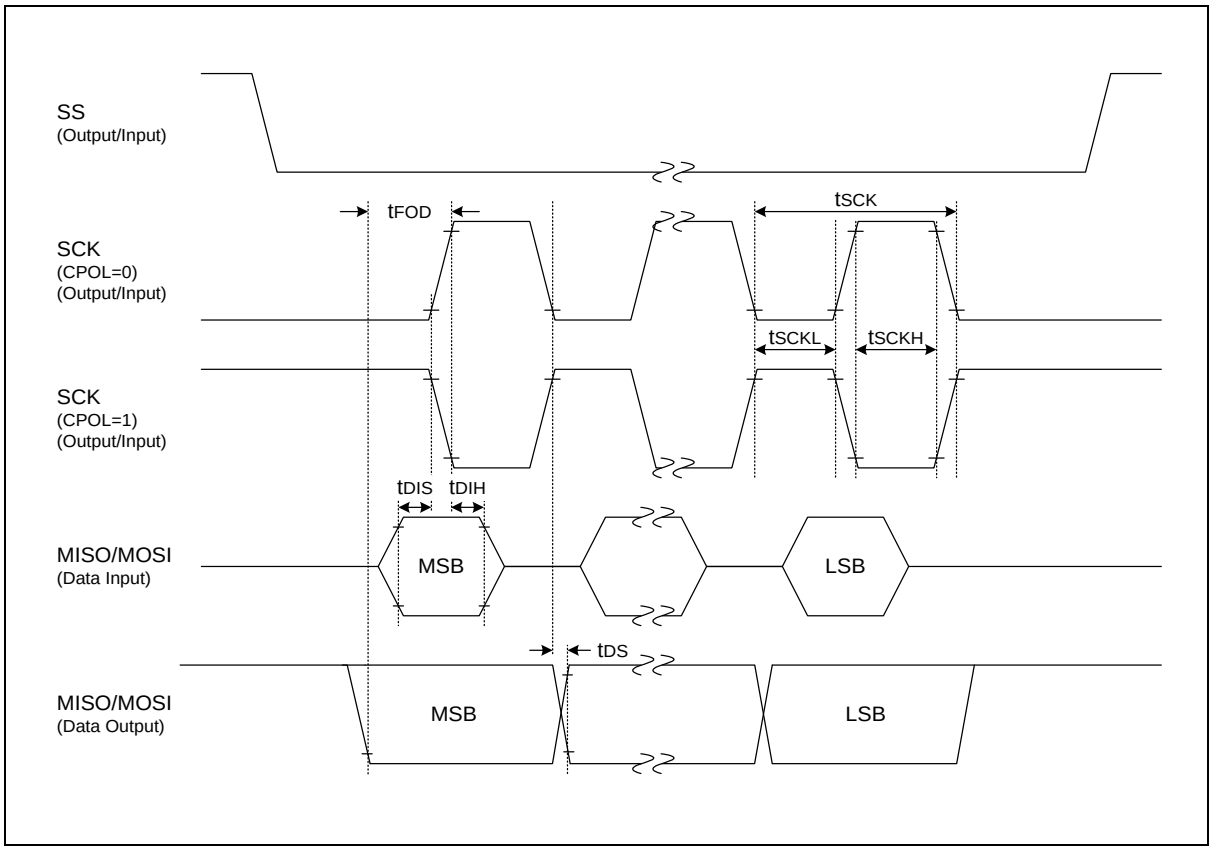


Figure 55. SPI Timing

25.13 I2C characteristics

Table 44. I2C Characteristics

(Temperature: -40℃ to +85℃, VDD = 1.8 to 5.5V)

Parameter	Symbol	Standard		Fast		Fast Plus		Units
		Min	Max	Min	Max	Min	Max	Units
Clock frequency	t_{SCL}	0	100	0	400	0	1000	KHz
Clock high pulse width	t_{SCLH}	4.0	—	0.6	—	0.26	—	us
clock low pulse width	t_{SCLL}	4.7	—	1.3	—	0.5	—	
Bus free time	t_{BF}	4.7	—	1.3	—	0.5	—	
Start condition setup time	t_{STSU}	4.7	—	0.6	—	0.26	—	
Start condition hold time	t_{STHD}	4.0	—	0.6	—	0.26	—	
Stop condition setup time	t_{SPSU}	4.0	—	0.6	—	0.26	—	
Stop condition hold time	t_{SPHD}	4.0	—	0.6	—	0.26	—	
Output valid from clock	t_{VD}	0	—	0	—	0	—	
Data input hold time	t_{DIH}	0	—	0	1.0	0	0.45	
Data input setup time	t_{DIS}	250	—	100	—	50	—	ns

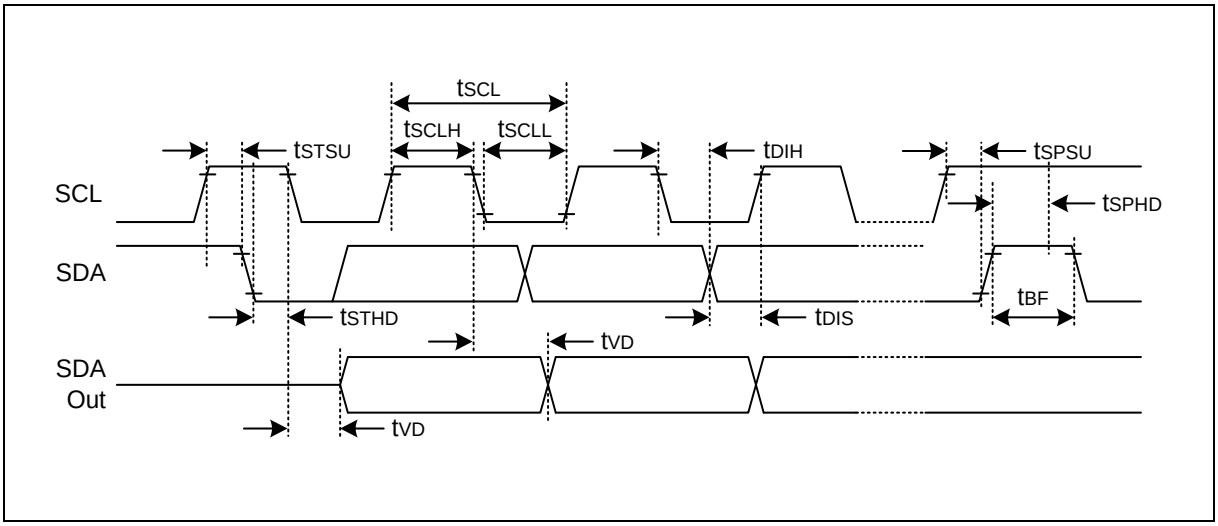


Figure 56. I2C Timing

25.14 USART UART timing characteristics

Table 45. UART Timing Characteristics

(Temperature: -40℃ to +85℃, VDD = 1.8 to 5.5V)

Parameter	Symbol	Min	Typ	Max	Units
Serial port clock cycle time	t_{SCK}	1250	t_{CPU} x 16	1650	ns
Output data setup to clock rising edge	t_{S1}	590	t_{CPU} x 13	—	
Clock rising edge to input data valid	t_{S2}	—	—	590	
Output data hold after clock rising edge	t_{H1}	t_{CPU} – 50	t_{CPU}	—	
Input data hold after clock rising edge	t_{H2}	0	—	—	
Serial port clock High, Low level width	t_{HIGH}, t_{LOW}	470	t_{CPU} x 8	970	

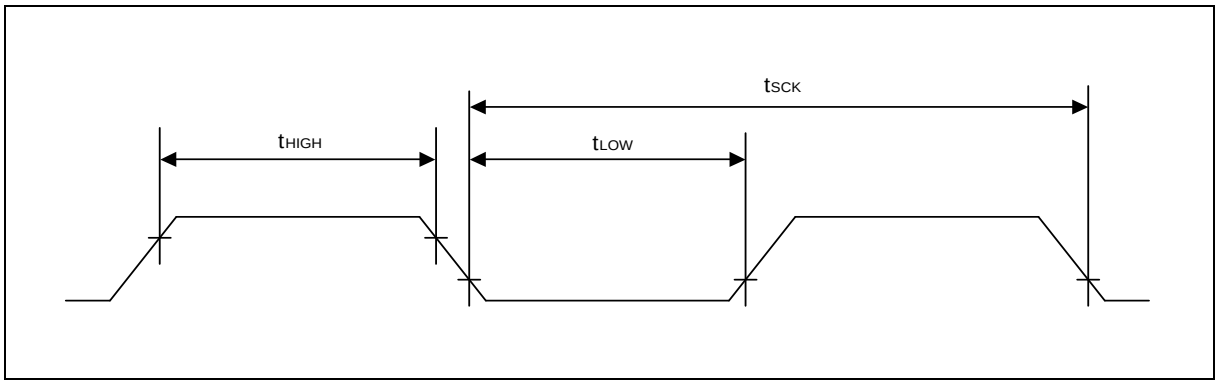


Figure 57. Waveform of UART Timing Characteristics

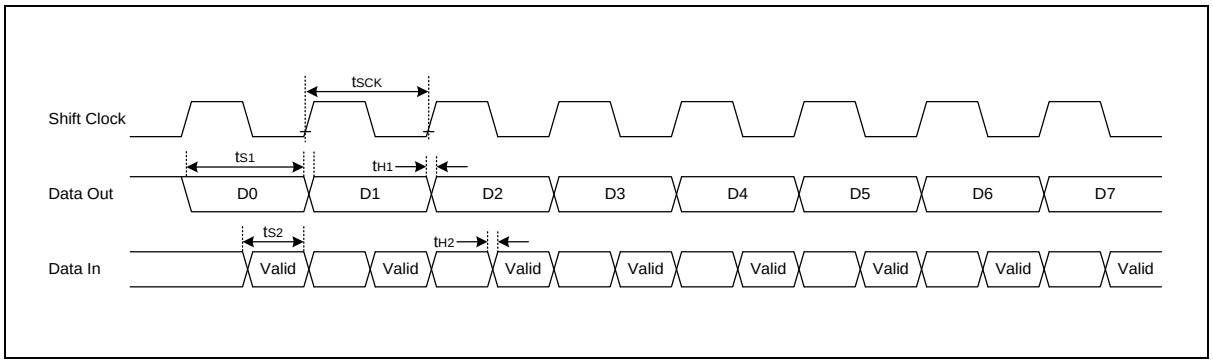


Figure 58. UART Module Timing

25.15 Data retention voltage in STOP mode

Table 46. Data Retention Voltage in STOP mode

(Temperature: -40℃ to +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Data retention supply voltage	V_{DDDR}	—	1.8	—	5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.8V, (T_A = 25°C), Deep sleep mode	—	—	1	uA

25.16 Internal Flash ROM characteristics

Table 47. Internal Flash ROM Characteristics

(Temperature: -40℃ to +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Page write time	t_{FSW}	—	—	30	—	us
Page erase time	t_{FSE}	—	—	4	—	ms
Chip erase time	t_{FCE}	—	—	8	—	ms
Read Access Time	t_{FRA}	—	30	—	80	ns
Flash program voltage	V_{PGM}	On erase/write	1.65	—	5.5	V
Endurance of write/erase	N_{FWE}	T_A=25 ˚C, Page unit	100,000	—	—	Times
Retention time	t_{FRT}		10	—	—	Years

25.17 Main oscillator characteristics

Table 48. Main Oscillator Characteristics

(Temperature: -40℃ to +85℃)

Oscillator	Parameter	Conditions	Min	Typ	Max	Units
Operating voltage	VDD	—	1.8	5.0	5.5	V
Operating current	IDD	—	—	—	2.5	mA
Power down current	I_{STOP}	—	—	0.2	30	nA
Output frequency	XOUT input frequency	VDDEXT≥1.8V ISEL_I<1:0>=2'b11	2.0	—	4.0	MHz
		VDDEXT≥2.0V ISEL_I<1:0>=2'b10	2.0	—	8.0	MHz
		VDDEXT≥2.2V ISEL_I<1:0>=2'b01	2.0	—	12.0	MHz
		VDDEXT≥2.4V ISEL_I<1:0>=2'b00	2.0	—	16	MHz
Start-up time	T_{start}	—	—	2	—	ms
Crystal input (low)	V_{IL}	—	—	—	0.2VDD	V
Crystal input (high)	V_{IH}	—	0.8VDD	—	—	V
Crystal out (low)	V_{OL}	—	—	—	0.2VDD	V
Crystal out (high)	V_{OH}	—	0.8VDD	—	—	V
External load cap	C_L	2M<f_{OUT}<4M	18	30	35	pf
		4M<f_{OUT}<12M	10	22	30	pf
		12M<f_{OUT}<16M	7	18	22	pf
Feedback resistance	R_{FB}	VDDEXT=5V	0.7	1.0	1.3	MΩ

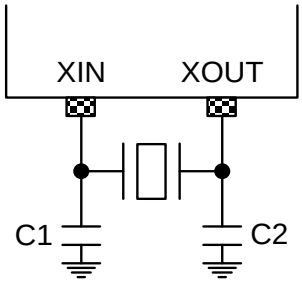


Figure 59. Crystal/Ceramic Oscillator

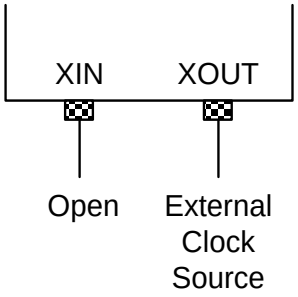


Figure 60. External Clock

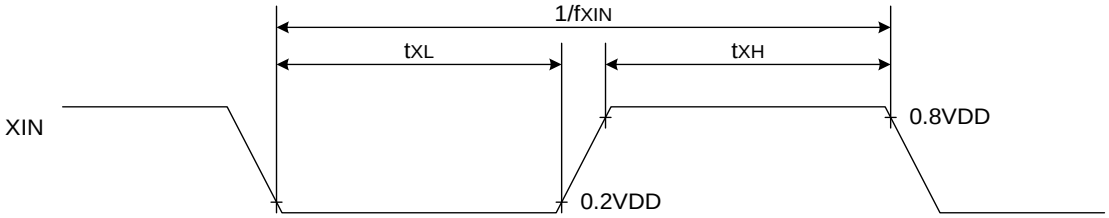


Figure 61. Clock Timing Measurement at XIN

25.18 Sub oscillator characteristics

Table 49. Sub Oscillator Characteristics

(Temperature: -40℃ to +85℃)

Oscillator	Parameter	Conditions	Min	Typ	Max	Units
Operating voltage	VDD	—	2.7	5.0	5.5	V
Operating current	IDD	ISEL_I[1:0]=2'b11 CL=6pf, Schmitt Off	—	0.26	0.82	uA
		ISEL_I[1:0]=2'b10 CL=7pf, Schmitt Off		0.3	0.94	uA
		ISEL_I[1:0]=2'b01 CL=7pf, Schmitt Off		0.34	1.13	uA
		ISEL_I[1:0]=2'b00 CL=12.5pf, Schmitt Off		0.49	1.44	uA
Power down current	I_{STOP}	—	—	—	15	nA
Output frequency	f_{SUB}	—	—	32.768	—	kHz
Start-up time	T_{start}	—	—	2	—	s
Crystal input (low)	V_{IL}	—	—	—	0.2VDD	V
Crystal input (High)	V_{IH}	—	0.8VDD	—	—	V
Crystal out (low)	V_{OL}	—	—	—	0.2VDD	V
Crystal out (high)	V_{OH}	—	0.8VDD	—	—	V
External load cap	R_{FB}		6	7	12.5	pF
Feedback resistance	C_L		5.5	11.2	22.8	MΩ

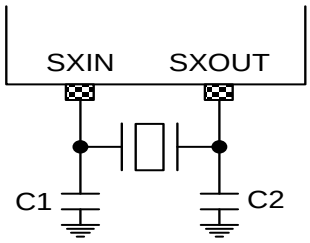


Figure 62. Crystal Oscillator

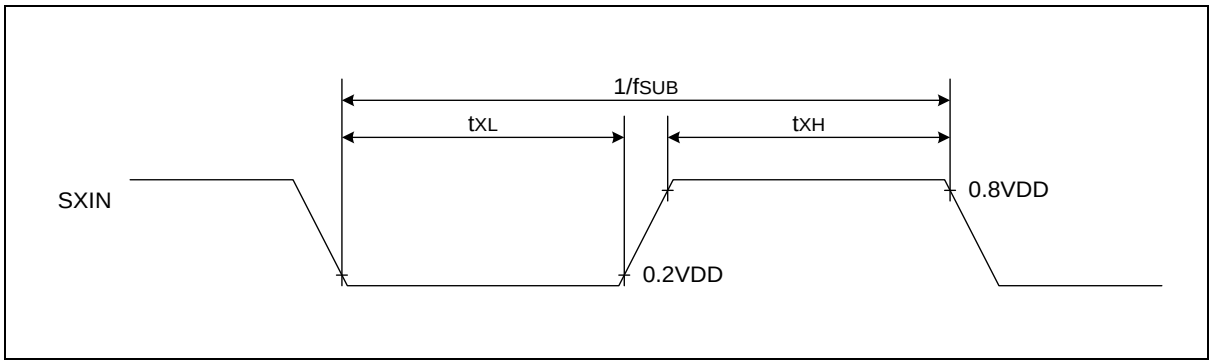


Figure 63. Clock Timing Measurement at SXIN

25.19 Operating voltage range

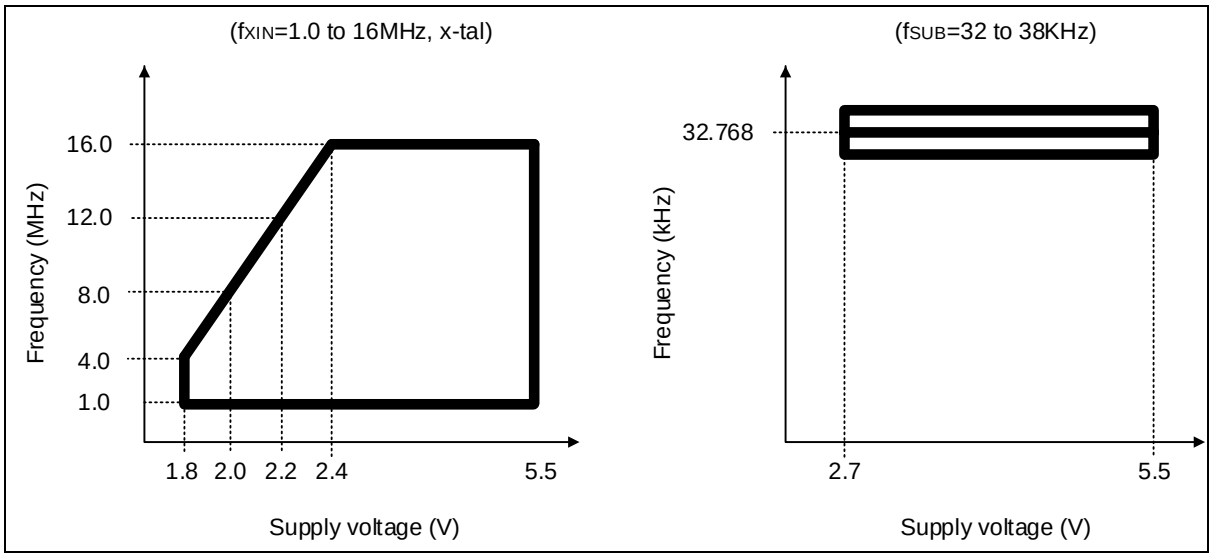


Figure 64. Operating Voltage Range

25.20 PLL electrical characteristics

Table 50. PLL Electrical Characteristics

(Temperature: -40℃ to +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating voltage	VDD		1.8	5	5.5	V
Operating current	I_{DD}	Enable	—	—	1	mA
		Disable	—	5	500	nA
Output frequency	f_{OUT}	—	—	—	144	MHz
Duty	f_{DUTY}		40	—	60	%
Input frequency	$f_{PLLINCLK}$		4	8	16	MHz
Locking time*	t_{LOCK}		190	—	—	us

25.21 Comparator characteristics

The measured value for the parameters and conditions listed below were confirmed by simulaion

Table 51. Comparator Characteristics

(Temperature: -40℃ to +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating voltage	VDD		2.0	5	5.5	V
Comparator offset error	V_{Offset}		—	±5	±10	mV
		Using internal VREF		±20	±70	
Hysteresis	$Vhys_{(None)}$	—	—	0		mV
	$Vhys_{(Low)}$	High speed mode	3	8	13	
		All other power modes	5	8	10	
	$Vhys_{(Mid)}$	High speed mode	7	15	26	
		All other power modes	9	15	19	
	$Vhys_{(High)}$	High speed mode	18	31	49	
		All other power modes	19	31	40	
Propagation delay for 200mv Step with 100mv overdrive	t_{PD}	Ultra-low power mode		2	4.5	us
		Low power mode		0.7	1.5	
		Medium power mode		0.3	0.6	
		High speed mode VDDEXT≥2.7V		50	100	ns
		High speed mode 2V<VDDEXT<2.7V		100	240	
Propagation delay for full Range step with 100mv Overdrive	t_{PD}	Ultra-low power mode		2	7	us
		Low power mode		0.7	2.1	
		Medium power mode		0.3	1.2	
		High speed mode VDDEXT≥2.7V		90	180	ns
		High speed mode 2V<VDDEXT<2.7V		110	300	
Comparator current	$IDD_{(COMP)}$	Ultra-low power mode (COMP1 only)	—	1.2	1.5	uA

Table 51. Comparator Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Comparator current	$IDD_{(COMP)}$	Ultra-low power mode (COMP1 and COMP2)	—	2.4	—	uA
		Low power mode (COMP1 only)	—	3	5	
		Low power mode (COMP1 and COMP2)	—	6	—	
		Medium power mode (COMP1 only)	—	10	15	
		Medium power mode (COMP1 and COMP2)	—	20	—	
		High Speed mode (COMP1 only)	—	75	100	
		High Speed mode (COMP1 and COMP2)	—	150	—	

Table 52. Interanal Voltage Reference Characteristics(For comparator)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating voltage	VDD		2.7	5	5.5	V
Output Voltage	$V_{OUT1.2V}$		1.162	1.223	1.284	
	$V_{OUT0.9V}$		0.871	0.917	0.963	
	$V_{OUT0.6V}$		0.580	0.611	0.642	
	$V_{OUT0.3V}$		0.290	0.305	0.320	

25.22 USB characteristics

Table 53. USB Characteristics

(Temperature: -40℃ to +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating voltage	VDD		3.0	-	5.5	V
	VDD33		2.97	3.3	3.63	V
	VDDIO2		2.97	3.3	3.63	
Pull down resistance on DP/DN	R_{PD}	Enable internal resistor	12	-	17	KΩ
Pull up resistance on DP/DN	R_{PU}	Enable internal resistor	1.1	-	1.9	KΩ
Output driver impedance	Z_{DRV}	Driving high and low	10	-	35	Ω

25.23 Temperature Sensor characteristics

Table 54. Temperature Sensor Characteristics

(Temperature: -40℃ to +85℃)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Operating Voltage	VDD		1.8	-	5.5	V
Temperature Accuracy error	$T_{SENSACC}$			±10		℃

The measured value for the parameters and conditions listed below were confirmed by simulaion

26. Development tools

This chapter introduces wide range of development tools for A31G32x. ABOV offers software tools, debuggers, and programmers to help a user in generating right results to match target applications. ABOV supports entire development ecosystem of the customers.

26.1 Compiler

ABOV semiconductor does not provide any compiler for A31G32x. However, since A31G32x have ARM's high-speed 32-bit Cortex-M0+ Cores for their CPU, you can use all kinds of third party's standard compiler such as Keil C Compiler. These compilers' output debug information can be integrated with our A-Link and A-Link Pro. Please visit our website www.abovsemi.com for more information regarding the A-Link and A-Link Pro.

26.2 Debugger

The A-Link and A-Link Pro support ABOV Semiconductor's A31G32x MCU emulation in SWD Interface. The A-Link and A-Link Pro use two wires interfacing between PC and MCU, which is attached to user's system. The A-Link and A-Link Pro can read or change the value of MCU's internal memory and I/O peripherals. In addition, the A-Link and A-Link Pro control MCU's internal debugging logic. This means A-Link and A-Link Pro control emulation, step run, monitoring and many more functions regarding debugging.

The A-Link and A-Link Pro run underneath MS operating system such as MS-Windows NT/ 2000/ XP/ Vista/ 7/ 8/ 8.1/ 10 (32-bit, 64-bit).

Programming information using the A-Link and A-Link Pro are provided in Figure 68. More detailed information about the A-Link and A-Link Pro, please visit our website www.abovsemi.com and download the debugger S/W and documents.

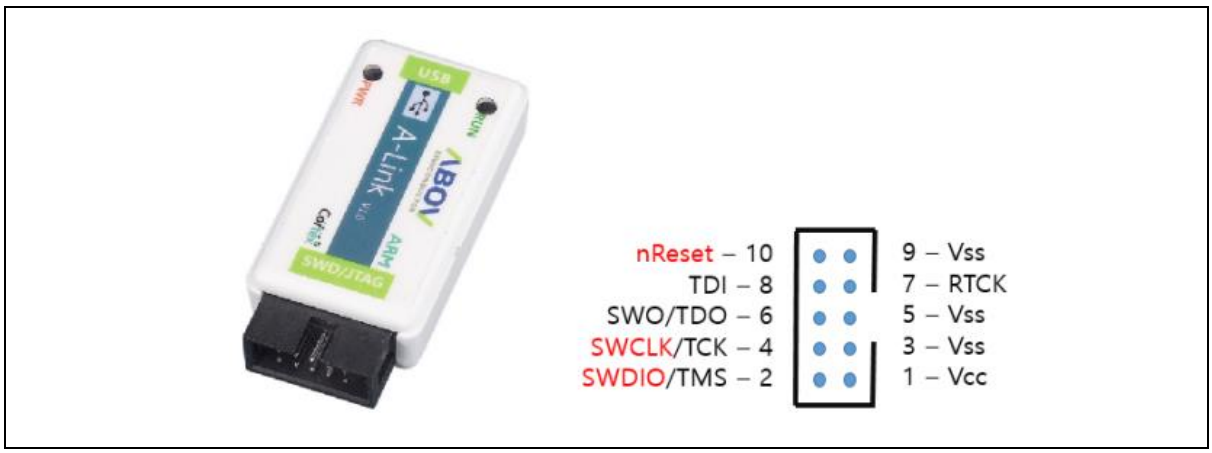


Figure 65. A-Link and Pin Descriptions

26.3 Programmer

E-PGM+

E-PGM+ is a single programmer, and allows a user to program on the device directly.

- Support ABOV devices
- 2~5 times faster than S-PGM+
- Main controller: 32-bit MCU @ 72MHz
- Buffer memory: 1MB

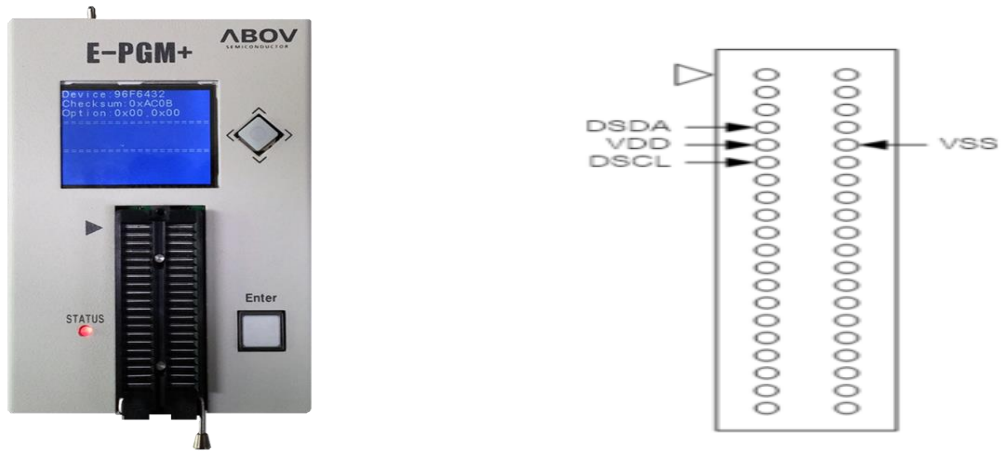


Figure 66. E-PGM+ (Single Writer) and Pin Descriptions

Gang programmer

E-Gang4 and E-Gang6 allows a user to program on multiple devices at a time. They run not only in PC controlled mode but also in standalone mode without PC control. USB interface is available and it is easy to connect to the handler.

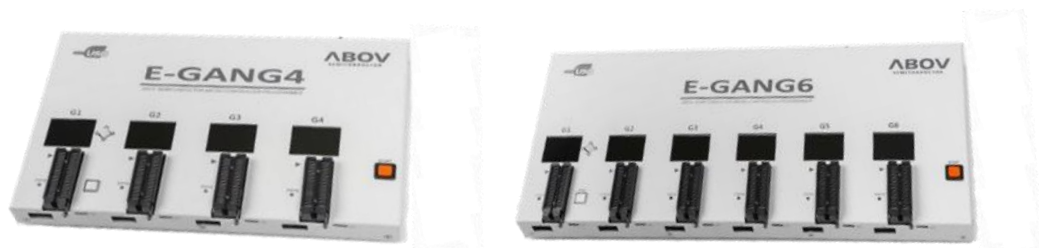


Figure 67. E-Gang4 and E-Gang6 (for Mass Production)

27. Circuit Design Guide

Refer to the Recommended Circuit and Layout Design as shown below.

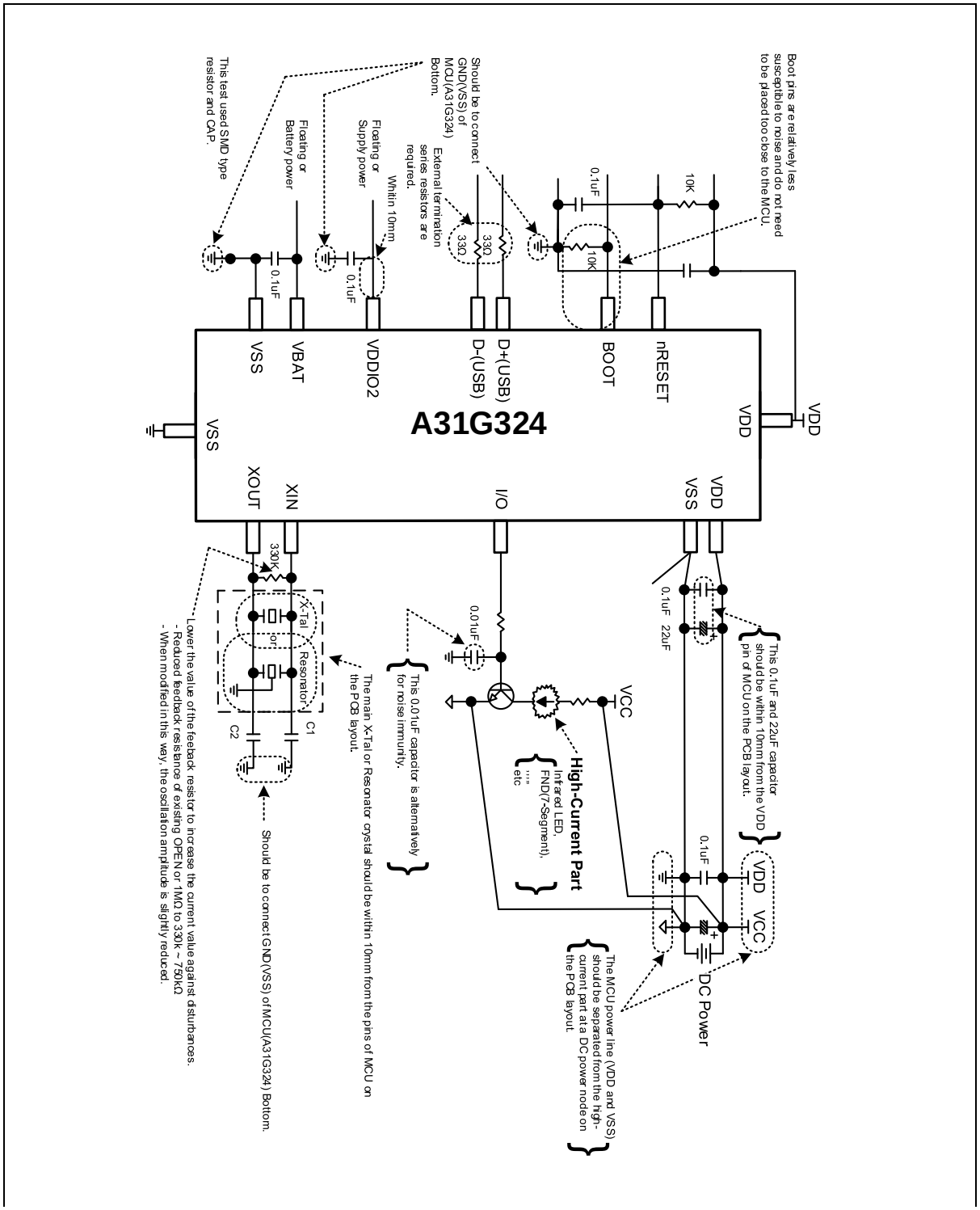


Figure 68. PCB Design Guide for On-Board Programming

28. Package information

This chapter provides A31G32x series package information.

28.1 64 LQFP package information

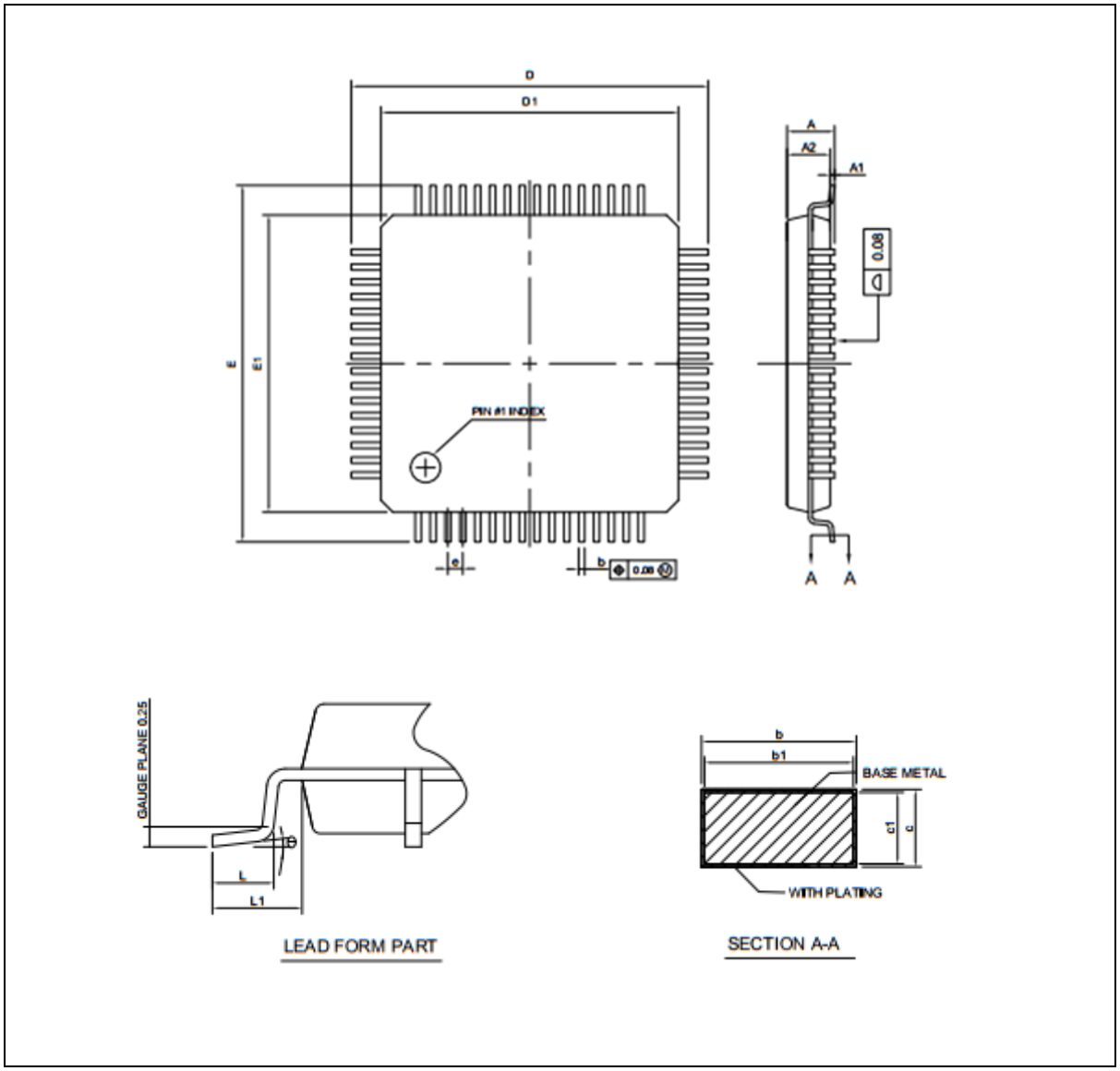


Figure 69. 64 LQFP Package Outline

Table 55. 64 LQFP Package Mechanical Data

Symbol	Dimension (mm)		
	Min.	**Nom.**	**Max.**
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	—	0.20
c1	0.09	—	0.16
D	11.80	12.00	12.20
D1	9.80	10.00	10.20
E	11.80	12.00	12.20
E1	9.80	10.00	10.20
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
Θ	0°	3.5°	7°

NOTES:

1. All dimension refer to JEDEC standard MS-026-BCD.
2. Dimensions ‘D1’ and ‘E1’ do not include MOLD PROTRUSION. Allowable PROTRUSION is 0.25 mm per side. ‘D1’ and ‘E1’ are maximum plastic body size dimensions including MOLD MISMATCH.
3. Dimension ‘b’ does not include DAMBAR PROTRUSION. Allowable DAMBAR PROTRUSION shall not cause the LEAD width to exceed the maximum ‘b’ dimension by more than 0.08 mm.
4. ‘A1’ is defined as the distance from the seating plane to the lowest point on the package body.

28.2 48 LQFP package information

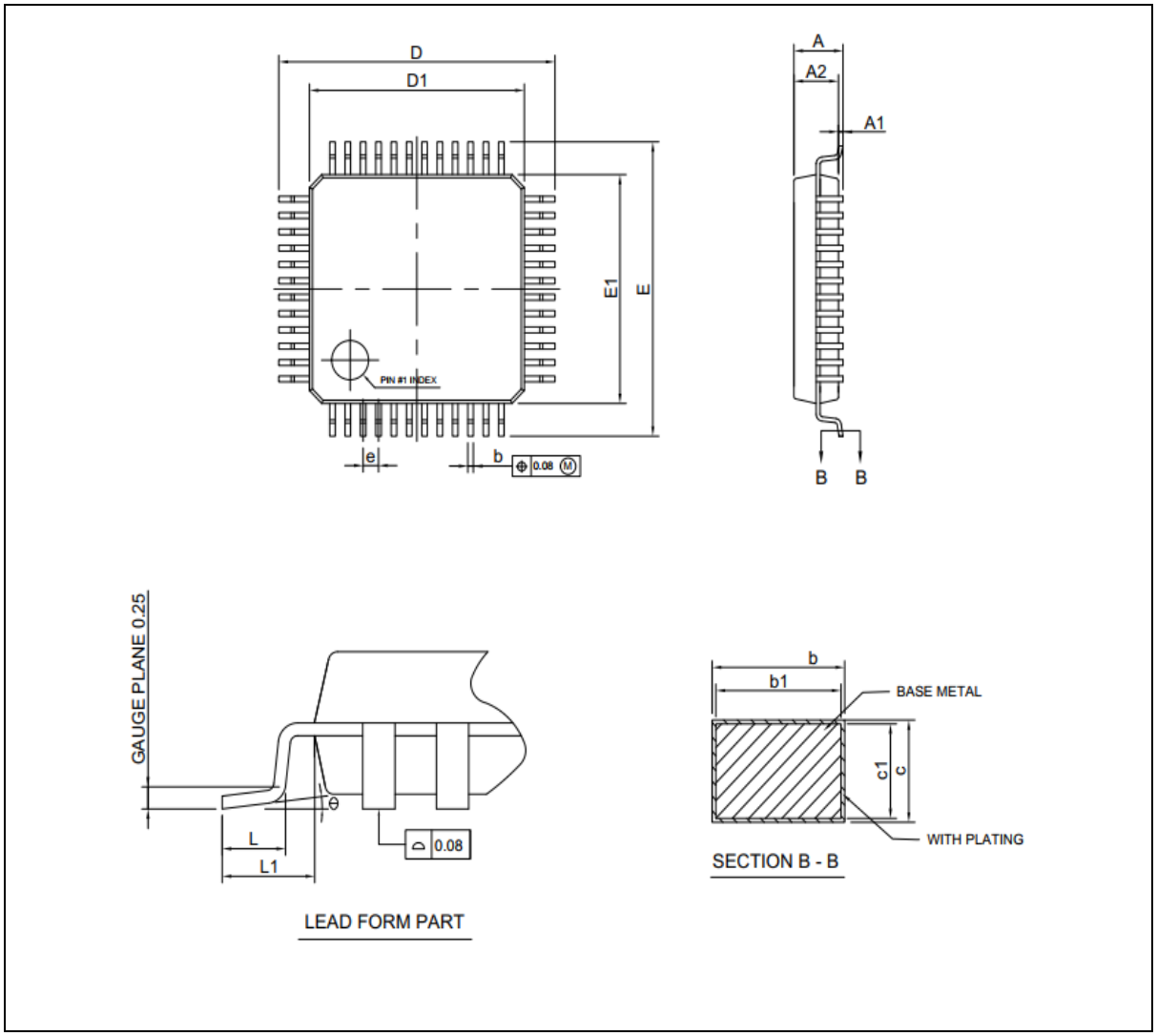


Figure 70. 48 LQFP Package Outline

Table 56. 48 LQFP Package Mechanical Data

Symbol	Dimension (mm)		
	Min.	Nom.	Max.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	—	0.20
c1	0.09	—	0.16
D	8.80	9.00	9.20
D1	6.80	7.00	7.20
E	8.80	9.00	9.20
E1	6.80	7.00	7.20
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
Θ	0°	3.5°	7°

NOTES:

1. All dimension refer to JEDEC standard MS-026-BBC.
2. Dimensions ‘D1’ and ‘E1’ do not include MOLD PROTRUSION. Allowable PROTRUSION is 0.25 mm per side. ‘D1’ and ‘E1’ are maximum plastic body size dimensions including MOLD MISMATCH.
3. Dimension ‘b’ does not include DAMBAR PROTRUSION. Allowable DAMBAR PROTRUSION shall not cause the LEAD width to exceed the maximum ‘b’ dimension by more than 0.08 mm.
4. ‘A1’ is defined as the distance from the seating plane to the lowest point on the package body.

28.3 48 QFN package information

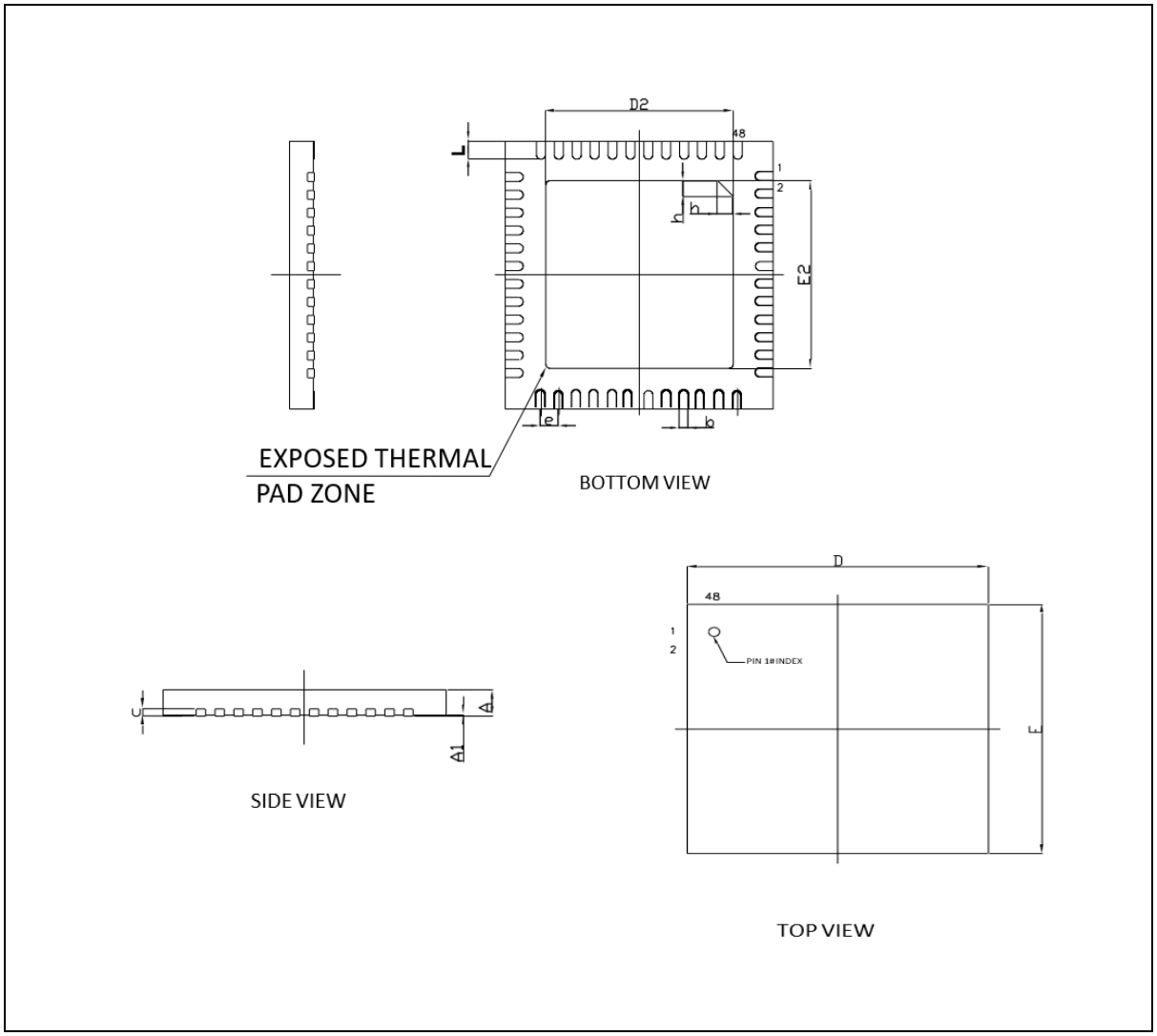


Figure 71. 48 QFN Package Outline

Table 57. 48 QFN Package Mechanical Data

Symbol	Dimension (mm)		
	Min.	**Nom.**	**Max.**
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
b	0.10	0.15	0.20
c	0.10	0.15	0.20
D	4.90	5.00	5.10
D2	3.60	3.70	3.80
E	4.90	5.00	5.10
E2	3.60	3.70	3.80
e	0.35 BSC		
L	0.30	0.35	0.40
h	0.30	0.35	0.40

NOTES:

1. Dimension ‘b’ applies to metallized terminal and is measured between 0.15mm and 0.3mm from the TERMINAL TIP. If the TERMINAL has the optinal radius on the other end of the TERMINAL, the Dimension ‘b’ should not be measured in that radius area.

29. Ordering information

Table 58. A31G32x Device Ordering Information

Device name	Flash	SRAM	SPI	USART	I2C	Timer	PWM	ADC	I/O ports	Package
A31G324RLN	128KB	16KB	2	4	2	6(16-bit)/2(32-bit)	8	16	51	LQFP 64
A31G324CLN*	128KB	16KB	2	3	2	6(16-bit)/2(32-bit)	8	10	37	LQFP 48
A31G324CUN*	128KB	16KB	2	3	2	6(16-bit)/2(32-bit)	8	10	37	QFN 48
A31G323RLN*	64KB	16KB	2	4	2	6(16-bit)/2(32-bit)	8	16	51	LQFP 64
A31G323CLN*	64KB	16KB	2	3	2	6(16-bit)/2(32-bit)	8	10	37	LQFP 48
A31G323CUN*	64KB	16KB	2	3	2	6(16-bit)/2(32-bit)	8	10	37	QFN 48

* For available options or further information on the devices with "*" marks, please contact the ABOV Sales Office

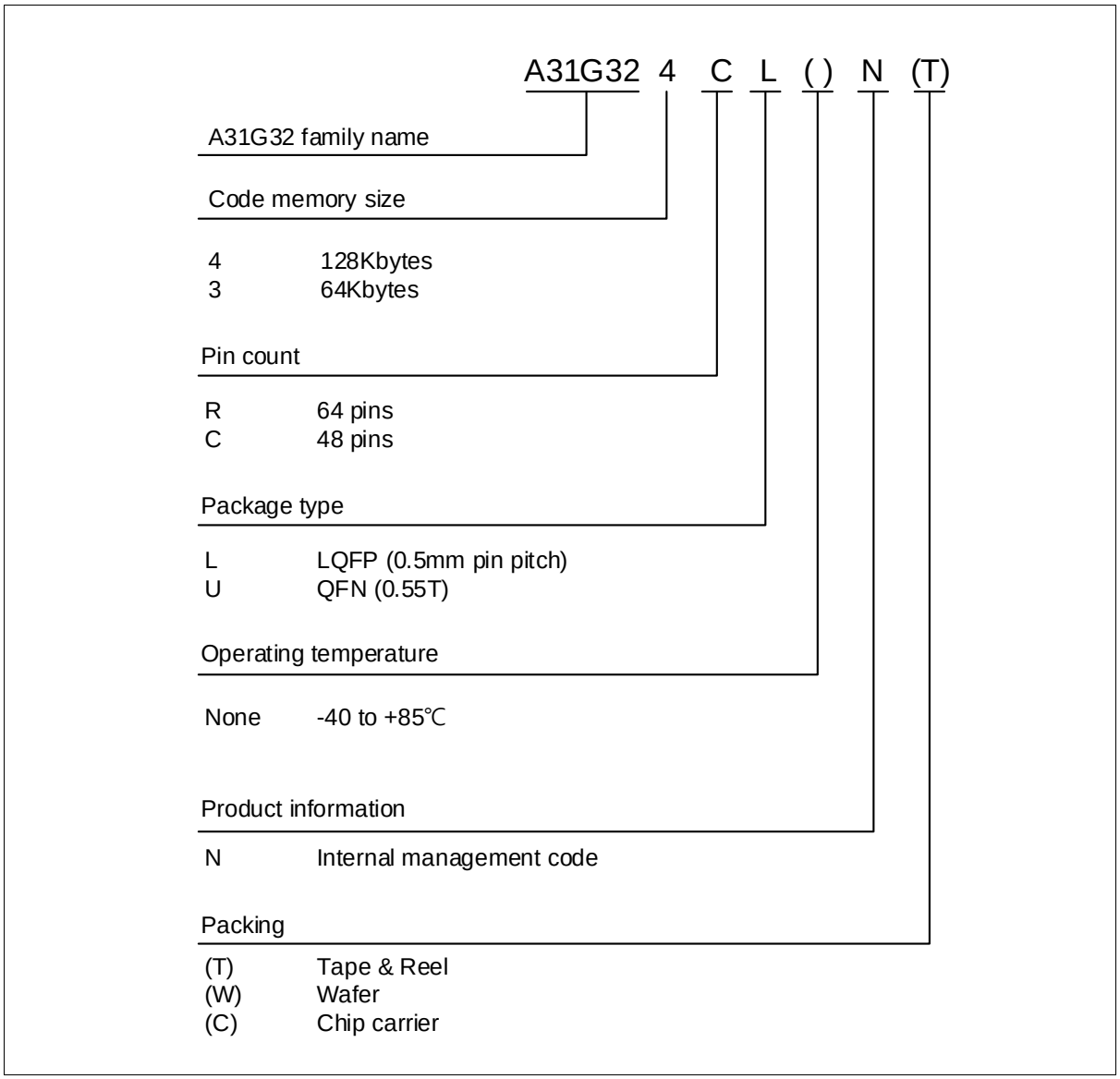


Figure 72. A31G32x Device Numbering Nomenclature

Revision history

Date	Revision	Description
Dec.4, 2020	1.00	First creation
Feb.23, 2021	1.01	Updated Recommended operating conditions and Main oscillator characteristics
Apr.18, 2022	1.02	Removed Industrial Grade Updated Product selection table & Ordering information Added the Figure 71. 48 QFN Package Outline Added the Figure 4. QFN 48 Pinouts
Aug.19, 2022	1.03	Updated Figure 4
Oct. 5, 2022	1.04	Revised the font of this document
Dec. 2, 2024	1.05	Updated the disclaimer.

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