A31G226, A31G224
Datasheet

32-bit Cortex-M0+ based General Purpose Microcontroller
Flash 128/256KB, SRAM 20KB, Data Flash 32KB, ADC, Comparator, LCD

Datasheet Version 1.14

Features

Core

- High performance Cortex-M0+ core
- Up to 48MHz clock speed

Memories

- 256/128KB code flash memory
  - Memory Bank Swap
  - Read protection for security
- 32KB data flash memory
  - Read protection for security
- 20KB SRAM

Clock, reset and power management

- Two main operating clocks: HCLK, PCLK
- Two system reset: cold reset, warm reset
- Low Voltage Detection (LVD)
  - Low voltage Interrupt, Low voltage Reset
- Power management for power consumption
  - Run, SLEEP, DEEP-SLEEP modes
- Monitoring System
  - MCLK, HSE, LSE clock monitoring

Interrupt management

- Nested Vector Interrupt Controller (NVIC) with 37 interrupt sources

Port Control and GPIO

- Sink type high current output port
- Strength input/output

Timers

- Watchdog Timer and Watch Timer
- Watch Timer
- 16-bit general purpose timers
- 32-bit 2-chnannel general purpose timers

16-bit Pulse-Width Modulation

- 3-phase complementary PWM generators

Direct Memory Access Controller

- 8 Channels Tx, Rx, Peri-to-Peri directions

Communication interfaces

- 2 UARTs, 4 USARTs, 3 I2Cs, 2 SPIs

1.0Msps 12-bit A/D Convertor

- Up to 18 channels inputs

12-bit D/A Converter

- 1 channel D/A outputs

Comparator

- 2 channels comparators

LCD Driver

- LCD Channel configuration (COM x SEG)
  - 80-pin: 8 x 37 or 3 x 42
  - 64-pin: 8 x 29 or 3 x 34
  - 48-pin: 8 x 21 or 3 x 26
- 3.3V external bias source voltage

CRC generator

- 7/8/16/32-bit CRC generator
- CRC-7, CRC-8, CRC-16, CRC-32

Temperature Sensor

- Count type with internal temp sensing clock

Development support

- SWD debug interface

Four types of package options

- LQFP80-1414 (0.65mm pitch)
- LQFP80-1212 (0.50mm pitch)
- LQFP64-1212 (0.65mm pitch)
- LQFP64-1010 (0.50mm pitch)
- LQFP48-0707 (0.50mm pitch)

Operating voltage

- 1.8V to 5.5V

Operating temperature

- Commercial grade (-40℃ to +105℃)

Product selection table

Table 1. Device Summary

Device name	Code Flash [KB]	Data Flash [KB]	SRAM [KB]	I2C [ch]	UART [ch]	USART [ch]	SPI [ch]	TIMER [ch]	PWM [ch]	12-bit ADC [ch]	LCD Driver [COM x SEG]	I/O ports [ch]	Op. Temp. [℃]	Package Type
A31G226ML2N	256	32	20	3	2	4	2	7(16bit)/ 2(32bit)	3	18	8 x 37 or 3 x 42	75	-40 ~105	80LQFP12
A31G226MM2N*	256	32	20	3	2	4	2	7(16bit)/ 2(32bit)	3	18	8 x 37 or 3 x 42	75	-40 ~105	80LQFP14
A31G226RM2N*	256	32	20	3	2	3	2	7(16bit)/ 2(32bit)	3	18	8 x 29 or 3 x 34	59	-40 ~105	64LQFP12
A31G226RL2N	256	32	20	3	2	3	2	7(16bit)/ 2(32bit)	3	18	8 x 29 or 3 x 34	59	-40 ~105	64LQFP10
A31G226CL2N*	256	32	20	2	2	2	2	7(16bit)/ 2(32bit)	3	14	8 x 21 or 3 x 26	43	-40 ~105	48LQFP7
A31G224MM2N*	128	32	20	3	2	4	2	7(16bit)/ 2(32bit)	3	18	8 x 37 or 3 x 42	75	-40 ~105	80LQFP14
A31G224ML2N*	128	32	20	3	2	4	2	7(16bit)/ 2(32bit)	3	18	8 x 37 or 3 x 42	75	-40 ~105	80LQFP12
A31G224RM2N*	128	32	20	3	2	3	2	7(16bit)/ 2(32bit)	3	18	8 x 29 or 3 x 34	59	-40 ~105	64LQFP12
A31G224RL2N*	128	32	20	3	2	3	2	7(16bit)/ 2(32bit)	3	18	8 x 29 or 3 x 34	59	-40 ~105	64LQFP10
A31G224CL2N*	128	32	20	2	2	2	2	7(16bit)/ 2(32bit)	3	14	8 x 21 or 3 x 26	43	-40 ~105	48LQFP7
A31G226MLN*	256	32	20	3	2	4	2	7(16bit)/ 2(32bit)	3	18	8 x 37 or 3 x 42	75	-40 ~85	80LQFP12
A31G226MMN*	256	32	20	3	2	4	2	7(16bit)/ 2(32bit)	3	18	8 x 37 or 3 x 42	75	-40 ~85	80LQFP14
A31G226RMN*	256	32	20	3	2	3	2	7(16bit)/ 2(32bit)	3	18	8 x 29 or 3 x 34	59	-40 ~85	64LQFP12
A31G226RLN*	256	32	20	3	2	3	2	7(16bit)/ 2(32bit)	3	18	8 x 29 or 3 x 34	59	-40 ~85	64LQFP10
A31G226CLN*	256	32	20	2	2	2	2	7(16bit)/ 2(32bit)	3	14	8 x 21 or 3 x 26	43	-40 ~85	48LQFP7
A31G224MMN*	128	32	20	3	2	4	2	7(16bit)/ 2(32bit)	3	18	8 x 37 or 3 x 42	75	-40 ~85	80LQFP14
A31G224MLN*	128	32	20	3	2	4	2	7(16bit)/ 2(32bit)	3	18	8 x 37 or 3 x 42	75	-40 ~85	80LQFP12
A31G224RMN*	128	32	20	3	2	3	2	7(16bit)/ 2(32bit)	3	18	8 x 29 or 3 x 34	59	-40 ~85	64LQFP12
A31G224RLN*	128	32	20	3	2	3	2	7(16bit)/ 2(32bit)	3	18	8 x 29 or 3 x 34	59	-40 ~85	64LQFP10
A31G224CLN*	128	32	20	2	2	2	2	7(16bit)/ 2(32bit)	3	14	8 x 21 or 3 x 26	43	-40 ~85	48LQFP7

* For available options or further information on the devices with "*" marks, please contact the ABOV sales offices.

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1 Description

A31G22x is a 32-bit general purpose microcontroller with up to 256 Kbytes of flash memory. It is a powerful microcontroller which provides effective solutions to various electrical appliances which require both low power consumption and high performance.

1.1 Features

In this section, features of A31G22x and peripheral counts are introduced.

Table 2. A31G22x Device Features and Peripheral Counts

Peripherals		Description
Core	CPU	• High Performance Low-Power Cortex-M0+ Core • 32-bit ARM Cortex-M0+ CPU • Uses general-purpose registers specified by the 32-bit Thumb®-2 instruction set • Data ordering format : Little-Endian • Von-Neumann Architecture • AHB-Lite / APB • 24-bit SYSTICK timer • SWD Debugger
	Interrupt	• NVIC (Nested-Vectored Interrupt Controller) • Up to 32 peripheral interrupts supported • Can be assigned with 4 different priority levels
Memory	Code flash	• A31G226: 256 Kbytes code flash memory • A31G224: 128 Kbytes code flash memory • Flash access wait — 0 clock wait: up to 20MHz — 1 clock wait: up to 40MHz — 2 clock wait: up to 48MHz • Supports 512B, 1KB, and 4KB erase • Supports bulk erase • Supports Read protection and Write Protection • Memory Bank Swap • Supports self-programming • Endurance : 10,000 Cycles at room temperatures • Retention for 10 years

Table 2. A31G22x Device Features and Peripheral Counts (continued)

Peripherals		Description
Memory	Data flash	• 32 KB data flash memory • Supports 512 Bytes, 1 KB, and 4 KB sector erase • Supports bulk erase • Supports read protection • Supports write protection • Supports byte-unit (8-bit) programming • Supports word-unit (32-bit) programming • Endurance : 100,000 Cycles at room temperatures • Retention for 10 years
	SRAM	• 20 Kbytes SRAM (0 wait) • Usable as a program work area • Supports code execution in SRAM
System Control Unit (SCU)	Operating frequency	• Up to 48 MHz
	Clock	• High speed internal oscillator (HSI) — 32 MHz (± 1.0% @ -20 ℃ to +85 ℃) — 32 MHz (± 1.5% @ -40 ℃ to +105 ℃) • Low speed internal oscillator (LSI) — 500 kHz (± 20% @- 40 ℃ to +105 ℃) • External main oscillator (HSE): 1 MHz to 16 MHz • External sub-oscillator (LSE): 32.768 kHz • Phase-locked loop (PLL): up to 48 MHz
	Clock monitoring	• System Fail-Safe function by Clock Monitoring — External main oscillator(HSE) — External sub oscillator(LSE) — Main system clock (MCLK)
	Operating mode	• RUN mode • SLEEP mode • STOP mode
	Reset	• nRESET pin reset • Core reset • Software reset • POR (Power On Reset) • LVR (Low Voltage Reset) • WTR (Watch Timer Reset) • WDTR (Watch Dog Timer Reset) • Reset due to clock oscillating error

Table 2. A31G22x Device Features and Peripheral Counts (continued)

Peripherals		Description
System Control Unit (SCU)	Wake-up	• Systick Timer (In SLEEP mode) • general-purpose input/output (GPIO) • Watch Dog Timer (WDT) • Watch Timer (WT) • Low-Voltage Indicator (LVI)
General Purpose I/O (GPIO)		• 75 Ports (PA[11:0], PB[15:0], PC[12:0], PD[5:0], PE[15:0], PF[11:0]): 80-Pin • 59 Ports (PA[11:0], PB[11:0], PC[6:0], PC[12:11], PD[5:0], PE[11:0], PF[7:0]) : 64-pin • 43 Ports (PA[8:0], PB[7:0], PC[4:0], PD[5:0], PE[7:0], PF[7:0]) : 48-Pin • 10-ch sink type high current output ports for driving high currents like LEDs • Strength ports for high speed SPI communication • The use of each pin can be set by setting the mux • Each pin can be configured as an external interrupt source, either the high/low level interrupt or the rising-/falling-edge interrupt • Pull-up/pull-down/debouncing can be set for each pin • Each pin bit can be individually set/reset • Supports wake-up events triggered by external asynchronous inputs
Direct Memory Access Controller (DMA)		• 8-ch direct memory access (DMA) support peripherals • UART0, UART1, CRC, SPI20, SPI21, ADC, DAC, USART10, USART11, USART12, USART13 • DMAC directions — Memory to Peripheral (Tx) — Peripheral to Memory (Rx) — Peripheral to- Peripheral (P2P)
Watch Timer (WT)		• 14-bit divider with extended 12-bit counter 1-ch • Wake up and periodic interrupts are supported
Watchdog Timer (WDT)		• 24-bit down counter timer: 1-ch • Reset, Wake up and periodic interrupts are supported
TIMER	Timer1x	• 16bit: 7-ch — Periodic timer mode, One-shot timer mode, PWM pulse mode, Capture mode • 12-bit prescaler • Synchronous start and clear function with TIMER30
	Timer2x	• 32-bit : 2-ch — Periodic timer mode, One-shot timer mode, PWM pulse mode, Capture mode • 12-bit prescaler

Table 2. A31G22x Device Features and Peripheral Counts (continued)

Peripherals		Description
PWM	Timer30	• 16bit: 3-phase complementary PWM generators phase complementary PWM Outputs — Periodic timer mode, Back-to-Back mode, Capture mode — 12-bit prescaler — Synchronous start and clear function with TIMERn (n=10 to 16)
Comm. function	UART	• Up to 2-ch
	USART	• Up to 4-ch — 80-pin : 4-ch — 64-pin : 3-ch — 48-pin : 3-ch
	SPI	• 2-ch • USART10, USART11 Port Re-Mapping • Strength control for high speed communication
	I2C	• Up to 3-ch — 80-pin : 3-ch — 64-pin : 3-ch — 48-pin : 2-ch
ADC		• 12-bit ADC : 1 Msps — 80-pin : 18-ch — 64-pin : 18-ch — 48-pni : 14-ch • ADC Trigger sources — TIMER1n (n=10 to 16) — TIMER30 — ADC Clock
DAC		• 12-bit DAC 1-ch — PA6 : output pin
CRC calculator		• CRC-32 / CRC-16 / CRC-8 / CRC-7 • DMA transmission
Comparator		• 2-unit comparators • 1-ch reference input of each comparator — External Input channel — Internal Input • 1-ch output of each comparator
Temperature Sensor		• 20-bit reference counter and 16-bit sensing counter • Internal oscillation for temperature sensing (LSITS)

Table 2. A31G22x Device Features and Peripheral Counts (continued)

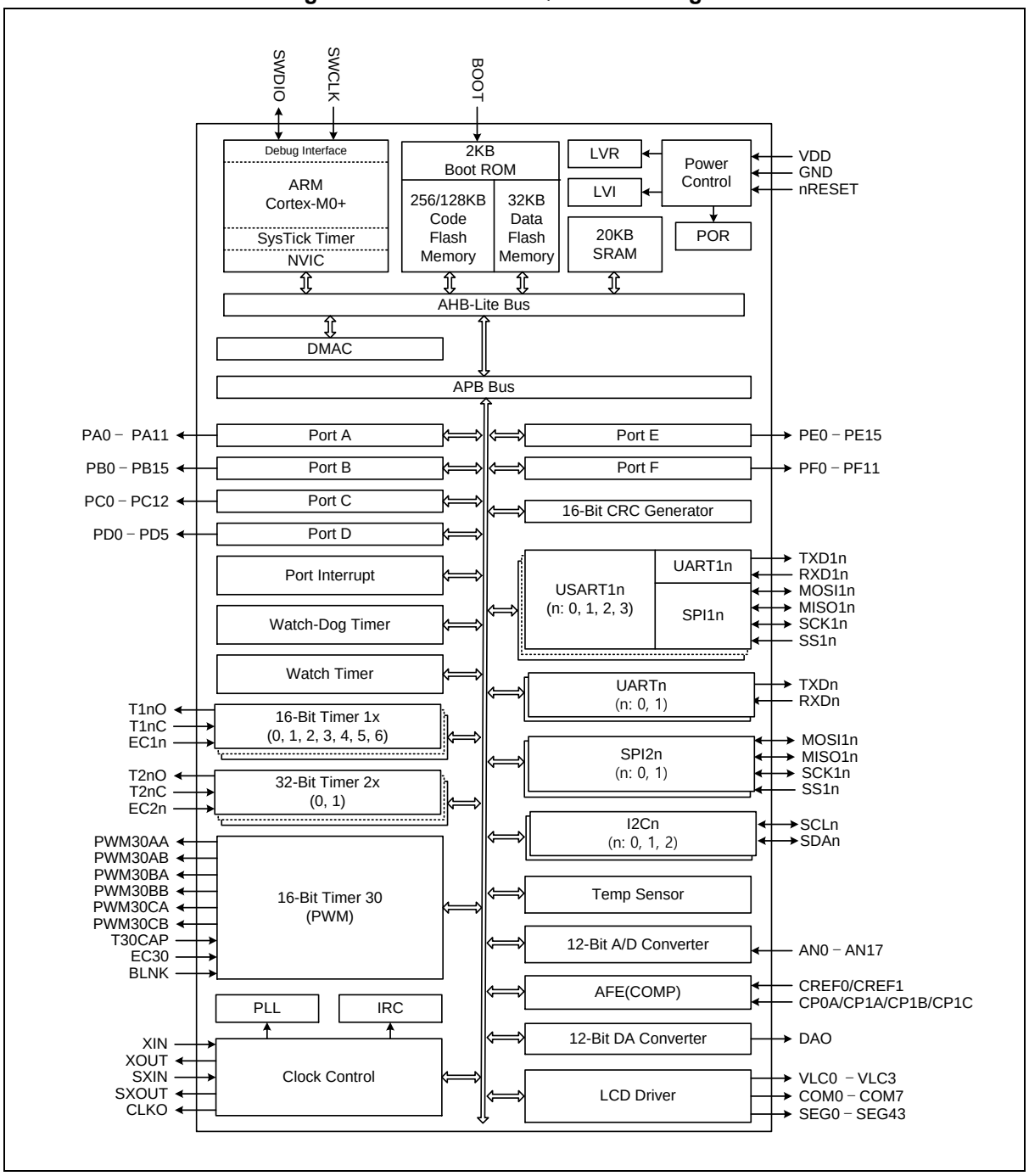
Peripherals	Description
LCD driver	• 80-pin — 8-COM x 37-SEG — 3-COM x 42-SEG • 64-pin — 8-COM x 29-SEG — 3-COM x 34-SEG • 48-pin — 8-COM x 21-SEG — 3-COM x 26-SEG • 3.3V external bias source voltage
Operating Voltage	• 1.8 V to 5.5 V
Operating temperature	• Commercial grade (-40 ℃ to +85 ℃) • Industrial grade (-40 ℃ to +105 ℃)
Package	• Three types of package options — 48-pin LQFP (0.50mm pitch) — 64-pin LQFP (0.50mm, 0.65mm pitch) — 80-pin LQFP (0.50mm, 0.65mm pitch)

1.2 Block diagram

In this section, A31G22x device with peripherals is described in a block diagram.

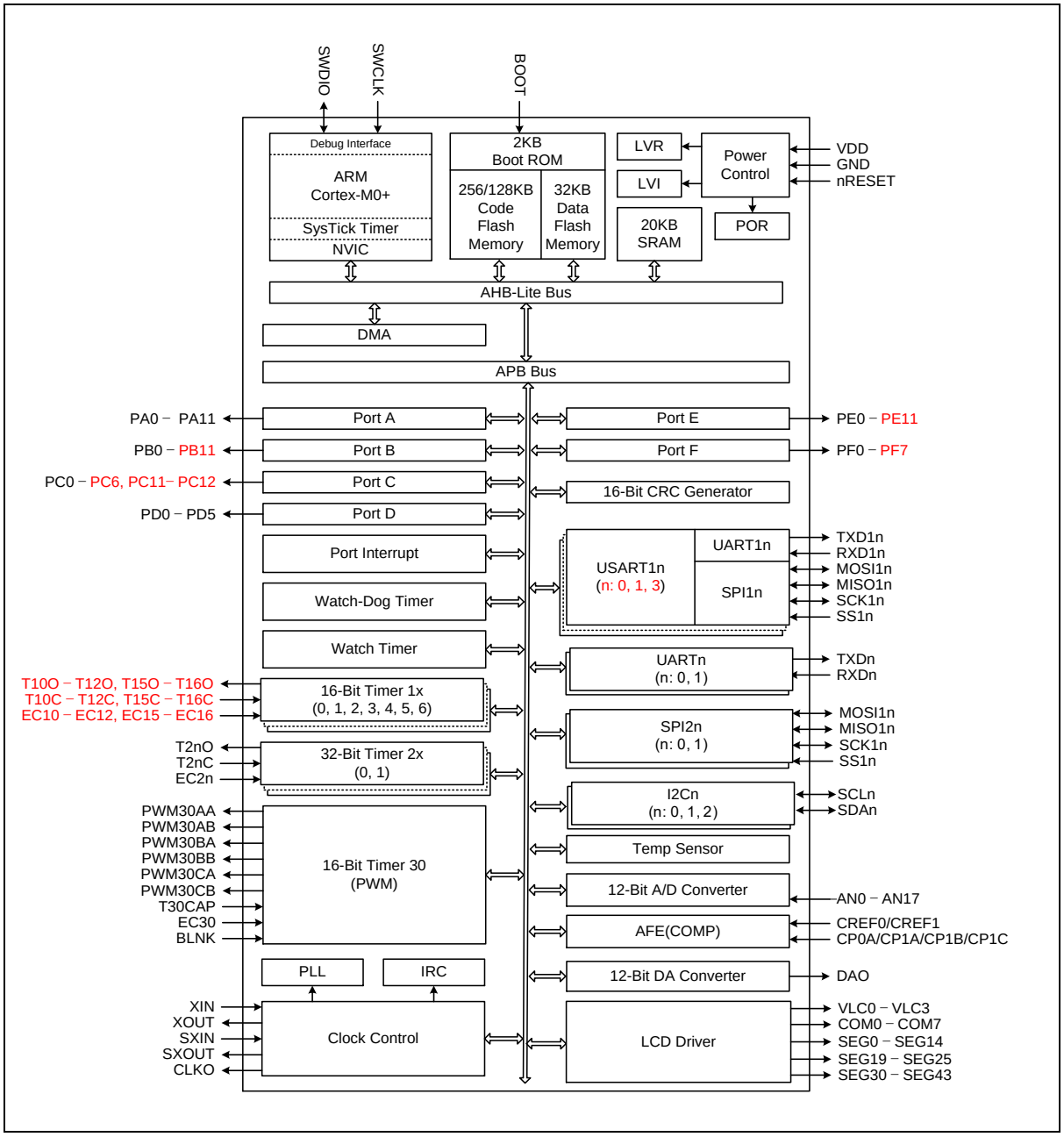
1.2.1 A31G226MM2N/ A31G226ML2N/ A31G224MM2N/ A31G224ML2N/ A31G226MMN/ A31G226MLN/ A31G224MMN/ A31G224MLN (80-LQFP)

Figure 1. A31G22x 80-LQFP Block Diagram



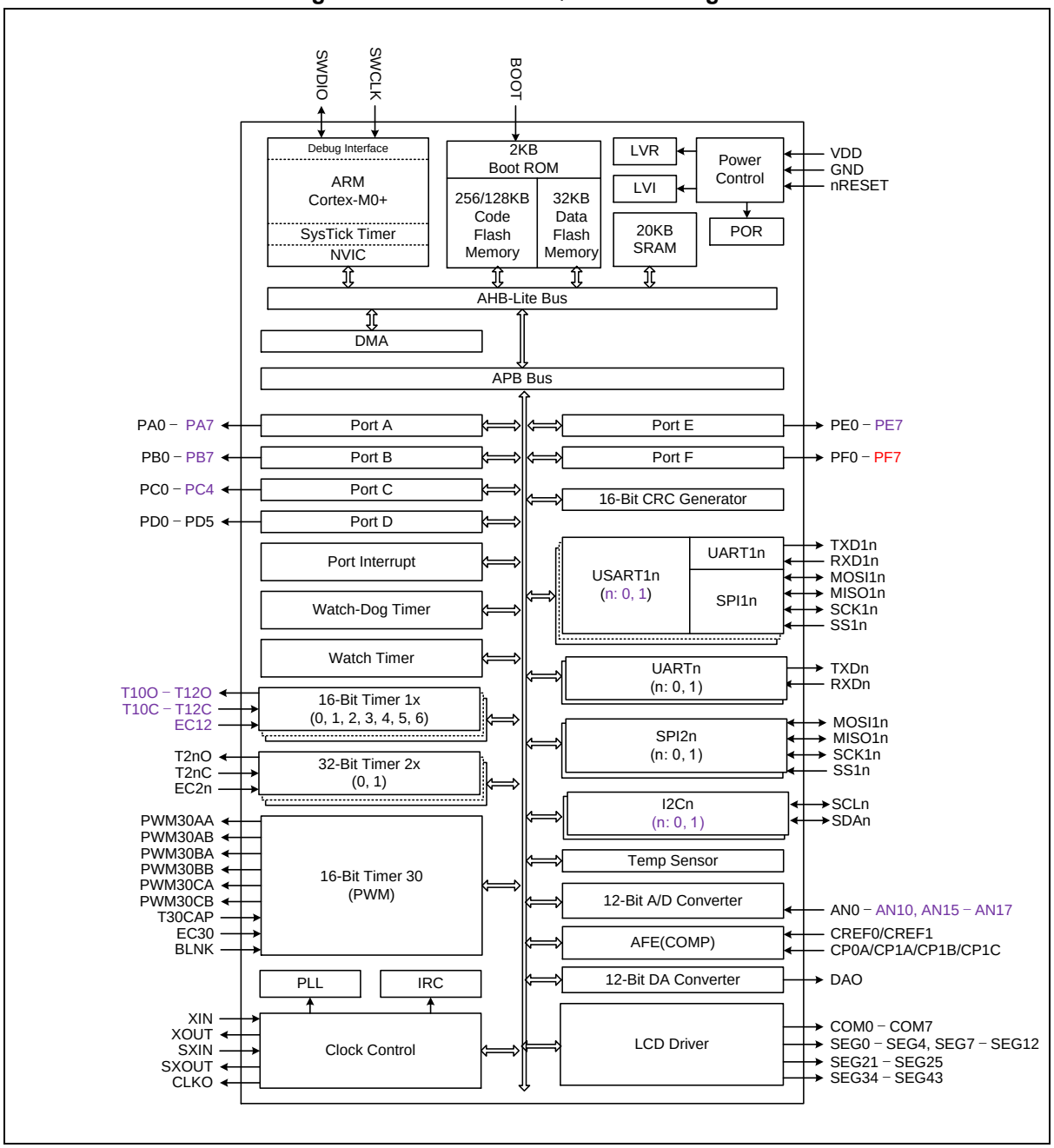
1.2.2 A31G226RM2N/ A31G226RL2N/ A31G224RM2N/ A31G224RL2N/ A31G226RMN/ A31G226RLN/ A31G224RMN/ A31G224RLN (64-LQFP)

Figure 2. A31G22x 64-LQFP Block Diagram



1.2.3 A31G226CL2N/ A31G224CL2N/ A31G226CLN/ A31G224CLN (48-LQFP)

Figure 3. A31G22x 48-LQFP Block Diagram



2 Pinouts and pin descriptions

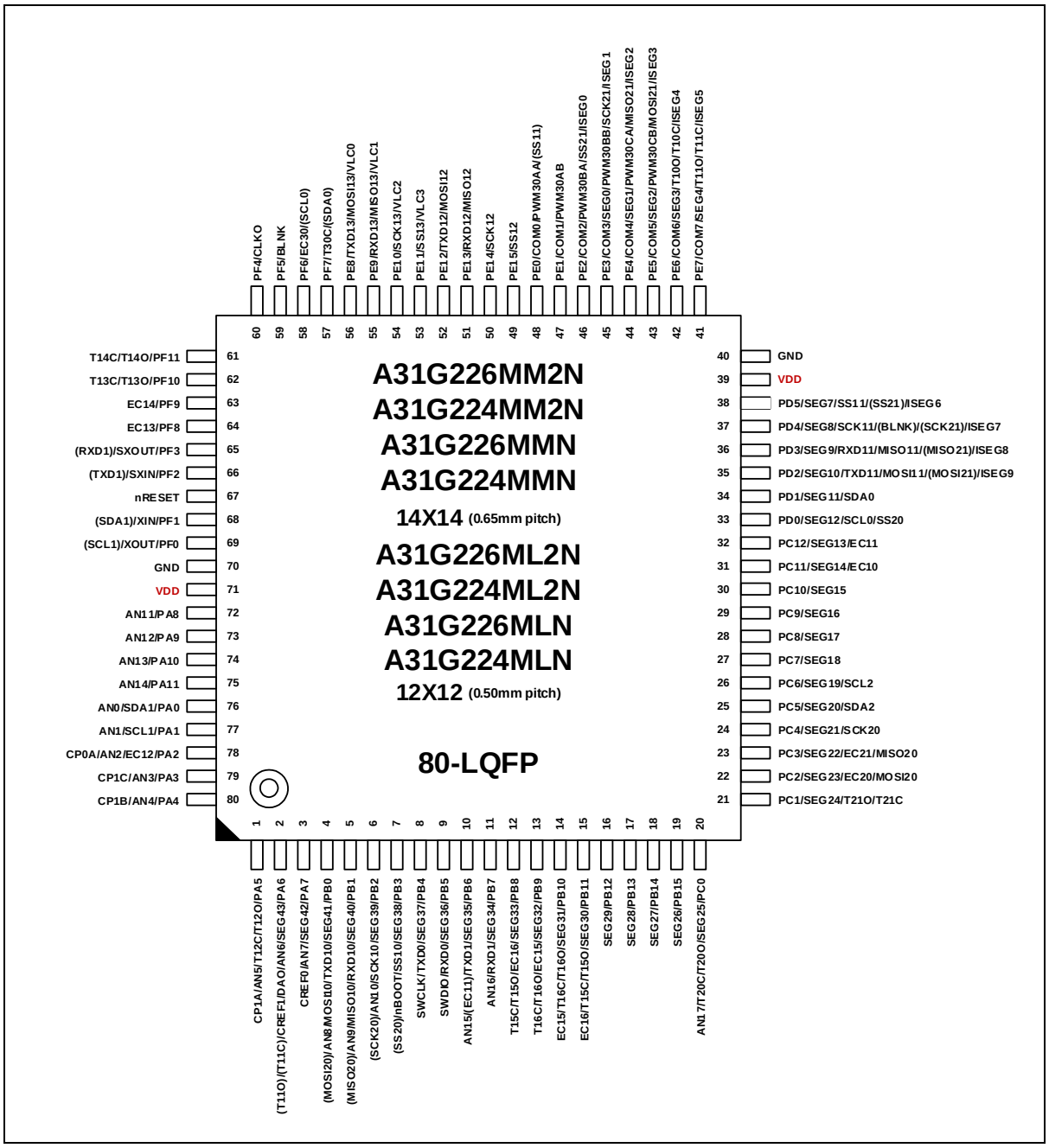
In this chapter, A31G22x devices' pinouts and pin descriptions are introduced.

2.1 Pinouts

2.1.1 A31G226MM2N/ A31G226ML2N/ A31G224MM2N/ A31G224ML2N/ A31G226MMN/ A31G226MLN/ A31G224MMN/ A31G224MLN (LQFP 80)

Pinouts of A31G22x 80-LQFP package are showed in Figure 4.

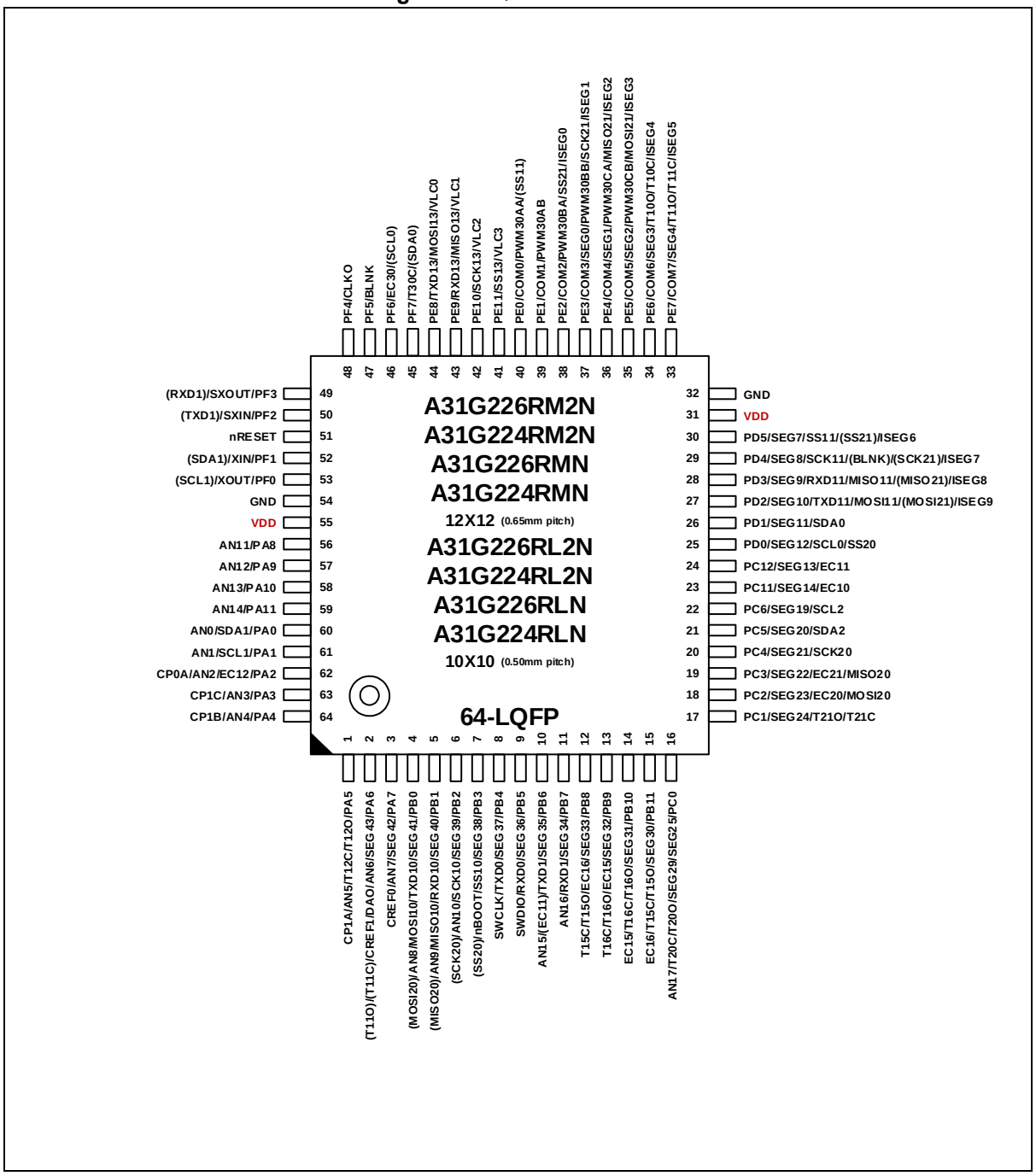
Figure 4. LQFP 80 Pinouts



2.1.2 A31G226RM2N/ A31G226RL2N/ A31G224RM2N/ A31G224RL2N/ A31G226RMN/ A31G226RLN/ A31G224RMN/ A31G224RLN (64-LQFP)

Pinouts of A31G22x 64-LQFP package are showed in Figure 5.

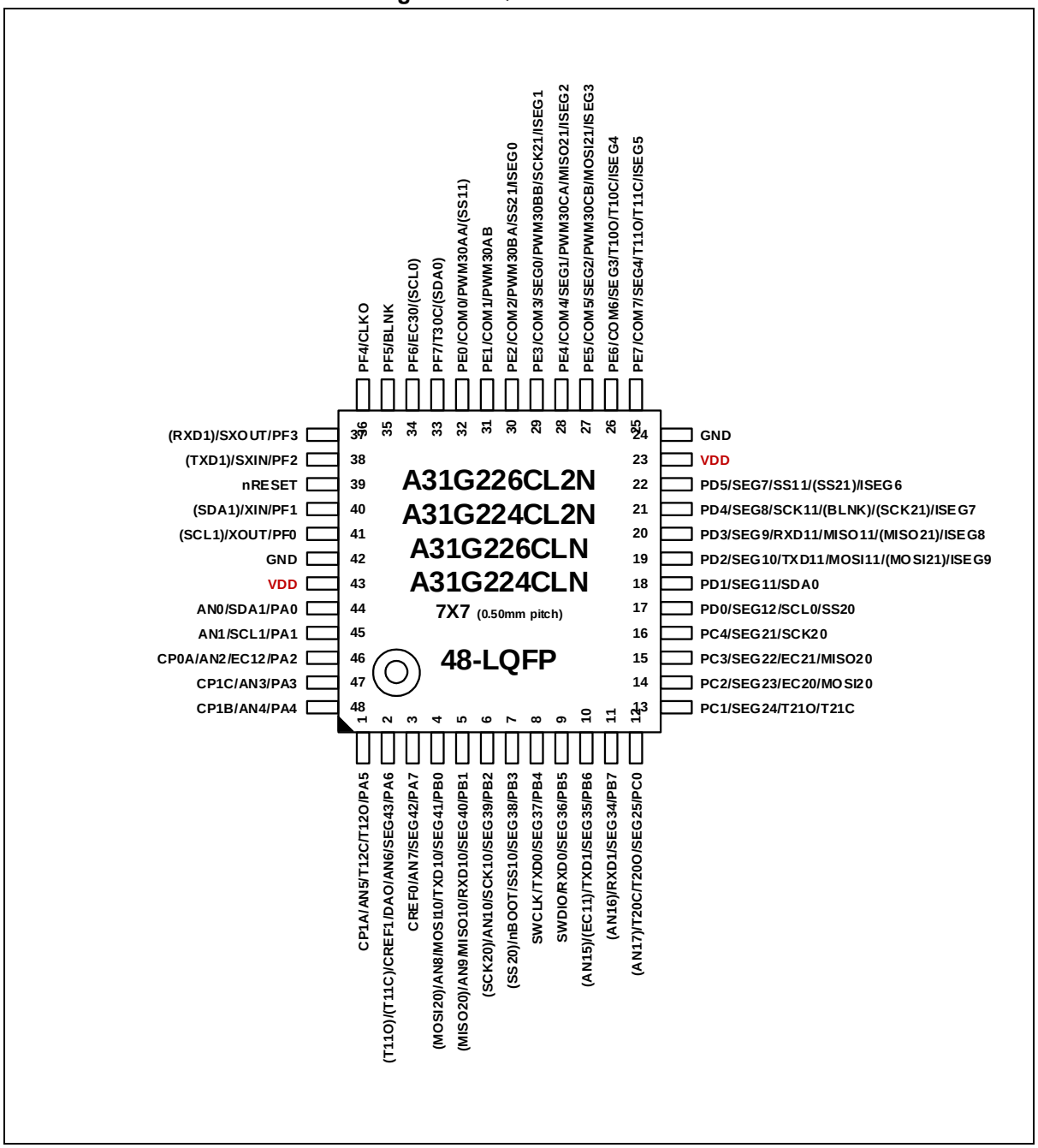
Figure 5. LQFP 64 Pinouts



2.1.3 A31G226CL2N/ A31G224CL2N/ A31G226CLN/ A31G224CLN (48-LQFP)

Pinouts of A31G22x 48-LQFP package are showed in Figure 6.

Figure 6. LQFP 48 Pinouts



2.2 Pin description

Pin configuration information in Table 3 contains two pairs of power/ground and other dedicated pins. These multi-function pins have up to ten selections of functions including GPIO. Configuration including pin ordering can be changed without notice.

Table 3. Pin Description

Pin no.			Pin no.	Type	Description	Remark
80-pin	64-pin	48-pin				
1	1	1	PA5*	IOUDS	PORT A Bit 5 Input/Output	
			T12O	O	Timer 12 Output	
			T12C	I	Timer 12 Capture Input	
			AN5	IA	Analog Input 5	
			CP1A	IA	Comparator input 1A	
2	2	2	PA6*	IOUDS	PORT A Bit 6 Input/Output	
			SEG43	O	LCD Segment Signal 43 Output	
			T11O	O	Timer 11 Output	
			T11C	I	Timer 11 Capture Input	
			AN6	IA	Analog Input 6	
			DAO	OA	Digital to analog output	
			CREF1	IA	Comparator 1 Reference Input	
3	3	3	PA7*	IOUDS	PORT A Bit 7 Input/Output	
			SEG42	O	LCD Segment Signal 42 Output	
			AN7	IA	Analog Input 7	
			CREF0	IA	Comparator 0 Reference Input	
4	4	4	PB0	IOUDS	PORT B Bit 0 Input/Output	
			SEG41	O	LCD Segment Signal 41 Output	
			TXD10*	O	UART Channel 10 TxD Input	
			MOSI10	I/O	SPI Channel 10 Master Out / Slave In	
			MOSI20	I/O	SPI Channel 20 Master Out / Slave In	
			AN8	IA	Analog Input 8	
5	5	5	PB1	IOUDS	PORT B Bit 1 Input/Output	
			SEG40	O	LCD Segment Signal 40 Output	
			RXD10*	I	UART Channel 10 RxD Input	
			MISO10	I/O	SPI10 Master-Input/Slave-Output Data signal	
			MISO20	I/O	SPI20 Master-Input/Slave-Output Data signal	
			AN9	IA	Analog Input 9	
6	6	6	PB2*	IOUDS	PORT B Bit 2 Input/Output	
			SEG39	O	LCD Segment Signal 39 Output	
			SCK10	I/O	SPI10 Data Clock Input/Output	
			SCK20	I/O	SPI20 Data Clock Input/Output	
			AN10	IA	Analog Input 10	
7	7	7	PB3	IOUDS	PORT B Bit 3 Input/Output	
			SEG38	O	LCD Segment Signal 38 Output	
			SS10	I/O	SPI10 Slave Select signal	
			SS20	I/O	SPI20 Slave Select signal	
			nBOOT*	I	Boot Mode Selection Pin	Pull-up

Table 3. Pin Description (continued)

Pin no.			Pin no.	Type	Description	Remark
80-pin	64-pin	48-pin				
8	8	8	PB4	IOUDS	PORT B Bit 4 Input/Output	
			SEG37	O	LCD Segment Signal 37 Output	
			TXD0	O	UART Channel 0 TxD Input	
			SWCLK*	I	SWD Clock Input	Pull-up
9	9	9	PB5*	IOUDS	PORT B Bit 5 Input/Output	
			SEG36	O	LCD Segment Signal 36 Output	
			RXD0	I	UART Channel 0 RxD Input	
			SWDIO*	I/O	SWD Data Input/Output	Pull-up
10	10	10	PB6*	IOUDS	PORT B Bit 6 Input/Output	
			SEG35	O	LCD Segment Signal 35 Output	
			TXD1	O	UART Channel 1 TxD Input	
			EC11	I	Timer 11 Event Count Input	
			AN15	IA	Analog Input 15	
11	11	11	PB7*	IOUDS	PORT B Bit 7 Input/Output	
			SEG34	O	LCD Segment Signal 34 Output	
			RXD1	I	UART Channel 1 RxD Input	
			AN16	IA	Analog Input 16	
12	12	-	PB8*	IOUDS	PORT B Bit 8 Input/Output	
			SEG33	O	LCD Segment Signal 33 Output	
			EC16	I	Timer 16 Event Count Input	
			T15O	O	Timer 15 Output	
			T15C	I	Timer 15 Capture Input	
13	13	-	PB9*	IOUDS	PORT B Bit 9 Input/Output	
			SEG32	O	LCD Segment Signal 32 Output	
			EC15	I	Timer 15 Event Count Input	
			T16O	O	Timer 16 Output	
			T16C	I	Timer 16 Capture Input	
14	14	-	PB10*	IOUDS	PORT B Bit 10 Input/Output	
			SEG31	O	LCD Segment Signal 31 Output	
			T16O	O	Timer 16 Output	
			T16C	I	Timer 16 Capture Input	
			EC15	I	Timer 15 Event Count Input	
15	15	-	PB11*	IOUDS	PORT B Bit 11 Input/Output	
			SEG30	O	LCD Segment Signal 30 Output	
			T15O	O	Timer 15 Output	
			T15C	I	Timer 15 Capture Input	
			EC16	I	Timer 16 Event Count Input	
16	-	-	PB12*	IOUDS	PORT B Bit 12 Input/Output	
			SEG29	O	LCD Segment Signal 29 Output	
17	-	-	PB13*	IOUDS	PORT B Bit 13 Input/Output	
			SEG28	O	LCD Segment Signal 28 Output	
18	-	-	PB14*	IOUDS	PORT B Bit 14 Input/Output	
			SEG27	O	LCD Segment Signal 27 Output	

Table 3. Pin Description (continued)

Pin no.			Pin no.	Type	Description	Remark
80-pin	64-pin	48-pin				
19	-	-	PB15*	IOUDS	PORT B Bit 15 Input/Output	
			SEG26	O	LCD Segment Signal 26 Output	
20	16	12	PC0*	IOUDS	PORT C Bit 0 Input/Output	
			SEG25	O	LCD Segment Signal 25 Output	
			T20O	O	Timer 20 Output	
			T20C	I	Timer 20 Capture Input	
			AN17	IA	Analog Input 17	
21	17	13	PC1*	IOUDS	PORT C Bit 1 Input/Output	Pull-up
			SEG24	O	LCD Segment Signal 24 Output	
			T21O	O	Timer 21 Output	
			T21C	I	Timer 21 Capture Input	
22	18	14	PC2*	IOUDS	PORT C Bit 2 Input/Output	Pull-up
			SEG23	O	LCD Segment Signal 23 Output	
			EC20	I	Timer 20 Event Count Input	
			MOSI20	I/O	SPI Channel 20 Master Out / Slave In	
23	19	15	PC3*	IOUDS	PORT C Bit 3 Input/Output	
			SEG22	O	LCD Segment Signal 22 Output	
			EC21	I	Timer 21 Event Count Input	
			MISO20	I/O	SPI20 Master-Input/Slave-Output Data signal	
24	20	16	PC4*	IOUDS	PORT C Bit 4 Input/Output	
			SEG21	O	LCD Segment Signal 21 Output	
			SCK20	I/O	SPI20 Data Clock Input/Output	
25	21	-	PC5*	IOUDS	PORT C Bit 5 Input/Output	
			SEG20	O	LCD Segment Signal 20 Output	
			SDA2	O	I^2C Channel 2 SDA In/Out	
26	22	-	PC6*	IOUDS	PORT C Bit 6 Input/Output	
			SEG19	O	LCD Segment Signal 19 Output	
			SCL2	O	I^2C Channel 2 SCL In/Out	
27	-	-	PC7*	IOUDS	PORT C Bit 7 Input/Output	
			SEG18	O	LCD Segment Signal 18 Output	
28	-	-	PC8*	IOUDS	PORT C Bit 8 Input/Output	
			SEG17	O	LCD Segment Signal 17 Output	
29	-	-	PC9*	IOUDS	PORT C Bit 9 Input/Output	
			SEG16	O	LCD Segment Signal 16 Output	
30	-	-	PC10*	IOUDS	PORT C Bit 10 Input/Output	
			SEG15	O	LCD Segment Signal 15 Output	
31	23	-	PC11*	IOUDS	PORT C Bit 11 Input/Output	
			SEG14	O	LCD Segment Signal 14 Output	
			EC10	I	Timer 10 Event Count Input	
32	24	-	PC12*	IOUDS	PORT C Bit 12 Input/Output	
			SEG13	O	LCD Segment Signal 13 Output	
			EC11	I	Timer 11 Event Count Input	

Table 3. Pin Description (continued)

Pin no.			Pin no.	Type	Description	Remark
80-pin	64-pin	48-pin				
33	25	17	PD0*	IOUDS	PORT D Bit 0 Input/Output	
			SEG12	O	LCD Segment Signal 12 Output	
			SCL0	O	I^2C Channel 0 SCL In/Out	
			SS20	I/O	SPI Channel 20 Slave Select signal	
34	26	18	PD1*	IOUDS	PORT D Bit 1 Input/Output	
			SEG11	O	LCD Segment Signal 11 Output	
			SDA0	O	I^2C Channel 0 SDA In/Out	
			EC10	I	Timer 10 Event Count Input	
35	27	19	PD2*	IOUDS	PORT D Bit 2 Input/Output	
			SEG10	O	LCD Segment Signal 10 Output	
			TXD11	O	UART Channel 11 TxD Input	
			MOSI11	I/O	SPI Channel 11 Master Out / Slave In	
			MOSI21	I/O	SPI Channel 21 Master Out / Slave In	
			ISEG9	O	Sink Type High Current Output	
36	28	20	PD3*	IOUDS	PORT D Bit 3 Input/Output	
			SEG9	O	LCD Segment Signal 9 Output	
			RXD11	I	UART Channel 11 RxD Input	
			MISO11	I/O	SPI11 Master-Input/Slave-Output Data signal	
			MISO21	I/O	SPI21 Master-Input/Slave-Output Data signal	
			ISEG8	O	Sink Type High Current Output	
37	29	21	PD4*	IOUDS	PORT D Bit 4 Input/Output	
			SEG8	O	LCD Segment Signal 8 Output	
			BLNK	I	External Sync Signal Input for T30 PWM	
			SCK11	I/O	SPI11 Data Clock Input/Output	
			SCK21	I/O	SPI21 Data Clock Input/Output	
			ISEG7	O	Sink Type High Current Output	
38	30	22	PD5*	IOUDS	PORT D Bit 5 Input/Output	
			SEG7	O	LCD Segment Signal 7 Output	
			SS11	I/O	SPI Channel 11 Slave Select signal	
			SS21	I/O	SPI Channel 21 Slave Select signal	
			ISEG6	O	Sink Type High Current Output	
39	31	23	VDD	P	VDD	
40	32	24	VSS	P	VS	
41	33	25	PE7*	IOUDS	PORT E Bit 7 Input/Output	
			COM7	O	LCD Common Signal 7 Outputs	
			SEG4	O	LCD Segment Signal 4 Output	
			T11O	O	Timer 11 Output	
			T11C	I	Timer 11 Capture Input	
			ISEG5	O	Sink Type High Current Output	

Table 3. Pin Description (continued)

Pin no.			Pin no.	Type	Description	Remark
80-pin	64-pin	48-pin				
42	34	26	PE6*	IOUDS	PORT E Bit 6 Input/Output	
			COM6	O	LCD Common Signal 6 Output	
			SEG3	O	LCD Segment Signal 3 Output	
			T10O	O	Timer 10 Output	
			T10C	I	Timer 10 Capture Input	
			ISEG4	O	Sink Type High Current Output	
43	35	27	PE5*	IOUDS	PORT E Bit 5 Input/Output	
			COM5	O	LCD Common Signal 5 Output	
			SEG2	O	LCD Segment Signal 2 Output	
			PWM30CB	O	Timer 30 PWM Output	
			MOSI21	I/O	SPI Channel 21 Master-Output / Slave-Input	
			ISEG3	O	Sink Type High Current Output	
44	36	28	PE4*	IOUDS	PORT E Bit 4 Input/Output	
			COM4	O	LCD Common Signal 4 Output	
			SEG1	O	LCD Segment Signal 1 Output	
			PWM30CA	O	Timer 30 PWM Output	
			MISO21	I/O	SPI21 Master-Input/Slave-Output Data signal	
			ISEG2	O	Sink Type High Current Output	
45	37	29	PE3*	IOUDS	PORT E Bit 3 Input/Output	
			COM3	O	LCD Common Signal 3 Output	
			SEG0	O	LCD Segment Signal 0 Output	
			PWM30BB	O	Timer 30 PWM Output	
			SCK21	I/O	SPI20 Data Clock Input/Output	
			ISEG1	O	Sink Type High Current Output	
46	38	30	PE2*	IOUDS	PORT E Bit 2 Input/Output	
			COM2	O	LCD Common Signal 2 Output	
			PWM30BA	O	Timer 30 PWM Output	
			SS21	I/O	SPI Channel 21 Slave Select signal	
			ISEG0	O	Sink Type High Current Output	
47	39	31	PE1*	IOUDS	PORT E Bit 1 Input/Output	
			COM1	O	LCD Common Signal 1 Output	
			PWM30AB	O	Timer 30 PWM Output	
48	40	32	PE0*	IOUDS	PORT E Bit 0 Input/Output	
			COM0	O	LCD Common Signal 0 Output	
			PWM30AA	O	Timer 30 PWM Output	
			SS11	I/O	SPI Channel 11 Slave Select signal	
49	-	-	PE15*	IOUDS	PORT E Bit 15 Input/Output	
			SS12	I/O	SPI Channel 12 Slave Select signal	
50	-	-	PE14*	IOUDS	PORT E Bit 14 Input/Output	
			SCK12	I/O	SPI12 Data Clock Input/Output	
51	-	-	PE13*	IOUDS	PORT E Bit 13 Input/Output	
			RXD12	I	UART Channel 12 RxD Input	
			MISO12	I/O	SPI12 Master-Input/Slave-Output Data signal	

Table 3. Pin Description (continued)

Pin no.			Pin no.	Type	Description	Remark
80-pin	64-pin	48-pin				
52	-	-	PE12*	IOUDS	PORT E Bit 12 Input/Output	
			TXD12	O	UART Channel 12 TxD Input	
			MOSI12	I/O	SPI Channel 12 Master Out / Slave In	
53	41	-	PE11*	IOUDS	PORT E Bit 11 Input/Output	
			SS13	I/O	SPI Channel 13 Slave Select signal	
			VLC3	IA	External LCD Voltage bias 3	
54	42	-	PE10*	IOUDS	PORT E Bit 10 Input/Output	
			SCK13	I/O	SPI13 Data Clock Input/Output	
			VLC2	IA	External LCD Voltage bias 2	
55	43	-	PE9*	IOUDS	PORT E Bit 9 Input/Output	
			RXD13	I	UART Channel 13 RxD Input	
			MISO13	I/O	SPI13 Master-Input/Slave-Output Data signal	
			VLC1	IA	External LCD Voltage bias 1	
56	44	-	PE8*	IOUDS	PORT E Bit 8 Input/Output	
			TXD13	O	UART Channel 13 TxD Input	
			MOSI13	I/O	SPI Channel 13 Master Out / Slave In	
			VLC0	IA	External LCD Voltage bias 0	
57	45	33	PF7*	IODS	PORT F Bit 7 Input/Output	Open-drain
			T30C	I	Timer 30 Capture Input	
			(SDA0)	O	I^2C Channel 0 SDA In/Out	
58	46	34	PF6*	IODS	PORT F Bit 6 Input/Output	Open-drain
			EC30	I	Timer 30 Event Count Input	
			(SCL0)	O	I^2C Channel 0 SCL In/Out	
59	47	35	PF5*	IODS	PORT F Bit 5 Input/Output	Open-drain
			BLNK	I	External Sync Signal Input for T30 PWM	
60	48	36	PF4*	IOUDS	PORT F Bit 4 Input/Output	
			CLKO	O	System Clock Output	
61	-	-	PF11*	IOUDS	PORT F Bit 11 Input/Output	
			T14O	O	Timer 14 Output	
			T14C	I	Timer 14 Capture Input	
62	-	-	PF10*	IOUDS	PORT F Bit 10 Input/Output	
			T13O	O	Timer 13 Output	
			T13C	I	Timer 13 Capture Input	
63	-	-	PF9*	IOUDS	PORT F Bit 9 Input/Output	
			EC14	I	Timer 14 Event Count Input	
64	-	-	PF8*	IOUDS	PORT F Bit 8 Input/Output	
			EC13	I	Timer 13 Event Count Input	
65	49	37	PF3*	IOUDS	PORT F Bit 3 Input/Output	
			SXOUT	O	Sub Oscillator Output	
			(RXD1)	I	UART Channel 1 RxD Input	

Table 3. Pin Description (continued)

Pin no.			Pin no.	Type	Description	Remark
80-pin	64-pin	48-pin				
66	50	38	PF2*	IOUDS	PORT F Bit 2 Input/Output	
			SXIN	I	Sub Oscillator Input	
			(TXD1)	O	UART Channel 1 TxD Input	
67	51	39	nRESET	IU	External Reset Input	Pull-up
68	52	40	PF1*	IOUDS	PORT F Bit 1 Input/Output	
			XIN	I	Main Oscillator Input	
			(SDA1)	O	I^2C Channel 2 SDA In/Out	
69	53	41	PF0*	IOUDS	PORT F Bit 0 Input/Output	
			XOUT	O	Main Oscillator Output	
			(SCL1)	O	I^2C Channel 2 SCL In/Out	
70	54	42	VSS	P	VSS	
71	55	43	VDD	P	VDD	
72	56	-	PA8	IOUDS	PORT A Bit 8 Input/Output	
			AN11	IA	Analog Input 11	
73	57	-	PA9*	IOUDS	PORT A Bit 9 Input/Output	
			AN12	IA	Analog Input 12	
74	58	-	PA10*	IOUDS	PORT A Bit 10 Input/Output	
			AN13	IA	Analog Input 13	
75	59	-	PA11*	IOUDS	PORT A Bit 11 Input/Output	
			AN14	IA	Analog Input 14	
76	60	44	PA0*	IOUDS	PORT A Bit 0 Input/Output	
			SDA1	O	I2C Channel 1 SDA In/Out	Open-drain
			AN0	IA	Analog Input 0	
77	61	45	PA1*	IOUDS	PORT A Bit 1 Input/Output	
			SCL1	O	I2C Channel 1 SCL In/Out	Open-drain
			AN1	IA	Analog Input 1	
78	62	46	PA2*	IOUDS	PORT A Bit 2 Input/Output	
			EC12	I	Timer 12 Event Count Input	
			AN2	IA	Analog Input 2	
			CP0A	IA	Comparator plus input 0	
79	63	47	PA3*	IOUDS	PORT A Bit 3 Input/Output	
			AN3	IA	Analog Input 3	
			CP1C	IA	Comparator plus input 1C	
80	64	48	PA4*	IOUDS	PORT A Bit 4 Input/Output	
			AN4	IA	Analog Input 4	
			CP1B	IA	Comparator plus input 1B	

NOTES:

1. I=Input, O=Output, U=Pull-up, D=Pull-down, S=Schmitt-Trigger Input Type, C=CMOS Input Type, A=Analog, P=Power
2. The * means 'Selected pin function after reset condition'.
3. Pin order may be changed with revision notice.
4. PB3 (nBOOT), nRESET, PB5 (SWDIO), PB4 (SWCLK) are default pull-up pins.
5. PC1 and PC2 are default pull-up pins.

3 System and memory overview

3.1 System architecture

Main system of A31G22x series consists of the followings:

- ARM® Cortex® -M0+ core
- General purpose DMAC (Direct Memory Access Controller)
- Internal SRAM
- Internal Code and Data Flash memory
- Two AHB buses

3.1.1 Cortex-M0+ core

The ARM® Cortex®-M0+ processor is the most energy-efficient ARM processor available. It builds on the very successful Cortex-M0+ processor, retaining full instruction set and tool compatibility, while further reducing energy consumption and increasing performance. Document “DDI 0484C” from ARM provides detail information of Cortex-M0+.

3.1.2 Interrupt controller

Table 4. Interrupt Vector Map

Priority	Vector Address	Interrupt Source
-16	0x0000_0000	Stack Pointer
-15	0x0000_0004	Reset Address
-14	0x0000_0008	NMI Handler
-13	0x0000_000C	Hard Fault Handler
-12	0x0000_0010	Reserved
-11	0x0000_0014	
-10	0x0000_0018	
-9	0x0000_001C	
-8	0x0000_0020	
-7	0x0000_0024	
-6	0x0000_0028	
-5	0x0000_002C	SVCall Handler
-4	0x0000_0030	Reserved
-3	0x0000_0034	
-2	0x0000_0038	PenSV Handler
-1	0x0000_003C	SysTick Handler

Table 4. Interrupt Vector Map (continued)

Priority	Vector Address	Interrupt Source
0	0x0000_0040	LVI
1	0x0000_0044	SYSCLKFAIL
2	0x0000_0048	WDT
3	0x0000_004C	GPIOA, GPIOB
4	0x0000_0050	GPIOC, GPIOD
5	0x0000_0054	GPIOE
6	0x0000_0058	GPIOF
7	0x0000_005C	TIMER10
8	0x0000_0060	TIMER11
9	0x0000_0064	TIMER12
10	0x0000_0068	I2C0
11	0x0000_006C	USART10
12	0x0000_0070	WT
13	0x0000_0074	TIMER30
14	0x0000_0078	I2C1
15	0x0000_007C	TIMER20
16	0x0000_0080	TIMER21
17	0x0000_0084	USART11
18	0x0000_0088	ADC
19	0x0000_008C	UART0
20	0x0000_0090	UART1
21	0x0000_0094	TIMER13
22	0x0000_0098	TIMER14
23	0x0000_009C	TIMER15
24	0x0000_00A0	TIMER16
25	0x0000_00A4	I2C2, SPI20
26	0x0000_00A8	USART12, USART13, SPI21
27	0x0000_00AC	DAC
28	0x0000_00B0	TS
29	0x0000_00B4	Reserved
30	0x0000_00B8	Reserved
31	0x0000_00BC	CMP, CRC

NOTES:

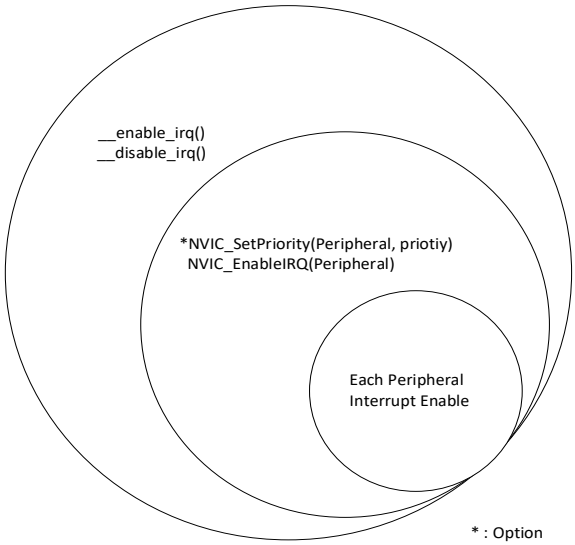
1. Each interrupt has an associated priority-level register. Each of them is 2 bits wide, occupying the two MSBs of the Interrupt Priority Level Registers. Each Interrupt Priority Level Register occupies 1 byte (8 bits).NVIC registers in the Cortex-M0+ processor can only be accessed using word-size transfers, so for each access, four Interrupt Priority Level Registers are accessed at the same time.

   ** __NVIC_PRIO_BITS = 2

2. Figure 7 is a caution when using Peripheral Interrupts. Interrupt don't work if only peripheral interrupts are enabled. Enable the function in core to enable interrupt.

   * __enable_irq > NVCI_EnableIRQ(Peripheral) > Each Peripheral Interrupt

Figure 7. Interrupt Block Diagram



3.2 Memory organization

Program memory, data memory, registers and I/O ports are organized in the same address space.

3.2.1 Register boundary address

Table 5 gives the boundary addresses of peripherals in A31G22x series.

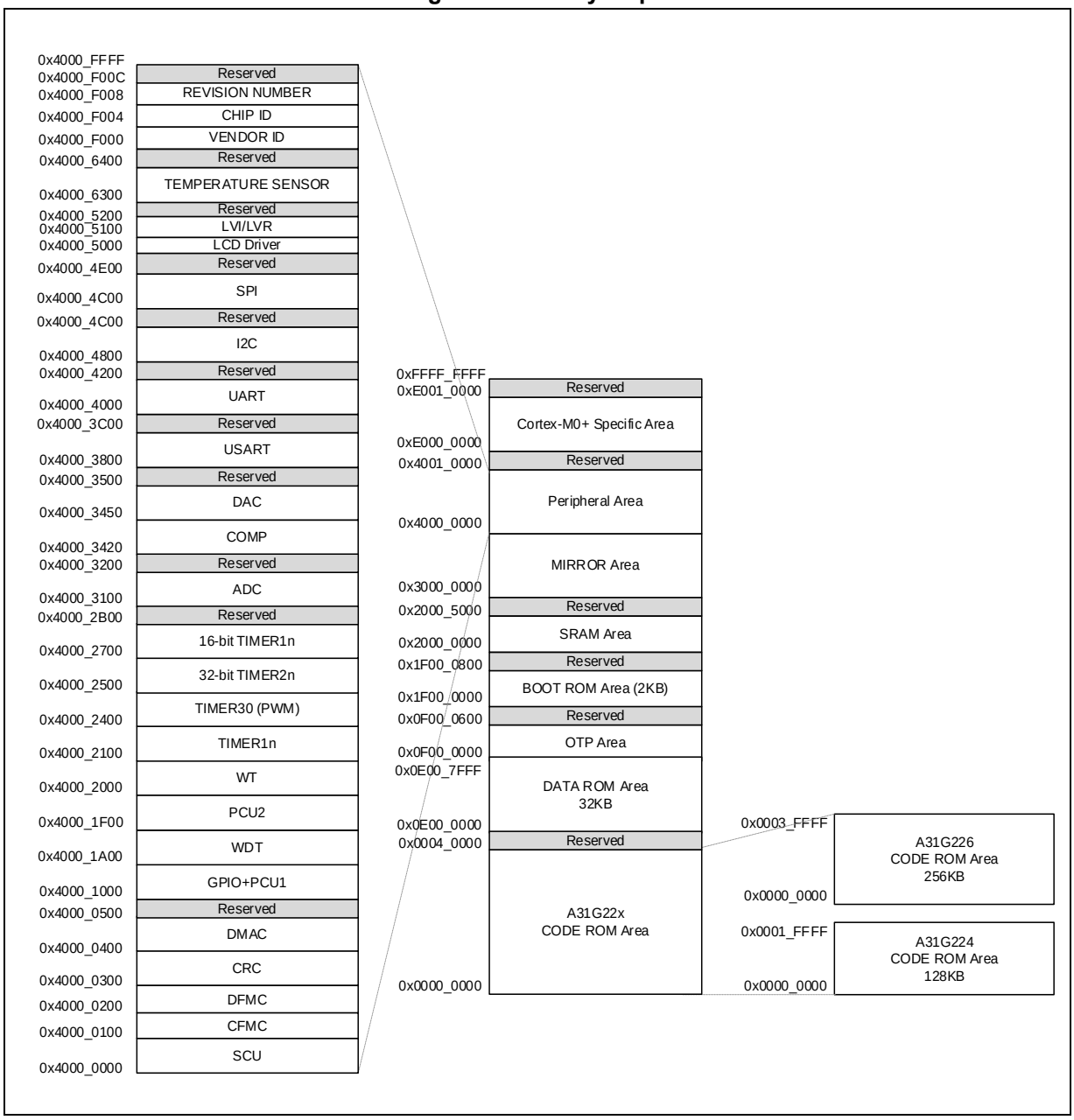
Table 5. A31G22x Memory Boundary Addresses

Boundary address	Memory area
0x4000_0000	SCU
0x4000_F000	SCUCC
0x4000_5100	SCULV
0x4000_1000/1100/1200/1300/1400/1500	PCU A/B/C/D/E/F
0x4000_0100	Code Flash Controller
0x4000_0200	Data Flash Controller
0x2000_0000	Internal SRAM
0x4000_0400/0410/0420/0430/0440/0450/0460/0470	DMAC 0/1/2/3/4/5/6/7
0x4000_1A00	WDT
0x4000_2000	WT
0x4000_2100/2200/2300/2700/2800/2900/2A00	Timer 10/11/12/13/14/15/16
0x4000_2500/2600	Timer 20/21
0x4000_2400	Timer 30
0x4000_3800/3900/3A00/3B00	USART 10/11/12/13
0x4000_4000/4100	UART 1/2
0x4000_4C00/4D00	SPI 20/21
0x4000_4800/4900/4A00	I2C 0/1/2
0x4000_3100	12-bit ADC
0x4000_3450	12-bit DAC
0x4000_3420	Comparator
0x4000_5000	LCD Driver
0x4000_0300	CRC
0x4000_6300	Temp sensor

3.2.2 Memory map

Figure 8 shows addressable memory space in memory map.

Figure 8. Memory Map



3.2.3 Embedded SRAM

A31G22x series has a block of 0-wait on-chip SRAM. The size of SRAM is 20KB and its base address is 0x2000_0000.

SRAM memory area is usually used for data memory and stack memory. Sometimes the code is dumped into the SRAM memory for fast operation or flash erase/programming operation. This device does not support memory remap strategy. So jump and return are required to perform the code in SRAM memory area.

3.2.4 Flash memory overview

A31G22x series provides internal 256KB code flash memory and its controller. This is enough to control the general system. Self-programming is available and ISP and SWD programming is also supported in boot or debugging mode.

Instruction and data cache buffer are present and overcome the low bandwidth flash memory. CPU can access flash memory with one wait state up to 48MHz bus frequency.

3.2.5 Boot mode

Pins for Boot mode

A31G22x has a Boot mode option to program internal flash memory. System enters in Boot mode by setting BOOT pin to ‘L’ at reset timing (Normal state is ‘H’).

In Boot mode, UART boot is available as well:

- USART10_TXD/USART10_RXD port is used in UART boot.

Pins for Boot mode are listed in Table 6.

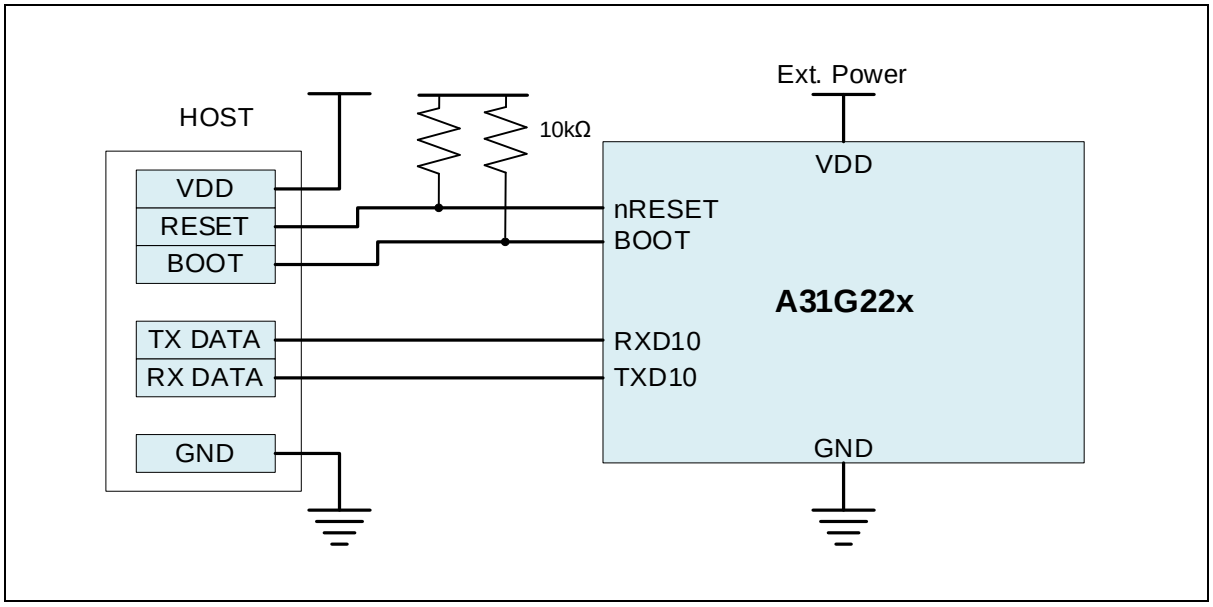
Table 6. Boot Mode Pin List

Block	Pin name	Dir	Description
SYSTEM	nRESET	I	Reset Input signal
	nBOOT	I	‘Low’ to enter Boot mode
UART mode of USART10	USART10_RXD/PB1	I	USART10 Boot Receive Data
	USART10_TXD/PB0	O	USART10 Boot Transmit Data

Connections for Boot mode

A user can design a target board using any of boot mode ports such as UART mode of USART10. A sample connection diagram of Boot mode is introduced in Figure 9:

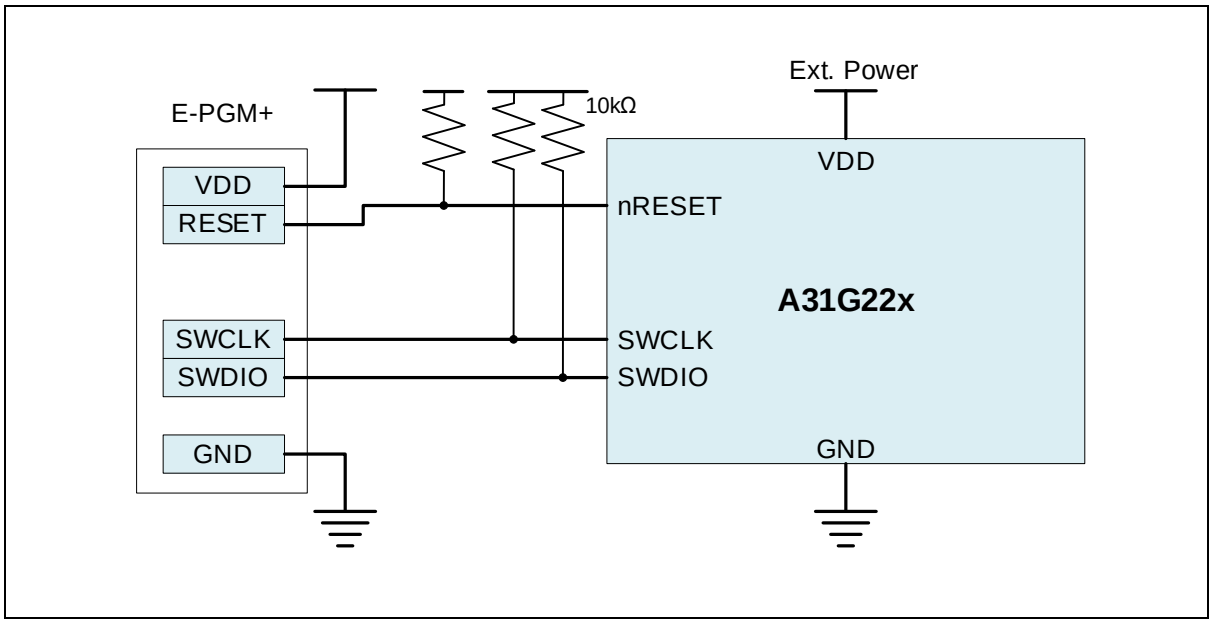
Figure 9. Connection Diagram of UART10 Boot



SWD mode connections

A user can use SWD mode for writing with E-PGM+ or A-Link (CMSIS-DAP) debugger. This mode can be used for writing & debugging.

Figure 10. Connection Diagram of E-PGM+ and SWD Port



4 System Control Unit (SCU)

A31G22x series has a built-in intelligent power control block which manages system analog blocks and operating modes. System Control Unit (SCU) block controls an internal reset and clock signals to maintain optimize system performance and power dissipation.

Four pins in Table 7 are assigned for SCU block.

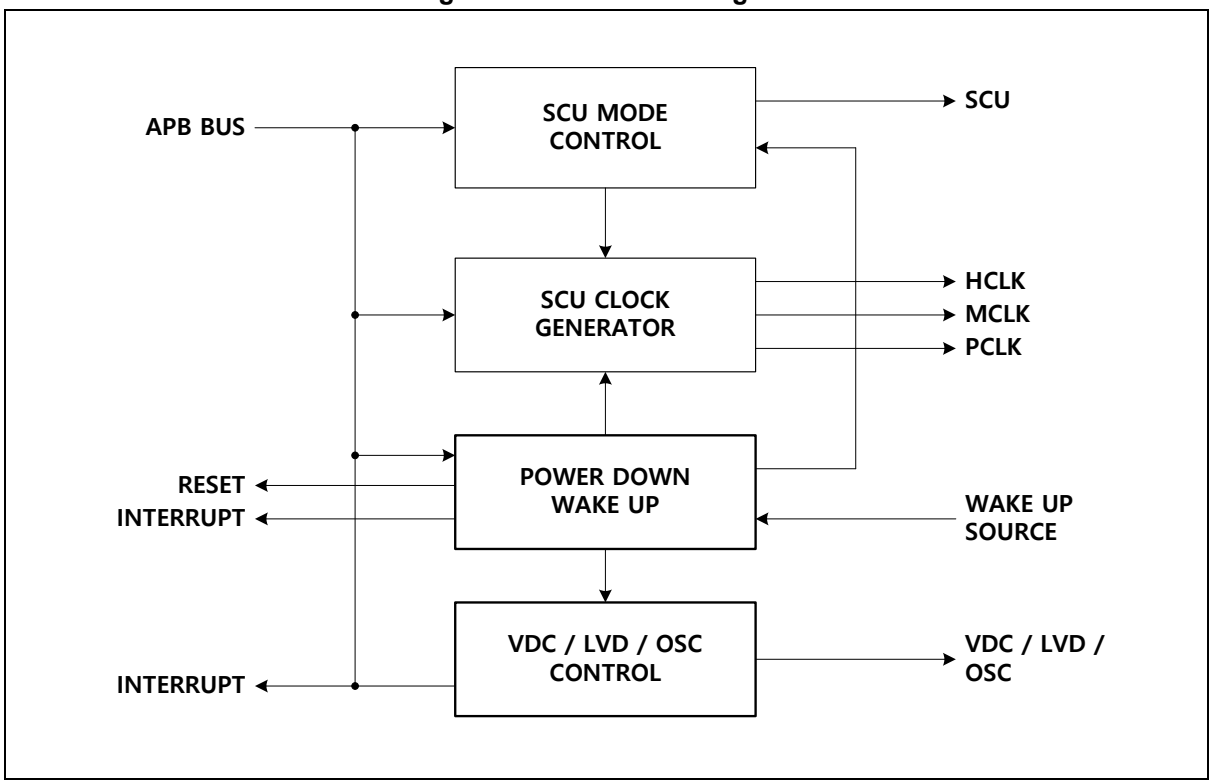
Table 7. SCU Pins

Pin name	Type	Description
nRESET	I	External Reset Input
XIN/XOUT	OSC	External Crystal Oscillator
SXIN/SXOUT	OSC	External sub-Crystal Oscillator
CLKO	O	Clock Output Monitoring Signal

4.1 SCU block diagram

SCU block diagram is introduced in Figure 11.

Figure 11. SCU Block Diagram

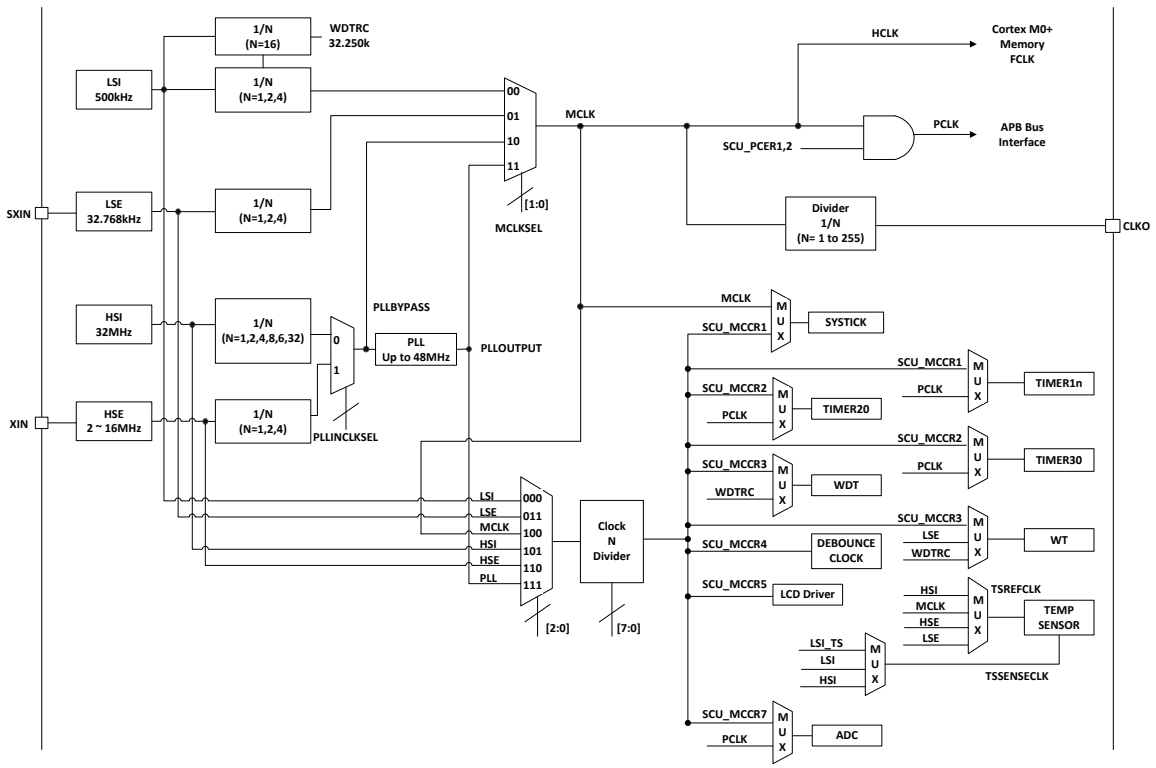


4.2 Clock system

A31G22x series has two main operating clocks. One is HCLK which produces a clock signal both for CPU and AHB bus system. The other is PCLK which produces a clock signal for peripheral systems.

A user can keep the clock system variation under software control. Through Figure 12 and Table 8, users learn about the clock system of A31G22x devices and clock sources.

Figure 12. Clock Tree Configuration



NOTES:

1. In the block diagram above, peripheral blocks not specified in the SCU_MCCRx register use PCLK as a reference clock by default.
2. If you want to use a peripheral clock based on LSI / LSE / HSI / HSE in your application, it is recommended to enable the clock source before enabling the peripheral.

All multiplexers switching clock sources have a glitch-free circuit in each. So a clock can be switched without glitch risks. When a user tries to change a clock mux control, both of clock sources must be alive. If one of them is not alive, clock change operation is stopped and system will be halted and not be recovered.

Table 8. Clock Sources

Clock name	Frequency	Description
HSE	1-16 MHz	High Speed External Oscillator
LSE	32.768KHz	Low Speed External Oscillator
HSI	32 MHz	High Speed Internal OSC
LSI	500KHz	Low Speed Internal OSC
LSITS	—	Internal OSC for temp sensor

4.2.1 HCLK clock domain

HCLK clock feeds the clock to the CPU and the AHB bus. Cortex-M0+ CPU requires 2 clocks related with FCLK and HCLK. FCLK is free running clock and it is always running except in DEEP-SLEEP mode. HCLK can be stopped in SLEEP mode.

BUS system and memory systems are operated by MCLK clock. Maximum bus operating clock speed is 48MHz.

4.2.2 PCLK clock domain

PCLK is the master clock of all peripherals. Each peripheral clock is enabled by SCU_PCER1, and SCU_PCER2 registers can be used by each peripheral. Before enabling the PCLK input clock of each block, it can't be accessible even reading its registers. It can be stopped in DEEP-SLEEP mode.

4.2.3 Clock configuration procedure

After powering up, the default system clock is fed by LSI (500KHz) clock. By default LSI is enabled at power up sequence. The other clock sources will be enabled by user controls with the LSI system clock.

HSI (32MHz) clock can be enabled by SCU_CSCR register.

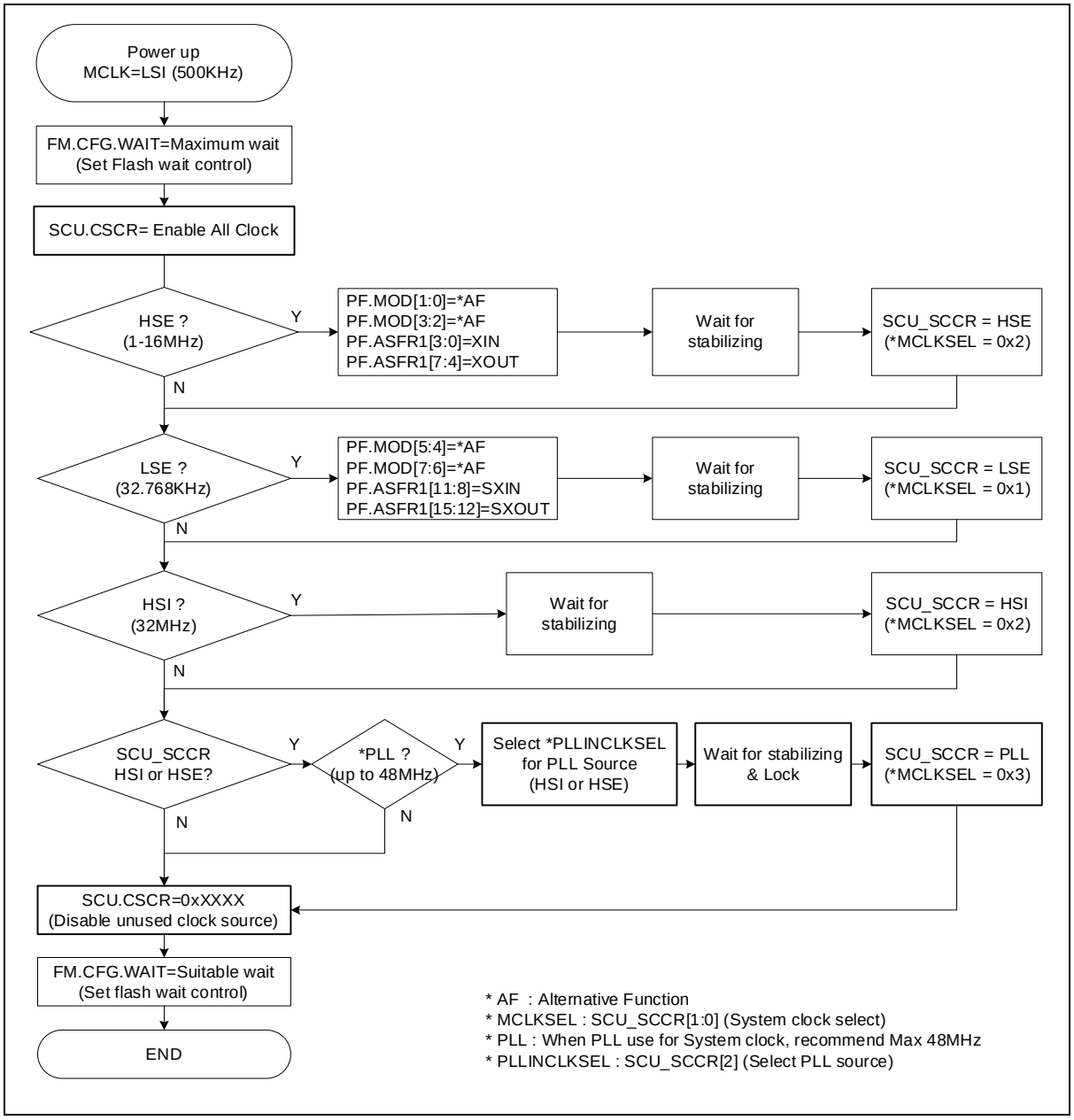
HSE (1-16MHz) clock can be enabled by SCU_CSCR register. Prior to enable the HSE block, the pin mux configuration should be set for XIN, XOUT function. PF1 and PF0 pins are shared with HSE's XIN and XOUT function – PF_MOD and PF_AFSR1 registers should be configured properly. After enabling the HSE block, you must wait for more than Typ. 200ms time to ensure stable operation of crystal oscillation.

LSE (32.768KHz) clock can be enabled by SCU_CSCR register. Prior to enable the LSE block, the pin mux configuration should be set for SXIN, SXOUT function. PF2 and PF3 pins are shared with LSE's SXIN and SXOUT function – PC_MOD and PC_AFSR1 registers should be configured properly.

After enabling the LSE block, you must wait for more than Typ. 2s time to ensure stable operation of crystal oscillation. You can change an MCLK by using the SCU_SCCR register.

You can find an example flow chart configuring the system clock in Figure 13.

Figure 13. Clock Change Procedure



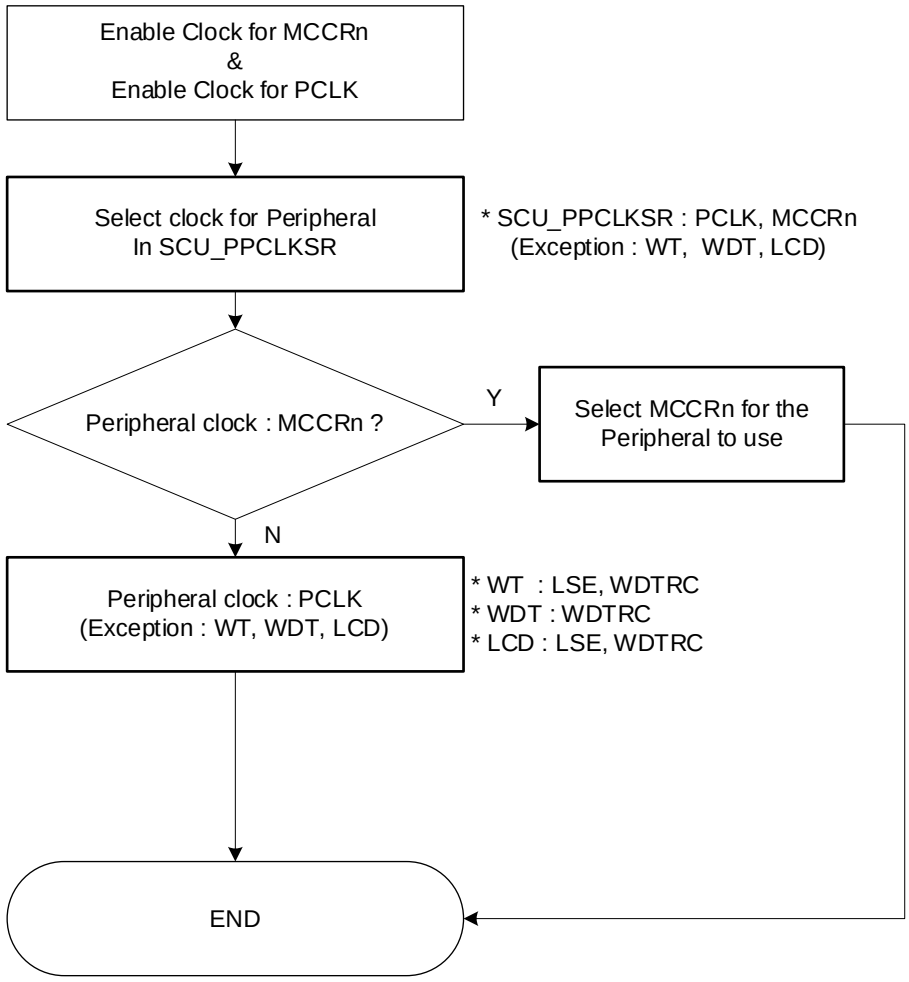
When you speed up the system clock to the maximum operating frequency, you should check flash wait control configuration. Flash read access time is one of limitation factor for performance. The wait control recommendation is suggested in Table 9.

Table 9. Flash Wait Control Recommendation

FM.CFG.WAIT	FLASH Access Wait	Available Max System clock frequency
00	0 clock wait	~20MHz
01	1 clock wait	~40MHz
10	2 clock wait	~48MHz

Figure 14 shows how to set the peripheral clock. Selecting a peripheral clock is a typical method of MCCRn and PCLK. Exceptionally WT, WDT, LCD use other clocks besides MCCRn and PCLK. (n = 1, 2, 3, 4, 5, 6 and 7).

Figure 14. Peripheral Clock Select (n: 1, 2, 3, 4, 5, 6 and 7)



NOTES:

1. The WDTRC clock outputs 32.250KHz frequency generated by dividing the 500KHz LSI clock by 16 in the internal logic.
2. This WDTRC clock can be the source clock of the WDT, WT, LCD and TIMER20 capture signals.

4.3 Reset

A31G22x series has two system reset options. One is to cold reset that is effective during power up or down sequence. The other is warm reset which is generated by several reset sources. A reset event makes a chip to turn to an initial state. Reset sources of the cold reset and the warm reset are listed in Table 10.

Table 10. Reset Sources of Cold Reset and Warm Reset

	Cold reset	Warm reset
Reset sources	• POR (Power On Reset) • LVR reset	• nRESET Pin • WDT reset • MCLK Fail reset • HSE Fail reset • S/W reset • CPU request reset

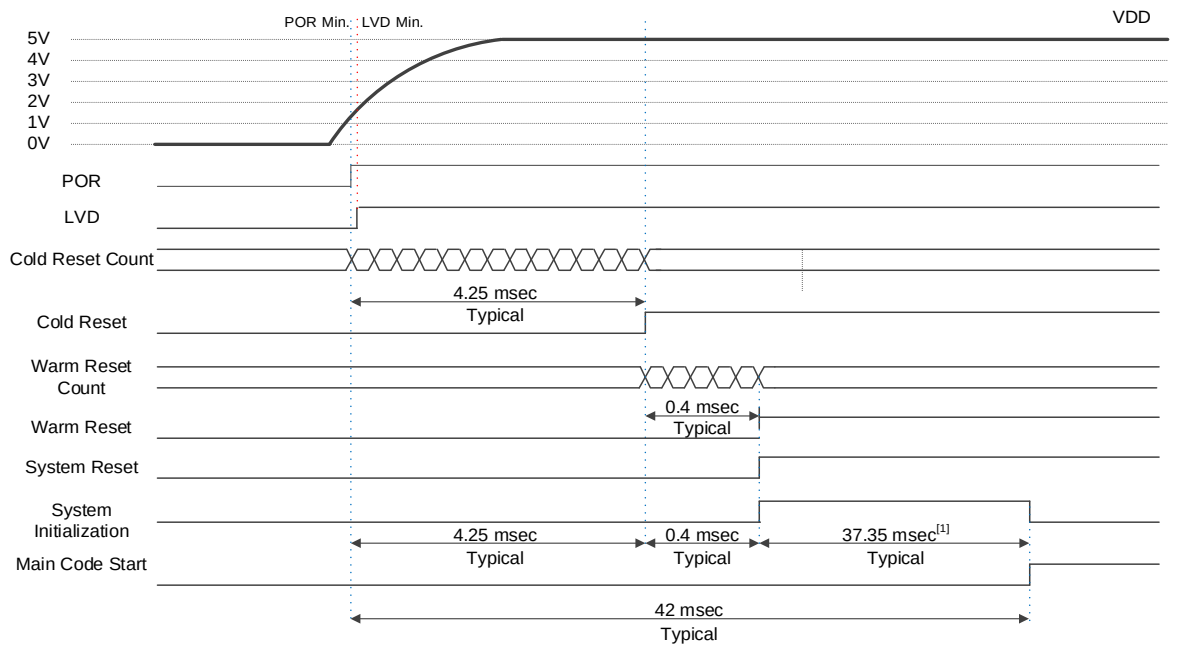
4.3.1 Cold reset

Cold reset is an important feature of a chip when power is up. This characteristic will affect overall system boot.

Internal VDC is enabled when VDD power is turn on. Internal POR trigger level is 1.2V of VDD voltage out level. At this time, boot operation is started. The LSI clock is enabled and counts 4ms time for internal VDC level stabilizing. In this time, VDD voltage level should be over than initial LVR level (1.56V). After 4ms counting, the cold reset is released and counts 0.4ms time for warm reset synchronizing. After releasing both cold and warm reset, BOOTROM and CPU are running.

Figure 15 shows power up sequence and internal reset waveforms.

Figure 15. Power up Procedure



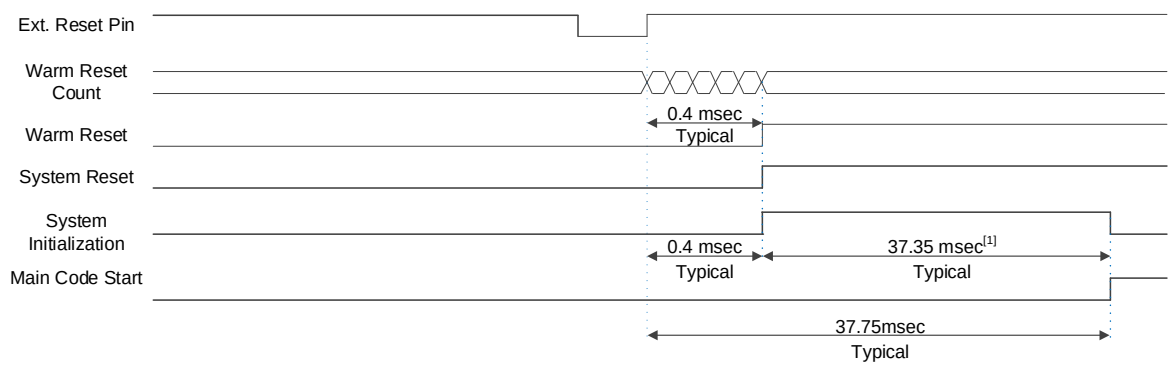
NOTE: [1] System Initialization time after warm reset is based on LSI clock operation.

4.3.2 Warm reset

Warm reset event has several reset sources and some parts of chip returns to an initial state when the warm reset condition is occurred.

The warm reset source is controlled by SCU_RSER register and the status is appeared in SCU_RSSR register. The reset for each peripheral blocks is controlled by SCU_PRER register. The reset can be masked independently.

Figure 16. Warm Reset Diagram



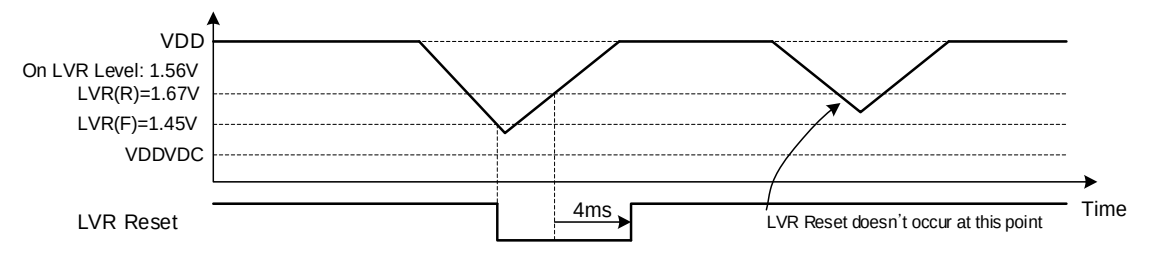
NOTE: [1] System Initialization time after warm reset is based on LSI clock operation.

4.3.3 LVR reset

Voltage level of LVR is set by low voltage reset configuration register (SCULV_LVRCNFG). Reset status of the LVR is shown in SCU_RSSR register.

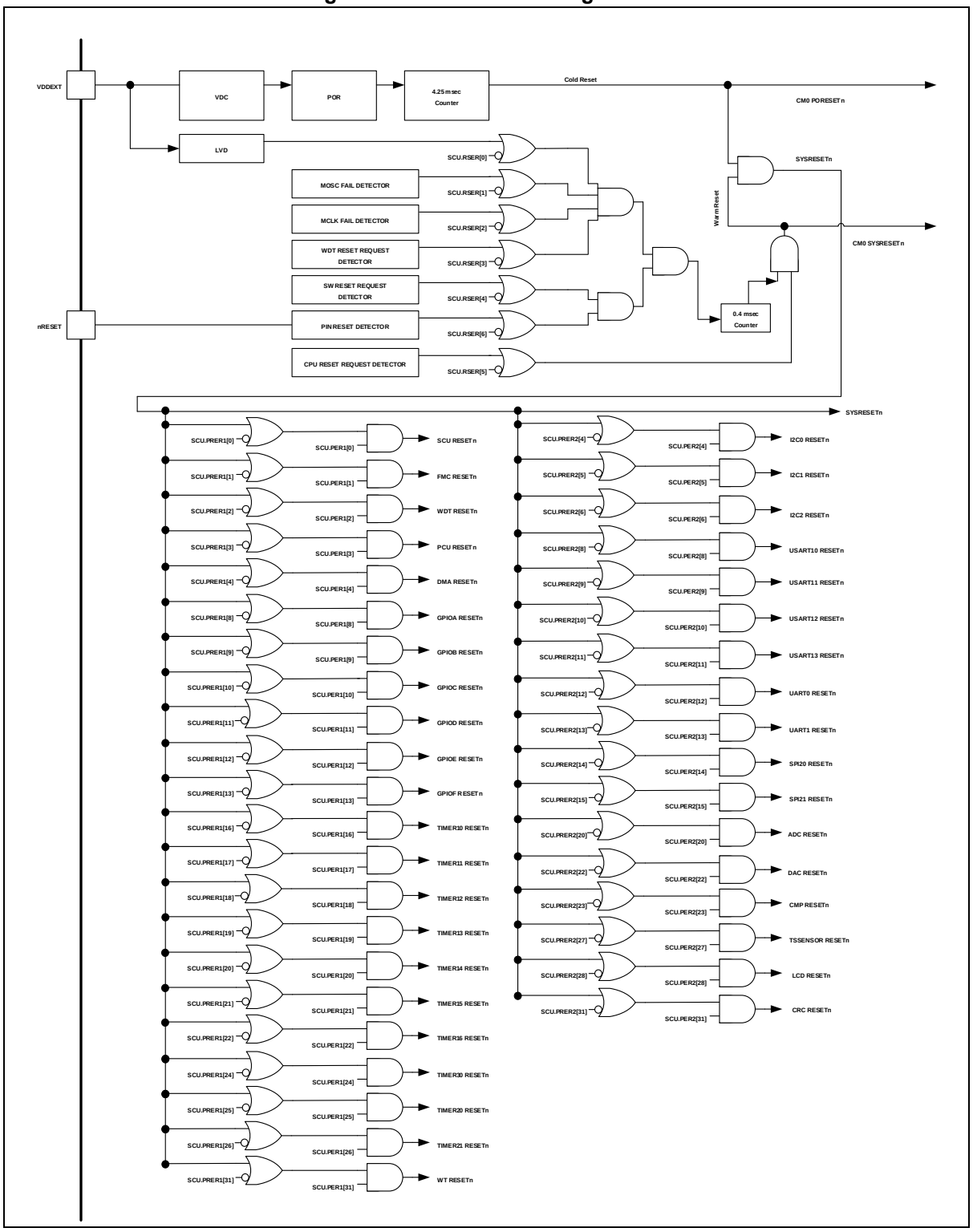
LVR (Low Voltage Reset) must be always enabled to guarantee the operation of the IC. The factory default LVR is set to 1.56V with a margin applied to the minimum operating voltage to guarantee the operation of the IC, but the Reset Detect Level can be changed with the SCU_LVRCNFIG register.

Figure 17. LVR Reset Timing Diagram



4.3.4 Reset tree

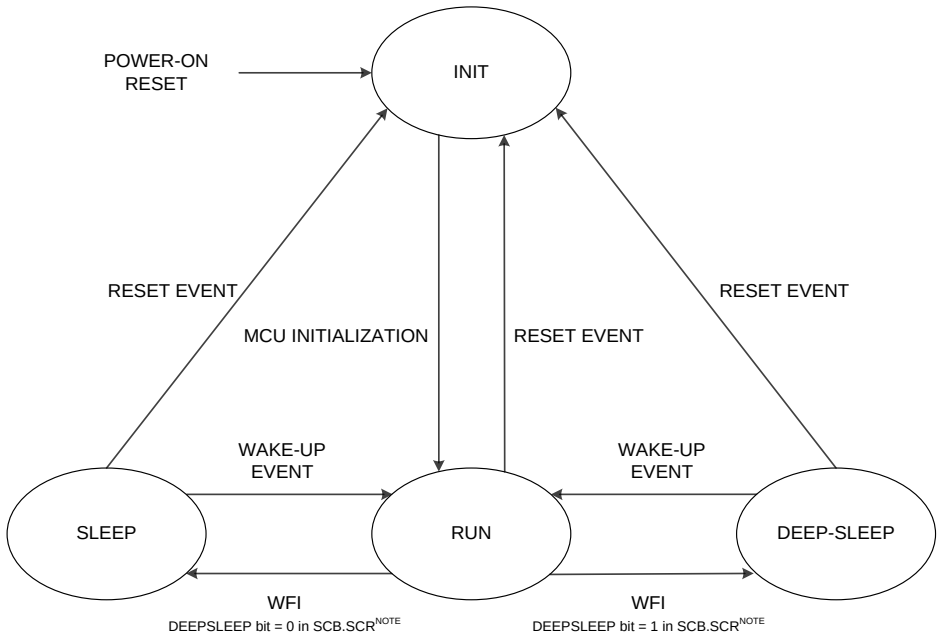
Figure 18. Reset Tree Configuration



4.4 Operation mode

INIT mode is an initial state of the chip when a reset is asserted. In RUN mode, CPU shows the maximum performance with high-speed clock system. SLEEP mode and DEEP- SLEEP mode can be used as a low power consumption mode. In the low power consumption mode, power is effectively managed to reduce power consumption by halting processor core and unused peripherals. Figure 19 describes transition between the operation modes.

Figure 19. Transition between Operation Modes



NOTE: SCB.SCR means System Control Register in System Control Block.

Table 11. Operation Mode

MODE	Condition	After the wake up event	After the reset event
RUN	POWER ON	N/A	INIT
SLEEP	WFI (Wait for Interrupt): SCB.SCR[2]*=0	RUN	INIT
DEEP-SLEEP	WFI (Wait for Interrupt): SCB.SCR[2]*=1	RUN	INIT

By default, SLEEP and DEEP-SLEEP modes automatically power off the LSE and LSI oscillation. As such, the peripherals fed with a clock signal from the LSE or LSI will stop operating in SLEEP or DEEP-SLEEP mode. To keep those peripherals running in this mode, the MCU can be configured in either of the following ways:

A. Set the LSI or LSE as the clock source to feed the peripherals that need to continue running in SLEEP or DEEP-SLEEP mode.

B. To continue using the LSE or LSI in SLEEP or DEEP-SLEEP mode, set the LSEAON or LSIAON bit in the SCU_SMR register to “1.” LSEAON and LSIAON bits will prevent the LSE or LSI from automatically being powered off. Next, configure the SCU_SCCR register manually to disable the clock sources that are NOT in use in SLEEP or DEEP-SLEEP mode.

4.4.1 RUN mode

In RUN mode, CPU and the peripheral hardware operate with a high-speed clock. After a reset followed by INIT state, the system enters in the RUN mode.

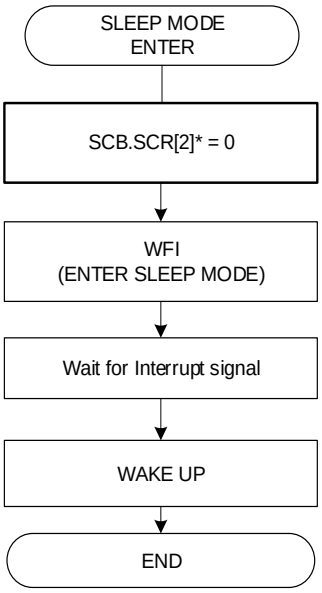
4.4.2 SLEEP mode

When the core goes under SLEEP using WFI instruction, the chip enters in IDLE state. In SLEEP mode, only CPU is stopped. Each peripheral function can be enabled by the function enable and clock enable bit in the PER and PCER register. By using the wake-up source enable register (SCU_WSER), designers can set the wake-up sources of various peripherals, including GPIOA through GPIOF (5–10), WT (4), WDT (3), main oscillator error (2), and LVD (0). When a wake-up event occurs based on the settings, the MCU will return to run mode after POR reset.

Table 12. SLEEP Mode Configuration

Mode	Condition	Wakeup source
SLEEP (Idle state)	WFI SCB.SCR[2]* = 0, VDCCON[18] = 0	Source included in WUER

Figure 20. SLEEP Mode Operation Sequence



NOTE: SCB.SCR is System Control Register in System Control Block.

4.4.3 DEEP-SLEEP mode

When the core goes under DEEP-SLEEP using WFI instruction, the chip enters in power down state. In DEEP-SLEEP mode, all peripherals are stopped. Once power is supplied, internal SRAM and registers maintain their values.

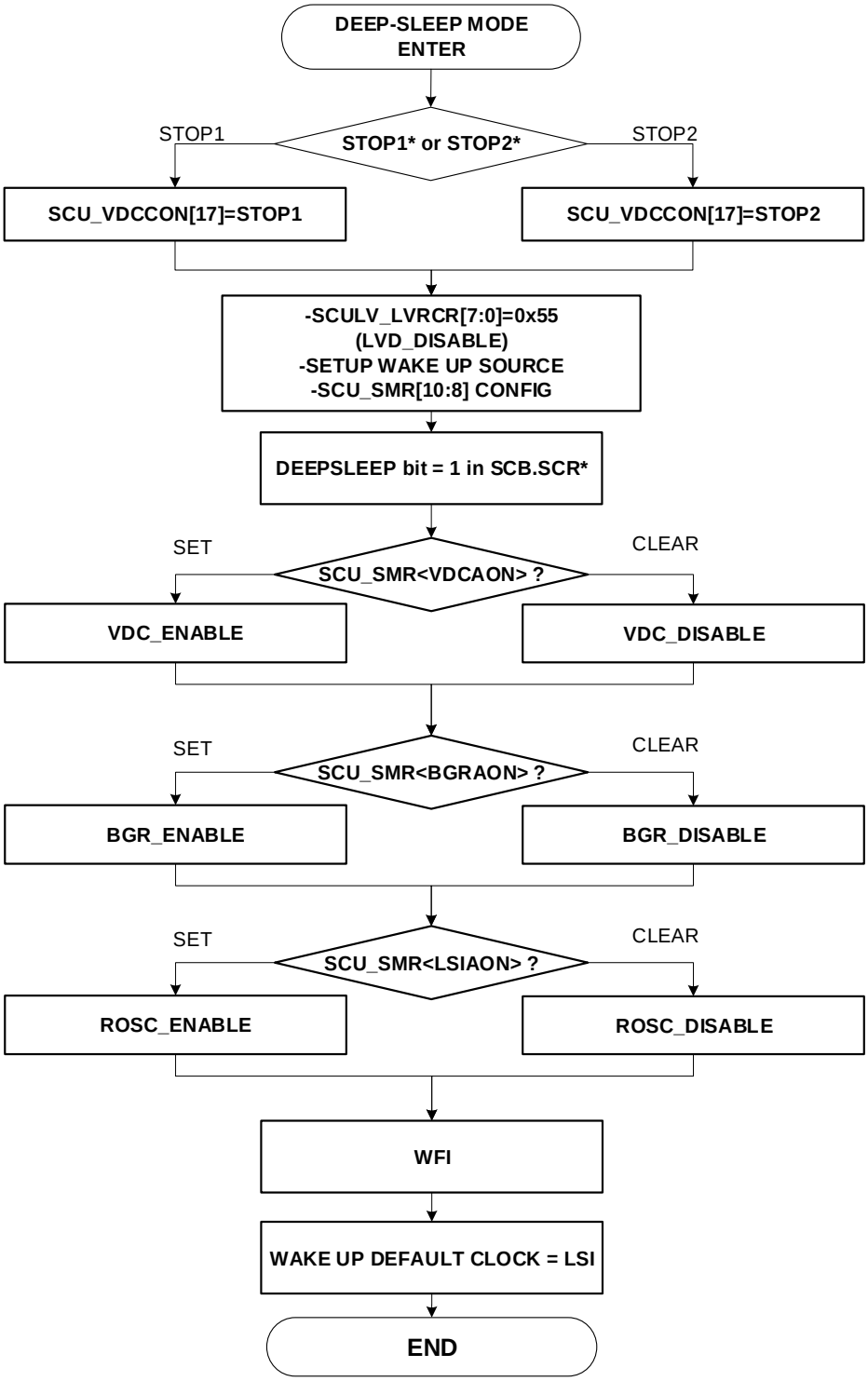
To wake up in DEEP-SLEEP mode, an interrupt request must be generated and can be selected in the SCU_WUER register. Stabilization time is 4ms after wakeup event occurs.

When entering in DEEP-SLEEP mode, LSI is selected as the MCLK, and HSE is selected as the PLL input clock. These are maintained after wakeup.

Table 13.DEEP-SLEEP Mode Configuration

Mode	Condition	Wakeup source
DEEP-SLEEP (Power down state)	WFI SCB.SCR[2]* = 1, VDCCON[18] = 0	Source included in WUER

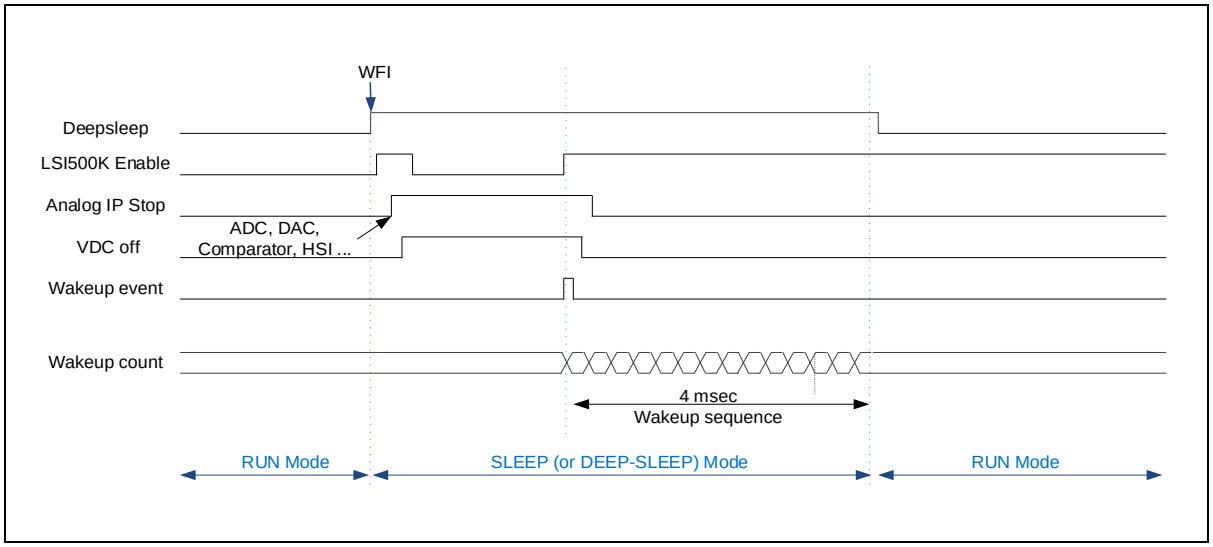
Figure 21. DEEP-SLEEP Mode Sequence



NOTES:

1. When STOP1, VDC load current is limited 500uA.
2. When STOP2, VDC load current is limited 10uA.
3. SCB.SCR is System Control Register in System Control Block.

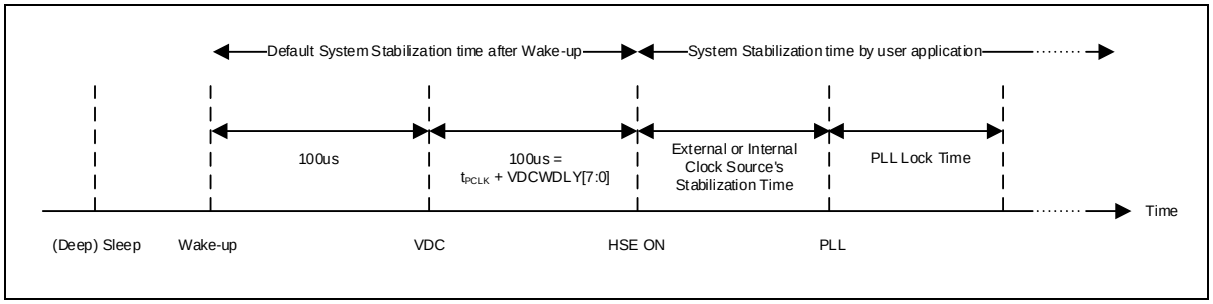
Figure 22. SLEEP and DEEP-SLEEP Mode Timing Diagram



4.4.4 Wake-up timing

Figure 23 shows stabilization timing of RUN mode after wake up from SLEEP mode or DEEP-SLEEP mode by configuring WUER register for wake-up sources.

Figure 23. System Stabilization Timing after wake-up



5 PCU and GPIO

Port Control Unit (PCU) configures and controls external I/Os as listed in the followings:

- External signal directions of each pins
- Interrupt trigger mode for each pins
- Internal pull-up/down register control and open drain control
- Remaps function to use USART1n channel as SPI2n channel. (n = 0, 1)
- Controls sink-type LED ports for high current driving (SEG0 to SEG9)
- SPI20 port strength configuration for high speed communication.

General Purpose Input/Output (GPIO) is corresponding to the most pins except dedicated-function pins. GPIO ports are controlled by GPIO block as listed in the followings:

- Output signal level (H/L) select
- External interrupt interface (Level, Rising edge, Falling edge, Both edge)
- Pull up/down enable or disable

Up to 75 pins in Table 14 are assigned for PCU and GPIO blocks.

Table 14. PCU and GPIO pins

Pin name	Type	80-pin: 75 ports	64-pin: 59 ports	48-pin: 43 ports
PA	IO	PA0 to PA11	PA0 to PA11	PA0 to PA8
PB	IO	PB0 to PB15	PB0 to PB11	PB0 to PB7
PC	IO	PC0 to PC12	PC0 to PC7 PC11 to PC12	PC0 to PC4
PD	IO	PD0 to PD5	PD0 to PD5	PD0 to PD5
PE	IO	PE0 to PE15	PE0 to PE11	PE0 to PE7
PF	IO	PF0 to PF11	PF0 to PF7	PE0 to PF7

5.1 PCU and GPIO block diagram

Figure 24 describes PCU in block diagram.

Figure 24. PCU Block Diagram

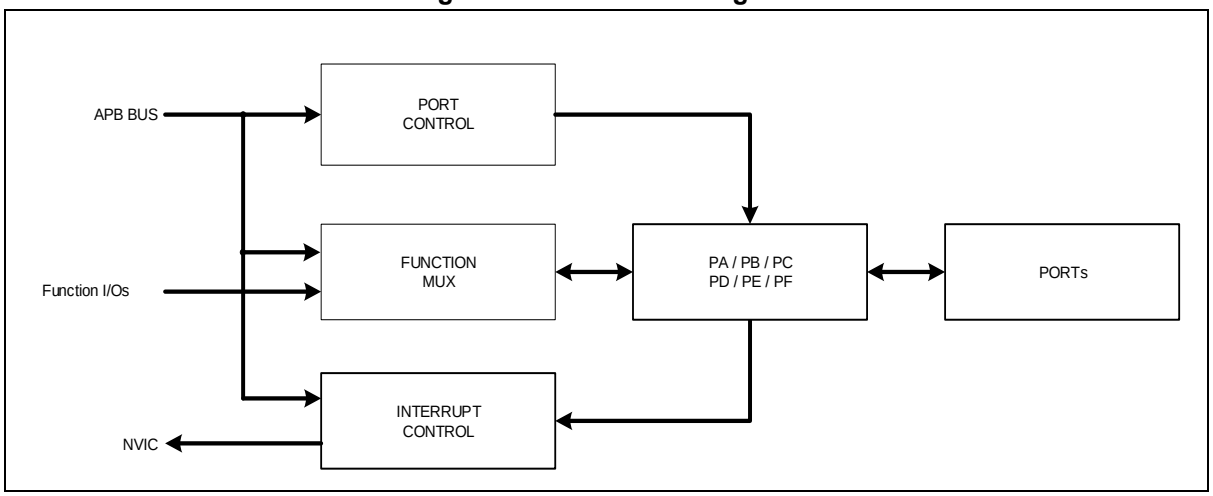


Figure 25 describes GPIO in block diagram, and Figure 26 introduces external interrupt I/O pins.

Figure 25. GPIO Block Diagram

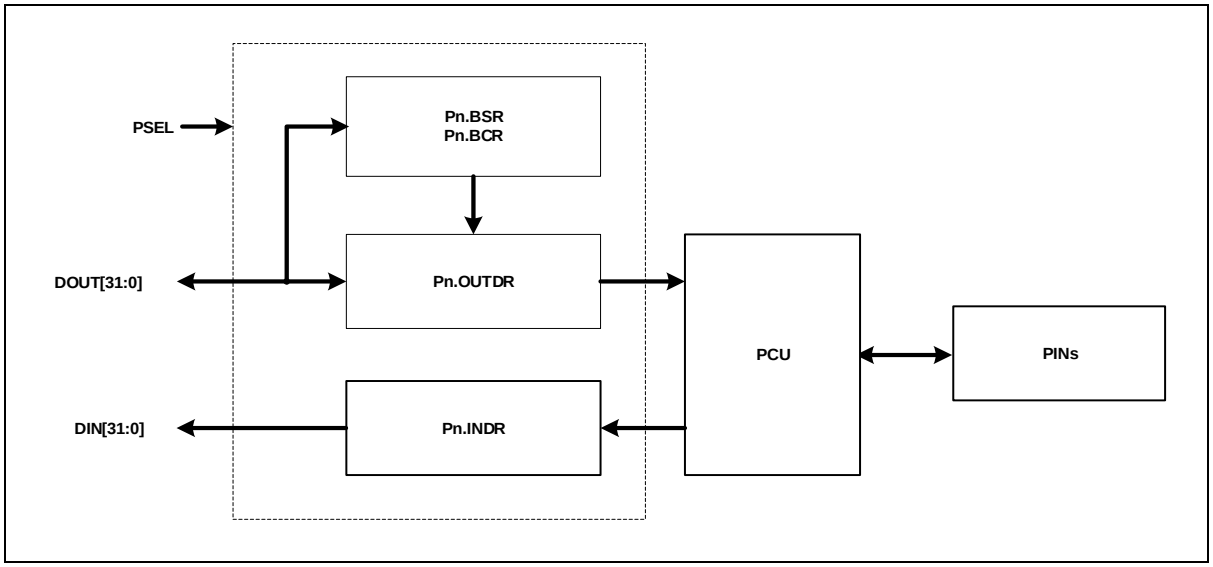


Figure 26. I/O Port Block Diagram (External Interrupt I/O Pins)

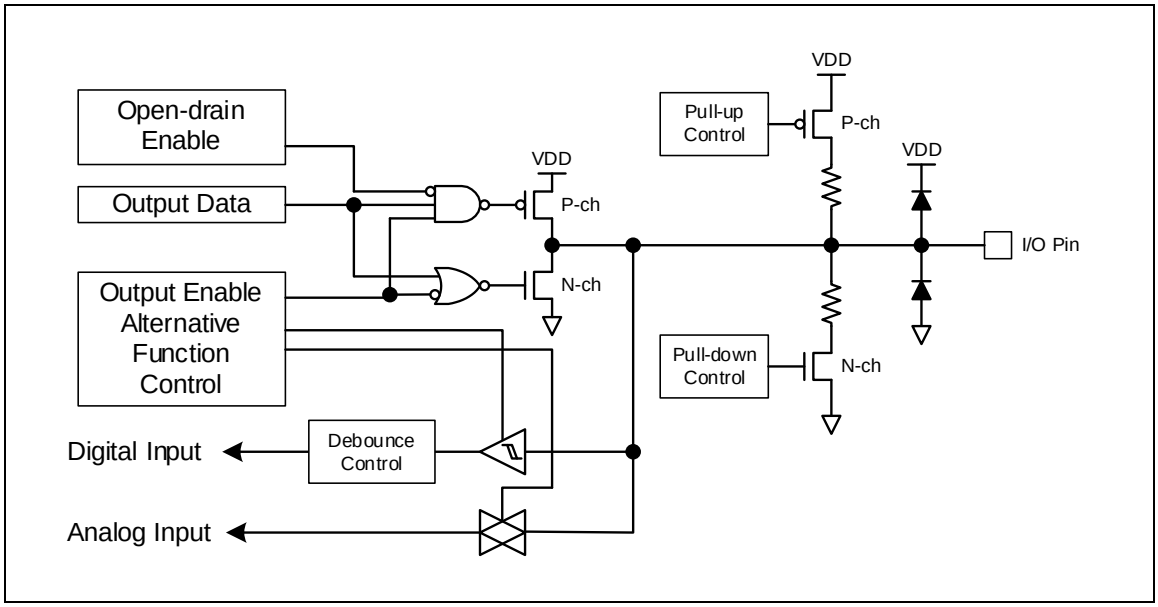
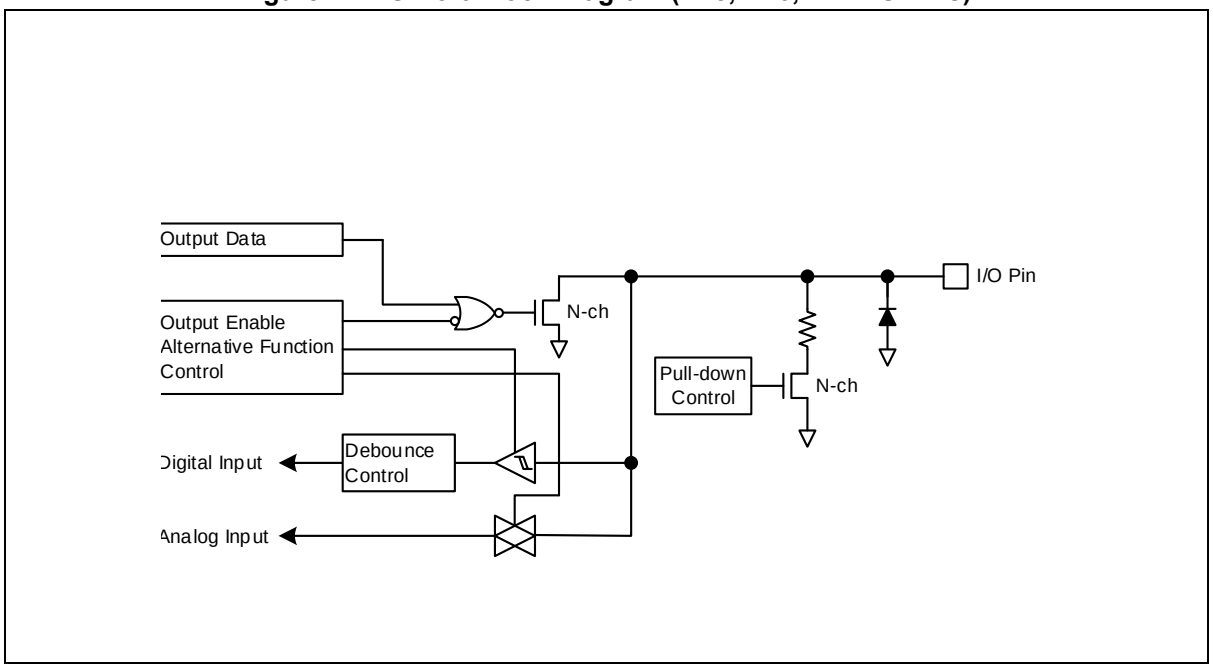


Figure 27. I/O Port Block Diagram (PF5, PF6, PF7 I/O Pins)



5.2 Pin multiplexing

GPIO pins have alternative function pins.

Table 15 shows pin multiplexing information.

Table 15. GPIO Alternative Function

Pin name	Alternative function				
	AF0	AF1	AF2	AF3	AF4
PA0		I2C1_SDA1		ADC_AN0	
PA1		I2C1_SCL1		ADC_AN1	
PA2		TIMER12_EC12		ADC_AN2/ CP0A	
PA3				ADC_AN3/ CP1C	
PA4				ADC_AN4/ CP1B	
PA5		TIMER12_T12O	TIMER12_T12C	ADC_AN5/ CP1A	
PA6	LCD_SEG43	TIMER11_T11O+	TIMER11_T11C+	ADC_AN6/ CREF1/ DAO	
PA7	LCD_SEG42			ADC_AN7/ CREF0	
PA8				ADC_AN11	
PA9				ADC_AN12	
PA10				ADC_AN13	
PA11				ADC_AN14	
PB0	LCD_SEG41	USART10_TXD10	USART10_MOSI10/ SPI20_MOSI20	ADC_AN8	
PB1	LCD_SEG40	USART10_RXD10	USART10_MISO10/ SPI20_MISO20	ADC_AN9	
PB2	LCD_SEG39		USART10_SCK10/ SPI20_SCK20	ADC_AN10	
PB3	LCD_SEG38	nBOOT	USART_SS10/ SPI20_SS20		
PB4	LCD_SEG37	UART0_TXD0	SWD_SWCLK		
PB5	LCD_SEG36	UART0_RXD0	SWD_SWDIO		
PB6	LCD_SEG35	UART1_TXD1	T11_EC11+	ADC_AN15	
PB7	LCD_SEG34	UART1_RXD1		ADC_AN16	
PB8	LCD_SEG33	T15_T15O	T15_T15C	T16_EC16	
PB9	LCD_SEG32	T16_T16O	T16_T16C	T15_EC15	
PB10	LCD_SEG31	T16_T16C	T15_EC15	T16_T16O	
PB11	LCD_SEG30	T15_T15C	T16_EC16	T15_T15O	
PB12	LCD_SEG29				
PB13	LCD_SEG28				
PB14	LCD_SEG27				
PB15	LCD_SEG26				
PC0	LCD_SEG25	T20_T20O	T20_T20C	ADC_AN17	
PC1	LCD_SEG24	T20_T21O	T20_T21C		
PC2	LCD_SEG23	T20_EC20	SPI20_MOSI20		
PC3	LCD_SEG22	T21_EC21	SPI20_MISO20		

Table 15. GPIO Alternative Function (continued)

Pin name	Alternative function				
	AF0	AF1	AF2	AF3	AF4
PC4	LCD_SEG21		SPI20_SCK20		
PC5	LCD_SEG20	I2C2_SDA2			
PC6	LCD_SEG19	I2C2_SCL2			
PC7	LCD_SEG18				
PC8	LCD_SEG17				
PC9	LCD_SEG16				
PC10	LCD_SEG15				
PC11	LCD_SEG14	T10_EC10			
PC12	LCD_SEG13	T11_EC11			
PD0	LCD_SEG12	I2C0_SCL0	SPI20_SS20		
PD1	LCD_SEG11	I2C0_SDA0	T10_EC10		
PD2	LCD_SEG10	USART11_TXD11	USART11_MOSI11/ SPI21_MOSI21		LED_ISEG9
PD3	LCD_SEG9	USART11_RXD11	USART11_MISO11/ SPI21_MISO21		LED_ISEG8
PD4	LCD_SEG8	T30_BLNK	USART11_SCK11/ SPI21_SCK21		LED_ISEG7
PD5	LCD_SEG7		USART11_SS11/ SPI21_SS21		LED_ISEG6
PE0	LCD_COM0	TIMER30_PWM30AA	USART11_SS11		
PE1	LCD_COM1	TIMER30_PWM30AB			
PE2	LCD_COM2	TIMER30_PWM30BA	SPI21_SS21		LED_ISEG0
PE3	LCD_COM3/ LCD_SEG0	TIMER30_PWM30BB	SPI21_SCK21		LED_ISEG1
PE4	LCD_COM4/ LCD_SEG1	TIMER30_PWM30C A	SPI21_MISO21		LED_ISEG2
PE5	LCD_COM5/ LCD_SEG2	TIMER30_PWM30C B	SPI21_MOSI21		LED_ISEG3
PE6	LCD_COM6/ LCD_SEG3	TIMER10_T10O	TIMER10_T10C		LED_ISEG4
PE7	LCD_COM7/ LCD_SEG4	TIMER11_T11O	TIMER11_T11C		LED_ISEG5
PE8		USART13_TXD13	USART13_MOSI13	LCD_VLC0	
PE9		USART13_RXD13	USART13_MISO13	LCD_VLC1	
PE10			USART13_SCK13	LCD_VLC2	
PE11			USART_SS13	LCD_VLC3	
PE12		USART12_TXD12	USART12_MOSI12		
PE13		USART12_RXD12	USART12_MISO12		
PE14			USART12_SCK12		
PE15			USART_SS12		

Table 15. GPIO Alternative Function (continued)

Pin name	Alternative function				
	AF0	**AF1**	**AF2**	**AF3**	**AF4**
PF0		I2C1_SCL1		XOUT	
PF1		I2C1_SDA1		XIN	
PF2		UART1_TXD1		SXIN	
PF3		UART1_RXD1		SXOUT	
PF4		CLKO			
PF5		TIMER30_BLNK			
PF6		TIMER30_EC30	I2C0_SCL0		
PF7		TIMER30_T30C	I2C1_SDA0		
PF8		TIMER13_EC13			
PF9		TIMER14_EC14			
PF10		TIMER13_T13O	TIMER13_T13C		
PF11		TIMER14_T14O	TIMER14_T14C		

NOTE: On connection with debugger host, SWCLK and SWDIO pins are always for SW-DP pins. So, the corresponding bits of PB_MOD/PB_TYP/PB_AFSR1/PB_PUPD registers may not be written by software.

6 Code Flash memory controller (CFMC)

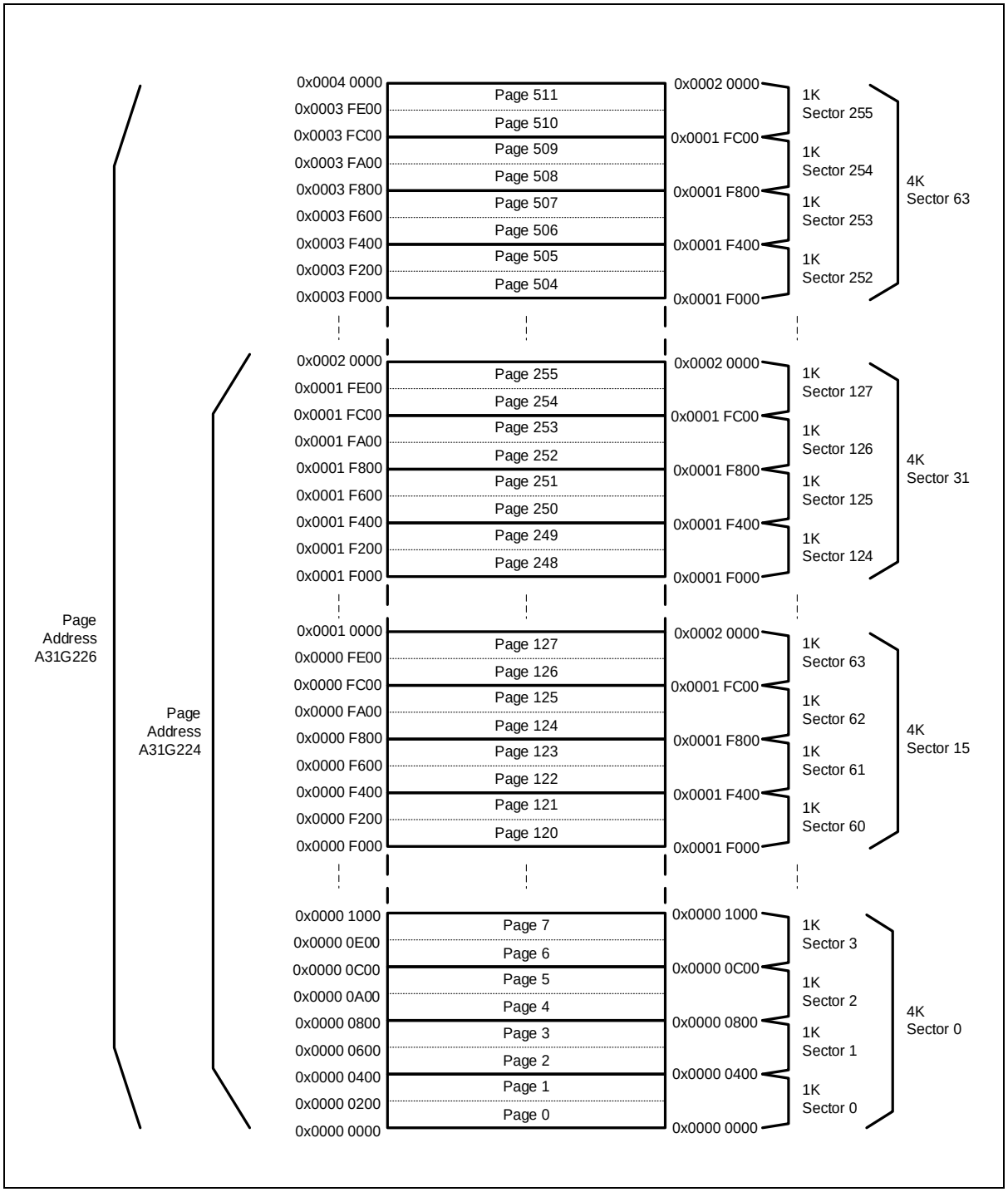
Code Flash Memory Controller is an internal flash memory interface controller, and includes following features as shown below:

- 256KB or 128KB code flash memory
- Wait, 0-wait to 6-wait (default : 5-wait)
- Read protection support
- Write protection support
  - Write protection with 16KB-unit
  - Write protection in 1KB-unit of the first region of the first region of each bank for the user boot loader
- Self-program and Self-erase on code flash memory
- Memory swap functions
- Endurance: 10,000 Cycles
- Data Retention: 10 Years

Table 16. Code Flash Memory Controller Features

Item	Description	
Size	256KB (A31G226)	128KB (A31G224)
Start Address	0x0000_0000	0x0000_0000
End Address	0x0003_FFFF	0x0001_FFFF
Page Size	512-byte	512-byte
Total Page Count	512 pages	256 pages
PGM Unit	1-word (4-byte) Self-PGM	1-word (4-byte) Self-PGM
Erase Unit	512-byte/ 1KB/ 4KB/ bulk	512-byte/ 1KB/ 4KB/ bulk

Figure 28. Code Flash Memory Map (A31G22x Code Flash)



7 Data Flash Memory Controller (DFMC)

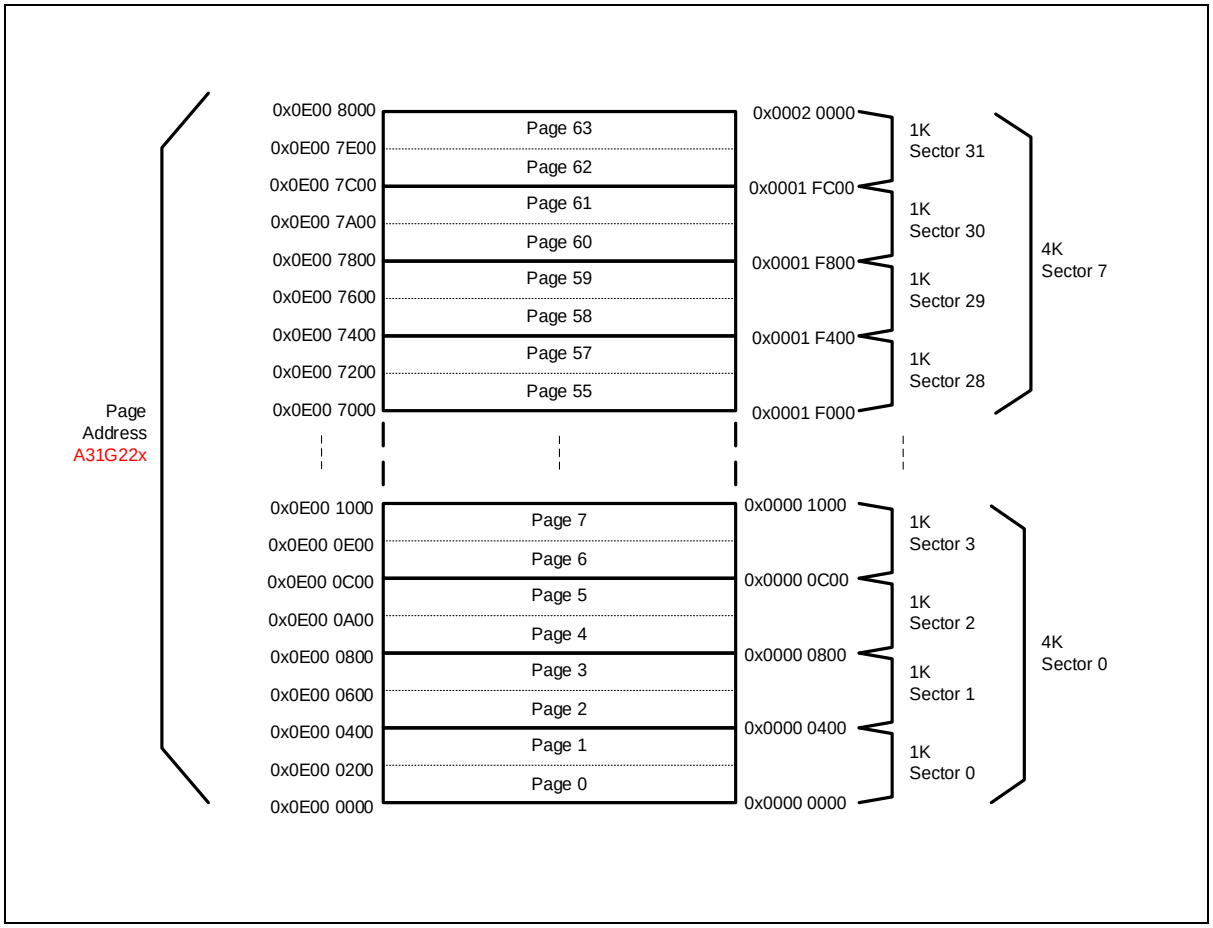
Data Flash Memory Controller is an internal flash memory interface controller, and includes following features as shown below:

- 32KB data flash memory
- Wait, 0-wait to 6-wait (default : 5-wait)
- Read protection support
- Write protection support with 1KB-unit
- A byte-unit(8-bit) program and word-byte(32-bit) unit program support
- Endurance: 100,000 Cycles
- Data Retention: 10 Years

Table 17. Data Flash Memory Controller Features

Item	Description
Size	32KB (A31G22x)
Start Address	0x0E00_0000
End Address	0x0E00_7FFF
Page Size	512-byte
Total Page Count	64 pages
PGM Unit	Byte PGM : 1-byte Word PGM : 1-word (4-byte)
Erase Unit	512-byte/ 1KB/ 4KB/ bulk

Figure 29. Data Flash Memory Map (A31G22x Data Flash)



8 Internal SRAM

The A31G22x has a block of 0-wait on-chip SRAM. The size of SRAM is 20KB.

The SRAM memory area is usually used for data memory and stack memory. Sometimes the code is dumped into the SRAM memory for fast operation or flash erase/program operation.

These SRAM can be accessed as a word (32-bit) alignment. The memory can be addressed at maximum system clock frequency without wait state and thus by both CPU and DMA.

Table 18. Base Address of SRAM

Name	Base address
SRAM	0x2000_0000

9 Direct Memory Access Controller (DMAC)

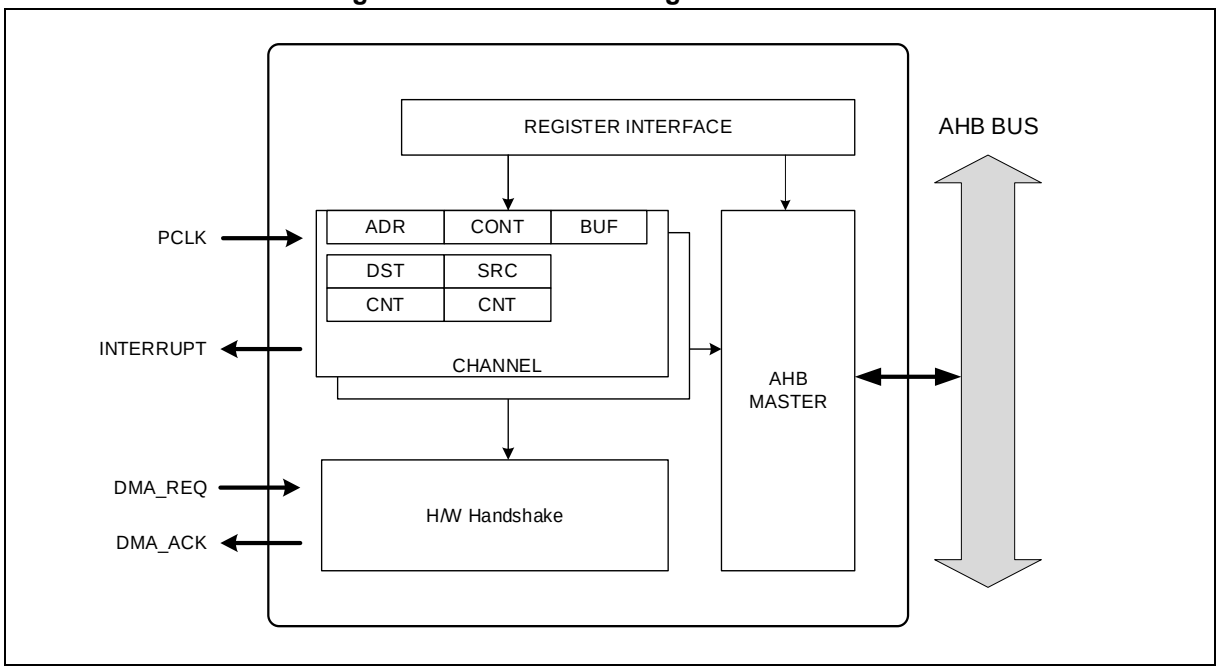
The direct memory access (DMA) controller is used for high-speed data transfers between peripherals and memories. DMA enables quick data transfers having memory to memory copying or moving of data within memory.

- 8 channels
- Single transfer only
- Support 8/16/32-bit data size
- Support multiple buffer with same size
- Interrupt condition is transferred through a peripheral interrupt.
- DMAC peripherals : UARTn Rx/Tx, USART1n Rx/Tx. CRC, SPI2n Rx/Tx, ADC, DAC
- DMAC directions
  - Memory to Peripheral (Tx)
  - Peripheral to Memory (Rx)
  - Peripheral to- Peripheral (P2P)

9.1 Block diagram

In this section, DMAC block diagram is introduced in Figure 30.

Figure 30. DMAC block diagram of A31G22x



10 Watchdog Timer (WDT)

Watchdog timer (WDT) rapidly detects CPU's malfunction such as endless looping caused by noise, and resumes the CPU to the normal state. WDT signal for malfunction detection can be used as either a CPU reset or an interrupt request. When WDT is not being used for malfunction detection, it can be used as a timer generating an interrupt at fixed intervals.

When WDT_CNT value is reached to WDT_WINDR value, a watchdog interrupt can be generated. The underflow time of WDT can be set by WDT_DR. If the underflow occurs, an internal reset is generated. WDT operates on the WDTRC embedded RC oscillator clock.

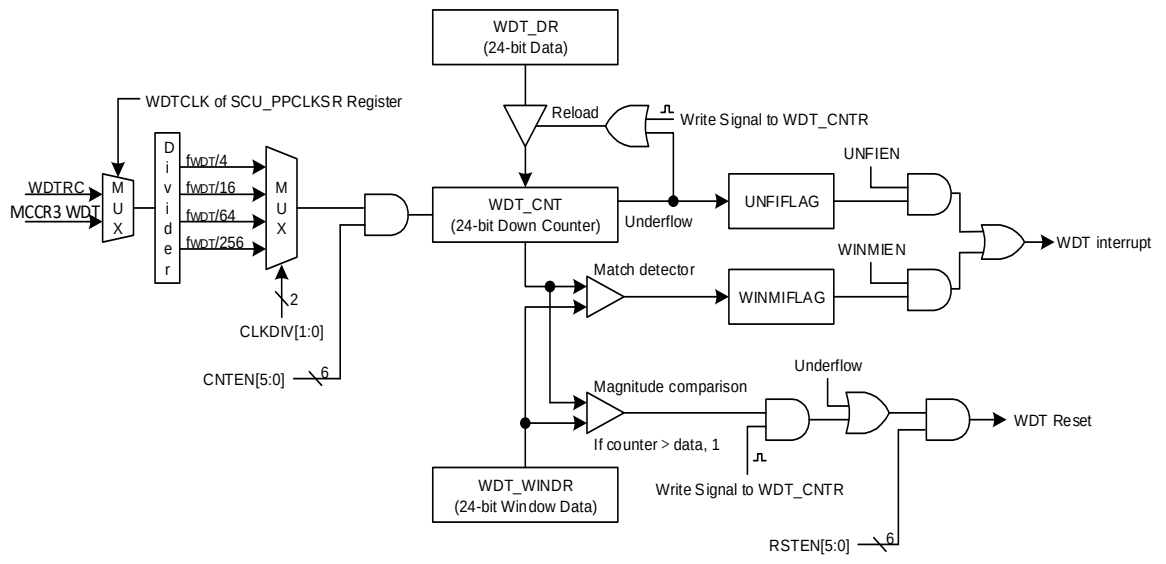
WDT of A31G22x series features followings:

- 24-bit down counter (WDT_CNT)
- Select reset or periodic interrupt
- Count clock selection
- Watchdog overflow output signal
- Counter window function

10.1 WDT block diagram

In this section, WDT block diagram is introduced in Figure 31.

Figure 31. WDT Block Diagram



NOTE: If a reload signal is generated, the WDT_DR value is reloaded to WDT_CNT register after 1 clock delay with the clock which is selected by the CLKDIV bits.

11 Watch Timer (WT)

Watch Timer (WT) has functions for RTC (Real Time Clock) operation. It is generally used for RTC design. WT consists of a clock source select block, a timer counter block, an output select block and watch timer control registers.

Prior to operate WT, a user needs to determine an input clock source and output interval, and to set WTEN as '1' in watch timer control register (WT_CR). It is able to execute simultaneously or individually. To stop or reset WT, clear the WTEN bit in WT_CR register.

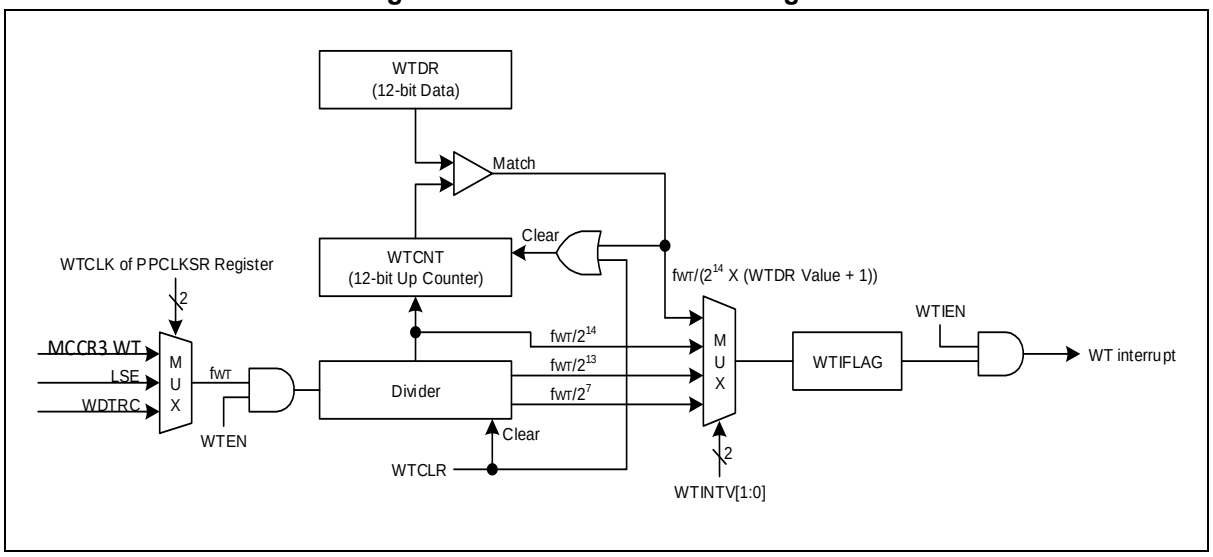
Watch timer counter block corporates a 12-bit up counter. In WT control register, it can control WT clear and set interval value at write time, and it can read 12-bit WT counter value at read time.

11.1 WT block diagram

As shown in Figure 32, WT of A31G22x series has the following blocks:

- 14-bit divider
- 12-bit up-counter

Figure 32. Watch Timer Block Diagram



12 16-bit timer

16-bit timer block comprises 7 channels of 16-bit general purpose timers. Each channel has an independent 16-bit counter and a dedicated prescaler that feeds a counting clock. 16-bit timer supports periodic timer, PWM pulse, one-shot and capture mode. In addition, one more optional free-run timer is provided. Main purpose of 16-bit timer is a periodical tick timer.

16-bit timer of A31G22x series features the followings:

- 16-bit up-counter
- Periodic timer mode
- One-shot timer mode
- PWM pulse mode
- Capture mode
- 12-bit prescaler
- Synchronous start and clear function with TIMER30

Table 19 introduces pins assigned for 16-bit timer.

Table 19. Pin Assignment of 16-bit Timer: External Pins

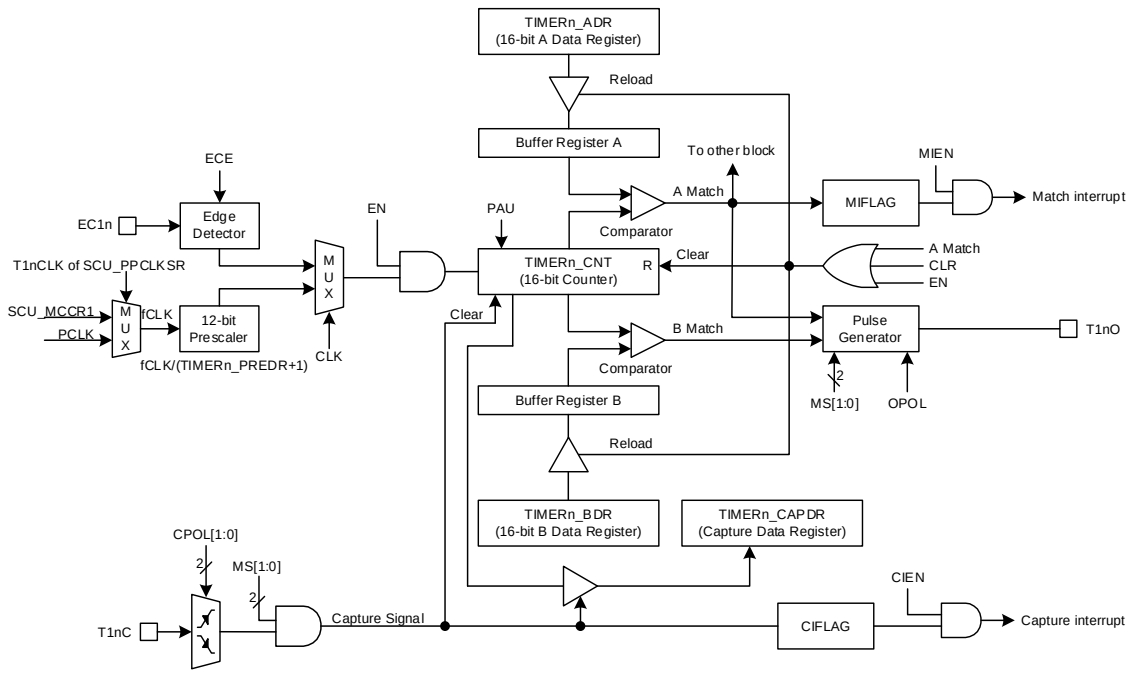
Pin name	Type	Description
EC1n	I	Timer 1n External Clock input
T1nC	I	Timer 1n Capture input
T1nO	O	Timer 1n Output

NOTE: n = 0, 1, 2, 3, 4, 5 and 6

12.1 16-bit timer block diagram

In this section, 16-bit timer is described in a block diagram in Figure 33.

Figure 33. 16-bit Timer 1n Block Diagram (n=0, 1, 2, 3, 4, 5 and 6)



NOTES:

1. The TnEN is automatically cleared to logic “0” after one pulse is generated at a PPG one-shot mode.
2. After the TnEN bit is set, the counting of TIMERn_CNT may be delayed 2 clocks or more.

13 32-bit timer

32-bit timer block comprises 2 channels of 32-bit general purpose timers. TIMER2n channels have an independent 32-bit counter and a dedicated prescaler that feeds a counting clock. 32-bit timer supports periodic timer, PWM pulse, one-shot and capture mode. In addition, one more optional free-run timer is provided. Main purpose of 32-bit timer is a periodical tick timer.

32-bit timer of A31G22x series features the followings:

- 32-bit up-counter
- Periodic timer mode
- One-shot timer mode
- PWM pulse mode
- Capture mode
- 12-bit prescaler

Table 20 introduces pins assigned for 32-bit timer.

Table 20. Pin Assignment of 32-bit Timer: External Pins

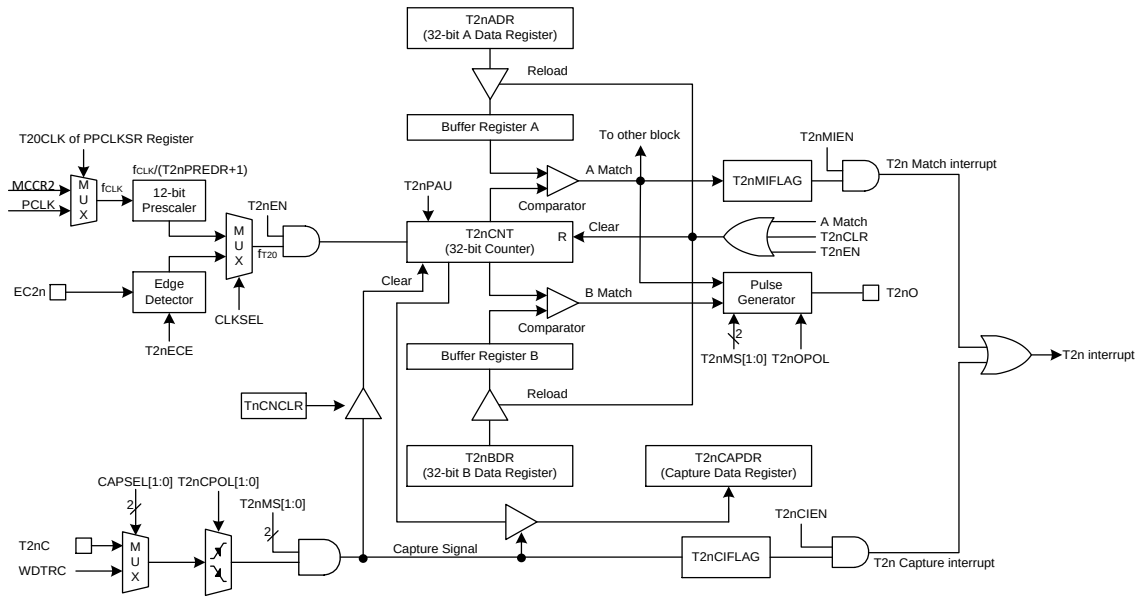
Pin name	Type	Description
EC2n	I	Timer 2n external clock input
T2nC	I	Timer 2n capture input
T2nO	O	Timer 2n Timer/PWM/one-shot output

NOTE: n = 0 and 1

13.1 32-bit timer block diagram

In this section, 32-bit timer is described in a block diagram in Figure 34.

Figure 34. 32-bit Timer Block Diagram



NOTES:

1. The clock source selection for PCLK or SCU_MCCR2 in the SCU_PPCLKSR register only supports TIMER20. (TIMER21 can only be used with PLCK.)
2. The T20EN is automatically cleared to logic “0” after one pulse is generated at a PPG one-shot mode.
3. After the T20EN bit is set, the counting of TIMER20_CNT may be delayed 2 clocks or more.

14 Timer counter 30

Timer counter 30 consists of a multiplexer, a comparator, 16-bit sized timer data registers A/B/C, and many other registers are used for its operation. Main features are listed in the followings:

- 3 phase complementary PWM generators
- 16-bit up/down-counter
- Periodic timer mode
- Back-to-Back mode
- Capture mode
- 12-bit prescaler

Table 21 introduces pins assigned for the timer counter 30.

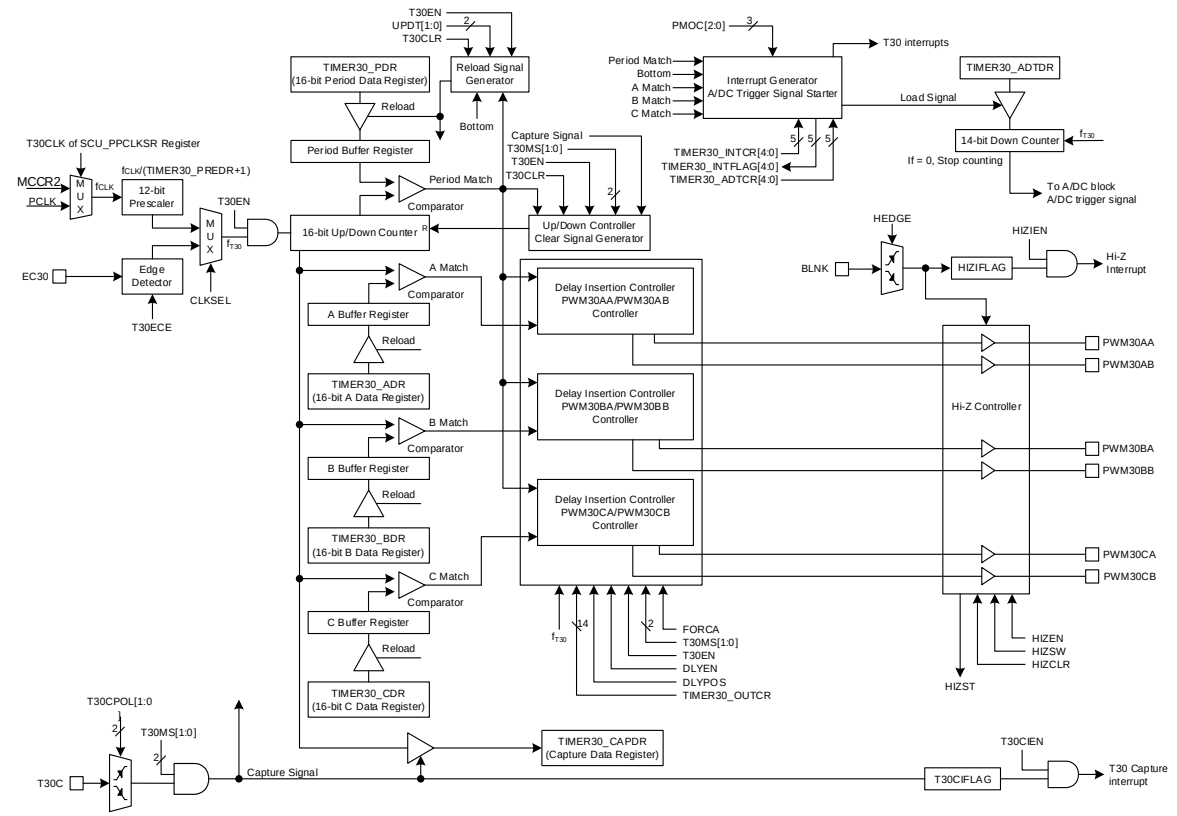
Table 21. Pin Assignment of Timer Counter 30: External Pins

Pin name	Type	Description
EC30	I	External clock input of TIMER30
T30CAP	I	Capture input of TIMER30
BLNK	I	External sync signal input of TIMER30
PWM30AA	O	PWM output
PWM30AB	O	PWM output
PWM30BA	O	PWM output
PWM30BB	O	PWM output
PWM30CA	O	PWM output
PWM30CB	O	PWM output

14.1 Timer counter 30 block diagram

In this section, timer counter 30 is introduced in a block diagram.

Figure 35. Timer Counter 30 Block Diagram



NOTES:

1. The Period/A/B/C match interrupts except for Bottom can occur in the interval mode.
2. The Period match interrupt only can occur in the capture mode.
   A. The 16-bit up/down counter in the capture mode is cleared to “0000H” after the counter value is loaded to the TIMER30_CAPDR register at valid edge.
   B. The HIZSW (high-impedance output software setting) bit can be used for debugging mode. That is, All TIMER30 PWM outputs can be high-impedance state with setting the HIZSW bit to ‘1’ by the UI of debugger.
   C. After the EN bit is set, the counting of TIMER30_CNT may be delayed 2 clocks or more.

15 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

Universal Synchronous and Asynchronous serial Receiver and Transmitter (USART) is a highly flexible serial communication device. The main features are listed below:

- Full Duplex Operation. (Independent Serial Receive and Transmit Registers)
- Asynchronous or Synchronous Operation.
- Baud Rate Generator.
- Supports Serial Frames with 5,6,7,8, or 9 Data bits and 1 or 2 Stop bits.
- Odd or Even Parity Generation and Parity Check are Supported by Hardware.
- Data Over-Run Detection.
- Framing Error Detection.
- Three Separate Interrupts on TX Completion, TX Data Register Empty and RX Completion.
- Double Speed Asynchronous communication mode.

Additional features are:

- 0% Error Baud Rate by floating point count register.
- Supports receive time out interrupt.
- Supports direct memory access and interrupt.

Table 22 introduces pins assigned for the USART.

Table 22. Pin Assignment of USART: External Pins

Pin name	Type	Description
TXDn	O	UART Channel n transmit output
RXDn	I	UART Channel n receive input
SSn	I/O	SPIn Slave select input / output
SCKn	I/O	SPIn Serial clock input / output
MOSIn	I/O	SPIn Serial data (Master output, Slave input)
MISOn	I/O	SPIn Serial data (Master input, Slave output)

NOTE: n = 10, 11, 12 and 13

15.1 USART block diagram

In this section, USART and SPIN are introduced in block diagrams.

Figure 36. USART Block Diagram (n = 10, 11, 12, and 13)

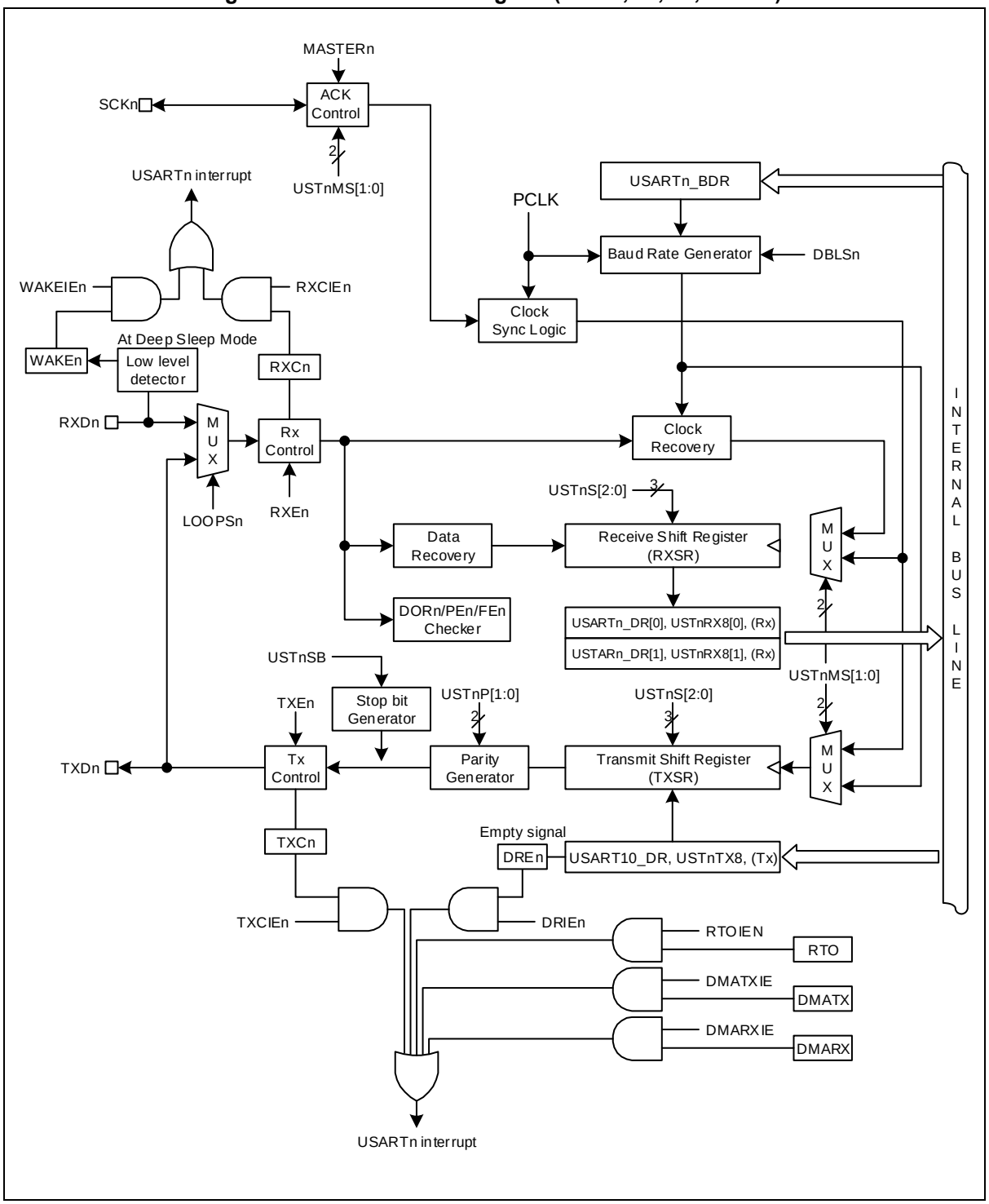
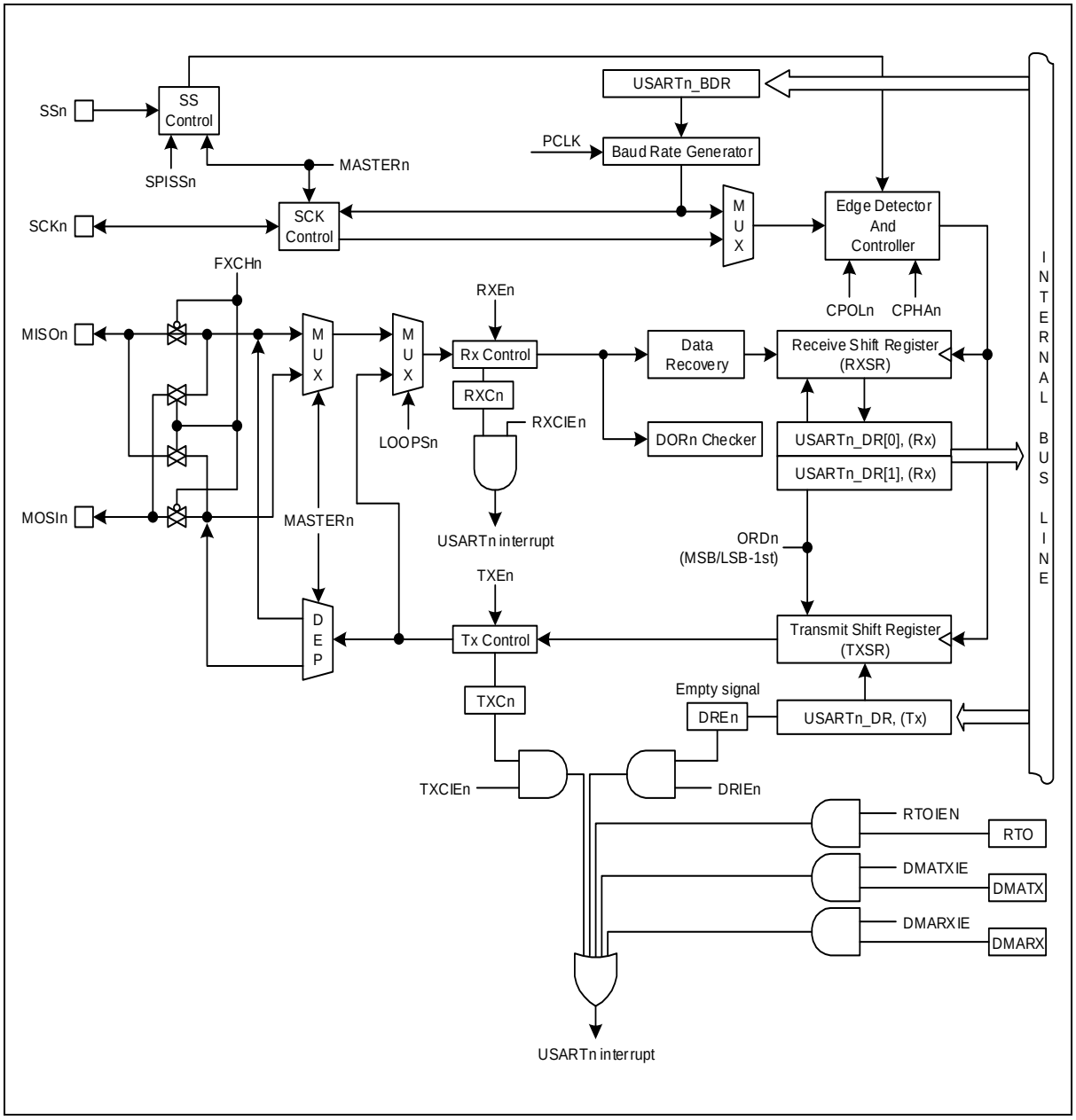


Figure 37. SPIN Block Diagram (n = 10, 11, 12, and 13)



16 Universal Asynchronous Receiver/Transmitter (UART)

2-channel UART (Universal Asynchronous Receiver/Transmitter) modules are provided. UART operation status including error status can be read from status register. The prescaler which generates proper baud rate, is exist for each UART channel. The prescaler can divide the UART clock source which is PCLK, from 1 to 65535. And baud rate generation is by clock which internally divided by 16 of the prescaled clock and 8-bit precision clock tuning function.

Programmable interrupt generation function will help to control the communication via UART channel

- Standard asynchronous control bit (start, stop, and parity) configurable
- Programmable serial communication
- 5, 6, 7 or 8 data bit transfer
- Even, odd, or no-parity bit insertion and detection
- 1, 1.5 or 2 stop bit-insertion and detection
- 16-bit baud rate generation with 8-bit fraction control
- Hardware inter-frame delay function
- Stop bit error detection
- Detail status register

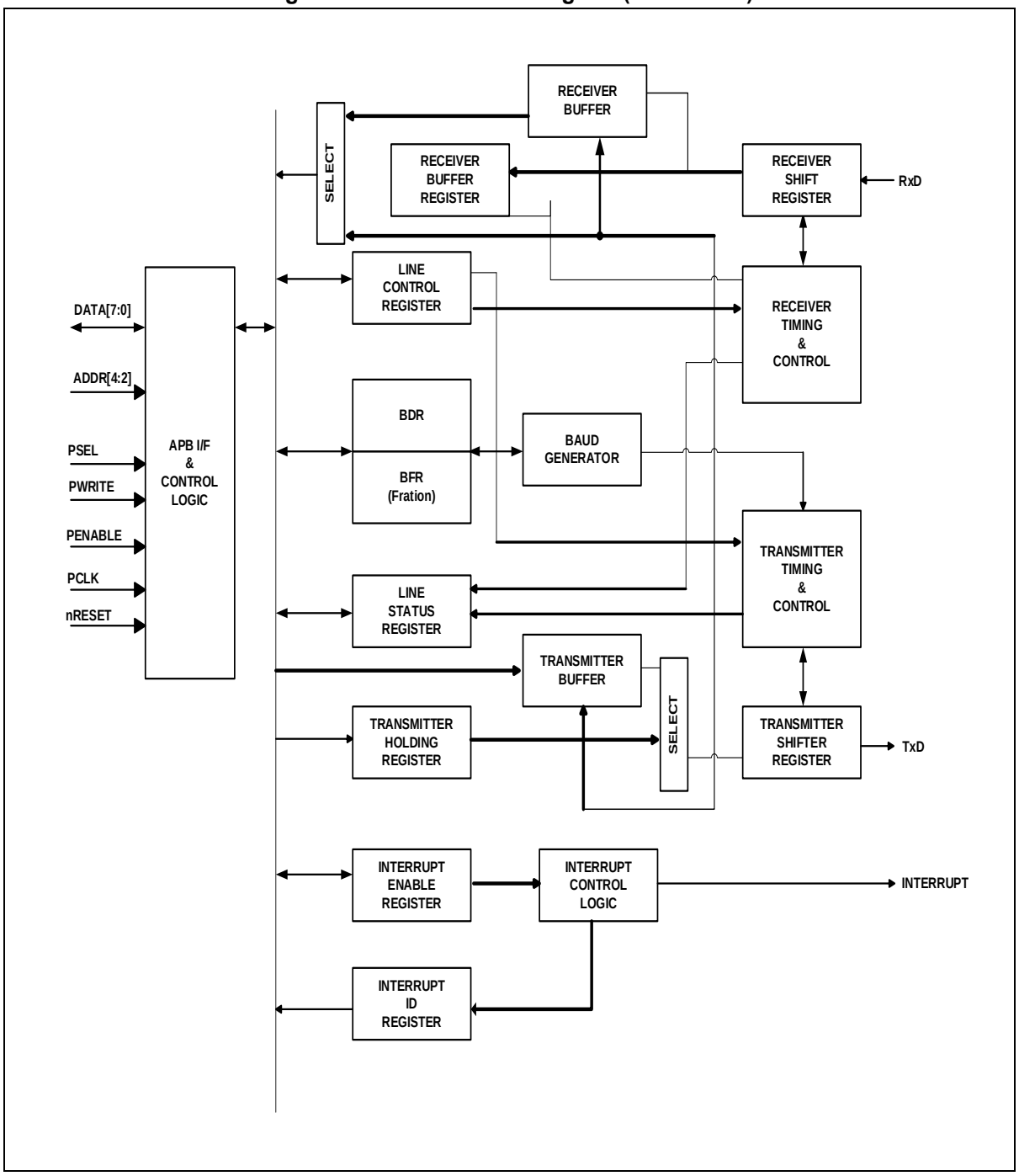
Table 23 introduces pins assigned for the UART channels.

Table 23. Pin Assignment of UART: External Pins

Pin name	Type	Description	A31G226MNN A31G226MLN A31G224MMN A31G224MLN (LQFP-80)	A31G226RMN A31G226RLN A31G224RMN A31G224RLN (LQFP-64)	A31G226CLN A31G224CLN (LQFP-48)
TXD0	O	UART Channel 0 transmit output	O	O	O
RXD1	I	UART Channel 0 receive input	O	O	O
TXD1	O	UART Channel 1 transmit output	O	O	O
RXD1	I	UART Channel 1 receive input	O	O	O

16.1 UART block diagram

Figure 38. UARTn Block Diagram (n = 0 and 1)



17 Serial Peripheral Interface (SPI)

A channel serial interface is provided for synchronous serial communications with external peripherals. SPI block support both of master and slave mode. Four signals will be used for SPI communication such as SS, SCK, MOSI, and MISO.

SPI of A31G22x series features the followings:

- Master or Slave operation.
- Programmable clock polarity and phase.
- 8, 9, 16, 17-bit wide transmit/receive register.
- 8, 9, 16, 17-bit wide data frame.
- Loop-back mode.
- Programmable start, burst, and stop delay time.
- DMA transfer operation.

Table 24 introduces pins assigned for SPI.

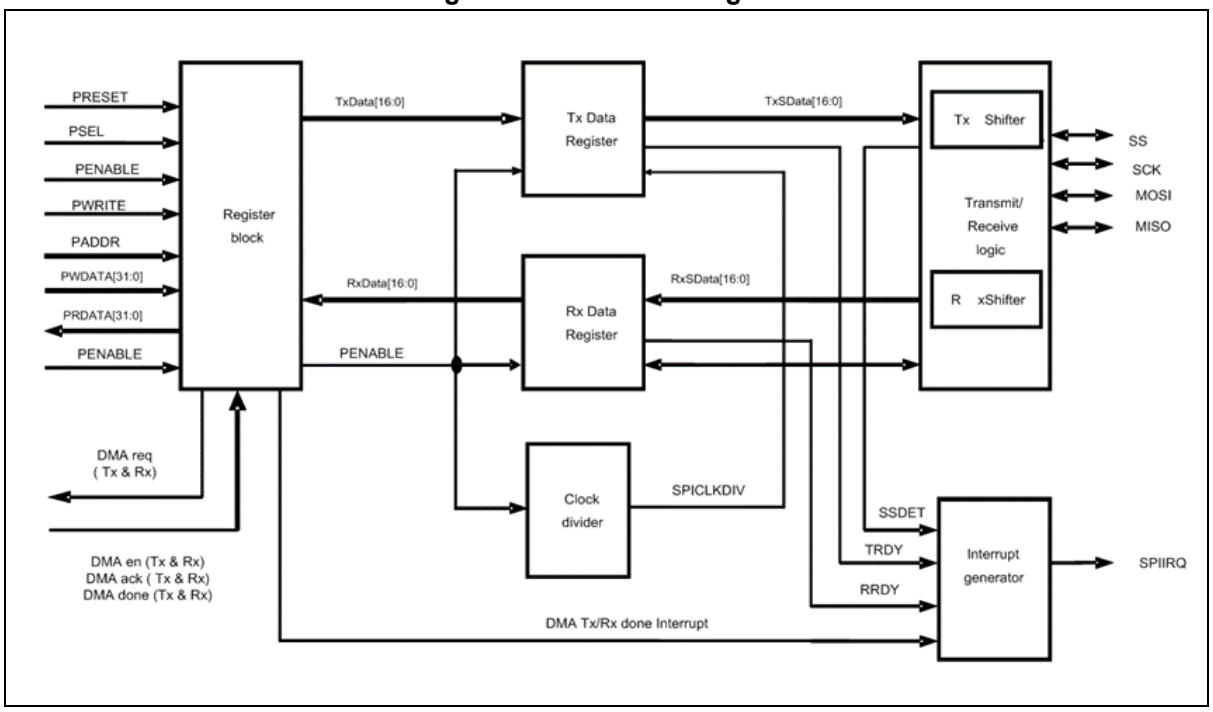
Table 24. Pin Assignment of SPI: External Pins

Pin name	Type	Description	A31G226MNN A31G226MLN A31G224MMN A31G224MLN (LQFP-80)	A31G226RMN A31G226RLN A31G224RMN A31G224RLN (LQFP-64)	A31G226CLN A31G224CLN (LQFP-48)
SS20	I/O	Slave Select signal of SPI0	O	O	O
SCK20	I/O	Serial Clock signal of SPI0	O	O	O
MOSI20	I/O	Master-Out Slave-In Data signal of SPI0	O	O	O
MISO20	I/O	Master-In Slave-Out Data signal of SPI0	O	O	O
SS21	I/O	Slave Select signal of SPI1	O	O	O
SCK21	I/O	Serial Clock signal of SPI1	O	O	O
MOSI21	I/O	Master-Out Slave-In Data signal of SPI1	O	O	O
MISO21	I/O	Master-In Slave-Out Data signal of SPI1	O	O	O

17.1 SPI block diagram

In this section, SPI is described in a block diagram in Figure 39.

Figure 39. SPI Block Diagram



18 I2C interface

I2C is one of industrial standard serial communication protocols, and which uses 2 bus lines such as Serial Data Line (SDAn) and Serial Clock Line (SCLn) to exchange data. Because both SDAn and SCLn lines are open-drain output, each line needs pull-up resistor respectively.

I2C features the followings (n = 0, 1 and 2):

- Compatible with I2C bus standard.
- Multi-master operation.
- Up to 400kHz data transfer read speed.
- 7-bit address.
- Support two slave address.
- Both master and slave operation.
- Bus busy detection

Introduces pins assigned for I2C interface.

Table 25. Pin Assignment of I2C: External Pins

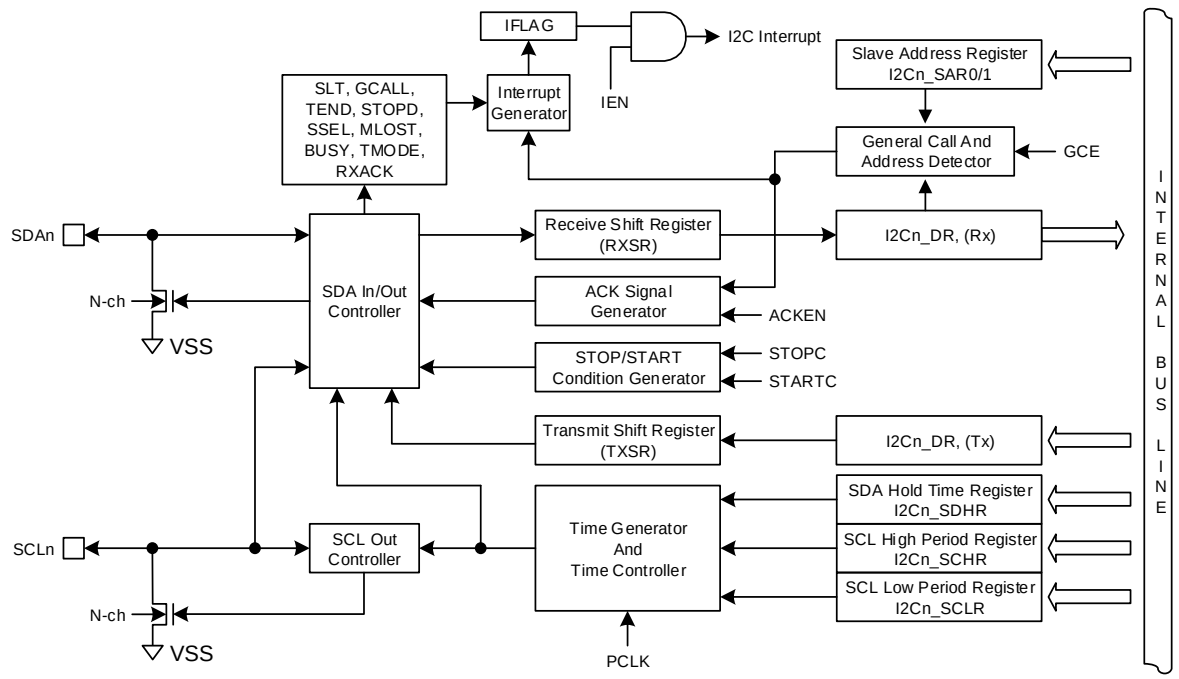
Pin name	Type	Description	A31G226MNN A31G226MLN A31G224MMN A31G224MLN (LQFP-80)	A31G226RMN A31G226RLN A31G224RMN A31G224RLN (LQFP-64)	A31G226CLN A31G224CLN (LQFP-48)
SCL0	I/O	I2C channel 0 Serial clock bus line (open-drain)	O	O	O
SDA0	I/O	I2C channel 0 Serial data bus line (open-drain)	O	O	O
SCL1	I/O	I2C channel 1 Serial clock bus line (open-drain)	O	O	O
SDA1	I/O	I2C channel 1 Serial data bus line (open-drain)	O	O	O
SCL2	I/O	I2C channel 2 Serial clock bus line (open-drain)	O	O	-
SDA2	I/O	I2C channel 2 Serial data bus line (open-drain)	O	O	-

NOTE: n = 0, 1 and 2

18.1 I2C block diagram

In this section, I2C interface block is described in a block diagram.

Figure 40. I2C Block Diagram



NOTE: When the corresponding port of I2C is a sub-function for SCL/SDA pin, the SCL/SDA pins are automatically set to the N-channel open-drain outputs and the input latch is read in the case of reading the pins. The corresponding pull-up resistor is determined by the control register.

19 12-bit ADC

ADC block of A31G22x series consists of an independent ADC unit featuring the followings:

- Max. 18 Channels Analog Input with 12-bit Resolution.
  - 80-pin: 18 channels
  - 64-pin: 18 channels
  - 48-pin: 14 channels
- Single mode and continuous conversion mode
- Maximum 8 sequential conversion support
- Software trigger support
- Two internal trigger source (TIMER1n and TIMER30) Support
- Adjustable sample and hold time
- Maximum 1MHz conversion rate (Max. 1Msps)
- ADC Main Clock Frequency: Max. 16MHz
- Operating Power Supply: AVDD : 2.1V ~ 5.5V
- Analog Input Range: 0.0V ~ AVDD

Table 26 introduces pins assigned for ADC.

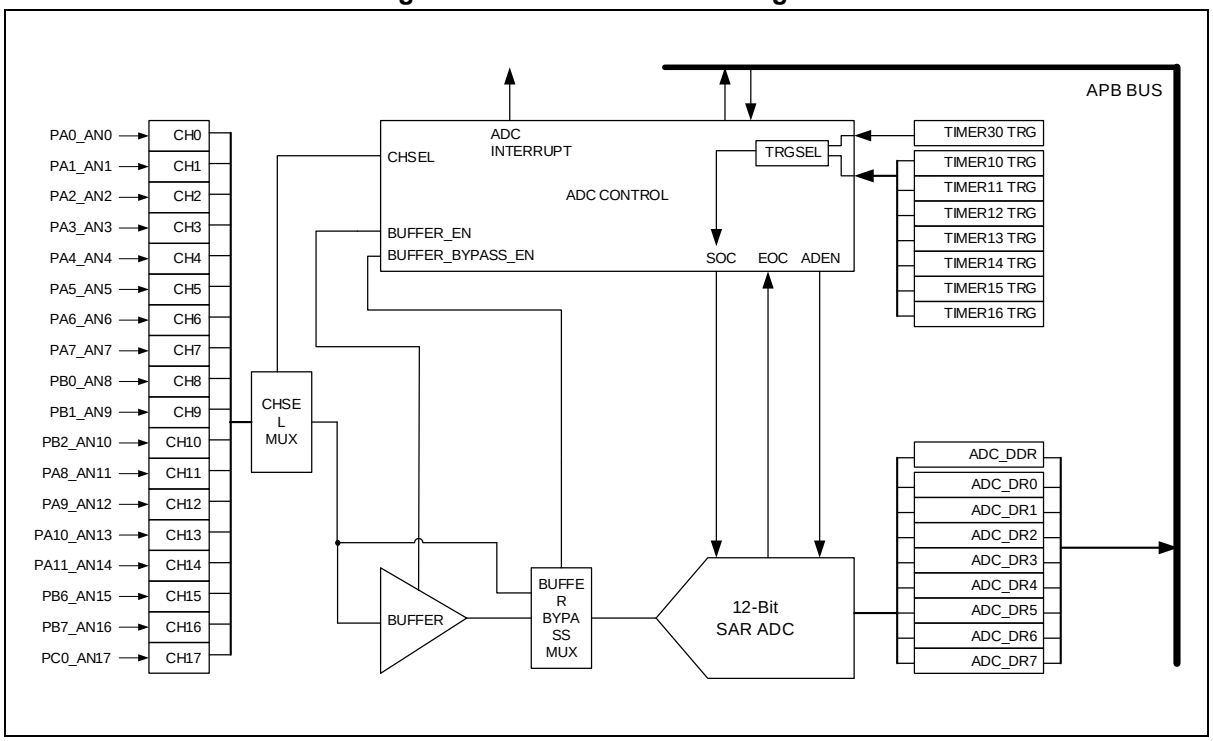
Table 26. Pin Assignment of ADC: External Signal

Pin name	Type	Description	A31G226MNN A31G226MLN A31G224MMN A31G224MLN (LQFP-80)	A31G226RMN A31G226RLN A31G224RMN A31G224RLN (LQFP-64)	A31G226CLN A31G224CLN (LQFP-48)
VDD	P	Analog Power (Reference Voltage)	O	O	O
VSS	P	Analog GND	O	O	O
AN0	A	ADC Input 0	O	O	O
AN1	A	ADC Input 1	O	O	O
AN2	A	ADC Input 2	O	O	O
AN3	A	ADC Input 3	O	O	O
AN4	A	ADC Input 4	O	O	O
AN5	A	ADC Input 5	O	O	O
AN6	A	ADC Input 6	O	O	O
AN7	A	ADC Input 7	O	O	O
AN8	A	ADC Input 8	O	O	O
AN9	A	ADC Input 9	O	O	O
AN10	A	ADC Input 10	O	O	O
AN11	A	ADC Input 11	O	O	Not Used
AN12	A	ADC Input 12	O	O	Not Used
AN13	A	ADC Input 13	O	O	Not Used
AN14	A	ADC Input 14	O	O	Not Used
AN15	A	ADC Input 15	O	O	O
AN16	A	ADC Input 16	O	O	O
AN17	A	ADC Input 17	O	O	O

19.1 12-bit ADC block diagram

In this section, 12-bit ADC is described in a block diagram in Figure 41.

Figure 41. 12-bit ADC Block Diagram



20 12-bit DAC

Digital-to-analog (D/A) converter uses successive approximation logic to convert 12-bit digital value to an analog output level.

DAC module has six registers which are the DAC control register (DACCR), DAC data high register (DACDRH), DAC data low register (DACDRL), DAC buffer high register (DACBRH), DAC buffer low register (DACBRL) and programmable gain selection register (PGSR).

Table 27 introduces pins assigned for DAC.

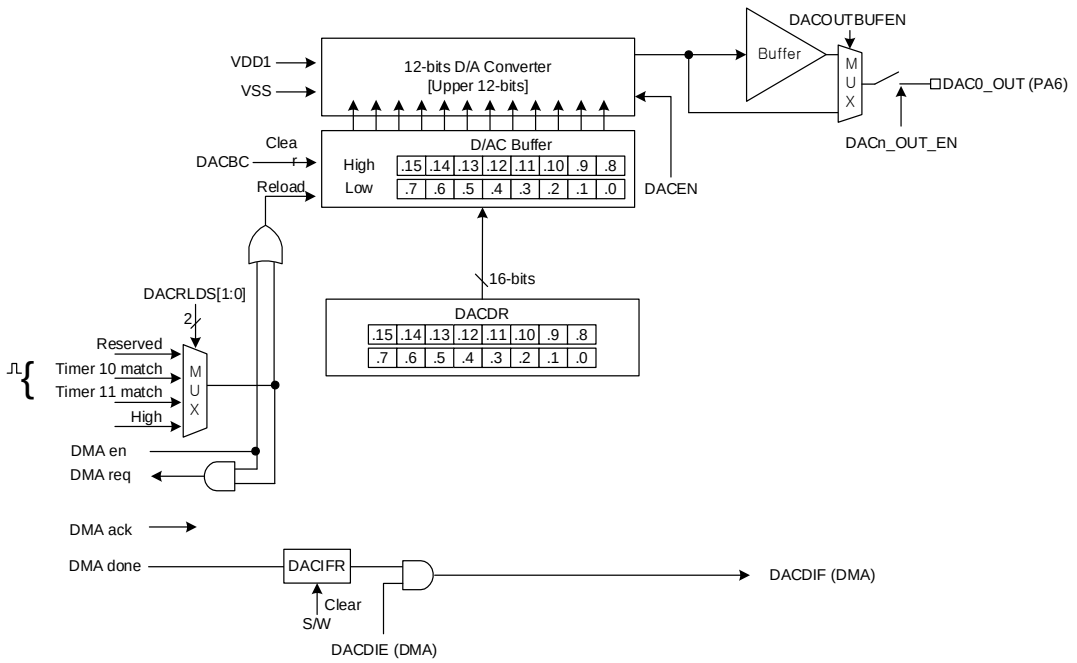
Table 27. Pin Assignment of DAC: External Signal

Pin name	Type	Description	A31G226MNN A31G226MLN A31G224MMN A31G224MLN (LQFP-80)	A31G226RMN A31G226RLN A31G224RMN A31G224RLN (LQFP-64)	A31G226CLN A31G224CLN (LQFP-48)
DAO	A	DAC output (Referenced VDD)	O	O	O

20.1 12-bit DAC block diagram and analog power pin

In Figure 42, 12-bit DAC is described in a block diagram.

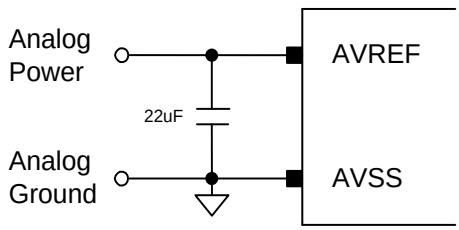
Figure 42. 12-bit DAC Block Diagram



NOTES:

1. Gain controller converts data in the sequence listed below:
   A. Get the DAC_DR[15:0] value.
   B. Adjust the data by selection gain.
   C. Write the data to the D/AC buffer.
2. DAC interface block doesn't work when DACRLDS bits of the DAC_CR register are set to "00b".

Figure 43. Analog Power (AVREF) Pin with a Capacitor



21 Comparator

Comparator of A31G22x series compares one analogue voltage level with external reference voltage, or internal reference voltage output voltage.

The comparator features the followings:

- 2 Comparators
- Internal BGR reference for comparator
- Comparator output de-bounce function
- Level and edge interrupt mode support for comparator
- DAC outputs is used as comparator input (Hidden)

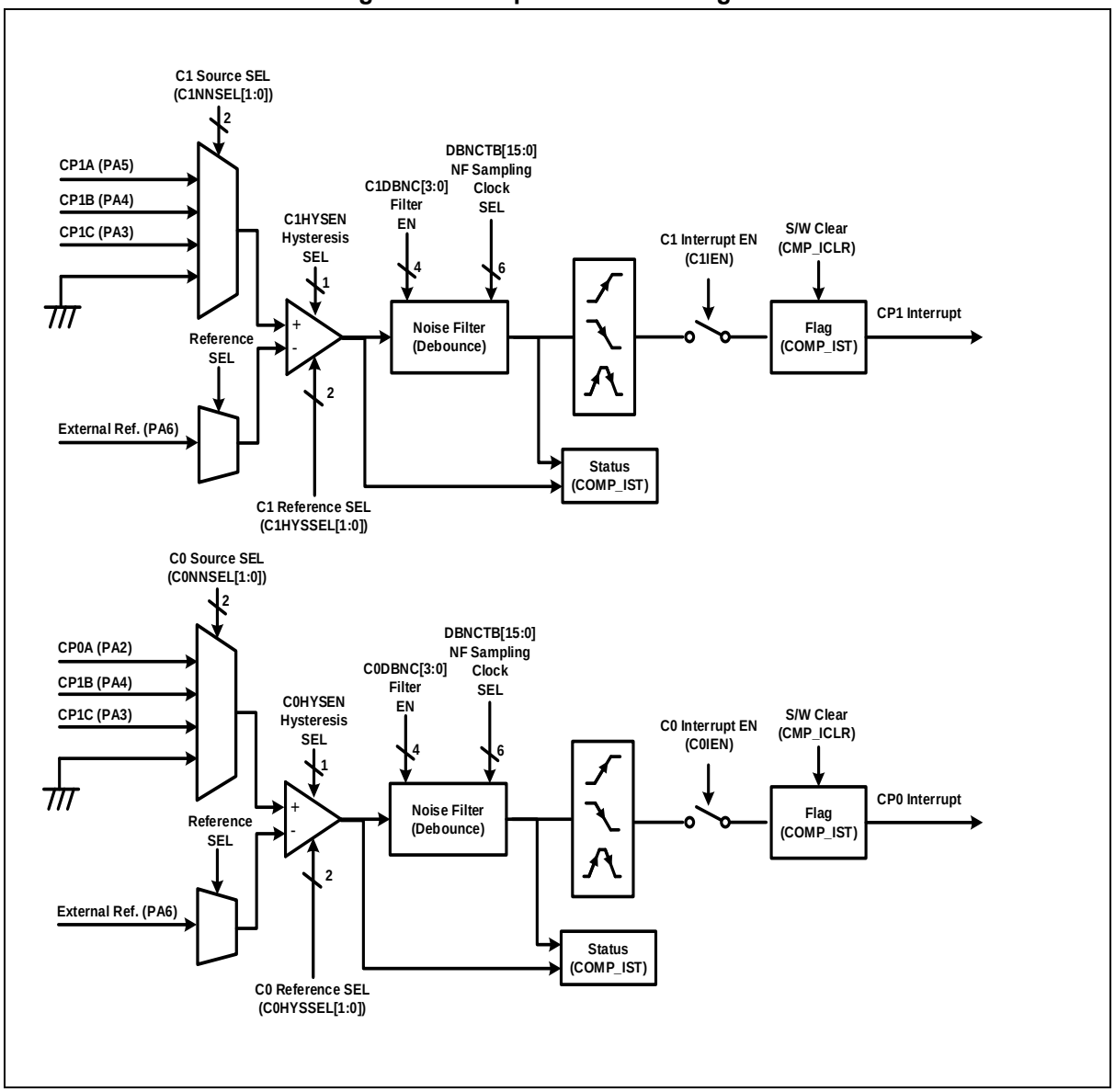
Table 28 introduces pins assigned for Comparator.

Table 28. Pin Assignment of Comparator: External Signal

Pin name	Type	Description	A31G226MNN A31G226MLN A31G224MMN A31G224MLN (LQFP-80)	A31G226RMN A31G226RLN A31G224RMN A31G224RLN (LQFP-64)	A31G226CLN A31G224CLN (LQFP-48)
CP0A	A	Comparator 0 input A	O	O	O
CP1A	A	Comparator 1 input A	O	O	O
CP1B	A	Comparator 0,1 input B	O	O	O
CP1C	A	Comparator 0,1 input C	O	O	O
CREF0	A	Comparator 0 reference input	O	O	O
CREF1	A	Comparator 1 reference input	O	O	O

21.1 Comparator block diagram

Figure 44. Comparator Block Diagram



22 LCD driver

The LCD driver is controlled by the LCD control register (LCD_CR) and LCD driver bias and contrast control register (LCD_BCCR). The LCLK[1:0] determines the frequency of COM signal scanning of each segment output. A RESET clears the LCD control register LCD_CR and LCD_BCCR values to logic ‘0’.

The LCD display can continue operating during IDLE and STOP modes.

The clock and duty for LCD driver is automatically initialized by hardware, whenever LCD_CR register data value is rewritten. So, don’t rewrite LCD_CR frequently.

LCD channel configuration (COM x SEG):

- 80-pin: 8 x 37 or 3 x 42
- 64-pin: 8 x 29 or 3 x 34
- 48-pin: 8 x 21 or 3 x 26

Table 29 introduces pins assigned for LCD Driver.

Table 29. Pin Assignment of LCD Driver: External Signal

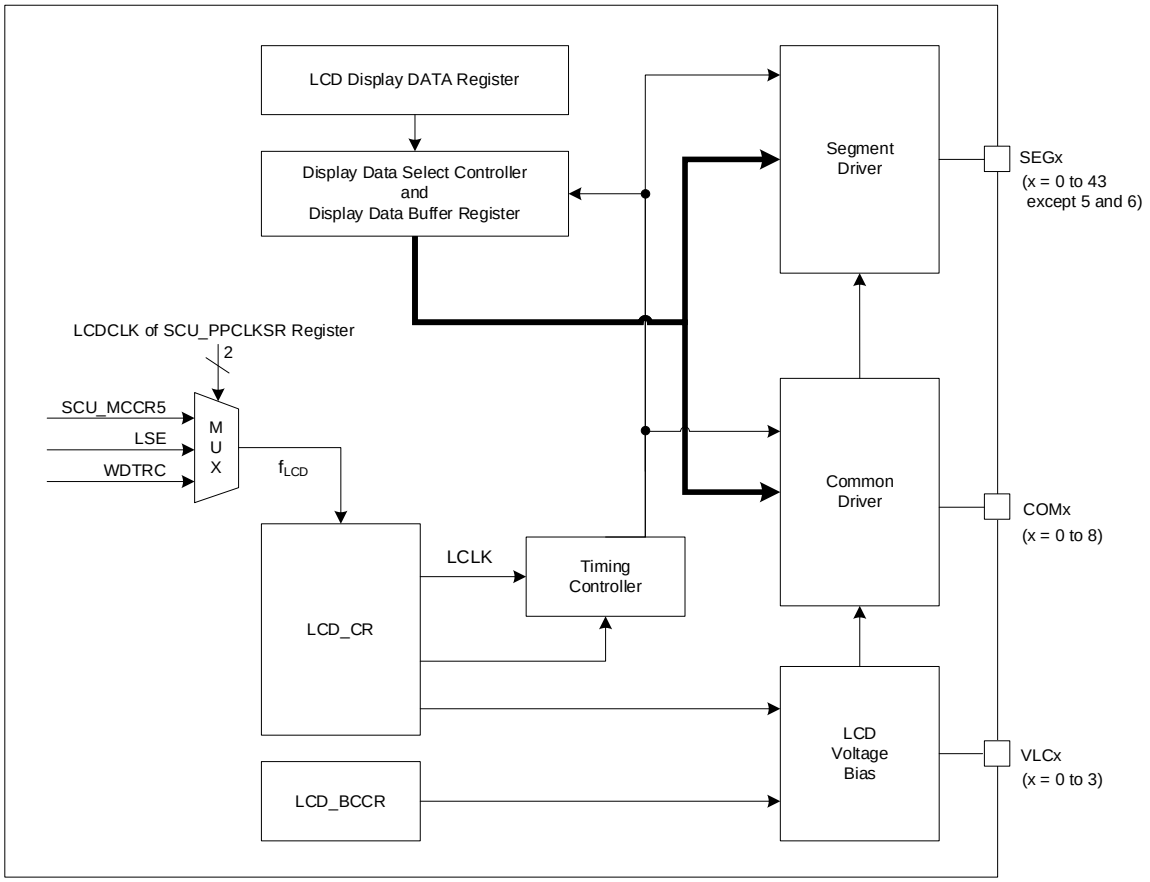
Pin name	Type	Description	A31G226MNN A31G226MLN A31G224MMN A31G224MLN (LQFP-80)	A31G226RMN A31G226RLN A31G224RMN A31G224RLN (LQFP-64)	A31G226CLN A31G224CLN (LQFP-48)
VLCx	A	LCD External Bias voltage input (x = 0 to 3)	O	O	X
COMx	O	LCD common signal outputs (x = 0 to 7)	O (Up to 8)	O (Up to 8)	O (Up to 8)
SEGx	O	LCD segment signal outputs (x = 0 to 43, except 5, 6*)	O (Up to 42)	O (Up to 34)	O (Up to 26)

***NOTE**: SEG5 and SEG6 pins in LQFP-80 package are not available. Please refer to 1.1 and 1.2 in A31G22x Errata sheet.

22.1 LCD Driver block diagram

Figure 45 describes the LCD block diagram.

Figure 45. LCD Driver Block Diagram



NOTES:

1. PE14 (SEG5) and PE15 (SEG6) pins do not support SEG alternative function. Also, LCD_DR5 and LCD_DR6 are not mapped for SEG control.
2. The pull-up resistors for PC1 (SEG23) and PC2 (SEG24) are initially enabled.

23 Cyclic Redundancy Check (CRC) Calculation Unit

Cyclic redundancy check (CRC) generator is used to get a 16-bit CRC code from Flash ROM and a generator polynomial. Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the functional safety standards, they offer a means of verifying the Flash memory integrity. CRC generator helps compute a signature of the software during runtime, to be compared with a reference signature.

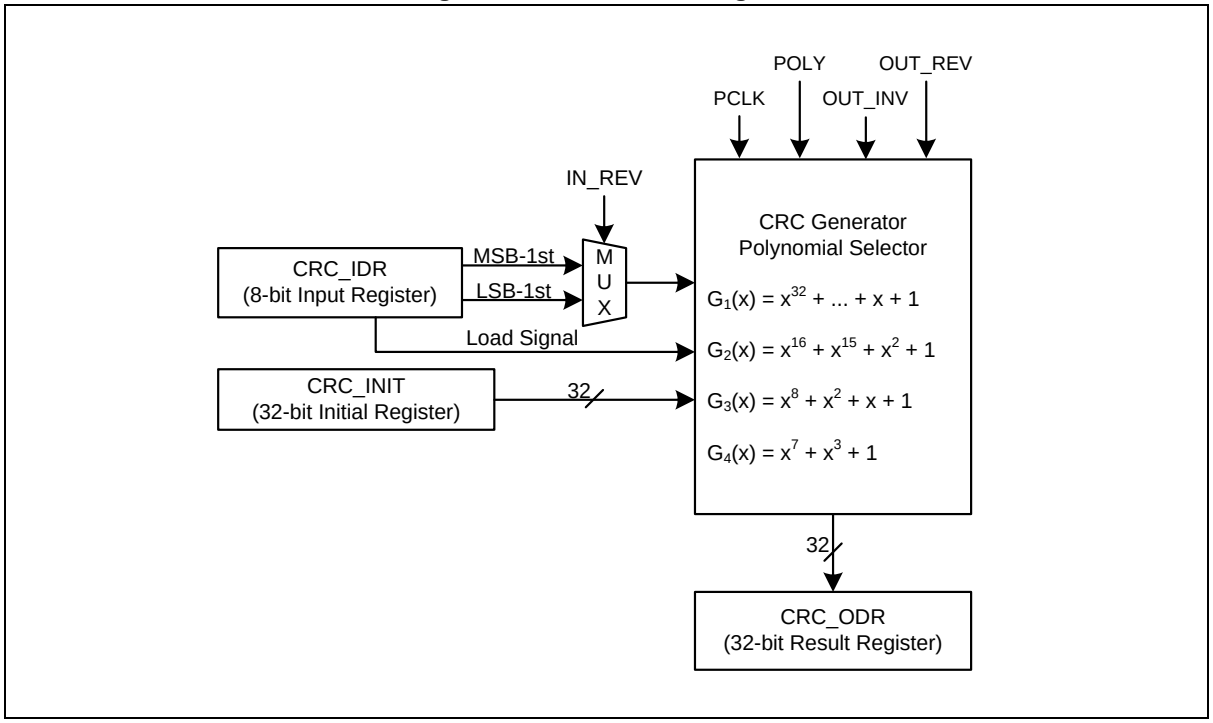
CRC generator of A31G22x series features the followings:

- Auto CRC (DMA) and User CRC Mode.
- Polynomial:
  - CRC-32 ($G_0(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$)
  - CRC-16 ($G_1(x) = x^{16} + x^{15} + x^2 + 1$),
  - CRC-8 ($G_2(x) = x^8 + x^2 + x + 1$)
  - CRC-7 ($G_3(x) = x^7 + x^3 + 1$)

23.1 CRC block diagram

Figure 46 describes the CRC block diagram.

Figure 46. CRC Block Diagram



24 Temp sensor

Temp sensor is to use the internal oscillator LSITS by default, which has a large temperature variation. The temperature-dependent LSITS frequency can be calculated based on a precisely trimmed internal oscillator or an external clock.

Reference clock and sense clock of the temp sensor can be changed by configuring TS_CR register. When selecting the clock, frequency of the reference clock must be faster than the sense clock frequency. In SCU, each clock must be activated by configuring corresponding register.

If value of RCCV using reference clock matches the RCCV in TS_RCCNT register set by the user, a match flag is generated and frequency of the sense clock is calculated by reading the value of SCCV in TS_SCCNT register at this time. Match flags can be used as interrupt sources.

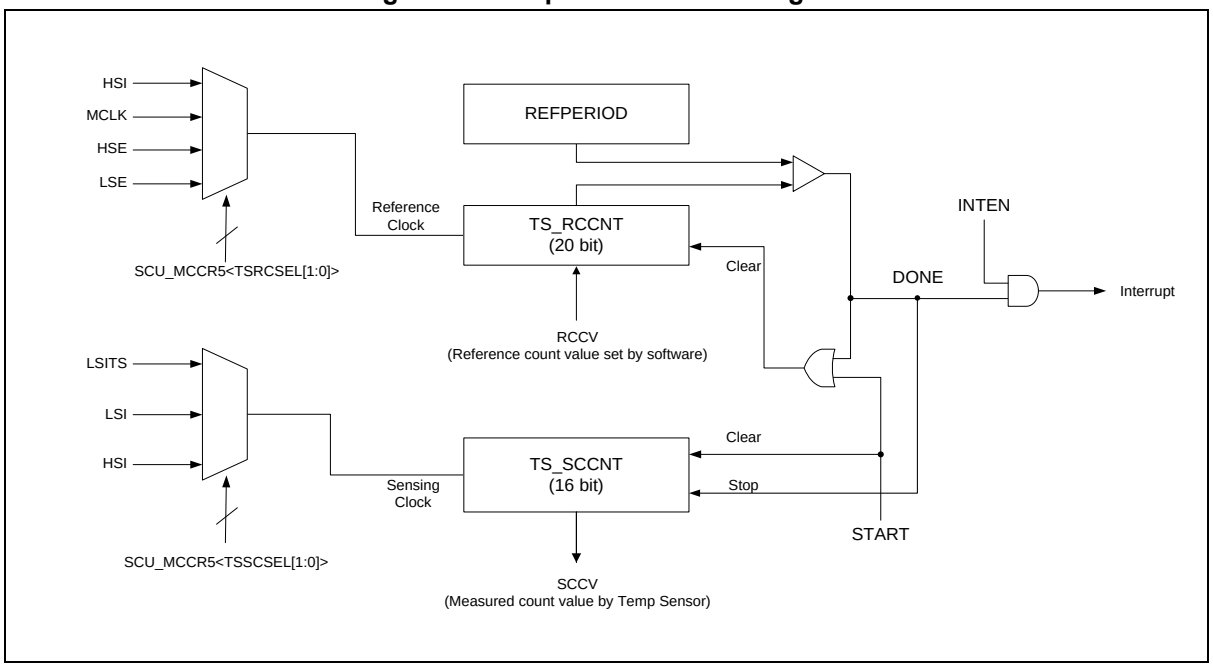
Glossary for this chapter

- HSI: HSI clock set by SCU_CSCR
- MCLK: System clock set by SCU_SCCR
- LSE: External sub oscillator
- LSITS: Internal temp sense oscillator
- LSI: Internal 500KHz oscillator

NOTE: If the TS clock source to be used in the operation of TS_SCCNT is selected as LSI or HSI instead of LSITS, the temperature sensor becomes a normal timer counter operation. Therefore, it is recommended to use a clock source with LSITS for temperature measurement.

24.1 Temp sensor block diagram

Figure 47. Temp Sensor Block Diagram



25 Electrical characteristics

25.1 Absolute maximum ratings

Absolute maximum ratings are limiting values of operating and environmental conditions which should not be exceeded under the worst possible conditions.

Table 30. Absolute maximum rating

Parameter	Symbol	Ratings	Unit	Remark
Supply Voltage	V_{DD}	-0.3 – +6.5	V	—
Normal Pin	V_I	-0.3 – VDD+0.3	V	Voltage on any pin with respect to V_{SS}
	V_O	-0.3 – VDD+0.3	V	
	I_{OH}	-20	mA	Maximum output current sourced by per I/O pin
	ΣI_{OH}	-100	mA	Total output current sourced by sum of all I/Os
	I_{OL}	25	mA	Maximum output current sunk by per I/O pin except I_{OL7}*.
	ΣI_{OL}	210	mA	Total output current sunk by sum of all I/Os
Total Power Dissipation	T_P	300	mW	—
Storage Temperature	T_{STG}	-55 – +125	℃	—

NOTE: I_{OL7} is output low level current specification when high current output function is enabled. Refer 25.13.2

25.2 Recommended operating conditions

Table 31. Recommended Operating Condition

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	Core and Peripherals	1.8	—	5.5	V
		CMP	2.0	—	5.5	V
		ADC	2.1	—	5.5	V
		DAC, LCD	2.7	—	5.5	V
		HSE	1.8	—	5.5	V
		LSE	2.7	—	5.5	V
Operating Frequency	f_{OP}	PLL	1	—	48	MHz
		HSE	1	—	16	MHz
		LSE	—	32.768	—	KHz
		HSI	31.52	32.00	32.48	MHz
		LSI	400	500	600	KHz
Operating Temperature	T_{OP}	Top	-40	+25	+105	℃

25.3 POR (Power-on Reset) characteristics

Table 32. POR Electrical Characteristics

The specifications of the parameters are guaranteed by design.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Current	I_{DD}	–	-	0.5	-	uA
POR Set Level	V_{SET}	–	1.05	1.20	1.35	V
POR Reset Level	V_{RESET}	–	1.00	1.10	1.20	V
Supply Rising Rate	T_{rVDD}		-	-	10	V/ms
Supply Falling Rate	T_{fVDD}		-	-	10	V/ms

25.4 LVR (Low Voltage Reset) characteristics

Table 33. Operating Condition of Low Voltage Reset

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating Temperature	T_A	-40	25	105	℃

Table 34. Low Voltage Reset Characteristics

The specifications of the parameters are guaranteed by design.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating voltage	V_{DD}	–	0.8	5.0	5.5	V
LVR detection level	V_{FLVR}	Falling detection voltage	1.45	1.56	1.67	V
			1.58	1.70	1.82	
			1.66	1.79	1.92	
			1.78	1.91	2.04	
			1.86	2.00	2.14	
			1.98	2.13	2.28	
			2.15	2.31	2.47	
			2.31	2.48	2.65	
			2.49	2.68	2.87	
			2.83	3.05	3.27	
			2.97	3.19	3.41	
			3.35	3.60	3.85	
			3.48	3.74	4.00	
			3.76	4.04	4.32	
			3.92	4.22	4.52	
			4.18	4.50	4.82	
	V_{RLVR}	Rising detection voltage	1.49	1.60	1.71	V
			1.62	1.74	1.86	
			1.70	1.83	1.96	
			1.83	1.96	2.09	
			1.92	2.06	2.20	
			2.04	2.19	2.34	
			2.21	2.37	2.53	
			2.37	2.54	2.71	
			2.56	2.75	2.94	
			2.91	3.13	3.35	
			3.05	3.28	3.51	
			3.45	3.70	3.95	
			3.58	3.84	4.10	
			3.86	4.15	4.44	
			4.03	4.33	4.63	

			4.30	4.62	4.94	
Noise cancelling time	t_{NC}	–	-	2	-	us
Operation current	I_{DD}	–	-	3.5	5.0	uA
Operation current(STOP)	$I_{DD, STOP}$	–	-	2.5	3.0	nA

NOTE: While the system is in DEEP-SLEEP mode, if LVD function is enabled, BGR function of VDC should be enabled by setting SCU_VDCCON<PDBGR> to '0'.

25.5 LVI (Low Voltage Indicator) characteristics

Table 35. Operating Condition of Low Voltage Reset

The specifications of the parameters are guaranteed by design.

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating Temperature	T_A	-40	25	105	℃

Table 36. Low Voltage Indicator Characteristics

The specifications of the parameters are guaranteed by design.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating voltage	V_{DD}		0.8	5.0	5.5	V
LVI detection level	V_{FLVI}	Falling detection voltage	1.86	2.00	2.14	V
			1.98	2.13	2.28	
			2.15	2.31	2.47	
			2.31	2.48	2.65	
			2.49	2.68	2.87	
			2.83	3.05	3.27	
			2.97	3.19	3.41	
			3.35	3.60	3.85	
			3.48	3.74	4.00	
			3.76	4.04	4.32	
			3.92	4.22	4.52	
			4.18	4.50	4.82	
	V_{RLVI}	Rising detection voltage	1.92	2.06	2.20	V
			2.04	2.19	2.34	
			2.21	2.37	2.53	
			2.37	2.54	2.71	
			2.56	2.75	2.94	
			2.91	3.13	3.35	
			3.05	3.28	3.51	
			3.45	3.70	3.95	
			3.58	3.84	4.10	
			3.86	4.15	4.44	

			4.03	4.33	4.63	
			4.30	4.62	4.94	
Noise cancelling time	t_{NC}	–	-	2	-	us
Operation current	I_{DD}	–	-	3.5	5.0	uA
Operation current (STOP)	$I_{DD, STOP}$	–	-	2.5	3.0	nA

NOTE: While the system is in DEEP-SLEEP mode, if LVD function is enabled, BGR function of VDC should be enabled by setting SCU_VDCCON<PDBGR> to '0'.

25.6 HSI (High Frequency Internal) RC oscillator characteristics

Table 37. Operating Condition of HSI

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating Voltage	VDD	1.8	5.0	5.5	V
Operating Temperature	T_A	-40	25	105	℃

Table 38. High Frequency Internal RC Oscillator Characteristics

The specifications of the parameters are guaranteed by design.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Frequency	f_{HSI}	V_{DD} = 1.8V to 5.5V T_A = – 20 °C to + 85 °C	31.68	32.0	32.32	MHz
Frequency	f_{HSI}	V_{DD} = 1.8V to 5.5V T_A = – 40 °C to + 105 °C	31.52	32.0	32.48	MHz
Tolerance	–	T_A = – 20 °C to + 85 °C	-1.0	–	1.0	%
		T_A = – 40 °C to + 105 °C	-1.5	–	1.5	%
Clock Duty Ratio	T_{OD}	–	–	50	–	%
Stabilization Time	t_{HFS}	–	100	–	–	us
IRC Current	I_{HSI}	Enable	–	190	–	uA
		Disable	–	1	–	uA

25.7 LSI (Low Frequency Internal) RC oscillator characteristics

Table 39. Operating Condition of LSI

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating Voltage	VDD	1.8	5.0	5.5	V
Operating Temperature	T_A	-40	25	105	℃

Table 40. Low Frequency (500KHz) Internal RC Oscillator Characteristics

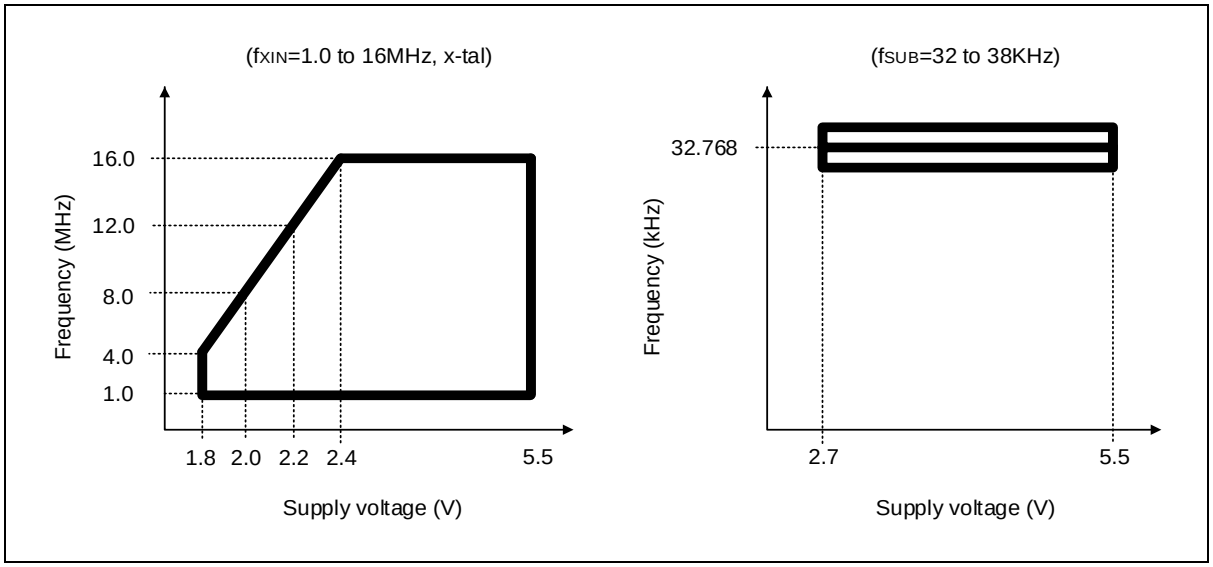
The specifications of the parameters are guaranteed by design.

Parameter	Symbol	Conditions	Min.	Typ	Max.	Units
Operating current NOTE	I_{LIRC}	Enable	—	1.5	2	uA
		Disable	—	1	20	nA
Frequency	f_{LSI}	V_{DD} = 1.8V to 5.5V T_A = – 40 °C to + 105 °C	400	500	600	KHz
Tolerance	–	V_{DD} = 1.8V to 5.5V T_A = – 40 °C to + 105 °C	-20	–	20	%

NOTE: LSI self-consumption current when LSI clock is not supplied to digital logic.

25.8 Operating voltage range

Figure 48. Operating Voltage Range



25.9 HSE (main oscillator) characteristics

Table 41. Operating Condition of HSE

Parameter	Symbol	Min	Typ.	Max	Units
Operating Voltage	VDD	1.8	5.0	5.5	V
Operating Temperature	T_A	-40	25	105	℃

Table 42. Main Oscillator Characteristics

The specifications of the parameters are guaranteed by design.

Oscillator	Parameter	Conditions	Min.	Typ.	Max.	Units
Operating current	I_{DD}	—	—	—	2.5	mA
Power down current	I_{STOP}	—	—	0.2	30	nA
Output frequency	XOUT input frequency	VDDEXT ≥ 1.8V SCU_EOSCR<ISEL[1:0]>='11' SCU_EOSCR<NCOPT[1:0]>='00'	1.0	—	4.0	MHz
		VDDEXT ≥ 2.0V SCU_EOSCR<ISEL[1:0]>='10' SCU_EOSCR<NCOPT[1:0]>='01'	1.0	—	8.0	MHz
		VDDEXT ≥ 2.2V SCU_EOSCR<ISEL[1:0]>='01' SCU_EOSCR<NCOPT[1:0]>='10'	1.0	—	12.0	MHz
		VDDEXT ≥ 2.4V SCU_EOSCR<ISEL[1:0]>='00' SCU_EOSCR<NCOPT[1:0]>='11'	1.0	—	16	MHz
Start-up time	T_{start}	—	—	2	—	ms
Crystal input (low)	V_{IL}	—	—	—	0.2VDD	V
Crystal input (high)	V_{IH}	—	0.8VDD	—	—	V
Crystal out (low)	V_{OL}	—	—	—	0.2VDD	V
Crystal out (high)	V_{OH}	—	0.8VDD	—	—	V
External load cap	C_L	1MHz < f_{OUT} < 4MHz	18	30	35	pf
		4MHz < f_{OUT} < 12MHz	10	22	30	pf
		12MHz < f_{OUT} < 16MHz	7	18	22	pf
Feedback resistance	R_{FB}	VDDEXT=5V	0.7	1.0	1.3	MΩ

Figure 49. Crystal/Ceramic Oscillator

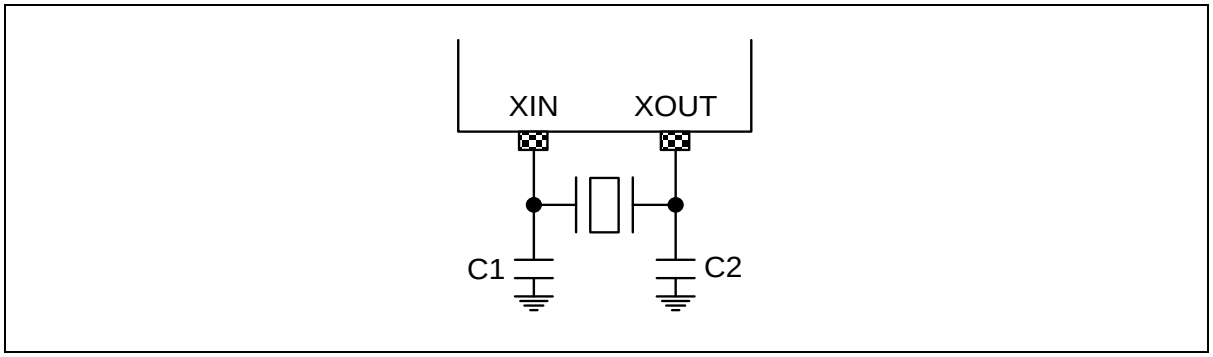


Figure 50. External Clock

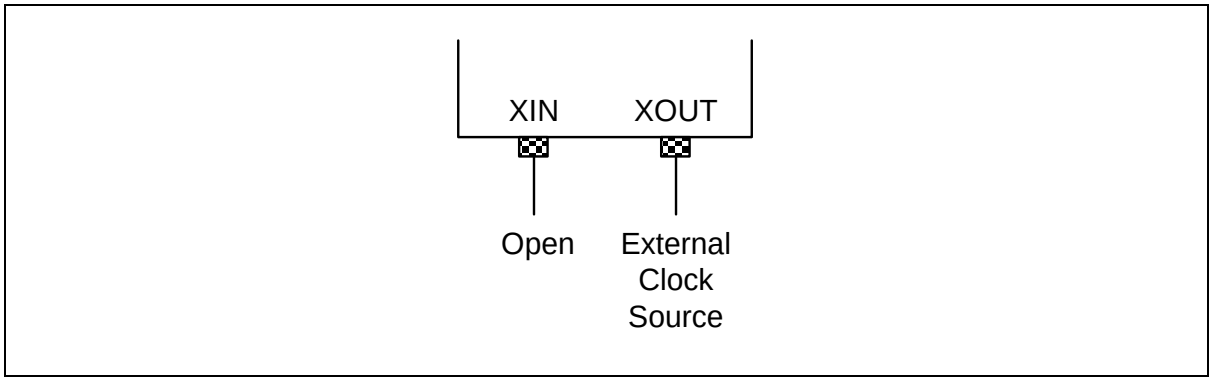
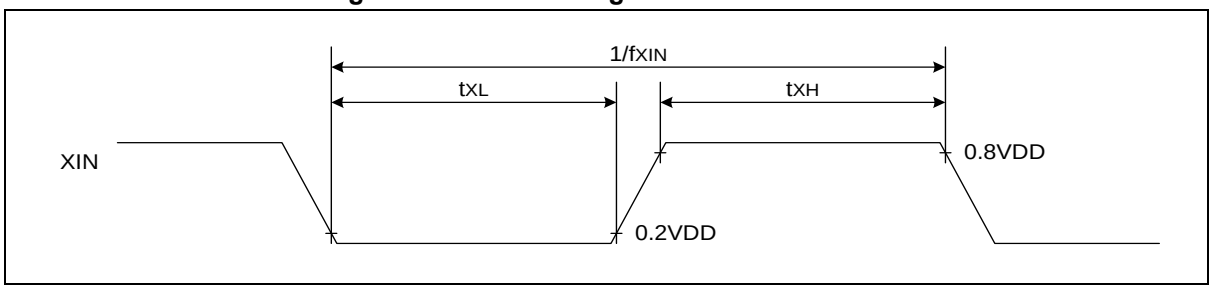


Figure 51. Clock Timing Measurement at XIN



25.10 LSE (sub oscillator) characteristics

Table 43. Operating Condition of LSE

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating Voltage	V_{DD}	2.7	5.0	5.5	V
Operating Temperature	T_A	-40	25	105	℃

Table 44. Sub Oscillator Characteristics

The specifications of the parameters are guaranteed by design.

Oscillator	Parameter	Conditions	Min.	Typ.	Max.	Units
Operating current	I_{DD}			3.0	5.0	uA
Power down current	I_{STOP}	—	—	0.2	15.0	nA
Output frequency	f_{SUB}	—	—	32.768	—	KHz
Start-up time	T_{start}	—	—	2	—	s
Crystal input (low)	V_{IL}	—	—	—	0.2VDD	V
Crystal input (High)	V_{IH}	—	0.8VDD	—	—	V
Crystal out (low)	V_{OL}	—	—	—	0.2VDD	V
Crystal out (high)	V_{OH}	—	0.8VDD	—	—	V
External load cap	R_{FB}	—	5	15	35	pF
Feedback resistance	C_L	—	7	12	24	MΩ

Figure 52. Crystal Oscillator

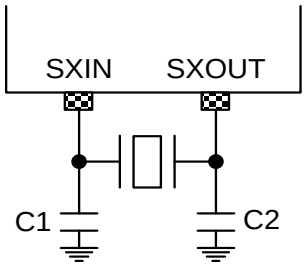
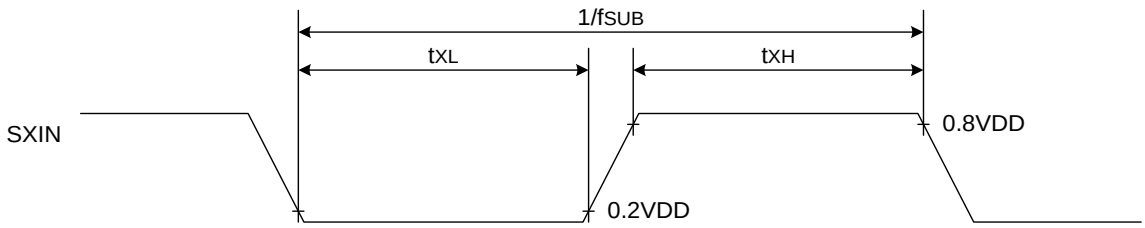


Figure 53. Clock Timing Measurement at SXIN



25.11 PLL electrical characteristics

Table 45. Operating Condition of PLL

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating Voltage	V_{DD}	1.8	5.0	5.5	V
Operating Temperature	T_A	-40	25	105	℃

Table 46. PLL Electrical Characteristics

The specifications of the parameters are guaranteed by design.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating current	I_{DD}	Enable	—	—	1	mA
		Disable	—	5	500	nA
Output frequency	f_{OUT}	—	1	—	48	MHz
Duty	f_{DUTY}		40	—	60	%
VCO Frequency	f_{VCO}		10	—	240	MHz
Frequency Peak-to-Peak Jitter	$f_{JITTER(P-P)}$				500	ps
VCO Linear Range	f_{VCO_LIN}		50	—	150	MHz
Input Frequency	$f_{PLLINCLK}$		4	8	16	MHz
Locking Time*	t_{LOCK}		—	60	100	us
Input Bandwidth	f_{IN}		1	2	3	MHz

NOTE: The tolerance of PLL output frequency is reflected based on PLL input clock source selected by PLLINCLKSEL in the SCU_SCCR[2] register.

25.12 Supply current characteristics

Table 47. Operating Condition of Supply Current

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating Voltage	V_{DD}	1.8	5.0	5.5	V
Operating Temperature	T_A	-40	25	105	℃

Table 48. Supply Current Characteristics

The specifications of the parameters are guaranteed by design.

Parameter	Symbol	Conditions		Typ.	Max	Units
Supply current	I_{DD1} (Run)	f_{XIN} = 8MHz	VDD = 5V	4.0	12.0	mA
		f_{HSI} = 32MHz		10.0	30.0	
		f_{HSI} = 12MHz		3.5	10.0	
		f_{LSI} = 500KHz		200	600	uA
		f_{LSE} = 32.768KHz		140	300	
	I_{DD2} (SLEEP)	f_{XIN} = 8MHz	VDD = 5V	5	15	mA
		f_{HIRC} = 32MHz		6	18	
		f_{HIRC} = 12MHz		2	6	
		F_{LIRC} = 500KHz		180	500	uA
		F_{LSE} = 32.768KHz		130	400	
	I_{DD3} (DEEP-SLEEP)	WDT(WDTRC) = ON, LSIAON=ENABLE NOTE3, LVD = ON, T_A = 25 °C	VDD = 5V	30	—	uA
	I_{DD4} (DEEP-SLEEP)	WDT(WDTRC) = ON, LSIAON=ENABLE NOTE3, LVD = OFF NOTE4, T_A = 25 °C		25	—	uA
	I_{DD5} (DEEP-SLEEP)	WDT(WDTRC) = OFF, LVD = ON, T_A = 25 °C		5	—	uA
	I_{DD6} (DEEP-SLEEP)	WDT(WDTRC) = OFF, LVD = OFF NOTE4, T_A = 25 °C		2	—	uA
		WDT(WDTRC) = OFF, LVD = OFF NOTE4, TA = 85 °C		10	—	uA
		WDT(WDTRC) = OFF, LVD = OFF N OTE4, TA = 105 °C		30	—	uA

NOTES:

1. All supply current items do not include the current of a low frequency internal RC oscillator and a peripheral block.
2. All supply current items include the current of the power-on reset (POR) block.
3. SCU_SMR<LSIAON> bit must be enabled in order to use the WDT as a wake up source in DEEP-SLEEP mode.

4. ‘LVD = OFF’ indicates that LVR reset function , LVR block and LVI block are disabled.
   SCU_RSER<LVRRST> = 0
   SCULV_LVRCR<LVREN> = 0x55
   SCULV_LVICR<LVIEN> = 0

25.13 I/O Port characteristics

Table 49. Operating Condition of I/O Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating Voltage	V_{DD}	1.8	5.0	5.5	V
Operating Temperature	T_A	-40	25	105	℃

25.13.1 General I/O characteristics

The parameters given in Table 50 for I/O static characteristics are derived from tests performed under the ambient temperature, and VDD supply voltage conditions summarized in Table 49.

Table 50. I/O static characteristics

The specifications of the parameters are guaranteed by design.

Parameter	Symbol	Conditions	Min.	Typ	Max.	Units
Input high voltage	V_{IH1}	PA, PB, PC, PD, PE, PF, nBOOT(PB3)	0.8*V_{DD}	—	V_{DD}	V
Input low voltage	V_{IL1}	PA, PB, PC, PD, PE, PF, nBOOT(PB3)	V_{GND}	—	0.2*V_{DD}	V
1.8 V Input high voltage	V_{IH2}	PF5, PF6, PF7 1.8 V input level in PCU_PLSR[2:0]	0.8*1.8	—	1.8	V
1.8 V Input low voltage	V_{IL2}	PF5, PF6, PF7 1.8 V input level in PCU_PLSR[2:0]	V_{GND}	—	0.2*1.8	V
Input high leakage current	I_{IHLKG}	All Input ports	—	—	1	uA
Input low leakage current	I_{ILLKG}	All Input ports	-1	—	—	uA
Pull-up resistor	R_{PU}	All Input pins, nBOOT(PB3)	40	—	70	KΩ
Pull-down resistor	R_{PD}	All Input pins, nBOOT(PB3)	40	—	70	KΩ
I/O pin capacitance	C_{IO}	—	—	—	10	pF

25.13.2 Output driving current

A31G22x GPIOs (general purpose input/outputs) can sink or source.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in 25.1:

• The sum of the currents sourced by all the I/Os on V_{DD}, plus the maximum run consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{OH}.

• The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{OL}.

Table 51. Output voltage Characteristics

The specifications of the parameters are guaranteed by design.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output High Level Voltage 1	V_{OH1}	$V_{DD} \geq 1.8$ V, $I_{OH1} = -1$ mA PA[5:0], PA[11:8], PF[4:0], PF[11:8], PE[15:8]	1.44	—	1.80	V
		$V_{DD} \geq 3.3$ V, $I_{OH1} = -2$ mA PA[5:0], PA[11:8], PF[4:0], PF[11:8], PE[15:8]	2.64	—	3.30	V
		$V_{DD} \leq 5.5$ V, $I_{OH1} = -5$ mA PA[5:0], PA[11:8], PF[4:0], PF[11:8], PE[15:8]	4.40	—	5.50	V
Output low level Current 1	V_{OL1}	$V_{DD} \geq 1.8$ V, $I_{OL1} = +1$ mA PA[5:0], PA[11:8], PF[4:0], PF[11:8], PE[15:8]	0.00	—	0.36	V
		$V_{DD} \geq 3.3$ V, $I_{OL1} = +3$ mA PA[5:0], PA[11:8], PF[4:0], PF[11:8], PE[15:8]	0.00	—	0.66	V
		$V_{DD} \leq 5.5$ V, $I_{OL1} = +7$ mA PA[5:0], PA[11:8], PF[4:0], PF[11:8], PE[15:8]	0.00	—	1.10	V
Output High Level Voltage 2	V_{OH2}	$V_{DD} \geq 1.8$ V, $I_{OH2} = -1$ mA PA[7:6], PB[15:3], PC0, PC1, PC[12:6], PD0, PD1, PD2, PD3, PD4, PD5	1.44	—	1.80	V
		$V_{DD} \geq 3.3$ V, $I_{OH2} = -3$ mA PA[7:6], PB[15:3], PC0, PC1, PC[12:6], PD0, PD1, PD2, PD3, PD4, PD5	2.64	—	3.30	V
		$V_{DD} \leq 5.5$ V, $I_{OH2} = -8$ mA PA[7:6], PB[15:3], PC0, PC1, PC[12:6], PD0, PD1, PD2, PD3, PD4, PD5	4.40	—	5.50	V
Output low level Current 2	V_{OL2}	$V_{DD} \geq 1.8$ V, $I_{OL2} = +1$ mA PA[7:6], PB[15:3], PC0, PC1, PC[12:6], PD0, PD1, PD2, PD3, PD4, PD5	0.00	—	0.36	V

		V_{DD} ≥ 3.3 V, I_{OL2} = +3 mA PA[7:6], PB[15:3], PC0, PC1, PC[12:6], PD0, PD1, PD2, PD3, PD4, PD5	0.00	—	0.66	V
		V_{DD} ≤ 5.5 V, I_{OL2} = +7 mA PA[7:6], PB[15:3], PC0, PC1, PC[12:6], PD0, PD1, PD2, PD3, PD4, PD5	0.00	—	1.10	V
Output High Level Voltage 3	V_{OH3}	V_{DD} ≥ 1.8 V, I_{OH3} = -2 mA PE0, PE1, PE[7:2]	1.44	—	1.80	V
		V_{DD} ≥ 3.3 V, I_{OH3} = -8 mA PE0, PE1, PE[7:2]	2.64	—	3.30	V
		V_{DD} ≤ 5.5 V, I_{OH3} = -19 mA PE0, PE1, PE[7:2]	4.40	—	5.50	V
Output low level Current 3	V_{OL3}	V_{DD} ≥ 1.8 V, I_{OL3} = +2 mA PE0, PE1, PE[7:2]	0.00	—	0.36	V
		V_{DD} ≥ 3.3 V, I_{OL3} = +6 mA PE0, PE1, PE[7:2]	0.00	—	0.66	V
		V_{DD} ≤ 5.5 V, I_{OL3} = +14 mA PE0, PE1, PE[7:2]	0.00	—	1.10	V
Output High Level Voltage 4	V_{OH4}	V_{DD} ≥ 1.8 V, I_{OH4} = Don't Care PF5, PF6, PF7	1.44	—	1.80	V
		V_{DD} ≥ 3.3 V, I_{OH4} = Don't Care PF5, PF6, PF7	2.64	—	3.30	V
		V_{DD} ≤ 5.5 V, I_{OH4} = Don't Care PF5, PF6, PF7	4.40	—	5.50	V
Output low level Current 4	V_{OL4}	V_{DD} ≥ 1.8 V, I_{OL4} = +1 mA PF5, PF6, PF7	0.00	—	0.36	V
		V_{DD} ≥ 3.3 V, I_{OL4} = +3 mA PF5, PF6, PF7	0.00	—	0.66	V
		V_{DD} ≤ 5.5 V, I_{OL4} = +7 mA PF5, PF6, PF7	0.00	—	1.10	V
Output High Level Voltage 5	V_{OH5}	V_{DD} ≥ 1.8 V, I_{OH5} = -1 mA PC2, PC3, PC4	1.44	—	1.80	V
		V_{DD} ≥ 3.3 V, I_{OH5} = -2 mA PC2, PC3, PC4	2.64	—	3.30	V
		V_{DD} = 5.5 V, I_{OH5} = -5 mA PC2, PC3, PC4	4.40	—	5.50	V
		Strength On[NOTE1] V_{DD} ≥ 1.8 V, I_{OH5} = -2 mA PC2, PC3, PC4	1.44	—	1.80	V
		Strength On[NOTE1] V_{DD} ≥ 3.3 V, I_{OH5} = -7 mA PC2, PC3, PC4	2.64	—	3.30	V
		Strength On[NOTE1] V_{DD} ≤ 5.5 V, I_{OH5} = -16 mA PC2, PC3, PC4	4.40	—	5.50	V

Output low level Current 5	V_{OL5}	V_{DD} ≥ 1.8 V, I_{OL5} = +1 mA PC2, PC3, PC4	0.00	—	0.36	V
		V_{DD} ≥ 3.3 V, I_{OL5} = +3 mA PC2, PC3, PC4	0.00	—	0.66	V
		V_{DD} ≤ 5.5 V, I_{OL5} = +7 mA PC2, PC3, PC4	0.00	—	1.10	V
		Strength On[NOTE1] V_{DD} ≥ 1.8 V, I_{OL5} = +2 mA PC2, PC3, PC4	0.00	—	0.36	V
		Strength On[NOTE1] V_{DD} ≥ 3.3 V, I_{OL5} = +8 mA PC2, PC3, PC4	0.00	—	0.66	V
		Strength On[NOTE1] V_{DD} ≤ 5.5 V, I_{OL5} = +19 mA PC2, PC3, PC4	0.00	—	1.10	V
Output High Level Voltage 6	V_{OH6}	V_{DD} ≥ 1.8 V, I_{OH6} = -1 mA PB0, PB1, PB2	1.44	—	1.80	V
		V_{DD} ≥ 3.3 V, I_{OH6} = -2 mA PB0, PB1, PB2	2.64	—	3.30	V
		V_{DD} ≤ 5.5 V, I_{OH6} = -5 mA PB0, PB1, PB2	4.40	—	5.50	V
		Strength On[NOTE1] V_{DD} ≥ 1.8 V, I_{OH6} = -2 mA PB0, PB1, PB2	1.44	—	1.80	V
		Strength On[NOTE1] V_{DD} ≥ 3.3 V, I_{OH6} = -7 mA PB0, PB1, PB2	2.64	—	3.30	V
		Strength On[NOTE1] V_{DD} ≤ 5.5 V, I_{OH6} = -16 mA PB0, PB1, PB2	4.40	—	5.50	V
Output low level Current 6	V_{OL6}	V_{DD} ≥ 1.8 V, I_{OL6} = +1 mA PB0, PB1, PB2	0.00	—	0.36	V
		V_{DD} ≥ 3.3 V, I_{OL6} = +5 mA PB0, PB1, PB2	0.00	—	0.66	V
		V_{DD} ≤ 5.5 V, I_{OL6} = +11 mA PB0, PB1, PB2	0.00	—	1.10	V
		Strength On[NOTE1] V_{DD} ≥ 1.8 V, I_{OL6} = +2 mA PB0, PB1, PB2	0.00	—	0.36	V
		Strength On[NOTE1] V_{DD} ≥ 3.3 V, I_{OL6} = +8 mA PB0, PB1, PB2	0.00	—	0.66	V
		Strength On[NOTE1] V_{DD} ≤ 5.5 V, I_{OL6} = +19 mA PB0, PB1, PB2	0.00	—	1.10	V
Output low level Current 7	V_{OL7}	High Current Output (Sink)[NOTE2] V_{DD} ≥ 1.8 V, I_{OL7} = +28 mA	0.00	—	0.36	V

		PD2, PD3, PD4, PD5, PE2, PE3, PE4, PE5, PE6, PE7				
		High Current Output (Sink)[NOTE2] V_{DD} ≥ 3.3 V, I_{OL7} = +53mA PD2, PD3, PD4, PD5, PE2, PE3, PE4, PE5, PE6, PE7	0.00	—	0.66	V
		High Current Output (Sink)[NOTE2] V_{DD} ≤ 5.5 V, I_{OL7} = +73mA PD2, PD3, PD4, PD5, PE2, PE3, PE4, PE5, PE6, PE7	0.00	—	1.10	V

NOTES:

1. GPIO's strength function is controlled by Px_STR register.
2. The sink type high current output driving of GPIOs is controlled by PCU2_ISEGPEN and PCU2_ISEGR, PCU2_ISEGIR registers. (Refer to A31G22x User's Manual.)

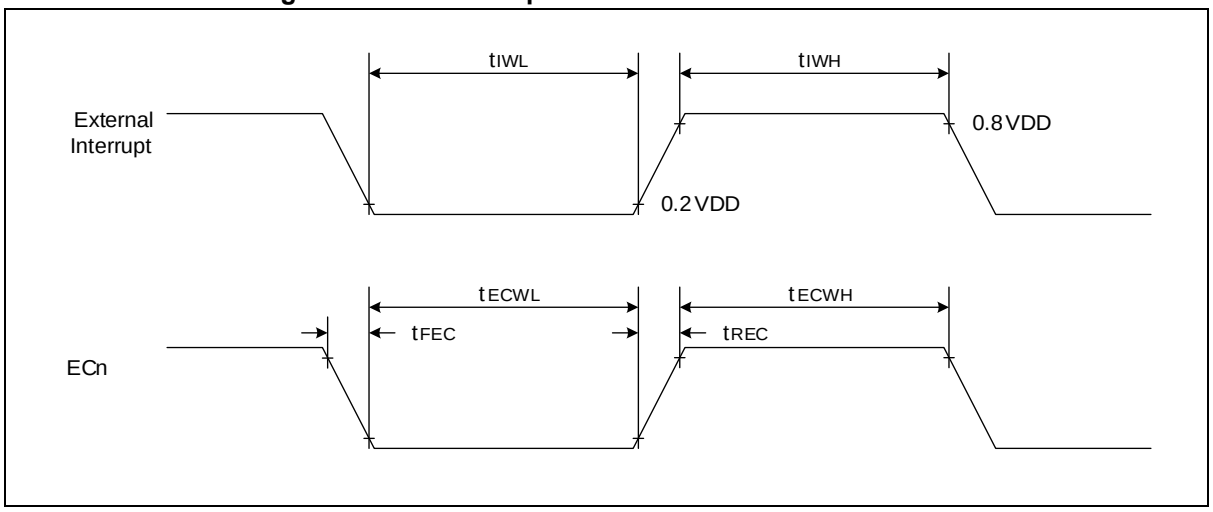
25.13.3 I/O AC characteristics

The definition and values of external input AC characteristics are given in Figure 54 and Table 54.

Table 52. External Input AC Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Interrupt input high low width	t_{IWH}, t_{IWL}	All external interrupts 1.8 V≤V_{DD}≤ 5.5 V -40 °C≤T_A ≤105 °C	100	—	—	ns
External counter input high low pulse width	t_{ECWH}, t_{ECWL}	ECn, All external counter input 1.8 V≤V_{DD}≤ 5.5 V -40 °C≤T_A ≤105 °C	100	—	—	
External counter transition time	t_{REC}, t_{FEC}	ECn, All external counter input 1.8 V≤V_{DD}≤ 5.5 V -40 °C≤T_A ≤105 °C	—	—	20	

Figure 54. External Input AC Characteristics definitions



25.14 nRESET pin characteristics

The nRESET pin input is connected to a internal permanent pull-up resistor, R_{PU}.

The parameters given in Table 53 are derived from tests performed under the ambient temperature and VDD supply voltage conditions summarized in Table 49.

Table 53. nRESET pin Characteristics

The specifications of the parameters are guaranteed by design.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
nRESET input high voltage	$V_{IH(nRST)}$	1.8 V ≤ V_{DD} ≤ 5.5 V	0.8*V_{DD}	—	V_{DD}	V
nRESET input low voltage	$V_{IL(nRST)}$	1.8 V ≤ V_{DD} ≤ 5.5 V	V_{GND}	—	0.2*V_{DD}	V
nRESET input hysteresis	$V_{HYS(nRST)}$	1.8 V ≤ V_{DD} ≤ 5.5 V	100	200	—	mV
nRESET Pull-up resistor	$R_{PU(nRST)}$	V_{IN} = V_{SS}	150	250	400	KΩ
nRESET input low width	t_{RST}	1.8 V≤V_{DD}≤ 5.5 V	10	—	—	us

Figure 55. nRESET pin low width definitions

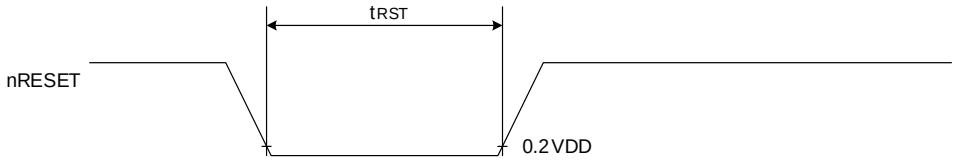
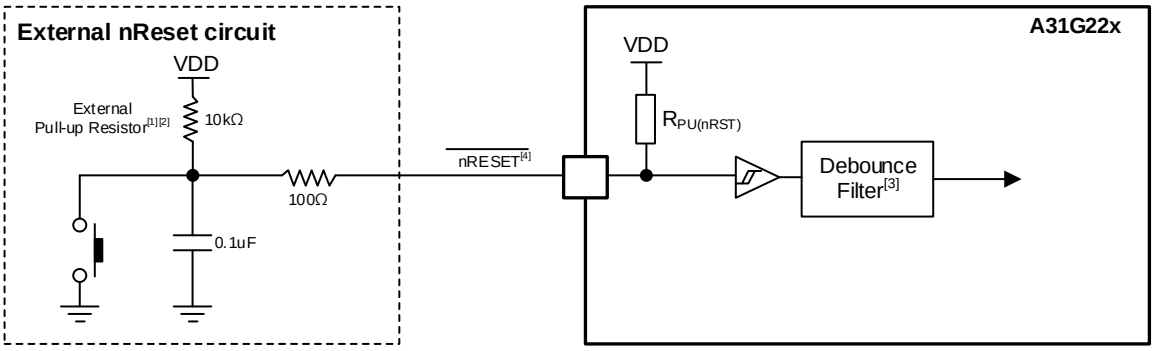


Figure 56. Recommended nRESET pin protection



NOTES:

[1] It is recommended to configure the circuit by connecting an external pull-up resistor to the nRESET pin.
[2] The external pull-up resistor should be less than the internal pull-up R_{PU} of nRESET.
[3] It is recommended to activate the nRESET debounce filter to prevent external noise from entering.
[4] The user must make sure that the level of the RESET pin can drop below the $V_{IL(nRST)}$ maximum level.

25.15 UART characteristics

Table 54. Operating Condition of UART

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating Voltage	V_{DD}	1.8	5.0	5.5	V
Operating Temperature	T_A	-40	25	105	℃

25.16 SPI characteristics

The parameters given in Table 56 for SPI are derived from tests performed under the ambient temperature, and f_{PCLK} frequency and V_{DD} supply voltage conditions summarized in Table 55.

Table 55. Operating Condition of SPIn (n = 20, 21)

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating Voltage	V_{DD}	1.8	5.0	5.5	V
Operating Temperature	T_A	-40	25	105	℃

Table 56. SPIn characteristics (n = 20, 21)

The specifications of the parameters are guaranteed by design.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
SPI clock frequency with strength on	f_{SCK1}	SPI20, SPI21 V_{DD}≤ 1.8 V	—	—	12	MHz
	f_{SCK2}	SPI20, SPI21 V_{DD}≤ 3.3 V	—	—	12	MHz
	f_{SCK3}	SPI20, SPI21 V_{DD}≤ 5.5 V	—	—	12	MHz
SPI clock frequency with strength off	f_{SCK4}	SPI20, SPI21 V_{DD}≤ 1.8 V	—	—	5	MHz
	f_{SCK5}	SPI20, SPI21 V_{DD}≤ 3.3 V	—	—	8	MHz
	f_{SCK6}	SPI20, SPI21 V_{DD}≤ 5.5 V	—	—	10	MHz
Duty cycle of SPI frequency (SCK)	Duty	Slave Mode	30	50	70	%
Capacitance load	C_{CL}	—	—	—	TBD	pF

25.17 USART SPI characteristics

Table 57. Operating Condition of USART SPI

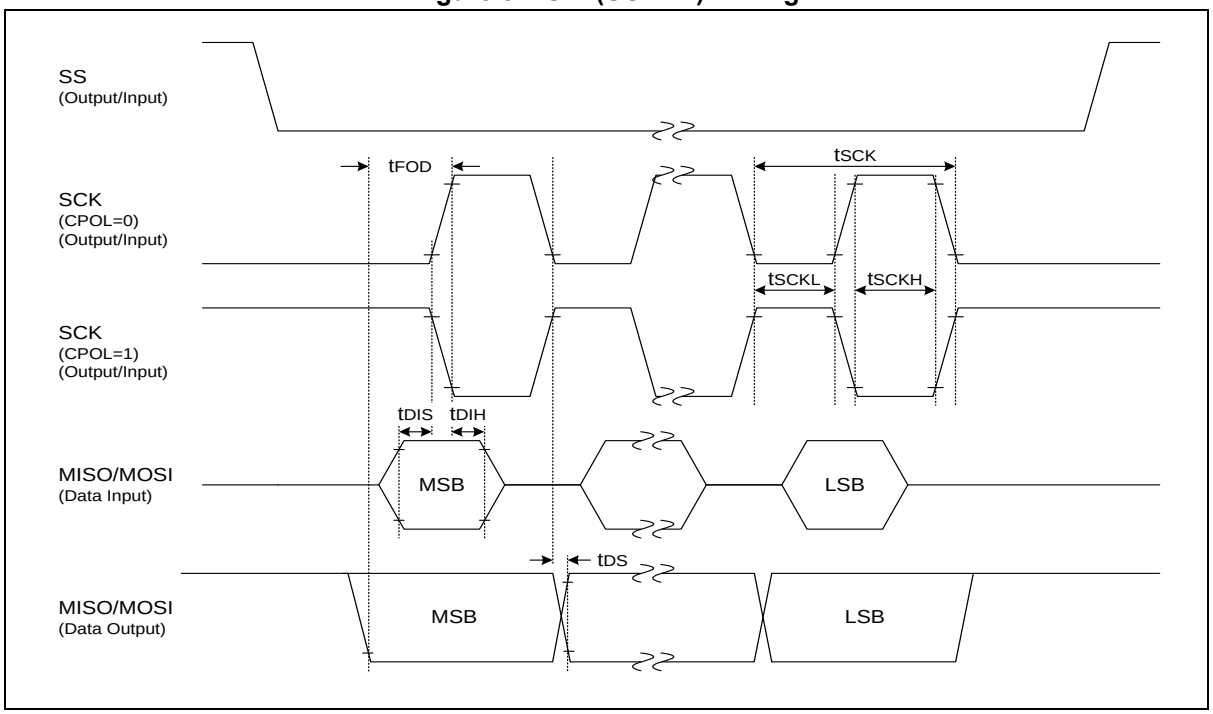
Parameter	Symbol	Min.	Typ.	Max.	Units
Operating Voltage	V_{DD}	1.8	5.0	5.5	V
Operating Temperature	T_A	-40	25	105	℃

Table 58. USART SPI Characteristics

The specifications of the parameters are guaranteed by design.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output clock pulse period	t_{SCK}	Internal SCK source	400	—	—	ns
Input clock pulse period		External SCK source	400	—	—	
Output clock high, low pulse width	t_{SCKH}, t_{SCKL}	Internal SCK source	180	—	—	
Input clock high, low pulse width		External SCK source	180	—	—	
First output clock delay time	t_{FOD}	Internal/external SCK source	200	—	—	
Output clock delay time	t_{DS}	—	—	—	100	
Input setup time	t_{DIS}	—	180	—	—	
Input hold time	t_{DIH}	—	180	—	—	

Figure 57. SPI (USART) Timing



25.18 USART UART timing characteristics

Table 59. Operating Condition of USART UART

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating Voltage	V_{DD}	1.8	5.0	5.5	V
Operating Temperature	T_A	-40	25	105	℃

Table 60. USART UART Timing Characteristics

The specifications of the parameters are guaranteed by design.

Parameter	Symbol	Min.	Typ	Max.	Units
Serial port clock cycle time	t_{SCK}	1250	t_{CPU} x 16	1650	ns
Output data setup to clock rising edge	t_{S1}	590	t_{CPU} x 13	—	
Clock rising edge to input data valid	t_{S2}	—	—	590	
Output data hold after clock rising edge	t_{H1}	t_{CPU} – 50	t_{CPU}	—	
Input data hold after clock rising edge	t_{H2}	0	—	—	
Serial port clock High, Low level width	t_{HIGH}, t_{LOW}	470	t_{CPU} x 8	970	

Figure 58. Waveform of UART Timing Characteristics

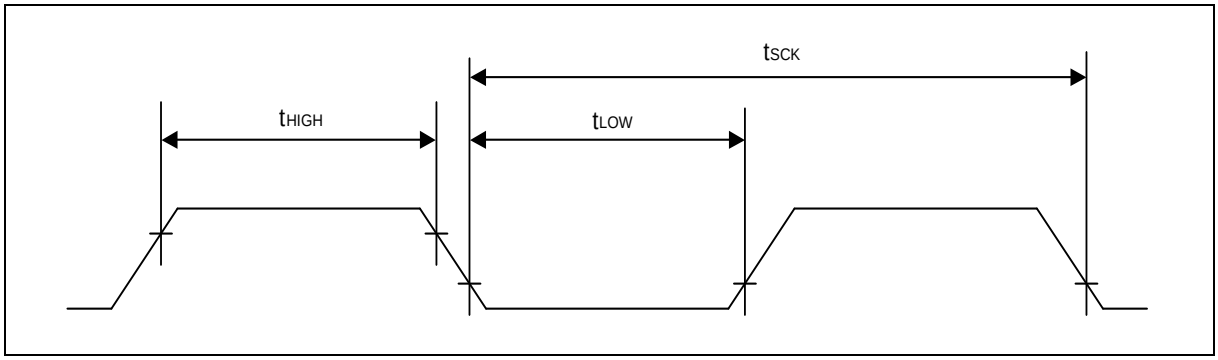
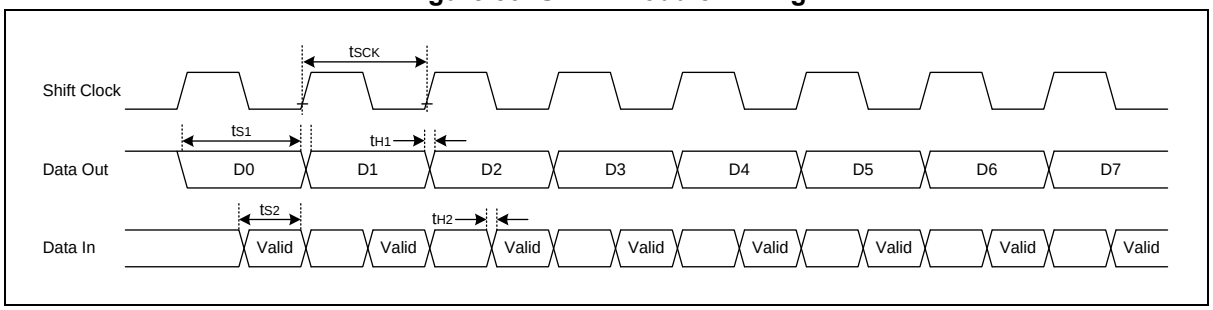


Figure 59. UART Module Timing



25.19 I2C characteristics

Table 61. Operating Condition of I2C

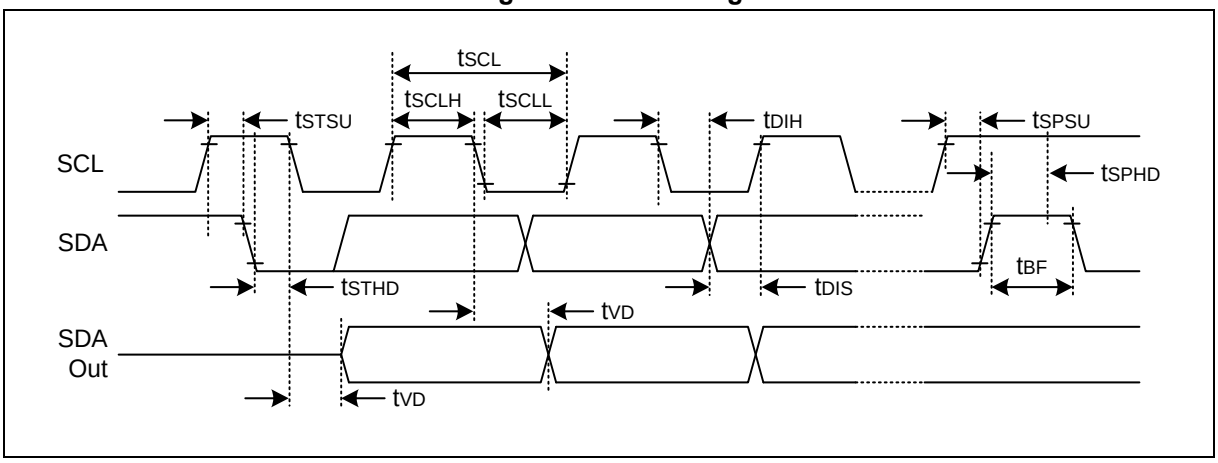
Parameter	Symbol	Min.	Typ.	Max.	Units
Operating Voltage	V_{DD}	1.8	5.0	5.5	V
Operating Temperature	T_A	-40	25	105	℃

Table 62. I2C Characteristics

The specifications of the parameters are guaranteed by design.

Parameter	Symbol	Standard		Fast		Units
		Min.	Max.	Min.	Max.	
Clock frequency	t_{SCL}	0	100	0	400	KHz
Clock high pulse width	t_{SCLH}	4.0	—	0.6	—	us
clock low pulse width	t_{SCLL}	4.7	—	1.3	—	
Bus free time	t_{BF}	4.7	—	1.3	—	
Start condition setup time	t_{STSU}	4.7	—	0.6	—	
Start condition hold time	t_{STHD}	4.0	—	0.6	—	
Stop condition setup time	t_{SPSU}	4.0	—	0.6	—	
Stop condition hold time	t_{SPHD}	4.0	—	0.6	—	
Output valid from clock	t_{VD}	0	—	0	—	
Data input hold time	t_{DIH}	0	—	0	1.0	
Data input setup time	t_{DIS}	250	—	100	—	ns

Figure 60. I2C Timing



25.20 Internal Code flash characteristics

Table 63. Operating Condition of Internal Code Flash

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating Voltage	V_{DD}	1.8	5.0	5.5	V
Operating Temperature	T_A	-40	25	105	℃

Table 64. Internal Code Flash Characteristics

The specifications of the parameters are guaranteed by design.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Max. available clock frequency	—	0-wait	—	—	20	MHz
Reset Cycle Time	$f_{RSTBUSY}$	—	5.6	8	10.4	us
Fuse Program Cycle Time	$f_{FRDBUSY}$	—	4.2	6	7.8	us
Normal Program Cycle Time	$t_{PGMBUSY}$	—	21	30	42	us
Normal Page Erase Cycle Time	$t_{PERSBUSY}$	—	2.8	4	5.2	ms
Sector Erase Cycle Time	$t_{SERSBUSY}$	—	2.8	4	5.2	ms
Chip Erase Cycle Time	$t_{MERSBUSY}$	—	5.6	8	10.4	ms
Endurance of write/erase	N_{FWE}	T_A=25 ˚C, Page unit	10,000	—	—	Times
Retention time	t_{FRT}	—	10	—	—	Years

25.21 Internal Data flash characteristics

Table 65. Operating Condition of Internal Data Flash

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating Voltage	V_{DD}	1.8	5.0	5.5	V
Operating Temperature	T_A	-40	25	105	℃

Table 66. Internal Data Flash Characteristics

The specifications of the parameters are guaranteed by design.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Max. available clock frequency	—	0-wait	—	—	20	MHz
Reset Cycle Time	$f_{RSTBUSY}$	—	5.6	8	10.4	us
Fuse Program Cycle Time	$f_{FRDBUSY}$	—	4.2	6	7.8	us
Normal Program Cycle Time	$t_{PGMBUSY}$	—	21	30	42	us
Normal Page Erase Cycle Time	$t_{PERSBUSY}$	—	2.8	4	5.2	ms
Sector Erase Cycle Time	$t_{SERSBUSY}$	—	2.8	4	5.2	ms
Chip Erase Cycle Time	$t_{MERSBUSY}$	—	5.6	8	10.4	ms
Endurance of write/erase	N_{FWE}	T_A=25 ˚C, Page unit	100,000	—	—	Times
Retention time	t_{FRT}	—	10	—	—	Years

25.22 ADC characteristics

Table 67. Operating Condition of ADC

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating Voltage	V_{DD}	2.1*	5.0	5.5	V
Operating Temperature	T_A	-40	25	105	℃

NOTE: If 12-bit ADC uses voltage of less than 2.0V, measurement error may be big. To avoid this, it is recommended to use voltage ranging from 2.1V to 5.5V for the ADC which is used for precision sensing of analog voltage.

Table 68. ADC Electrical Characteristics

The specifications of the parameters are guaranteed by design.

Parameter	Symbol	Condition	Min.	Typ.	Max.	unit
Resolution	—	—	—	—	12	Bit
Number of Channel	—	—	14	18	—	CH
Analog input range	V_{AVREF}	V_{AVREF}=V_{DD} V_{SS}=V_{GND}	VSS	—	AVREF	V
Operating Current	I_{DD}	V_{DD} = 5.0V MCLK=20MHz Input buffer OFF	—	2.4	—	mA
		V_{DD} = 5.0V MCLK=20MHz Input buffer ON	—	3.0	—	mA
Standby Current	I_{ST}	—	—	50	—	nA
Full Scale Input Range	V_{IN}	V_{AVDD}=V_{DD}	V_{GND}		V_{AVDD}	V
Differential nonlinearity	DNL	—	—	±1	±2	LSB
Integral nonlinearity	INL	—	—	±2	±4	LSB
Zero offset error	ZOE	—	—	±2	—	LSB
Full scale error	FSE	—	—	±2	—	LSB
Input clock frequency	MCLK	VDD > 3.3V	—	—	20	MHz
		VDD > 2.7V	—	—	13.3	
		VDD > 2.0V	—	—	3	
Conversion time	t_{CONV}	TSMP_I<4:0> 2~32*MCLK	15*MCLK	—	45*MCLK	us
Conversion frequency ratio	C_{RATE}	VDD > 3.3V	—	—	1.0	Msps
		VDD > 2.7V	—	—	0.7	
		VDD > 2.0V	—	—	0.15	
Sampling time	t_{SAMPLE}	VDD > 3.3V	—	—	10	us
		VDD > 2.7V	—	—	10	
		VDD > 2.0V	—	—	10	

25.23 DAC characteristics

Table 69. Operating Condition of DAC

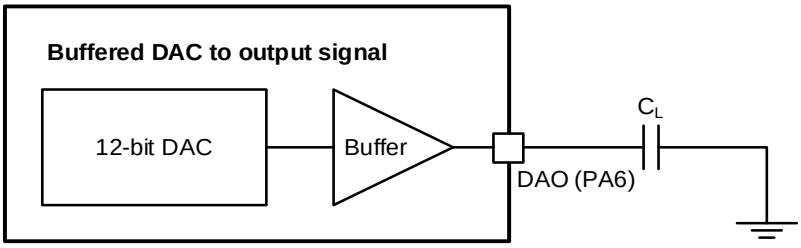
Parameter	Symbol	Min.	Typ.	Max.	Units
Operating Voltage	V_{DD}	2.7	5.0	5.5	V
Operating Temperature	T_A	-40	25	105	℃

Table 70. DAC Electrical Characteristics

The specifications of the parameters are guaranteed by design.

Parameter	Symbol	Condition	Min.	Typ.	Max.	unit
Resolution			—	—	12	Bit
DAC Output Voltage	D_{AOUT}	0x0A3(min) ~ 0xF5B(max) (@AVDD=5V) 0x12F(min) ~ 0xECF(max) (@AVDD=2.7V)	0.2	—	VDD-0.2	V
Operating Current	$I_{AVDD,rms}$	No load, middle code(0x800)	—	0.95	1.48	mA
DNL	—	No R-Load, DAC Output Voltage	—	2	8	LSB
INL	—	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095)	—	4	8	LSB
Offset	—	Offset Error is difference between measured value at Code (0x800) and the ideal value(AVDD/2)	—	—	10	mV
Conversion Time	$t_{SETTLINB}$	—	—	2	4	us
Capacitive load	C_L	Maximum capacitive load at DAC_OUT pin when Buffer is enabled.	—	—	50	pF

Figure 61. 12-bit buffered DAC



NOTE: The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external current load. The buffer can be enabled by configuring the DAC_BUF_EN[10] bit in the DAC_CR register. (Refer to A31G22x User's Manual)

25.24 Comparator characteristics

Table 71. Operating Condition of Comparator

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating Voltage	V_{DD}	2.0	5.0	5.5	V
Operating Temperature	T_A	-40	25	105	℃

Table 72. Comparator Characteristics

The specifications of the parameters are guaranteed by design.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Current	$I_{DD(RMS)}$	-	—	70	100	uA
Input Voltage Range	V_{ICM}	-	V_{GND}+50 mV	—	V_{DD}-50mV	V
Propagation Delay	tPD (t_{PHL}, t_{PLH})	V_{OV} > 10mV	—	0.5	2	us
Input Offset	V_{OS}	VDDEDXT=4.5V, VIN=1/2 VDDEXT, Before Offset Calibration	—	±10	±20	mV
		VDDEDXT=4.5V, VIN=1/2 VDDEXT, After Offset Calibration	—	—	±5	mV
Hysteresis	V_{HYS}	V_{DD}=4.5V, HYSSEL=0	—	±5	±25	mV
		V_{DD}=4.5V, HYSSEL=1	—	±20	±60	mV

25.25 LCD driver characteristics

Table 73. Operating Condition of LCD Driver

Parameter	Symbol	Min	Typ.	Max	Units
Operating Voltage	V_{DD}	2.7	5.0	5.5	V
Operating Temperature	T_A	-40	25	105	℃

Table 74. LCD DriverCharacteristics

The specifications of the parameters are guaranteed by design.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
LCD Voltage	VLC0	LCD contrast = DISABLED, 1/4 bias	—	—	—	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 0x00	Typ.x0.94	V_{DD}x16/31	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 0x01	Typ.x0.94	V_{DD}x16/30	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 0x02	Typ.x0.94	V_{DD}x16/29	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 0x03	Typ.x0.94	V_{DD}x16/28	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 0x04	Typ.x0.94	V_{DD}x16/27	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 0x05	Typ.x0.94	V_{DD}x16/26	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 0x06	Typ.x0.94	V_{DD}x16/25	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 0x07	Typ.x0.94	V_{DD}x16/24	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 0x08	Typ.x0.94	V_{DD}x16/23	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 0x09	Typ.x0.94	V_{DD}x16/22	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 0x0A	Typ.x0.94	V_{DD}x16/21	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load	Typ.x0.94	V_{DD}x16/20	Typ.x1.06	V

		VLCD[3:0] = 0x0B				
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 0x0C	Typ.x0.94	V_{DD}x16/19	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 0x0D	Typ.x0.94	V_{DD}x16/18	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 0x0E	Typ.x0.94	V_{DD}x16/17	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 0x0F	Typ.x0.94	V_{DD}x16/16	Typ.x1.06	V
LCD Mid Bias Voltage[NOTE]	VLC1	V_{DD} = 2.7V to 5.5V, LCD clock = 0Hz, 1/4 bias, No panel load	Typ-0.2	3/4xVLC0	Typ+0.2	V
	VLC2		Typ-0.2	2/4xVLC0	Typ+0.2	V
	VLC3		Typ-0.2	1/4xVLC0	Typ+0.2	V
LCD Driver Output Impedance	RLO	VLCD = 3.0V	–	5	10	kΩ
LCD Bias Dividing Resistor	RLCD1	1/4 bias, T_A = 25°C	7.5	10	12.5	kΩ
	RLCD2		38	50	62	
	RLCD3		60	80	100	
	RLCD4		180	240	300	

NOTE: It is middle output voltage when the VDD and the VLC0 node are connected.

25.26 TS characteristics

The specifications of the parameters are guaranteed by design.

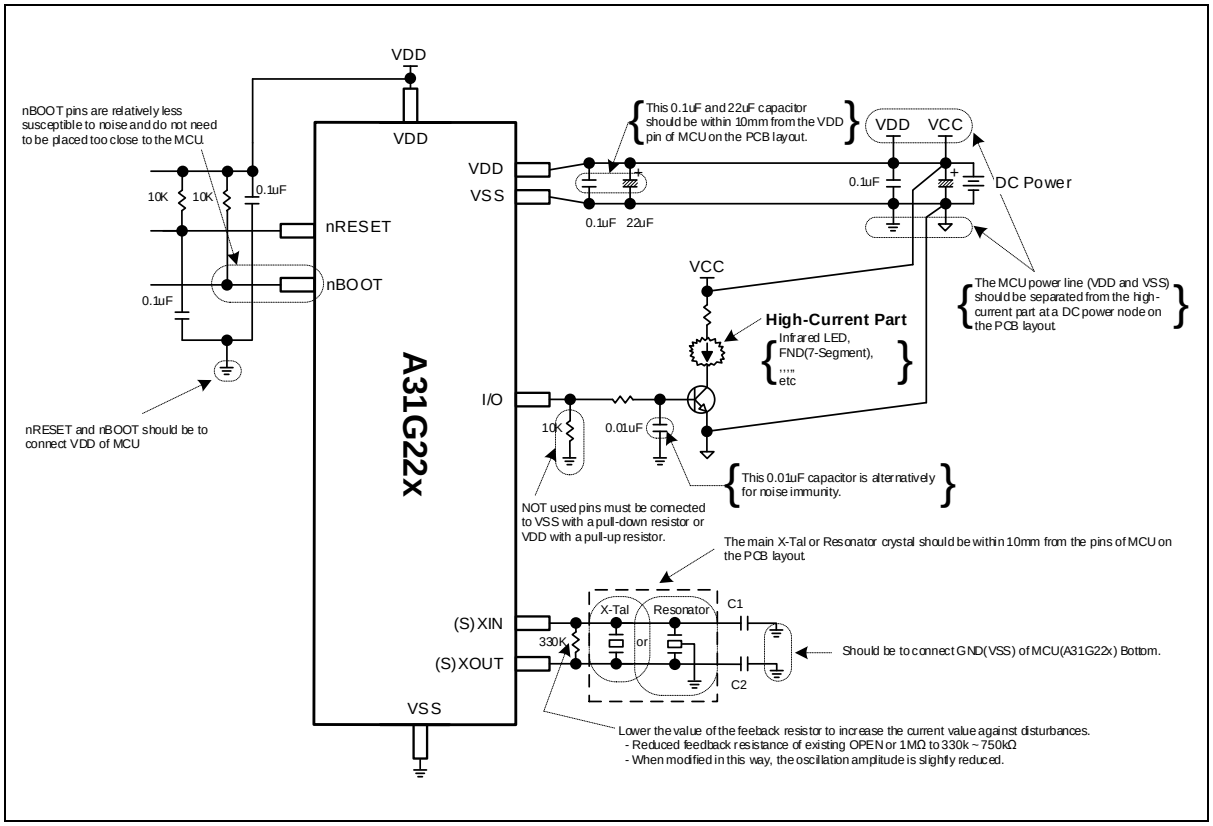
Table 75. Operating condition and characteristics of Temp Sensor

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating Voltage	V_{DD}	2.7	5.0	5.5	V
Sensing Temperature	T_S	-40	25	105	℃
Temperature Accuracy Error	$T_{SENSEACC}$	—	±10	—	℃

26 Recommended circuit and layouts

26.1 Recommended circuit layout

Figure 62. A31G22x recommended circuit layout



27 Development tools

27.1 Compiler

ABOV semiconductor does not provide any compiler for A31G22x. However, since A31G22x have ARM's high-speed 32-bit Cortex-M0+ Cores for their CPU, you can use all kinds of third party's standard compiler such as Keil C Compiler. These compilers' output debug information can be integrated with our A-Link and A-Link Pro. Please visit our website www.abovsemi.com for more information regarding the A-Link and A-Link Pro.

27.2 Debugger

The A-Link and A-Link Pro support ABOV Semiconductor's A31G22x MCU emulation in SWD Interface. The A-Link and A-Link Pro use two wires interfacing between PC and MCU, which is attached to user's system. The A-Link and A-Link Pro can read or change the value of MCU's internal memory and I/O peripherals. In addition, the A-Link and A-Link Pro control MCU's internal debugging logic. This means A-Link and A-Link Pro control emulation, step run, monitoring and many more functions regarding debugging.

The A-Link and A-Link Pro run underneath MS operating system such as MS-Windows NT/ 2000/ XP/ Vista/ 7/ 8/ 8.1/ 10 (32-bit, 64-bit).

Programming information using the A-Link and A-Link Pro are provided in Figure 63. More detailed information about the A-Link and A-Link Pro, please visit our website www.abovsemi.com and download the debugger S/W and documents.

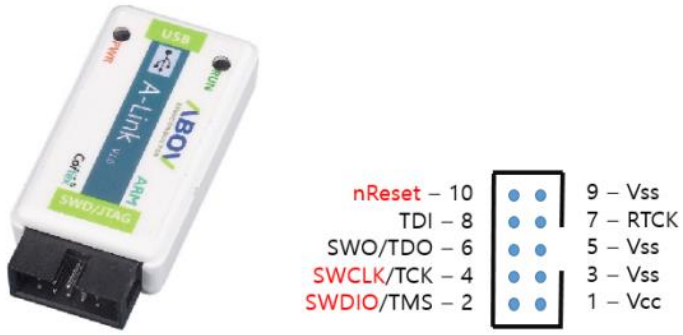


Figure 63. A-Link and Pin Descriptions

27.3 Programmer

27.3.1 E-PGM+

E-PGM+ is a single programmer, and allows a user to program on the device directly.

- Support ABOV devices
- 2~5 times faster than S-PGM+
- Main controller: 32-bit MCU @ 72MHz
- Buffer memory: 1MB

Figure 64. E-PGM+ (Single Writer) and Pin Descriptions

27.3.2 Gang programmer

E-Gang4 and E-Gang6 allows a user to program on multiple devices at a time. They run not only in PC controlled mode but also in standalone mode without PC control. USB interface is available and it is easy to connect to the handler.

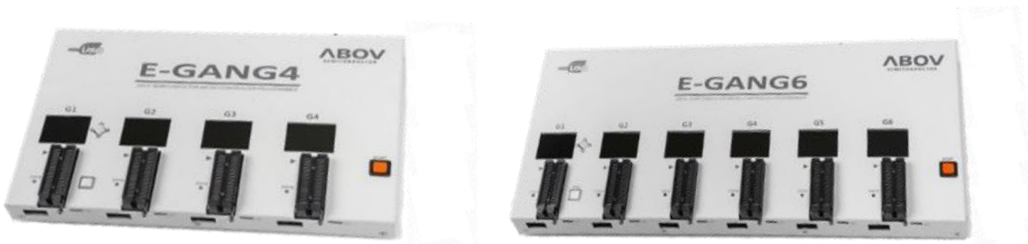


Figure 65. E-Gang4 and E-Gang6 (for Mass Production)

27.4 SWD debug mode and E-PGM+ connection

Connections for SWD debugger interface or EPGM+ is described in “Figure 10. Connection Diagram of E-PGM+ and SWD Port”.

28 Package information

This chapter provides A31G22x series package information.

28.1 80 LQFP (14x14) package information

Figure 66. 80 LQFP (14x14) Package

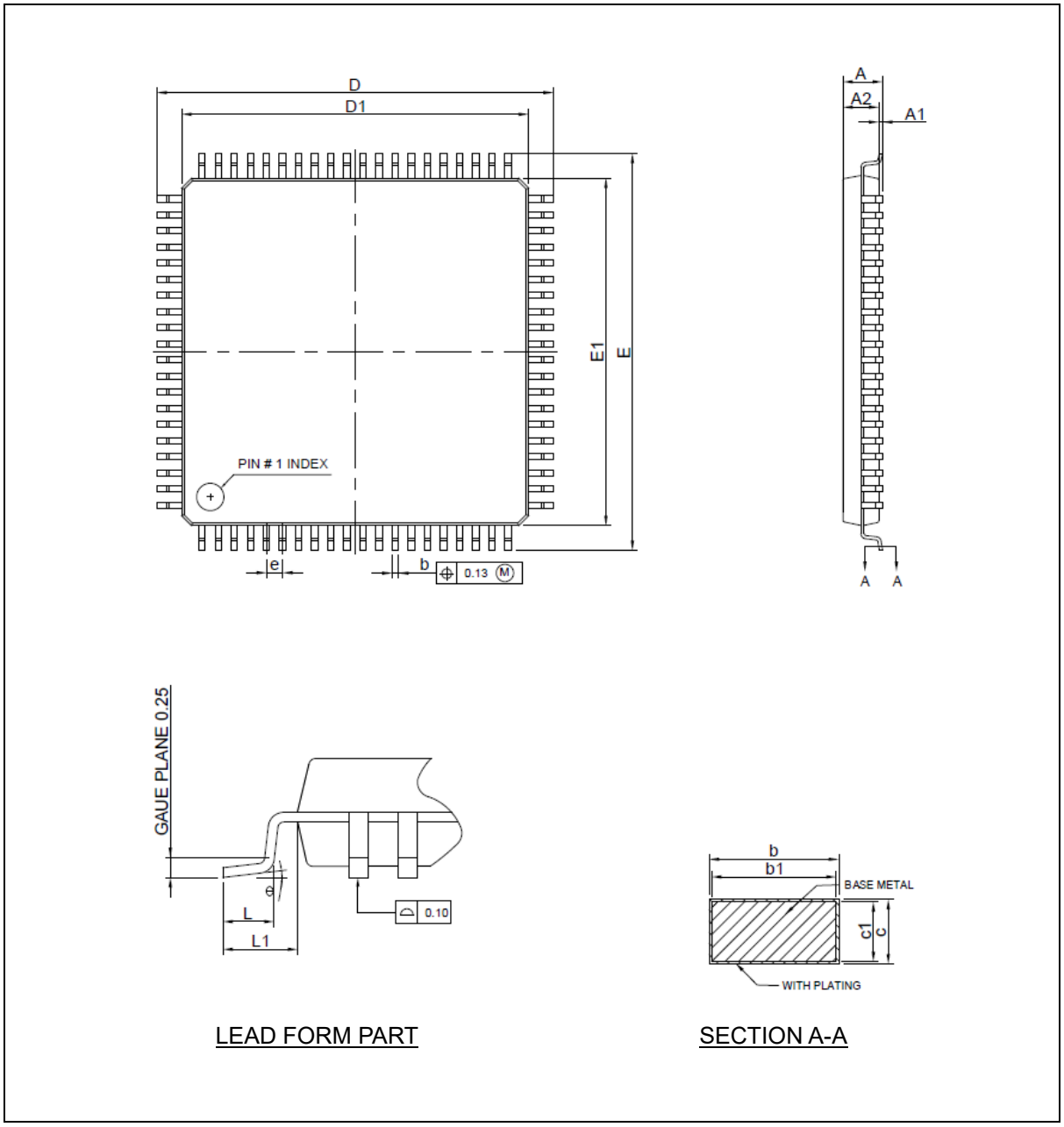


Table 76. 80 LQFP (14 x 14) Package Mechanical Data

Symbol	Dimension (mm)		
	Min.	Nom.	Max.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.22	0.32	0.38
b1	0.22	0.30	0.33
c	0.09	—	0.20
c1	0.09	—	0.16
D	15.80	16.00	16.20
D1	13.80	14.00	14.20
E	15.80	16.00	16.20
E1	13.80	14.00	14.20
e	0.65 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
Θ	0°	3.5°	7°

NOTES:

1. All dimensions refer to JEDEC standard MS-026-BEC.
2. Dimension ‘D1’ and ‘E1’ do not include mold protrusions. Allowable protrusion is 0.25mm per side. ‘D1’ and ‘E1’ are maximum plastic body size dimensions including mold mismatch.
3. Dimension ‘b’ does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum ‘b’ dimension by more than 0.08mm.
4. ‘A1’ is defined as the distance from the seating plane to the lowest point on the package body.

28.2 80 LQFP (12x12) package information

Figure 67. 80 LQFP (12x12) Package

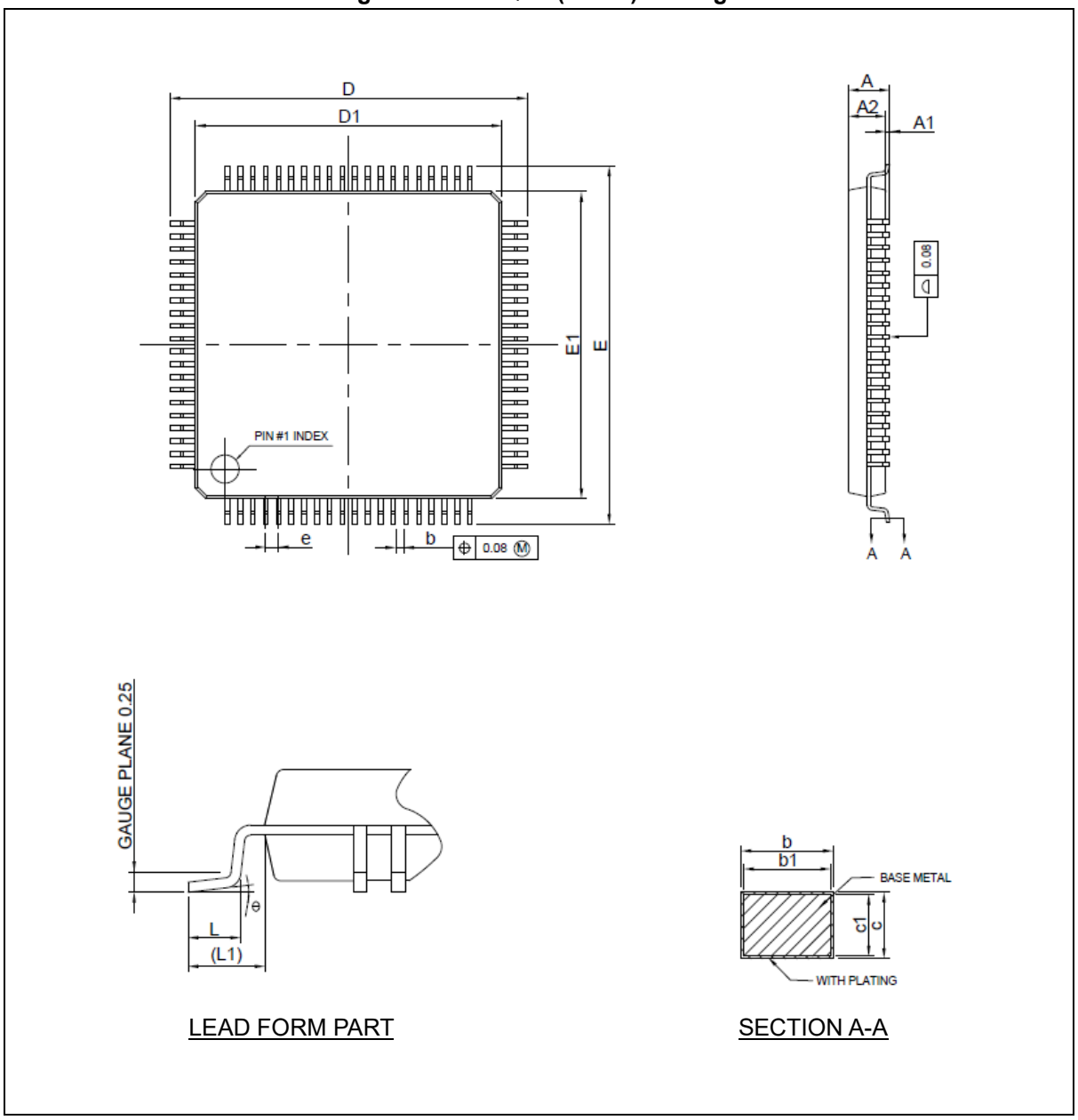


Table 77. 80 LQFP (12 x 12) Package Mechanical Data

Symbol	Dimension (mm)		
	Min.	Nom.	Max.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	—	0.20
c1	0.09	—	0.16
D	13.80	14.00	14.20
D1	11.80	12.00	12.20
E	13.80	14.00	14.20
E1	11.80	12.00	12.20
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
Θ	0°	3.5°	7°

NOTES:

1. All dimensions refer to JEDEC standard MS-026-BDD.
2. Dimension ‘D1’ and ‘E1’ do not include mold protrusions. Allowable protrusion is 0.25mm per side. ‘D1’ and ‘E1’ are maximum plastic body size dimensions including mold mismatch.
3. Dimension ‘b’ does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum ‘b’ dimension by more than 0.08mm.
4. ‘A1’ is defined as the distance from the seating plane to the lowest point on the package body.

28.3 64 LQFP (12x12) package information

Figure 68. 64 LQFP (12x12) Package Outline

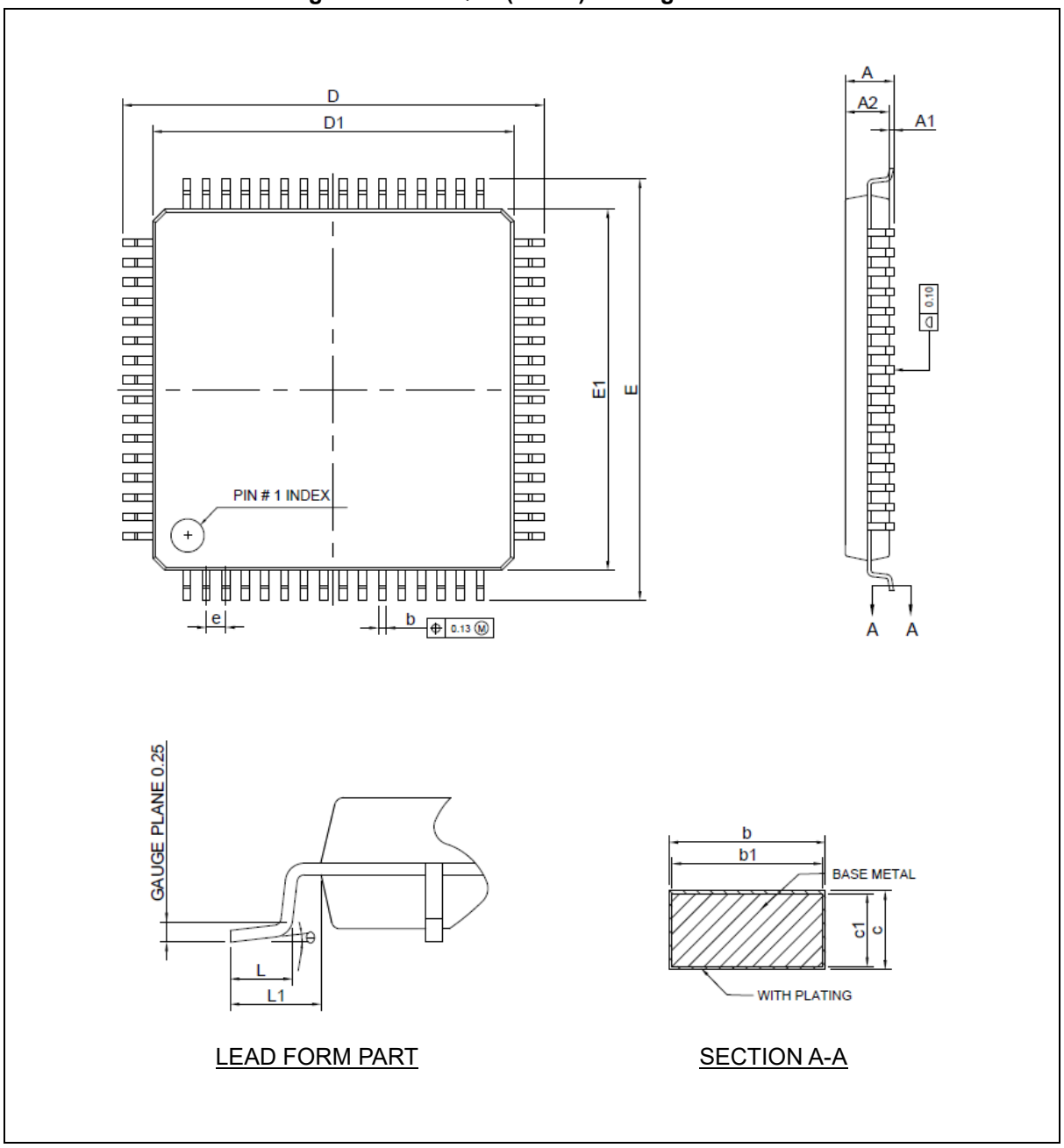


Table 78. 64 LQFP (12 x 12) Package Mechanical Data

Symbol	Dimension (mm)		
	Min.	Nom.	Max.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.22	0.32	0.38
b1	0.25	0.30	0.33
c	0.09	—	0.20
c1	0.09	—	0.16
D	13.80	14.00	14.20
D1	11.80	12.00	12.20
E	13.80	14.00	14.20
E1	11.80	12.00	12.20
e	0.65 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
Θ	0°	3.5°	7°

NOTES:

1. All dimensions refer to JEDEC standard MS-026-BDC.
2. Dimension ‘D1’ and ‘E1’ do not include mold protrusions. Allowable protrusion is 0.25mm per side. ‘D1’ and ‘E1’ are maximum plastic body size dimensions including mold mismatch.
3. Dimension ‘b’ does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum ‘b’ dimension by more than 0.08mm.
4. ‘A1’ is defined as the distance from the seating plane to the lowest point on the package body.

28.4 64 LQFP (10x10) package information

Figure 69. 64 LQFP (10x10) Package

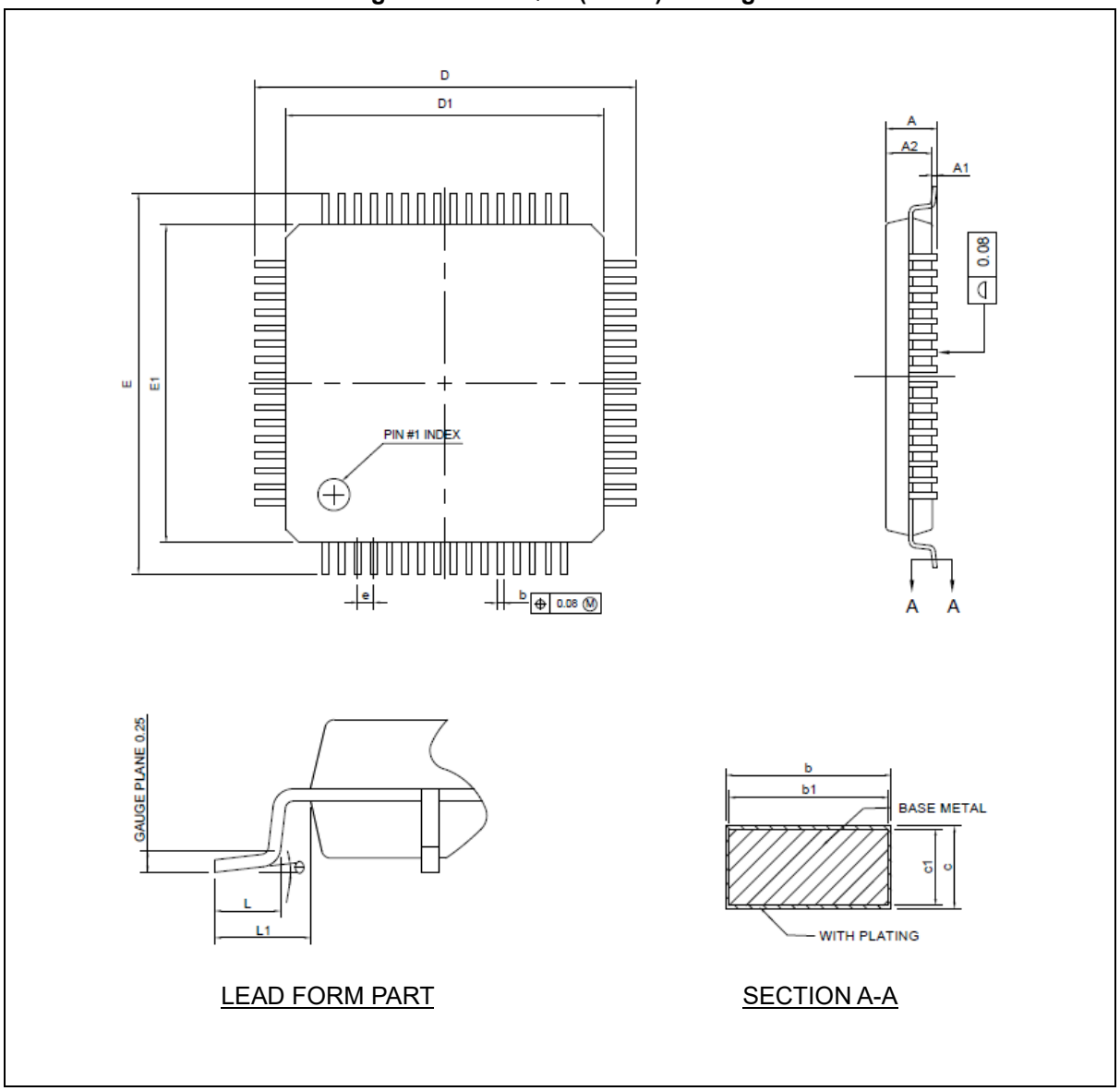


Table 79. 64 LQFP (10 x 10) Package Mechanical Data

Symbol	Dimension (mm)		
	Min.	Nom.	Max.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	—	0.20
c1	0.09	—	0.16
D	11.80	12.00	12.20
D1	9.80	10.00	10.20
E	11.80	12.00	12.20
E1	9.80	10.00	10.20
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
Θ	0°	3.5°	7°

NOTES:

1. All dimensions refer to JEDEC standard MS-026-BCD.
2. Dimension ‘D1’ and ‘E1’ do not include mold protrusions. Allowable protrusion is 0.25mm per side. ‘D1’ and ‘E1’ are maximum plastic body size dimensions including mold mismatch.
3. Dimension ‘b’ does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum ‘b’ dimension by more than 0.08mm.
4. ‘A1’ is defined as the distance from the seating plane to the lowest point on the package body.

28.5 48 LQFP (7 x 7) package information

Figure 70. 48 LQFP (7 x 7) Package

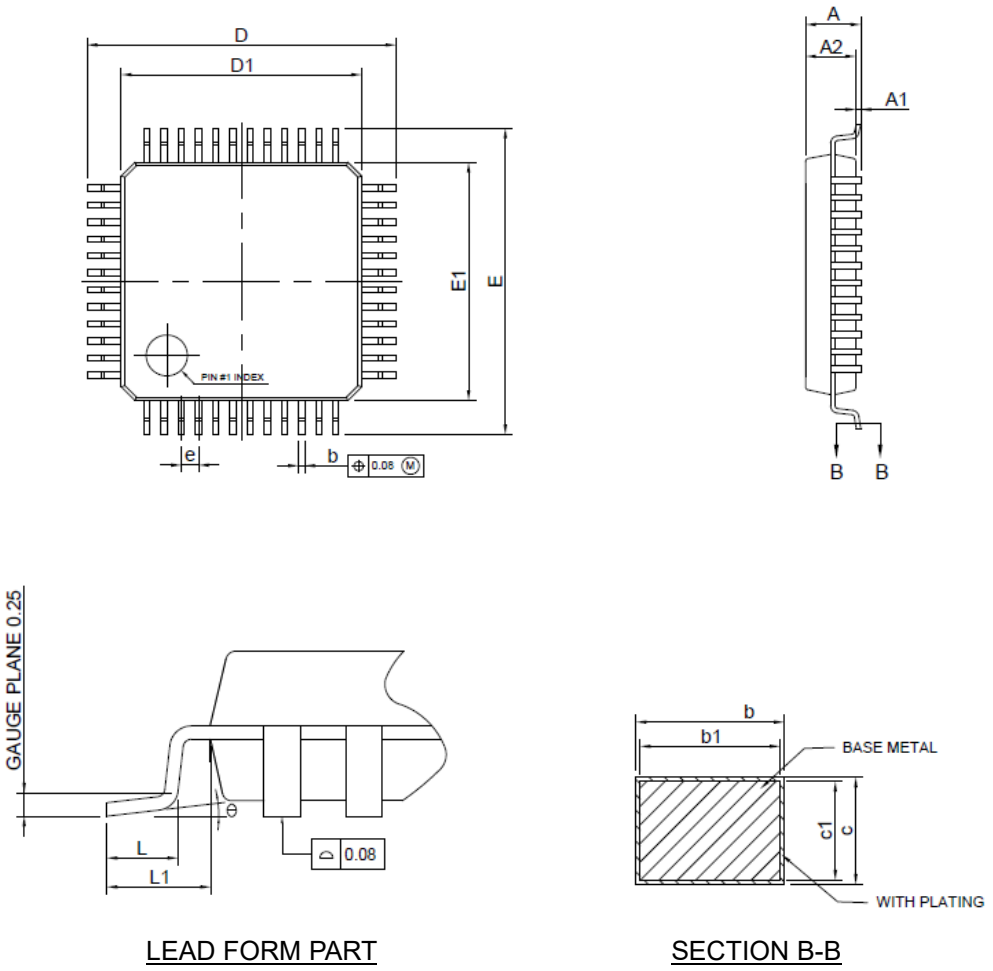


Table 80. 48 LQFP (7 x 7) Package Mechanical Data

Symbol	Dimension (mm)		
	Min.	Nom.	Max.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	—	0.20
c1	0.09	—	0.16
D	8.80	9.00	9.20
D1	6.80	7.00	7.20
E	8.80	9.00	9.20
E1	6.80	7.00	7.20
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
Θ	0°	3.5°	7°

NOTES:

1. All dimensions refer to JEDEC standard MS-026-BBC.
2. Dimension ‘D1’ and ‘E1’ do not include mold protrusions. Allowable protrusion is 0.25mm per side. ‘D1’ and ‘E1’ are maximum plastic body size dimensions including mold mismatch.
3. Dimension ‘b’ does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum ‘b’ dimension by more than 0.08mm.
4. ‘A1’ is defined as the distance from the seating plane to the lowest point on the package body.

29 Ordering information

Table 81. A31G22x Device Ordering Information

Device name	Code Flash [KB]	Data Flash [KB]	SRAM [KB]	I2C [ch]	UART [ch]	USART [ch]	SPI [ch]	TIMER [ch]	PWM [ch]	12-bit ADC [ch]	LCD Driver [COM x SEG]	I/O ports [ch]	Op. Temp. [℃]	Package Type
A31G226ML2N	256	32	20	3	2	4	2	7(16bit)/ 2(32bit)	3	18	8 x 37 or 3 x 42	75	-40 ~105	80LQFP12
A31G226MM2N*	256	32	20	3	2	4	2	7(16bit)/ 2(32bit)	3	18	8 x 37 or 3 x 42	75	-40 ~105	80LQFP14
A31G226RM2N*	256	32	20	3	2	3	2	7(16bit)/ 2(32bit)	3	18	8 x 29 or 3 x 34	59	-40 ~105	64LQFP12
A31G226RL2N*	256	32	20	3	2	3	2	7(16bit)/ 2(32bit)	3	18	8 x 29 or 3 x 34	59	-40 ~105	64LQFP10
A31G226CL2N*	256	32	20	2	2	2	2	7(16bit)/ 2(32bit)	3	14	8 x 21 or 3 x 26	43	-40 ~105	48LQFP7
A31G224MM2N*	128	32	20	3	2	4	2	7(16bit)/ 2(32bit)	3	18	8 x 37 or 3 x 42	75	-40 ~105	80LQFP14
A31G224ML2N*	128	32	20	3	2	4	2	7(16bit)/ 2(32bit)	3	18	8 x 37 or 3 x 42	75	-40 ~105	80LQFP12
A31G224RM2N*	128	32	20	3	2	3	2	7(16bit)/ 2(32bit)	3	18	8 x 29 or 3 x 34	59	-40 ~105	64LQFP12
A31G224RL2N	128	32	20	3	2	3	2	7(16bit)/ 2(32bit)	3	18	8 x 29 or 3 x 34	59	-40 ~105	64LQFP10
A31G224CL2N*	128	32	20	2	2	2	2	7(16bit)/ 2(32bit)	3	14	8 x 21 or 3 x 26	43	-40 ~105	48LQFP7
A31G226MLN*	256	32	20	3	2	4	2	7(16bit)/ 2(32bit)	3	18	8 x 37 or 3 x 42	75	-40 ~85	80LQFP12
A31G226MMN*	256	32	20	3	2	4	2	7(16bit)/ 2(32bit)	3	18	8 x 37 or 3 x 42	75	-40 ~85	80LQFP14
A31G226RMN*	256	32	20	3	2	3	2	7(16bit)/ 2(32bit)	3	18	8 x 29 or 3 x 34	59	-40 ~85	64LQFP12
A31G226RLN*	256	32	20	3	2	3	2	7(16bit)/ 2(32bit)	3	18	8 x 29 or 3 x 34	59	-40 ~85	64LQFP10
A31G226CLN*	256	32	20	2	2	2	2	7(16bit)/ 2(32bit)	3	14	8 x 21 or 3 x 26	43	-40 ~85	48LQFP7
A31G224MMN*	128	32	20	3	2	4	2	7(16bit)/ 2(32bit)	3	18	8 x 37 or 3 x 42	75	-40 ~85	80LQFP14
A31G224MLN*	128	32	20	3	2	4	2	7(16bit)/ 2(32bit)	3	18	8 x 37 or 3 x 42	75	-40 ~85	80LQFP12
A31G224RMN*	128	32	20	3	2	3	2	7(16bit)/ 2(32bit)	3	18	8 x 29 or 3 x 34	59	-40 ~85	64LQFP12
A31G224RLN*	128	32	20	3	2	3	2	7(16bit)/ 2(32bit)	3	18	8 x 29 or 3 x 34	59	-40 ~85	64LQFP10
A31G224CLN*	128	32	20	2	2	2	2	7(16bit)/ 2(32bit)	3	14	8 x 21 or 3 x 26	43	-40 ~85	48LQFP7

: For available options for further information on the device with a '' mark, please contact the ABOV Sales Offices.

Figure 71. A31G22x Device Numbering Nomenclature

A31G226 Device Nomenclature

A31G22 6 M L 2 N (T)

A31G22x Family Name

Code Memory Size

6	256 Kbytes
4	128 Kbytes

Pin Count

M	80 pin
R	64 pin
C	48 pin

Package type

L	LQFP1	0.5mm pin pitch
M	LQFP2	0.65mm pin pitch

Temperature

None	-40℃ ~ 85℃
2	-40℃ ~ 105℃

Product Information

N	Internal management code

Packing

None	Tray
(W)	Wafer
(C)	Chip Carrier

Revision history

Date	Revision	Description
Dec. 22, 2020	1.00	First release.
Jan. 11, 2021	1.01	The symbol and unit of conversion frequency ratio in Table 68. ADC Electrical Characteristics have been modified.
Feb. 02, 2021	1.02	Modified the descriptions in 1.1
Apr. 02, 2021	1.03	Updated the number of channels of LCD driver
Jul. 12, 2021	1.04	Modified typo 'I_{OL3}' to 'I_{OL7}' of V_{OL7} and added notification to Table 30
Jul. 12, 2021	1.05	Removed Figure 43. Removed AVREF signal in Figure 1, Figure 2, Figure 3.
Aug. 10, 2021	1.06	Modified the terminology, block diagram and descriptions of the Temp Sensor chapter.
Aug. 24, 2021	1.07	Modified the 'Figure 62. A31G22x recommended circuit layout'
Oct. 5, 2021	1.08	Corrected typo of Figure 8 and Table 1 Corrected the terminology of operating modes.
Nov. 23, 2021	1.09	Updated that SEG5 and SEG6 pins for LCD driver control are not supported. - Modified Features: LCD Driver 80-pin - Modified Figure 4, Figure 6 - Modified Table1, Table2, Table 3, Table 15, Table 29 - Modified the description of Features and Ch 22 - Modified Table 81 Updated Figure 45 Updated Figure 71 Corrected Typo - 4.4.1, 4.4.4
Dec. 14, 2021	1.10	Updated Figure 62 Modified The start-up time of HSE Characteristics from Typ. 200 ms to Typ. 2 ms. Modified Stabilization time of HSI characteristics from Max. 100 us to Min. 100 us. Updated Figure 35 Modified Table 16 and Table 17 Changed the titles from 'CRC and Checksum' to 'CRC' because CRC checksum is not supported. Added the notification and pull-up state of PC1, PC2 pin in Table 3. Updated Figure 43 LCD block diagram and added notifications. Modified the description of 4.4 Corrected typo
Aug. 24, 2021	1.11	Modified the Table 15 USART13_RXD13 -> USRAT13_TXD13, USART13_TXD13 -> USART13_RXD13 Removed RTC function
Nov. 04, 2022	1.12	Revision the font of this document
Jan. 18. 2023	1.13	- Modified "Table 125. I/O static characteristics" I/O pin capacitance

		to max. 10pF. -Change pull-up min/max value in Table 50. I/O static characteristics
Dec. 02, 2024	1.14	Updated the disclaimer.

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