A31C14x Datasheet

Cortex®-M0+ 32-bit Microcontroller, 32 MHz, Up to 128 KB Code Flash, 8 KB SRAM, 12-bit ADC

DS Rev. 1.03

Features

Core

- Arm® 32-bit Cortex®-M0+ Core
- Maximum operating frequency 32 MHz

Memory

- Up to 128 KB code flash memory
- 8 KB SRAM

Reset and Power Management

- Power-on/power-down reset (POR/LVR/LVI)
- Low-power modes: SLEEP, DEEP-SLEEP (STOP1, STOP2)

Clock Management

- High-Speed Internal Oscillator 32 MHz (HSI)
  - ±1.5% @ 0°C to +60°C
  - ±3.0% @ -40°C to +85°C
  - ±4.0% @ -40°C to +105°C
- Low-Speed Internal Oscillator 32 kHz (LSI)
  - ±10% @ 0°C to +60°C, V_{DD} = 3.0 V
  - ±30% @ −40°C to +85°C, V_{DD} = 3.0 V
- High-Speed External Oscillator (HSE, main oscillator)
  - 4 MHz to 12 MHz
- Low-Speed External Oscillator (LSE, sub-oscillator)
  - 32.768 kHz

GPI/O

- Up to general-purpose 62 I/O pins with interrupt capability
- All mappable on external interrupt vectors
- Multi-function pins capable of selection for up to six different functions, including GPIO

DMA Controller

- 6-channel DMAs
- 8-/16-/32-bit data transfers
- Operates in conjunction with seven types of peripherals

WDT

- 32-bit down-count timer
- Reset and periodic interrupts
- Eight types of prescaler

FRT

- 32-bit free-run timer

16-bit Timer

- Up to 10 channels
  - 10-input capture and output channels
- Timer operating modes:
  - Periodic timer mode
  - One-shot mode
  - PWM mode
  - Capture mode
- 10-bit prescaler

Serial Interfaces

- UART
  - Up to two 16450 asynchronous serial communication ports
- USART
  - Up to three synchronous serial communication port
- I2C
  - Up to three communication port

ADC

- One independent ADC block
- Up to 18-channel of analog inputs
- Multiple operating modes:
  - Single conversion
  - Sequence conversion
  - Burst conversion
  - Multiple conversion

Comparator

- Two Comparators

CRC Calculation Unit

- CRC operating modes:
  - CRC32 (0x04C1_1DB7)
  - CRC16-USB (0x8005)
  - CRC16-CCITT (0x1021)
  - CRC8-CCITT (0x07)
- Support for byte reversal of input/output data
- Compatible with DMA

Operating Voltages

- 1.8 V to 5.5 V

Operating Temperature

- Commercial grade (−40°C to +85°C)
- Industrial grade (−40°C to +105°C)

Development Support

- Serial Wire Debug (SWD) interface

Packages

- 64-LQFP-1010 (0.5 mm pitch)
- 64-LQFP-1414 (0.8 mm pitch)
- 48-LQFP-0707 (0.5 mm pitch)
- 48-QFN-0707 (0.5 mm pitch)
- 48-QFN-0606 (0.4 mm pitch)
- 44-LQFP-1010 (0.8 mm pitch)
- 32-QFN-0505 (0.5 mm pitch)
- 28-TSSOP
- 20-TSSOP
- 20-QFN

Family Devices

- A31C144: Flash 128 KB, SRAM 8 KB
- A31C143: Flash 64 KB, SRAM 8 KB

Applications

- General purpose

Product Selection Table

Table 1. Device Summary

Part Number	Flash	SRAM	USART	UART	I2C	CMP	ADC	TIMER	I/O Port	Package
A31C144RLN	128KB	8KB	3	2	3	2	18	10	62	64-LQFP-1010
A31C144RL2N*	128KB	8KB	3	2	3	2	18	10	62	64-LQFP-1010
A31C144RN2N*	128KB	8KB	3	2	3	2	18	10	62	64-LQFP-1414
A31C144CLN*	128KB	8KB	2	2	2	2	15	10	46	48-LQFP-0707
A31C144CUN*	128KB	8KB	2	2	2	2	15	10	46	48-QFN-0707
A31C144CYN*	128KB	8KB	2	2	2	2	15	10	46	48-QFN-0606
A31C144SNN*	128KB	8KB	2	2	2	2	13	10	42	44-LQFP-1010
A31C144SN2N*	128KB	8KB	2	2	2	2	13	10	42	44-LQFP-1010
A31C144KYN*	128KB	8KB	2**	1	2	2	13	10	30	32-QFN-0505
A31C144GRN*	128KB	8KB	2**	1	2	0	9	10	26	28-TSSOP
A31C143RLN*	64KB	8KB	3	2	3	2	18	10	62	64-LQFP-1010
A31C143CLN*	64KB	8KB	2	2	2	2	15	10	46	48-LQFP-0707
A31C143CYN*	64KB	8KB	2	2	2	2	15	10	46	48-QFN-0606
A31C143SNN*	64KB	8KB	2	2	2	2	13	10	42	44-LQFP-1010
A31C143KYN*	64KB	8KB	2**	1	2	2	13	10	30	32-QFN-0505
A31C143GRN*	64KB	8KB	2**	1	2	0	9	10	26	28-TSSOP
A31C143FUN*	64KB	8KB	1	1	2	0	8	10	18	20-QFN-0404
A31C143FRN*	64KB	8KB	1	1	2	0	8	10	18	20-TSSOP

* For available options or further information on the device with "*" marks, please contact the ABOV sales offices.

** UART: 2, SPI: 1

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1. Introduction

This document provides an overview of the features supported by A31C14x series, including high-level information and brief explanations of each feature.

Refer to Table 3 for the list of features supported by the A31C14x series.

2. Descriptions

The A31C14x series is a high-performance and energy-efficient 32-bit microcontroller series based on Arm Cortex-M0+ core, with up to 128 KB of flash memory and 8 KB of SRAM.

2.1 Product Category Definition

Table 2 provides an overview of the memory capacity for available devices in the A31C14x series.

This document provides an overview of the features supported by each device, including high-level information and brief explanations for each feature.

Refer to Table 3 for the list of features supported by product category.

Table 2. A31C14x Series Memory Capacity

Device	Memory Capacity	
	Flash	RAM
A31C144	128 KB	8 KB
A31C143	64 KB	8 KB

2.2 Device Overview

Table 3 summarizes and lists the features specific to the device in the A31C14x series while considering the largest package.

Table 3. A31C14x Series Features

Peripheral		Description
Core	CPU	• Max. operating frequency: 32 MHz • 32-bit Arm Cortex-M0+ Core • Register settings in CPU: - Uses general-purpose registers specified by the 32-bit Thumb instruction set: R0-R12 - Main Stack Pointer (MSP) and Process Stack Pointer (PSP): R13 - Link Register (LR): R14 - Program Counter (PC): R15 • Data alignment in little-endian • Von Neumann Architecture • AHB/APB
	Interrupt	• NVIC (Nested-Vectored Interrupt Controller) • Up to 32 peripheral interrupts available. • 2-bit width of group priority: four levels of priority
Memory	Code Flash	• Capacity: - A31C144: 128 KB - A31C143: 64 KB • Erase unit: Page (512 bytes), sector (2 KB) or bulk (full chip) • Program unit: Word (4 bytes) • Read-Protection • Self-programming • CRC code generation and verification for the flash memory • Endurance: - A31C144: Page 0 to 251 (126 KB): 10,000 cycles Page 252 to 255 (2 KB): 100,000 cycles - A31C143: Page 0 to 123 (62 KB): 10,000 cycles Page 124 to 127 (2 KB): 100,000 cycles • Lifetime: 10 years

Table 3. A31C14x Series Features (continued)

Peripheral		Description
Memory	Boot ROM	• Initiating the microcontroller's boot mode by receiving an external input signal at the nBOOT pin • UART mode of USART10 • In-system programming • Users can store information in the internal flash memory by using an application board to write data to the memory.
	SRAM	• Capacity: 8 KB • Capable of functioning as a program's working area • High-speed execution for time-critical codes • Capability to remap into an interrupt vector area
System Control Unit (SCU)	Operating frequency	Up to 32 MHz
	Clock	• High-Speed Internal (HSI) oscillator: 32 MHz - ±1.5% @ 0°C to +60°C - ±3.0% @ −40°C to +85°C - ±4.0% @ −40°C to +105°C • Low-Speed Internal Oscillator (LSI): 32 kHz - ±10% @ 0°C to +60°C, V_{DD} = 3.0 V - ±30% @ −40°C to +85°C, V_{DD} = 3.0 V • High-Speed External (HSE) main oscillator: 4 MHz to 12 MHz • Low-Speed External (LSE) sub-oscillator: 32.768 kHz
	Clock monitoring	• System Fail-Safe function by clock monitoring - High-Speed External (HSE) main oscillator - Low-Speed External (LSE) sub-oscillator - Main system clock (MCLK)
	Operation mode	• RUN mode • SLEEP mode • DEEP-SLEEP (STOP1, STOP2) mode
	Reset	• nRESET Pin reset (PC9) • Core reset • Software reset • POR (Power-On Reset) • LVR (Low Voltage Reset) • WDTR (Watchdog Timer Reset) • Reset due to clock oscillating error
	POR	POR generator: Capable of generating a reset signal by detecting an internal 1.48 V

Table 3. A31C14x Series Features (continued)

Peripheral		Description
SCU (System Control Unit)	LVDI	• Four Low-voltage detection levels • Supports interrupts • Supports wake-up from DEEP-SLEEP mode
	Wake-up	• Wake-up by GPIO pin • Wake-up by FRT • Wake-up by WDT • Wake-up by LVI • Wake-up by USART
GPIO (General-Purpose I/O)		• Input/Output (I/O) port for general purpose • 64-LQFP - I/O pins: 62 • 48-LQFP, 48-QFN - I/O pins: 46 • 44-LQFP - I/O pins: 42 • 32-QFN - I/O pins: 30 • 28-TSSOP - I/O pins: 26 • Selectable input and output configuration for each pin: - Push-pull output - Open drain output - Input • Pin configurations through multiplexer settings • Configurable as an external interrupt source with the following options: - Rising-edge (high-level) - Falling-edge (low-level) - Edge-triggered (both rising-edge and falling-edge) • Configurable pull-up/down resistors and debouncing. • Configurable independently to be set or reset through its corresponding bit. • Wake-up events triggered by external asynchronous inputs.

Table 3. A31C14x Series Features (continued)

Peripheral		Description
DMA (Direct Memory Access) Controller		• Direct Memory Access (DMA) supporting peripherals - 6-channels • 8- /16- /32-bit data transfers • Operates in conjunction with 7 types of peripherals - UART0, UART1, USART10, USART11, USART12, CRC, ADC
Timer	16-bit Timer	• General-purpose 16-bit up-count timer • 10 channels - 10 input capture and output channels (TnIO) • Timer operating modes - Periodic timer mode - One-shot mode - PWM mode - Capture mode • Interrupt events - Timer/counter match interrupt - Timer overflow interrupt • Free selectable clock sources: - PCLK configurable through the peripheral clock enable register1 (SCU_PCER1) - LSI, LSE, MCLK, HSI, HSE configurable through the miscellaneous clock control register 3 (SCU_MCCR3) • Timer signals output through TnIO pins • 10-bit prescaler
	WDT (Watchdog Timer)	• 32-bit down-count timer • Reset and periodic interrupts • Free selectable clock sources: - LSI, LSE, HSI, HSE configurable through the miscellaneous clock control register 1 (SCU_MCCR1) • Selectable eight different prescalers
	FRT (Free-run Timer)	• 32-bit Free-run Timer - Timer for system time measurement - 32-bit up-count timer • Interrupt event - Period interrupt - Overflow interrupt

Table 3. A31C14x Series Features (continued)

Peripheral		Description
Serial Interface	UART	• Two channels of 16450 asynchronous serial communication ports • Configurable standard asynchronous communication bits (start, stop, and parity) • Flexible communication available through programming - 5- to 8-bit data transfers - Even/Odd/Non-parity generation and checking - 1-bit, 1.5-bit, or 2-bit stop-bit generation and checking • 8-bit fraction controller and 16-bit baud rate generator
	I2C	• Three channels of standard I2C communication protocol • Master and slave modes • 7-bit addressing for slave mode • Configurable SCL signal's high-/low-periods and SDA signal's hold time
	USART	• Three channels • Full-Duplex Operation • Asynchronous or Synchronous serial communication • 8-bit fraction controller and 16-bit baud rate generator • Flexible communication available through programming - 5- to 9-bit data transfers - Even-/Odd-/Non-parity generation and checking - 1-, 2-bit stop bit generation and checking • Receive Character Detection and Receive Time-Out function • Data overrun and Frame error detection • Three Separate Interrupts on TX Completion, TX Data Register Empty and RX Completion • Double Speed Asynchronous communication mode

Table 3. A31C14x Series Features (continued)

Peripheral	Description
12-bit ADC	• One unit of ADC block • 18 analog input channels • Multiple operating modes: - Single conversion - Sequence conversion - Burst conversion - Multiple conversion • Up to eight sequential conversions • Software triggers • internal trigger sources (timers)
Comparator	• Two internal comparators with two input sources. • Various input and reference sources are available.
CRC	• CRC operating modes: - CRC32 (0x04C1_1DB7) - CRC16_IBM (0x8005) - CRC16_CCITT (0x1021) - CRC8_CCITT (0x07) • Support for byte reversal of input/output data • Compatible with DMA
Operating voltage	1.8 V to 5.5 V
Operating temperature	• Commercial grade (−40°C to +85°C) • Industrial grade (−40°C to +105°C)
Package	• 10 types of package options - 64-LQFP-1010 (0.5 mm pitch) - 64-LQFP-1414 (0.8 mm pitch) - 48-LQFP-0707 (0.5 mm pitch) - 48-QFN-0707 (0.5 mm pitch) - 48-QFN-0606 (0.4 mm pitch) - 44-LQFP-1010 (0.8 mm pitch) - 32-QFN-0505 (0.5 mm pitch) - 28-TSSOP - 20-QFN-0404 (0.5 mm pitch) - 20-TSSOP

Table 4. Summary of A31C14x Peripherals

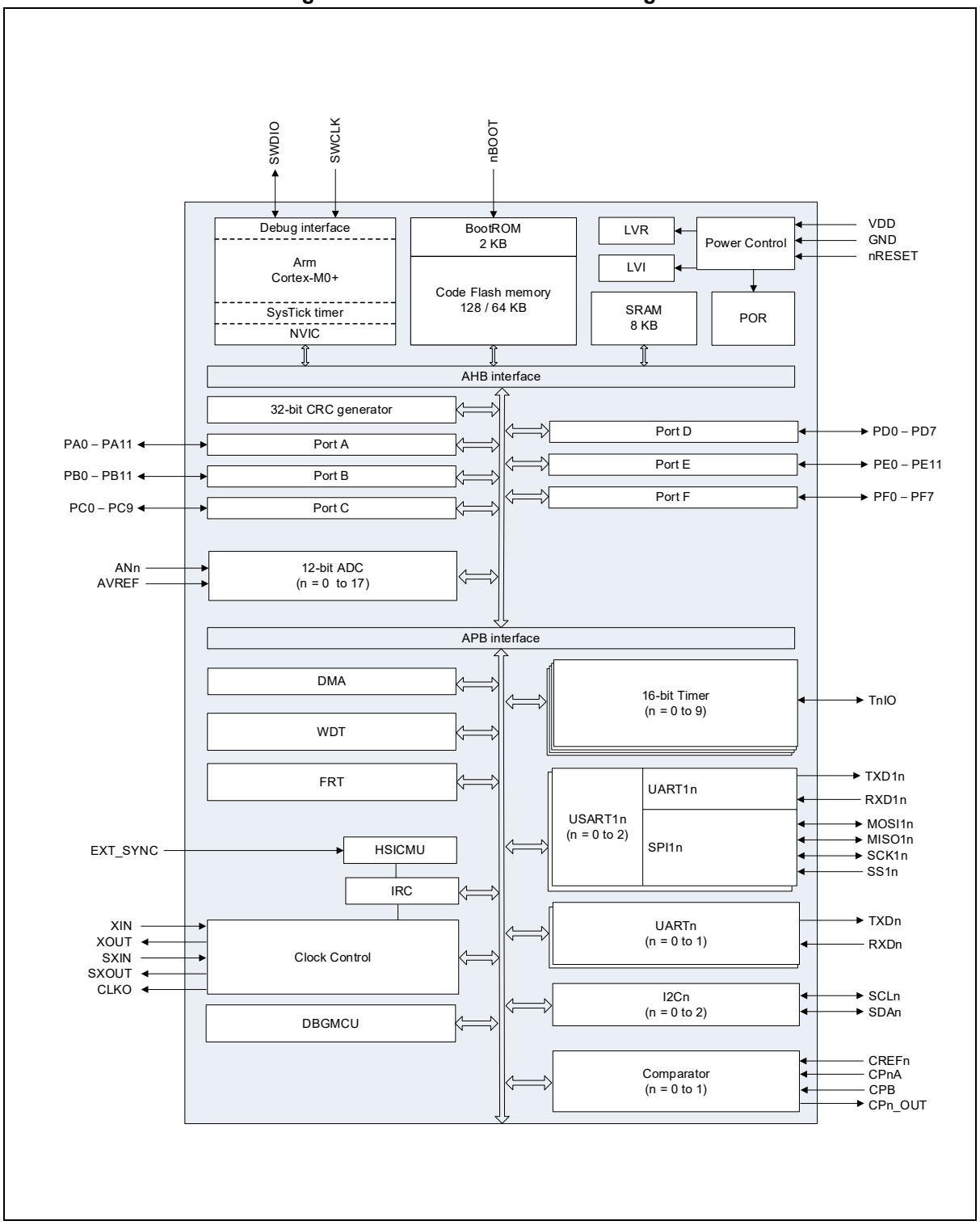
Peripheral		A31C14xRLN C144RL2N/RN2N	A31C14x CLN/CUN/ CYN	A31C14x SNN/SN2 N	A31C14x KYN	A31C14x GRN	A31C143 FRN/FUN
Core		Cortex-M0+ 32 MHz					
Code flash memory		128 KB / 64 KB					
SRAM		8 KB					
Timers	General purpose	10 (16-bit)					
	SysTick timer	1					
	WDT	1					
	FRT	1					
Communic ation Interfaces	UART	2	2	2	1	1	1
	I2C	3	2	2	2	2	2
	USART	3	2	2	2 (UART: 2, SPI: 1)		1
DMA		6					
GPIO		62	46	42	30	26	18
ADCs Number of channels		150 ksps					
		18	15	13	13	9	8
Comparator		2	2	2	2	0	0
CRC		1					
Operating Voltages		1.8 V to 5.5 V					
Operating Temperature		Ambient operating temperature: −40°C to +85°C/−40°C to +105°C (1)					
Packages		64-LQFP	48-LQFP/ 48-QFN	44-LQFP	32-QFN	28-TSSOP	20-TSSOP/ 20-QFN

NOTE:

1. The operating temperature range of -40°C to 105°C is supported only for the A31C144RL2N/RN2N/SN2N variant.

2.3 Block Diagram

Figure 1. A31C14x Series Block Diagram



2.4 Functional Overview

The following sections provide overviews of the features of the A31C14x series microcontroller.

2.4.1 Cortex-M0+ Core

The A31C14x series adopts the energy-efficient 32-bit microcontroller core, Cortex-M0+ of Arm, as its CPU. The Cortex-M0+, designed for low-power consumption, uses the ARMv6-M Instruction set to improve performance and energy efficiency.

Refer to the technical reference manual "ARM DDI 0484C" for detailed information on Cortex-M0+.

2.4.2 SRAM

The A31C14x series has a block of zero-wait on-chip SRAM. The size of the SRAM is 8KB. The base address is 0x2000_0000.

The SRAM memory area is commonly utilized for storing data and as a stack memory. It can also store program code for faster execution or during flash erase/programming operations.

2.4.3 Boot Configuration

The A31C14x series offers a boot mode for programming the internal Flash memory. The boot mode can be entered by setting the nBOOT pin to 'L' during the system reset process (the normal state is 'H').

The boot mode supports the UART boot, which uses the UART interface to transmit and receive boot data (TXD10/RXD10).

The pins for the boot mode are listed in Table 5.

Table 5. Boot Mode Pin List

Block	Pin Name	I/O	Pin Direction	Description
SYSTEM	nRESET	PC9	Input	Receive the reset signal
	nBOOT	PB3	Input	Set the boot mode
UART mode (USART10)	RXD10	PB1	Input	Receive the UART boot data
	TXD10	PB0	Output	Transmit the UART boot data

2.4.4 Power Supply

The device operates with a supply voltage of 1.8 V to 5.5 V (V_{DD}). The analog peripherals are also powered through V_{DD}, internally connected to AV_{DD} within the microcontroller.

Table 6. Power Supply

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	V_{DD}	1.8	5.5	V

During a power-up process, a reset plays an important role and affects the entire process of the system booting. The A31C14x series has two power-related reset options, as described below:

- POR_RST (Power-On Reset): Controls the voltage less than 1.48 V.
- LVD_RST (Low-Voltage Detect Reset): Controls the voltage of less than 1.70 V (default).

If the power level is higher than the POR and is below the flash operating voltage, the Code Read operation may malfunction. To prevent this abnormal Code Read operation, the LVD_RST generates the SYSRESETn internal signal, and the microcontroller enters the reset mode to prevent the abnormal operation. The minimum level that the LVR can set is 1.70 V, which meets the minimum flash operating voltage.

2.4.5 Operation Mode

2.4.5.1 Transition of Operation Mode

INIT mode is the initial state of the chip when a reset is asserted.

In RUN mode, the CPU operates at the maximum performance with the high-speed clock system.

SLEEP and DEEP-SLEEP modes can be used as low-power consumption modes. In the low-power consumption mode, power is effectively managed to reduce power consumption by halting the processor core and any unused peripherals.

2.4.5.2 RUN Mode

The CPU and peripheral hardware operate with a high-speed clock in RUN mode. After a reset, the system will enter RUN mode if the INIT state is detected.

2.4.5.3 SLEEP Mode

Once the microcontroller enters SLEEP mode, the CPU becomes inactive. By setting the SCU_PER and SCU_PCER registers, users can determine which peripherals will be inactive in SLEEP mode.

2.4.5.4 DEEP-SLEEP (STOP1, STOP2) Mode

The microcontroller enters DEEP-SLEEP mode when the core goes under the stop state using WFI instruction.

2.4.5.5 Reset Mode

The A31C14x series has two system reset options: a cold reset, which is effective during power-up or down sequences, and a warm reset, which is triggered by multiple reset sources.

The reset features of the A31C14x series are as follows:

- Power-On Reset (POR)
- Low-Voltage Detect Reset (LVR)
- nRESET pin reset
- Watchdog Timer (WDT) reset
- Software reset
- Clock oscillating error reset
- CPU request reset

2.4.6 Clocks and Start-Up

The A31C14x series has two main operating clocks: HCLK, which generates clock signals for the CPU and AHB system, and PCLK, which generates clock signals for peripheral systems.

2.4.6.1 HCLK Clock

The Cortex-M0+ core requires two clocks: HCLK and FCLK. While the HCLK supplies the clock for both the CPU and AHB, the FCLK remains enabled unless the system enters DEEP-SLEEP mode. Conversely, during SLEEP mode, the HCLK can be disabled while the FCLK continues to function.

The HCLK clocks the buses and memories. As the bus clock frequency is limited to a maximum of 32 MHz, the HCLK frequency must not exceed 32 MHz.

2.4.6.2 PCLK Clock

The PCLK can be used as a clock source for any peripheral. The SCU_PCER registers determine whether the PCLK is enabled or disabled for each peripheral. If a peripheral block's PCLK input is not enabled, its registers cannot be read. Additionally, it is important to note that the PCLK stops operating in DEEP-SLEEP mode.

2.4.6.3 Clock Configuration Procedure

After power on, HSI (4 MHz, 32 MHz/8) operates as a system clock by default. The HSI is enabled during the power-up sequence, and the HSE is configured by user controls with the HSI system clock.

Before enabling the HSE block, the pin mux for XIN and XOUT must be configured. During this process, avoiding affecting other bits of the PC_MR and PC_CR registers is important. After enabling the HSE block, it is necessary to wait for the crystal oscillation to be stabilized before proceeding.

The sub-oscillator, Low-Speed External (LSE, operating at 32.768 kHz) clock, can be enabled using the SCU_CSCR register (Clock Source Control Register). Like the HSE, the LSE must be enabled after configuring the pin mux for SXIN and SXOUT and allowing sufficient time for the oscillation to stabilize.

2.4.7 Interrupts and Events

2.4.7.1 NVIC (Nested Vectored-Interrupt Controller)

The A31C14x series includes up to 32 maskable interrupt sources that manage sixteen priority levels. The Nested Vector Interrupt Controller (NVIC) controls 16 interrupt lines of the Cortex-M0+.

The NVIC has the following advantages:

- Interrupt processing with reduced interrupt latency
- Direct transfer of Interrupt Vector Table (IVT) address to the core
- The fast interrupt processing capability
- Interrupts with higher priority precede those with lower priority, even if they occur after the lower priority interrupts.
- Automatic saving of processor state
- Interrupt restoring without instructional overhead at the end of the interrupt

The NVIC hardware block provides flexible and efficient interrupt management with minimal interrupt latency.

2.4.7.2 Extended Interrupt (EXTI)

The Extended Interrupt feature enables the system to generate event requests or wake up from STOP mode. Each external line can be configured independently to detect trigger events such as rising or falling edges or both edges and level events such as low or high.

2.4.8 GPIO

2.4.8.1 PCU Module

The A31C14x series has a Port Control Unit (PCU) module that controls the input and output (I/O) ports.

Users can configure the functionality, input/output direction, pull-up/pull-down, and debounce the pins for their applications by setting the PCU registers.

2.4.8.2 GPIO Module

Pins other than those specified as V_{DD}, GND, or for certain purposes can be used as General-Purpose Input/Output (GPIO) pins.

The GPIO module controls the general I/O pins. Output pins can be configured to output high- or low-level signals by setting the corresponding bits of the GPIO control register. On the other hand, the input status of logic input pins can be monitored through the control registers.

2.4.9 Embedded Flash Memory

The flash memory controller serves as an interface between the core and the embedded flash memory and is responsible for managing the data stored on the flash memory.

The flash memory of the A31C14x series has the following features:

- 128 KB or 64 KB of code flash memory with write protection bits.
- Erase units
  - Page (512 bytes)
  - Sector (2 KB)
  - Bulk (full chip)
- Program unit: Word (4 bytes)
- Zero wait (less than 27 MHz), 1- to 15-wait
- Code flash memory read protection
- Code flash memory write protection

2.4.10 HSICMU

The High-Speed Internal OSC Clock Management Unit (HSICMU) integrated into the A31C14x series is designed for the auto-trimming of the Internal OSC clock. The synchronization signal can also be derived from the LSE oscillator or HSE oscillator output, or it can be generated by user software.

The following are characteristics of the High-Speed Internal OSC Clock Management Unit (HSICMU) built in the A31C14x series.

- Selectable synchronization source with programmable prescaler and polarity:
  - HSE (4 MHz to 12 MHz)
  - LSE (32.768 kHz)
  - External pin (PB1)
- Possibility to generate synchronization pulses by software.
- Automatic oscillator trimming capability with no need for CPU action.
- 16-bit frequency error counter with automatic error value capture and reload
- Programmable limit for automatic frequency error value evaluation and status reporting

2.4.11 DMA Controller

The direct memory access (DMA) controller is used for high-speed data transfers between peripherals and memories. DMA allows quick data transfers by copying or moving data between memory locations or between memory and peripherals without involving the core.

The DMA has the following features:

- 6 channels
- 8-/16-/32-bit data transfers
- Multiple buffers of the same size
- Peripheral interrupts trigger DMA transfers

2.4.12 Timers

2.4.12.1 16-bit Timers

This 16-bit Timer supports four operating modes: Periodic Mode, PWM Mode, One-shot Mode, and Capture Mode.

Users can use a divided PCLK or an external clock as a clock source for the 16-bit Timer. An internal 10-bit prescaler allows to generate a variety of base clocks for the timer.

Interrupts can be triggered at regular intervals when the timer is used in Periodic Mode. Users can set the period and duty to form a PWM signal used in PWM Mode.

In One-shot Mode, the timer can generate one PWM waveform. The Capture Mode allows measuring the pulse intervals of an external input signal based on the predefined conditions. In addition, this timer can transmit signals to control other devices and is primarily used as a periodic tick timer or as a wake-up source.

2.4.12.2 FRT

The A31C14x series has one built-in 32-bit up count Free-run Timer (FRT). The FRT can operate with an overflow interrupt or a match interrupt based on its register settings and can remain active even in DEEP-SLEEP (STOP1, STOP2) mode.

2.4.12.3 WDT

The Watchdog Timer (WDT) detects errors in the microcontroller caused by external interference or unexpected, logical conditions. These errors cause the application program to deviate from its normal sequence. If the microcontroller loses control, the WDT will reset the microcontroller, allowing it to return to normal operation.

The WDT of the A31C14x series is a 32-bit down counter. If the WDT is set as a reset source, the microcontroller restarts when the down counter reaches zero.

When it is not used to monitor the microcontroller, the WDT can be used as a cycle timer along with an interrupt.

2.4.12.4 SysTick Timer

Although the SysTick timer is primarily designed for real-time operating systems, it can also be utilized as a standard down-counter.

The SysTick timer has the following features:

- 24-bit down-counter
- Automatic reload
- Maskable system interrupt generation when the counter reaches zero.
- Programmable clock source

2.4.13 UART

The built-in UART module allows users to specify settings for transmitting and receiving data and provides the ability to read the status of the UART. By providing information about the current state of transmission and reception processes, including types and conditions, the UART module enables users to monitor potential errors such as parity, overrun, framing, or break interrupts during data reception.

The UART module includes a programmable baud-rate generator for each channel, which generates an internal clock for its corresponding UART unit. This is achieved by dividing a prescaled clock using a baud-rate divisor ranging from 1 to 65,535, then dividing the result by 16.

Users can program interrupts that can control UART communication.

Furthermore, the built-in DMA allows the UART module to transfer data directly to or from memory without involving the CPU, reducing CPU usage, and increasing data transfer speed.

2.4.14 I2C

The I2C (Inter-integrated Circuit) interface built in the A31C14x series complies with the standard I2C communication protocol. It is used for serial communication between internal and external devices via the I2C protocol.

Equipped with one unit, it supports both master and slave modes and can transmit and receive data in bytes by using interrupts or polling.

The I2C interface of the A31C14x series operates in Standard mode (100 kHz) or Fast mode (400 kHz). In addition, it also supports General calls.

The I2C interface facilitates communication with multiple peripherals that share the same bus type. To utilize I2C, it is recommended to configure the SCL and SDA pins as open-drain and attach external pull-up resistors to ensure that their output signals are maintained in the 'High' state.

Table 7. Features of I2C

I2C features	I2C
7-bit addressing mode	O
Standard mode (up to 100 kbit/s)	O
Fast mode (up to 400 kbit/s)	O
General call	O

2.4.15 USART

Universal Synchronous and Asynchronous serial Receiver and Transmitter (USART) is a highly flexible serial communication device. The major features are listed below:

- Full-Duplex Operation. (Independent Serial Receive and Transmit Registers)
- Asynchronous or Synchronous Operation.
- Baud Rate Generator.
- Supports Serial Frames with 5,6,7,8, or 9 Data bits and 1 or 2 Stop bits.
- Odd or Even Parity Generation and Parity Check are Supported by Hardware.
- Data Over Run Detection.
- Framing Error Detection.
- Three Separate Interrupts on TX Completion, TX Data Register Empty and RX Completion.
- Double Speed Asynchronous communication mode.

Additional features are :

- 0% Error Baud Rate by floating point count register.
- Supports receive time out interrupt.
- Supports direct memory access and interrupt.

2.4.16 ADC

The A31C14x series features a 12-bit resolution Analog-to-Digital Converter (ADC) module. It consists of an independent controllable unit and A31C14x supports up to 18 different analog inputs. This ADC module supports AD conversion of multiple channels in different modes, including single mode, sequential mode, multiple mode, burst mode. It can sample the voltage inputs of multiple channels at critical times, which is required for various applications and can be achieved using the triggering functionality in association with TIMER.

Once the AD conversion is complete, the result is left aligned in 16-bit data registers.

The ADC is mapped to the AHB and capable of high-speed operation based on the internal clock source. In addition, it uses built-in DMA to reduce the microcontroller core load while enabling fast data sampling.

The analog input monitoring and comparison capabilities of the ADC allow the applications to determine whether the input voltage is above or below the predefined level.

2.4.17 Comparator

The A31C14x series has two comparators. The comparator can output the result of comparing two analog voltages via an I/O pin or by generating interrupts.

The comparator of the A31C14x series has the following features:

- Two built-in comparators
- Support two input sources.
  - CP0A, CP1A, CPB, Internal V_{DD} 1.0 V
  - CPRE0, CPRE1, Internal V_{DD} 1.0 V
- Control of the interrupt signal edges: either the falling or rising edge
- Noise filtering capability
- Four available hysteresis voltages (40 mV, 80 mV, 120 mV, and 160 mV)

2.4.18 CRC Module

The Cyclic Redundancy Check (CRC) module is used to calculate 32-bit, 16-bit IBM, 16-bit CCITT and 8-bit CCITT CRC codes from 8-bit or 32-bit data size. The user application can utilize CRC-based technologies to ensure the integrity of data transfers, storage, and flash memories in compliance with functional safety standards. With this module, users can verify the integrity of data transfers and flash memory.

Specifically, the CRC module of the A31C14x series supports DMA.

2.5 Development Support

This chapter describes the development support features of the device. The device provides standard Arm® development support, including toolchain compatibility, debug interface, trace support, and on-board debug/programming connection.

Refer to the feature list, pin description, and electrical characteristics for detailed information.

2.5.1 Toolchain Support

The device supports software development using standard Arm-compatible toolchains, including Arm® Keil® MDK, IAR Embedded Workbench® for Arm, and GCC-based toolchains.

Device-specific startup files, linker scripts, header files, and software examples are provided separately for each product series and software package.

2.5.2 Debug Interface

2.5.2.1 Serial Wire Debug Port (SW-DP)

The device provides an Arm® Serial Wire Debug Port (SW-DP) for software debugging and in-system flash memory programming. The SW-DP uses a two-pin debug interface, SWDIO and SWCLK, to access the CPU debug logic, memory, registers, and on-chip debug resources.

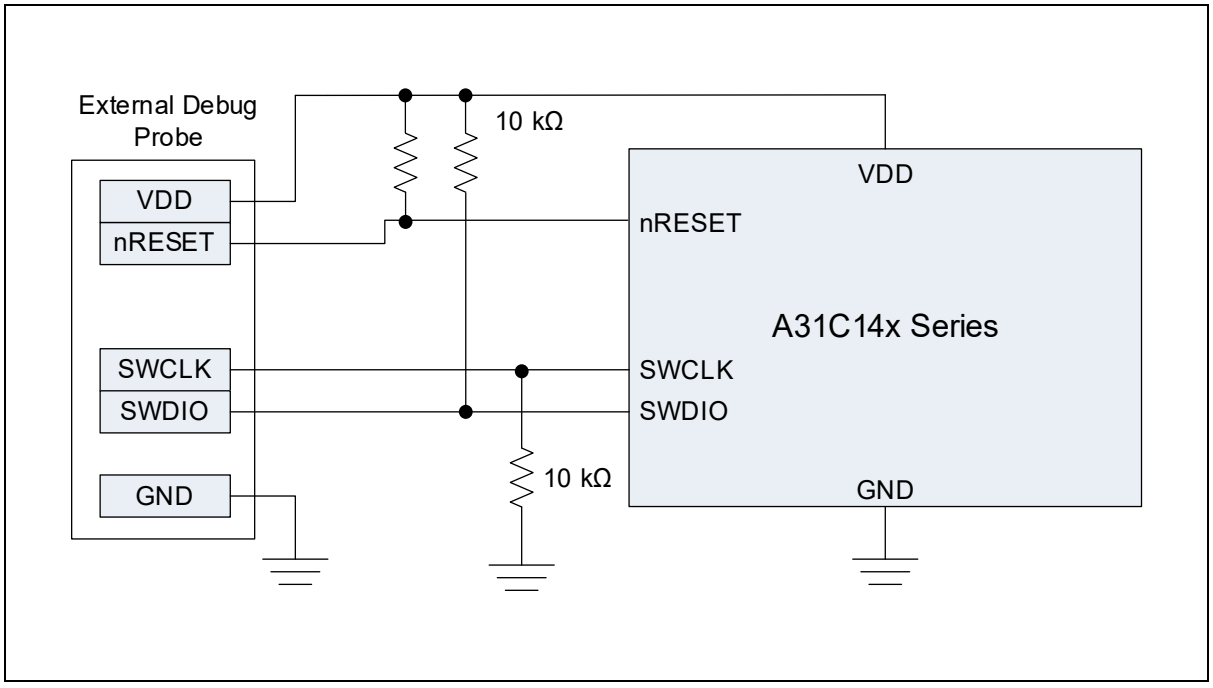
The SWD pins may be multiplexed with GPIO or other alternate functions depending on the product and package. If the SWD pins are used for application functions, the target board and firmware must be designed so that the pins remain accessible during debugging or programming.

2.5.2.2 SWD Connection Guide

For on-board debugging and programming, the target board should provide access to SWDIO, SWCLK, VDD, VSS, and nRESET. The nRESET connection is recommended to improve debug connection reliability and device recovery.

The VDD pin provides the target voltage reference for the external debug probe. It should be connected to the target board supply voltage unless otherwise specified by the debug probe manufacturer.

Figure 2. SWD Interface Connection



3. Pinouts and Pin Descriptions

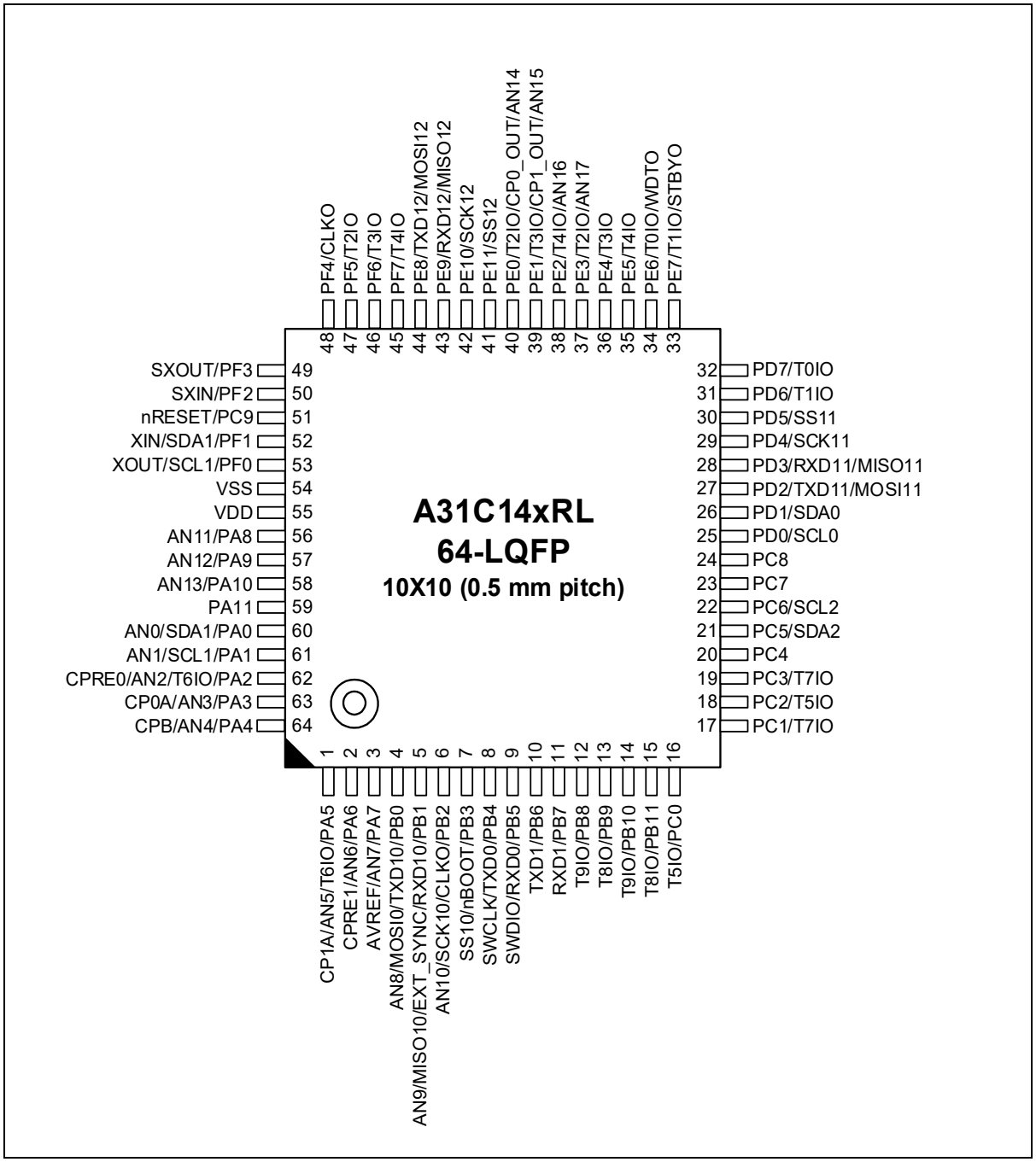
In this chapter, pinouts and pin descriptions of the A31C14x series are described.

3.1 Pinouts

The figures in this section show top views of the packages.

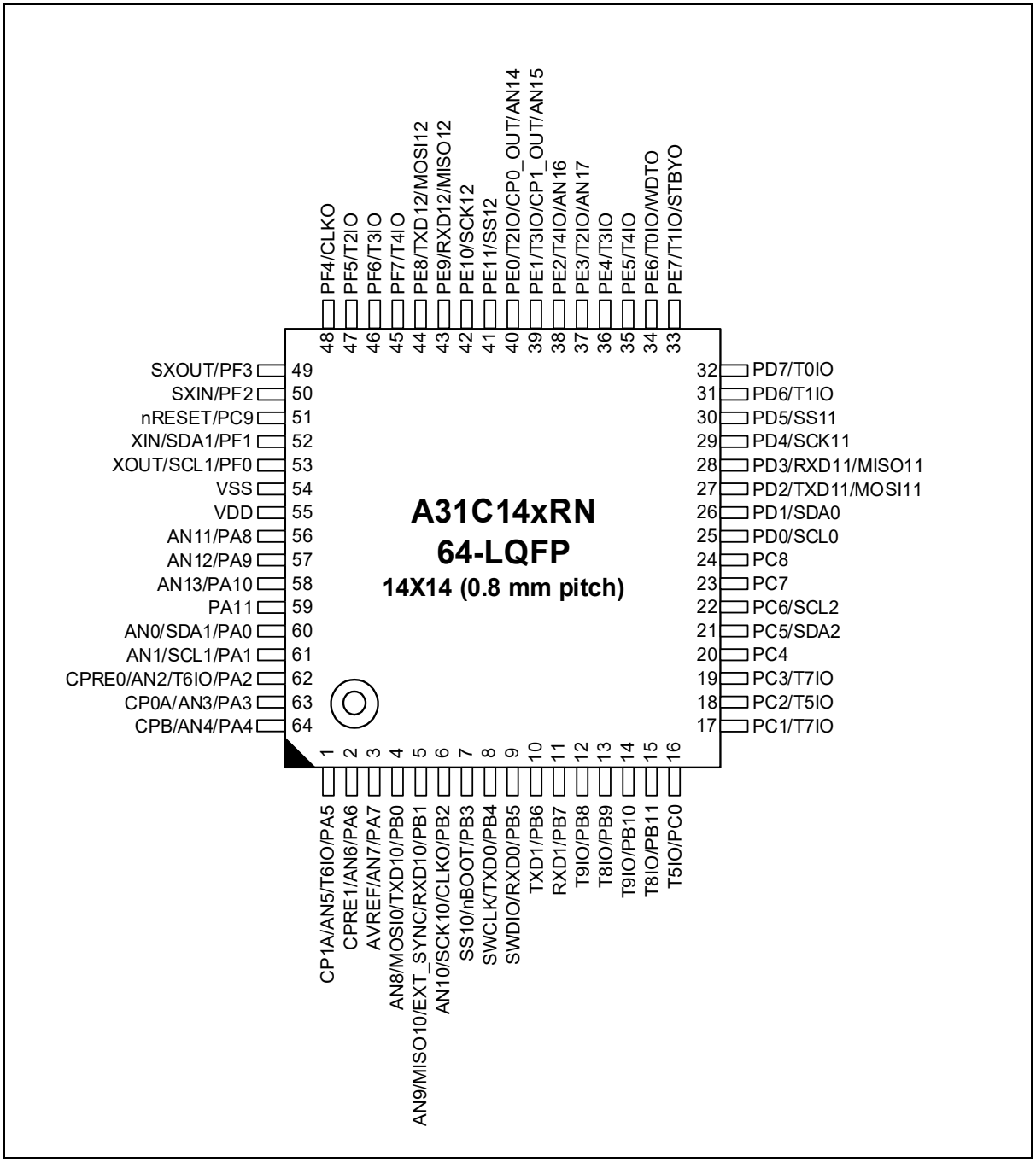
3.1.1 A31C14xRL (64-LQFP-1010)

Figure 3. A31C14xRL (64-LQFP 10x10) Pinouts



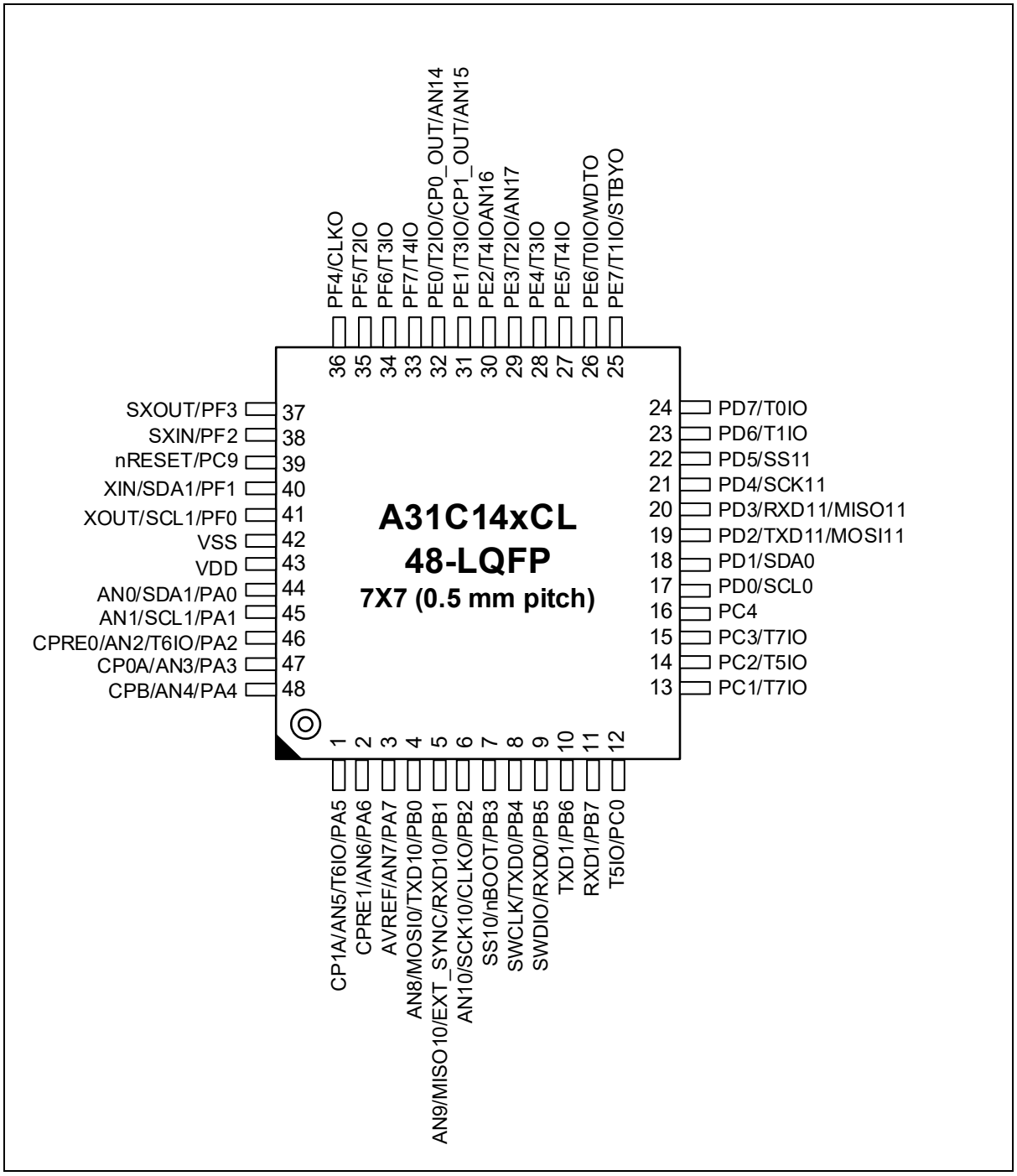
3.1.2 A31C144RN (64-LQFP-1414)

Figure 4. A31C144RN (64-LQFP 14x14) Pinouts



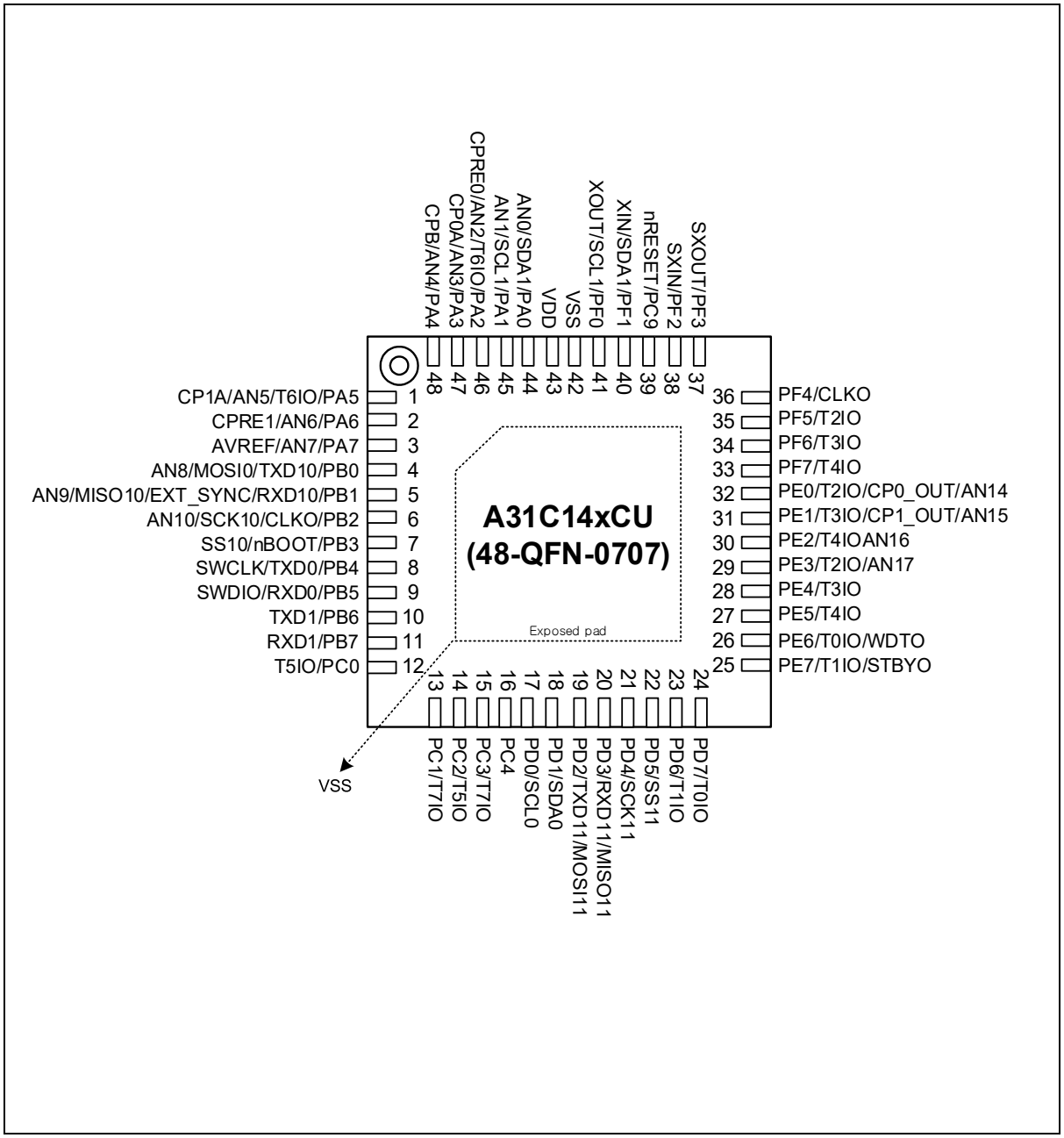
3.1.3 A31C14xCL (48-LQFP-0707)

Figure 5. A31C14xCL (48-LQFP 7x7) Pinouts



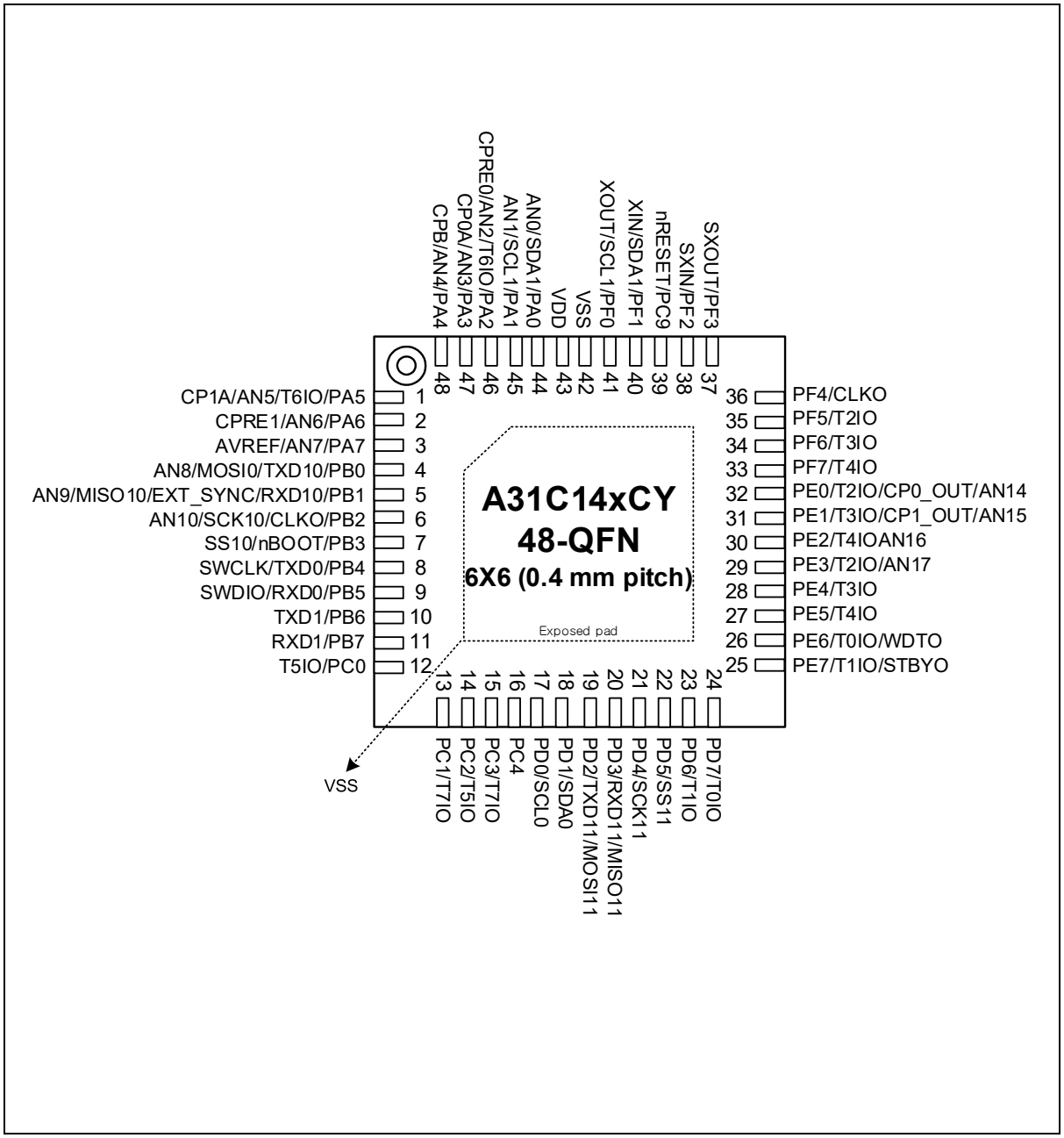
3.1.4 A31C14xCU (48-QFN-0707)

Figure 6. A31C14xCU (48-QFN 7x7) Pinouts



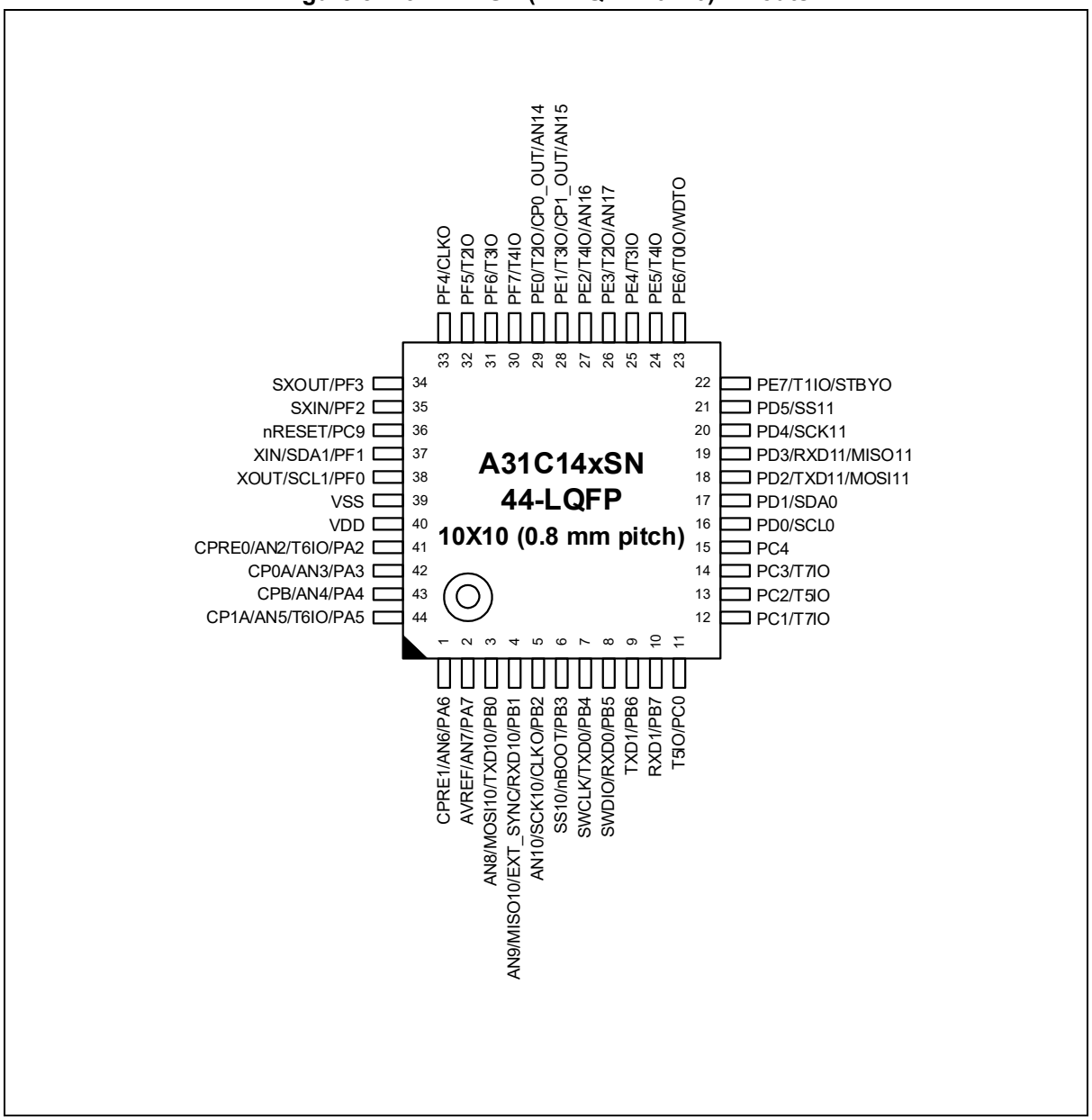
3.1.5 A31C14xCY (48-QFN-0606)

Figure 7. A31C14xCY (48-QFN 6x6) Pinouts



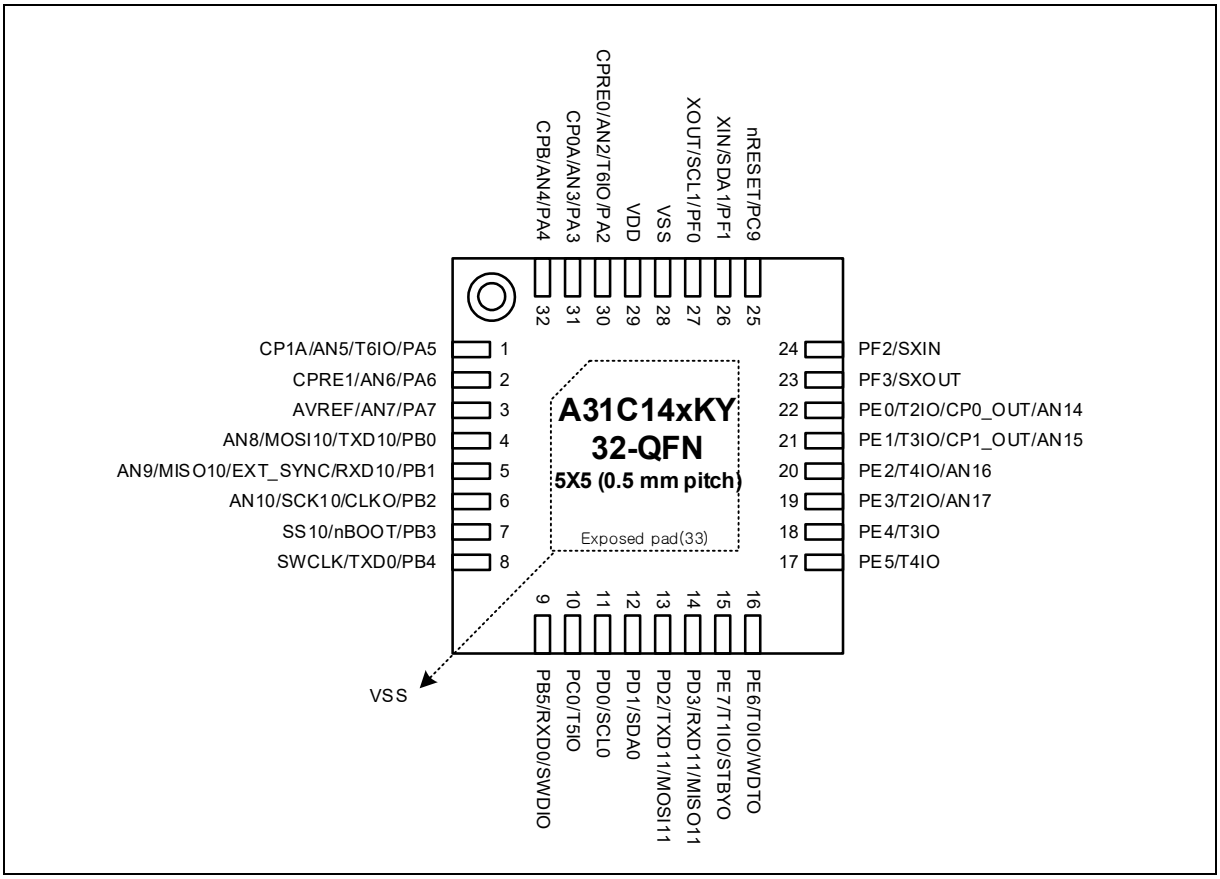
3.1.6 A31C14xSN (44-LQFP-1010)

Figure 8. A31C14xSN (44-LQFP 10x10) Pinouts



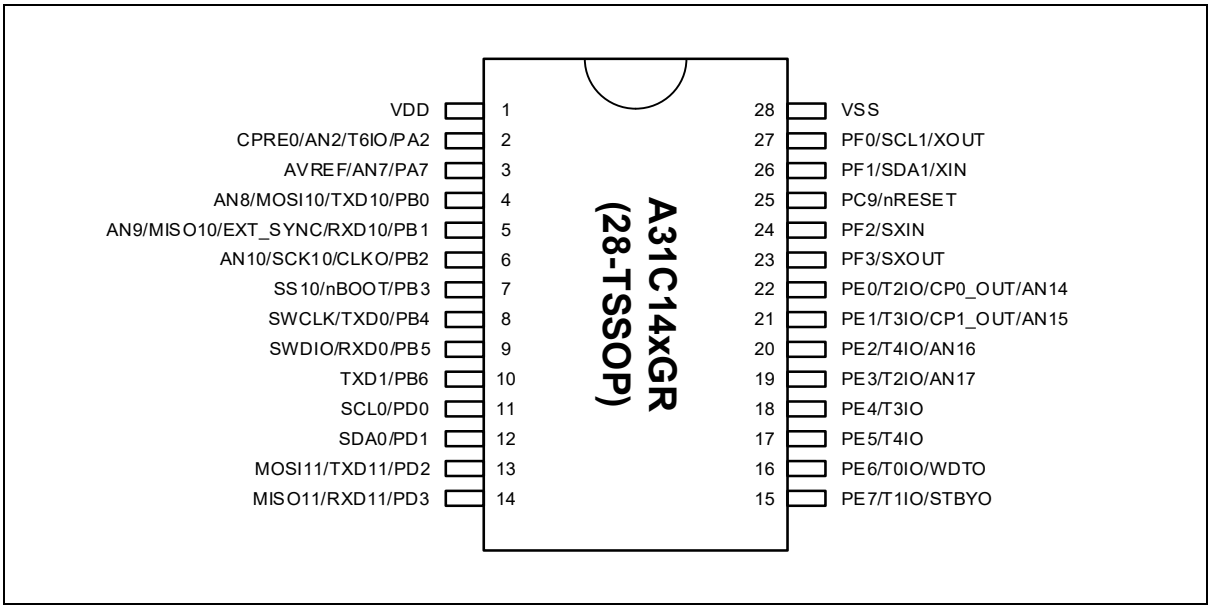
3.1.7 A31C14xKY (32-QFN-0505)

Figure 9. A31C14xKY (32-QFN 5x5) Pinouts



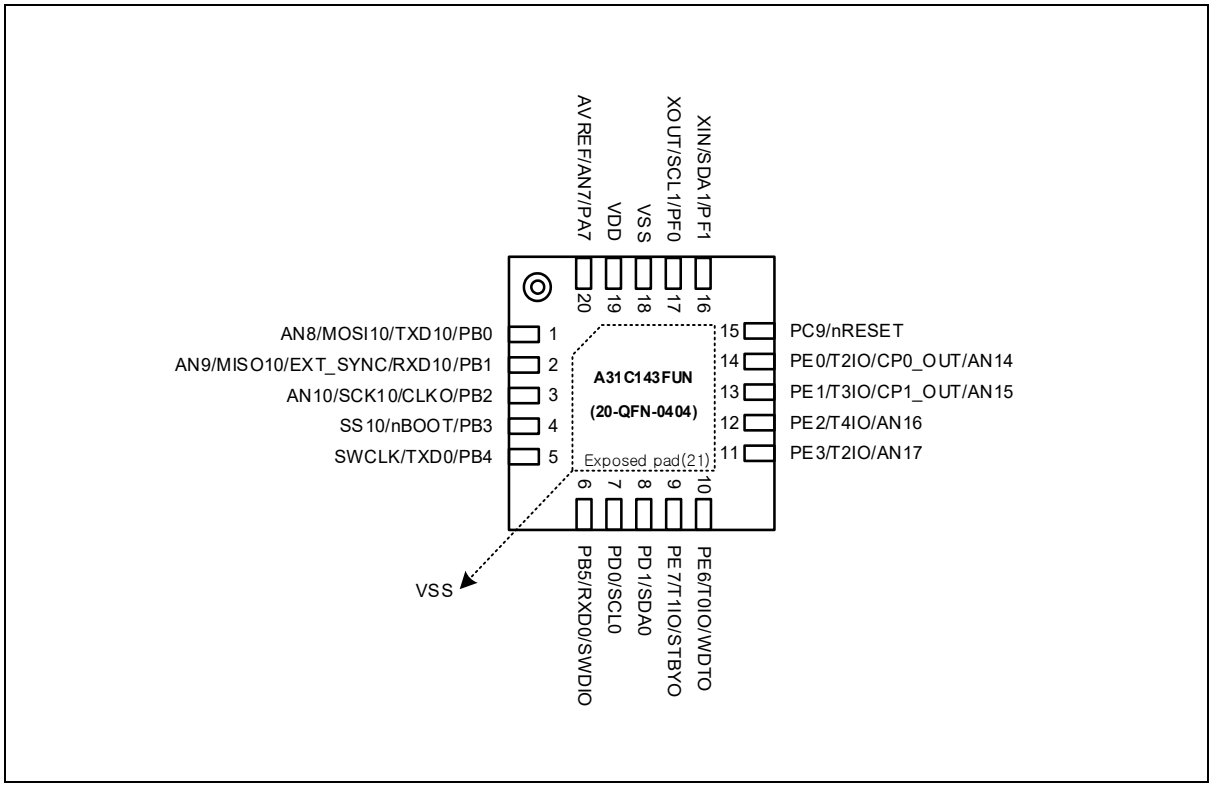
3.1.8 A31C14xGR (28-TSSOP)

Figure 10. A31C14xGR (28-TSSOP) Pinouts



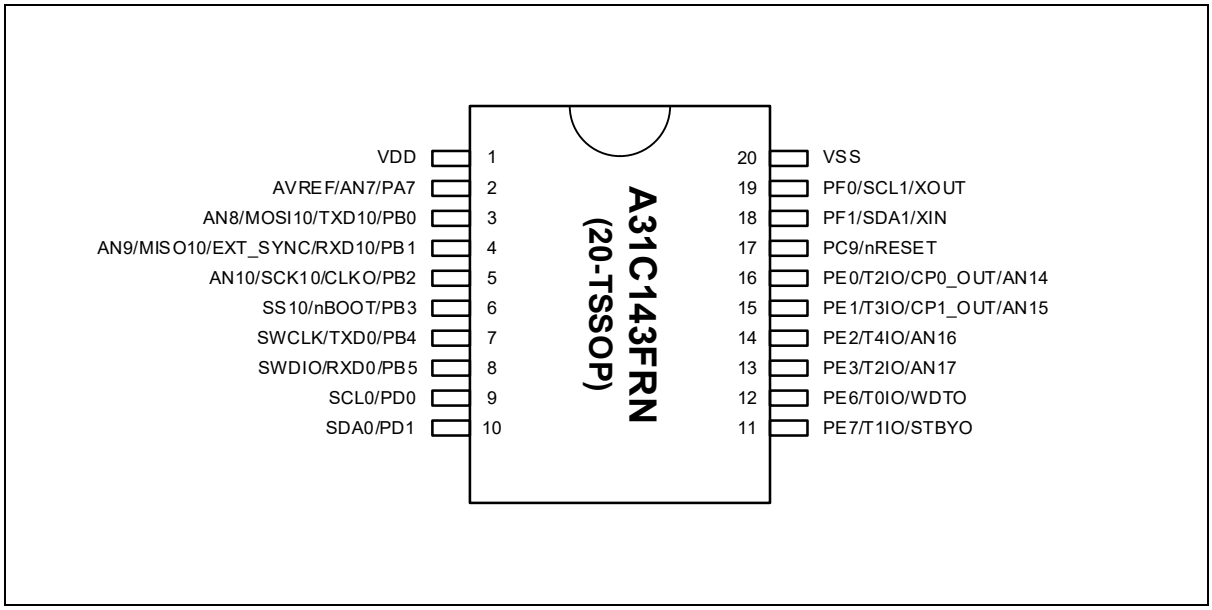
3.1.9 A31C143FU (20-QFN-0404)

Figure 11. A31C143FU (20-QFN 4x4) Pinouts



3.1.10 A31C143FR (20-TSSOP)

Figure 12. A31C143FR (20-TSSOP) Pinouts



3.2 Pin Description

Table 8. Legend and Abbreviations Used in Pin Description

Name	Abbreviation	Definition
Pin name	• The pin name remains constant. • Users can assign a function to the pin using the alternate function.	
Pin type	I	Input
	O	Output
	I/O	Input/Output
	U	Pull-up
	D	Pull-down
	S	Schmitt-Trigger input
	C	CMOS input
	A	Analog
	P	Power

NOTES:

1. After a reset, all the pins are configured to function as defined by their initial values.
2. Unused pins are set to output from firmware. (Low output is recommended).
3. PB3 (nBOOT), PC9 (nRESET), PB5 (SWDIO) and the default pull-up pins and PB4 (SWCLK) are default pull-down pins.
4. Do not configure unused pins as floating inputs.
5. After a reset, the internal pull-up for the boot pin is enabled.
6. After a reset, the internal pull-up for the Serial Wire Data I/O (SWDIO) is enabled and the internal pull-down for the Serial Wire Clock (SWCLK) is enabled.
7. The SWCLK and SWDIO pins should not be switched to other functions while they are being used.
8. When the PF1 (XIN), PF0 (XOUT), PF3 (SXOUT), and PF2 (SXIN) pins are configured for a function other than a clock, and if the clock is enabled by software, the other functions may not operate normally.

The pin configuration information in Table 9 contains two pairs of power/ground and other dedicated pins. These multi-function pins have up to six selections of functions, including GPIO. Configuration, including pin ordering, can be changed without notice.

Table 9. Pin Description

Pin No.							Pin Name	Type	Description	Remark
64-pin	48-pin	44-pin	32-pin	28-pin	20-pin (QFN)	20-pin (TSSOP)				
1	1	44	1	-	-	-	PA5	IOUS	Port A bit 5 input/output	
							T6IO	IO	Timer 6 input/output	
							AN5(2)	IA	Analog Input 5	
							CP1A(2)	IA	COMP 1 Pos Input A	
2	2	1	2	-	-	-	PA6	IOUS	Port A bit 6 input/output	
							AN6(2)	IA	Analog input 6	
							CPRE1(2)	IA	Comparator 1 Reference Input	
3	3	2	3	3	20	2	PA7	IOUS	Port A bit 7 input/output	
							AVREF	IA	Analog Reference Input	
							AN7(2)	IA	Analog input 7	
4	4	3	4	4	1	3	PB0	IOUS	Port B bit 0 input/output	
							TXD10	O	UART(USART) CH0 data output	
							MOSI10	IO	SPI(USART) CH0 Master out/Slave input	
							AN8(2)	IA	Analog input 8	
5	5	4	5	5	2	4	PB1	IOUS	Port B bit 1 input/output	
							RXD10	I	UART(USART) CH0 data Input	
							EXT_SYNC	I	HSICMU External Sync Input	
							MISO10	IO	SPI(USART) CH0 Master input/Slave output	
							AN9(2)	IA	Analog input 9	
6	6	5	6	6	3	5	PB2	IOUS	Port B bit 2 input/output	
							CLKO	O	System clock output	
							SCK10	IO	SPI(USART) CH0 clock input/output	
							AN10(2)	IA	Analog input 10	
7	7	6	7	7	4	6	PB3	IOUS	Port B bit 3 input/output	
							nBOOT(2)(3)(5)	I	Boot mode selection input	Pull-Up
							SS10	IO	SPI(USART) CH0 slave select input	
8	8	7	8	8	5	7	PB4	IOUS	Port B bit 4 input/output	
							TXD0	O	UART CH0 TXD output	
							SWCLK(2)(3)(6)(7)	I	SWD clock input	Pull-Down
9	9	8	9	9	6	8	PB5	IOUS	Port B bit 5 input/output	
							RXD0	I	UART CH0 RXD input	
							SWDIO(2)(3)(6)(7)	IO	SWD data input/output	Pull-Up
10	10	9	-	10	-	-	PB6	IOUS	Port B bit 6 input/output	
							TXD1	O	UART CH1 data output	

Table 9. Pin Description (continued)

Pin No.							Pin Name	Type	Description	Remark
64-pin	48-pin	44-pin	32-pin	28-pin	20-pin (QFN)	20-pin (TSSOP)				
11	11	10	-	-	-	-	PB7	IOUS	Port B bit 7 input/output	
							RXD1	I	UART CH1 data input	
12	-	-	-	-	-	-	PB8	IOUS	Port B bit 8 input/output	
							T9IO	IO	Timer 9 input/output	
13	-	-	-	-	-	-	PB9	IOUS	Port B bit 9 input/output	
							T8IO	IO	Timer 8 input/output	
14	-	-	-	-	-	-	PB10	IOUS	Port B bit 10 input/output	
							T9IO	IO	Timer 9 input/output	
15	-	-	-	-	-	-	PB11	IOUS	Port B bit 11 input/output	
							T8IO	IO	Timer 8 input/output	
16	12	11	10	-	-	-	PC0	IOUS	Port C bit 0 input/output	
							T5IO	IO	Timer 5 input/output	
17	13	12	-	-	-	-	PC1	IOUS	Port C bit 1 input/output	
							T7IO	IO	Timer 7 input/output	
18	14	13	-	-	-	-	PC2	IOUS	Port C bit 0 input/output	
							T5IO	IO	Timer 5 input/output	
19	15	14	-	-	-	-	PC3	IOUS	Port C bit 3 input/output	
							T7IO	IO	Timer 7 input/output	
20	16	15	-	-	-	-	PC4	IOUS	Port C bit 4 input/output	
21	-	-	-	-	-	-	PC5	IOUS	Port C bit 5 input/output	
							SDA2	IO	I2C CH2 SDA input/output	Open-Drain
22	-	-	-	-	-	-	PC6	IOUS	Port C bit 6 input/output	
							SCL2	IO	I2C CH2 SCL input/output	Open-Drain
23	-	-	-	-	-	-	PC7	IOUS	Port C bit 7 input/output	
24	-	-	-	-	-	-	PC8	IOUS	Port C bit 8 input/output	
25	17	16	11	11	7	9	PD0	IOUS	Port D bit 0 input/output	
							SCL0	IO	I2C CH0 SCL input/output	Open-Drain
26	18	17	12	12	8	10	PD1	IOUS	Port D bit 1 input/output	
							SDA0	IO	I2C CH0 SDA input/output	Open-Drain
27	19	18	13	13	-	-	PD2	IOUS	Port D bit 2 input/output	
							TXD11	O	UART(USART) CH1 data output	
							MOSI11	IO	SPI(USART) CH1 Master out/Slave input	
28	20	19	14	14	-	-	PD3	IOUS	Port D bit 3 input/output	
							RXD11	I	UART(USART) CH1 data input	
							MISO11	IO	SPI(USART) CH1 Master input/Slave output	
29	21	20	-	-	-	-	PD4	IOUS	Port D bit 4 input/output	
							SCK11	IO	SPI(USART) CH1 clock input/output	
30	22	21	-	-	-	-	PD5	IOUS	Port D bit 5 input/output	
							SS11	IO	SPI(USART) CH1 slave select input	

Table 9. Pin Description (continued)

Pin No.							Pin Name	Type	Description	Remark
64-pin	48-pin	44-pin	32-pin	28-pin	20-pin (QFN)	20-pin (TSSOP)				
31	23	-	-	-	-	-	PD6	IOUS	Port D bit 6 input/output	
							T1IO	IO	Timer 1 input/output	
32	24	-	-	-	-	-	PD7	IOUS	Port D bit 7 input/output	
							T0IO	IO	Timer 0 input/output	
33	25	22	15	15	9	11	PE7	IOUS	Port E bit 7 input/output	
							T1IO	IO	Timer 1 input/output	
							STBYO	O	Deep Sleep mode output	
34	26	23	16	16	10	12	PE6	IOUS	Port E bit 6 input/output	
							T0IO	IO	Timer 0 input/output	
							WDTO	O	Watchdog timer overflow output	
35	27	24	17	17	-	-	PE5	IOUS	Port E bit 5 input/output	
							T4IO	IO	Timer 4 input/output	
36	28	25	18	18	-	-	PE4	IOUS	Port E bit 4 input/output	
							T3IO	IO	Timer 3 input/output	
37	29	26	19	19	11	13	PE3	IOUS	Port E bit 3 input/output	
							T2IO	IO	Timer 2 input/output	
							AN17[2]	IA	Analog input 17	
38	30	27	20	20	12	14	PE2	IOUS	Port E bit 2 input/output	
							T4IO	IO	Timer 4 input/output	
							AN16[2]	IA	Analog input 16	
39	31	28	21	21	13	15	PE1	IOUS	Port E bit 1 input/output	
							T3IO	IO	Timer 3 input/output	
							CP1OUT	O	Comparator 0 output	
							AN15[2]	IA	Analog input 15	
40	32	29	22	22	14	16	PE0	IOUS	Port E bit 0 input/output	
							T2IO	IO	Timer 2 input/output	
							CP0OUT	O	Comparator 0 output	
							AN14[2]	IA	Analog input 14	
41	-	-	-	-	-	-	PE11	IOUS	Port E bit 11 input/output	
							SS12	IO	SPI(USART) CH2 slave select input	
42	-	-	-	-	-	-	PE10	IOUS	Port E bit 10 input/output	
							SCK12	IO	SPI(USART) CH2 clock input/output	
43	-	-	-	-	-	-	PE9	IOUS	Port E bit 9 input/output	
							RXD12	I	UART(USART) CH2 data input	
							MISO12	IO	SPI(USART) CH2 Master input/Slave output	
44	-	-	-	-	-	-	PE8	IOUS	Port E bit 8 input/output	
							TXD12	O	UART(USART) CH2 data output	
							MOSI12	IO	SPI(USART) CH2 Master out/Slave input	
45	33	30	-	-	-	-	PF7	IOUS	Port F bit 7 input/output	
							T4IO	IO	Timer 4 input/output	

Table 9. Pin Description (continued)

Pin No.							Pin Name	Type	Description	Remark
64-pin	48-pin	44-pin	32-pin	28-pin	20-pin (QFN)	20-pin (TSSOP)				
46	34	31	-	-	-	-	PF6	IOUS	Port F bit 6 input/output	
							T3IO	IO	Timer 3 input/output	
47	35	32	-	-	-	-	PF5	IOUS	Port F bit 5 input/output	
							T2IO	IO	Timer 2 input/output	
48	36	33	-	-	-	-	PF4	IOUS	Port F bit 4 input/output	
							CLKO	O	System clock output	
49	37	34	23	23	-	-	PF3	IOUS	Port F bit 3 input/output	
							SXOUT(2)(8)	OA	Sub crystal oscillator output	
50	38	35	24	24	-	-	PF2	IOUS	Port F bit 2 input/output	
							SXIN(2)(8)	IA	Sub crystal oscillator input	
51	39	36	25	25	15	17	PC9	IOUS	Port C bit 9 input/output	
							nRESET(2)(3)	I	External reset input	Pull-Up
52	40	37	26	26	16	18	PF1	IOUS	Port F bit 1 input/output	
							SDA1	IO	I2C CH1 SDA input/output	Open-Drain
							XIN(2)(8)	IA	External crystal oscillator input	
53	41	38	27	27	17	19	PF0	IOUS	Port F bit 0 input/output	
							SCL1	IO	I2C CH1 SCL input/output	Open-Drain
							XOUT(2)(8)	IA	External crystal oscillator output	
54	42	39	28	28	18	20	VSS	P	Ground	
55	43	40	29	1	19	1	VDD	P	VDD	
56	-	-	-	-	-	-	PA8	IOUS	Port A bit 8 input/output	
							AN11(2)	IA	Analog input 11	
57	-	-	-	-	-	-	PA9	IOUS	Port A bit 9 input/output	
							AN12(2)	IA	Analog input 12	
58	-	-	-	-	-	-	PA10	IOUS	Port A bit 10 input/output	
							AN13(2)	IA	Analog input 13	
59	-	-	-	-	-	-	PA11	IOUS	Port A bit 11 input/output	
60	44	-	-	-	-	-	PA0	IOUS	Port A bit 0 input/output	
							SDA1	IO	I2C CH1 SDA input/output	Open-Drain
							AN0(2)	IA	Analog input 0	
61	45	-	-	-	-	-	PA1	IOUS	Port A bit 1 input/output	
							SCL1	IO	I2C CH1 SCL input/output	Open-Drain
							AN1(2)	IA	Analog input 1	
62	46	41	30	2	-	-	PA2	IOUS	Port A bit 2 input/output	
							T6IO	IO	Timer 2 input/output	
							AN2(2)	IA	Analog input 2	
							CPRE0(2)	IA	Comparator 0 reference	
63	47	42	31	-	-	-	PA3	IOUS	Port A bit 3 input/output	
							AN3(2)	IA	Analog input 3	
							CP0A(2)	IA	Comparator 0 plus input A	
64	48	43	32	-	-	-	PA4	IOUS	Port A bit 4 input/output	
							AN4(2)	IA	Analog input 4	
							CPB(2)	IA	Comparator 0/1 plus input B	

3.3 Alternate Function Pins

The GPIO pins have alternate functions, as described in Table 10.

Table 10. GPIO Alternate Function (1)

Pin Name	Alternate Function					
	AF0	AF1	AF2	AF3	AF4	AF7
PA0	PA0	SDA1				AN0*
PA1	PA1	SCL1				AN1*
PA2	PA2		T6IO			AN2/CPRE0*
PA3	PA3					AN3/CP0A*
PA4	PA4					AN4/CPB*
PA5	PA5		T6IO			AN5/CP1A*
PA6	PA6					AN6/CPRE1*
PA7	PA7					AN7/AVREF*
PA8	PA8					AN11*
PA9	PA9					AN12*
PA10	PA10					AN13*
PA11	PA11					*
PB0	PB0	TXD10			MOSI10	AN8*
PB1	PB1	RXD10		EXT_SYNC	MISO10	AN9*
PB2	PB2			CLKO	SCK10	AN10*
PB3	PB3			nBOOT*	SS10	
PB4	PB4	TXD0		SWCLK*		
PB5	PB5	RXD0		SWDIO*		
PB6	PB6	TXD1				*
PB7	PB7	RXD1				*
PB8	PB8		T9IO			*
PB9	PB9		T8IO			*
PB10	PB10		T9IO			*
PB11	PB11		T8IO			*
PC0	PC0		T5IO			*
PC1	PC1		T7IO			*
PC2	PC2		T5IO			*
PC3	PC3		T7IO			*
PC4	PC4					*
PC5	PC5	SDA2				*
PC6	PC6	SCL2				*
PC7	PC7					*
PC8	PC8					*
PC9	PC9			nRESET*		

Table 10. GPIO Alternate Function (1) (continued)

Pin Name	Alternate Function					
	AF0	AF1	AF2	AF3	AF4	AF7
PD0	PD0	SCL0				*
PD1	PD1	SDA0				*
PD2	PD2	TXD11			MOSI11	*
PD3	PD3	RXD11			MISO11	*
PD4	PD4				SCK11	*
PD5	PD5				SS11	*
PD6	PD6		T1IO			*
PD7	PD7		T0IO			*
PE0	PE0		T2IO		CP0OUT	AN14*
PE1	PE1		T3IO		CP1OUT	AN15*
PE2	PE2		T4IO			AN16*
PE3	PE3		T2IO			AN17*
PE4	PE4		T3IO			*
PE5	PE5		T4IO			*
PE6	PE6		T0IO	WDTO		*
PE7	PE7		T1IO	STBYO		*
PE8	PE8	TXD12			MOSI12	*
PE9	PE9	RXD12			MISO12	*
PE10	PE10				SCK12	*
PE11	PE11				SS12	*
PF0	PF0	SCL1				XOUT*
PF1	PF1	SDA1				XIN*
PF2	PF2					SXIN*
PF3	PF3					SXOUT*
PF4	PF4			CLKO		*
PF5	PF5		T2IO			*
PF6	PF6		T3IO			*
PF7	PF7		T4IO			*

NOTES:

1. Unused pins are set to output from firmware (low output is recommended).

* After a reset, all the pins are configured to function defined by their initial values. The initial value of the pin depends on the package type. This configuration is in compliance with the 64-pin standard.

4. Electrical Characteristics

4.1 Parameter Conditions

Unless otherwise specified, all voltages are referenced to GND.

4.1.1 Minimum and Maximum Values

Unless otherwise specified, our production tests guarantee the minimum and maximum values of the device under the worst-case conditions of ambient temperature, supply voltage, and frequency.

Data based on characterization results, design simulation, and/or technical characteristics are not tested in production but are indicated in the table footnotes.

4.1.2 Typical Value

Unless otherwise specified, typical data is based on the conditions of T_A = 25°C and V_{DD} = 5.0 V. The typical data are provided only as design recommendations and are not tested.

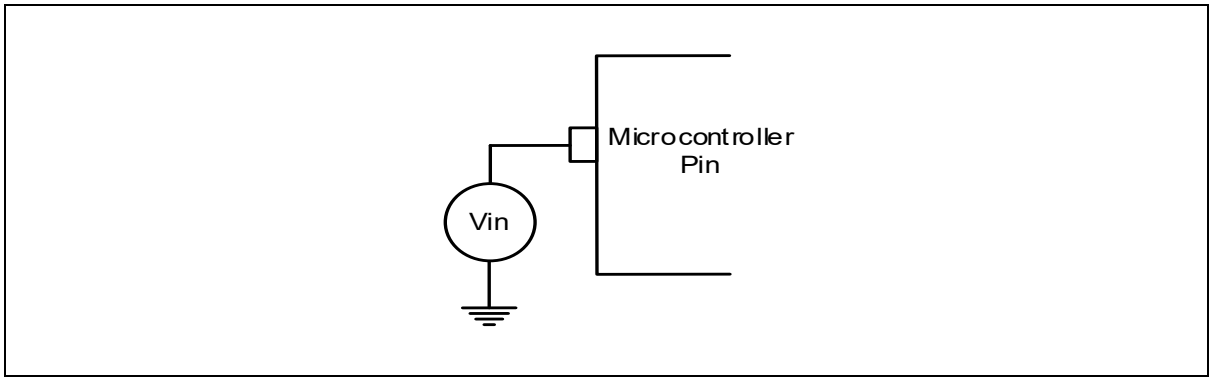
4.1.3 Typical Curves

Unless otherwise specified, all typical curves are provided only as design recommendations and are not tested.

4.1.4 Pin Input Voltage

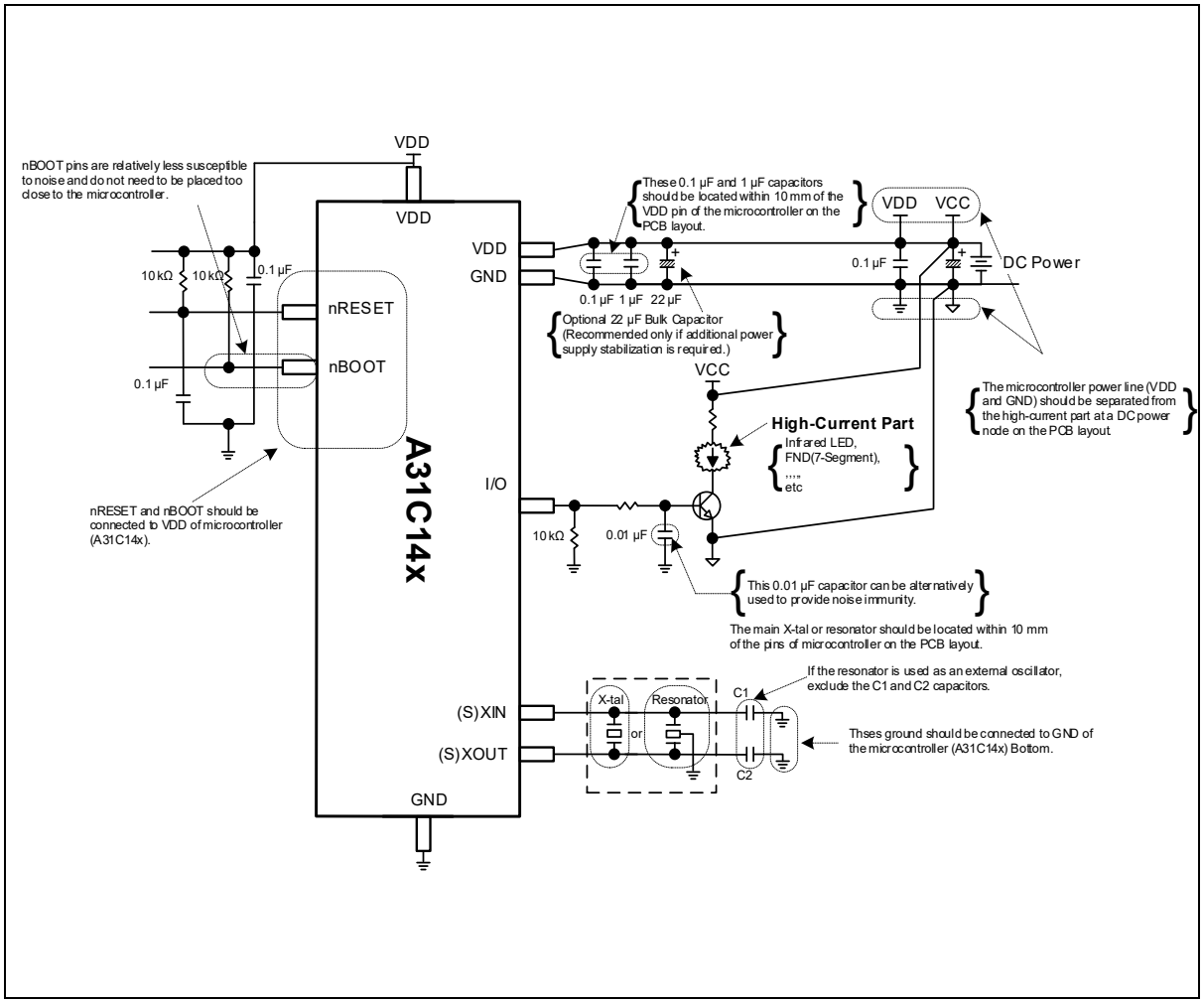
The input voltage measurement on a pin of the device is described in Figure 13.

Figure 13. Pin Input Voltage



4.1.5 Power Supply Scheme

Figure 14. Power Supply Scheme

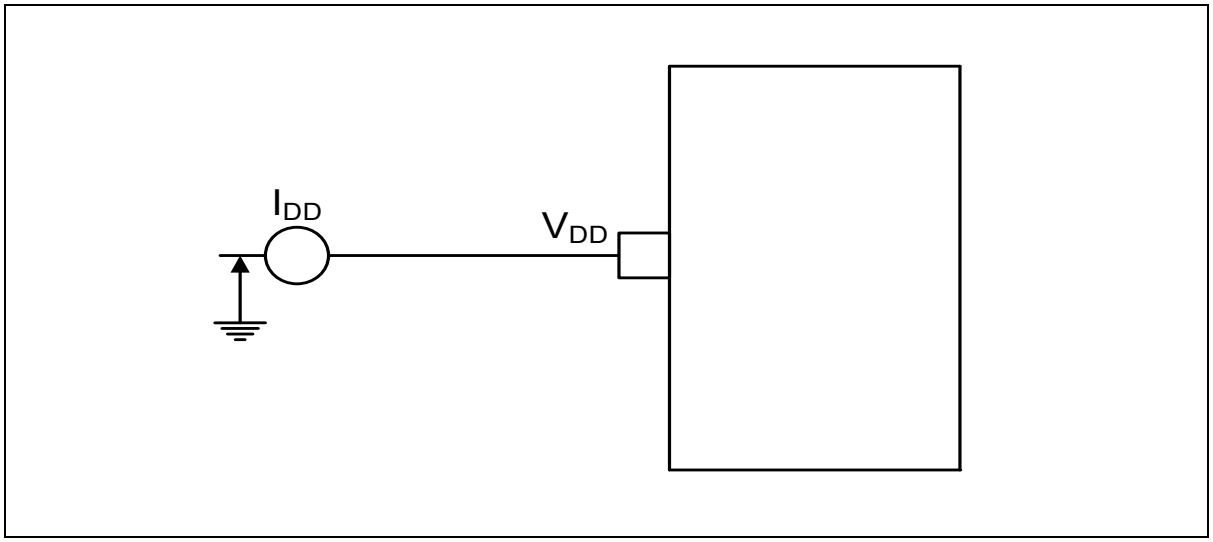


NOTES:

1. As shown above, each power supply pair (V_{DD}/GND, etc.) must be decoupled with filtering ceramic capacitors. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.
2. Product A31C14x requires 1 µF and 0.1 µF bypass capacitors to be mounted on the VDD line.

4.1.6 Current Consumption Measurement

Figure 15. Current Consumption Measurement



NOTE:

1. The I_{DD} parameter represents the total microcontroller's current consumption, including the current supplying V_{DD}.

4.2 Absolute Maximum Ratings

Exceeding stresses specified in Table 11 for voltage characteristics, Table 12 for current characteristics, or Table 13 for thermal characteristics may result in permanent damage to the device. The values in the tables are stress ratings only and do not imply that the device will function properly under these conditions. Prolonged exposure to these maximum rating conditions may impact on the device's reliability. It is important to operate the device within its specified maximum ratings to ensure reliable performance.

Table 11. Voltage Characteristics

Symbol	Ratings	Min.	Max.	Unit
V_{DD}–GND(1)	External main supply voltage (including V_{DD})	-0.5	6.0	V
V_I(2)	Input voltage on I/O	-0.5	Max (V_{DD}) + 0.5	V
V_O	Output voltage on I/O	-0.5	Max (V_{DD}) + 0.5	V

NOTES:

1. All main power (V_{DD}) and ground (GND) pins must always be connected to the external power supply within the permitted range.
2. V_I maximum must always be respected.

Table 12. Current Characteristics

Symbol	Ratings	Max.	Unit
$\sum I_{VDD}$	Total current into the sum of all V_{DD} power lines (source)(1)	-120	mA
$\sum I_{GND}$	Total current out of the sum of all GND ground lines (sink)(1)	120	mA
$I_{VDD(PIN)}$	Maximum current into each V_{DD} power pin (source)(1)	-100	mA
$I_{GND(PIN)}$	Maximum current out of each GND ground pin (sink)(1)	100	mA
$I_{IO(PIN)}$	Output current sunk by any I/O	15	mA
	Output current sourced by any I/O and control pin	-9	mA
$\sum I_{IO(PIN)}$	Total output current sunk by the sum of all I/Os and control pins(2)	45	mA
	Total output current sourced by the sum of all I/Os and control pins(2)	-27	mA
I_{IL}	Input low leakage current	1	µA
I_{IH}	Input high leakage current	1	µA
P_T	Total power dissipation	600	mW

NOTES:

1. All main power (V_{DD}) and ground (GND) pins must always be connected to the external power supplies in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.

Table 13. Thermal Characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-55 to +125	°C
T_J	Maximum junction temperature	+105	°C

4.3 Operating Condition

4.3.1 General Operating Condition

Table 14. General Operating Condition

(Temperature: -40°C to +85°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	Core and Peripherals	1.8(1)	-	5.5	V
		ADC/CMP used	2.4	-	5.5	V
FREQ	Operating frequency	HSE	4	-	12	MHz
		LSE	-	32.768	-	kHz
		HSI(2)	-	32	-	MHz
		LSI(3)	-	32	-	kHz
V_{IN}	I/O input voltage	5 V I/O	-0.3	-	V_{DD}	V
T_A	Ambient temperature	-	-40	-	85	°C
T_J	Junction temperature range	-	-40	40	125	°C

NOTES:

1. When RESET is released, functionality is guaranteed down to V_{LVR5} Min.
2. Refer to 4.3.8.1 for more detailed information.
3. Refer to 4.3.8.2 for more detailed information.

4.3.2 Power-On Reset Characteristics

Table 15. POR Electrical Characteristics

(Temperature: -40°C to +85°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{DD}	Operating current	-	-	120	-	nA
V_{set}	POR set level	-	1.38	1.48	1.6	V
V_{reset}	POR reset level	-	0.98	1.28	1.58	V
t_R	V_{DD} voltage rising time	-	0.02	-	20	ms/V
t_F	V_{DD} voltage falling time	-	0.4	-	20	ms/V

4.3.3 Operating Condition at Power-Up/Power-Down

Table 16. Operating Condition at Power-Up/Power-Down

(Temperature: -40°C to +85°C)

Symbol	Parameter	Condition	Min.	Max.	Unit
T_{VDD}	V_{DD} rise time rate	-	0.02	20	ms/V
	V_{DD} fall time rate	-	0.4	20	ms/V

4.3.4 Reset and Power Control Block Characteristics (LVR, LVI)

Table 17. Low-Voltage Reset Characteristics

(Temperature: -40°C to +85°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Operating voltage	-		5	5.5	V
V_{LVR0_F}	Detection level	Falling voltage	1.5	1.6	1.7	V
V_{LVR1_F}			2.5	2.7	2.9	
V_{LVR2_F}			3.4	3.7	4	
V_{LVR3_F}			3.82	4.22	4.62	
V_{LVR0_R}	Detection level	Rising voltage	1.6	1.7	1.78	V
V_{LVR1_R}			2.56	2.86	3.16	
V_{LVR2_R}			3.52	3.92	4.32	
V_{LVR3_R}			4.07	4.47	4.87	
-	Hysteresis	-	30	100	300	mV
-	Noise cancelling time	-	-	2	6	µs
I_{DD}	Operation current	-	-	4	6	µA
$I_{DD, STOP}$	Operation current (STOP)	-	-	3	100	nA

Table 18. Low-Voltage Indicator Characteristics

(Temperature: -40°C to +85°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Operating voltage	-		5	5.5	V
V_{LVI0_F}	Detection level	Falling voltage	2	2.21	2.41	V
V_{LVI1_F}			2.71	3.01	3.31	
V_{LVI2_F}			3.6	4	4.4	
V_{LVI3_F}			4.11	4.51	4.91	
V_{LVI0_R}	Detection level	Rising voltage	2.14	2.34	2.54	V
V_{LVI1_R}			2.89	3.19	3.49	
V_{LVI2_R}			3.84	4.24	4.64	
V_{LVI3_R}			4.38	4.78	5.18	
-	Hysteresis	-	30	100	300	mV
-	Noise cancelling time	-	-	2.2	6	µs
I_{DD}	Operation current	-	-	3.5	5	µA
$I_{DD, STOP}$	Operation current (STOP)	-	-	3	100	nA

4.3.5 Embedded Voltage Reference

Table 19. Embedded Internal Voltage Reference

(Temperature: -40°C to +85°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{REFINT}	Internal reference Voltage 1	-	0.97	1	1.03	V
V_{CORE}	Internal reference Voltage 2	-	1.534	1.59	1.646	

NOTE:

1. Guaranteed by design.

4.3.6 Supply Current Characteristics

The amount of current consumed by the device is determined by various factors and parameters, including but not limited to the operating voltage, ambient temperature, load on I/O pins, software configuration, operating frequency, switching rate of I/O pins, location of the program in memory, and the binary code being executed.

The current consumption is measured under the conditions specified in Table 20.

4.3.6.1 Supply Current Consumption

Table 20. Supply Current Characteristics

(Temperature: -40°C to +85°C)

Symbol	Parameter	Condition					Voltage Scaling	Typ.	Max.	unit
		LSI (32 kHz)	HSI (32 MHz)	HSE[2] (8 MHz)	LSE (32.768 kHz)	f_{MCLK}				
I_{DD1} (Run)	Normal Operation[1]	STOP	RUN	STOP	STOP	f_{HSI}	5.0 V	3	-	mA
		STOP	STOP	RUN	STOP	f_{HSE}	5.0 V	2	-	mA
		STOP	STOP	STOP	RUN	f_{LSE}	5.0 V	650	-	μA
I_{DD2} (SLEEP)	SLEEP mode[1]	STOP	RUN	STOP	STOP	f_{HSI}	5.0 V	2.2	-	mA
		STOP	STOP	RUN	STOP	f_{HSE}	5.0 V	1.8	-	mA
		STOP	STOP	STOP	RUN	f_{LSE}	5.0 V	550	-	μA
I_{DD3} (STOP1)	DEEP-SLEEP mode[1]	VDC=STOP, WDT(LSE)=ON					5.0 V	5		μA
		VDC=STOP, WDT(LSI)=ON					5.0 V	4.5		μA
I_{DD3} (STOP2)		VDC=STOP, LVD=ON					5.0 V	50		μA
		VDC=STOP, LVD=OFF					5.0 V	1		μA

NOTES:

1. All peripherals are turned off.
2. When HSE 8MHz test, HSEISEL = 0x10, HSENFSEL = 0x01 were set.

4.3.6.2 I/O System Current Consumption

In the I/O system, current consumption can be separated into two components: Static and Dynamic.

4.3.6.3 I/O Static Current Consumption

When I/O pins configured as inputs with pull-up are externally held low, they generate a current consumption. This current consumption can be calculated using the values of the pull-up/pull-down resistors specified in the I/O port characteristics.

Any external pull-down or load must also be considered to estimate the current output pins consumption.

The current consumption of I/O pins configured as inputs may increase when an intermediate voltage level is applied externally. This additional consumption is caused by the input Schmitt-trigger circuits that detect the input value. Unless such a configuration is necessary for the application, this current consumption can be avoided by configuring these I/Os in analog mode. This is especially relevant for ADC and CMP input pins, which should be set up as analog inputs.

4.3.6.4 I/O Dynamic Current Consumption

Besides the internal peripheral current consumption, the application's I/Os also contribute to the overall current consumption. When an I/O pin switches, it draws current from the microcontroller's supply voltage to power the I/O pin circuitry and to charge/discharge any capacitive loads (either internal or external) connected to the pin.

4.3.7 External Clock Source Characteristics

4.3.7.1 High-Speed External Clock Generated from Crystal/Ceramic Resonator

The High-Speed External (HSE) clock can be generated using a crystal/ceramic resonator oscillator with a frequency range of 4 to 12 MHz. The information provided in this paragraph is based on characterization results obtained using typical external components listed in Table 21.

Placing the resonator and load capacitors as close as possible to the oscillator pins in the application is recommended to minimize output distortion and start-up stabilization time.

For further information on the resonator characteristics, such as frequency, package, and accuracy, it is advisable to refer to the crystal resonator manufacturer.

Table 21. HSE Oscillator Characteristics (1)

(Temperature: -40°C to +85°C)

Symbol	Parameter	Condition(2)	Min.	Typ.	Max.	Unit
V_{DD}	Operating voltage	-	1.8	5	5.5	V
$I_{DD(HSE)}$	HSE current consumption	-	-	-	3	mA
I_{STOP}	Power down current	-	-	-	100	nA
f_{OSC_IN}	Oscillator frequency	-	4	-	12	MHz
f_{OUT}	Output frequency	$V_{DD} \geq 1.8$ V(5)	-	-	4	MHz
		$V_{DD} \geq 2.0$ V(6)	4	-	8	
		$V_{DD} \geq 2.2$ V(7)	4	-	12	
V_{IL}	Crystal input (low)	-	-	-	0.2 × V_{DD}	V
V_{IH}	Crystal input (high)	-	0.8 × V_{DD}	-	-	V
V_{OL}	Crystal out (low)	-	-	-	0.2 × V_{DD}	V
V_{OH}	Crystal out (high)	-	0.8 × V_{DD}	-	-	V
C_{L1}, C_{L2}	External load capacitor	4 MHz ≤ f_{OUT} ≤ 8 MHz	7	15	26	pF
		8 MHz ≤ f_{OUT} ≤ 12 MHz	7	15	22	pF
R_F	Feedback resistor	V_{DD} = 5 V	0.7	1	1.3	MΩ
$t_{SU(HSE)}$(3)	Start-up time	f_{OSC_IN} = 8 MHz	-	-	2	ms

NOTES:

1. Guaranteed by design.
2. The resonator characteristics that the crystal/ceramic resonator manufacturer provides.
3. tSU(HSE) is the start-up time measured from the moment when it is enabled (by software) to a stabilized 8 MHz oscillation. This value is measured for a standard crystal resonator and can vary significantly with the crystal manufacturer.
4. HSEISEL = 0x3, HSENFSEL = 0x0 (0x00 is the longest noise filter)
5. HSEISEL = 0x3, HSENFSEL = 0x1
6. HSEISEL = 0x2, HSENFSEL = 0x2
7. HSEISEL = 0x1, HSENFSEL = 0x2

Figure 16. Crystal/Ceramic Oscillator

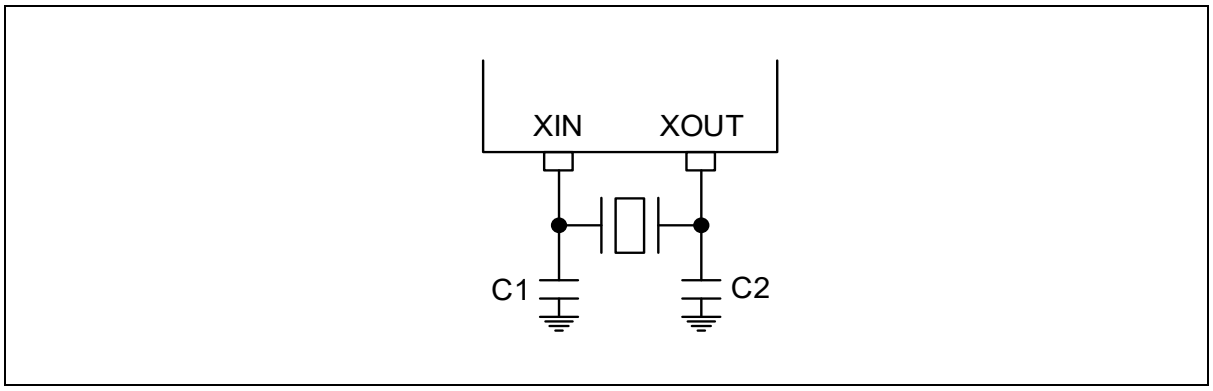


Figure 17. External Clock

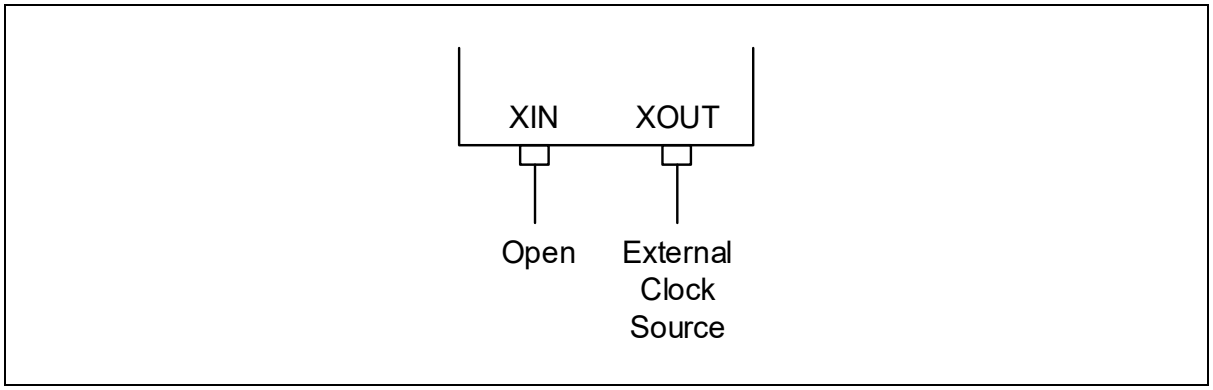
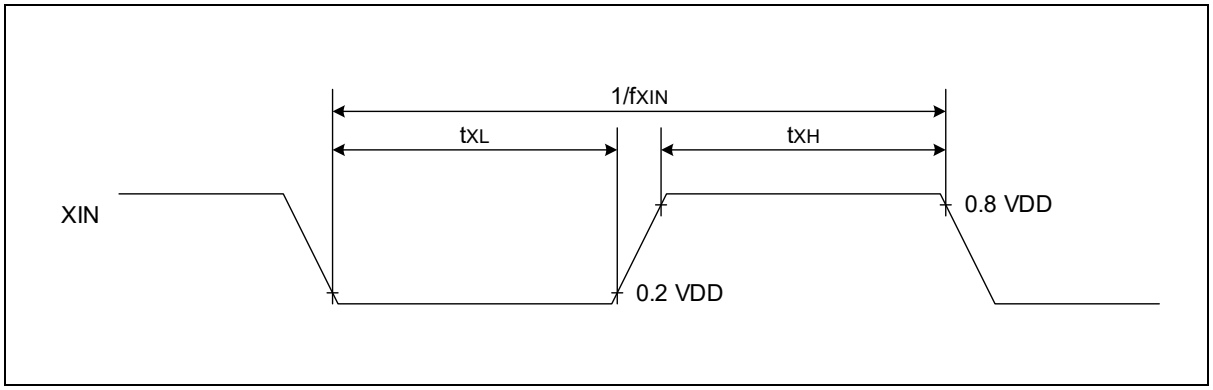


Figure 18. Clock Timing Measurement at XIN

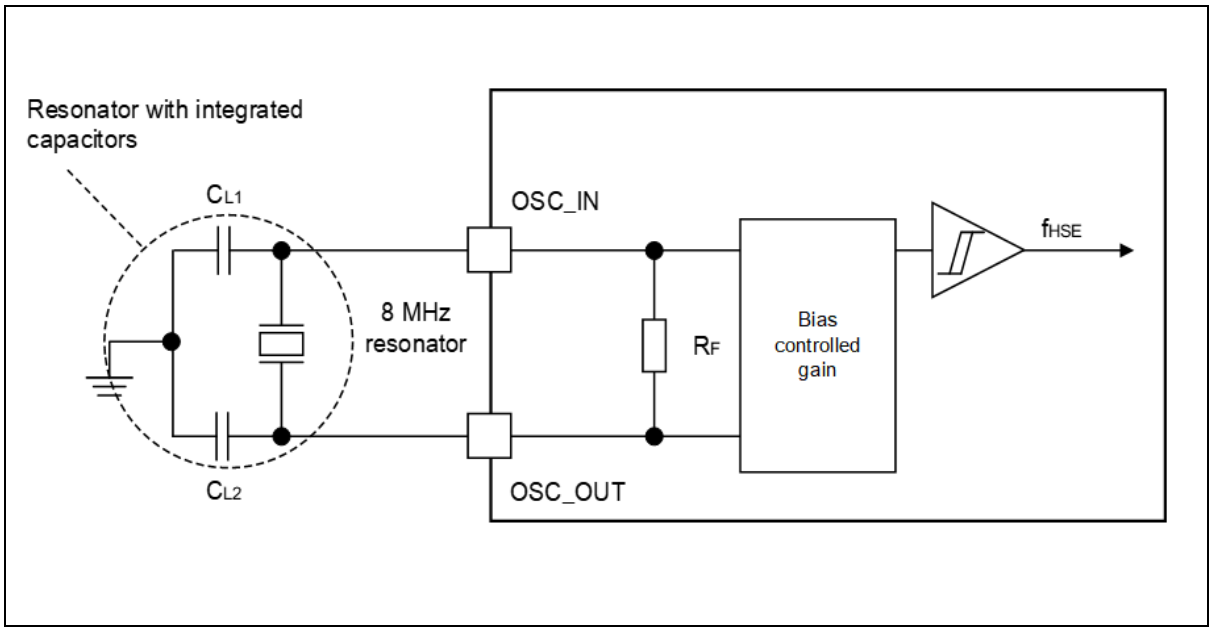


It is recommended to use high-quality external ceramic capacitors designed for high-frequency applications and selected to match the requirements of the crystal or resonator.

The C_L1 and C_L2 capacitors are usually the same size, and the crystal manufacturer specifies a load capacitance that is the series combination of both capacitors. However, the capacitance of the printed circuit board (PCB) and microcontroller's pins should also be considered, which must be included in the calculation of the overall capacitance.

Figure 19 shows a circuit diagram of a typical application with an 8 MHz crystal.

Figure 19. Typical Application with 8 MHz Crystal



4.3.7.2 Low-Speed External Clock Generated from Crystal Resonator

The Low-Speed External (LSE) clock can be generated using a crystal/ceramic resonator oscillator with 32.768 kHz. The information provided in this paragraph is based on characterization results obtained using typical external components listed in Table 22.

Placing the resonator and load capacitors as close as possible to the oscillator pins in the application is recommended to minimize output distortion and start-up stabilization time.

For further information on the resonator characteristics, such as frequency, package, and accuracy, it is advisable to refer to the crystal resonator manufacturer.

Table 22. LSE Oscillator Characteristics (1) (fLSE = 32.768 kHz)

(Temperature: -40°C to +85°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Operating voltage	-	1.8	5	5.5	V
$I_{DD(LSE)}$	LSE current consumption	-	-	3	5	μA
I_{STOP}	Power down current	-	-	-	100	nA
f_{OSC_IN}	Oscillator frequency	-	-	32.768		kHz
C_{L1}, C_{L2}	External load capacitor	-	10	20	25	pF
R_F	Feedback resistor	-	5	10.5	20	MΩ
$t_{SU(LSE)}$(2)	Start-up time	-	-	-	1	s

NOTES:

1. Guaranteed by design.
2. $t_{SU(LSE)}$ is the start-up time measured from the moment when it is enabled (by software) to a stabilized 32.768 kHz oscillation. This value is measured for a standard crystal resonator and can vary significantly with the crystal manufacturer.

Figure 20. Crystal Oscillator

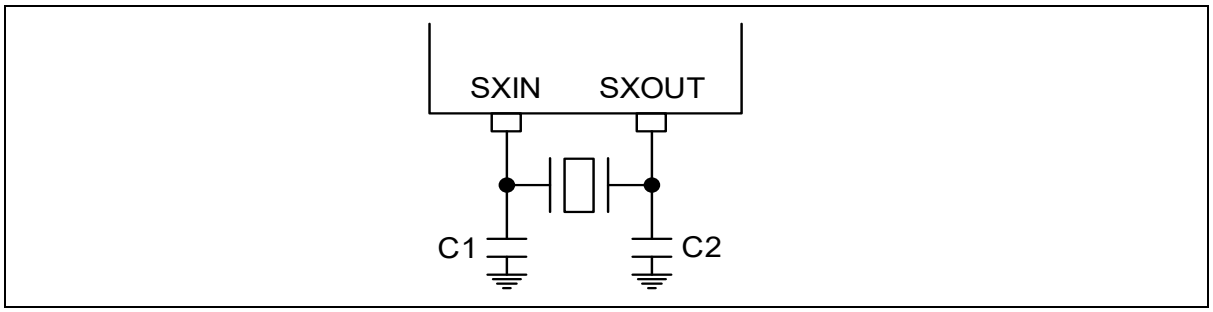


Figure 21. Clock Timing Measurement at SXIN

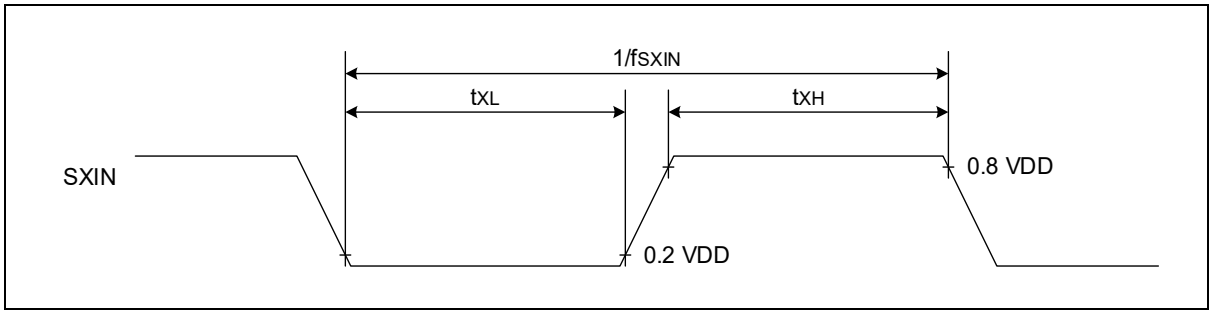
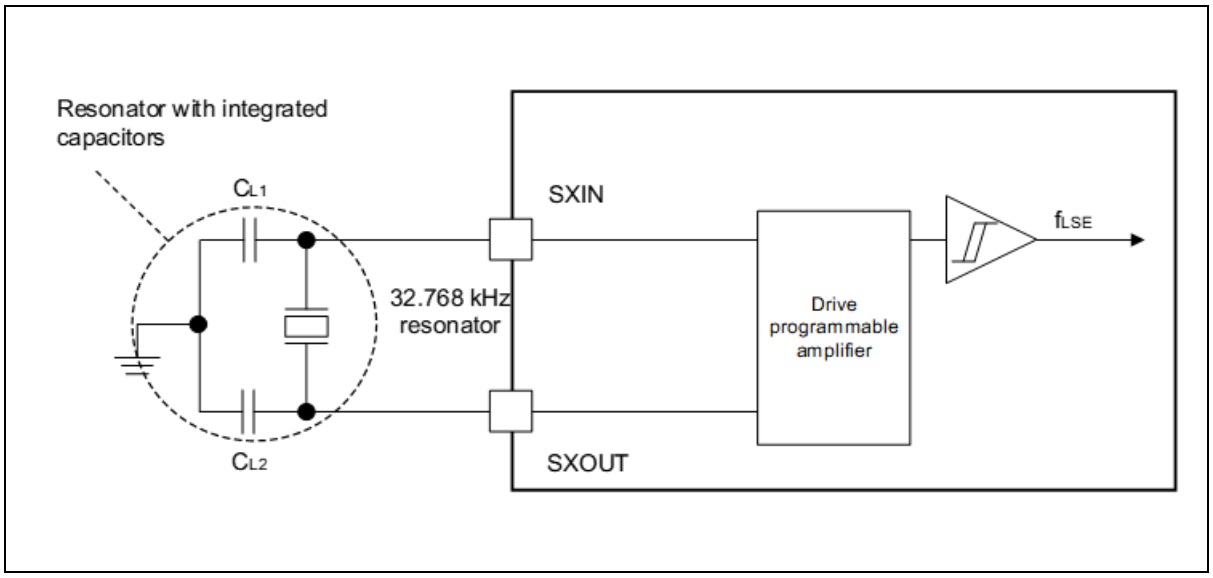


Figure 22. Typical Application with 32.768 kHz Crystal



NOTE:

1. An external resistor must not be connected between SXIN and SXOUT, as no external resistor is required.

4.3.8 Internal Clock Source Characteristics

The parameters listed in Table 23 and Table 24 are obtained through tests conducted under ambient temperature and supply voltage conditions specified in Table 14.

4.3.8.1 High-Speed Internal (HSI32) RC Oscillator

Table 23. HSI32 Oscillator Characteristics (1)

(Temperature: -40°C to +85°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{HSI32}	HSI32 frequency	-	-	32	-	MHz
f_E	Frequency error	@ 0°C to 60°C	-1.5	-	1.5	%
		@ −40°C to 85°C	-3	-	3	%
		@ −40°C to 105°C	-4	-	4	%
DuCy (HSI32)	Duty cycle	-	-	50	-	%
Δ_{VDD} (HSI32)	HSI32 oscillator frequency drift over V_{DD}	V_{DD}=1.8 V to 5.5 V	-	0	-	%
t_{SU} (HSI32)	HSI32 oscillator start-up time	-	-	-	3	µs
t_{STAB} (HSI32)	HSI32 oscillator stabilization time	-	-	1.5	5	µs
I_{DD} (HSI32)	HSI32 oscillator power consumption	-	-	300	-	µA

NOTE:

1. Guaranteed by characterization results and design.

4.3.8.2 Low-Speed Internal (LSI) 32 kHz RC Oscillator

Table 24. LSI Oscillator Characteristics (1)

(Temperature: -40°C to +85°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{OUT}	Output frequency	-	-	32	-	kHz
f_E	Frequency error (V_{DD} = 3.0V)	@ 0°C to 60 °C	-10	-	10	%
		@ -40°C to 85 °C	-30	-	30	%
t_{VREG_SU}	32 kHz oscillator start-up time (after LSI32K LDO enabled)	V_{DD} = 5.0 V	-	-	60	µs
t_{STAB}	32 kHz oscillator stabilization time (after LSI32K enabled)	5 % of target frequency	-	-	500	µs
I_{LIRC}	32 kHz oscillator power consumption	The LSI oscillator is enabled. V_{DD}=1.8 to 5.5 V	-	150	-	nA
		The LSI oscillator is disabled. V_{DD}=1.8 to 5.5 V	-	-	10	

NOTE:

1. Guaranteed by design, not tested in production.

4.3.9 Flash Memory Characteristics

Table 25. Flash Memory Characteristics

(Temperature: -40°C to +85°C)

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
t_{PROG}	Program time	-		-	25	-	µs
t_{PER}	Page erase time	-		-	2	-	ms
t_{SER}	Sector erase time	-		-	2	-	ms
t_{MER}	Macro erase time	-		-	8	-	ms
N_{FWE}	Endurance of write/erase	• A31C144: Page 0 to 251 • A31C143: Page 0 to 123	T_A=25°C, page unit	10,000	-	-	times
		• A31C144: Page 252 to 255 • A31C143: Page 124 to 127		100,000			
t_{FRT}	Retention time	-		10	-	-	years

4.3.10 I/O Port Characteristics

Table 26. DC Electrical Characteristics

(Temperature: -40°C to +85°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input low voltage	All GPIOs	-	-	0.2 × V_{DD}	V
V_{IH}	Input high voltage	All GPIOs	0.8 × V_{DD}	-	-	V
V_{OL}	Output low voltage	V_{DD}=5 V, I_{OL} = 15 mA	-	-	0.2 × V_{DD}	V
V_{OH}	Output high voltage	V_{DD}=5 V, I_{OH}=–9 mA	0.8 × V_{DD}	-	-	V
I_{OL}	Output low current	V_{DD}=3 V, V_{OL}=0.2×V_{DD}	-	10	-	mA
I_{OH}	Output high current	V_{DD}=3 V, V_{OH}=0.8×V_{DD}	-	-5	-	mA
I_{IL}	Input low leakage current	All Input ports	-1	-	-	µA
I_{IH}	Input high leakage current	All Input ports	-	-	1	µA
R_{PU}	Pull-up resistor	All GPIOs, V_{IN} = GND	30	50	70	kΩ
R_{PD}	Pull-down resistor	All GPIOs, V_{IN} = VDD	30	50	70	kΩ

4.3.10.1 General Input/Output Characteristics

Unless otherwise specified, the parameters in Table 27 are obtained through tests conducted under the conditions specified in Table 14. All I/Os conform to CMOS standard.

Table 27. I/O Static Characteristics

(Temperature: -40°C to +85°C)

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
V_{IL}	I/O input low level voltage	5 V GPIO	1.8 V ≤ V_{DD} ≤ 5.5 V	-	-	0.2 × V_{DD}	V
V_{IH}	I/O input high level voltage	5 V GPIO	1.8 V ≤ V_{DD} ≤ 5.5 V	0.8 × V_{DD}	-	-	V
V_{HYS}(2)	Input hysteresis	5 V GPIO	1.8 V ≤ V_{DD} ≤ 5.5 V $V_{DDTYPICAL}$ = 5 V	-	1	-	V
I_{leak}	Input leakage current(2)	5 V GPIO	1.8 ≤ V_{IN} ≤ V_{DD} x 1.1	-1	-	1	µA
R_{PU}	Weak pull-up equivalent resistor	V_{IN} = GND		30	50	70	kΩ
R_{PD}	Weak pull-down equivalent resistor	V_{IN} = V_{DD}		30	50	70	
C_{IO}	I/O pin capacitance	I/O pin capacitance		-	5	-	pF

NOTES:

1. Data based on characterization results are not tested in production.
2. Guaranteed by design.

4.3.10.2 Output Driving Current

To ensure compliance with the absolute maximum ratings specified in chapter 4.2, it is necessary to limit the number of I/O pins driving current in the user application.

- The total current sourced by all I/O pins on V_{DD} and the maximum operating current of the microcontroller on V_{DD} (during Run mode) must not exceed the absolute maximum rating ΣI_{VDD} specified in Table 12.
- The total current sunk by all I/O pins on GND and the maximum operating current of the microcontroller on GND (during Run mode) must not exceed the absolute maximum rating ΣI_{GND} specified in Table 12.

4.3.10.3 Output Voltage Levels

Unless otherwise specified, the parameters in Table 28 are obtained through tests conducted under ambient temperature and supply voltage conditions specified in Table 14.

Table 28. Output Voltage Characteristics

(Temperature: -40°C to +85°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{OL}	Output low level voltage for an I/O pin	V_{DD} = 5 V, I_{OL} = 15 mA	-	-	0.2 × V_{DD}	V
V_{OH}	Output high level voltage for an I/O pin	V_{DD} = 5 V, I_{OH} = –9 mA	0.8 × V_{DD}	-	-	

4.3.11 ADC Characteristics

Table 29. ADC Electrical Characteristics

(Temperature: -40°C to +85°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	unit
V_{DD}	Operating voltage	-	2.4	5	5.5	V
AVREF	Analog reference voltage	-	-	-	VDD	V
V_{AN}	Analog input range	-	VSS	-	AVREF	V
-	Resolution	-	-	-	12	bit
I_{DDA}	Operating current	VDD = 5.0 V @ fMCLK = 4.57 MHz	-	1	2	mA
ACLK	Input clock frequency		-	-	4.57	MHz
t_{CONV}	Conversion time	@ VDD ≥ 2.4 V	-	-	6.56	μs
		@ VDD ≤ 2.4 V	-	-	14.99	
F_{CONV}	Conversion frequency	@ VDD ≥ 2.4 V	-	-	152.38	kHz
		@ VDD ≤ 2.4 V	-	-	66.67	kHz
INL	DC accuracy	-	-	±4	±8	LSB
DNL		-	-	±1	±2	
ZOE	Zero offset error	-	-	±4	±8	
FSE	Full scale error	-	-	±6	±12	

NOTE:

1. Guaranteed by design.

Table 30. Recommended ADC Resolution

(Temperature: -40°C to +85°C)

V_{DD}[V]	Resolution	Condition
2.6	12-bit/Upper 12-bit	ACLK ≤ 0.5 MHz
2.5	12-bit/Upper 12-bit	
2.4	12-bit/Upper 12-bit	
2.3	12-bit/Upper 12-bit	
2.2	11-bit/Upper 11-bit	
2.1	10-bit/Upper 10-bit	
2.0	9-bit/Upper 9-bit	
1.9	8-bit/Upper 8-bit	
1.8	7-bit/Upper 7-bit	

NOTES:

1. When V_{DD} is lower than 2.2 V, the resolution will get worse.
2. If V_{DD} is less than or equal to 2.2 V, the resolution degrades by 1-bit whenever V_{DD} drops 0.1 V. (V_{DD} under 2.2 V resolution has no test.)
3. Guaranteed by design.

4.3.11.1 General PCB Design Guidelines

The power supply must be separated, as shown in Figure 14. The decoupling capacitors across the V_{DD}/AV_{DD} are ceramic (good quality) capacitors and must be placed as close as possible to the chip.

4.3.12 Comparator Characteristics

Table 31. Comparator Characteristics

(Temperature: -40°C to +85°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Operating voltage	-	2.4	5	5.5	V
I_{DD}	Operating current	-	-	-	115	μA
V_{IVR}	Input voltage range	-	GND +0.1	-	V_{DD} -0.1	V
V_{IO}	Input offset voltage	-	-	±4	±10	mV
t_D	Propagation delay	-	-	0.5	2	μs
V_{HYSS}	Hysteresis	HYSTSEL[1:0] = '00'	20	40	60	mV
		HYSTSEL[1:0] = '01'	40	80	120	
		HYSTSEL[1:0] = '10'	60	120	180	
		HYSTSEL[1:0] = '11'	80	160	240	

4.3.13 Communication Interfaces Characteristics

4.3.13.1 I2C Interface Characteristics

The I2C interface conforms to the timing requirements specified in the I2C-bus specification, in addition to the user timing requirements listed below:

- Standard mode (Sm): up to 100 kbps bit rate
- Fast mode (Fm): up to 400 kbps bit rate

The I2C timing requirements are guaranteed by design when the I2C peripheral is configured correctly, and the I2C clock frequency is equal to or greater than the minimum value listed in the table below.

Table 32. I2C Characteristics

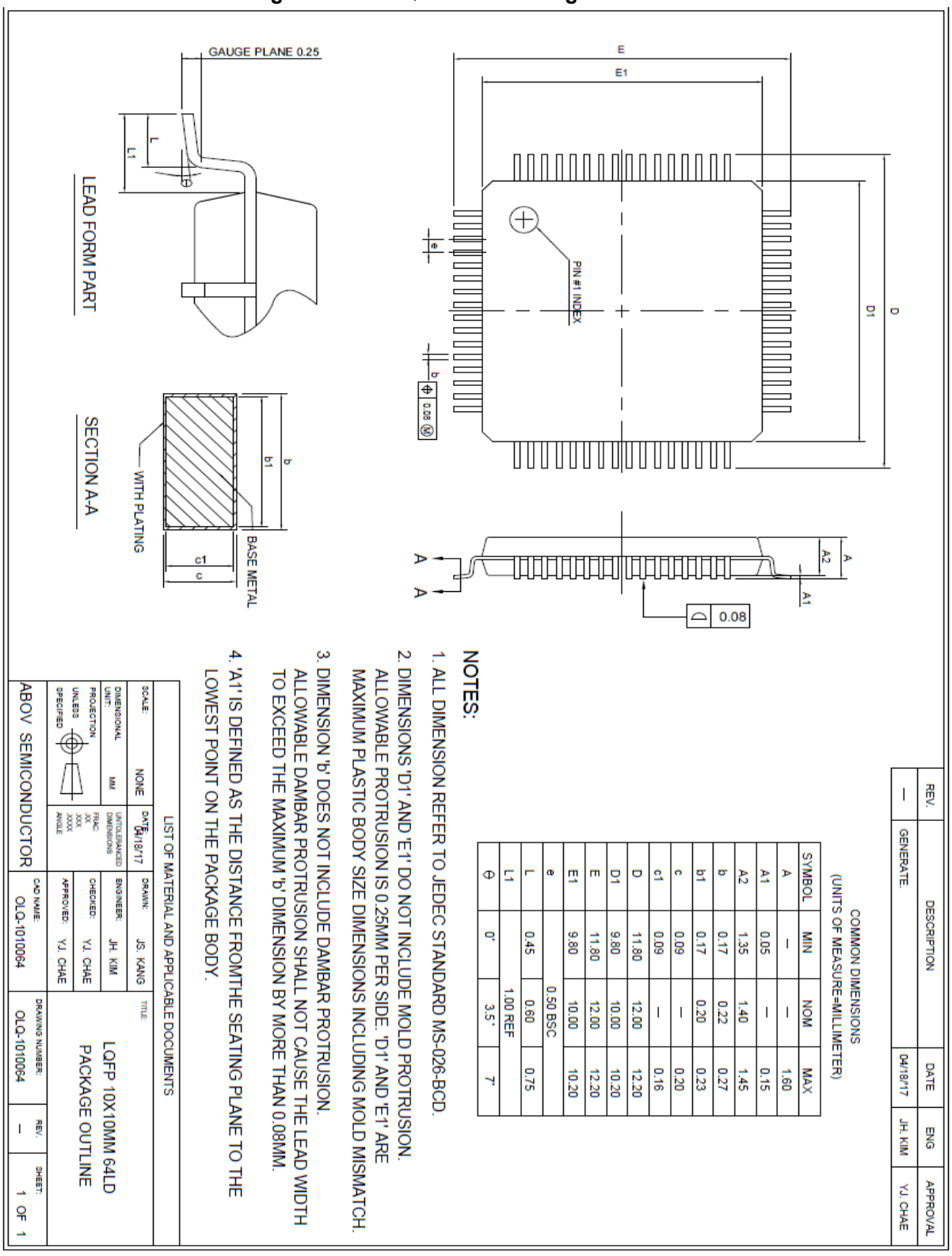
(Temperature: -40°C to +85°C)

Symbol	Parameter	Standard		Fast		Unit
		Min.	Max.	Min.	Max.	
t_{SCL}	Clock frequency	0	100	0	400	kHz
t_{SCLH}	Clock high pulse width	4.0	-	0.6	-	µs
t_{SCLL}	clock low pulse width	4.7	-	1.3	-	
t_{BF}	Bus free time	4.7	-	1.3	-	
t_{STSU}	Start condition setup time	4.7	-	0.6	-	
t_{STHD}	Start condition hold time	4.0	-	0.6	-	
t_{SPSU}	Stop condition setup time	4.0	-	0.6	-	
t_{SPHD}	Stop condition hold time	4.0	-	0.6	-	
t_{VD}	Output valid from clock	0	-	0	-	
t_{DIH}	Data input hold time	0	-	0	1.0	
t_{DIS}	Data input setup time	250	-	100	-	ns

5. Package Information

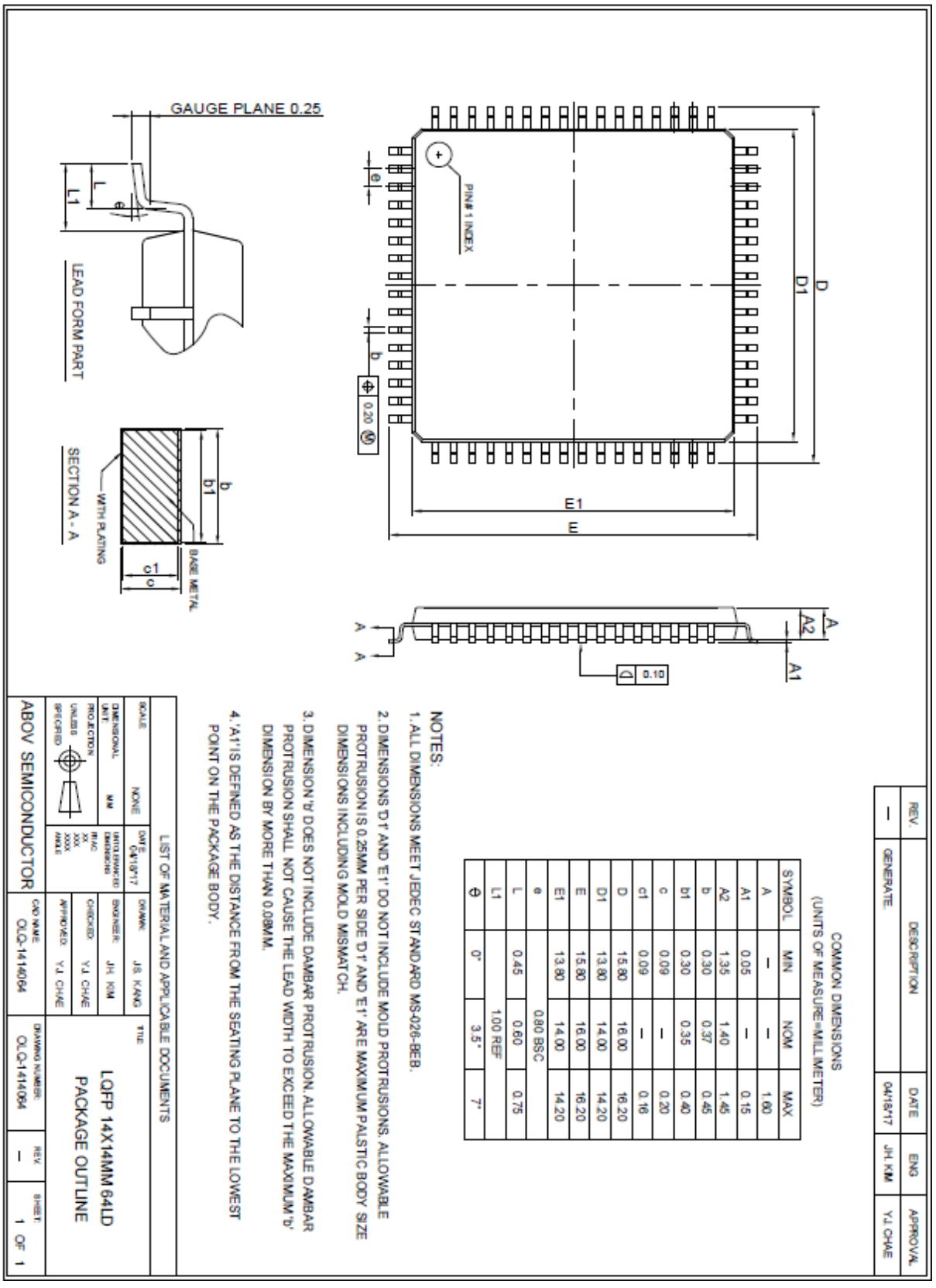
5.1 64-LQFP (10x10) Package Information

Figure 23. 64-LQFP-1010 Package Dimension



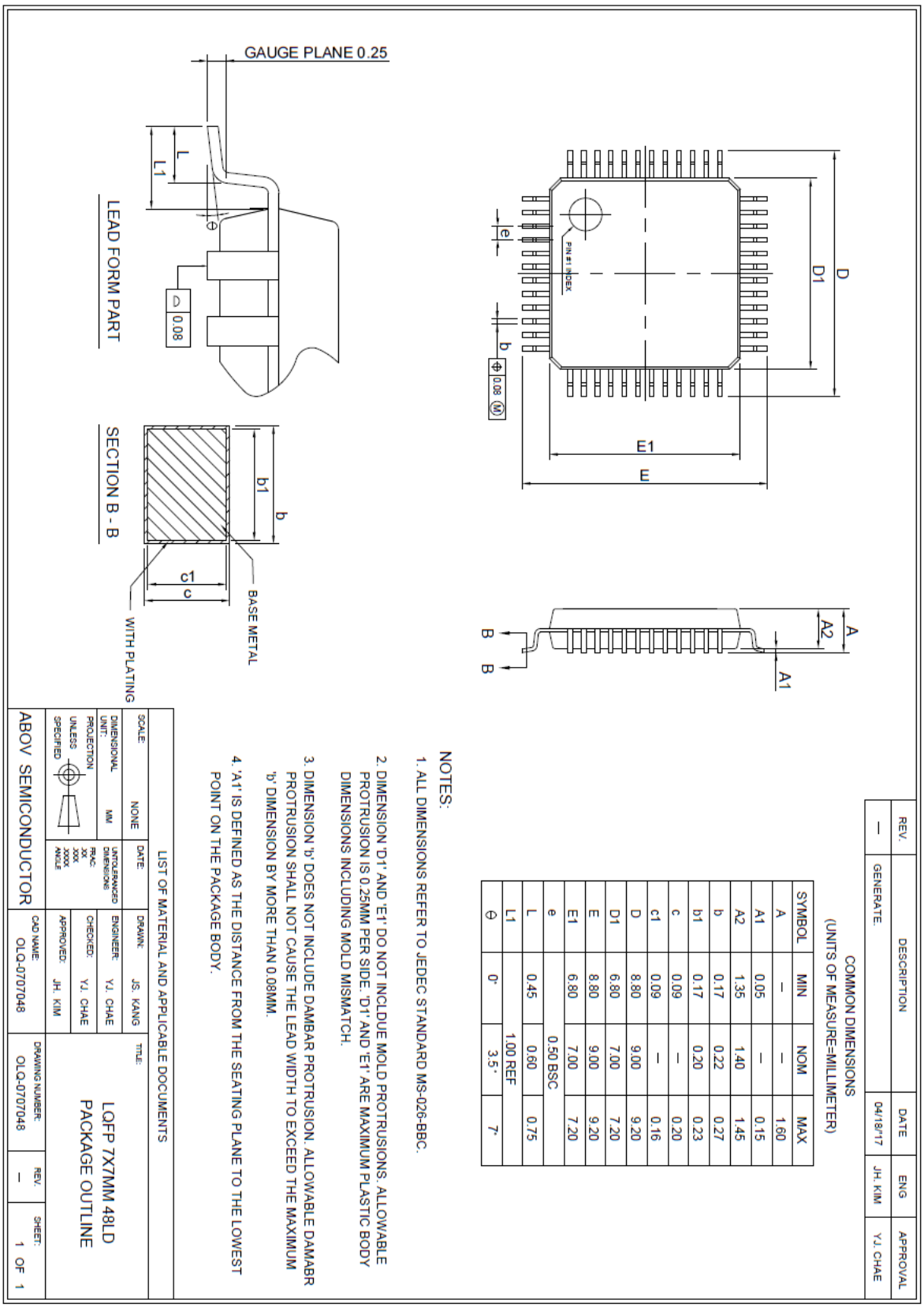
5.2 64-LQFP (14x14) Package Information

Figure 24. 64-LQFP-1414 Package Dimension



5.3 48-LQFP (7x7) Package Information

Figure 25. 48-LQFP-0707 Package Dimension



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	—	0.20
c1	0.09	—	0.16
D	8.80	9.00	9.20
D1	6.80	7.00	7.20
E	8.80	9.00	9.20
E1	6.80	7.00	7.20
e		0.50 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	3.5°	7°

NOTES:

1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026-BBC.
2. DIMENSION 'D1' AND 'E1' DO NOT INCLDUE MOLD PROTRUSIONS. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. 'D1' AND 'E1' ARE MAXIMUM PLASTIC BODY DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMABR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM 'b' DIMENSION BY MORE THAN 0.08MM.
4. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

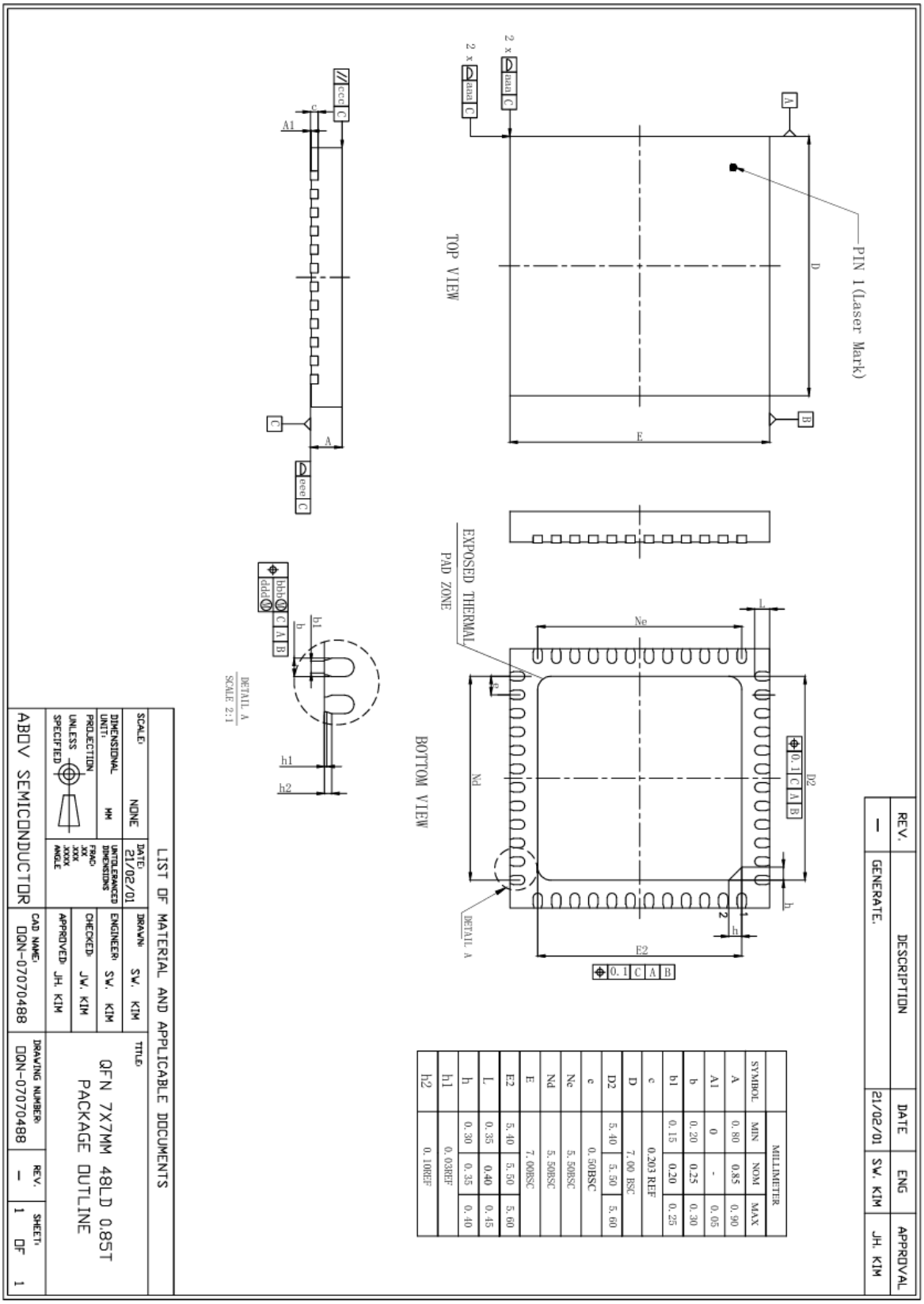
REV.	DESCRIPTION	DATE	ENG	APPROVAL
—	GENERATE.	04/18/17	JH. KIM	YJ. CHAE

LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE: NONE	DATE:	DRAWN: JS. KANG	TITLE: LQFP 7X7MM 48LD PACKAGE OUTLINE
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS FRAC: XX .XX .XXX ANGLE	ENGINEER: YJ. CHAE	
PROJECTION UNLESS SPECIFIED		CHECKED: YJ. CHAE	
ABOV SEMICONDUCTOR	CAD NAME: OLQ-0707048	APPROVED: JH. KIM	DRAWING NUMBER: OLQ-0707048 REV.: — SHEET: 1 OF 1

5.4 48-QFN (7x7) Package Information

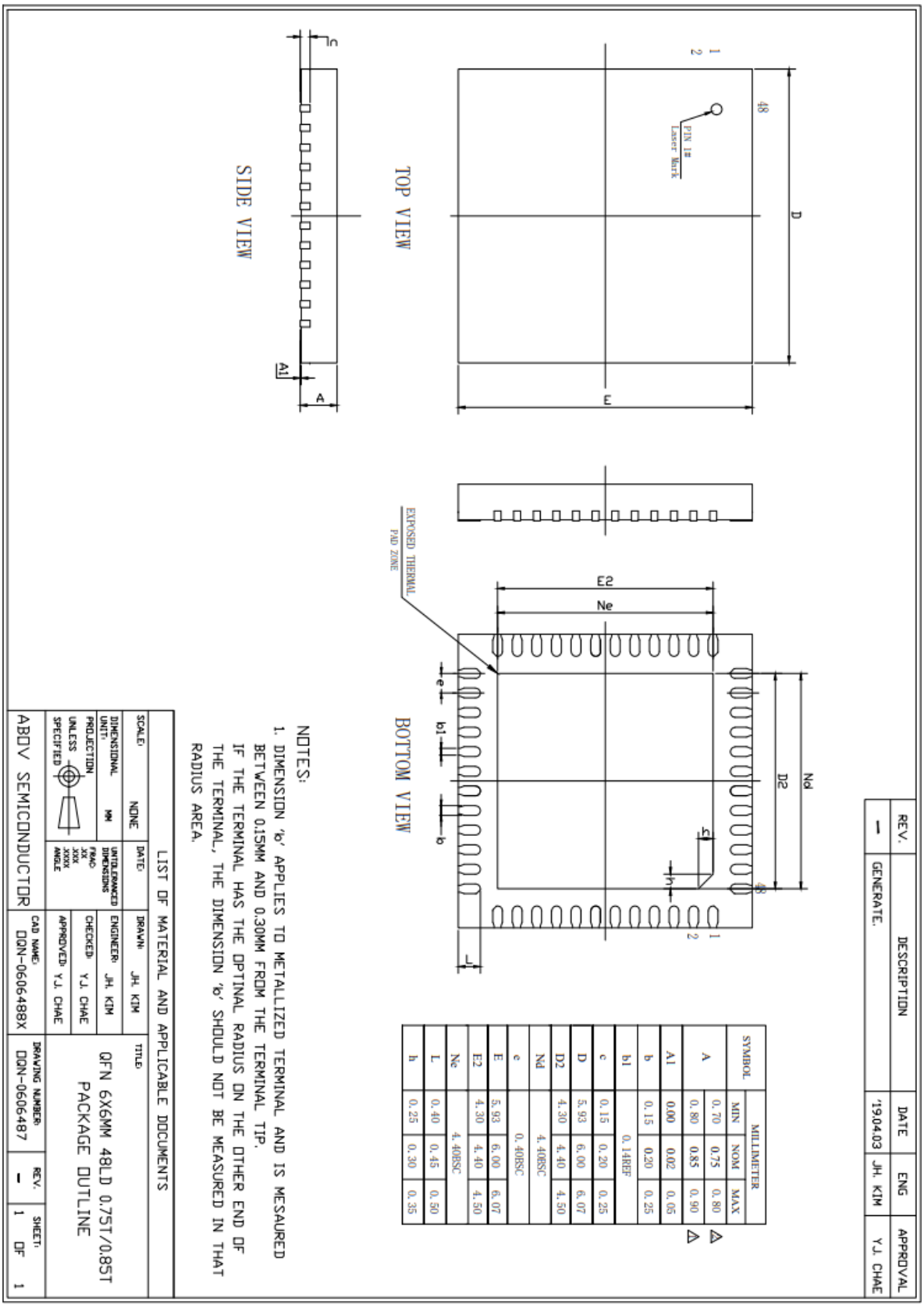
Figure 26. 48-QFN-0707 Package Dimension



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	-	0.05
b	0.20	0.25	0.30
b1	0.15	0.20	0.25
c		0.203 REF	
D		7.00 BSC	
D2	5.40	5.50	5.60
e		0.50BSC	
Ne		5.50BSC	
Nd		5.50BSC	
E		7.00BSC	
E2	5.40	5.50	5.60
L	0.35	0.40	0.45
h	0.30	0.35	0.40
h1		0.03REF	
h2		0.10REF	

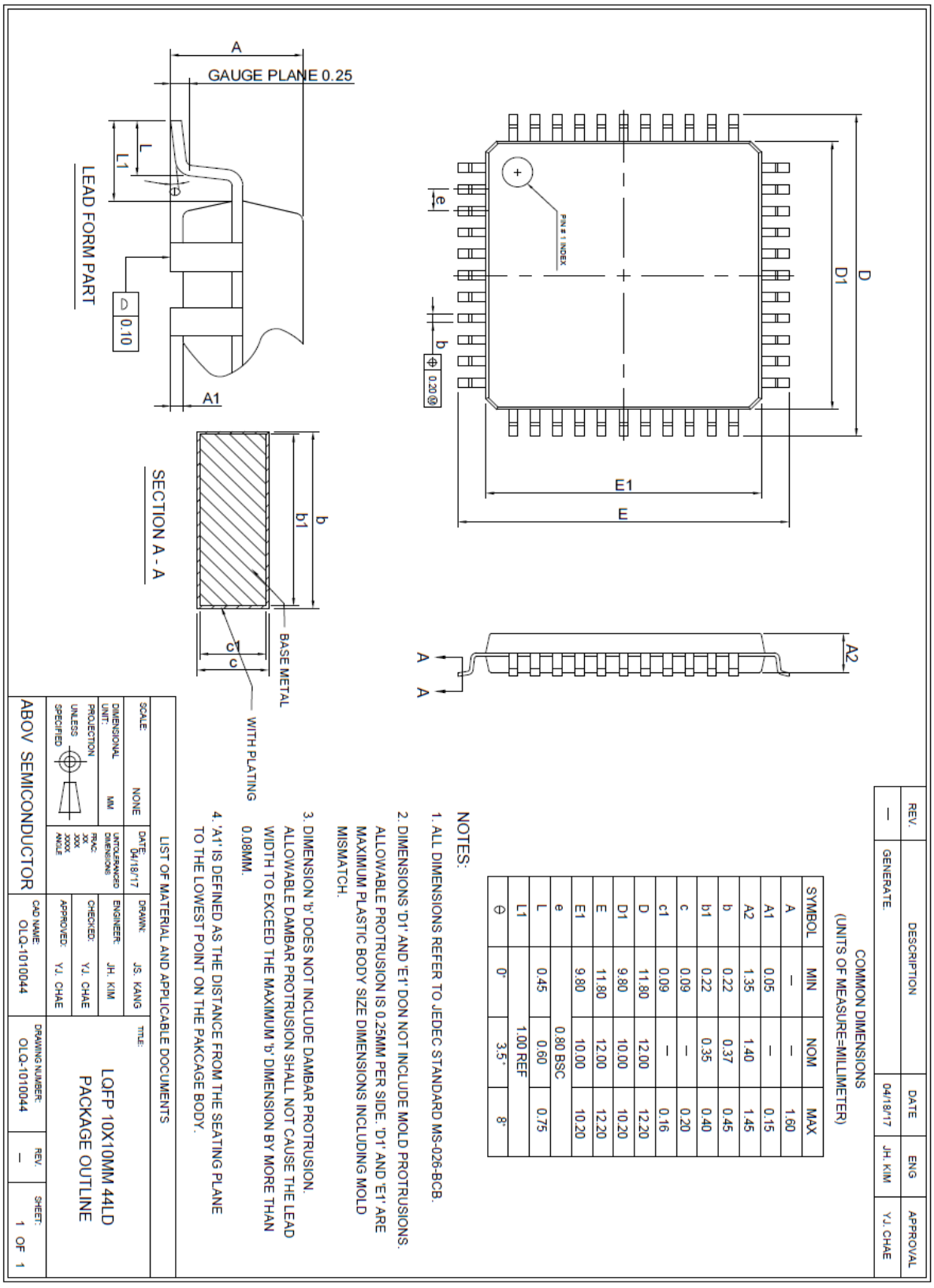
5.5 48-QFN (6x6) Package Information

Figure 27. 48-QFN-0606 Package Dimension



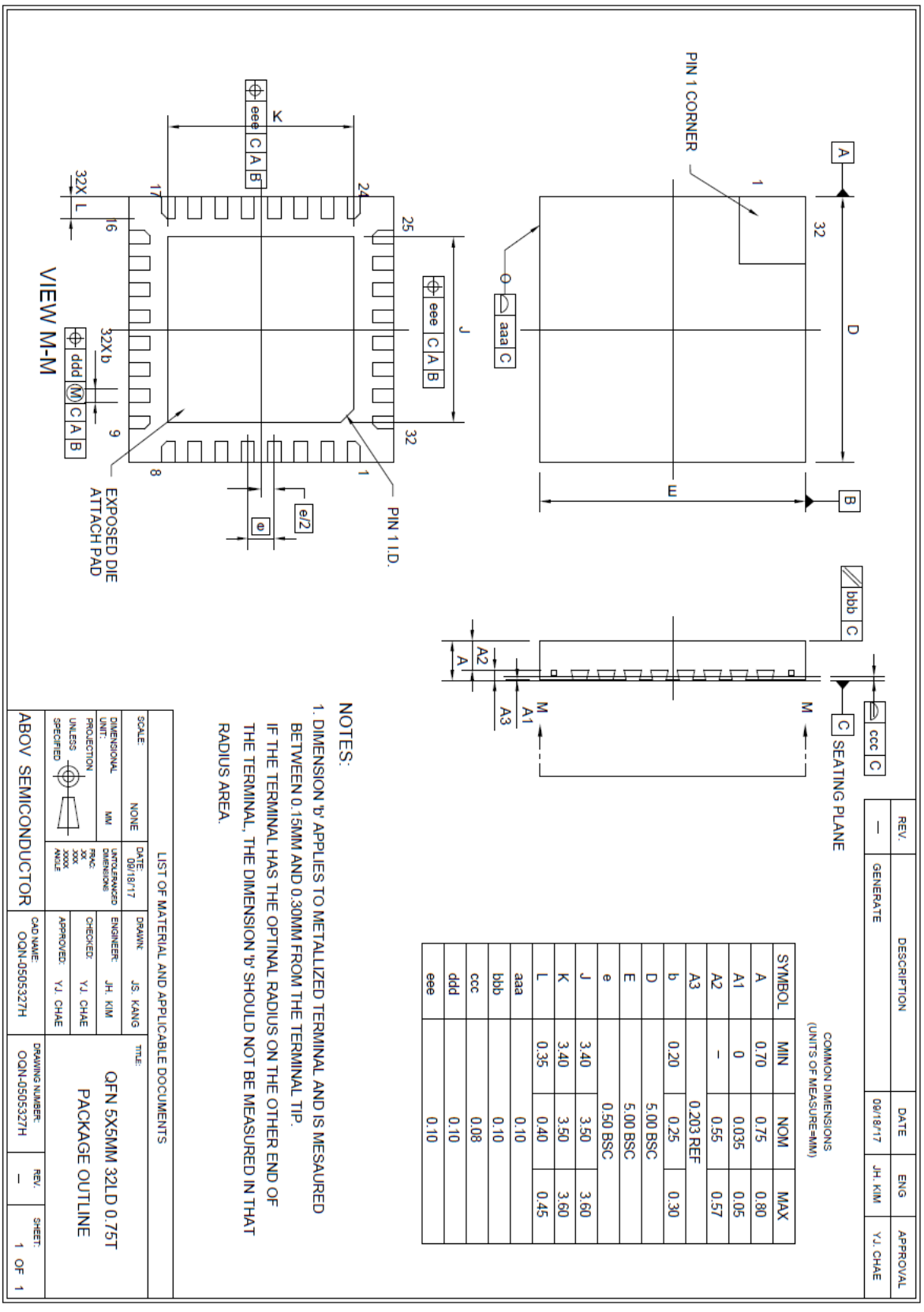
5.6 44-LQFP (10x10) Package Information

Figure 28. 44-LQFP-1010 Package Dimension



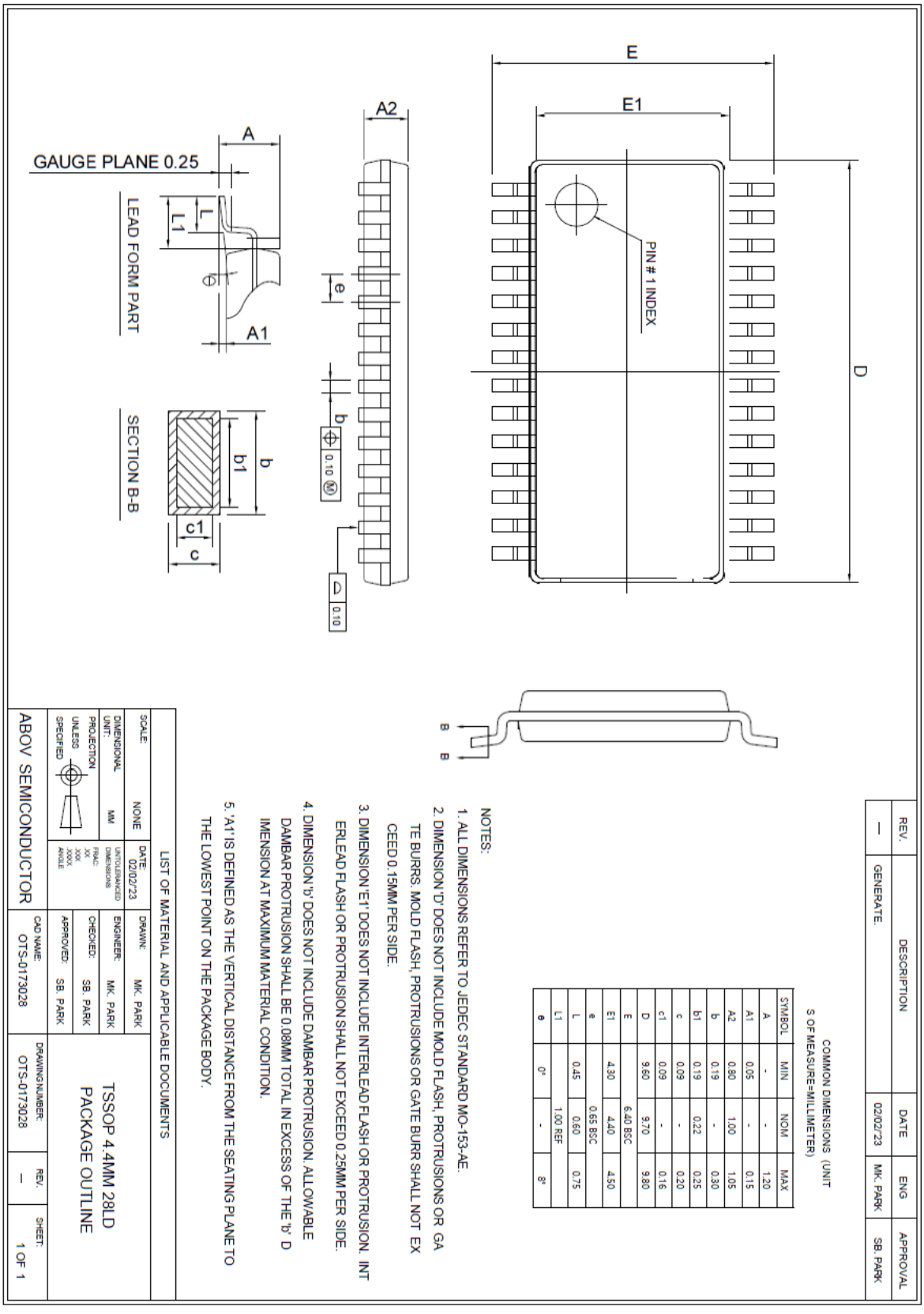
5.7 32-QFN (5x5) Package Information

Figure 29. 32-QFN-0505 Package Dimension



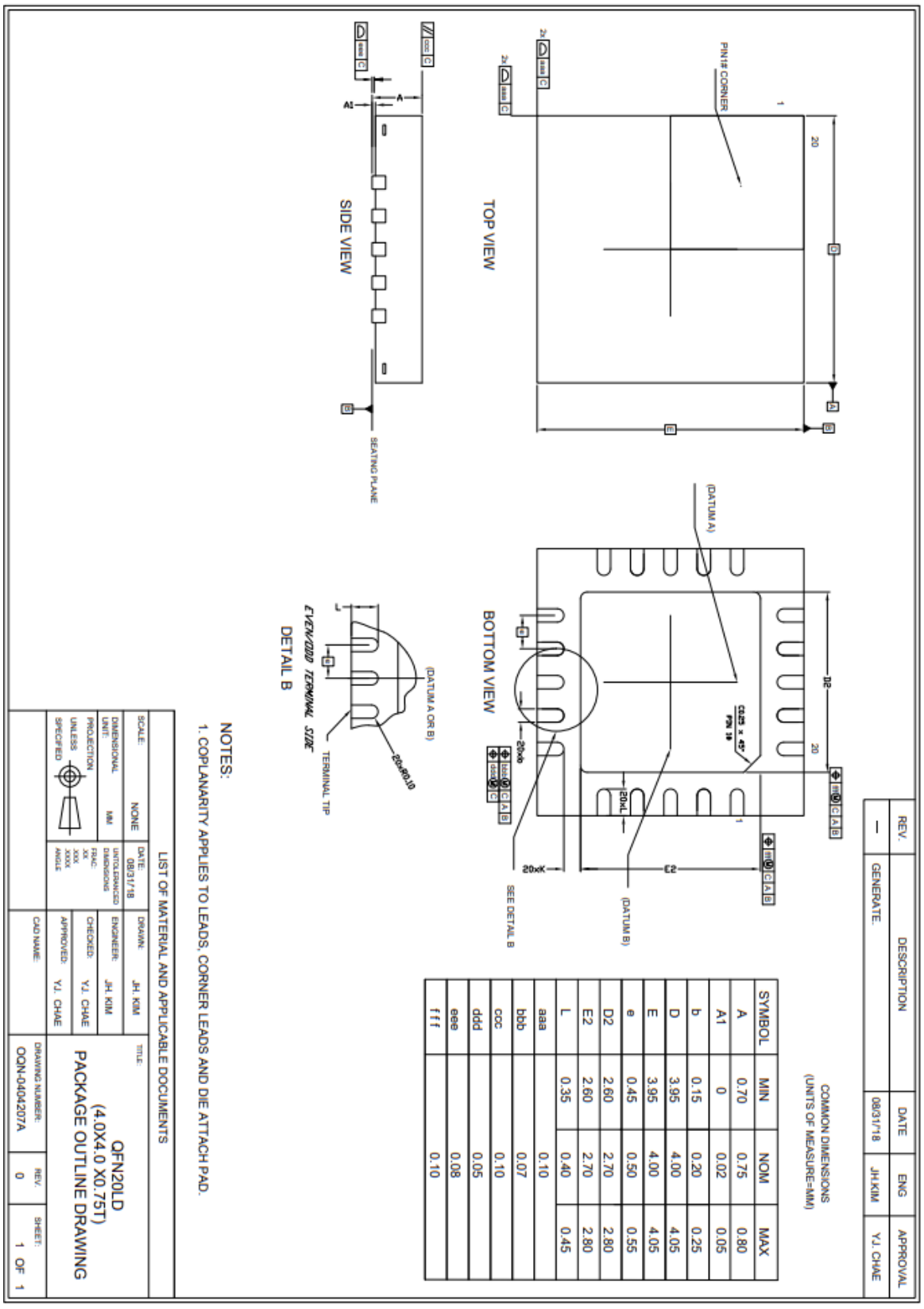
5.8 28-TSSOP Package Information

Figure 30. 28-TSSOP Package Dimension



5.9 20-QFN (4x4) Package Information

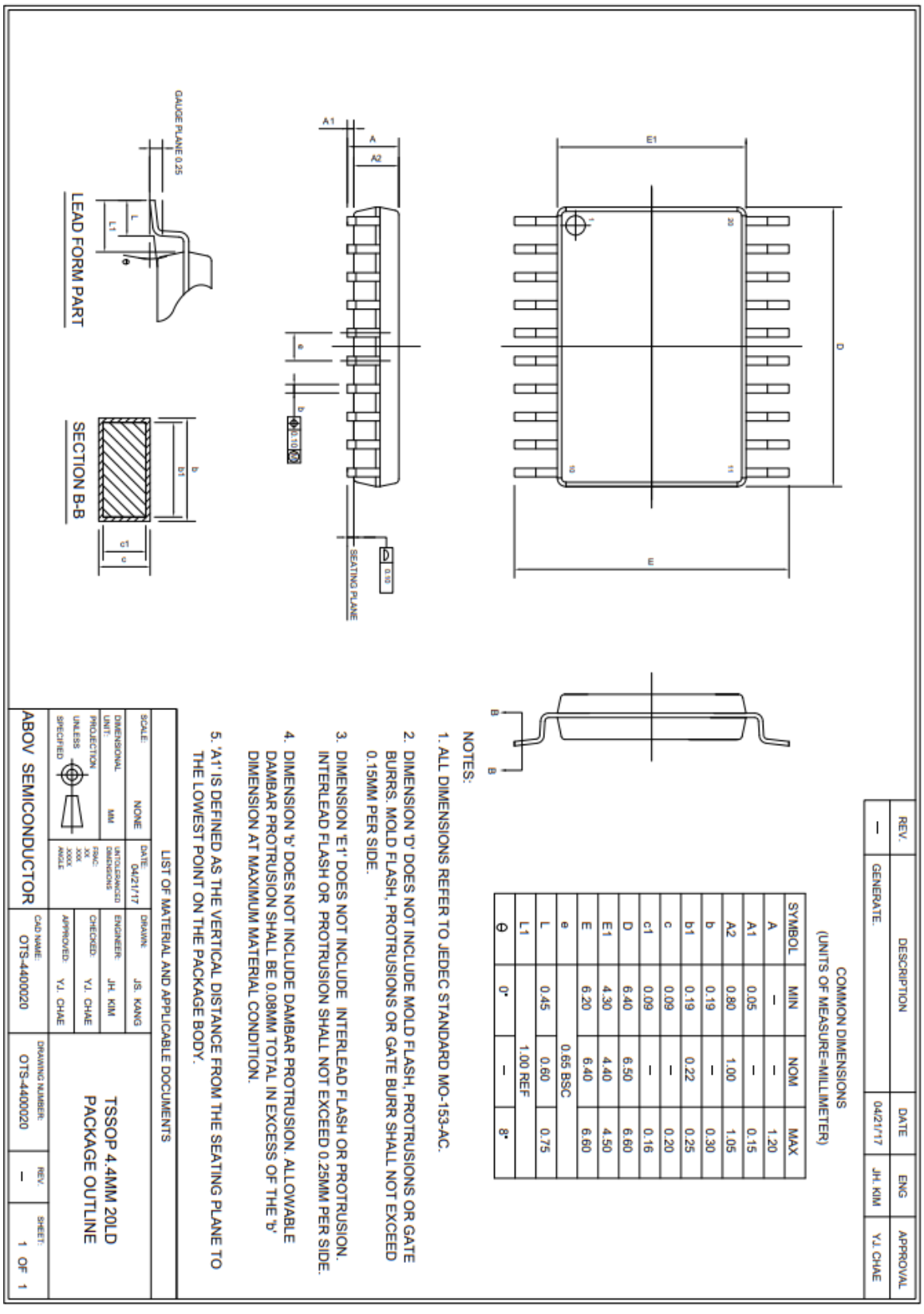
Figure 31. 20-QFN-0404 Package Dimension



SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
D	3.95	4.00	4.05
E	3.95	4.00	4.05
e	0.45	0.50	0.55
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
L	0.35	0.40	0.45
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

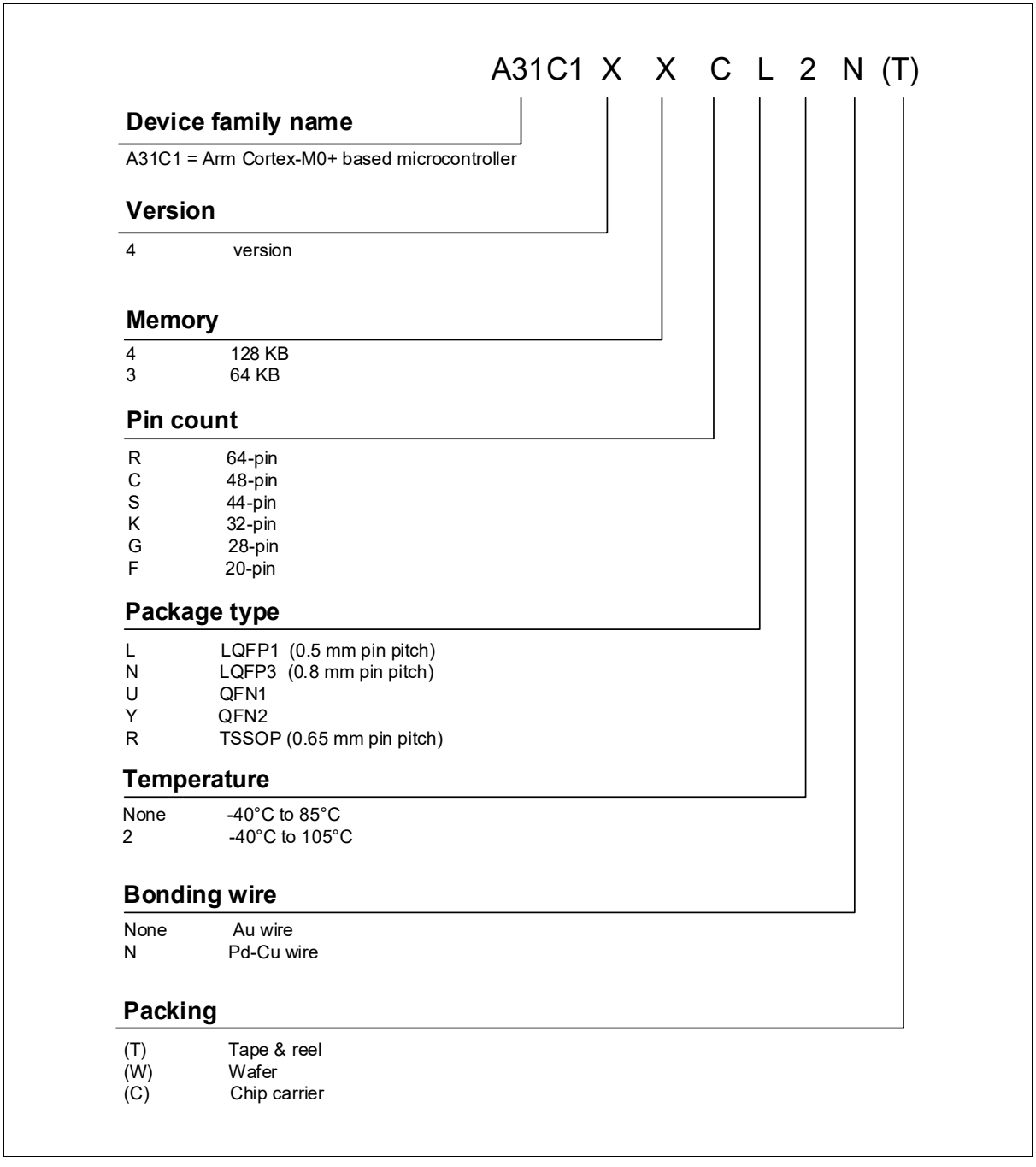
5.10 20-TSSOP Package Information

Figure 32. 20-TSSOP Package Dimension



6. Ordering Information

Figure 33. Device Numbering Nomenclature – Part Number Decoder



NOTE:

1. For a list of available options (memory, package, etc.) or further information on any aspect of this device, contact the nearest ABOV sales office.

Revision History

Revision	Date	Notes
1.00	Sep. 26, 2025	Initial release
1.01	Jan. 30, 2026	• Updated the minimum operating voltage value for ADC and CMP in Table 14 • Updated ADC input clock frequency in Table 29 • Added Section 4.3.5
1.02	Jul. 30, 2026	• Modified Figure 14 and Table 26 • Modified start-up time in Table 21. HSE Oscillator Characteristics (1) • Added additional content to Table 24. LSI Oscillator Characteristics (1) • Added New Package (20-QFN/20-TSSOP) • Modified Flash Endurance Cycles in Table 3 and Table 25 • Modified the default configuration of PD0, PD1, PE2, and PE3 pins in Table 9
1.03	Aug. 24, 2026	Added a new package (48-QFN 7x7)

Korea

Regional Office, Seoul
R&D, Marketing & Sales
8th Fl., 330, Yeongdong-daero, Gangnam-gu, Seoul,
06177, Korea

Tel: +82-2-2193-2200
Fax: +82-2-508-6903
www.abovsemi.com

HQ, Ochang
R&D, QA, and Test Center
37, Gangni 1-gil, Ochang-eup, Cheongwon-gun,
Chungcheongbuk-do, 28126, Korea

Tel: +82-43-219-5200
Fax: +82-43-217-3534
www.abovsemi.com

Domestic Sales
Tel: +82-2-2193-2206
Fax: +82-2-508-6903
Email: sales_kr@abov.co.kr

Global Sales
Tel: +82-2-2193-2281
Fax: +82-2-508-6903
Email: sales_gl@abov.co.kr

China Sales
Tel: +86-755-8287-2205
Fax: +86-755-8287-2204
Email: sales_cn@abov.co.kr

Japan Sales
Tel: +81-6-6225-7758

Email: sales_jp@abov.co.kr

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