# A31C12x Datasheet

## Cortex®-M0+ 32-bit Microcontroller, 32 MHz, Up to 32 KB Code Flash, 6 KB SRAM, 12-bit ADC

DS Rev. 1.02

# Features

### Core

- Arm® 32-bit Cortex® -M0+ Core
- Up to 32 MHz

### Memories

- Up to 32 KB code flash memory
- 6 KB SRAM

### Reset and Power Management

- Power-on/power-down reset (POR/LVR/LVI)
- Low-power modes: SLEEP, DEEP-SLEEP (STOP1, STOP2)

### Clock Management

- High-Speed Internal Oscillator 32 MHz (HSI)
  - ±1.0% @0°C to +65°C
  - ±1.5% @-20°C to +85°C
  - ±2.5% @-40°C to +85°C
- Low-Speed Internal Oscillator 32 kHz (LSI)
  - ±30% @ −40°C to +85°C
- High-Speed External Oscillator (HSE)
  - 4 MHz to 12 MHz
- Low-Speed External Oscillator (LSE)
  - 32.768 kHz

### GPIO

- Up to 30 general-purpose I/O pins with interrupt capability
- All mappable on external interrupt vectors
- Multi-function pins capable of selecting for up to six different functions, including GPIO.

### DMAC

- Up to 4-channel DMAs
- 8-/16-/32-bit data transfers
- Compatible with eight different types of peripherals

### WDT

- 32-bit down-count timer
- Reset and periodic interrupts
- Eight different prescalers

### FRT

- 32-bit Free-Run Timer

### 16-bit Timer

- Up to 7 channels
  - 7-input capture channels
  - 7-output channels
- Timer operating modes:
  - Periodic timer mode
  - One-shot mode
  - PWM mode
  - Capture mode
- 10-bit prescaler

### Serial Interfaces

- UART × 1
- USART × 2
- I2C × 2

### 12-bit ADC

- One unit of 12-bit ADC
- Up to 13-channel of analog inputs
- Multiple operating modes:
  - Single conversion
  - Sequence conversion
  - Burst conversion
  - Multiple conversion

### CRC Calculation Unit

- CRC operating modes:
  - CRC32 (0x04C1_1DB7)
  - CRC16-USB (0x8005)
  - CRC16-CCITT (0x1021)
  - CRC8-CCITT (0x07)
- Support for byte reversal of input/output data
- Compatible with DMA

### Development Support

- Serial Wire Debug (SWD) interface

### Operating Voltage

- 1.8 V to 5.5 V

### Operating Temperature

Commercial grade (−40°C to +85°C)

### Package

- 32-QFN-0505 (0.5mm pitch)
- 32-LQFP
- 28-TSSOP
- 24-QFN
- 20-QFN
- 20-TSSOP

### Family Members

- A31C122: 32 KB of flash, 6 KB of SRAM
- A31C121: 16 KB of flash, 6 KB of SRAM

### Applications

- General Purpose

# Product Selection Table

**Table 1. Device Summary**

| Part Number | Flash | SRAM | USART | UART | I2C | ADC | TIMER | I/O Port | Package |
|---|---|---|---|---|---|---|---|---|---|
| A31C122KYN | 32 KB | 6 KB | 2** | 1 | 2 | 13 | 7 | 30 | 32-QFN |
| A31C122KNN | 32 KB | 6 KB | 2** | 1 | 2 | 13 | 7 | 30 | 32-LQFP |
| A31C122GRN* | 32 KB | 6 KB | 2** | 1 | 2 | 9 | 7 | 26 | 28-TSSOP |
| A31C122LUN* | 32 KB | 6 KB | 2** | 1 | 2 | 8 | 7 | 22 | 24-QFN |
| A31C122FUN* | 32 KB | 6 KB | 1 | 1 | 2 | 8 | 7 | 18 | 20-QFN |
| A31C122FRN* | 32 KB | 6 KB | 1 | 1 | 2 | 8 | 7 | 18 | 20-TSSP |
| A31C121KYN* | 16 KB | 6 KB | 2** | 1 | 2 | 13 | 7 | 30 | 32-QFN |
| A31C121KNN* | 16 KB | 6 KB | 2** | 1 | 2 | 13 | 7 | 30 | 32-LQFP |
| A31C121GRN* | 16 KB | 6 KB | 2** | 1 | 2 | 9 | 7 | 26 | 28-TSSOP |
| A31C121LUN* | 16 KB | 6 KB | 2** | 1 | 2 | 8 | 7 | 22 | 24-QFN |
| A31C121FUN* | 16 KB | 6 KB | 1 | 1 | 2 | 8 | 7 | 18 | 20-QFN |
| A31C121FRN* | 16 KB | 6 KB | 1 | 1 | 2 | 8 | 7 | 18 | 20-TSSP |

* For available options or further information on the device with "*" marks, please contact the ABOV sales office.

** UART: 2, SPI: 1

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# 1. Introduction

This document provides an overview of the features supported by A31C12x series, including high-level information and brief explanation of each feature.

Refer to Table 3 for the list of features supported by the A31C12x series.

# 2. Descriptions

The A31C12x series is the high-performance and energy-efficient 32-bit microcontroller based on Arm Cortex-M0+ core, with up to 32 KB of flash memory and 6 KB of SRAM.

## 2.1 Product Category Definition

Table 2 provides an overview of the memory capacity for available devices in the A31C12x series.

This document provides an overview of the features supported by each device, including high-level information and brief explanations for each feature.

Refer to Table 3 for the list of features supported by product category.

**Table 2. A31C12x Series Memory Capacity**

| Device | Memory capacity | |
|---|---|---|
| | Flash | RAM |
| A31C122 | 32 KB | 6 KB |
| A31C121 | 16 KB | 6 KB |

## 2.2 Device Overview

Table 3 summarizes and lists the features specific to the device in the A31C12x series while considering the largest package.

**Table 3. A31C12x Series Features**

| Peripheral | | Description |
|---|---|---|
| Core | CPU | • Max. operating frequency: 32 MHz<br>• 32-bit Arm Cortex-M0+ Core<br>• Register settings in CPU:<br>- Uses general-purpose registers specified by the 32-bit Thumb instruction set: R0-R12<br>- Main Stack Pointer (MSP) and Process Stack Pointer (PSP): R13<br>- Link Register (LR): R14<br>- Program Counter (PC): R15<br>• Data alignment in little-endian<br>• Von Neumann Architecture<br>• AHB/APB |
| | Interrupt | • NVIC (Nested-Vectored Interrupt Controller)<br>• Up to 32 peripheral interrupts available.<br>• 2-bit width of group priority: four levels of priority |
| Memory | Code Flash | • Capacity:<br>- A31C122: 32 KB<br>- A31C121: 16 KB<br>• Erase unit: Page (512 bytes), sector (2 KB) or bulk (full chip)<br>• Program unit: Word (4 bytes)<br>• Read-Protection<br>• Self-programming<br>• CRC code generation and verification for the flash memory<br>• Endurance:<br>- A31C122:<br>Page 0 to 59 (30 KB): 10,000 cycles<br>Page 60 to 63 (2 KB): 100,000 cycles<br>- A31C121:<br>Page 0 to 27 (14 KB): 10,000 cycles<br>Page 28 to 31 (2 KB): 100,000 cycles<br>• Lifetime: 10 years |
| | SRAM | • Capacity: 6 KB<br>• Capable of functioning as a program's working area<br>• High-speed execution for time-critical codes<br>• Capability to remap into an interrupt vector area |
| | Boot ROM | • Initiating the microcontroller's boot mode by receiving an external input signal at the nBOOT pin<br>• UART mode of USART10<br>• In-system programming<br>• Users can store information in the internal flash memory by using an application board to write data to the memory. |

**Table 3. A31C12x Series Features (continued)**

| Peripheral | | Description |
|---|---|---|
| SCU (System Control Unit) | Clock | • High-Speed Internal (HSI) oscillator: 32 MHz<br>- ±1.0% @ 0°C to +65°C<br>- ±1.5% @-20°C to +85°C<br>- ±2.5% @-40°C to +85°C<br>• Low-Speed Internal Oscillator (LSI): 32 kHz<br>- ±30% @ −40°C to +85°C<br>• High-Speed External (HSE) main oscillator: 4 MHz to 12 MHz<br>• Low-Speed External (LSE) sub-oscillator: 32.768 kHz |
| | Clock Monitoring | • System Fail-Safe function by clock monitoring<br>- High-Speed External (HSE) main oscillator<br>- Low-Speed External (LSE) sub-oscillator<br>- Main system clock (MCLK) |
| | Operation Mode | • RUN mode<br>• SLEEP mode<br>• DEEP-SLEEP (STOP1, STOP2) mode |
| | Reset | • nRESET Pin reset (PC9)<br>• Core reset<br>• Software reset<br>• POR (Power-On Reset)<br>• LVR (Low Voltage Reset)<br>• WDTR (Watch Dog Timer Reset)<br>• Reset due to clock oscillating error |
| | VDC | Low-Dropout (LDO) regulator built in for low voltage operation |
| | POR | POR generator: Capable of generating a reset signal by detecting an internal 1.48 V |
| | LVDI | • Four Low-voltage detection levels<br>• Supports interrupts<br>• Supports wake-up from DEEP-SLEEP mode |
| | Wake-up | • Wake-up by GPIO pin<br>• Wake-up by FRT<br>• Wake-up by WDT<br>• Wake-up by LVI<br>• Wake-up by USART |
| DMA (Direct Memory Access) Controller | | • Direct Memory Access (DMA) supporting peripherals<br>- Four channels<br>• 8- /16- /32-bit data transfers<br>• Compatible with 12 different types of peripherals<br>• UART0, USART10, USART11, CRC, ADC |

**Table 3. A31C12x Series Features (continued)**

| Peripheral | | Description |
|---|---|---|
| GPIO (General-Purpose I/O) | | • Input/Output (I/O) port for general purpose<br>• 32-QFN, 32-LQFP<br>- I/O pins: 30<br>• 28-TSSOP<br>- I/O pins: 26<br>• 24-QFN<br>- I/O pins: 22<br>• 20-QFN, 20-TSSOP<br>- I/O pins: 18<br>• Selectable input and output configuration for each pin:<br>- Push-pull output<br>- Open drain output<br>- Input<br>• Pin configurations through multiplexer settings<br>• Configurable as an external interrupt source with the following options:<br>- Rising-edge (high-level)<br>- Falling-edge (low-level)<br>- Edge-triggered (both rising-edge and falling-edge)<br>• Configurable pull-up/down resistors and debouncing<br>• Configurable independently to be set or reset through its corresponding bit<br>• Wake-up events triggered by external asynchronous inputs |
| Timer | 16-bit Timer | • General-purpose 16-bit up-count timer<br>• Seven channels<br>- 7 input capture and output channels (TnIO)<br>• Timer operating modes<br>- Periodic timer mode<br>- One-shot mode<br>- PWM mode<br>- Capture mode<br>• Interrupt events<br>- Timer/counter match interrupt<br>- Timer overflow interrupt<br>• Free selectable clock sources:<br>- PCLK configurable through the peripheral clock enable register1 (SCU_PCER1)<br>- LSI, LSE, MCLK, HSI, HSE configurable through the miscellaneous clock control register 3 (SCU_MCCR3)<br>• Timer signals output through TnIO pins<br>• 10-bit prescaler |
| | WDT | • 32-bit down-count timer<br>• Reset and periodic interrupts<br>• Free selectable clock sources:<br>- LSI, LSE, HSI, HSE configurable through the miscellaneous clock control register 1 (SCU_MCCR1)<br>• Selectable eight different prescalers |

**Table 3. A31C12x Series Features (continued)**

| Peripheral | | Description |
|---|---|---|
| Timer | FRT | • 32-bit Free-Run Timer<br>- Timer for system time measurement<br>- 32-bit up-count timer<br>• Interrupt event<br>- Period interrupt<br>- Overflow interrupt |
| Serial Interface | UART | • 16450 asynchronous serial communication ports<br>• Channel support<br>- One channel<br>• Configurable standard asynchronous communication bits (start, stop, and parity)<br>• Flexible communication available through programming<br>- 5- to 8-bit data transfers<br>- Even/Odd/Non-parity generation and checking<br>- 1-bit, 1.5-bit, or 2-bit stop-bit generation and checking<br>• 8-bit fraction controller and 16-bit baud rate generator |
| | I2C | • Standard I2C communication protocol<br>• Channel support<br>- Two channels<br>• Master and slave modes<br>• 7-bit addressing for slave mode<br>• Configurable SCL signal's high-/low-periods and SDA signal's hold time |
| | USART | • Full Duplex Operation. (Independent Serial Receive and Transmit Registers)<br>• Channel support<br>- Two channels (UART:2, SPI:1)<br>• Asynchronous or Synchronous Operation<br>• 8-bit fraction controller and 16-bit baud rate generator<br>• Flexible communication available through programming<br>- 5- to 9-bit data transfers<br>- Even/Odd/Non-parity generation and checking<br>- 1-bit, 2-bit stop bit generation and checking<br>• Receive Character Detection and Receive Time Out function<br>• Data overrun & Frame error detection<br>• Three Separate Interrupts on TX Completion, TX Data Register Empty and RX Completion<br>• Double Speed Asynchronous communication mode |
| 12-bit ADC | | • One independent ADC block<br>• 13 channels of analog input<br>• Multiple operating modes:<br>- Single conversion<br>- Sequence conversion<br>- Burst conversion<br>- Multiple conversion<br>• Up to eight sequential conversions<br>• Software triggers<br>• internal trigger sources (Timers)<br>• Adjustable sample time and hold time |

**Table 3. A31C12x Series Features (continued)**

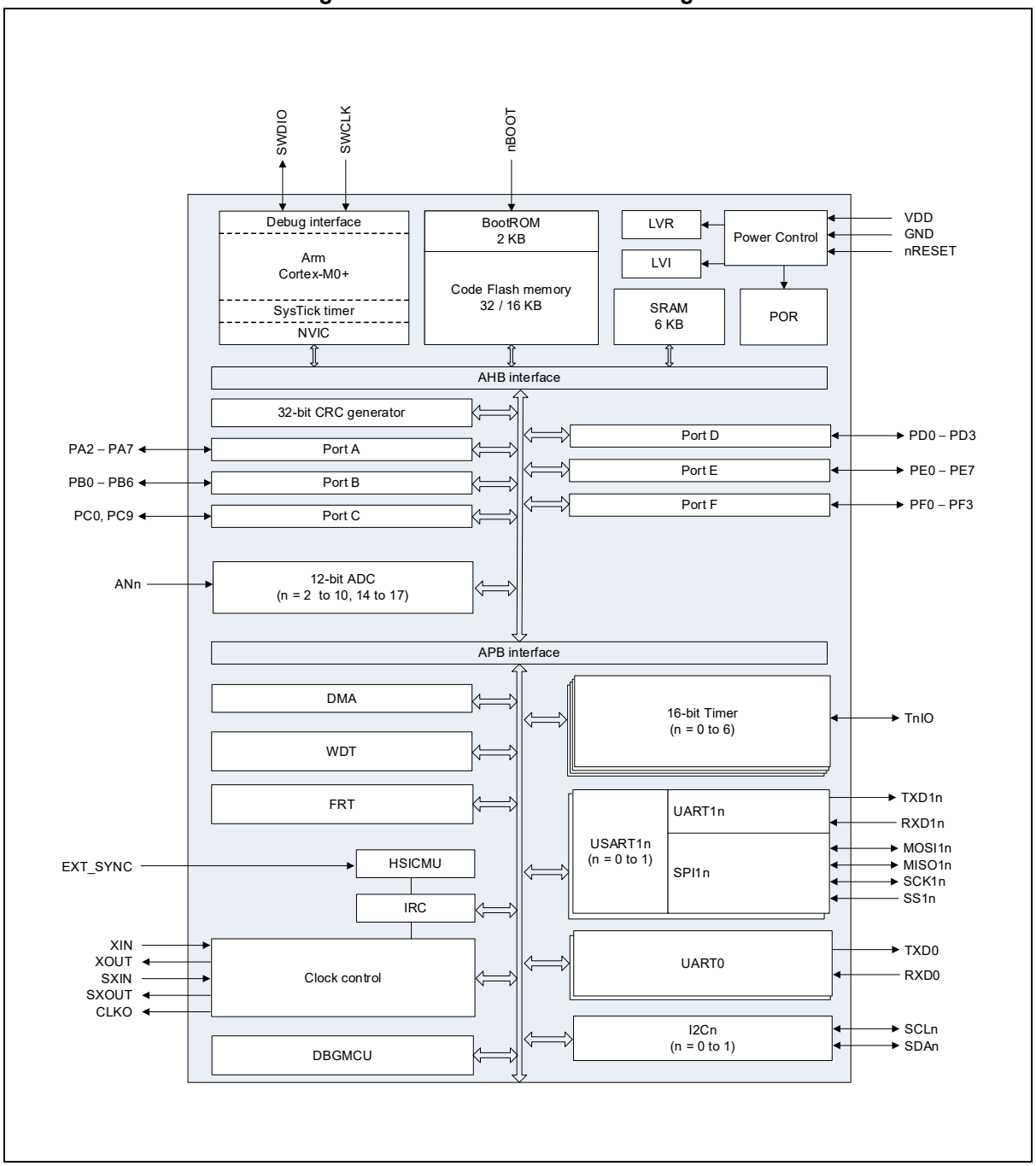
| Peripheral | Description |
|---|---|
| CRC<br>(Cyclic Redundancy Check) | • CRC operating modes:<br>- CRC32 (0x04C1_1DB7)<br>- CRC16_USB (0x8005)<br>- CRC16_CCITT (0x1021)<br>- CRC8_CCITT (0x07)<br>• Support for byte reversal of input/output data<br>• Compatible with DMA |
| Operating frequency | Up to 32 MHz |
| Operating voltage | 1.8 V to 5.5 V |
| Operating temperature | Commercial grade (−40°C to +85°C) |
| Package | • Six types of package options<br>- 32-QFN-0505<br>- 32-LQFP<br>- 28-TSSOP<br>- 24-QFN-0404<br>- 20-QFN-0404<br>- 20-TSSOP |

**Table 4. Summary of A31C12x Peripherals**

| Peripheral | | A31C12xKYN/KNN | A31C12xGRN | A31C12xLUN | A31C12xFRN/FUN |
|---|---|---|---|---|---|
| Code flash memory | | 32 KB / 16 KB | | | |
| SRAM | | 6 KB | | | |
| Timers | General Purpose | 7 (16-bit) | | | |
| | SysTick | 1 | | | |
| | WDT | 1 | | | |
| | FRT | 1 | | | |
| Communication Interfaces | UART | 1 | | | |
| | I2C | 2 | | | |
| | USART | 2 (UART: 2 or SPI: 1) | | | 1 |
| DMA | | 4 | | | |
| GPIO | | 30 | 26 | 22 | 18 |
| ADCs | | 150 ksps | | | |
| Number of channels | | 13 | 9 | 8 | 8 |
| CRC | | 1 | | | |
| Max. Operating frequency | | 32 MHz | | | |
| Operating voltage | | 1.8 V to 5.5 V | | | |
| Operating temperature | | Ambient operating temperature: −40°C to +85°C | | | |
| Packages | | 32-QFN/ 32-LQFP | 28-TSSOP | 24-QFN | 20-TSSOP/ 20-QFN |

## 2.3 Block Diagram

**Figure 1. A31C12x Series Block Diagram**



## 2.4 Functional Overview

The following sections provide overviews of the features of the A31C12x series microcontroller.

### 2.4.1 Cortex-M0+ Core

The A31C12x series adopts the energy-efficient 32-bit microcontroller core, Cortex-M0+ of Arm, as its CPU. The Cortex-M0+, designed for low-power consumption, uses the ARMv6-M Instruction set to improve performance and energy efficiency.

Refer to the technical reference manual "ARM DDI 0484C" for detailed information on Cortex-M0+.

### 2.4.2 Embedded SRAM

The A31C12x series has a block of zero-wait on-chip SRAM. The size of the SRAM is 6KB. The base address is 0x2000_0000.

The SRAM memory area is commonly utilized for storing data and as a stack memory. It can also store program code for faster execution or during flash erase/programming operations.

### 2.4.3 Boot Configuration

The A31C12x series offers a boot mode for programming the internal flash memory. The boot mode can be entered by setting the nBOOT pin to 'L' during the system reset process (the normal state is 'H').

The boot mode supports the UART boot, which uses the UART interface to transmit and receive boot data (TXD10/RXD10).

The pins for the boot mode are listed in Table 5.

**Table 5. Boot Mode Pin List**

| Block | Pin Name | I/O | Pin Direction | Description |
|---|---|---|---|---|
| SYSTEM | nRESET | PC9 | Input | Receive the reset signal |
| | nBOOT | PB3 | Input | Set the boot mode |
| UART mode (USART10) | RXD10 | PB1 | Input | Receive the UART boot data |
| | TXD10 | PB0 | Output | Transmit the UART boot data |

### 2.4.4 Power Supply

The device operates with a supply voltage of 1.8 V to 5.5 V ($V_{DD}$). The analog peripherals are also powered through $V_{DD}$, internally connected to $AV_{DD}$ within the microcontroller.

**Table 6. Power Supply**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 1.8 | 5.5 | V |

During a power-up process, a reset plays an important role and affects the entire process of the system booting. The A31C12x series has two power-related reset options, as described below:

- POR_RST (Power-On Reset): Controls the voltage less than 1.48 V
- LVD_RST (Low-Voltage Detect Reset): Controls the voltage less than 1.70 (default)

If the power level is higher than the POR and is below the flash operating voltage, the Code Read operation may malfunction. To prevent this abnormal Code Read operation, the LVD_RST generates the SYSRESETn internal signal, and the microcontroller enters the reset mode to prevent the abnormal operation. The minimum level that the LVR can set is 1.70V, which meets the minimum flash operating voltage.

## 2.4.5 Operation Mode

### 2.4.5.1 Transition of Operation Mode

INIT mode is the initial state of the chip when a reset is asserted.

In RUN mode, the CPU operates at the maximum performance with the high-speed clock system.

SLEEP and DEEP-SLEEP modes can be used as low-power consumption modes. In the low-power consumption mode, power is effectively managed to reduce power consumption by halting the processor core and any unused peripherals.

### 2.4.5.2 RUN Mode

The CPU and peripheral hardware operate with a high-speed clock in RUN mode. After a reset, the system will enter RUN mode if the INIT state is detected.

### 2.4.5.3 SLEEP Mode

Once the microcontroller enters SLEEP mode, the CPU becomes inactive. By setting the SCU_PER and SCU_PCER registers, users can determine which peripherals will be inactive in SLEEP mode.

### 2.4.5.4 DEEP-SLEEP (STOP1, STOP2) Mode

The microcontroller enters DEEP-SLEEP mode when the core goes under the stop state using WFI instruction.

### 2.4.5.5 Reset Mode

The A31C12x series has two system reset options: a cold reset, which is effective during power-up or down sequences, and a warm reset, which is triggered by multiple reset sources.

The reset features of the A31C12x series are as follows:

- Power-On Reset (POR)
- Low-Voltage Detect Reset (LVR)
- nRESET pin reset
- Watchdog Timer (WDT) reset
- Software reset
- Clock oscillating error reset
- CPU request reset

## 2.4.6 Clocks and Start-Up

The A31C12x series has two main operating clocks: HCLK, which generates clock signals for the CPU and AHB system, and PCLK, which generates clock signals for peripheral systems.

### 2.4.6.1 HCLK Clock

The Cortex-M0+ core requires two clocks: HCLK and FCLK. While the HCLK supplies the clock for both the CPU and AHB, the FCLK remains enabled unless the system enters DEEP-SLEEP mode. Conversely, during SLEEP mode, the HCLK can be disabled while the FCLK continues to function.

The HCLK clocks the buses and memories. As the bus clock frequency is limited to a maximum of 32 MHz, the HCLK frequency must not exceed 32 MHz.

### 2.4.6.2 PCLK Clock

The PCLK can be used as a clock source for any peripheral. The SCU_PCER registers determine whether the PCLK is enabled or disabled for each peripheral. If a peripheral block's PCLK input is not enabled, its registers cannot be read. Additionally, it is important to note that the PCLK stops operating in DEEP-SLEEP mode.

### 2.4.6.3 Clock Configuration Procedure

After power on, HSI (4 MHz, 32 MHz/8) operates as a system clock by default. The HSI is enabled during the power-up sequence, and the HSE is configured by user controls with the HSI system clock.

Before enabling the HSE block, the pin mux for XIN and XOUT must be configured. During this process, avoiding affecting other bits of the PC_MR and PC_CR registers is important. After enabling the HSE block, it is necessary to wait for the crystal oscillation to be stabilized before proceeding.

The sub-oscillator, Low-Speed External (LSE, operating at 32.768 kHz) clock, can be enabled using the SCU_CSCR register (Clock Source Control Register). Like the HSE, the LSE must be enabled after configuring the pin mux for SXIN and SXOUT and allowing sufficient time for the oscillation to stabilize.

## 2.4.7 Interrupts and Events

### 2.4.7.1 NVIC (Nested Vectored-Interrupt Controller)

The A31C12x series includes up to 32 maskable interrupt sources that manage sixteen priority levels. The Nested Vector Interrupt Controller (NVIC) controls 16 interrupt lines of the Cortex-M0+.

The NVIC has the following advantages:

- Interrupt processing with reduced interrupt latency
- Direct transfer of Interrupt Vector Table (IVT) address to the core
- The fast interrupt processing capability
- Interrupts with higher priority precede those with lower priority, even if they occur after the lower priority interrupts.
- Automatic saving of processor state
- Interrupt restoring without instructional overhead at the end of the interrupt

The NVIC hardware block provides flexible and efficient interrupt management with minimal interrupt latency.

### 2.4.7.2 EXTI (Extended Interrupt)

The Extended Interrupt feature enables the system to generate event requests or wake up from STOP mode. Each external line can be configured independently to detect trigger events such as rising or falling edges or both edges and level events such as low or high.

## 2.4.8 GPIO

### 2.4.8.1 PCU Module

The A31C12x series has a Port Control Unit (PCU) module that controls the input and output (I/O) ports.

Users can configure the functionality, input/output direction, pull-up/pull-down, and debounce the pins for their applications by setting the PCU registers.

### 2.4.8.2 GPIO Module

Pins other than those specified as $V_{DD}$, GND, or for certain purposes can be used as General-Purpose Input/Output (GPIO) pins.

The GPIO module controls the general I/O pins. Output pins can be configured to output high- or low-level signals by setting the corresponding bits of the GPIO control register. On the other hand, the input status of logic input pins can be monitored through the control registers.

## 2.4.9 Embedded Flash Memory

The flash memory controller serves as an interface between the core and the embedded flash memory and is responsible for managing the data stored on the flash memory.

The flash memory of the A31C12x series has the following features:

- 32 KB or 16 KB of code flash memory with write protection bits.
- Erase units
  - Page (512 bytes)
  - Sector (2 KB)
  - Bulk (full chip)
- Program unit: Word (4 bytes)
- Zero wait (less than 25 MHz), 1- to 15-wait
- Code flash memory read protection
- Code flash memory write protection

### 2.4.10 HSICMU

The High-Speed Internal OSC Clock Management Unit (HSICMU) integrated into the A31C12x series is designed for the auto-trimming of the Internal OSC clock. The synchronization signal can also be derived from the LSE oscillator or HSE oscillator output, or it can be generated by user software.

The following are characteristics of the High Speed Internal OSC Clock Management Unit (HSICMU) built in the A31C12x series.

- Selectable synchronization source with programmable prescaler and polarity:
  - HSE (4 MHz to 12 MHz)
  - LSE (32.768 kHz)
  - External pin (PB1)
- Possibility to generate synchronization pulses by software.
- Automatic oscillator trimming capability with no need of CPU action.
- 16-bit frequency error counter with automatic error value capture and reload
- Programmable limit for automatic frequency error value evaluation and status reporting

### 2.4.11 DMAC

The direct memory access (DMA) controller is used for high-speed data transfers between peripherals and memories. DMA allows quick data transfers by copying or moving data between memory locations or between memory and peripherals without involving the core.

The DMA has the following features:

- Four channels
- 8-/16-/32-bit data transfers
- Multiple buffers with the same size.
- Peripheral interrupts trigger DMA transfers.

## 2.4.12 Timers

### 2.4.12.1 16-bit Timers

This 16-bit Timer supports four operating modes: Periodic Mode, PWM Mode, One-shot Mode, and Capture Mode.

Users can use a divided PCLK or an external clock as a clock source for the 16-bit Timer. An internal 10-bit prescaler allows to generate a variety of base clocks for the timer.

Interrupts can be triggered at regular intervals when the timer is used in Periodic Mode. Users can set the period and duty to form a PWM signal used in PWM Mode.

In One-shot Mode, the timer can generate one PWM waveform. The Capture Mode allows measuring the pulse intervals of an external input signal based on the predefined conditions. In addition, this timer can transmit signals to control other devices and is primarily used as a periodic tick timer or as a wake-up source.

### 2.4.12.2 FRT

The A31C12x series has one built-in 32-bit up count Free-Run Timer (FRT). The FRT can operate with an overflow interrupt or a match interrupt based on its register settings and can remain active even in DEEP-SLEEP (STOP1, STOP2) mode.

### 2.4.12.3 WDT

The Watchdog Timer (WDT) detects errors in the microcontroller caused by external interference or logically unexpected conditions. These errors cause the application program to deviate from its normal sequence. If the microcontroller loses control, the WDT will reset the microcontroller, allowing it to return to normal operation.

The WDT of the A31C12x series is a 32-bit down counter. If the WDT is set as a reset source, the microcontroller restarts when the down counter reaches zero.

When it is not used to monitor the microcontroller, the WDT can be used as a cycle timer along with an interrupt.

#### 2.4.12.4 SysTick Timer

Although the SysTick timer is primarily designed for real-time operating systems, it can also be utilized as a standard down-counter.

The SysTick timer has the following features:

- 24-bit down-counter
- Automatic reload
- Maskable system interrupt generation when the counter reaches zero.
- Programmable clock source

### 2.4.13 UART

The built-in UART (Universal Asynchronous Receiver/Transmitter) module allows users to specify settings for transmitting and receiving data and provides the ability to read the status of the UART. By providing information about the current state of transmission and reception processes, including types and conditions, the UART module enables users to monitor potential errors such as parity, overrun, framing, or break interrupts during data reception.

The UART module includes a programmable baud-rate generator for each channel, which generates an internal clock for its corresponding UART unit. This is achieved by dividing a prescaled clock using a baud-rate divisor ranging from 1 to 65,535, then dividing the result by 16.

Users can program interrupts that can control UART communication.

Furthermore, the built-in DMA allows the UART module to transfer data directly to or from memory without involving the CPU, reducing CPU usage, and increasing data transfer speed.

### 2.4.14 I2C Interface

The I2C (Inter-integrated Circuit) interface built in the A31C1xx series complies with the standard I2C communication protocol. It is used for serial communication between internal and external devices via the I2C protocol.

Equipped with one unit, it supports both master and slave modes and can transmit and receive data in bytes by using interrupts or polling.

The I2C interface of the A31C12x series operates in Standard mode (100 kHz) or Fast mode (400 kHz). In addition, it also supports General calls.

The I2C interface facilitates communication with multiple peripherals that share the same bus type. To utilize I2C, it is recommended to configure the SCL and SDA pins as open-drain and attach external pull-up resistors to ensure that their output signals are maintained in the 'High' state.

**Table 7. Features of I2C**

| I2C Features | I2C |
|---|---|
| 7-bit addressing mode | O |
| Standard mode (up to 100 kbit/s) | O |
| Fast mode (up to 400 kbit/s) | O |
| General call | O |

### 2.4.15 USART

Universal Synchronous and Asynchronous serial Receiver and Transmitter (USART) is a highly flexible.

serial communication device. The main features are listed below:

- Full Duplex Operation. (Independent Serial Receive and Transmit Registers)
- Asynchronous or Synchronous Operation.
- Baud Rate Generator.
- Supports Serial Frames with 5,6,7,8, or 9 Data bits and 1 or 2 Stop bits.
- Odd or Even Parity Generation and Parity Check are Supported by hardware.
- Data Over Run Detection.
- Framing Error Detection.
- Three Separate Interrupts on TX Completion, TX Data Register Empty and RX Completion.
- Double Speed Asynchronous communication mode.

Additional features are :

- 0% Error Baud Rate by floating point count register.
- Supports receive time out interrupt.
- Supports direct memory access and interrupt.

### 2.4.16 ADC

The A31C12x series features a 12-bit resolution Analog-to-Digital Converter (ADC) module. It consists of an independently controllable units and A31C12x supports up to 13 different analog inputs. This ADC module supports A/D conversion of multiple channels in different modes, including single mode, sequential mode, multiple mode, burst mode. It can sample the voltage inputs of multiple channels at critical times, which is required for various applications and can be achieved using the triggering functionality in association with timers.

Once the A/D conversion is complete, the result is left aligned in 16-bit data registers.

The ADC is mapped to the AHB and capable of high-speed operation based on the internal clock source. In addition, it uses built-in DMA to reduce microcontroller’s core load while enabling fast data sampling.

The analog input monitoring and comparison capabilities of the ADC allow the applications to determine whether the input voltage is above or below the predefined level.

### 2.4.17 CRC

The Cyclic Redundancy Check (CRC) module is used to calculate 32-bit, 16-bit IBM, 16-bit CCITT and 8-bit CCITT CRC codes from 8-bit or 32-bit data size. The user application can utilize CRC-based technologies to ensure the integrity of data transfers, storage, and flash memories in compliance with functional safety standards. With this module, users can verify the integrity of data transfers and flash memory.

Specifically, the CRC module of the A31C12x series supports DMA feature.

## 2.5 Development Support

This chapter describes the development support features of the device. The device provides standard Arm® development support, including toolchain compatibility, debug interface, trace support, and on-board debug/programming connection.

Refer to the feature list, pin description, and electrical characteristics for detailed information.

### 2.5.1 Toolchain Support

The device supports software development using standard Arm-compatible toolchains, including Arm® Keil® MDK, IAR Embedded Workbench® for Arm, and GCC-based toolchains.

Device-specific startup files, linker scripts, header files, and software examples are provided separately for each product series and software package.

## 2.5.2 Debug Interface

### 2.5.2.1 Serial Wire Debug Port (SW-DP)

The device provides an Arm® Serial Wire Debug Port (SW-DP) for software debugging and in-system flash memory programming. The SW-DP uses a two-pin debug interface, SWDIO and SWCLK, to access the CPU debug logic, memory, registers, and on-chip debug resources.

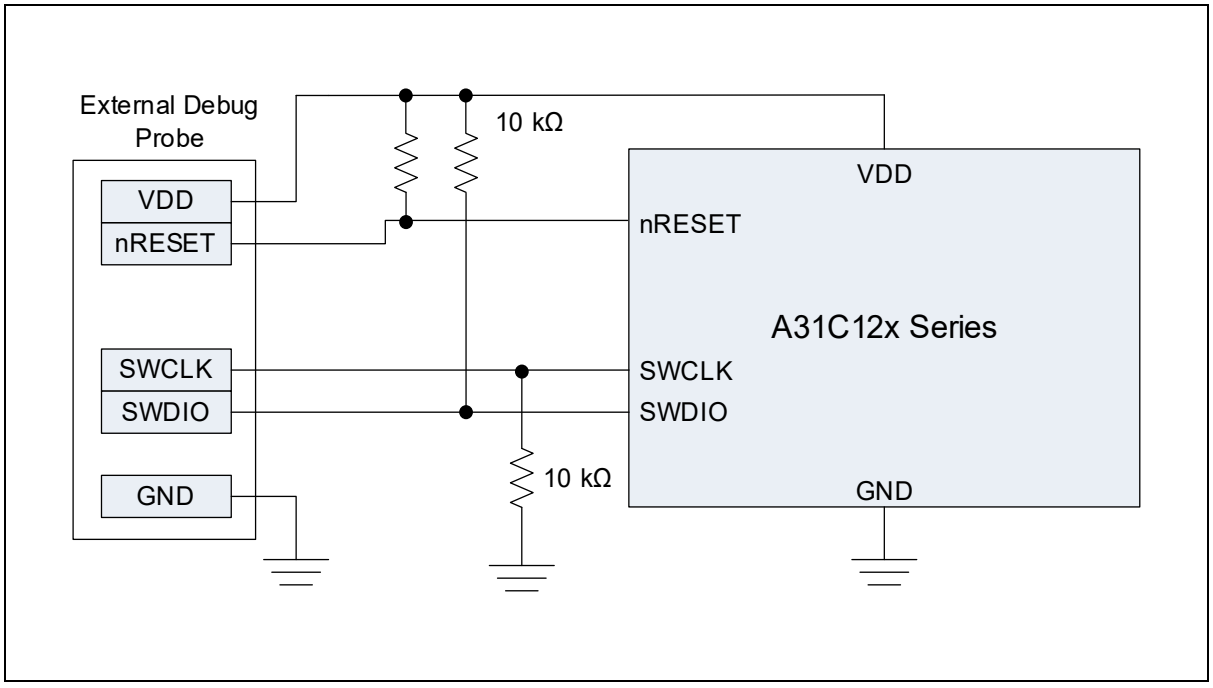
The SWD pins may be multiplexed with GPIO or other alternate functions depending on the product and package. If the SWD pins are used for application functions, the target board and firmware must be designed so that the pins remain accessible during debugging or programming.

### 2.5.2.2 SWD Connection Guide

For on-board debugging and programming, the target board should provide access to SWDIO, SWCLK, VDD, VSS, and nRESET. The nRESET connection is recommended to improve debug connection reliability and device recovery.

The VDD pin provides the target voltage reference for the external debug probe. It should be connected to the target board supply voltage unless otherwise specified by the debug probe manufacturer.

**Figure 2. SWD Interface Connection**



# 3. Pinouts and Pin Descriptions

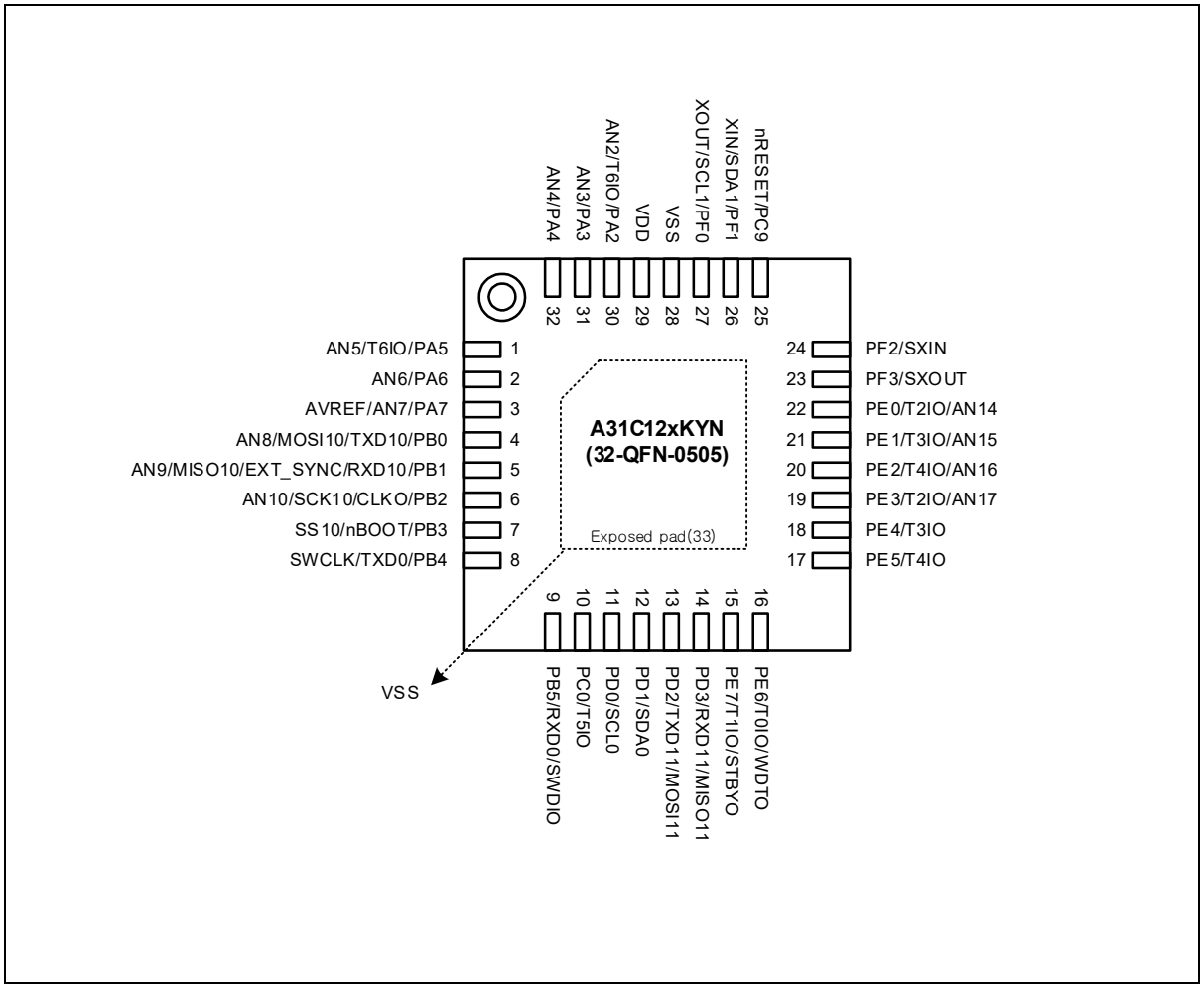
In this chapter, pinouts and pin descriptions of the A31C12x series are described.

## 3.1 Pinouts

Figure 3, Figure 4, Figure 5, Figure 6, Figure 7, and Figure 8 show the top views of the packages.

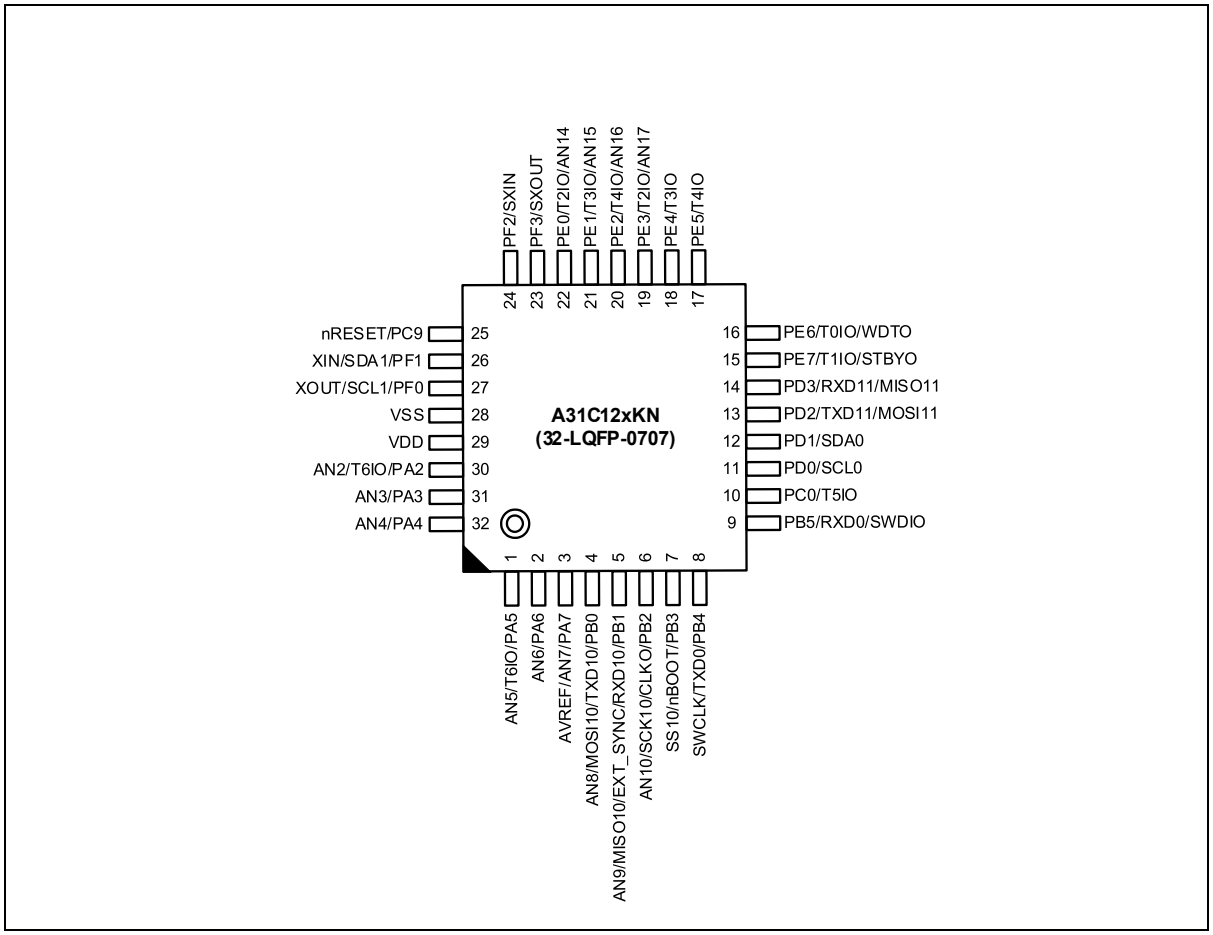
### 3.1.1 A31C12xKYN (32-QFN)

**Figure 3. A31C12xKYN (32-QFN) Pinouts**



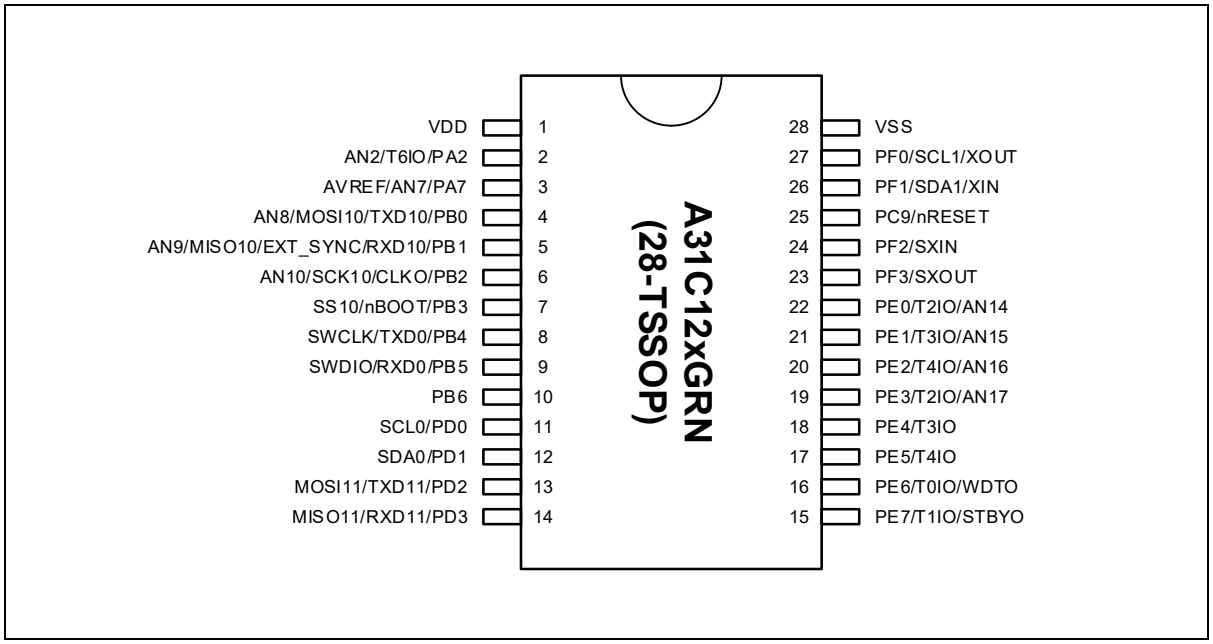
### 3.1.2 A31C12xKNN (32-LQFP)

**Figure 4. A31C12xKNN (32-LQFP) Pinouts**



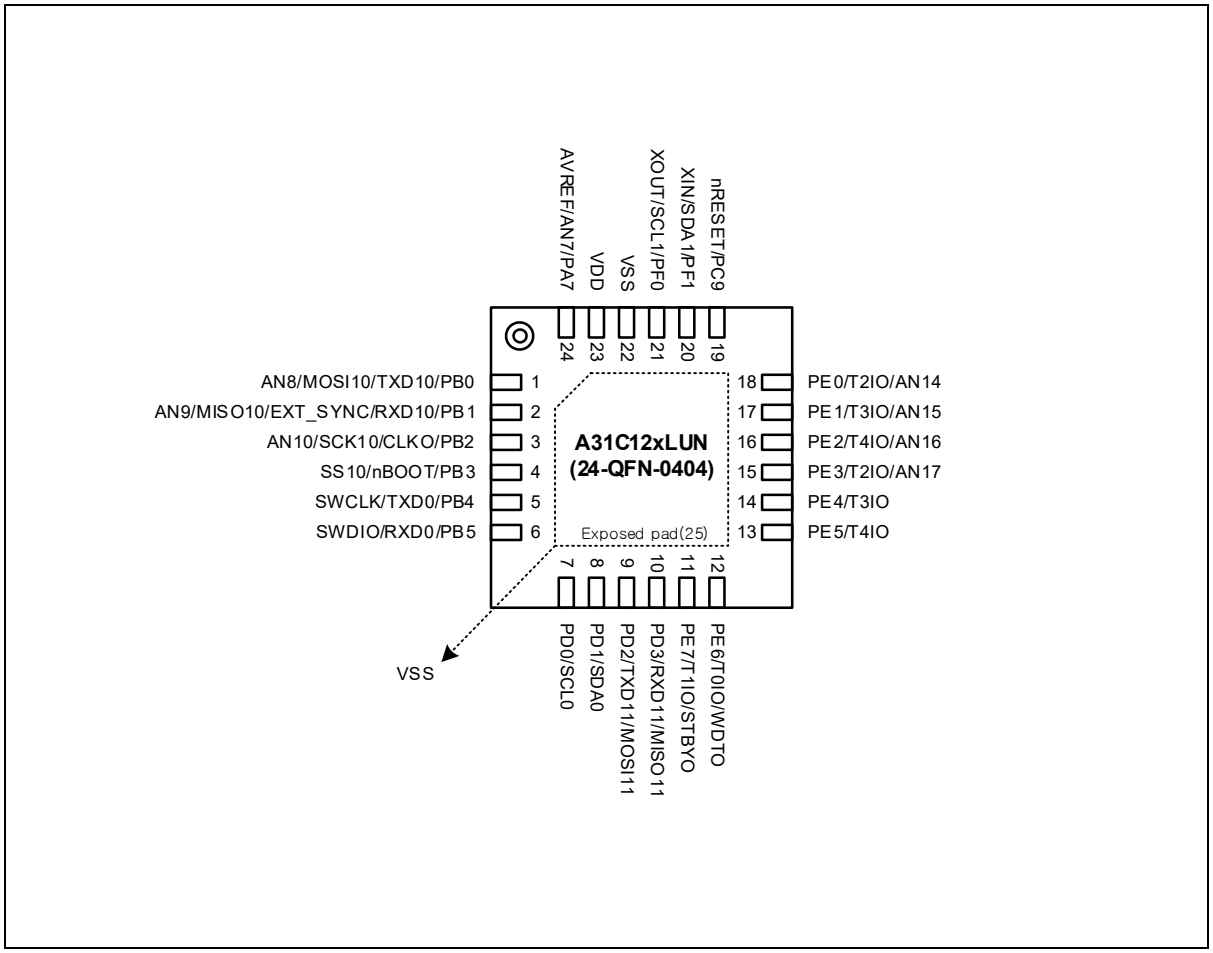
### 3.1.3 A31C12xGRN (28-TSSOP)

**Figure 5. A31C12xGRN (28-TSSOP) Pinouts**



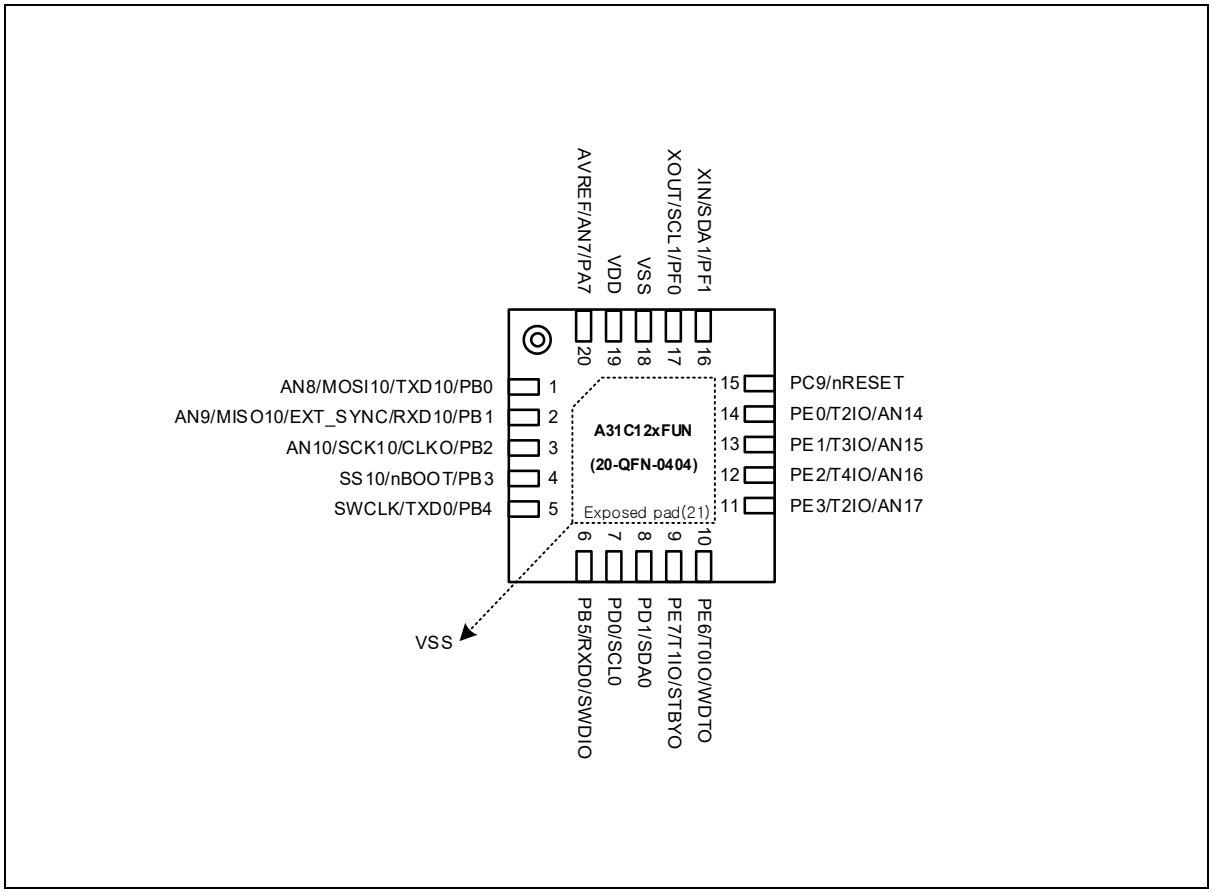
### 3.1.4 A31C12xLUN (24-QFN)

**Figure 6. A31C12xLUN (24-QFN) Pinouts**



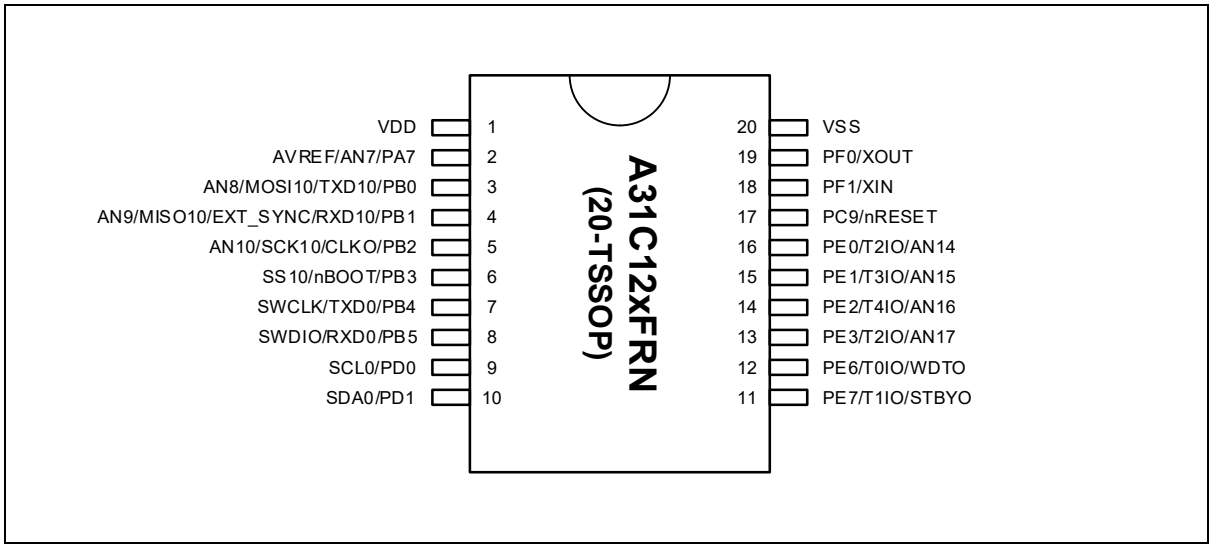
### 3.1.5 A31C12xFUN (20-QFN)

**Figure 7. A31C12xFUN (20-QFN) Pinouts**




### 3.1.6 A31C12xFRN (20-TSSOP)

**Figure 8. A31C12xFRN (20-TSSOP) Pinouts**



## 3.2 Pin Description

**Table 8. Legend and Abbreviations Used in Pin Description**

| Name | Abbreviation | Definition |
|---|---|---|
| Pin name | • The pin name remains constant.<br>• Users can assign a function to the pin using the alternate function. | |
| Pin type | I | Input |
| | O | Output |
| | I/O | Input/Output |
| | U | Pull-up |
| | D | Pull-down |
| | S | Schmitt-Trigger input |
| | C | CMOS input |
| | A | Analog |
| | P | Power |

**NOTES:**

1. After a reset, all the pins are configured to function as defined by their initial values.
2. Unused pins are set to output from Firmware. (Low output is recommended).
3. PB3 (nBOOT), PC9 (nRESET), PB5 (SWDIO) and the default pull-up pins and PB4 (SWCLK) are default pull-down pin.
4. Do not configure unused pins as floating inputs.
5. After a reset, the internal pull-up for the boot pin is enabled.
6. After a reset, the internal pull-up for the Serial Wire Data I/O (SWDIO) is enabled and the internal pull-down for the Serial Wire Clock (SWCLK) is enabled.
7. The SWCLK and SWDIO pins should not be switched to other functions while they are being used.
8. When the PF1 (XIN), PF0 (XOUT), PF3 (SXOUT), and PF2 (SXIN) pins are configured for a function other than a clock, and if the clock is enabled by software, the other functions may not operate normally.
9. When the A31C12x uses the 32-QFN, 32-LQFP or 28-TSSOP PKG, the port can be selected using the PIN_REMAP[0] bit of the PCU_PIN_REMAP register. For more information, refer to the A31C12x User's Manual.

The pin configuration information in Table 9 contains two pairs of power/ground and other dedicated pins. These multi-function pins have up to six selections of functions, including GPIO. Configuration, including pin ordering, can be changed without notice.

**Table 9. Pin Description (A31C12x)**

| Pin No | | | | | Pin Name | Type | Description | Remark |
|---|---|---|---|---|---|---|---|---|
| 32-Pin | 28-Pin | 24-Pin | 20-Pin (QFN) | 20-Pin (TSSOP) | | | | |
| 1 | - | - | - | - | PA5 | IOUS | Port A bit 5 input/output | |
| | | | | | T6IO | IO | Timer 6 input/output | |
| 2 | - | - | - | - | PA6 | IOUS | Port A bit 6 input/output | |
| 3 | 3 | 24 | 20 | 2 | PA7 | IOUS | Port A bit 7 input/output | |
| | | | | | AVREF | IA | Analog Reference Input | |
| | | | | | AN7(2) | IA | Analog input 7 | |
| 4 | 4 | 1 | 1 | 3 | PB0 | IOUS | Port B bit 0 input/output | |
| | | | | | TXD10 | O | UART(USART) CH0 data output | |
| | | | | | MOSI10 | IO | SPI(USART) CH0 Master out/Slave input | |
| | | | | | AN8(2) | IA | Analog input 8 | |
| 5 | 5 | 2 | 2 | 4 | PB1 | IOUS | Port B bit 1 input/output | |
| | | | | | RXD10 | I | UART(USART) CH0 data Input | |
| | | | | | EXT_SYNC | I | HSICMU External Sync Input | |
| | | | | | MISO10 | IO | SPI(USART) CH0 Master input/Slave output | |
| | | | | | AN9(2) | IA | Analog input 9 | |
| 6 | 6 | 3 | 3 | 5 | PB2 | IOUS | Port B bit 2 input/output | |
| | | | | | CLKO | O | System clock output | |
| | | | | | SCK10 | IO | SPI(USART) CH0 clock input/output | |
| | | | | | AN10(2) | IA | Analog input 10 | |
| 7 | 7 | 4 | 4 | 6 | PB3 | IOUS | Port B bit 3 input/output | |
| | | | | | nBOOT(2)(3)(5) | I | Boot mode selection input | Pull-up |
| | | | | | SS10 | IO | SPI(USART) CH0 slave select input | |
| 8 | 8 | 5 | 5 | 7 | PB4 | IOUS | Port B bit 4 input/output | |
| | | | | | TXD0 | O | UART CH0 TXD output | |
| | | | | | SWCLK(2)(3)(6)(7) | I | SWD clock input | Pull-down |
| 9 | 9 | 6 | 6 | 8 | PB5 | IOUS | Port B bit 5 input/output | |
| | | | | | RXD0 | I | UART CH0 RXD input | |
| | | | | | SWDIO(2)(3)(6)(7) | IO | SWD data input/output | Pull-up |
| - | 10 | - | - | - | PB6(9) | IOUS | Port B bit 6 input/output | |
| 10 | - | - | - | - | PC0(9) | IOUS | Port C bit 0 input/output | |
| | | | | | T5IO | IO | Timer 5 input/output | |
| 11 | 11 | 7 | 7 | 9 | PD0 | IOUS | Port D bit 0 input/output | |
| | | | | | SCL0 | IO | I2C CH0 SCL input/output | |

**Table 9. Pin Description (A31C12x) (continued)**

| Pin No | | | | | Pin Name | Type | Description | Remark |
|---|---|---|---|---|---|---|---|---|
| 32-Pin | 28-Pin | 24-Pin | 20-Pin (QFN) | 20-Pin (TSSOP) | | | | |
| 12 | 12 | 8 | 8 | 10 | PD1 | IOUS | Port D bit 1 input/output | |
| | | | | | SDA0 | IO | I2C CH0 SDA input/output | |
| 13 | 13 | 9 | - | - | PD2 | IOUS | Port D bit 2 input/output | |
| | | | | | TXD11 | O | UART(USART) CH1 data output | |
| | | | | | MOSI11 | IO | SPI(USART) CH1 Master out/Slave input | |
| 14 | 14 | 10 | - | - | PD3 | IOUS | Port D bit 3 input/output | |
| | | | | | RXD11 | I | UART(USART) CH1 data input | |
| | | | | | MISO11 | IO | SPI(USART) CH1 Master input/Slave output | |
| 15 | 15 | 11 | 9 | 11 | PE7 | IOUS | Port E bit 7 input/output | |
| | | | | | T1IO | IO | Timer 1 input/output | |
| | | | | | STBYO | O | Deep Sleep mode output | |
| 16 | 16 | 12 | 10 | 12 | PE6 | IOUS | Port E bit 6 input/output | |
| | | | | | T0IO | IO | Timer 0 input/output | |
| | | | | | WDTO | O | Watchdog Timer overflow output | |
| 17 | 17 | 13 | - | - | PE5 | IOUS | Port E bit 5 input/output | |
| | | | | | T4IO | IO | Timer 4 input/output | |
| 18 | 18 | 14 | - | - | PE4 | IOUS | Port E bit 4 input/output | |
| | | | | | T3IO | IO | Timer 3 input/output | |
| 19 | 19 | 15 | 11 | 13 | PE3 | IOUS | Port E bit 3 input/output | |
| | | | | | T2IO | IO | Timer 2 input/output | |
| | | | | | AN17(2) | IA | Analog input 17 | |
| 20 | 20 | 16 | 12 | 14 | PE2 | IOUS | Port E bit 2 input/output | |
| | | | | | T4IO | IO | Timer 4 input/output | |
| | | | | | AN16(2) | IA | Analog input 16 | |
| 21 | 21 | 17 | 13 | 15 | PE1 | IOUS | Port E bit 1 input/output | |
| | | | | | T3IO | IO | Timer 3 input/output | |
| | | | | | AN15(2) | IA | Analog input 15 | |
| 22 | 22 | 18 | 14 | 16 | PE0 | IOUS | Port E bit 0 input/output | |
| | | | | | T2IO | IO | Timer 2 input/output | |
| | | | | | AN14(2) | IA | Analog input 14 | |
| 23 | 23 | - | - | - | PF3 | IOUS | Port F bit 3 input/output | |
| | | | | | SXOUT(2)(8) | OA | Sub crystal oscillator output | |
| 24 | 24 | - | - | - | PF2 | IOUS | Port F bit 2 input/output | |
| | | | | | SXIN(2)(8) | IA | Sub crystal oscillator input | |
| 25 | 25 | 19 | 15 | 17 | PC9 | IOUS | Port C bit 9 input/output | |
| | | | | | nRESET(2)(3) | I | External reset input | Pull-up |
| 26 | 26 | 20 | 16 | 18 | PF1 | IOUS | Port F bit 1 input/output | |
| | | | | | SDA1 | IO | I2C CH1 SDA input/output | |
| | | | | | XIN(2)(8) | IA | External crystal oscillator input | |

**Table 9. Pin Description (A31C12x) (continued)**

| Pin No | | | | | Pin Name | Type | Description | Remark |
|---|---|---|---|---|---|---|---|---|
| 32-Pin | 28-Pin | 24-Pin | 20-Pin (QFN) | 20-Pin (TSSOP) | | | | |
| 27 | 27 | 21 | 17 | 19 | PF0 | IOUS | Port F bit 0 input/output | |
| | | | | | SCL1 | IO | I2C CH1 SCL input/output | |
| | | | | | XOUT(2)(8) | IA | External crystal oscillator output | |
| 28 | 28 | 22 | 18 | 20 | VSS | P | Ground | |
| 29 | 1 | 23 | 19 | 1 | VDD | P | VDD | |
| 30 | 2 | - | - | - | PA2 | IOUS | Port A bit 2 input/output | |
| | | | | | T6IO | IO | Timer 2 input/output | |
| | | | | | AN2(2) | IA | Analog input 2 | |
| 31 | - | - | - | - | PA3 | IOUS | Port A bit 3 input/output | |
| | | | | | AN3(2) | IA | Analog input 3 | |
| 32 | - | - | - | - | PA4 | IOUS | Port A bit 4 input/output | |
| | | | | | AN4(2) | IA | Analog input 4 | |

## 3.3 Alternate Function Pins

Table 10 describes the GPIO alternate functions.

**Table 10. GPIO Alternate Function (A31C12x) (1)**

| Pin Name | Alternate Function | | | | | |
|---|---|---|---|---|---|---|
| | AF0 | AF1 | AF2 | AF3 | AF4 | AF7 |
| PA2 | PA2 | | T6IO | | | AN2* |
| PA3 | PA3 | | | | | AN3* |
| PA4 | PA4 | | | | | AN4* |
| PA5 | PA5 | | T6IO | | | AN5* |
| PA6 | PA6 | | | | | AN6* |
| PA7 | PA7 | | | | | AN7/AVREF* |
| PB0 | PB0 | TXD10 | | | MOSI10 | AN8* |
| PB1 | PB1 | RXD10 | | EXT_SYNC | MISO10 | AN9* |
| PB2 | PB2 | | | CLKO | SCK10 | AN10* |
| PB3 | PB3 | | | nBOOT* | SS10 | |
| PB4 | PB4 | TXD0 | | SWCLK* | | |
| PB5 | PB5 | RXD0 | | SWDIO* | | |
| PB6 | PB6 | | | | | * |
| PC0 | PC0 | | T5IO | | | * |
| PC9 | PC9 | | | nRESET* | | |
| PD0 | PD0 | SCL0 | | | | * |
| PD1 | PD1 | SDA0 | | | | * |
| PD2 | PD2 | TXD11 | | | MOSI11 | * |
| PD3 | PD3 | RXD11 | | | MISO11 | * |
| PE0 | PE0 | | T2IO | | | AN14* |
| PE1 | PE1 | | T3IO | | | AN15* |
| PE2 | PE2 | | T4IO | | | AN16* |
| PE3 | PE3 | | T2IO | | | AN17* |
| PE4 | PE4 | | T3IO | | | * |
| PE5 | PE5 | | T4IO | | | * |
| PE6 | PE6 | | T0IO | WDTO | | * |
| PE7 | PE7 | | T1IO | STBYO | | * |
| PF0 | PF0 | SCL1 | | | | XOUT* |
| PF1 | PF1 | SDA1 | | | | XIN* |
| PF2 | PF2 | | | | | SXIN* |
| PF3 | PF3 | | | | | SXOUT* |

**NOTES:**

1. Unused pins are set to output from firmware (low output is recommended).

* After a reset, all the pins are configured to function defined by their initial values. The initial value of the pin depends on the package type. This configuration is in compliance with the 32-pin standard.

# 4. Electrical Characteristics

## 4.1 Parameter Conditions

Unless otherwise specified, all voltages are referenced to GND.

### 4.1.1 Minimum and Maximum Values

Unless otherwise specified, our production tests guarantee the minimum and maximum values of the device under the worst-case conditions of ambient temperature, supply voltage, and frequency.

Data based on characterization results, design simulation, and/or technical characteristics are not tested in production but are indicated in the table footnotes.

### 4.1.2 Typical Value

Unless otherwise specified, typical data are based on the conditions of $T_A$ = 25°C and $V_{DD}$ = 5.0V. The typical data are provided only as design recommendations and are not tested.

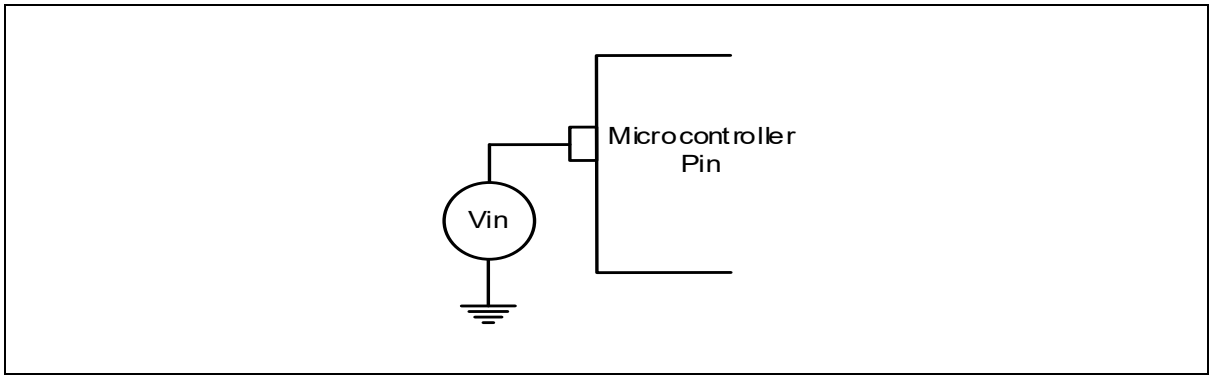
### 4.1.3 Typical Curves

Unless otherwise specified, all typical curves are provided only as design recommendations and are not tested.

### 4.1.4 Pin Input Voltage

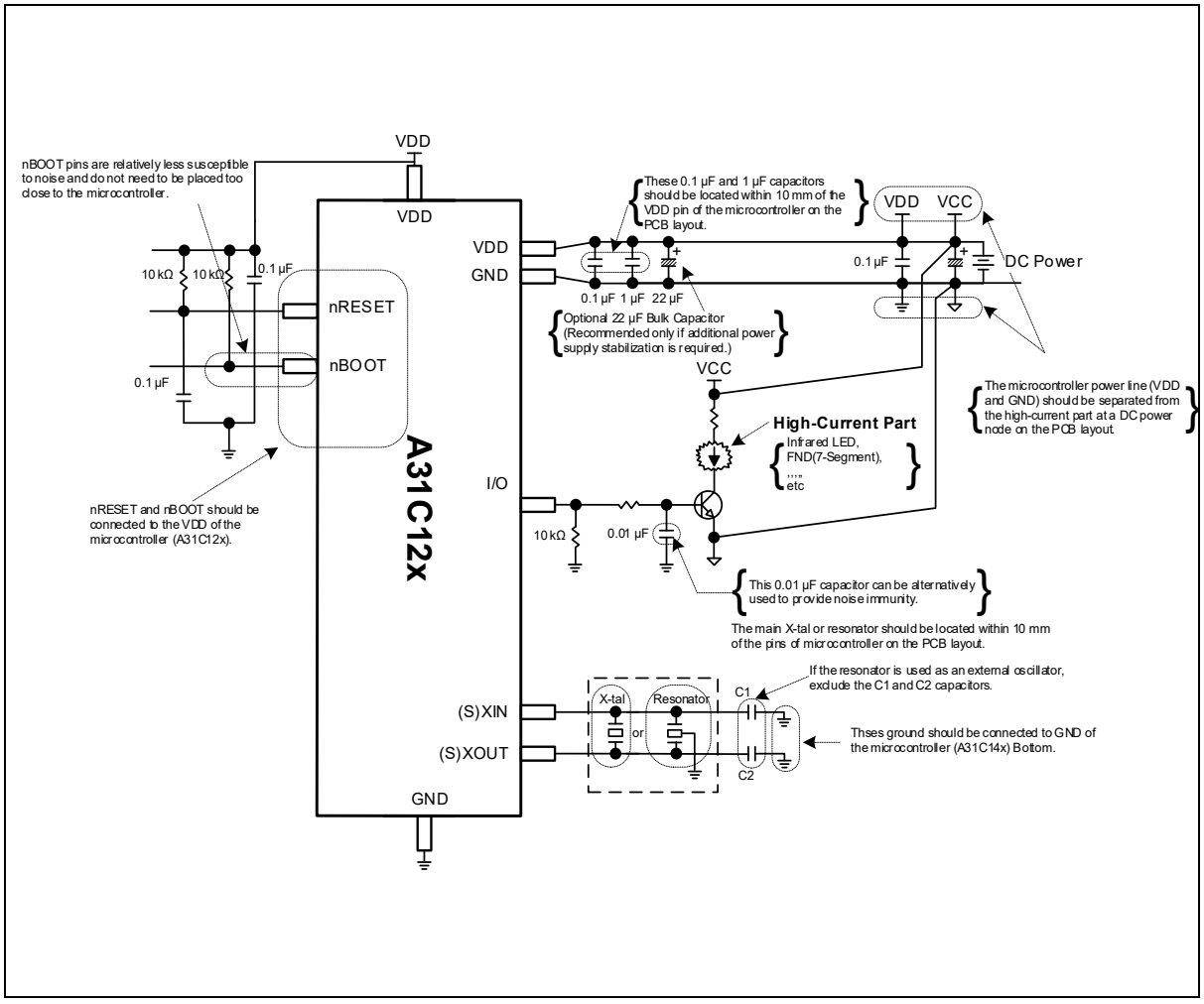
The input voltage measurement on a pin of the device is described in Figure 9.

**Figure 9. Pin Input Voltage**



### 4.1.5 Power Supply Scheme

**Figure 10. Power Supply Scheme**

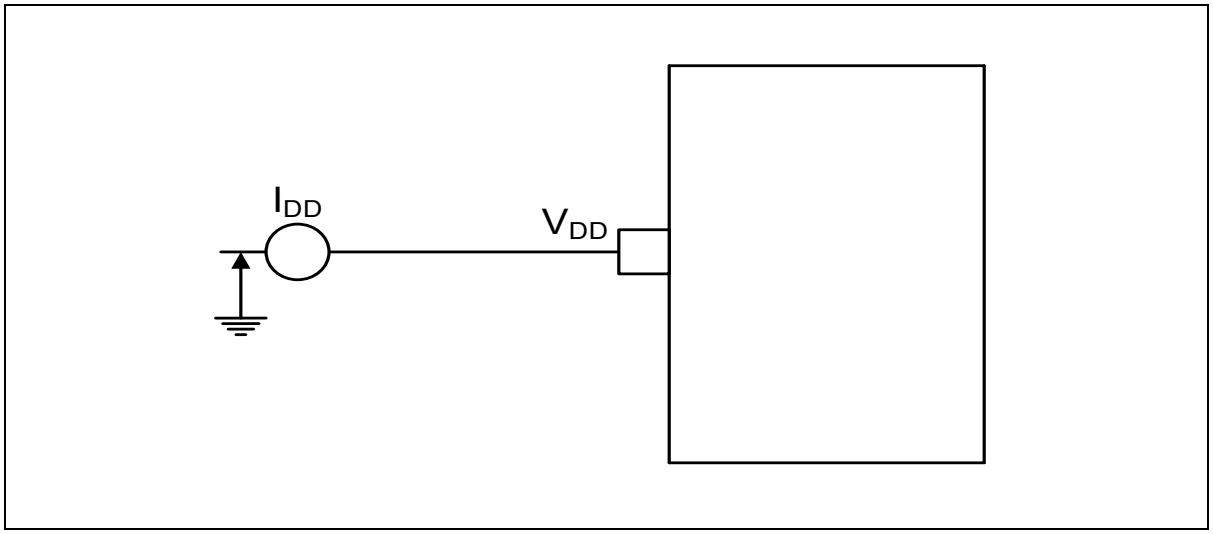



**NOTES:**

1. As shown above, each power supply pair (VDD/GND, etc.) must be decoupled with filtering ceramic capacitors. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.
2. The A31C12x requires 1 µF and 0.1 µF bypass capacitors to be mounted on the VDD line.

### 4.1.6 Current Consumption Measurement

**Figure 11. Current Consumption Measurement**




**NOTE:**

1. The IDD parameter represents the total microcontroller's current consumption, including the current supplying VDD.

## 4.2 Absolute Maximum Ratings

Exceeding stresses specified in Table 11 for voltage characteristics, Table 12 for current characteristics, or Table 13 for thermal characteristics may result in permanent damage to the device. The values in the tables are stress ratings only and do not imply that the device will function properly under these conditions. Prolonged exposure to these maximum rating conditions may impact on the device's reliability. It is important to operate the device within its specified maximum ratings to ensure reliable performance.

**Table 11. Voltage Characteristics**

| Symbol | Ratings | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$–GND(1) | External main supply voltage (including $V_{DD}$) | -0.5 | 6.0 | V |
| $V_I$(2) | Input voltage on I/O | -0.5 | Max ($V_{DD}$) + 0.5 | V |
| $V_O$ | Output voltage on I/O | -0.5 | Max ($V_{DD}$) + 0.5 | V |

**NOTES:**

1. All main power (VDD) and ground (GND) pins must always be connected to the external power supply within the permitted range.
2. VI maximum must always be respected.

**Table 12. Current Characteristics**

| Symbol | Ratings | Max. | Unit |
|---|---|---|---|
| $\sum I_{VDD}$ | Total current into the sum of all $V_{DD}$ power lines (source)(1) | -120 | mA |
| $\sum I_{GND}$ | Total current out of the sum of all GND ground lines (sink)(1) | 120 | mA |
| $I_{VDD(PIN)}$ | Maximum current into each $V_{DD}$ power pin (source)(1) | -100 | mA |
| $I_{GND(PIN)}$ | Maximum current out of each GND ground pin (sink)(1) | 100 | mA |
| $I_{IO(PIN)}$ | Output current sunk by any I/O | 15 | mA |
| | Output current sourced by any I/O and control pin | -9 | mA |
| $\sum I_{IO(PIN)}$ | Total output current sunk by the sum of all I/Os and control pins(2) | 45 | mA |
| | Total output current sourced by the sum of all I/Os and control pins(2) | -27 | mA |
| $I_{IL}$ | Input low leakage current | 1 | µA |
| $I_{IH}$ | Input high leakage current | 1 | µA |
| $P_T$ | Total power dissipation | 600 | mW |

**NOTES:**

1. All main power ($V_{DD}$) and ground (GND) pins must always be connected to the external power supplies in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.

**Table 13. Thermal Characteristics**

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | -55 to +125 | °C |
| $T_J$ | Maximum junction temperature | +105 | °C |

# 4.3 Operating Condition

## 4.3.1 General Operating Condition

**Table 14. General Operating Condition**

(Temperature: -40°C to +85°C)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | Core and Peripherals | 1.8(1) | - | 5.5 | V |
| | | ADC used | 2.4 | - | 5.5 | V |
| FREQ | Operating frequency | HSE | 4 | - | 12 | MHz |
| | | LSE | - | 32.768 | - | kHz |
| | | HSI(2) | - | 32 | - | MHz |
| | | LSI(3) | - | 32 | - | kHz |
| $V_{IN}$ | I/O input voltage | 5 V I/O | -0.3 | - | $V_{DD}$ | V |
| $T_A$ | Ambient temperature | - | -40 | - | 85 | °C |
| $T_J$ | Junction temperature range | - | -40 | 40 | 125 | °C |

**NOTES:**

1. When RESET is released, functionality is guaranteed down to VLVR5 Min.
2. Please refer to 4.3.8.1 for more detailed information.
3. Please refer to 4.3.8.2 for more detailed information.

## 4.3.2 POR (Power-On Reset) Characteristics

**Table 15. POR Electrical Characteristics**

(Temperature: -40°C to +85°C)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Operating current | - | - | 120 | - | nA |
| $V_{set}$ | POR set level | - | 1.38 | 1.48 | 1.6 | V |
| $V_{reset}$ | POR reset level | - | 0.98 | 1.28 | 1.58 | V |
| $t_R$ | $V_{DD}$ voltage rising time | - | 0.02 | - | 20 | ms/V |
| $t_F$ | $V_{DD}$ voltage falling time | - | 0.4 | - | 20 | ms/V |

## 4.3.3 Operating Condition at Power-Up/Power-Down

**Table 16. Operating Condition at Power-Up/Power-Down**

(Temperature: -40°C to +85°C)

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $T_{VDD}$ | $V_{DD}$ rise time rate | - | 0.02 | 20 | ms/V |
| | $V_{DD}$ fall time rate | - | 0.4 | 20 | ms/V |

### 4.3.4 Reset and Power Control Block Characteristics (LVR, LVI)

**Table 17. Low-Voltage Reset Characteristics**

(Temperature: -40°C to +85°C)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operating voltage | - | - | 5 | 5.5 | V |
| $V_{LVR0_F}$ | Detection level | Falling voltage | 1.5 | 1.6 | 1.7 | V |
| $V_{LVR1_F}$ | | | 2.5 | 2.7 | 2.9 | |
| $V_{LVR2_F}$ | | | 3.4 | 3.7 | 4 | |
| $V_{LVR3_F}$ | | | 3.82 | 4.22 | 4.62 | |
| $V_{LVR0_R}$ | Detection level | Rising voltage | 1.6 | 1.7 | 1.78 | V |
| $V_{LVR1_R}$ | | | 2.56 | 2.86 | 3.16 | |
| $V_{LVR2_R}$ | | | 3.52 | 3.92 | 4.32 | |
| $V_{LVR3_R}$ | | | 4.07 | 4.47 | 4.87 | |
| - | Hysteresis | - | 30 | 100 | 300 | mV |
| - | Noise cancelling time | - | - | 2 | 6 | μs |
| $I_{DD}$ | Operation current | - | - | 4 | 6 | μA |
| $I_{DD, STOP}$ | Operation current (STOP) | - | - | 3 | 100 | nA |

**Table 18. Low-Voltage Indicator Characteristics**

(Temperature: -40°C to +85°C)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operating voltage | - | - | 5 | 5.5 | V |
| $V_{LVI0_F}$ | Detection level | Falling voltage | 2 | 2.21 | 2.41 | V |
| $V_{LVI1_F}$ | | | 2.71 | 3.01 | 3.31 | |
| $V_{LVI2_F}$ | | | 3.6 | 4 | 4.4 | |
| $V_{LVI3_F}$ | | | 4.11 | 4.51 | 4.91 | |
| $V_{LVI0_R}$ | Detection level | Rising voltage | 2.14 | 2.34 | 2.54 | V |
| $V_{LVI1_R}$ | | | 2.89 | 3.19 | 3.49 | |
| $V_{LVI2_R}$ | | | 3.84 | 4.24 | 4.64 | |
| $V_{LVI3_R}$ | | | 4.38 | 4.78 | 5.18 | |
| - | Hysteresis | - | 30 | 100 | 300 | mV |
| - | Noise cancelling time | - | - | 2.2 | 6 | μs |
| $I_{DD}$ | Operation current | - | - | 3.5 | 5 | μA |
| $I_{DD, STOP}$ | Operation current (STOP) | - | - | 3 | 100 | nA |

### 4.3.5 Embedded Voltage Reference

**Table 19. Embedded Internal Voltage Reference**

(Temperature: -40°C to +85°C)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CORE}$ | Internal reference Voltage 2 | - | 1.534 | 1.59 | 1.646 | V |

## 4.3.6 Supply Current Characteristics

The amount of current consumed by the device is determined by various factors and parameters, including but not limited to the operating voltage, ambient temperature, load on I/O pins, software configuration, operating frequency, switching rate of I/O pins, location of the program in memory, and the binary code being executed.

The current consumption is measured under the conditions specified in Table 20.

### 4.3.6.1 Supply Current Consumption

**Table 20. Supply Current Characteristics**

(Temperature: -40°C to +85°C)

| Symbol | Parameter | Condition | | | | | Voltage Scaling | Typ. | Max. | unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | LSI (32 kHz) | HSI (32 MHz) | HSE (8 MHz) | LSE (32.768 kHz) | $f_{MCLK}$ | | | | |
| $I_{DD1}$ (Run) | Normal Operation(1) | STOP | RUN | STOP | STOP | $f_{HSI}$ | 5.0 V | 3 | - | mA |
| | | STOP | STOP | RUN | STOP | $f_{HSE}$ | 5.0 V | 2 | - | mA |
| | | STOP | STOP | STOP | RUN | $f_{LSE}$ | 5.0 V | 650 | - | µA |
| $I_{DD2}$ (SLEEP) | SLEEP mode(1) | STOP | RUN | STOP | STOP | $f_{HSI}$ | 5.0 V | 2.2 | - | mA |
| | | STOP | STOP | RUN | STOP | $f_{HSE}$ | 5.0 V | 1.8 | - | mA |
| | | STOP | STOP | STOP | RUN | $f_{LSE}$ | 5.0 V | 550 | - | µA |
| $I_{DD3}$ (STOP1) | DEEP-SLEEP mode(1) | VDC=STOP, WDT(LSE)=ON | | | | | 5.0 V | 5 | - | µA |
| | | VDC=STOP, WDT(LSI)=ON | | | | | 5.0 V | 4.5 | - | µA |
| $I_{DD3}$ (STOP2) | | VDC=STOP, LVD=ON | | | | | 5.0 V | 50 | - | µA |
| | | VDC=STOP, LVD=OFF | | | | | 5.0 V | 1 | - | µA |

**NOTES:**

1. All peripherals are turned off.
2. During the HSE 8 MHz test, HSEISEL was set to 0x10, HSENFEN to 0x01, and HSENFSEL to 0x01.

### 4.3.6.2 I/O System Current Consumption

In the I/O system, current consumption can be separated into two components: Static and Dynamic.

#### 4.3.6.3 I/O Static Current Consumption

When I/O pins configured as inputs with pull-up are externally held low, they generate a current consumption. This current consumption can be calculated using the values of the pull-up/pull-down resistors specified in the I/O port characteristics.

Any external pull-down or load must also be considered to estimate the current output pins consumption.

The current consumption of I/O pins configured as inputs may increase when an intermediate voltage level is applied externally. This additional consumption is caused by the input Schmitt-trigger circuits that detect the input value. Unless such a configuration is necessary for the application, this current consumption can be avoided by configuring these I/Os in analog mode. This is especially relevant for ADC and CMP input pins, which should be set up as analog inputs.

#### 4.3.6.4 I/O Dynamic Current Consumption

Besides the internal peripheral current consumption, the application's I/Os also contribute to the overall current consumption. When an I/O pin switches, it draws current from the microcontroller's supply voltage to power the I/O pin circuitry and to charge/discharge any capacitive loads (either internal or external) connected to the pin.

## 4.3.7 External Clock Source Characteristics

### 4.3.7.1 High-Speed External Clock Generated from Crystal/Ceramic Resonator

The High-Speed External (HSE) clock can be generated using a crystal/ceramic resonator oscillator with a frequency range of 4 to 12 MHz. The information provided in this paragraph is based on characterization results obtained using typical external components listed in Table 21.

Placing the resonator and load capacitors as close as possible to the oscillator pins in the application is recommended to minimize output distortion and start-up stabilization time.

For further information on the resonator characteristics, such as frequency, package, and accuracy, it is advisable to refer to the crystal resonator manufacturer.

**Table 21. HSE Oscillator Characteristics (1)**

(Temperature: -40°C to +85°C)

| Symbol | Parameter | Condition(2) | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operating voltage | - | 1.8 | 5 | 5.5 | V |
| $I_{DD(HSE)}$ | HSE current consumption | - | - | - | 3 | mA |
| $I_{STOP}$ | Power down current | - | - | - | 100 | nA |
| $f_{OSC_IN}$ | Oscillator frequency | - | 4 | - | 12 | MHz |
| $f_{OUT}$ | Output frequency | $V_{DD} \geq 1.8$ V(4) | - | - | 4 | MHz |
| | | $V_{DD} \geq 2.0$ V(5) | 4 | - | 8 | |
| | | $V_{DD} \geq 2.2$ V(6) | 4 | - | 12 | |
| $V_{IL}$ | Crystal input (low) | - | - | - | 0.2 × $V_{DD}$ | V |
| $V_{IH}$ | Crystal input (high) | - | 0.8 × $V_{DD}$ | - | - | V |
| $V_{OL}$ | Crystal out (low) | - | - | - | 0.2 × $V_{DD}$ | V |
| $V_{OH}$ | Crystal out (high) | - | 0.8 × $V_{DD}$ | - | - | V |
| $C_{L1}$, $C_{L2}$ | External load capacitor | 4 MHz ≤ $f_{OUT}$ ≤ 8 MHz | 7 | 15 | 26 | pF |
| | | 8 MHz ≤ $f_{OUT}$ ≤ 12 MHz | 7 | 15 | 22 | pF |
| $R_F$ | Feedback resistor | $V_{DD}$ = 5 V | 0.7 | 1 | 1.3 | MΩ |
| $t_{SU(HSE)}$(3) | Start-up time | $f_{OSC_IN}$ = 8 MHz | - | - | 2 | ms |

**NOTES:**

1. Guaranteed by design.
2. The resonator characteristics that the crystal/ceramic resonator manufacturer provides.
3. tSU(HSE) is the start-up time measured from the moment when it is enabled (by software) to a stabilized 8 MHz oscillation. This value is measured for a standard crystal resonator and can vary significantly with the crystal manufacturer.
4. HSEISEL = 0x3, HSENFSEL = 0x0 (0x00 is the longest noise filter)
5. HSEISEL = 0x3, HSENFSEL = 0x1
6. HSEISEL = 0x2, HSENFSEL = 0x2
7. HSEISEL = 0x1, HSENFSEL = 0x2

**Figure 12. Crystal/Ceramic Oscillator**

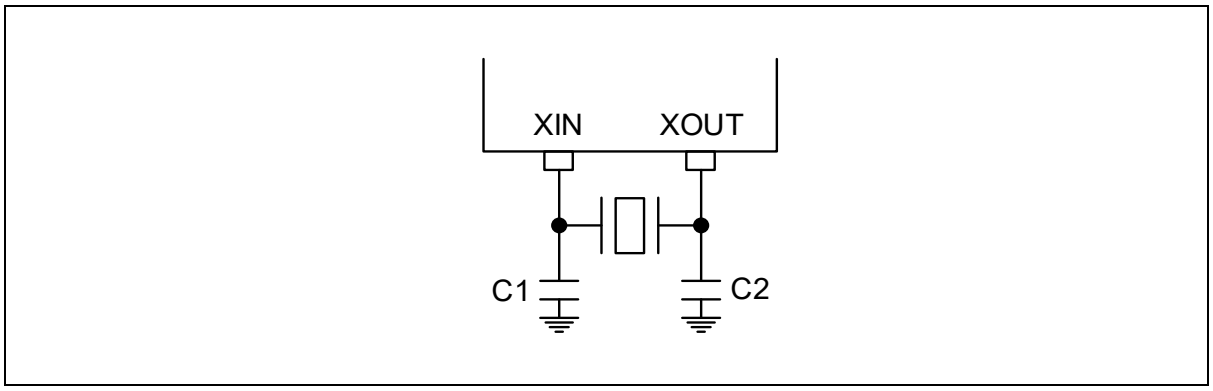



**Figure 13. External Clock**

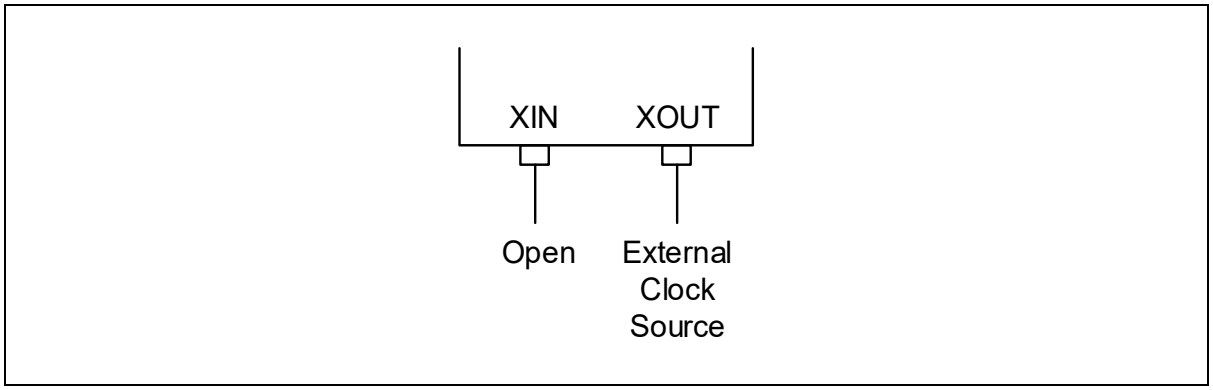
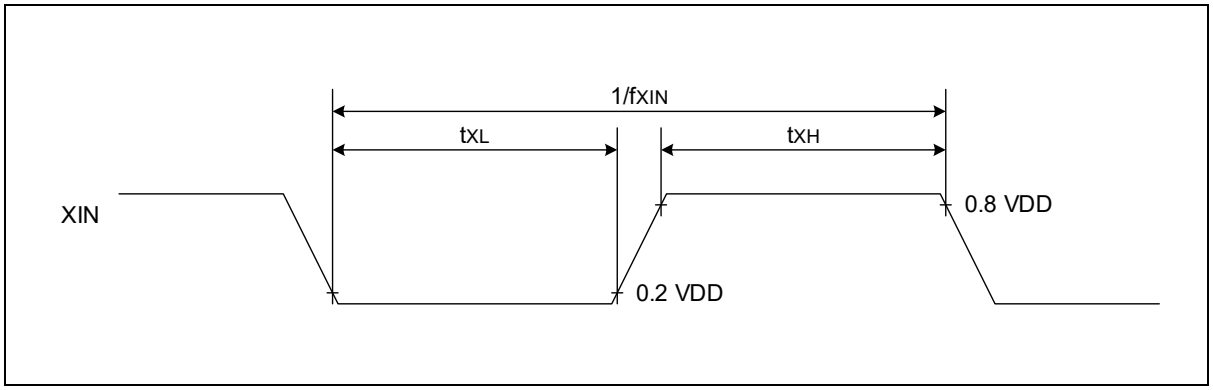



**Figure 14. Clock Timing Measurement at XIN**

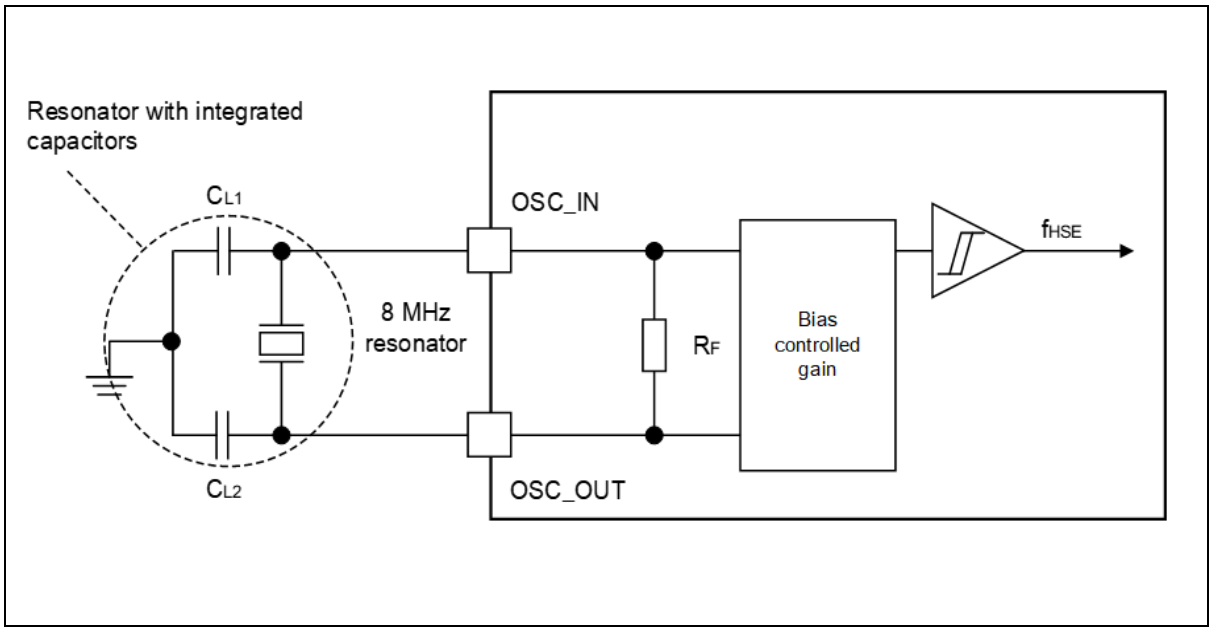


It is recommended to use high-quality external ceramic capacitors designed for high-frequency applications and selected to match the requirements of the crystal or resonator.

The $C_L1$ and $C_L2$ capacitors are usually the same size, and the crystal manufacturer specifies a load capacitance that is the series combination of both capacitors. However, the capacitance of the printed circuit board (PCB) and microcontroller's pins should also be considered, which must be included in the calculation of the overall capacitance.

Figure 15 shows a circuit diagram of a typical application with an 8 MHz crystal.

**Figure 15. Typical Application with 8 MHz Crystal**



#### 4.3.7.2 LSE Clock Generated from Crystal Resonator

The Low-Speed External (LSE) clock can be generated using a crystal/ceramic resonator oscillator with 32.768 kHz. The information provided in this paragraph is based on characterization results obtained using typical external components listed in Table 22.

Placing the resonator and load capacitors as close as possible to the oscillator pins in the application is recommended to minimize output distortion and start-up stabilization time.

For further information on the resonator characteristics, such as frequency, package, and accuracy, it is advisable to refer to the crystal resonator manufacturer.

**Table 22. LSE Oscillator Characteristics (1) (fLSE = 32.768 kHz)**

(Temperature: -40°C to +85°C)

| Symbol | Parameter | Condition(2) | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operating voltage | - | 1.8 | 5 | 5.5 | V |
| $I_{DD(LSE)}$ | LSE current consumption | - | - | 3 | 5 | μA |
| $I_{STOP}$ | Power down current | - | - | - | 100 | nA |
| $f_{OSC_IN}$ | Oscillator frequency | - | - | 32.768 | - | kHz |
| $C_{L1}$, $C_{L2}$ | External load capacitor | - | 10 | 20 | 25 | pF |
| $R_F$ | Feedback resistor | - | 5 | 10.5 | 20 | MΩ |
| $t_{SU(LSE)}$(2) | Start-up time | - | - | - | 1 | s |

**NOTES:**

1. Guaranteed by design.
2. $t_{SU(LSE)}$ is the start-up time measured from the moment when it is enabled (by software) to a stabilized 32.768 kHz oscillation. This value is measured for a standard crystal resonator and can vary significantly with the crystal manufacturer.

**Figure 16. Crystal Oscillator**

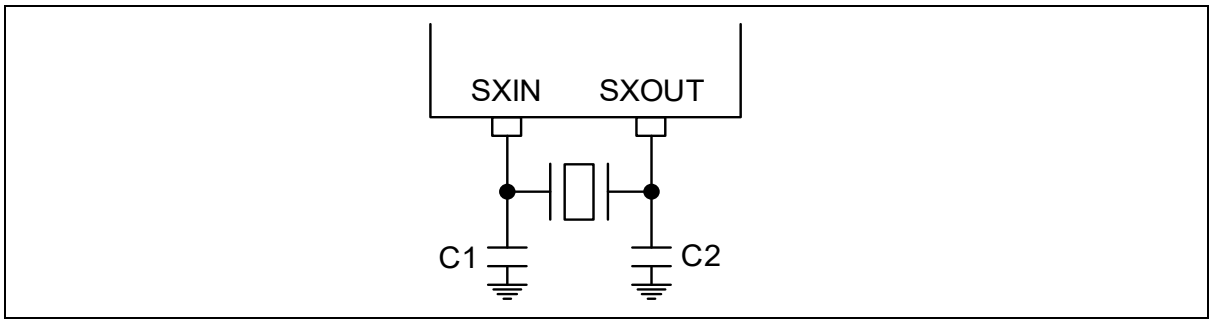



**Figure 17. Clock Timing Measurement at SXIN**

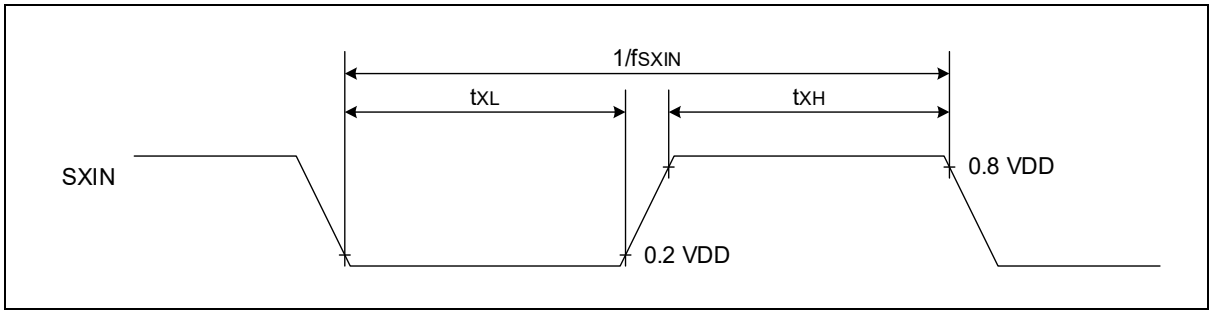
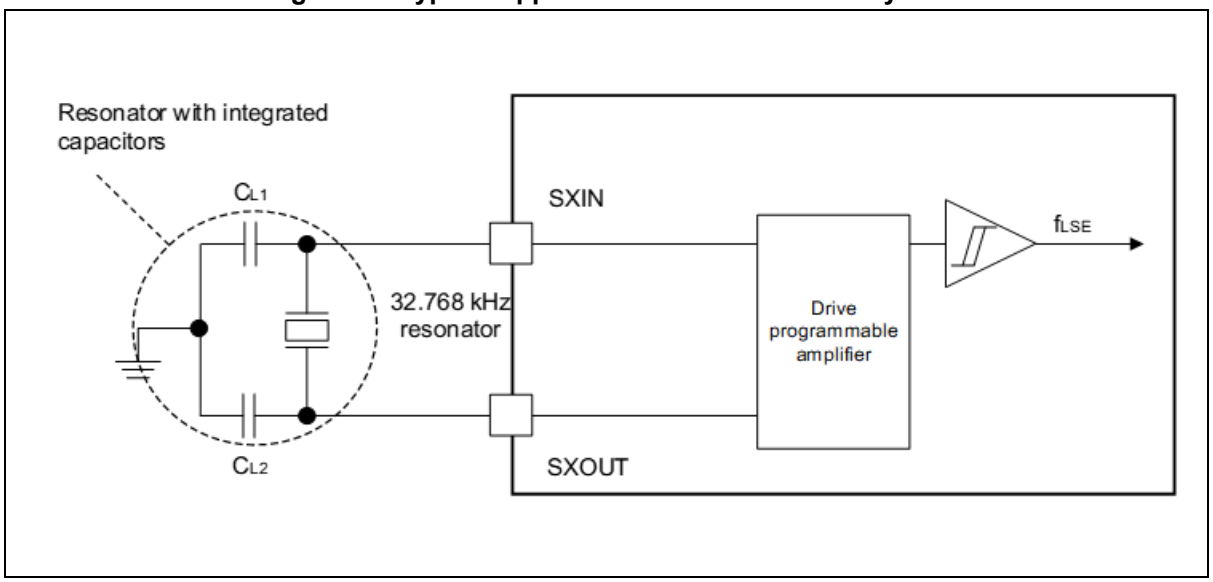



**Figure 18. Typical Application with 32.768 kHz Crystal**




**NOTE:**

1. An external resistor is not required between SXIN and SXOUT and adding one is forbidden.

## 4.3.8 Internal Clock Source Characteristics

The parameters listed in Table 23 and Table 24 are obtained through tests conducted under ambient temperature and supply voltage conditions specified in Table 14.

### 4.3.8.1 HSI32 (High-Speed Internal) RC Oscillator

**Table 23. HSI32 Oscillator Characteristics (1)**

(Temperature: -40°C to +85°C)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{HSI32}$ | HSI32 frequency | - | - | 32 | - | MHz |
| $f_E$ | Frequency error | @ 0°C to 65°C | -1.0 | - | 1.0 | % |
| | | @ −20°C to 85°C | -1.5 | - | 1.5 | % |
| | | @ −40°C to 85°C | -2.5 | - | 2.5 | % |
| DuCy (HSI32) | Duty cycle | - | - | 50 | - | % |
| $\Delta_{VDD}$ (HSI32) | HSI32 oscillator frequency drift over $V_{DD}$ | $V_{DD}$=1.8 V to 5.5 V | - | 0.2 | - | % |
| $t_{SU}$ (HSI32) | HSI32 oscillator start-up time | - | - | - | 4.5 | µs |
| $t_{STAB}$ (HSI32) | HSI32 oscillator stabilization time | - | - | - | 7.8 | µs |
| $I_{DD}$ (HSI32) | HSI32 oscillator power consumption | - | - | 400 | - | µA |

**NOTE:**

1. Guaranteed by characterization results and design.

### 4.3.8.2 LSI 32 kHz RC Oscillator

**Table 24. LSI Oscillator Characteristics (1)**

(Temperature: -40°C to +85°C)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output frequency | - | - | 32 | - | kHz |
| $f_E$ | Frequency error | @ −40°C to 85°C | -30 | - | 30 | % |
| $t_{VREG_SU}$ | 32 kHz oscillator start-up time (after LSI32K enabled) | $V_{DD}$ = 5.0 V | - | 20 | - | µs |
| $t_{STAB}$ | 32 kHz oscillator stabilization time (after LSI32K enabled) | 5 % of target frequency | - | 50 | - | µs |
| $I_{LIRC}$ | 32 kHz oscillator power consumption | The LSI oscillator is enabled. $V_{DD}$=1.8 to 5.5 V | - | 150 | 250 | nA |
| | | The LSI oscillator is disabled. $V_{DD}$=1.8 to 5.5 V | - | 2 | 40 | |

**NOTE:**

1. Guaranteed by design.

### 4.3.9 Flash Memory Characteristics

**Table 25. Flash Memory Characteristics**

(Temperature: -40°C to +85°C)

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $t_{PROG}$ | Program time | - | | - | 25 | - | µs |
| $t_{PER}$ | Page erase time | - | | - | 2 | - | ms |
| $t_{SER}$ | Sector erase time | - | | - | 2 | - | ms |
| $t_{MER}$ | Macro erase time | - | | - | 8 | - | ms |
| $N_{FWE}$ | Endurance of write/erase | • A31C122: Page 0 to 59<br>• A31C121: Page 0 to 27 | $T_A$=25°C, page unit | 10,000 | - | - | times |
| | | • A31C122: Page 60 to 63<br>• A31C121: Page 28 to 31 | | 100,000 | | | |
| $t_{FRT}$ | Retention time | - | | 10 | - | - | years |

### 4.3.10 I/O Port Characteristics

**Table 26. DC Electrical Characteristics**

(Temperature: -40°C to +85°C)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input low voltage | All GPIOs | - | - | $0.2\times V_{DD}$ | V |
| $V_{IH}$ | Input high voltage | All GPIOs | $0.8\times V_{DD}$ | - | - | V |
| $V_{OL}$ | Output low voltage | $V_{DD}$=5 V, $I_{OL}$ = 15 mA | - | - | $0.2\times V_{DD}$ | V |
| $V_{OH}$ | Output high voltage | $V_{DD}$=5 V, $I_{OH}$=–9 mA | $0.8\times V_{DD}$ | - | - | V |
| $I_{OL}$ | Output low current | $V_{DD}$=3 V, $V_{OL}$=$0.2\times V_{DD}$ | - | 10 | - | mA |
| $I_{OH}$ | Output high current | $V_{DD}$=3 V, $V_{OH}$=$0.8\times V_{DD}$ | - | -5 | - | mA |
| $I_{IL}$ | Input low leakage current | All Input ports | -1 | - | - | μA |
| $I_{IH}$ | Input high leakage current | All Input ports | - | - | 1 | μA |
| $R_{PU}$ | Pull-up resistor | $R_{MAX}$: $V_{DD}$ = 1.8 V<br>$R_{MIN}$: $V_{DD}$ = 5 V | 30 | 50 | 70 | kΩ |

#### 4.3.10.1 General Input/Output Characteristics

Unless otherwise specified, the parameters in Table 27 are obtained through tests conducted under the conditions specified in Table 14. All I/Os conform to CMOS standard.

**Table 27. I/O Static Characteristics**

(Temperature: -40°C to +85°C)

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IL}$ | I/O input low level voltage | 5 V GPIO | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | - | - | $0.2\times V_{DD}$ | V |
| $V_{IH}$ | I/O input high level voltage | 5 V GPIO | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | $0.8\times V_{DD}$ | - | - | V |
| $V_{HYS}$(2) | Input hysteresis | 5 V GPIO | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V<br>$V_{DDTYPICAL}$ = 5 V | - | 1 | - | V |
| $I_{leak}$ | Input leakage current(2) | 5 V GPIO | 1.8 ≤ $V_{IN}$ ≤ $V_{DD}$ x 1.1 | -1 | | 1 | uA |
| $R_{PU}$ | Weak pull-up equivalent resistor | $V_{IN}$ = GND | | 30 | 50 | 70 | kΩ |
| $R_{PD}$ | Weak pull-down equivalent resistor | $V_{IN}$ = $V_{DD}$ | | 30 | 50 | 70 | |
| $C_{IO}$ | I/O pin capacitance | I/O pin capacitance | | - | 5 | - | pF |

**NOTES:**

1. Data based on characterization results are not tested in production.
2. Guaranteed by design.

#### 4.3.10.2 Output Driving Current

To ensure compliance with the absolute maximum ratings specified in chapter 4.2, it is necessary to limit the number of I/O pins driving current in the user application.

- The total current sourced by all I/O pins on $V_{DD}$ and the maximum operating current of the microcontroller on $V_{DD}$ (during Run mode) must not exceed the absolute maximum rating $\Sigma I_{VDD}$ specified in Table 12.
- The total current sunk by all I/O pins on GND and the maximum operating current of the microcontroller on GND (during Run mode) must not exceed the absolute maximum rating $\Sigma I_{GND}$ specified in Table 12.

#### 4.3.10.3 Output Voltage Levels

Unless otherwise specified, the parameters in Table 28 are obtained through tests conducted under ambient temperature and supply voltage conditions specified in Table 14.

**Table 28. Output Voltage Characteristics**

(Temperature: -40°C to +85°C)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OL}$ | Output low level voltage for an I/O pin | $V_{DD}$ = 5 V, $I_{OL}$ = 15 mA | - | - | 0.2 × $V_{DD}$ | V |
| $V_{OH}$ | Output high level voltage for an I/O pin | $V_{DD}$ = 5 V, $I_{OH}$ = –9 mA | 0.8 × $V_{DD}$ | - | - | |

### 4.3.11 ADC (Analog to Digital Converter) Characteristics

**Table 29. ADC Electrical Characteristics**

(Temperature: -40°C to +85°C)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operating voltage | - | 2.4 | 5 | 5.5 | V |
| AVREF | Analog reference voltage | - | - | - | VDD | V |
| $V_{AN}$ | Analog input range | - | VSS | - | AVREF | V |
| - | Resolution | - | - | - | 12 | bit |
| $I_{DDA}$ | Operating current | VDD = 5.0 V<br>@ fMCLK = 4.57 MHz | - | 1 | 2 | mA |
| $A_{CLK}$ | Input clock frequency | | - | - | 4.57 | MHz |
| $t_{CONV}$ | Conversion time | @ VDD ≥ 2.4 V | | - | 6.56 | µs |
| | | @ VDD ≤ 2.4 V | | - | 14.99 | |
| $F_{CONV}$ | Conversion frequency | @ VDD ≥ 2.4 V | - | - | 152.38 | MHz |
| | | @ VDD ≤ 2.4 V | - | - | 66.67 | MHz |
| INL | DC accuracy | - | - | ±4 | ±8 | LSB |
| DNL | | - | - | ±1 | ±2 | |
| ZOE | Zero offset error | - | - | ±4 | ±8 | |
| FSE | Full scale error | - | - | ±6 | ±12 | |

**NOTE:**

1. Guaranteed by design.

**Table 30. Recommended ADC Resolution**

(Temperature: -40°C to +85°C)

| $V_{DD}$[V] | Resolution | Condition |
|---|---|---|
| 2.6 | 12-bit/Upper 12-bit | $A_{CLK}$ ≤ 0.5 MHz |
| 2.5 | 12-bit/Upper 12-bit | |
| 2.4 | 12-bit/Upper 12-bit | |
| 2.3 | 12-bit/Upper 12-bit | |
| 2.2 | 11-bit/Upper 11-bit | |
| 2.1 | 10-bit/Upper 10-bit | |
| 2.0 | 9-bit/Upper 9-bit | |
| 1.9 | 8-bit/Upper 8-bit | |
| 1.8 | 7-bit/Upper 7-bit | |

**NOTES:**

1. When $V_{DD}$ is lower than 2.2 V, the resolution will get worse.
2. If $V_{DD}$ is less than or equal to 2.2 V, the resolution degrades by 1-bit whenever $V_{DD}$ drops 0.1 V. ($V_{DD}$ under 2.2 V resolution has no test.)
3. Guaranteed by design.

#### 4.3.11.1 General PCB Design Guidelines

The power supply must be separated, as shown in Figure 10. The decoupling capacitors across the $V_{DD}$/$AV_{DD}$ are ceramic (good quality) capacitors and must be placed as close as possible to the chip.

## 4.3.12 Communication Interfaces Characteristics

### 4.3.12.1 I2C Interface Characteristics

The I2C interface conforms to the timing requirements specified in the I2C-bus specification, in addition to the user timing requirements listed below:

- Standard mode (Sm): up to 100 kbps bit rate
- Fast mode (Fm): up to 400 kbps bit rate

The I2C timing requirements are guaranteed by design when the I2C peripheral is configured correctly, and the I2C clock frequency is equal to or greater than the minimum value listed in the table below.

**Table 31. I2C Characteristics**

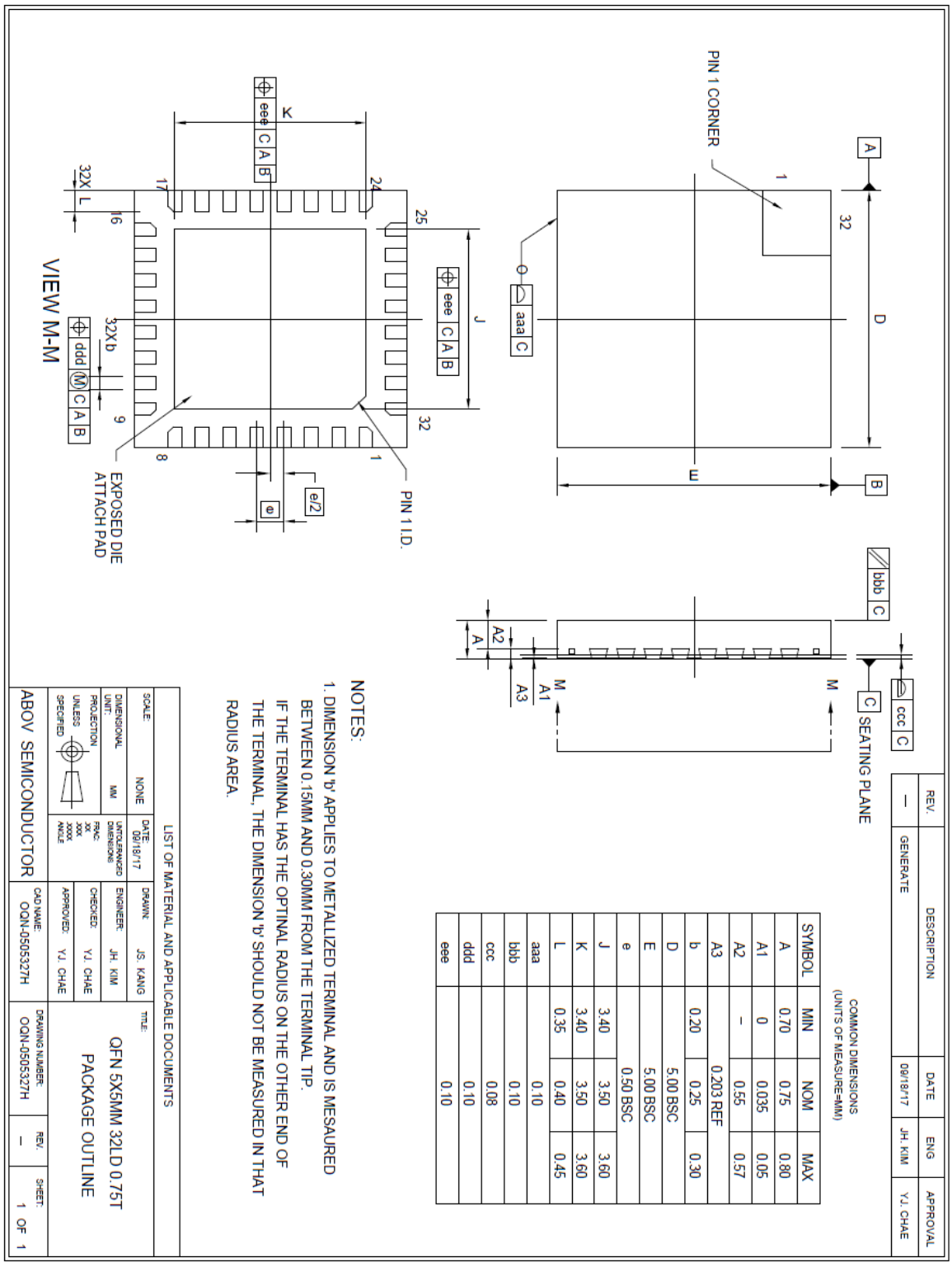
(Temperature: -40°C to +85°C)

| Symbol | Parameter | Standard | | Fast | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{SCL}$ | Clock frequency | 0 | 100 | 0 | 400 | kHz |
| $t_{SCLH}$ | Clock high pulse width | 4.0 | - | 0.6 | - | µs |
| $t_{SCLL}$ | clock low pulse width | 4.7 | - | 1.3 | - | |
| $t_{BF}$ | Bus free time | 4.7 | - | 1.3 | - | |
| $t_{STSU}$ | Start condition setup time | 4.7 | - | 0.6 | - | |
| $t_{STHD}$ | Start condition hold time | 4.0 | - | 0.6 | - | |
| $t_{SPSU}$ | Stop condition setup time | 4.0 | - | 0.6 | - | |
| $t_{SPHD}$ | Stop condition hold time | 4.0 | - | 0.6 | - | |
| $t_{VD}$ | Output valid from clock | 0 | - | 0 | - | |
| $t_{DIH}$ | Data input hold time | 0 | - | 0 | 1.0 | |
| $t_{DIS}$ | Data input setup time | 250 | - | 100 | - | ns |

# 5. Package Information

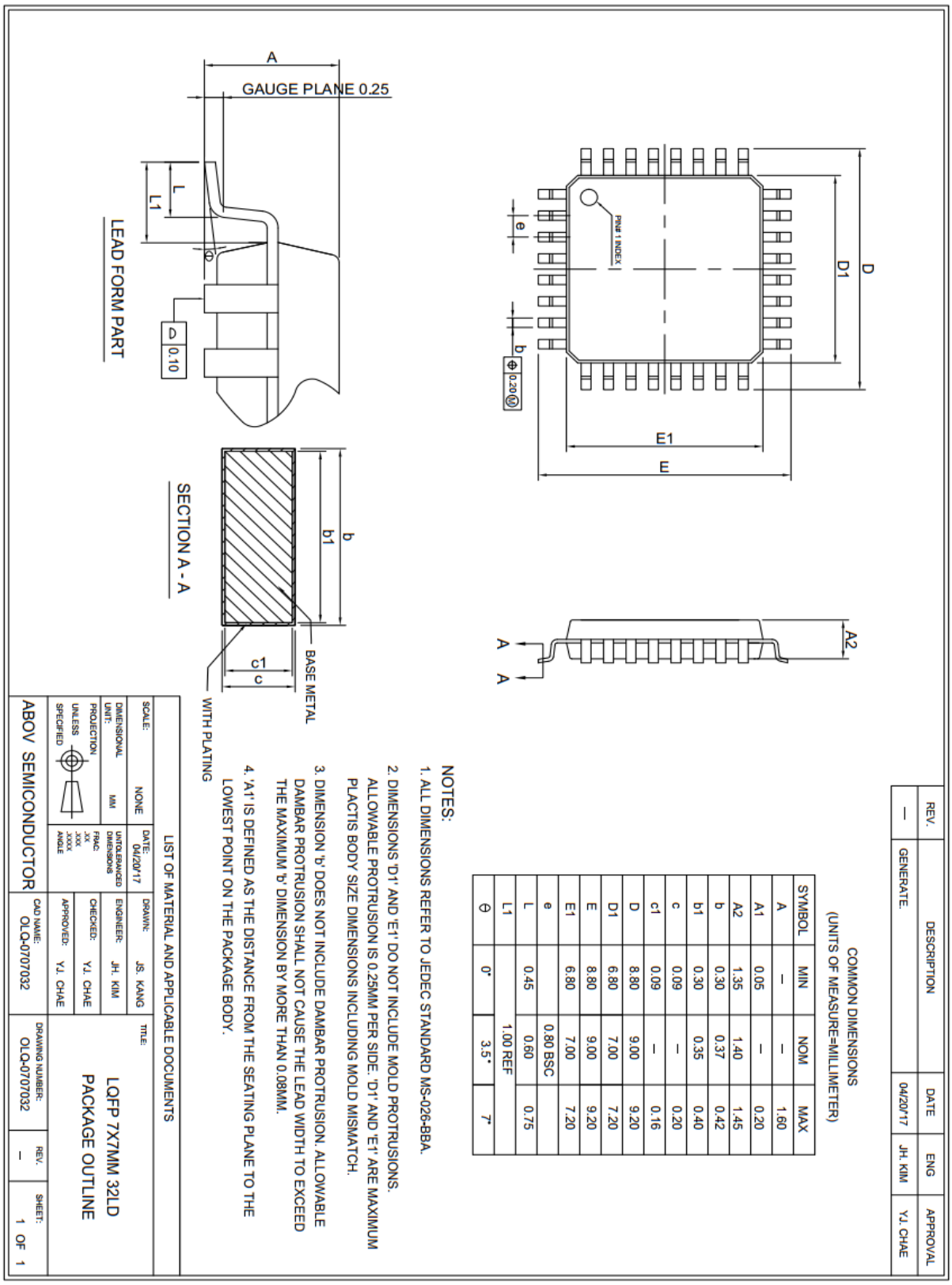
## 5.1 32-QFN Package Information

**Figure 19. Package Dimension (32-QFN)**



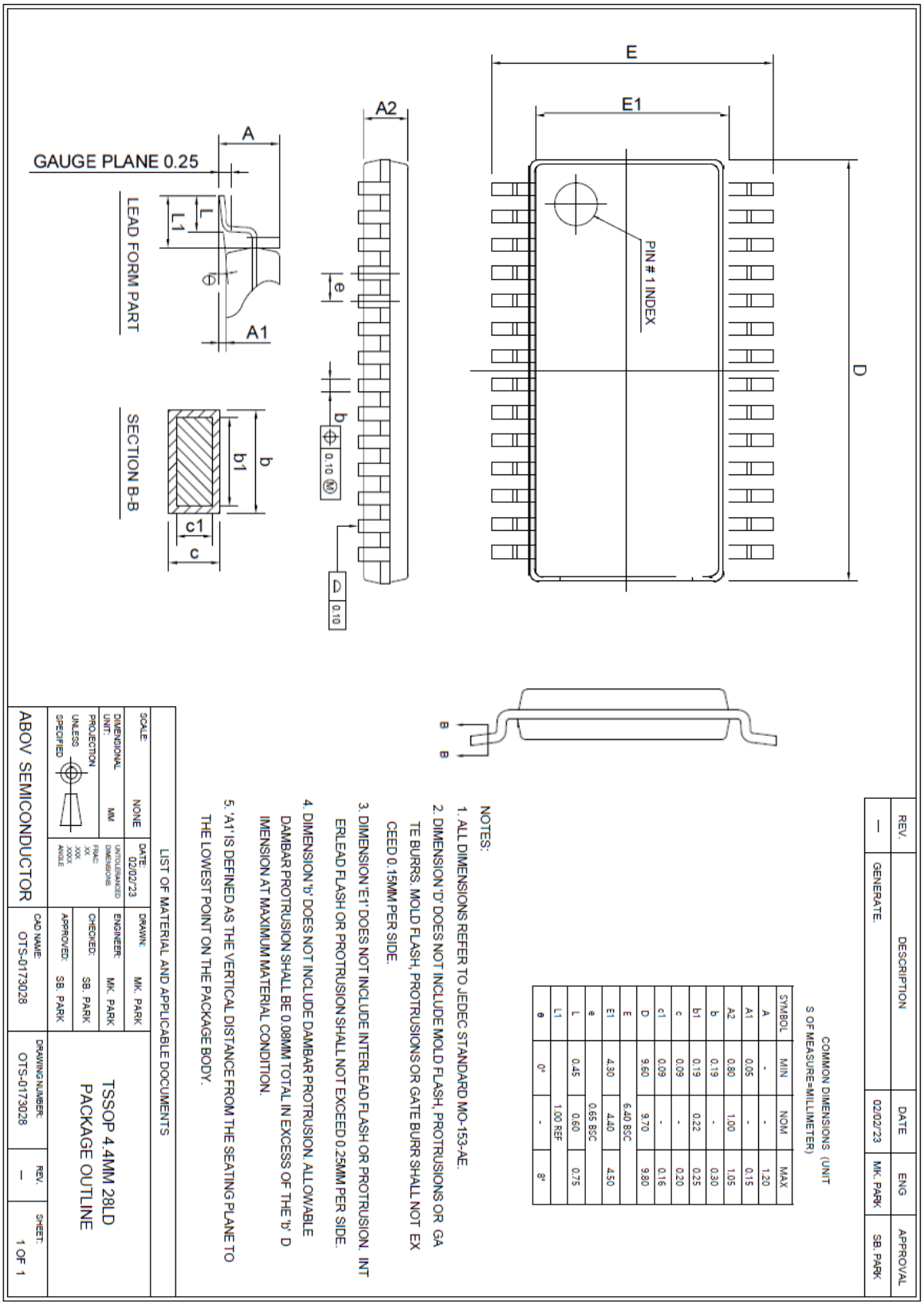
## 5.2 32-LQFP Package Information

**Figure 20. Package Dimension (32-LQFP)**



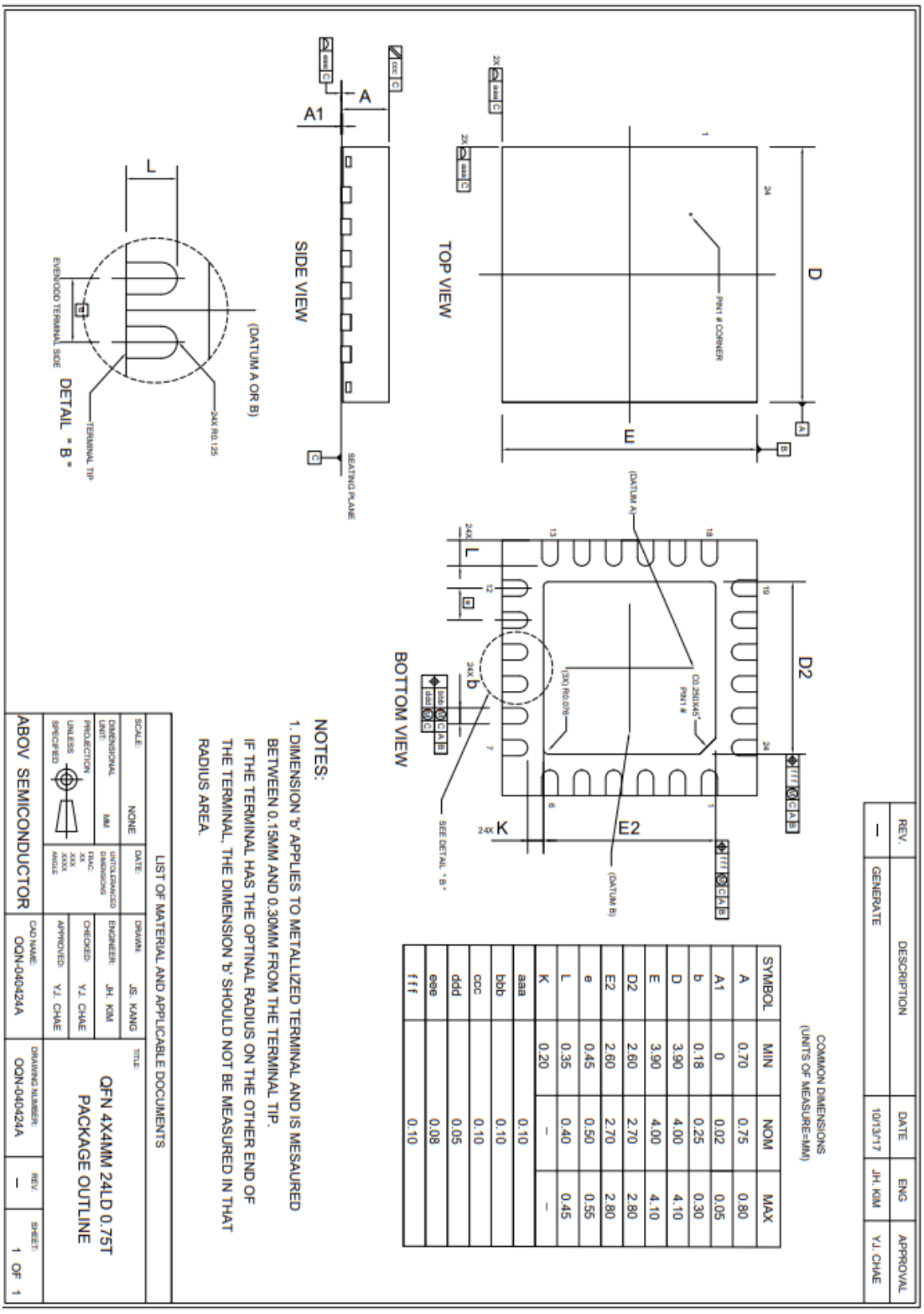
## 5.3 28-TSSOP Package Information

**Figure 21. Package Dimension (28-TSSOP)**



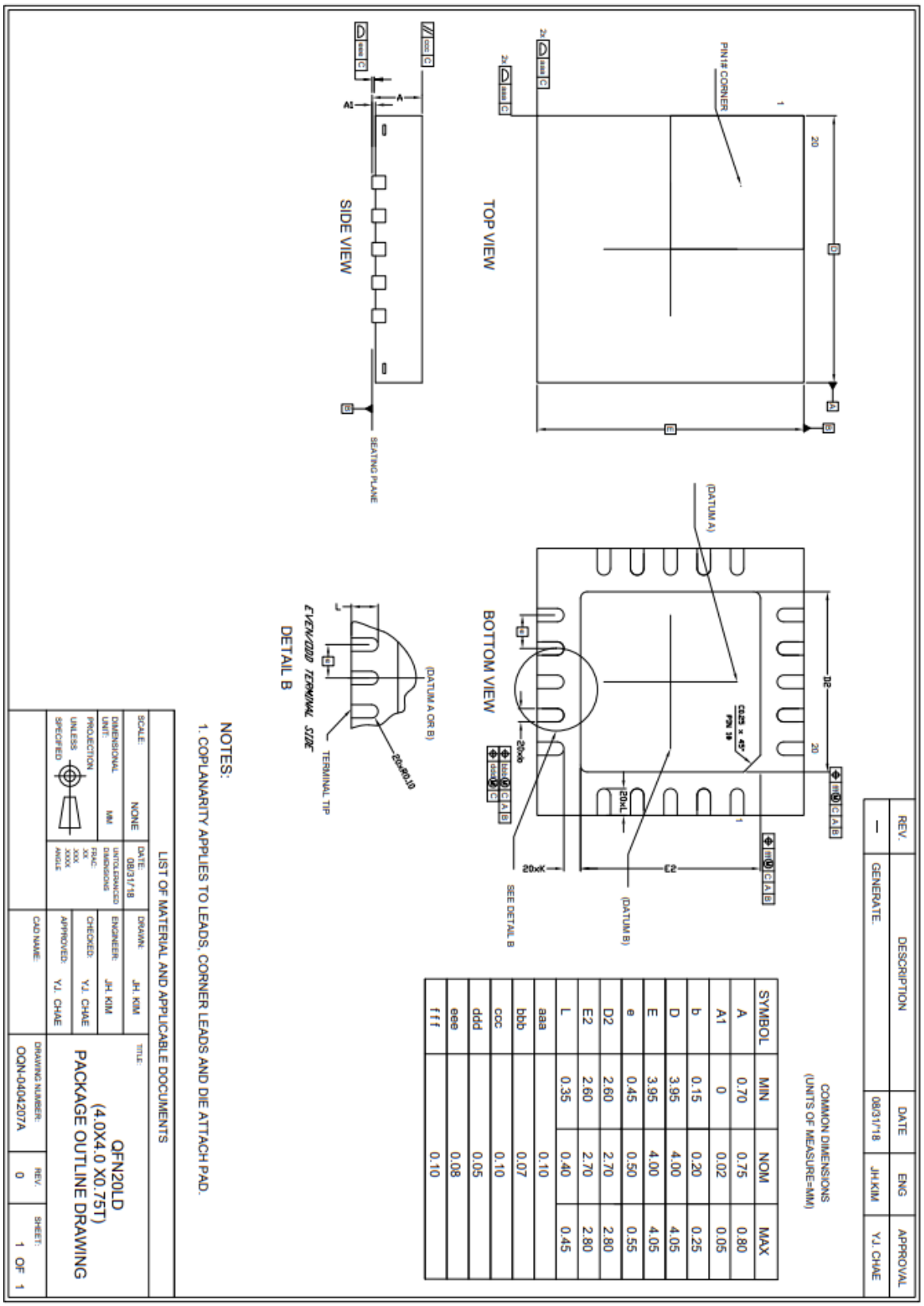
## 5.4 24-QFN Package Information

**Figure 22. Package Dimension (24-QFN)**



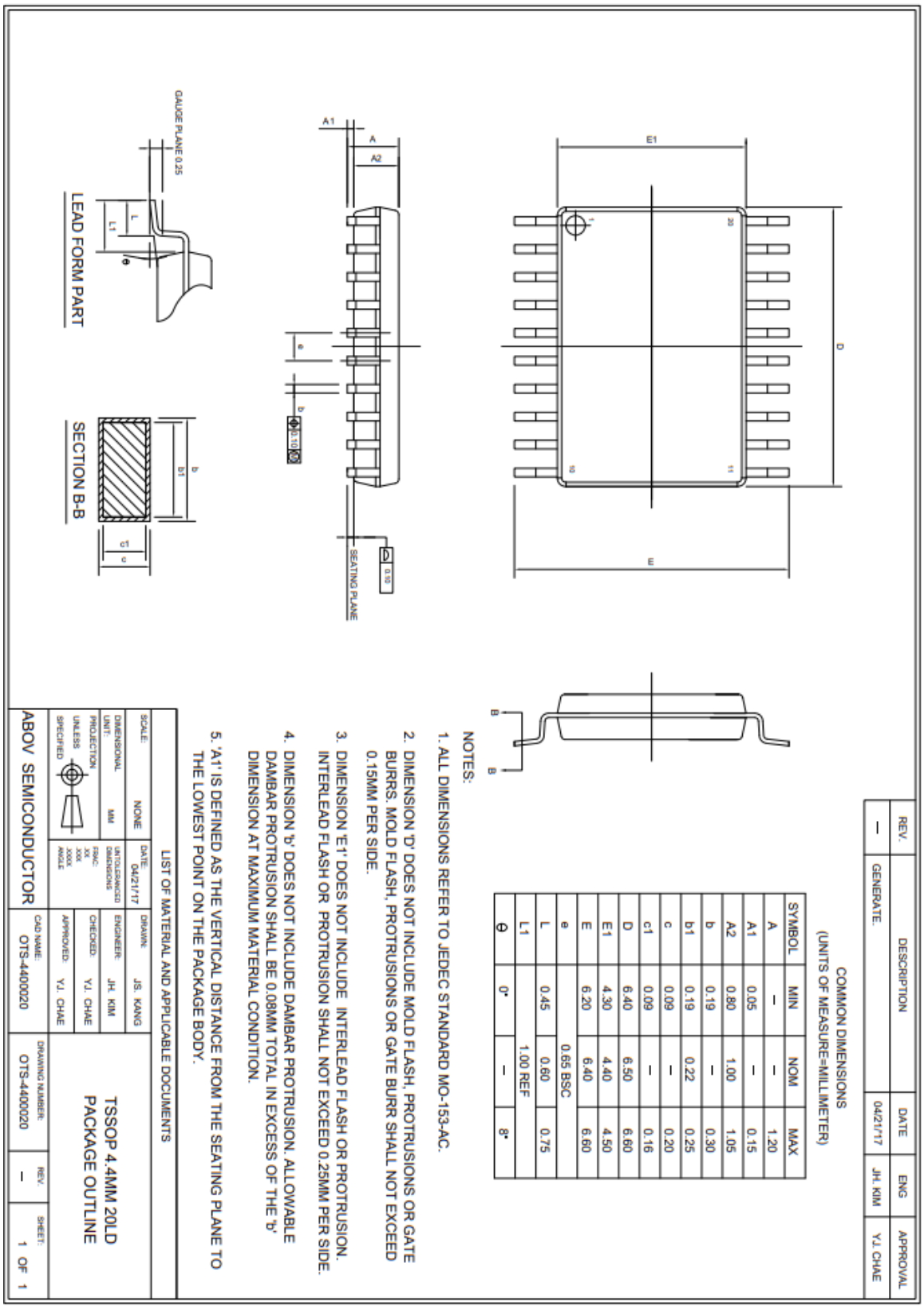
## 5.5 20-QFN Package Information

**Figure 23. Package Dimension (20-QFN)**



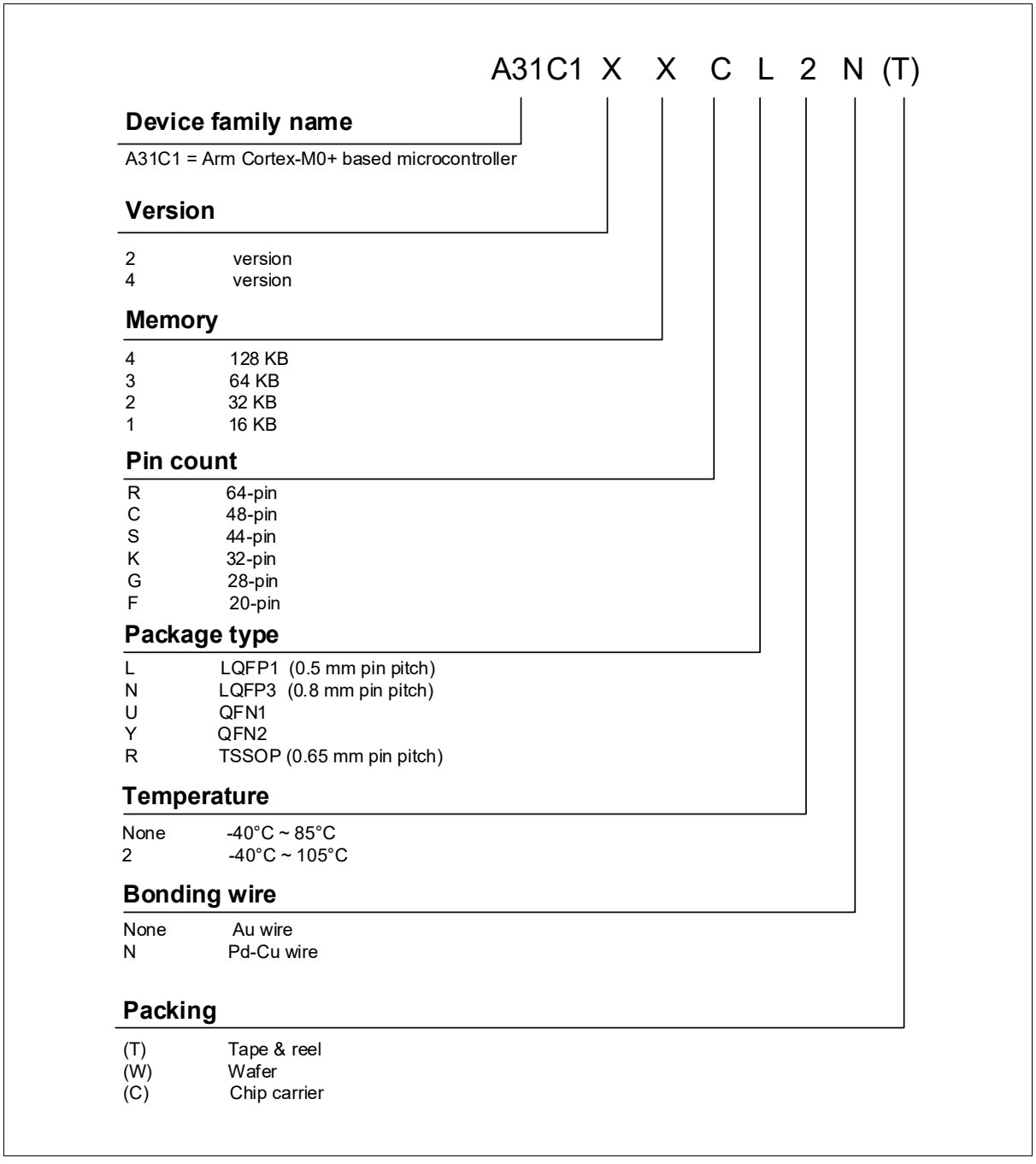
## 5.6 20-TSSOP Package Information

**Figure 24. Package Dimension (20-TSSOP)**



# 6. Ordering Information

**Figure 25. Device Numbering Nomenclature – Part Number Decoder**




**NOTE:**

1. For a list of available options (memory, package, etc.) or further information on any aspect of this device, contact the nearest ABOV sales office.

# Revision History

| Version | Date | Notes |
|---|---|---|
| 1.00 | Feb. 24, 2026 | Initial release |
| 1.01 | Apr. 2, 2026 | Updated IRC specification |
| 1.02 | Jul. 30, 2026 | • Modified Figure 10<br>• Modified Flash Endurance Cycles in Table 3 and Table 25<br>• Updated 2.5 Development Support section |

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