A31C111 Datasheet

Cortex®-M0+ 32-bit Microcontroller, 32 MHz, 16 KB Code Flash, 2 KB SRAM, 12-bit ADC

DS Rev. 1.01

Features

Core

- Arm® 32-bit Cortex® -M0+ Core
- Maximum operating frequency 32 MHz

Memories

- Up to 16 KB code flash memory
- 2 KB SRAM

Reset and Power Management

- Power-on/power-down reset (POR/LVR/LVI)
- Low-power modes: SLEEP, DEEP-SLEEP (STOP1, STOP2)

Clock Management

- High-Speed Internal Oscillator 32 MHz (HSI)
  - ±1.0% @ 0°C to +65°C
  - ±1.5% @-20°C to +85°C
  - ±2.5% @-40°C to +85°C
- Low-Speed Internal Oscillator 32 kHz (LSI)
  - ±30% @ −40°C to +85°C

GPIO

- Up to 18 I/O pins with interrupt capability
- All mappable on external interrupt vectors
- Multi-function pins capable of selection for up to six different functions, including GPIO

12-bit ADC

- One independent ADC block
- Up to 8-channel of analog inputs
- Multiple operating modes:
  - Single conversion
  - Sequence conversion
  - Burst conversion
  - Multiple conversion

Internal LDO Regulator

16-bit Timer

- Up to 4-channels
  - 4-input capture channels
  - 4-output channels
- Timer operating modes:
  - Periodic timer mode
  - One-shot mode
  - PWM mode
  - Capture mode
- 10-bit prescaler

WDT

- 32-bit down-count timer
- Reset and periodic interrupts
- Eight prescaler selections

Serial Interfaces

- UART
  - One 16450 asynchronous serial communication port
- USART
  - One synchronous serial communication port
- I2C
  - One communication port

CRC Calculation Unit

- CRC operating modes:
  - CRC32 (0x04C1_1DB7)
  - CRC16-USB (0x8005)
  - CRC16-CCITT (0x1021)
  - CRC8-CCITT (0x07)
- Support for byte reversal of input/output data

Operating Voltage

- 1.7 V to 5.5 V

Operating Temperature

- Commercial grade (−40°C to +85°C)

Packages

- 20-QFN-0404
- 20-QFN-0303
- 20-TSSOP
- 16-SOPN
- 10-SSOP

Development Support

- Serial Wire Debug (SWD) interface

Applications

- General purpose

Product Selection Table

Table 1. Device Summary

Part Number	Flash	SRAM	USART	UART	I2C	ADC	TIMER	I/O Port	Package
A31C111FUN	16 KB	2 KB	1	1	1	8	4	18	20-QFN-0404
A31C111FYN *	16 KB	2 KB	1	1	1	8	4	18	20-QFN-0303
A31C111FRN *	16 KB	2 KB	1	1	1	8	4	18	20-TSSOP
A31C111AEN *	16 KB	2 KB	1	1	1	8	4	14	16-SOPN
A31C111TSN *	16 KB	2 KB	1**	1	1	4	2	8	10-SSOP

* For available options or further information on devices with a "*" mark, please contact the ABOV sales office.

** SPI is not supported on the 10-pin SSOP package because the USART SCK pin is not available.

Contents

Features 1
Product Selection Table 2
1. Introduction 7
2. Descriptions 8
2.1 Product Category Definition 8
2.2 Device Overview 9
2.3 Block Diagram 16
2.4 Functional Overview 17
2.4.1 Cortex-M0+ Core 17
2.4.2 Embedded SRAM 17
2.4.3 Boot Configuration 17
2.4.4 Power Supply 18
2.4.5 Operation Mode 19
2.4.5.1 Transition of Operation Mode 19
2.4.5.2 RUN Mode 19
2.4.5.3 SLEEP Mode 19
2.4.5.4 DEEP-SLEEP (STOP1, STOP2) Mode 19
2.4.5.5 Reset Mode 19
2.4.6 Clocks and Start-Up 20
2.4.6.1 HCLK Clock 20
2.4.6.2 PCLK Clock 20
2.4.6.3 Clock Configuration Procedure 20
2.4.7 Interrupts and Events 21
2.4.7.1 NVIC (Nested Vectored-Interrupt Controller) 21
2.4.7.2 EXTI (Extended Interrupt) 21
2.4.8 GPIO 22
2.4.8.1 PCU Module 22
2.4.8.2 GPIO Module 22
2.4.9 Embedded Flash Memory 22
2.4.10 Timers 23
2.4.10.1 16-bit Timers 23
2.4.10.2 WDT 23
2.4.10.3 SysTick Timer 23
2.4.11 UART 24
2.4.12 I2C 24
2.4.13 USART 25
2.4.14 ADC 25
2.4.15 CRC 26
2.5 Development Support 27
2.5.1 Toolchain Support 27
2.5.2 Debug Interface 28
2.5.2.1 Serial Wire Debug Port (SW-DP) 28
2.5.2.2 SWD Connection Guide 28
3. Pinouts and Pin Descriptions 29
3.1 Pinouts 29
3.1.1 A31C111FU (20-QFN-0404) 29
3.1.2 A31C111FY (20-QFN-0303) 30

3.1.3 A31C111FR (20-TSSOP) 31
3.1.4 A31C111AE (16-SOPN) 31
3.1.5 A31C111TS (10-SSOP) 32
3.2 Pin Description 33
3.3 Alternate Function Pins 36
4. Electrical Characteristics 37
4.1 Parameter Conditions 37
4.1.1 Minimum and Maximum Values 37
4.1.2 Typical Value 37
4.1.3 Typical Curves 37
4.1.4 Pin Input Voltage 37
4.1.5 Power Supply Scheme 38
4.1.6 Current Consumption Measurement 39
4.2 Absolute Maximum Ratings 40
4.3 Operating Condition 41
4.3.1 General Operating Condition 41
4.3.2 Power-On Reset (POR) Characteristics 41
4.3.3 Operating Condition at Power-Up/Power-Down 41
4.3.4 Reset and Power Control Block Characteristics (LVR, LVI) 42
4.3.5 Embedded Voltage Reference 43
4.3.6 Supply Current Characteristics 44
4.3.6.1 Supply Current Consumption 44
4.3.6.2 I/O System Current Consumption 44
4.3.6.3 I/O Static Current Consumption 44
4.3.6.4 I/O Dynamic Current Consumption 45
4.3.7 Internal Clock Source Characteristics 46
4.3.7.1 High-Speed Internal RC Oscillator (HSI32) 46
4.3.7.2 Low-Speed Internal 32 kHz RC Oscillator (LSI) 46
4.3.8 Flash Memory Characteristics 47
4.3.9 I/O Port Characteristics 48
4.3.9.1 General Input/Output Characteristics 49
4.3.9.2 Output Driving Current 49
4.3.9.3 Output Voltage Levels 50
4.3.10 ADC Characteristics 51
4.3.10.1 General PCB Design Guidelines 51
4.3.11 Communication Interfaces Characteristics 52
4.3.11.1 I2C Interface Characteristics 52
5. Package Information 53
5.1 20-QFN-0404 Package Information 53
5.2 20-QFN-0303 Package Information 54
5.3 20-TSSOP Package Information 55
5.4 16-SOPN Package Information 56
5.5 10-SSOP Package Information 57
6. Ordering Information 58
Revision History 59

List of Tables

Table 1. Device Summary 2
Table 2. A31C111 Series Memory Capacity 8
Table 3. A31C111 Series Features 9
Table 4. Summary of A31C111 Peripherals 15
Table 5. Boot Mode Pin List 17
Table 6. Power Supply 18
Table 7. Features of I2C 24
Table 8. Legend and Abbreviations Used in Pin Description 33
Table 9. Pin Description 34
Table 10. GPIO Alternate Function (1) 36
Table 11. Voltage Characteristics 40
Table 12. Current Characteristics 40
Table 13. Thermal Characteristics 40
Table 14. General Operating Condition 41
Table 15. POR Electrical Characteristics 41
Table 16. Operating Condition at Power-Up/Power-Down 41
Table 17. Low-Voltage Reset Characteristics 42
Table 18. Low-Voltage Indicator Characteristics 42
Table 19. Embedded Internal Voltage Reference 43
Table 20. Supply Current Characteristics 44
Table 21. HSI32 Oscillator Characteristics (1) 46
Table 22. LSI Oscillator Characteristics (1) 46
Table 23. Flash Memory Characteristics 47
Table 24. DC Electrical Characteristics 48
Table 25. I/O Static Characteristics 49
Table 26. Output Voltage Characteristics 50
Table 27. ADC Electrical Characteristics 51
Table 28. Recommended ADC Resolution 51
Table 29. I2C Characteristics 52

List of Figures

Figure 1. A31C111 Series Block Diagram 16
Figure 2. SWD Interface Connection 28
Figure 3. A31C111FU (20-QFN-0404) Pinouts 29
Figure 4. A31C111FY (20-QFN-0303) Pinouts 30
Figure 5. A31C111FR (20-TSSOP) Pinouts 31
Figure 6. A31C111AE (16-SOPN) Pinouts 31
Figure 7. A31C111TS (10-SSOP) Pinouts 32
Figure 8. Pin Input Voltage 37
Figure 9. Power Supply Scheme 38
Figure 10. Current Consumption Measurement 39
Figure 11. Package Dimension (20-QFN-0404) 53
Figure 12. Package Dimension (20-QFN-0303) 54
Figure 13. Package Dimension (20-TSSOP) 55
Figure 14. Package Dimension (16-SOPN) 56
Figure 15. Package Dimension (10-SSOP) 57
Figure 16. A31C111 Series Device Ordering Information 58

1. Introduction

This document provides an overview of the features supported by the device, including high-level information and brief explanations for each feature.

Refer to Table 3 for the list of features supported by the device.

2. Descriptions

The A31C111 series is a high-performance and energy-efficient 32-bit microcontroller based on Arm Cortex-M0+ core, with up to 16 KB of flash memory and 2 KB of SRAM.

2.1 Product Category Definition

Table 2 provides an overview of the memory capacity for available devices in the A31C111 series.

This document provides an overview of the features supported by each device, including high-level information and brief explanations for each feature.

Refer to Table 3 for the list of features supported by product category.

Table 2. A31C111 Series Memory Capacity

Device	Memory Capacity	
	Flash	RAM
A31C111	16 KB	2 KB

2.2 Device Overview

Table 3 summarizes and lists the features specific to the device in the A31C111 series while considering the largest package.

Table 3. A31C111 Series Features

Peripheral		Description
Core	CPU	• Max. operating frequency: 32 MHz • 32-bit Arm Cortex-M0+ Core • Register settings in CPU: - Uses general-purpose registers specified by the 32-bit Thumb instruction set: R0-R12 - Main Stack Pointer (MSP) and Process Stack Pointer (PSP): R13 - Link Register (LR): R14 - Program Counter (PC): R15 • Data alignment in little-endian • Von Neumann Architecture • AHB/APB
	Interrupt	• NVIC (Nested-Vectored Interrupt Controller) • Up to 32 peripheral interrupts available. • 2-bit width of group priority: four levels of priority
Memory	Code Flash	• Capacity: 16 KB • Erase unit: Page (512 bytes), sector (2 KB) or bulk (full chip) • Program unit: Word (4 bytes) • Read-Protection • Self-programming • CRC code generation and verification for the flash memory • Endurance - Page 0 to 27 (14 KB) 10,000 cycles - Page 28 to 31 (2 KB) 100,000 cycles • Lifetime: 10 years
	Boot ROM	• Initiating the microcontroller's boot mode by receiving an external input signal at the nBOOT pin • UART mode of USART10 • In-system programming - Users can store information in the internal flash memory by using an application board to write data to the memory.

Table 3. A31C111 Series Features (continued)

Peripheral		Description
Memory	SRAM	• Capacity: 2 KB • Capable of functioning as a program's working area • High-speed execution for time-critical codes • Capability to remap into an interrupt vector area
SCU (System Control Unit)	Operating frequency	Up to 32 MHz
	Clock	• High-Speed Internal Oscillator (HSI): 32 MHz - ±1.0% @ 0°C to +60°C - ±1.5% @ −20°C to +85°C - ±2.5% @ −40°C to +85°C • Low-Speed Internal Oscillator (LSI): 32 kHz - ±30% @ −40°C to +85°C
	Operation mode	• RUN mode • SLEEP mode • DEEP-SLEEP (STOP1, STOP2) mode
	Reset	• nRESET Pin reset (PC9) • Core reset • Software reset • POR (Power-On Reset) • LVR (Low Voltage Reset) • WDTR (Watchdog Timer Reset)
	VDC	Built-in LDO regulator for low voltage operation
	POR	POR generator: Capable of generating a reset signal by detecting an internal 1.48 V
	LVDI	• Four Low-voltage detection levels • Supports interrupts • Supports wake-up from DEEP-SLEEP mode
	Wake-up	• Wake-up by GPIO pins • Wake-up by Watchdog Timer (WDT) • Wake-up by LVI • Wake-up by USART

Table 3. A31C111 Series Features (continued)

Peripheral	Description
GPIO (General-Purpose I/O)	• I/O ports for general purpose • 20-QFN, 20-TSSOP - I/O pins: 18 • 16-SOPN - I/O pins: 14 • 10-SSOP - I/O pins: 8 • Selectable input and output configuration for each pin: - Push-pull output - Open drain output - Input • Pin configurations through multiplexer settings • Configurable as an external interrupt source with the following options: - Rising-edge (high-level) - Falling-edge (low-level) - Edge-triggered (both rising-edge and falling-edge) • Configurable pull-up/down resistors and debouncing • Configurable independently to be set or reset through its corresponding bit • Wake-up events triggered by external asynchronous inputs

Table 3. A31C111 Series Features (continued)

Peripheral		Description
Timer	16-bit Timer	• General-purpose 16-bit up-count timer • Four channels - 4 (TnIO) input capture channels - 4 (TnIO) output channels • Timer operating modes - Periodic timer mode - One-shot mode - PWM mode - Capture mode • Interrupt events - Timer/counter match interrupt - Timer overflow interrupt • Free selectable clock sources: - PCLK configurable through the peripheral clock enable register1 (SCU_PCER1) - LSI, MCLK, HSI configurable through the miscellaneous clock control register 3 (SCU_MCCR3) • Timer signals output through TnIO pins • 10-bit prescaler
	WDT (Watchdog timer)	• 32-bit down-count timer • Reset and periodic interrupts • Free selectable clock sources: - LSI, HSI configurable through the miscellaneous clock control register 1 (SCU_MCCR1) • Selectable eight different prescalers

Table 3. A31C111 Series Features (continued)

Peripheral		Description
Serial Interface	UART	• 16450 asynchronous serial communication ports • Channel support - One channel • Configurable standard asynchronous communication bits (start, stop, and parity) • Flexible communication available through programming - 5- to 8-bit data transfers - Even-/ Odd-/ Non-parity generation and checking - 1-bit, 1.5-bit, or 2-bit stop-bit generation and checking • 8-bit fraction controller and 16-bit baud rate generator
	I2C	• Standard I2C communication protocol • Channel support - One channel • Master and slave modes • 7-bit addressing for slave mode • Configurable SCL signal's high-/low-periods and SDA signal's hold time
	USART	• Full-Duplex Operation. (Independent Serial Receive and Transmit Registers) • Channel support - One channel • Asynchronous or Synchronous Operation • 8-bit fraction controller and 16-bit baud rate generator • Flexible communication available through programming - 5- to 9-bit data transfers - Even/Odd/Non-parity generation and checking - 1-bit, 2-bit stop bit generation and checking • Receive Character Detection and Receive Time Out function • Data overrun & Frame error detection • Three Separate Interrupts on TX Completion, TX Data Register Empty and RX Completion • Double-Speed Asynchronous communication mode

Table 3. A31C111 Series Features (continued)

Peripheral	Description
12-bit ADC	• One independent ADC block • Analog input channels - 20-QFN, 20-TSSOP: 8 channels - 16-SOPN: 8 channels - 10-SSOP: 4 channels • Multiple operating modes: - Single conversion - Sequence conversion - Burst conversion - Multiple conversion • Up to eight sequential conversions • Software triggers • Internal trigger sources (timers)
CRC (Cyclic Redundancy Check)	• CRC operating modes: - CRC32 (0x04C1_1DB7) - CRC16_USB (0x8005) - CRC16_CCITT (0x1021) - CRC8_CCITT (0x07) • Support for byte reversal of input/output data
Operating voltage	1.7 V to 5.5 V
Operating temperature	Commercial grade (−40°C to +85°C)
Package	• Three types of package options - 20-QFN-0404 - 20-QFN-0303 - 20-TSSOP - 16-SOPN - 10-SSOP

Table 4. Summary of A31C111 Peripherals

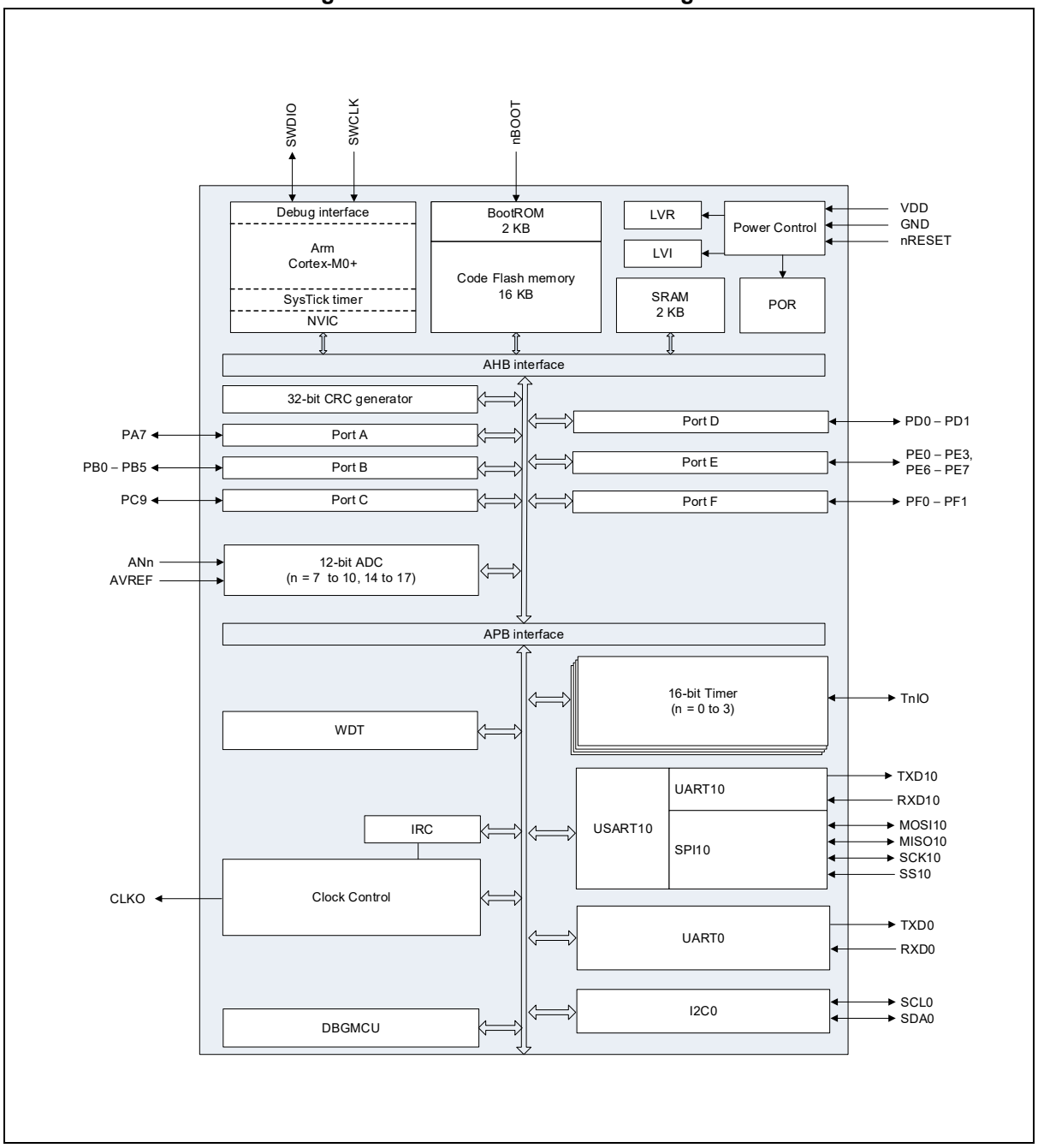
Peripheral		A31C111 FUN	A31C111 FYN	A31C111 FRN	A31C111 AEN	A31C111 TSN
Code flash memory		16 KB				
SRAM		4				
Timers	GP Timer	4 (16-bit)	4 (16-bit)	4 (16-bit)	4 (16-bit)	2 (16-bit)
	SysTick timer	1				
	WDT	1				
Communication Interfaces	UART	1	1	1	1	1
	I2C	1	1	1	1	1
	USART	1	1	1	1	1*
GPIO		18	18	18	14	8
ADCs		150 ksps				
Number of channels		8	8	8	8	4
Max. CPU frequency		32 MHz				
CRC		1				
Operating voltage		1.7 V to 5.5 V				
Operating temperature		Ambient operating temperature: −40°C to +85°C				
Packages		20-QFN 0404	20-QFN 0303	20-TSSOP	16-SOPN	10-SSOP

NOTE:

1. SPI is not supported on the 10-pin SSOP package because the USART SCK pin is not available.

2.3 Block Diagram

Figure 1. A31C111 Series Block Diagram



2.4 Functional Overview

The following sections provide overviews of the features of the A31C111 series microcontroller.

2.4.1 Cortex-M0+ Core

The A31C111 series adopts the energy-efficient 32-bit microcontroller core, Cortex-M0+ of ARM, as its CPU. The Cortex-M0+, designed for low-power consumption, uses the ARMv6-M Instruction set to improve performance and energy efficiency.

Refer to the technical reference manual "ARM DDI 0484C" for detailed information on Cortex-M0+.

2.4.2 Embedded SRAM

The A31C111 series has a block of zero-wait on-chip SRAM. The size of the SRAM is 2 KB. The base address is 0x2000_0000.

The SRAM memory area is commonly utilized for storing data and as a stack memory. It can also store program code for faster execution or during flash erase/programming operations.

2.4.3 Boot Configuration

The A31C111 series offers a boot mode for programming the internal flash memory. The boot mode can be entered by setting the nBOOT pin to 'L' during the system reset process (the normal state is 'H').

The boot mode supports the UART boot, which uses the UART interface to transmit and receive boot data (TXD10/RXD10).

The pins for the boot mode are listed in Table 5.

Table 5. Boot Mode Pin List

Block	Pin Name	I/O	Pin Direction	Description
SYSTEM	nRESET	PC9	Input	Receive the reset signal
	nBOOT	PB3	Input	Set the boot mode
UART mode (USART10)	RXD10	PB1	Input	Receive the UART boot data
	TXD10	PB0	Output	Transmit the UART boot data

2.4.4 Power Supply

The device operates with a supply voltage of 1.7 V to 5.5 V (V_{DD}). The analog peripherals are also powered through V_{DD}, internally connected to AV_{DD} within the microcontroller.

Table 6. Power Supply

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	V_{DD}	1.7	5.5	V

During a power-up process, a reset plays an important role and affects the entire process of the system booting. The A31C111 series has two power-related reset options, as described below:

- POR_RST (Power-On Reset): Controls the voltage less than 1.48 V
- LVD_RST (Low-Voltage Detect Reset): Controls the voltage less than 1.58 (default)

If the power level is higher than the POR and is below the flash operating voltage, the Code Read operation may malfunction. To prevent this abnormal Code Read operation, the LVD_RST generates the SYSRESETn internal signal, and the microcontroller enters the reset mode to prevent the abnormal operation. The minimum level that the LVR can set is 1.58V, which meets the minimum flash operating voltage.

2.4.5 Operation Mode

2.4.5.1 Transition of Operation Mode

INIT mode is the initial state of the chip when a reset is asserted. In RUN mode, the CPU operates at the maximum performance with the high-speed clock system. SLEEP and DEEP-SLEEP modes can be used as low-power consumption modes. In the low-power consumption mode, power is effectively managed to reduce power consumption by halting the processor core and any unused peripherals.

2.4.5.2 RUN Mode

The CPU and peripheral hardware operate with a high-speed clock in RUN mode. After a reset, the system will enter RUN mode if the INIT state is detected.

2.4.5.3 SLEEP Mode

Once the microcontroller enters SLEEP mode, the CPU becomes inactive. By setting the SCU_PER and SCU_PCER registers, users can determine which peripherals will be inactive in SLEEP mode.

2.4.5.4 DEEP-SLEEP (STOP1, STOP2) Mode

The microcontroller enters DEEP-SLEEP mode when the core goes under the stop state using WFI instruction.

2.4.5.5 Reset Mode

The A31C111 series has two system reset options: a cold reset, which is effective during power-up or down sequences, and a warm reset, which is triggered by multiple reset sources.

The reset features of the A31C111 series are as follows:

- Power-On Reset (POR)
- Low-Voltage Detect Reset (LVR)
- nRESET pin reset
- Watchdog Timer (WDT) reset
- Software reset
- Clock oscillating error reset
- CPU request reset

2.4.6 Clocks and Start-Up

The A31C111 series has two main operating clocks: HCLK, which generates clock signals for the CPU and AHB system, and PCLK, which generates clock signals for peripheral systems.

2.4.6.1 HCLK Clock

The Cortex-M0+ core requires two clocks: HCLK and FCLK. While the HCLK supplies the clock for both the CPU and AHB, the FCLK remains enabled unless the system enters DEEP-SLEEP mode. Conversely, during SLEEP mode, the HCLK can be disabled while the FCLK continues to function.

The HCLK clocks the buses and memories. As the bus clock frequency is limited to a maximum of 32 MHz, the HCLK frequency must not exceed 32 MHz.

2.4.6.2 PCLK Clock

The PCLK can be used as a clock source for any peripheral. The SCU_PCER registers determine whether the PCLK is enabled or disabled for each peripheral. If a peripheral block's PCLK input is not enabled, its registers cannot be read. Additionally, it is important to note that the PCLK stops operating in DEEP-SLEEP mode.

2.4.6.3 Clock Configuration Procedure

After power-on, HSI (4 MHz, 32 MHz/8) operates as a system clock by default. The HSI is enabled during the power-up sequence.

2.4.7 Interrupts and Events

2.4.7.1 NVIC (Nested Vectored-Interrupt Controller)

The A31C111 series includes up to 32 maskable interrupt sources that manage sixteen priority levels. The Nested Vector Interrupt Controller (NVIC) controls 16 interrupt lines of the Cortex-M0+.

The NVIC has the following advantages:

- Interrupt processing with reduced interrupt latency
- Direct transfer of Interrupt Vector Table (IVT) address to the core
- The fast interrupt processing capability
- Interrupts with higher priority precede those with lower priority, even if they occur after the lower priority interrupts.
- Automatic saving of processor state
- Interrupt restoring without instructional overhead at the end of the interrupt

The NVIC hardware block provides flexible and efficient interrupt management with minimal interrupt latency.

2.4.7.2 EXTI (Extended Interrupt)

The Extended Interrupt feature enables the system to generate event requests and wake up from STOP mode. Each external line can be configured independently to detect trigger events such as rising or falling edges or both edges and level events such as low or high.

2.4.8 GPIO

2.4.8.1 PCU Module

The A31C111 series has a Port Control Unit (PCU) module that controls the input and output (I/O) ports.

Users can configure the functionality, input/output direction, pull-up/pull-down, and debounce the pins for their applications by setting the PCU registers.

2.4.8.2 GPIO Module

Pins other than those specified as V_{DD}, GND, or for certain purposes can be used as General-Purpose Input/Output (GPIO) pins.

The GPIO module controls the general I/O pins. Output pins can be configured to output high- or low-level signals by setting the corresponding bits of the GPIO control register. On the other hand, the input status of logic input pins can be monitored through the control registers.

2.4.9 Embedded Flash Memory

The flash memory controller serves as an interface between the core and the embedded flash memory and is responsible for managing the data stored on the flash memory.

The flash memory of the A31C111 series has the following features:

- 16 KB of code flash memory with write protection bits.
- Erase units
  - Page (512 bytes)
  - Sector (2 KB)
  - Bulk (full chip)
- Program unit: Word (4 bytes)
- Zero wait (less than 25 MHz), 1- to 15-wait
- Code flash memory read protection
- Code flash memory write protection

2.4.10 Timers

2.4.10.1 16-bit Timers

This 16-bit Timer supports four operating modes: Periodic Mode, PWM Mode, One-shot Mode, and Capture Mode.

Users can use a divided PCLK or an external clock as a clock source for the 16-bit Timer. An internal 10-bit prescaler allows to generate a variety of base clocks for the timer.

Interrupts can be triggered at regular intervals when the timer is used in Periodic Mode. Users can set the period and duty to form a PWM signal used in PWM Mode.

In One-shot Mode, the timer can generate one PWM waveform. The Capture Mode allows measuring the pulse intervals of an external input signal based on the predefined conditions. In addition, this timer can transmit signals to control other devices and is primarily used as a periodic tick timer or as a wake-up source.

2.4.10.2 WDT

The Watchdog Timer (WDT) detects errors in the microcontroller caused by external interference or logically unexpected conditions. These errors cause the application program to deviate from its normal sequence. If the microcontroller loses control, the WDT will reset the microcontroller, allowing it to return to normal operation.

The WDT of the A31C111 series is a 32-bit down counter. If the WDT is set as a reset source, the microcontroller restarts when the down counter reaches zero.

When it is not used to monitor the microcontroller, the WDT can be used as a cycle timer along with an interrupt.

2.4.10.3 SysTick Timer

Although the SysTick timer is primarily designed for real-time operating systems, it can also be utilized as a standard down-counter.

The SysTick timer has the following features:

- 24-bit down-counter
- Automatic reload
- Maskable system interrupt generation when the counter reaches zero.
- Programmable clock source

2.4.11 UART

The built-in UART (Universal Asynchronous Receiver/Transmitter) module allows users to specify settings for transmitting and receiving data and provides the ability to read the status of the UART. By providing information about the current state of transmission and reception processes, including types and conditions, the UART module enables users to monitor potential errors such as parity, overrun, framing, or break interrupts during data reception.

The UART module includes a programmable baud-rate generator for each channel, which generates an internal clock for its corresponding UART unit. This is achieved by dividing a prescaled clock using a baud-rate divisor ranging from 1 to 65,535, then dividing the result by 16.

Users can program interrupts that can control UART communication.

2.4.12 I2C

The I2C (Inter-integrated Circuit) interface built in the A31C111 series complies with the standard I2C communication protocol. It is used for serial communication between internal and external devices via the I2C protocol.

Equipped with one unit, it supports both master and slave modes and can transmit and receive data in bytes by using interrupts or polling.

The I2C interface of the A31C111 series operates in Standard mode (100 kHz) or Fast mode (400 kHz). In addition, it also supports General calls.

The I2C interface facilitates communication with multiple peripherals that share the same bus type. To utilize I2C, it is recommended to configure the SCL and SDA pins as open-drain and attach external pull-up resistors to ensure that their output signals are maintained in the 'High' state.

Table 7. Features of I2C

I2C Features	I2C
7-bit addressing mode	O
Standard mode (up to 100 kbit/s)	O
Fast mode (up to 400 kbit/s)	O
General call	O

2.4.13 USART

Universal Synchronous and Asynchronous serial Receiver and Transmitter (USART) is a highly flexible serial communication device. The main features are listed below:

- Full Duplex Operation. (Independent Serial Receive and Transmit Registers)
- Asynchronous or Synchronous Operation.
- Baud Rate Generator.
- Supports Serial Frames with 5,6,7,8, or 9 Data bits and 1 or 2 Stop bits.
- Odd or Even Parity Generation and Parity Check are Supported by Hardware.
- Data Over Run Detection.
- Framing Error Detection.
- Three Separate Interrupts on TX Completion, TX Data Register Empty and RX Completion.
- Double Speed Asynchronous communication mode.

Additional features are :

- 0% Error Baud Rate by floating point count register.
- Supports receive time out interrupt.
- Supports direct memory access and interrupt.

2.4.14 ADC

The A31C111 series features a 12-bit resolution Analog-to-Digital Converter (ADC) module. It consists of an independently controllable unit and A31C111 supports up to 8 different analog inputs. This ADC module supports A/D conversion of multiple channels in different modes, including single mode, sequential mode, multiple mode, burst mode. It can sample the voltage inputs of multiple channels at critical times, which is required for various applications and can be achieved using the triggering functionality in association with TIMER.

Once the A/D conversion is complete, the result is left aligned in 16-bit data registers.

The ADC is mapped to the AHB and capable of high-speed operation based on the internal clock source.

The analog input monitoring and comparison capabilities of the ADC allow the applications to determine whether the input voltage is above or below the predefined level.

2.4.15 CRC

The Cyclic Redundancy Check (CRC) module is used to calculate 32-bit, 16-bit USB, 16-bit CCITT and 8-bit CCITT CRC codes from 8-bit or 32-bit data size. The user application can utilize CRC-based technologies to ensure the integrity of data transfers, storage, and flash memories in compliance with functional safety standards. With this module, users can verify the integrity of data transfers and flash memory.

2.5 Development Support

This chapter describes the development support features of the device. The device provides standard Arm® development support, including toolchain compatibility, debug interface, trace support, and on-board debug/programming connection.

Refer to the feature list, pin description, and electrical characteristics for detailed information.

2.5.1 Toolchain Support

The device supports software development using standard Arm-compatible tool chains, including Arm® Keil® MDK, IAR Embedded Workbench® for Arm, and GCC-based tool chains.

Device-specific startup files, linker scripts, header files, and software examples are provided separately for each product series and software package.

2.5.2 Debug Interface

2.5.2.1 Serial Wire Debug Port (SW-DP)

The device provides an Arm® Serial Wire Debug Port (SW-DP) for software debugging and in-system flash memory programming. The SW-DP uses a two-pin debug interface, SWDIO and SWCLK, to access the CPU debug logic, memory, registers, and on-chip debug resources.

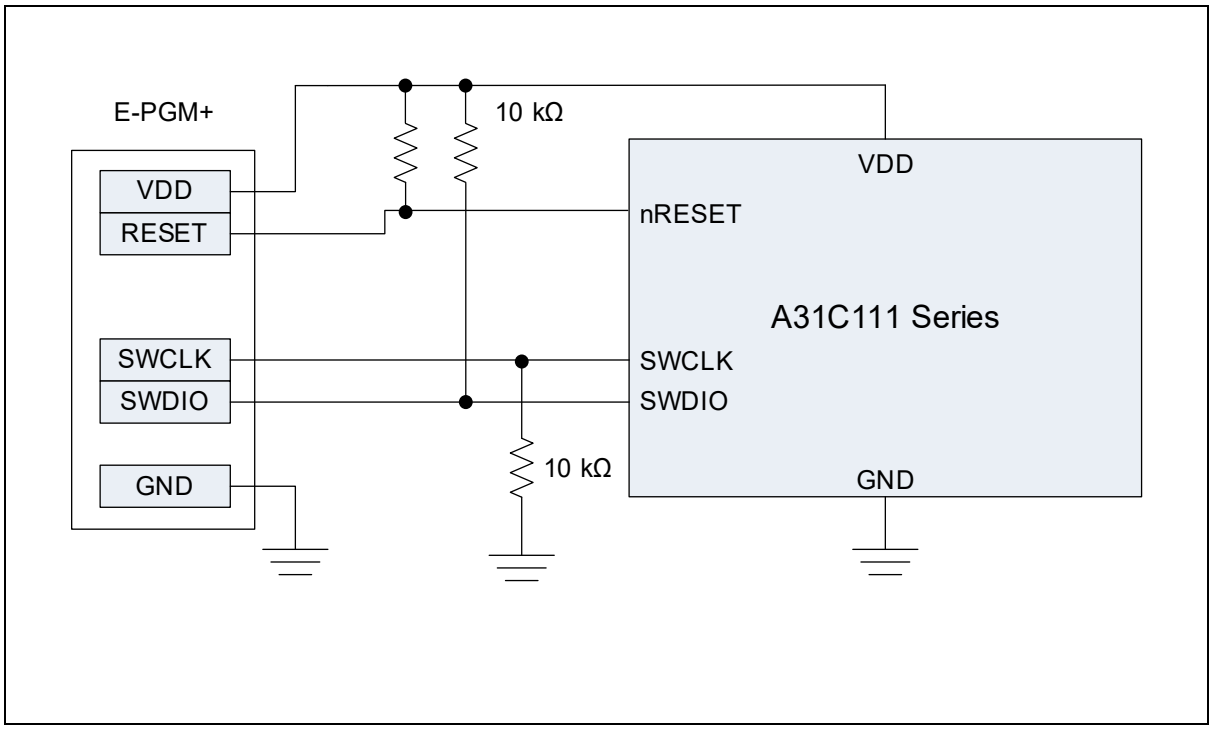
The SWD pins may be multiplexed with GPIO or other alternate functions depending on the product and package. If the SWD pins are used for application functions, the target board and firmware must be designed so that the pins remain accessible during debugging or programming.

2.5.2.2 SWD Connection Guide

For on-board debugging and programming, the target board should provide access to SWDIO, SWCLK, VDD, VSS, and nRESET. The nRESET connection is recommended to improve debug connection reliability and device recovery.

The VDD pin provides the target voltage reference for the external debug probe. It should be connected to the target board supply voltage unless otherwise specified by the debug probe manufacturer.

Figure 2. SWD Interface Connection



3. Pinouts and Pin Descriptions

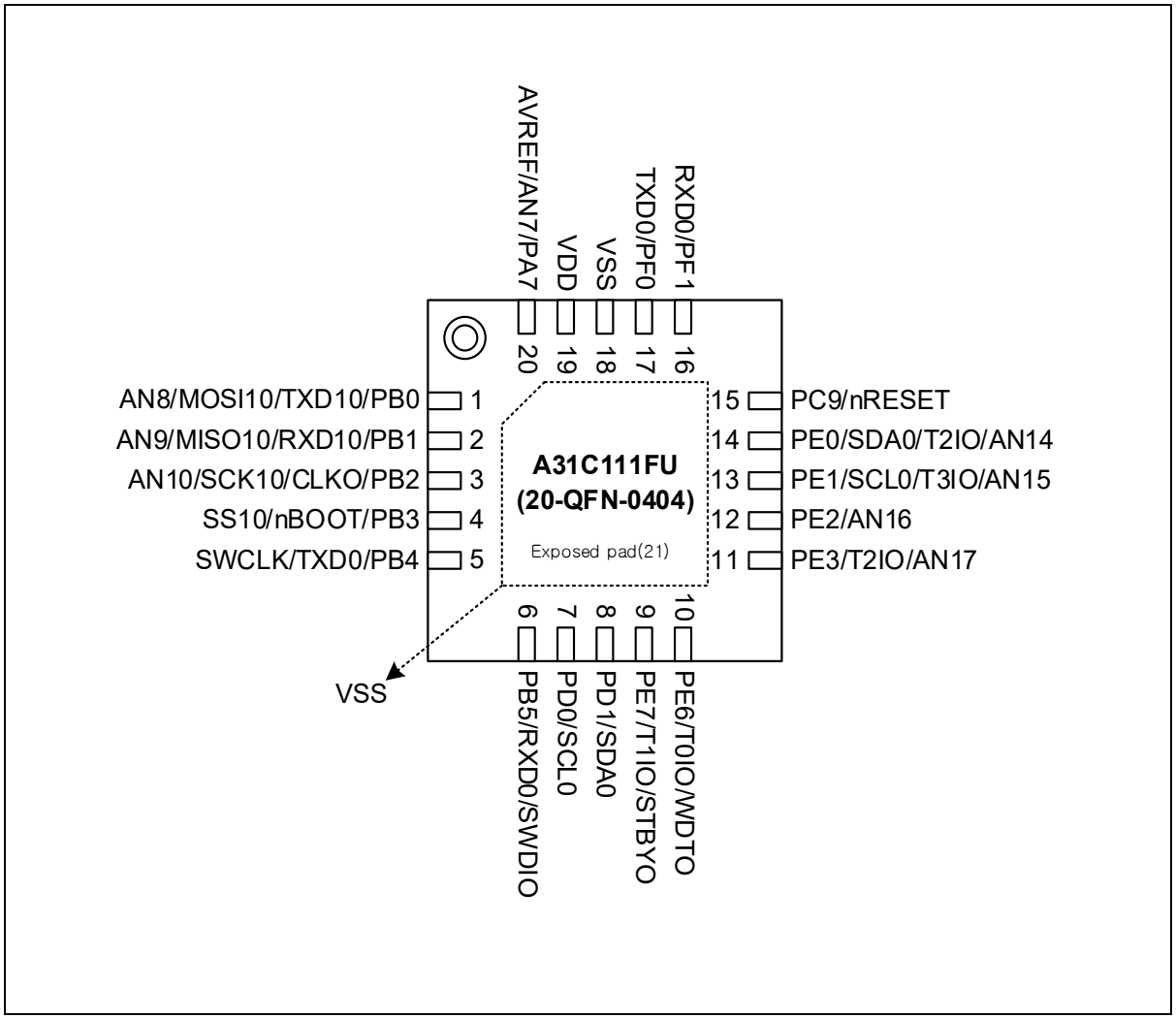
In this chapter, pinouts and pin descriptions of the A31C111 series are described.

3.1 Pinouts

Figure 3 through Figure 7 show the top views of the packages.

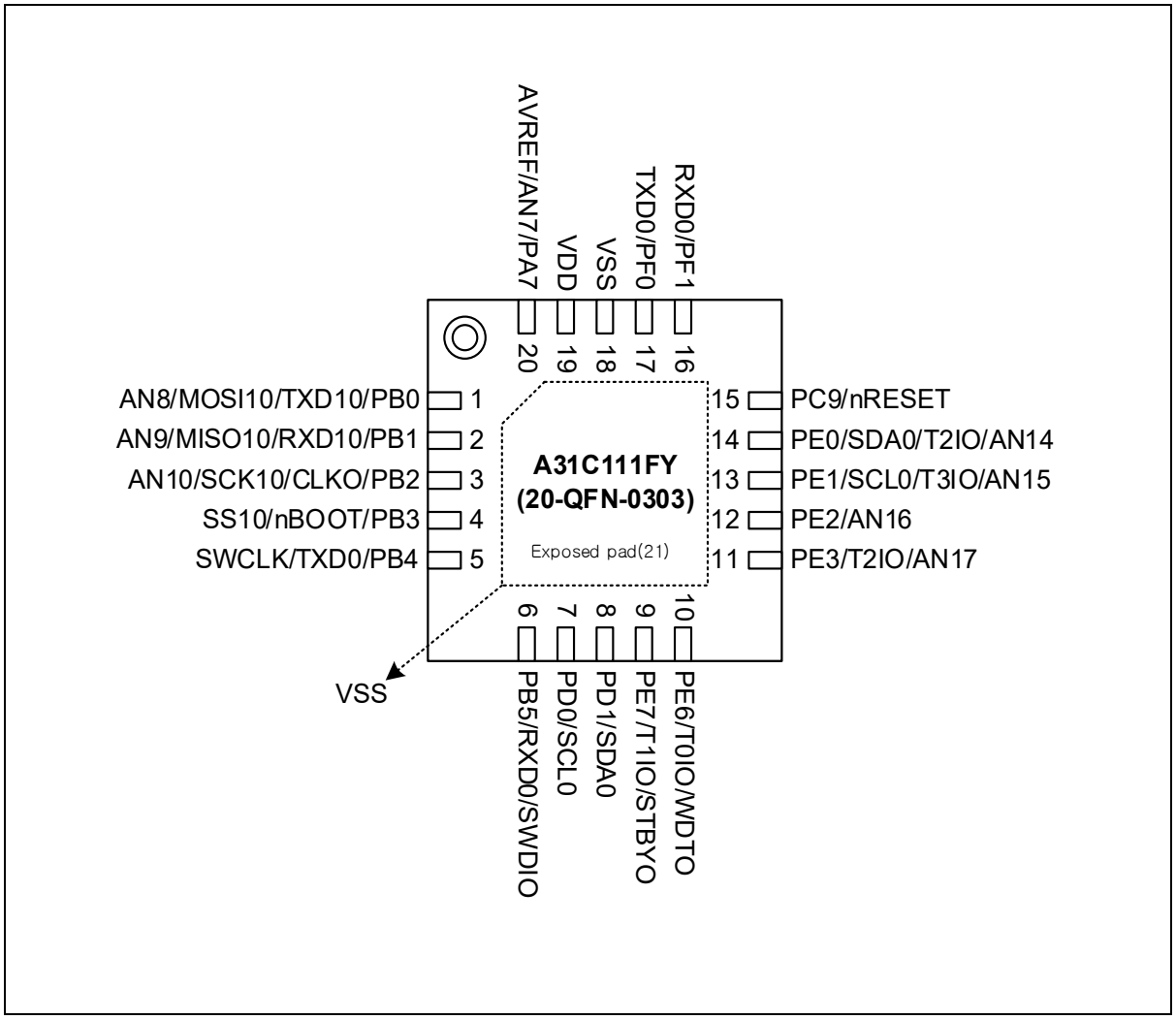
3.1.1 A31C111FU (20-QFN-0404)

Figure 3. A31C111FU (20-QFN-0404) Pinouts



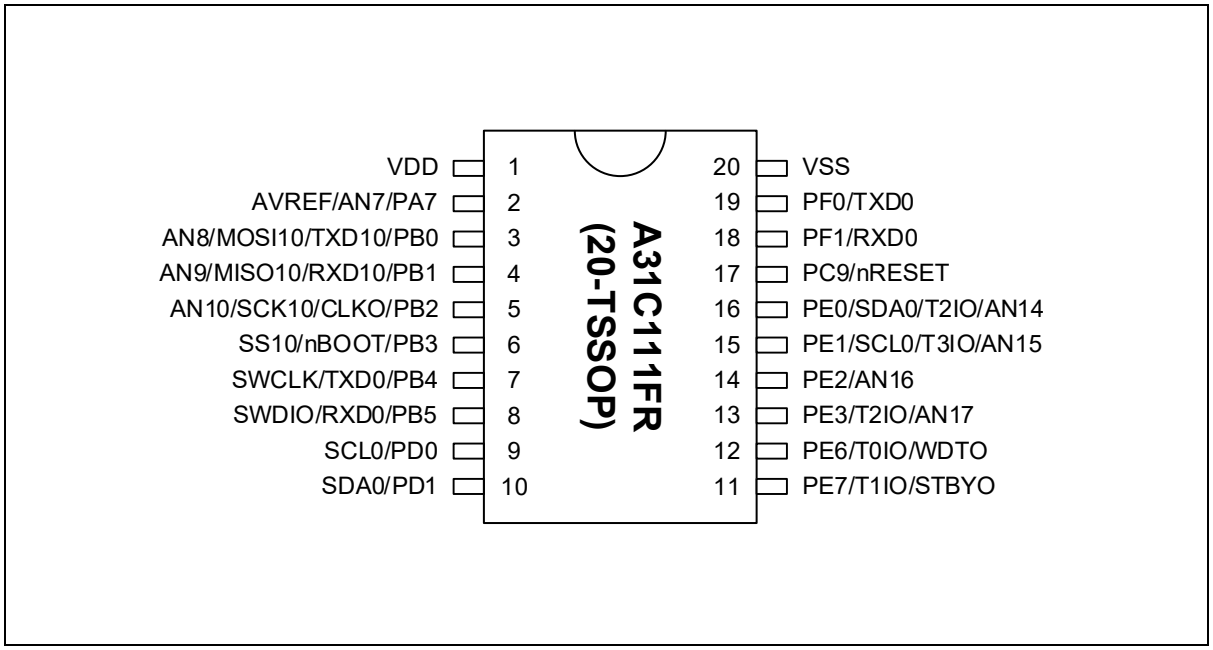
3.1.2 A31C111FY (20-QFN-0303)

Figure 4. A31C111FY (20-QFN-0303) Pinouts



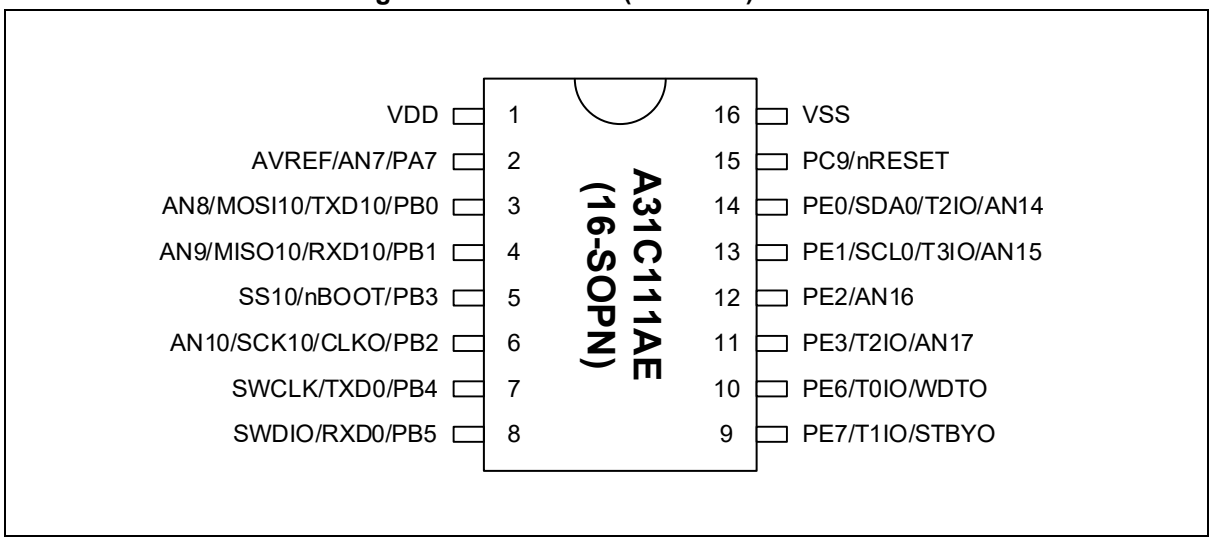
3.1.3 A31C111FR (20-TSSOP)

Figure 5. A31C111FR (20-TSSOP) Pinouts



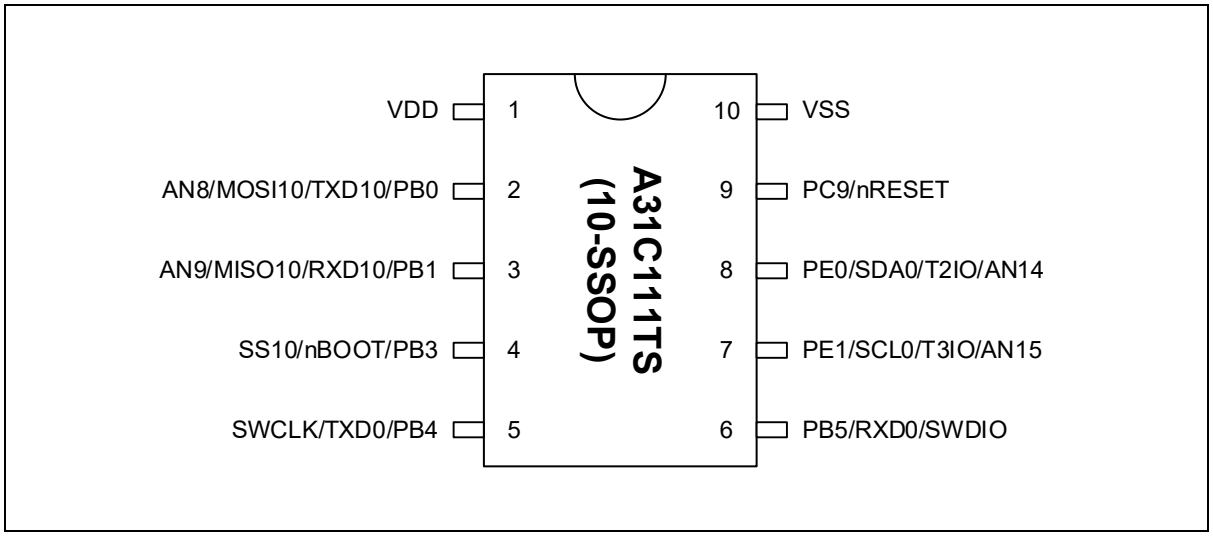
3.1.4 A31C111AE (16-SOPN)

Figure 6. A31C111AE (16-SOPN) Pinouts



3.1.5 A31C111TS (10-SSOP)

Figure 7. A31C111TS (10-SSOP) Pinouts



3.2 Pin Description

Table 8. Legend and Abbreviations Used in Pin Description

Name	Abbreviation	Definition
Pin name	• The pin name remains constant. • Users can assign a function to the pin using the alternate function.	
Pin type	I	Input
	O	Output
	I/O	Input/Output
	U	Pull-up
	D	Pull-down
	S	Schmitt-Trigger input
	C	CMOS input
	A	Analog
	P	Power

NOTES:

1. After a reset, all the pins are configured to function as defined by their initial values.
2. Unused pins are set to output from Firmware. (Low output is recommended).
3. PB3 (nBOOT), PC9 (nRESET), PB5 (SWDIO) and the default pull-up pins and PB4 (SWCLK) are default pull-down pin.
4. Do not configure unused pins as floating inputs.
5. After a reset, the internal pull-up for the boot pin is enabled.
6. After a reset, the internal pull-up for the Serial Wire Data I/O (SWDIO) is enabled and the internal pull-down for the Serial Wire Clock (SWCLK) is enabled.
7. The SWCLK and SWDIO pins should not be switched to other functions while they are being used.

The pin configuration information in Table 9 contains two pairs of power/ground and other dedicated pins. These multi-function pins have up to six selections of functions, including GPIO. Configuration, including pin ordering, can be changed without notice.

Table 9. Pin Description

Pin No.				Pin Name	Type	Description	Remark
20-pin (QFN)	20-pin (TSSOP)	16-pin	10-pin				
1	3	3	2	PB0	IOUS	Port B bit 0 input/output	
				TXD10	O	UART(USART) CH0 data output	
				MOSI10	IO	SPI(USART) CH0 Master out/Slave input	
				AN8[1]	IA	Analog input 8	
2	4	4	3	PB1	IOUS	Port B bit 1 input/output	
				RXD10	I	UART(USART) CH0 data Input	
				MISO10	IO	SPI(USART) CH0 Master input/Slave output	
				AN9[1]	IA	Analog input 9	
3	5	6	-	PB2	IOUS	Port B bit 2 input/output	
				CLKO	O	System clock output	
				SCK10	IO	SPI(USART) CH0 clock input/output	
				AN10[1]	IA	Analog input 10	
4	6	5	4	PB3	IOUS	Port B bit 3 input/output	
				nBOOT[1][2][5]	I	Boot mode selection input	Pull-up
				SS10	IO	SPI(USART) CH0 slave select input	
5	7	7	5	PB4	IOUS	Port B bit 4 input/output	
				TXD0	O	UART CH0 TXD output	
				SWCLK[1][2][6][7]	I	SWD clock input	Pull-down
6	8	8	6	PB5	IOUS	Port B bit 5 input/output	
				RXD0	I	UART CH0 RXD input	
				SWDIO[1][2][6][7]	IO	SWD data input/output	Pull-up
7	9	-	-	PD0	IOUS	Port D bit 0 input/output	
				SCL0	IO	I2C CH0 SCL input/output	
8	10	-	-	PD1	IOUS	Port D bit 1 input/output	
				SDA0	IO	I2C CH0 SDA input/output	
9	11	9	-	PE7	IOUS	Port E bit 7 input/output	
				T1IO	IO	Timer 1 input/output	
				STBYO	O	Deep Sleep mode output	
10	12	10	-	PE6	IOUS	Port E bit 6 input/output	
				T0IO	IO	Timer 0 input/output	
				WDTO	O	Watchdog timer overflow output	

Table 9. Pin Description (continued)

Pin No.				Pin Name	Type	Description	Remark
20-pin (QFN)	20-pin (TSSOP)	16-pin	10-pin				
11	13	11	-	PE3	IOUS	Port E bit 3 input/output	
				T2IO	IO	Timer 2 input/output	
				AN17(1)	IA	Analog input 17	
12	14	12	-	PE2	IOUS	Port E bit 2 input/output	
				AN16(1)	IA	Analog input 16	
13	15	13	7	PE1	IOUS	Port E bit 1 input/output	
				SCL0	IO	I2C CH0 SCL input/output	
				T3IO	IO	Timer 3 input/output	
				AN15(1)	IA	Analog input 15	
14	16	14	8	PE0	IOUS	Port E bit 0 input/output	
				SDA0	IO	I2C CH0 SDA input/output	
				T2IO	IO	Timer 2 input/output	
				AN14(1)	IA	Analog input 14	
15	17	15	9	PC9	IOUS	Port C bit 9 input/output	
				nRESET(1)(2)	I	External reset input	Pull-up
16	18	-	-	PF1	IOUS	Port F bit 1 input/output	
				RXD0	I	UART CH0 RXD input	
17	19	-	-	PF0	IOUS	Port F bit 0 input/output	
				TXD0	O	UART CH0 TXD output	
18	20	16	10	VSS	P	Ground	
19	1	1	1	VDD	P	VDD	
20	2	2	-	PA7	IOUS	Port A bit 7 input/output	
				AVREF	IA	Analog reference input	
				AN7(1)	IA	Analog input 7	

3.3 Alternate Function Pins

The GPIO pins have alternate functions, as described in Table 10.

Table 10. GPIO Alternate Function [1]

Pin Name	Alternate Function					
	AF0	AF1	AF2	AF3	AF4	AF7
PA7	PA7					AN7/AVREF [2]
PB0	PB0	TXD10			MOSI10	AN8 [2]
PB1	PB1	RXD10			MISO10	AN9 [2]
PB2	PB2			CLKO	SCK10	AN10 [2]
PB3	PB3			nBOOT [2]	SS10	
PB4	PB4	TXD0		SWCLK [2]		
PB5	PB5	RXD0		SWDIO [2]		
PC9	PC9			nRESET [2]		
PD0	PD0	SCL0				[2]
PD1	PD1	SDA0				[2]
PE0	PE0	SDA0	T2IO			AN14 [2]
PE1	PE1	SCL0	T3IO			AN15 [2]
PE2	PE2					AN16 [2]
PE3	PE3		T2IO			AN17 [2]
PE6	PE6		T0IO	WDTO		[2]
PE7	PE7		T1IO	STBYO		[2]
PF0	PF0				TXD0	[2]
PF1	PF1				RXD0	[2]

NOTES:

1. Unused pins are set to output from firmware (low output is recommended).
2. After a reset, all the pins are configured to function defined by their initial values. The initial value of the pin depends on the package type. This configuration follows the 20-pin standard.

4. Electrical Characteristics

4.1 Parameter Conditions

Unless otherwise specified, all voltages are referenced to GND.

4.1.1 Minimum and Maximum Values

Unless otherwise specified, our production tests guarantee the minimum and maximum values of the device under the worst-case conditions of ambient temperature, supply voltage, and frequency.

Data based on characterization results, design simulation, and/or technical characteristics are not tested in production but are indicated in the table footnotes.

4.1.2 Typical Value

Unless otherwise specified, typical data are based on the conditions of T_A = -40°C to 85°C and V_{DD} = 5.0 V. The typical data are provided only as design recommendations and are not tested.

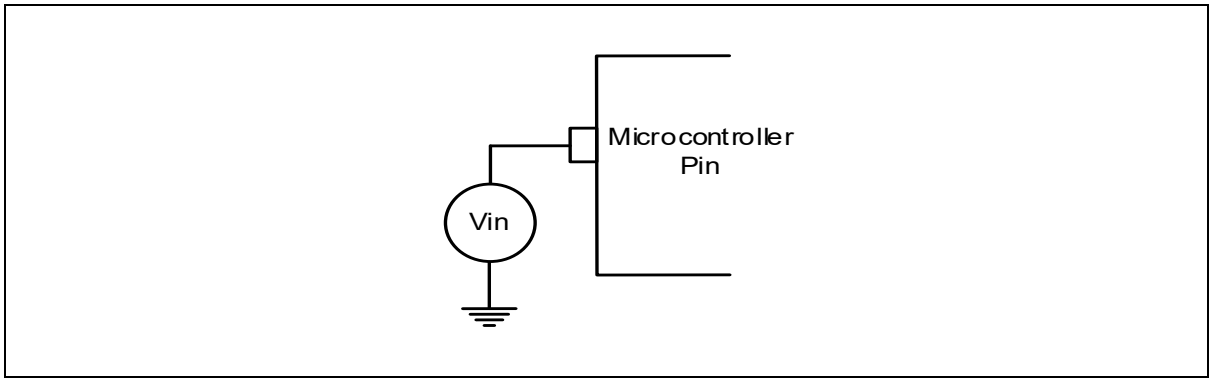
4.1.3 Typical Curves

Unless otherwise specified, all typical curves are provided only as design recommendations and are not tested.

4.1.4 Pin Input Voltage

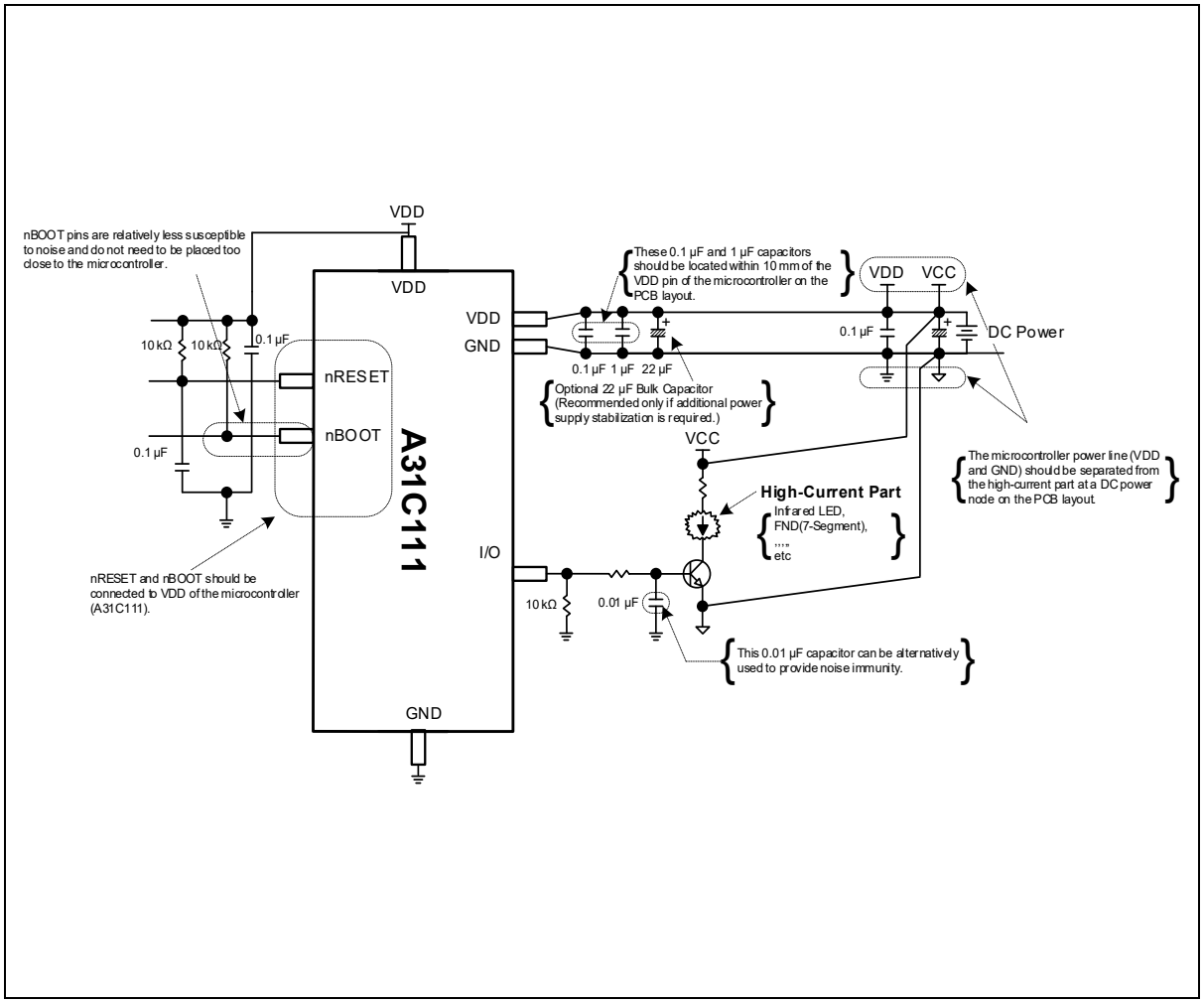
The input voltage measurement on a pin of the device is described in Figure 8.

Figure 8. Pin Input Voltage



4.1.5 Power Supply Scheme

Figure 9. Power Supply Scheme

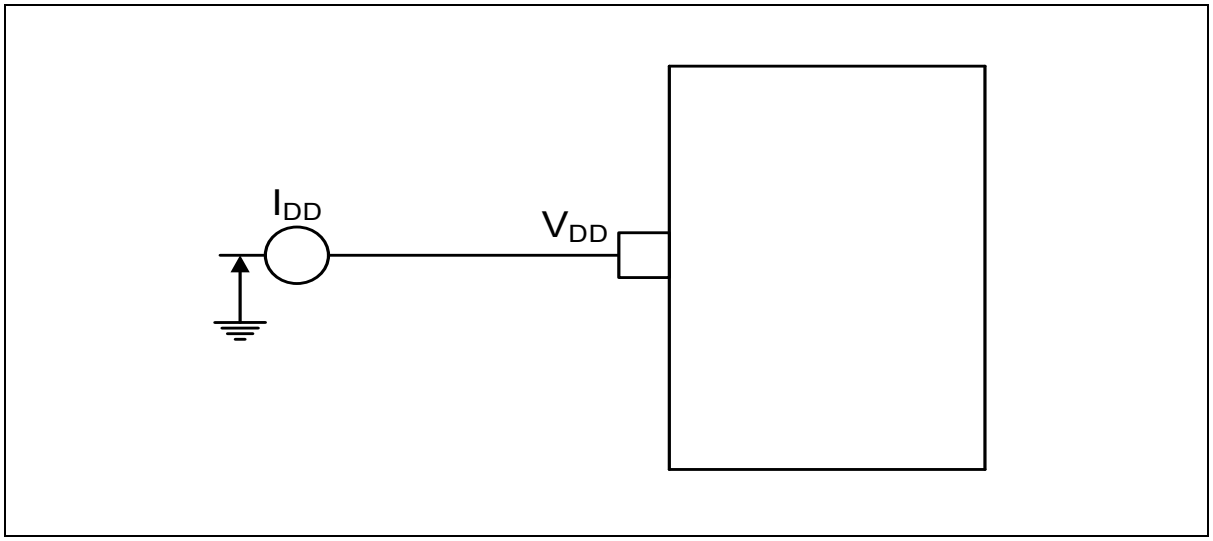


NOTES:

1. As shown above, each power supply pair (V_{DD}/GND, etc.) must be decoupled with filtering ceramic capacitors. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.
2. Product A31C111 requires 1 µF and 0.1 µF bypass capacitors to be mounted on the VDD line.

4.1.6 Current Consumption Measurement

Figure 10. Current Consumption Measurement



NOTE:

1. The I_{DD} parameter represents the total microcontroller's current consumption, including the current supplying V_{DD}.

4.2 Absolute Maximum Ratings

Exceeding stresses specified in Table 11 for voltage characteristics, Table 12 for current characteristics, or Table 13 for thermal characteristics may result in permanent damage to the device. The values in the tables are stress ratings only and do not imply that the device will function properly under these conditions. Prolonged exposure to these maximum rating conditions may impact on the device's reliability. It is important to operate the device within its specified maximum ratings to ensure reliable performance.

Table 11. Voltage Characteristics

Symbol	Ratings	Min.	Max.	Unit
V_{DD}–GND(1)	External main supply voltage (including V_{DD})	-0.5	6.0	V
V_I(2)	Input voltage on I/O	-0.5	Max (V_{DD}) + 0.5	V
V_O	Output voltage on I/O	-0.5	Max (V_{DD}) + 0.5	V

NOTES:

1. All main power (V_{DD}) and ground (GND) pins must always be connected to the external power supply within the permitted range.
2. V_I maximum must always be respected.

Table 12. Current Characteristics

Symbol	Ratings	Max.	Unit
$\sum I_{VDD}$	Total current into the sum of all V_{DD} power lines (source)(1)	-120	mA
$\sum I_{GND}$	Total current out of the sum of all GND ground lines (sink)(1)	120	mA
$I_{VDD(PIN)}$	Maximum current into each V_{DD} power pin (source)(1)	-100	mA
$I_{GND(PIN)}$	Maximum current out of each GND ground pin (sink)(1)	100	mA
$I_{IO(PIN)}$	Output current sunk by any I/O	15	mA
	Output current sourced by any I/O and control pin	-9	mA
$\sum I_{IO(PIN)}$	Total output current sunk by the sum of all I/Os and control pins(2)	45	mA
	Total output current sourced by the sum of all I/Os and control pins(2)	-27	mA
I_{IL}	Input low leakage current	1	µA
I_{IH}	Input high leakage current	1	µA
P_T	Total power dissipation	600	mW

NOTES:

1. All main power (V_{DD}) and ground (GND) pins must always be connected to the external power supplies in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.

Table 13. Thermal Characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-55 to +125	°C
T_J	Maximum junction temperature	+105	°C

4.3 Operating Condition

4.3.1 General Operating Condition

Table 14. General Operating Condition

(Temperature: -40°C to +85°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	Core and Peripherals	1.7(1)	-	5.5	V
		ADC used	2.4	-	5.5	V
FREQ	Operating frequency	HSI(2)	-	32	-	MHz
		LSI(3)	-	32	-	kHz
V_{IN}	I/O input voltage	5 V I/O	-0.3	-	V_{DD}	V
T_A	Ambient temperature	-	-40	-	85	°C
T_J	Junction temperature range	-	-40	40	125	°C

NOTES:

1. When RESET is released, functionality is guaranteed down to V_{LVR5} Min.
2. Refer to 4.3.7.1 for more detailed information.
3. Refer to 4.3.7.2 for more detailed information.

4.3.2 Power-On Reset (POR) Characteristics

Table 15. POR Electrical Characteristics

(Temperature: -40°C to +85°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{DD}	Operating current	-	-	120	-	nA
V_{set}	POR set level	-	1.1	1.48	1.65	V
V_{reset}	POR reset level	-	0.98	1.15	1.58	V
t_R	V_{DD} voltage rising time	-	0.02	-	20	ms/V
t_F	V_{DD} voltage falling time	-	0.4	-	20	ms/V

4.3.3 Operating Condition at Power-Up/Power-Down

Table 16. Operating Condition at Power-Up/Power-Down

(Temperature: -40°C to +85°C)

Symbol	Parameter	Condition	Min.	Max.	Unit
T_{VDD}	V_{DD} rise time rate	-	0.02	20	ms/V
	V_{DD} fall time rate	-	0.4	20	ms/V

4.3.4 Reset and Power Control Block Characteristics (LVR, LVI)

Table 17. Low-Voltage Reset Characteristics

(Temperature: -40°C to +85°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Operating voltage	-	-	5	5.5	V
V_{LVR0_F}	Detection level	Falling voltage	1.43	1.5	1.67	V
V_{LVR1_F}			2.5	2.7	2.9	
V_{LVR2_F}			3.4	3.7	4	
V_{LVR3_F}			3.82	4.22	4.62	
V_{LVR0_R}	Detection level	Rising voltage	1.45	1.58	1.69	V
V_{LVR1_R}			2.56	2.86	3.16	
V_{LVR2_R}			3.52	3.92	4.32	
V_{LVR3_R}			4.07	4.47	4.87	
-	Hysteresis	-	30	100	300	mV
-	Noise cancelling time	-	-	2	6	μs
I_{DD}	Operation current	-	-	4	6	μA
$I_{DD, STOP}$	Operation current (STOP)	-	-	3	100	nA

Table 18. Low-Voltage Indicator Characteristics

(Temperature: -40°C to +85°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Operating voltage	-	-	5	5.5	V
V_{LVI0_F}	Detection level	Falling voltage	2	2.21	2.41	V
V_{LVI1_F}			2.71	3.01	3.31	
V_{LVI2_F}			3.6	4	4.4	
V_{LVI3_F}			4.11	4.51	4.91	
V_{LVI0_R}	Detection level	Rising voltage	2.14	2.34	2.54	V
V_{LVI1_R}			2.89	3.19	3.49	
V_{LVI2_R}			3.84	4.24	4.64	
V_{LVI3_R}			4.38	4.78	5.18	
-	Hysteresis	-	30	100	300	mV
-	Noise cancelling time	-	-	2.2	6	μs
I_{DD}	Operation current	-	-	3.5	5	μA
$I_{DD, STOP}$	Operation current (STOP)	-	-	3	100	nA

4.3.5 Embedded Voltage Reference

Table 19. Embedded Internal Voltage Reference

(Temperature: -40°C to +85°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CORE}	Internal reference Voltage 2	-	1.534	1.59	1.646	V

4.3.6 Supply Current Characteristics

The amount of current consumed by the device is determined by various factors and parameters, including but not limited to the operating voltage, ambient temperature, load on I/O pins, software configuration, operating frequency, switching rate of I/O pins, location of the program in memory, and the binary code being executed.

The current consumption is measured under the conditions specified in Table 20.

4.3.6.1 Supply Current Consumption

Table 20. Supply Current Characteristics

(Temperature: -40°C to +85°C)

Symbol	Parameter	Condition			Voltage Scaling	Typ.	Max.	Unit
		LSI (32 kHz)	HSI (32 MHz)	f_{MCLK}				
I_{DD1} (Run)	Normal Operation (1)	STOP	RUN	f_{HSI}	5.0 V	3	-	mA
		RUN	STOP	f_{LSI}	5.0 V	750	-	µA
I_{DD2} (SLEEP)	SLEEP mode(1)	STOP	RUN	f_{HSI}	5.0 V	2.2	-	mA
		RUN	STOP	f_{LSI}	5.0 V	650	-	µA
I_{DD3} (STOP1)	DEEP-SLEEP mode (1)	VDC=STOP, WDT(LSI)=ON			5.0 V	4.5	-	µA
I_{DD3} (STOP2)		VDC=STOP, LVD=ON			5.0 V	50	-	µA
		VDC=STOP, LVD=OFF			5.0 V	1	-	µA

NOTE:

1. All peripherals are turned off.

4.3.6.2 I/O System Current Consumption

In the I/O system, current consumption can be separated into two components: Static and Dynamic.

4.3.6.3 I/O Static Current Consumption

When I/O pins configured as inputs with pull-up are externally held low, they generate a current consumption. This current consumption can be calculated using the values of the pull-up/pull-down resistors specified in the I/O port characteristics.

Any external pull-down or load must also be considered to estimate the current output pins consumption.

The current consumption of I/O pins configured as inputs may increase when an intermediate voltage level is applied externally. This additional consumption is caused by the input Schmitt-trigger circuits that detect the input value. Unless such a configuration is necessary for the application, this current consumption can be avoided by configuring these I/Os in analog mode. This is especially relevant for ADC and CMP input pins, which should be set up as analog inputs.

4.3.6.4 I/O Dynamic Current Consumption

Besides the internal peripheral current consumption, the application's I/Os also contribute to the overall current consumption. When an I/O pin switches, it draws current from the microcontroller's supply voltage to power the I/O pin circuitry and to charge/discharge any capacitive loads (either internal or external) connected to the pin.

4.3.7 Internal Clock Source Characteristics

The parameters listed in Table 21 and Table 22 are obtained through tests conducted under ambient temperature and supply voltage conditions specified in Table 14.

4.3.7.1 High-Speed Internal RC Oscillator (HSI32)

Table 21. HSI32 Oscillator Characteristics (1)

(Temperature: -40°C to +85°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{HSI32}	HSI32 frequency	-	-	32	-	MHz
f_E	Frequency error	@ 0°C to 65°C	-1.0	-	1.0	%
		@ −20°C to 85°C	-1.5	-	1.5	%
		@ −40°C to 85°C	-2.5	-	2.5	%
DuCy (HSI32)	Duty cycle	-	-	50	-	%
Δ_{VDD} (HSI32)	HSI32 oscillator frequency drift over V_{DD}	V_{DD}=1.7 V to 5.5 V	-	0.2	-	%
t_{SU} (HSI32)	HSI32 oscillator start-up time	-	-	-	4.5	µs
t_{STAB} (HSI32)	HSI32 oscillator stabilization time	-	-	-	7.8	µs
I_{DD} (HSI32)	HSI32 oscillator power consumption	-	-	400	-	µA

NOTE:

1. Guaranteed by characterization results and design.

4.3.7.2 Low-Speed Internal 32 kHz RC Oscillator (LSI)

Table 22. LSI Oscillator Characteristics (1)

(Temperature: -40°C to +85°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{OUT}	Output frequency	@ -40°C to 85 °C	-	32	-	kHz
f_E	Frequency error (V_{DD} = 3.0V)	@ -40°C to 85 °C	-30	-	30	%
t_{VREG_SU}	32 kHz oscillator start-up time (after LSI32K LDO enabled)	V_{DD} = 5.0 V	-	20	-	µs
t_{STAB}	32 kHz oscillator stabilization time (after LSI32K enabled)	5 % of target frequency	-	50	-	µs
I_{LIRC}	32 kHz oscillator power consumption	The LSI oscillator is enabled. V_{DD}=1.7 to 5.5 V	-	150	250	nA
		The LSI oscillator is disabled. V_{DD}=1.7 to 5.5 V	-	2	40	

NOTE:

1. Guaranteed by design.

4.3.8 Flash Memory Characteristics

Table 23. Flash Memory Characteristics

(Temperature: -40°C to +85°C)

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
t_{PROG}	Program time	-		-	25	-	μs
t_{PER}	Page erase time	-		-	2	-	ms
t_{SER}	Sector erase time	-		-	2	-	ms
t_{MER}	Macro erase time	-		-	8	-	ms
N_{FWE}	Endurance of write/erase	Page 0 to 27	T_A=25°C, page unit	10,000	-	-	times
		Page 28 to 31		100,000	-	-	
t_{FRT}	Retention time	-		10	-	-	years

4.3.9 I/O Port Characteristics

Table 24. DC Electrical Characteristics

(Temperature: -40°C to +85°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IL1}	Input low voltage	All GPIOs	-	-	0.2 × V_{DD}	V
V_{IH1}	Input high voltage	All GPIOs	0.8 × V_{DD}	-	-	V
V_{IL2}	Input low voltage for 1.2 V	All GPIOs	-	-	0.3	V
V_{IH2}	Input high voltage for 1.2 V	All GPIOs	1.08	-	-	V
V_{OL}	Output low voltage	V_{DD}=5 V, I_{OL} = 15 mA	-	-	0.2 × V_{DD}	V
V_{OH}	Output high voltage	V_{DD}=5 V, I_{OH}=–9 mA	0.8 × V_{DD}	-	-	V
I_{OL}	Output low current	V_{DD}=3 V, V_{OL}=0.2×V_{DD}	-	10	-	mA
I_{OH}	Output high current	V_{DD}=3 V, V_{OH}=0.8×V_{DD}	-	-5	-	mA
I_{IL1}	Input low leakage current	All Input ports	-1	-	-	µA
I_{IH1}	Input high leakage current	All Input ports	-	-	1	µA
I_{IL2}	Input low leakage current for 1.2 V	All Input ports	-1	-	-	µA
I_{IH2}	Input high leakage current for 1.2 V	All Input ports	-	-	1	µA
R_{PU}	Pull-up resistor	R_{MAX}: V_{DD} = 1.7 V R_{MIN}: V_{DD} = 5 V	30	50	70	kΩ
R_{PD}	Pull-down resistor	R_{MAX}: V_{DD} = 1.7 V R_{MIN}: V_{DD} = 5 V	30	50	70	kΩ

4.3.9.1 General Input/Output Characteristics

Unless otherwise specified, the parameters in Table 25 are obtained through tests conducted under the conditions specified in Table 14. All I/Os conform to CMOS standard.

Table 25. I/O Static Characteristics

(Temperature: -40°C to +85°C)

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
V_{IL1}	I/O input low level voltage	5 V GPIO	1.7 V ≤ V_{DD} ≤ 5.5 V	-	-	0.2 × V_{DD}	V
V_{IH1}	I/O input high level voltage	5 V GPIO	1.7 V ≤ V_{DD} ≤ 5.5 V	0.8 × V_{DD}	-	-	V
V_{HYS1}(2)	Input hysteresis	5 V GPIO	1.7 V ≤ V_{DD} ≤ 5.5 V $V_{DDTYPICAL}$ = 5 V	-	1	-	V
I_{leak1}	Input leakage current(2)	5 V GPIO	1.7 ≤ V_{IN} ≤ V_{DD} × 1.1	-1	-	1	µA
V_{IL2}	I/O input low level voltage for 1.2 V	1.2 V GPIO	1.7 ≤ V_{IN} ≤ 1.8 V	-	-	0.3	V
V_{IH2}	I/O input high level voltage for 1.2 V	1.2 V GPIO	1.7 ≤ V_{IN} ≤ 1.8 V	1.08	-	-	V
V_{HYS2}(2)	Input hysteresis for 1.2 V	1.2 V GPIO	1.7 ≤ V_{IN} ≤ 1.8 V $V_{DDTYPICAL}$ = 1.8 V	-	0.3	-	V
I_{leak2}	Input leakage current for 1.2 V (2)	1.2 V GPIO	1.7 ≤ V_{IN} ≤ 1.8 V	-1	-	1	µA
R_{PU}	Weak pull-up equivalent resistor	V_{IN} = GND		30	50	70	kΩ
R_{PD}	Weak pull-down equivalent resistor	V_{IN} = V_{DD}		30	50	70	
C_{IO}	I/O pin capacitance	I/O pin capacitance		-	5	-	pF

NOTES:

1. Data based on characterization results are not tested in production.
2. Guaranteed by design.

4.3.9.2 Output Driving Current

To ensure compliance with the absolute maximum ratings specified in chapter 4.2, it is necessary to limit the number of I/O pins driving current in the user application.

- The total current sourced by all I/O pins on V_{DD} and the maximum operating current of the microcontroller on V_{DD} (during Run mode) must not exceed the absolute maximum rating ΣI_{VDD} specified in Table 12.
- The total current sunk by all I/O pins on GND and the maximum operating current of the microcontroller on GND (during Run mode) must not exceed the absolute maximum rating ΣI_{GND} specified in Table 12.

4.3.9.3 Output Voltage Levels

Unless otherwise specified, the parameters in Table 26 are obtained through tests conducted under ambient temperature and supply voltage conditions specified in Table 14.

Table 26. Output Voltage Characteristics

(Temperature: -40°C to +85°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{OL}	Output low level voltage for an I/O pin	V_{DD} = 5 V, I_{OL} = 15 mA	-	-	0.2 × V_{DD}	V
V_{OH}	Output high level voltage for an I/O pin	V_{DD} = 5 V, I_{OH} = –9 mA	0.8 × V_{DD}	-	-	

4.3.10 ADC Characteristics

Table 27. ADC Electrical Characteristics

(Temperature: -40°C to +85°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Operating voltage	-	2.4	5	5.5	V
AVREF	Analog reference voltage	-	-	-	VDD	V
V_{AN}	Analog input range	-	VSS	-	AVREF	V
-	Resolution	-	-	-	12	bit
I_{DDA}	Operating current	VDD = 5.0 V @ fMCLK = 4.5714 MHz	-	1	2	mA
ACLK	Input clock frequency		-	-	4.5714	MHz
t_{CONV}	Conversion time	@ VDD ≥ 2.4 V		-	6.56	µs
		@ VDD ≤ 2.4 V		-	14.99	
F_{CONV}	Conversion frequency	@ VDD ≥ 2.4 V	-	-	152.38	kHz
		@ VDD ≤ 2.4 V	-	-	66.67	kHz
INL	DC accuracy	-	-	±4	±8	LSB
DNL		-	-	±1	±2	
ZOE	Zero offset error	-	-	±4	±8	
FSE	Full scale error	-	-	±6	±12	

NOTE:

1. Guaranteed by design.

Table 28. Recommended ADC Resolution

V_{DD}[V]	Resolution	Condition
2.6	12-bit/Upper 12-bit	ACLK ≤ 0.5 MHz
2.5	12-bit/Upper 12-bit	
2.4	12-bit/Upper 12-bit	
2.3	12-bit/Upper 12-bit	
2.2	11-bit/Upper 11-bit	
2.1	10-bit/Upper 10-bit	
2.0	9-bit/Upper 9-bit	
1.9	8-bit/Upper 8-bit	
1.8	7-bit/Upper 7-bit	

NOTES:

1. When V_{DD} is lower than 2.2 V, the resolution will get worse.
2. If V_{DD} is less than or equal to 2.2 V, the resolution degrades by 1-bit whenever V_{DD} drops 0.1 V. (V_{DD} under 2.2 V resolution has no test.)
3. Guaranteed by design.

4.3.10.1 General PCB Design Guidelines

The power supply must be separated, as shown in Figure 9. The decoupling capacitors across the V_{DD}/AV_{DD} are ceramic (good quality) capacitors and must be placed as close as possible to the chip.

4.3.11 Communication Interfaces Characteristics

4.3.11.1 I2C Interface Characteristics

The I2C interface conforms to the timing requirements specified in the I2C-bus specification, in addition to the user timing requirements listed below:

- Standard mode (Sm): up to 100 kbps bit rate
- Fast mode (Fm): up to 400 kbps bit rate

The I2C timing requirements are guaranteed by design when the I2C peripheral is configured correctly, and the I2C clock frequency is equal to or greater than the minimum value listed in the table below.

Table 29. I2C Characteristics

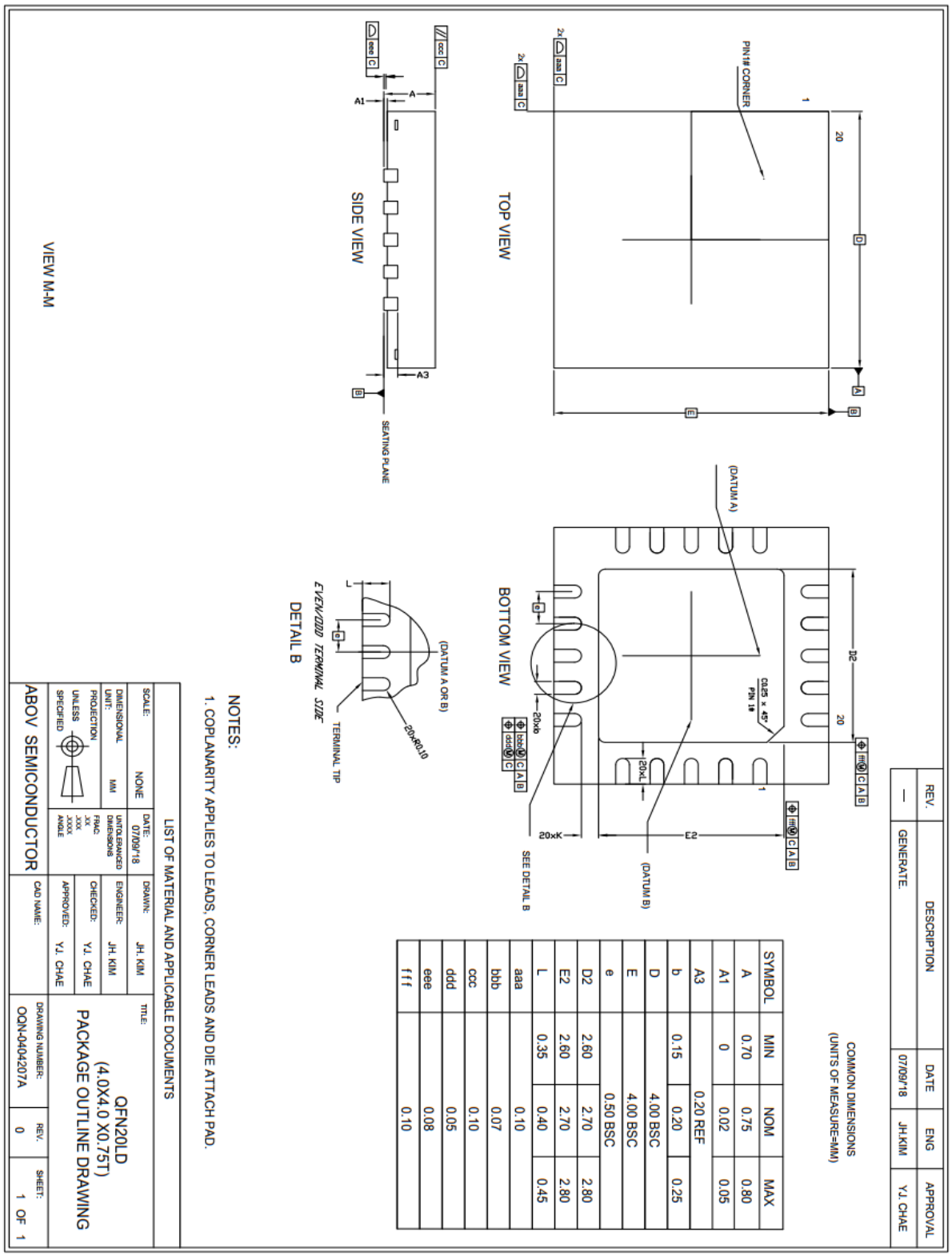
(Temperature: -40°C to +85°C)

Symbol	Parameter	Standard		Fast		Unit
		Min.	Max.	Min.	Max.	
t_{SCL}	Clock frequency	0	100	0	400	kHz
t_{SCLH}	Clock high pulse width	4.0	-	0.6	-	µs
t_{SCLL}	clock low pulse width	4.7	-	1.3	-	
t_{BF}	Bus free time	4.7	-	1.3	-	
t_{STSU}	Start condition setup time	4.7	-	0.6	-	
t_{STHD}	Start condition hold time	4.0	-	0.6	-	
t_{SPSU}	Stop condition setup time	4.0	-	0.6	-	
t_{SPHD}	Stop condition hold time	4.0	-	0.6	-	
t_{VD}	Output valid from clock	0	-	0	-	
t_{DIH}	Data input hold time	0	-	0	1.0	
t_{DIS}	Data input setup time	250	-	100	-	ns

5. Package Information

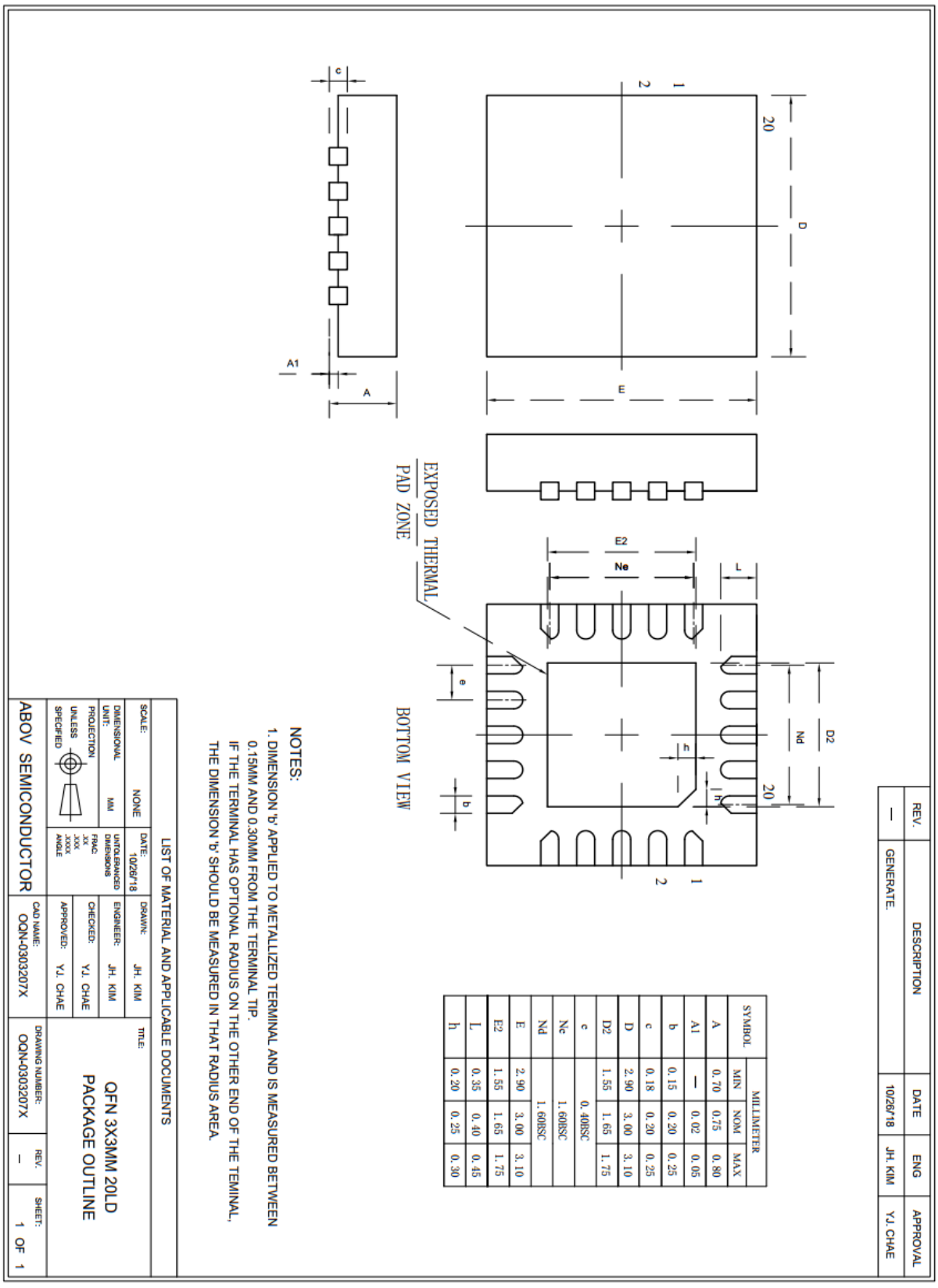
5.1 20-QFN-0404 Package Information

Figure 11. Package Dimension (20-QFN-0404)



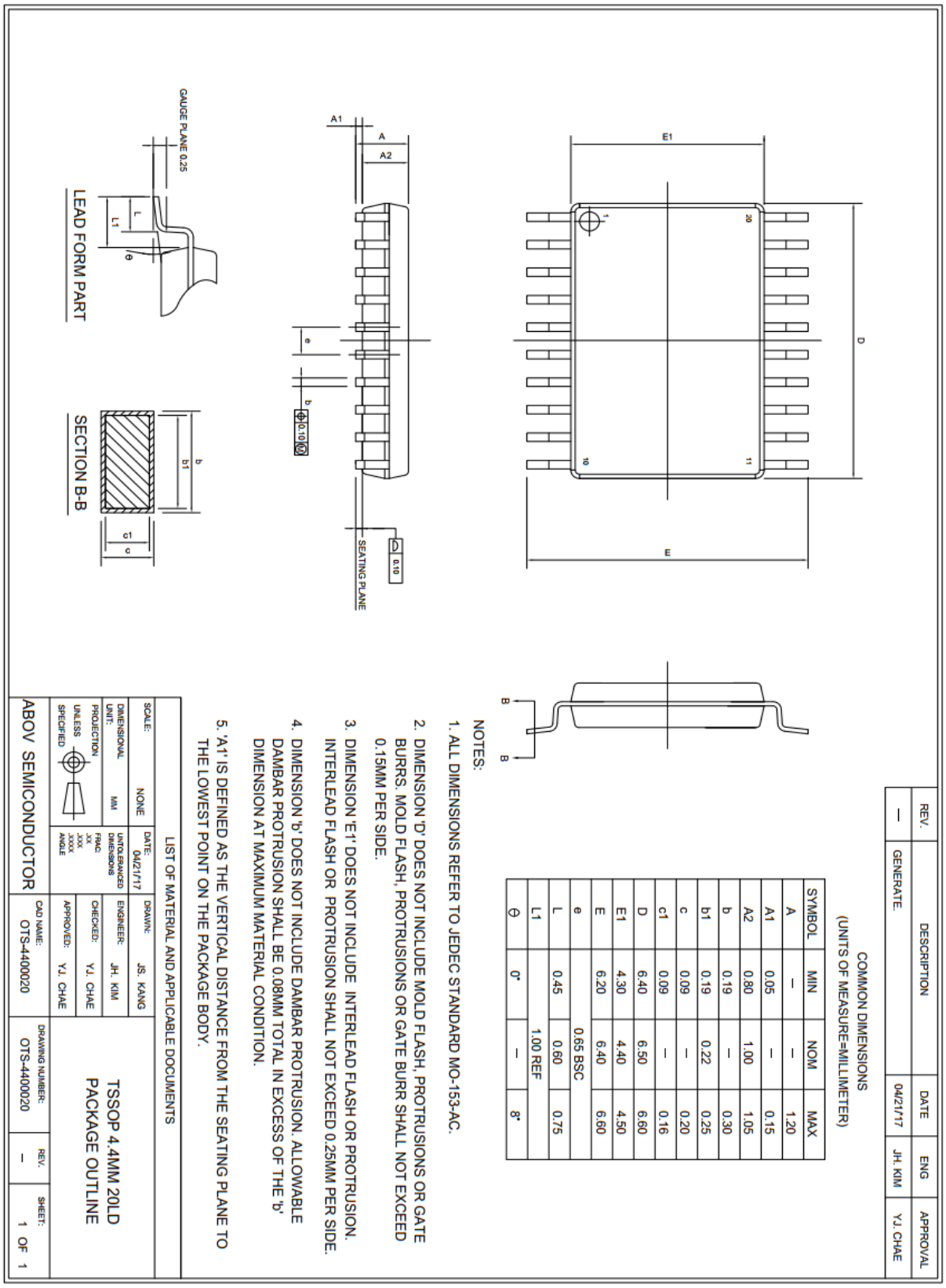
5.2 20-QFN-0303 Package Information

Figure 12. Package Dimension (20-QFN-0303)



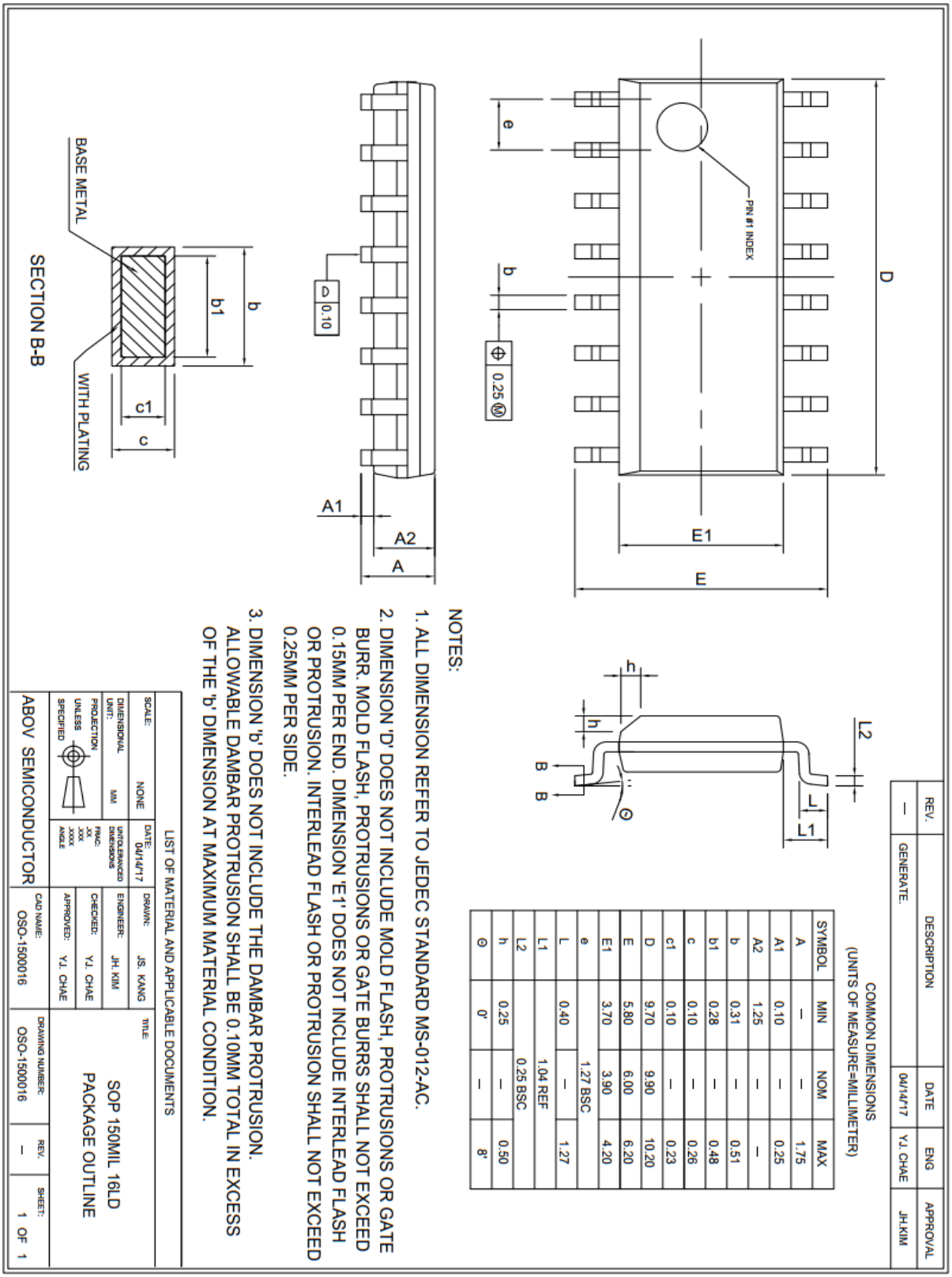
5.3 20-TSSOP Package Information

Figure 13. Package Dimension (20-TSSOP)



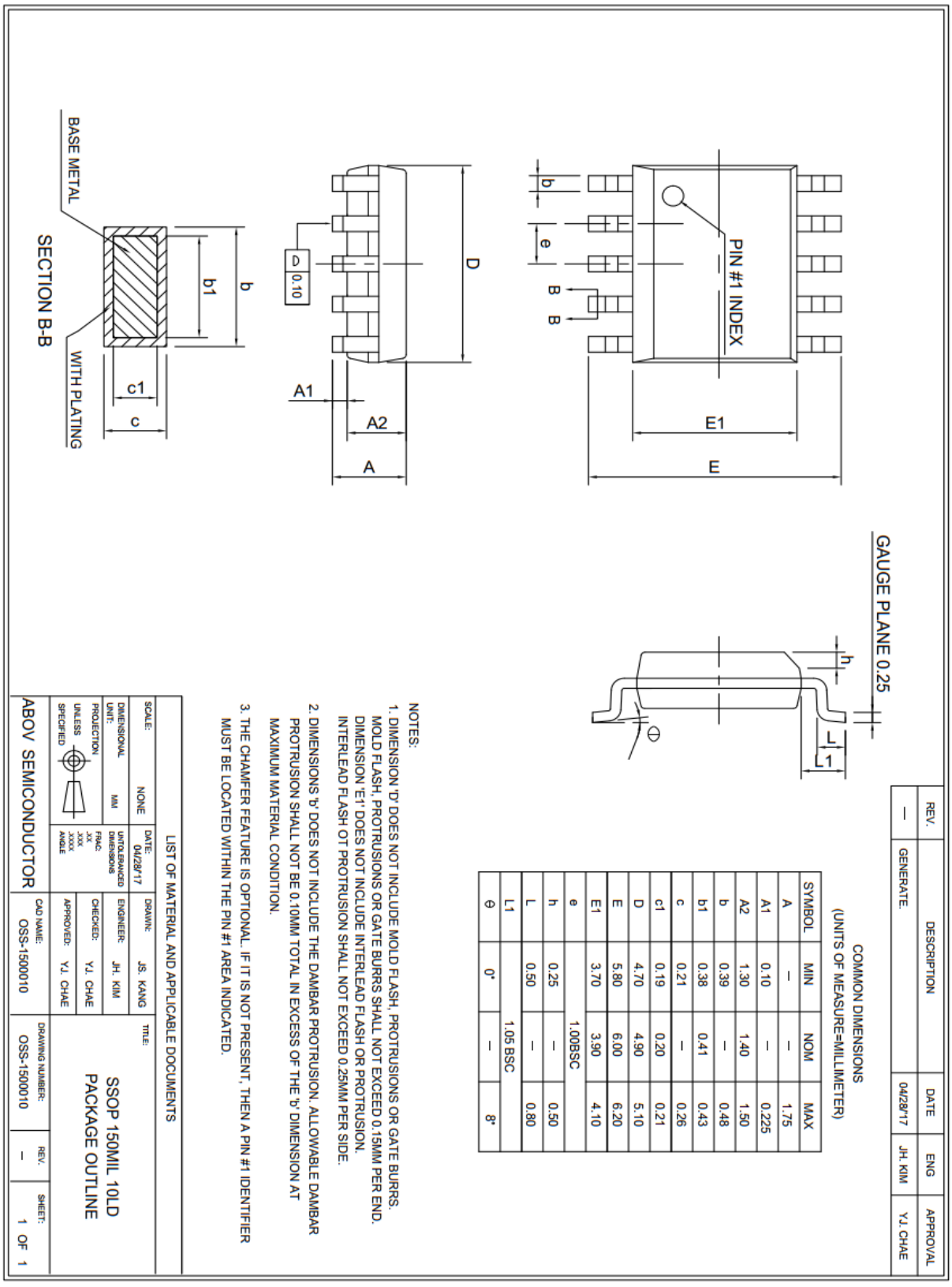
5.4 16-SOPN Package Information

Figure 14. Package Dimension (16-SOPN)



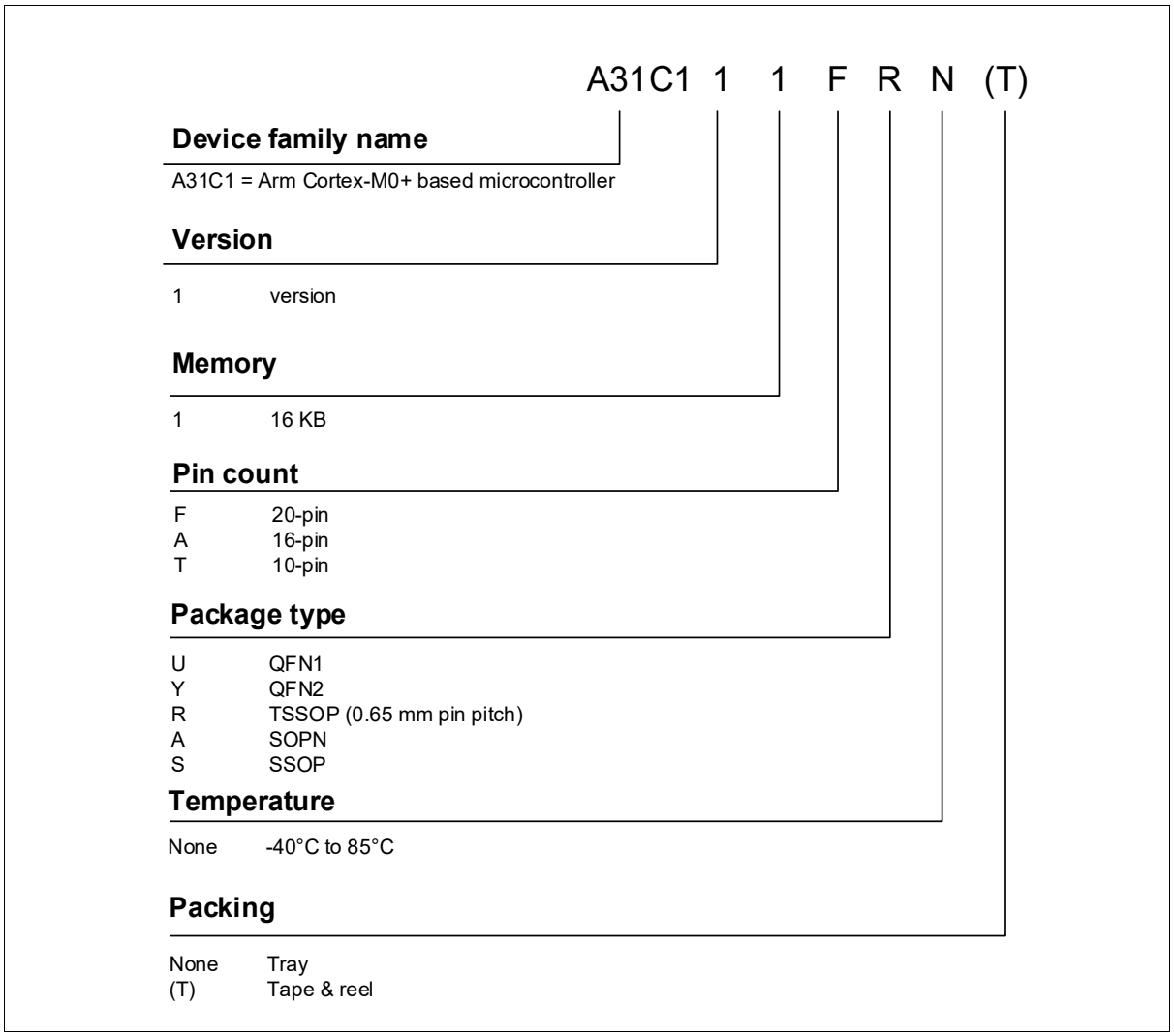
5.5 10-SSOP Package Information

Figure 15. Package Dimension (10-SSOP)



6. Ordering Information

Figure 16. A31C111 Series Device Ordering Information



NOTE:

1. For a list of available options (memory, package, etc.) or further information on any aspect of this device, contact the nearest ABOV sales office.

Revision History

Revision	Date	Notes
1.00	Jun. 19, 2026	Initial release
1.01	Aug. 6, 2026	• Modified Figure 9 • Modified Flash Endurance Cycles in Table 3 and Table 23 • Added Figure 4. A31C111FY (20-QFN-0303) Pinouts

Korea

Regional Office, Seoul
R&D, Marketing & Sales
8th Fl., 330, Yeongdong-daero, Gangnam-gu, Seoul, 06177, Korea

Tel: +82-2-2193-2200
Fax: +82-2-508-6903
www.abovsemi.com

HQ, Ochang
R&D, QA, and Test Center
37, Gangni 1-gil, Ochang-eup, Cheongwon-gun, Chungcheongbuk-do, 28126, Korea

Tel: +82-43-219-5200
Fax: +82-43-217-3534
www.abovsemi.com

Domestic Sales
Tel: +82-2-2193-2206
Fax: +82-2-508-6903
Email: sales_kr@abov.co.kr

Global Sales
Tel: +82-2-2193-2281
Fax: +82-2-508-6903
Email: sales_gl@abov.co.kr

China Sales
Tel: +86-755-8287-2205
Fax: +86-755-8287-2204
Email: sales_cn@abov.co.kr

Japan Sales
Tel: +81-6-6225-7758
Email: sales_jp@abov.co.kr

ABOV Disclaimer

IMPORTANT NOTICE – PLEASE READ CAREFULLY

ABOV Semiconductor (“ABOV”) reserves the right to make changes, corrections, enhancements, modifications, and improvements to ABOV products and/or to this document at any time without notice. **ABOV DOES NOT GIVE WARRANTIES AS TO THE ACCURACY OR COMPLETENESS OF THE INFORMATION INCLUDED HEREIN.** Purchasers should obtain the latest relevant information on ABOV products before placing orders. Purchasers are entirely responsible for the choice, selection, and use of ABOV products and ABOV assumes no liability for application assistance or the design of purchasers’ products. **NO LICENSE, EXPRESS OR IMPLIED, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY ABOV HEREIN. ABOV DISCLAIMS ALL EXPRESS AND IMPLIED WARRANTIES AND SHALL NOT BE RESPONSIBLE OR LIABLE FOR ANY INJURIES OR DAMAGES RELATED TO USE OF ABOV PRODUCTS IN SUCH UNAUTHORIZED APPLICATIONS.** ABOV and the ABOV logo are trademarks of ABOV. For additional information about ABOV trademarks, please refer to https://www.abovsemi.com/en/about/corporate_identity.php. All other products or service names are the property of their respective owners. Information in this document supersedes and replaces the information previously supplied in any former versions of this document.

© 2026 ABOV Semiconductor – All rights reserved