eMMC Specification

(XTRA VII Series, 153ball)

Version 1.3

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1. GENERAL DESCRIPTION

1.1. Introduction

FLEXXON's XTRA VII eMMC is fully comply with JEDEC eMMC5.1 Standard. It is combine of an embedded flash controller and standard NAND flash memory in one JEDEC standard package, 153Balls (11.5mm x 13mm).

FLEXXON eMMC provides high performance, good reliability and advanced power management. It is suitable for small, low power electronic devices.

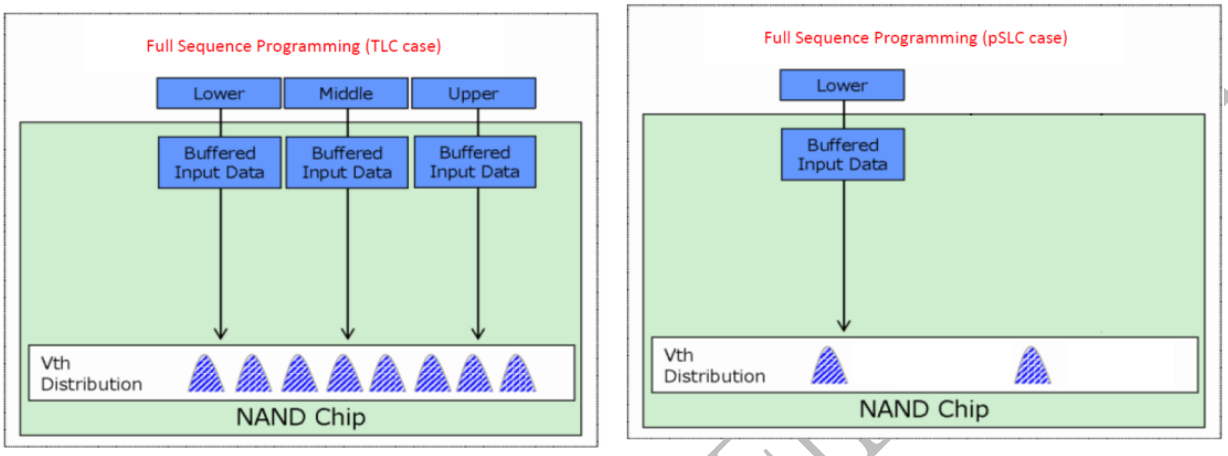
1.2. Product Overview

FLEXXON XTRA VII eMMC 5.1 includes the following features:

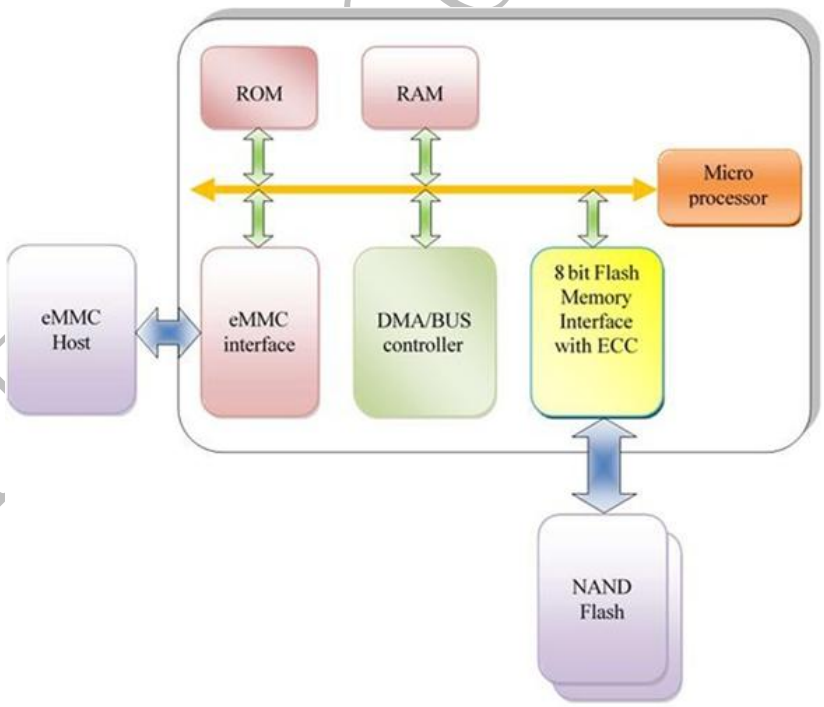
- Compliant with eMMC Specification Ver. 5.1
- Flash Type:
  - 3D pSLC: 4GB~16GB
- Package of eMMC
  - 11.5 mm x 13 mm x 1.0 mm
- Temperature Range
  - Operation (Gold Grade): -25°C ~ 85°C
  - Operation (Diamond Grade): -40°C ~ 85°C
  - Storage: -40°C ~ 85°C
- Operating Voltage
  - VCC: 3.3V
  - VCCQ: 1.8V/3.3V
- Bus Mode
  - High-speed eMMC protocol
  - Clock frequency: 0 ~ 200MHz
- Low Power Consumption
- Supports three data bus widths: 1 bit (default), 4 bits, 8 bits
- Supports High Speed Mode HS400
- Supports Production State Awareness
- Supports Field Firmware Update
- Supports Power Off Notification
- Support Enhanced Data Strobe
- Support Secure Write Protection
- RoHS compliant

1.3. 3D pSLC

3D Pseudo SLC can be considered as an extended version of 3D TLC. While 3D TLC does Full Sequence Programming into 8 Vth distribution, 3D pSLC only does Lower page programming into 2 Vth distribution. Accordingly, because only Lower pages are programmed, 3D pSLC provides better performance and endurance than 3D TLC. Moreover, 3D pSLC performs similarly with SLC, yet 3D pSLC is more cost-effective.



1.4. FUNCTION BLOCK DIAGRAM



2. PRODUCT SPECIFICATIONS

2.1. Performance

Table 2-1 eMMC Maximum Performance

Density	Sequential Read (MB/s)	Sequential Write (MB/s)
4GB	270	180
8GB	270	180
16GB	270	180

Notes:

1. 8-bit bus width; HS400 mode; Vcc = 3.3V, V_{CCQ} = 1.8V
2. Performance may differ according to flash configuration and platform.

2.2. Power Consumption

Table 2-2 eMMC Max Power Consumption

Capacity	Read (mA)		Write (mA)		Standby (mA)
	V_{CCQ}	Vcc	V_{CCQ}	Vcc	
4GB	100	46	82	44	0.15
8GB	100	50	82	47	0.15
16GB	103	50	84	47	0.15

Notes:

1. RMS current is measured at TA=25C, 8-bit bus width without clock frequency.
2. Performance of is measured at V_{CC}=3.3V, V_{CCQ}=1.8V in HS400 mode.

2.3. Partition Capacity

Table 2-4 eMMC Partition Capacity

Capacity	Boot Partition 1	Boot Partition 2	RPMB
8GB	4096 KB	4096 KB	4096 KB
16GB	4096 KB	4096 KB	4096 KB

3. INTERFACE DESCRIPTION

3.1. FLEXXON eMMC I/F Ball Array

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	
14	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	14
13	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	13
12	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	12
11	NC	NC	NC									NC	NC	NC	11
10	NC	NC	NC		NC	NC	NC	VSS	VCC	NC		NC	NC	NC	10
9	NC	NC	NC		NC					VCC		NC	NC	NC	9
8	NC	NC	NC		NC					VSS		NC	NC	NC	8
7	NC	NC	NC		VSS					NC		NC	NC	NC	7
6	VSS	DAT7	VCCQ		VCC					NC		CLK	NC	VSSQ	6
5	DAT2	DAT6	NC		NC	VCC	VSS	DS	VSS	RST_n		CMD	VSSQ	VCCQ	5
4	DAT1	DAT5	VSSQ	NC								VCCQ	VCCQ	VSSQ	4
3	DAT0	DAT4	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	VCCQ	3
2	NC	DAT3	VDDi	NC	NC	NC	NC	NC	NC	NC	NC	NC	VSSQ	NC	2
1	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	

Figure 3-1 eMMC interface in 153Balls Array (Top View)

3.2. Pins and Signal Description

Table 3-1 Function Pin Assignment, 153 balls

eMMC Interface			
Ball No.	**Ball Signal**	**Type**	**Description**
A3	DAT0	I/O/PP	Data I/O: Bidirectional channel used for data transfer
A4	DAT1		
A5	DAT2		
B2	DAT3		
B3	DAT4		
B4	DAT5		
B5	DAT6		
B6	DAT7		
M5	CMD	I/O/PP	Command: A bidirectional channel used for device initialization and command transfers.
M6	CLK	Input	Clock: Each cycle directs a 1-bit transfer on the command and DAT lines
K5	RST_n	Input	Hardware Reset
E6	VCC	Supply	Supply Voltage for Core
F5	VCC		
J10	VCC		
K9	VCC		
C6	VCCQ	Supply	Supply Voltage for I/O
M4	VCCQ		
N4	VCCQ		
P3	VCCQ		
P5	VCCQ		
A6	VSS	Supply	Supply Voltage ground for Core
E7	VSS		
G5	VSS		
H10	VSS		
J5	VSS		
K8	VSS		
C4	VSSQ	Supply	Supply Voltage ground for I/O
N2	VSSQ		
N5	VSSQ		
P4	VSSQ		
P6	VSSQ		
H5	DS	O/PP	Data strobe
C2	VDDi		Connect capacitor from VDDi to GND for stabilize internal power.

Note:

NC: No connect in eMMC. Left it floating.

4. EMMC REGISTERS

4.1. OCR Register

The 32-bit Operation Conditions Register (OCR) stores the VDD voltage profile of the Device and the access mode indication. The OCR register should be implemented by all Device.

Table 4-1 OCR Register Table

OCR slice	Description	Value	Width
[31]	Card power up status bit (busy)[1]		
[30:29]	Access mode	00b (byte mode) 10b (sector mode)	2
[28:24]	Reserved	0 0000b	5
[23:15]	2.7 – 3.6V	1 1111 1111b	9
[14:8]	2.0 – 2.6V	000 0000b	7
[7]	1.7 – 1.95V	1b	1
[6:0]	Reserved	000 0000b	7
Note [1]: This bit is set to Low if the Device has not finished the power up routine			

4.2. CID Register

The Card Identification (CID) register is 128 bits wide. It contains the Device identification information used during the Device identification phase. For details, refer to JEDEC Standard Specification No. JESD84-B52.

Table 4-2 CID Register Table

Name	Field	CID Slice	Value	Width
Manufacturer ID	MID	[127:120]	Ebh	8
Reserved	-	[119:114]	0h	6
Device/BGA	CBX	[113:112]	1h	2
OEM/ Application ID	OID	[111:104]	0Dh	8
Product Name	PNM	[103:56]	eMMC	48
Product Revision	PRV	[55:48]	10h	8
Product Serial Number	PSN	[47:16]	Random by Production	32
Manufacturing Date	MDT	[15:8]	Manufacturing date	8
CRC7 Checksum	CRC	[7:1]	CRC7	7
Not used, always “1”	-	[0:0]	1h	1

4.3. CSD Register

The Device-Specific Data (CSD) register provides information on how to access the contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, etc. For details, refer to JEDEC Standard Specification No. JESD84-B52.

Table 4-3 CSD Register Table

Name	Field	Width	Type	CSD Slice	Value
CSD structure	CSD_STRUCTURE	2	R	[127:126]	3h
System specification version	SPEC_VERS	4	R	[125:122]	4h
Reserved	-	2	R	[121:120]	0h
Data read access-time 1	TAAC	8	R	[119:112]	4Fh
Data read access-time 2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]	1h
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]	32h
Device command classes	CCC	12	R	[95:84]	8F5h
Max. read data block length	READ_BL_LEN	4	R	[83:80]	9h
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0h
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0h
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0h
DSR implemented	DSR_IMP	1	R	[76:76]	0h
Reserved	-	2	R	[75:74]	0h
Device size	C_SIZE	12	R	[73:62]	FFFh
Max. read current @ VDD min	VDD_R_CURR_MIN	3	R	[61:59]	7h
Max. read current @ VDD max	VDD_R_CURR_MAX	3	R	[58:56]	7h
Max. write current @ VDD min	VDD_W_CURR_MIN	3	R	[55:53]	7h
Max. write current @ VDD max	VDD_W_CURR_MAX	3	R	[52:50]	7h
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	7h
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	1Fh
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	1Fh
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	0Fh
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	1h
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	0h
Write speed factor	R2W_FACTOR	3	R	[28:26]	2h
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	9h
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0h
Reserved	-	4	R	[20:17]	0h
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0h
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0h
Copy flag (OTP)	COPY	1	R/W	[14:14]	0h

Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0h
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0h
File format	FILE_FORMAT	2	R/W	[11:10]	0h
ECC code	ECC	2	R/W/E	[9:8]	0h
CRC	CRC	7	R/W/E	[7:1]	2Eh
Not used, always '1'	-	1	-	[0:0]	1h

4.4. Extended CSD Register

The Extended CSD register defines the Device properties and selected modes. It is 512 byes long. The most significant 320 bytes are the Properties segment, which defines the Device capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the Device is working in. These modes can be changed by the host by means of the SWITCH command. For details, refer to JEDEC Standard Specification No. JESD84-B52.

4.5. RCA Register

The writable 16-bit Relative Device Address (RCA) register carries the Device address assigned by the host during the Device identification. This address is used for the addressed host-Device communication after the Device identification procedure. The default value of the RCA register is 0x0001. The value 0x0000 is reserved to set all Devices into the *Stand-by State* with CMD7.

4.6. DSR Register

The 16-bit driver stage register (DSR) is described in detail in JEDEC Standard Specification, JESD84-B52 Section 7.6. It can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of Devices). The CSD register carries the information about the DSR register usage. The default value of the DSR register is 0x404.

5. ELECTRICAL CHARACTERISTICS

5.1. Power Supply

Table 5-1 eMMC power supply

Parameter	Symbol	Min	Max	Unit
Supply voltage (NAND)	Vcc	2.7	3.6	V
Supply voltage (I/O)	V_{CCQ}	2.7	3.6	V
		1.7	1.95	V
Supply Power-Up for 1.8V	tPRUL		25	ms
Supply Power-Up for 3.3V	tPRUH		35	ms

5.2. Bus Signal Levels

Figure 5-1 Bus Signal Levels

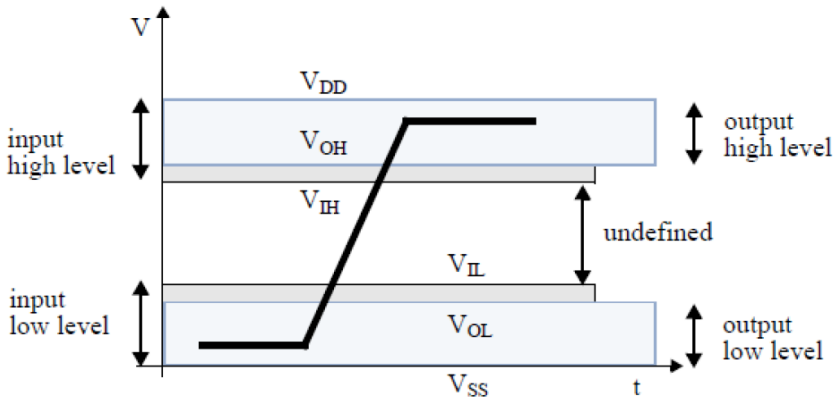


Table 5-2 Bus Signals Levels

Parameter	Symbol	Min	Max	Unit	Remark
Open-Drain Bus Signal Level					
Output High Voltage	V_{OH}	VDD – 0.2	-	V	I_{OH} = -100 uA
Output Low Voltage	V_{OL}	-	0.3	V	I_{OL} = 2 mA
Push-pull bus signal level (2.7V~3.6V)					
Output High Voltage	V_{OH}	0.75 * VCCQ	-	V	I_{OH} = -100 uA @ V_{CCQ} min
Output Low Voltage	V_{OL}	-	0.125 * VCCQ	V	I_{OL} = 100 uA @ V_{CCQ} min
Input High Voltage	V_{IH}	0.625 * VCCQ	VCCQ + 0.3	V	
Input Low Voltage	V_{IL}	VSS – 0.3	0.25 * VCCQ	V	
Push-pull bus signal level (1.7V~1.95V)					
Output High Voltage	V_{OH}	VCCQ – 0.45V	-	V	I_{OH} = -2 mA
Output Low Voltage	V_{OL}	-	0.45V	V	I_{OL} = 2 mA
Input High Voltage	V_{IH}	0.65 * VCCQ	VCCQ + 0.3	V	
Input Low Voltage	V_{IL}	V_{SS} – 0.3	0.35 * V_{DD}	V	

5.3. Bus Timing (High-Speed Mode)

Figure 5-2 Timing diagram data input/output referenced to clock (High Speed Mode)

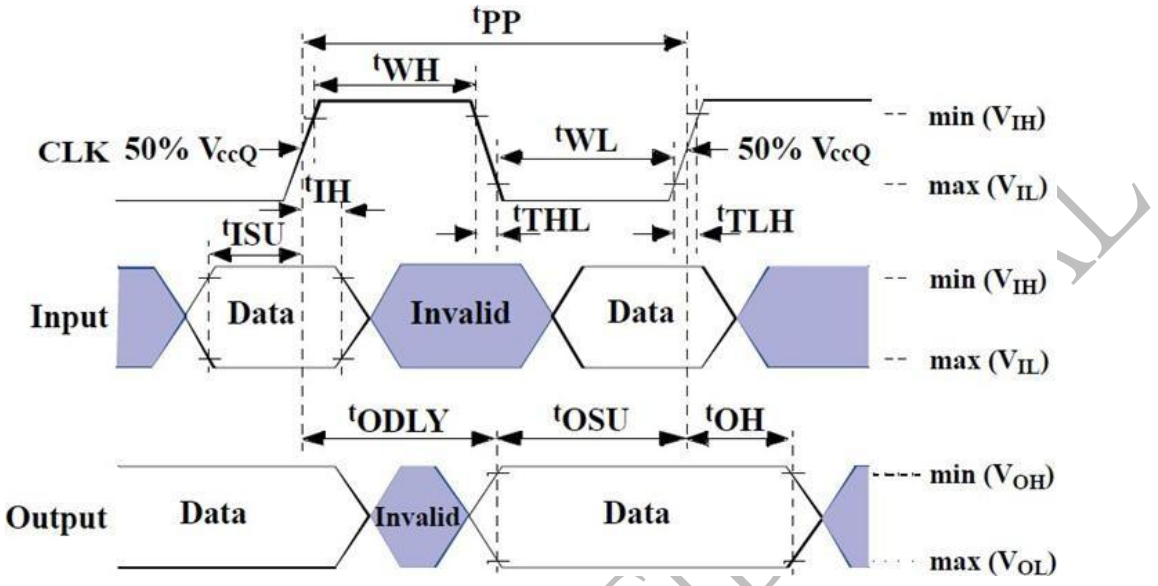


Table 5-3: backward-compatible device mode timing (High Speed)

Parameter	Symbol	Min.	Max.	Unit	Remark
Input MMC_CLK					
Clock frequency data transfer mode	f_{PP}	0	26	MHz	$C_L \leqq$ 30pF
Clock frequency identification mode	f_{OD}	0	400	KHz	
Clock low time / Clock high time	t_{WL}/t_{WH}	10	-	ns	$C_L \leqq$ 30pF
Clock rise time / Clock fall time	t_{TLH}/t_{THL}	-	10	ns	$C_L \leqq$ 30pF
Input MMC_CMD/ MMC_DATA, reference to MMC_CLK					
Input set-up time	t_{ISU}	3	-	ns	$C_L \leqq$ 30pF
Input hold time	t_{IH}	3	-	ns	$C_L \leqq$ 30pF
Output MMC_CMD/ MMC_DATA, reference to MMC_CLK					
Output set-up time	t_{OSU}	11.7	-	ns	$C_L \leqq$ 30pF
Output hold time	t_{OH}	8.3	-	ns	$C_L \leqq$ 30pF

(1) Clock timing is measured at 50% of VCCQ.
(2) Clock rise and fall times are measured by min (VIH) and max (VIL).

Table 5-3-1: Bus Timing Parameters Values (High Speed)

Parameter	Symbol	Min.	Max.	Unit	Remark
Input MMC_CLK					
Clock frequency data transfer mode	f_{PP}	0	52	MHz	$C_L \leq 30pF$
Clock frequency identification mode	f_{OD}	0	400	KHz	
Clock low time / Clock high time	t_{WL}/t_{WH}	6.5	-	ns	$C_L \leq 30pF$
Clock rise time / Clock fall time	t_{TLH}/t_{THL}	-	3	ns	$C_L \leq 30pF$
Input MMC_CMD, MMC_DAT (referenced to MMC_CLK)					
Input set-up time	t_{ISU}	3	-	ns	$C_L \leq 30pF$
Input hold time	t_{IH}	3	-	ns	$C_L \leq 30pF$
Output MMC_CMD, MMC_DAT (referenced to MMC_CLK)					
Output delay time during data transfer	t_{ODLY}	-	13.7	ns	$C_L \leq 30pF$
Output hold time	t_{OH}	2.5	-	ns	$C_L \leq 30pF$

(1) Clock timing is measured at 50% of VCCQ.
(2) Clock rise and fall times are measured by min (VIH) and max (VIL).
(3) Inputs CMD, DAT rise and fall times are measured by min (VIH) and max (VIL), and outputs CMD, DAT rise and fall times are measured by min (VOH) and max (VOL).

5.4. Bus Timing (DDR Mode)

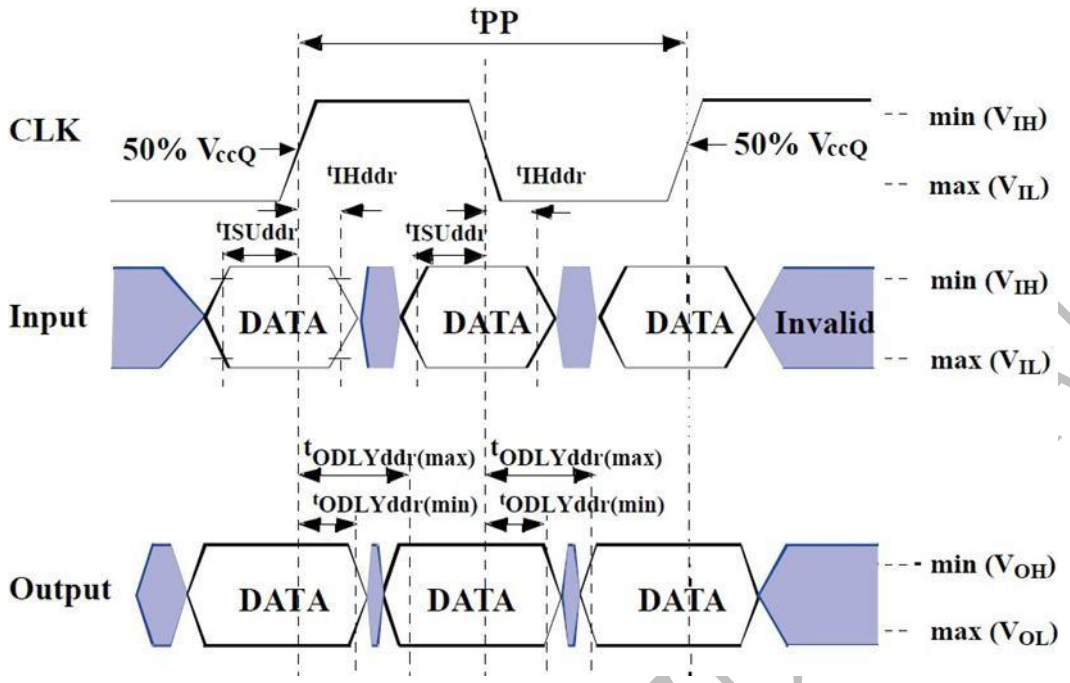


Figure 5-4 Timing diagram data input/output referenced to clock (DDR Mode)

Table 5-4: Bus Timing – Parameters Values (DDR)

Parameter	Symbol	Min.	Max.	Unit	Remark
Input MMC_CLK					
Clock duty cycle	-	45	55	%	
Clock rise time / Clock fall time	t_{TLH}/t_{THL}	-	3	ns	$C_L \leq 30pF$
Input MMC_CMD (referenced to MMC_CLK)					
Input set-up time	t_{ISUddr}	3	-	ns	$C_L \leq 20pF$
Input hold time	t_{IHddr}	3	-	ns	$C_L \leq 20pF$
Output MMC_CMD (referenced to MMC_CLK)					
Output delay time during data transfer	t_{ODLY}	-	13.7	ns	$C_L \leq 20pF$
Output hold time	t_{OH}	2.5	-	ns	$C_L \leq 20pF$
Signal rise time	t_{RISE}	-	3	ns	$C_L \leq 20pF$
Signal fall time	t_{FALL}	-	3	ns	$C_L \leq 20pF$
Input MMC_DAT (referenced to MMC_CLK)					
Input set-up time	t_{ISUddr}	2.5	-	ns	$C_L \leq 20pF$
Input hold time	t_{IHddr}	2.5	-	ns	$C_L \leq 20pF$
Output MMC_DAT (referenced to MMC_CLK)					
Output delay time during data transfer	$t_{ODLYddr}$	1.5	7	ns	$C_L \leq 20pF$
Signal rise time	t_{RISE}	-	2	ns	$C_L \leq 20pF$
Signal fall time	t_{FALL}	-	2	ns	$C_L \leq 20pF$

(1) Clock timing is measured at 50% of VCCQ.

(2) Inputs DAT rise and fall times are measured by min (VIH) and max (VIL), and outputs DAT rise and fall times are measured by min (VOH) and max (VOL).

5.5. Bus Timing (HS200 mode)

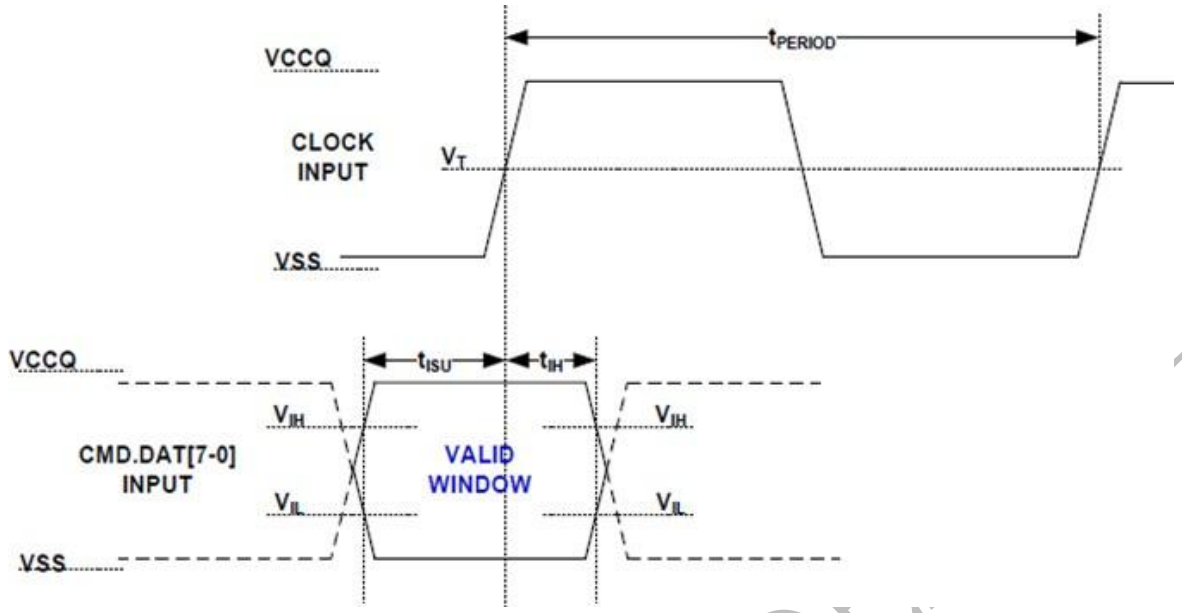


Figure 5-5: Timing diagram data input referenced to clock (HS200 Mode)

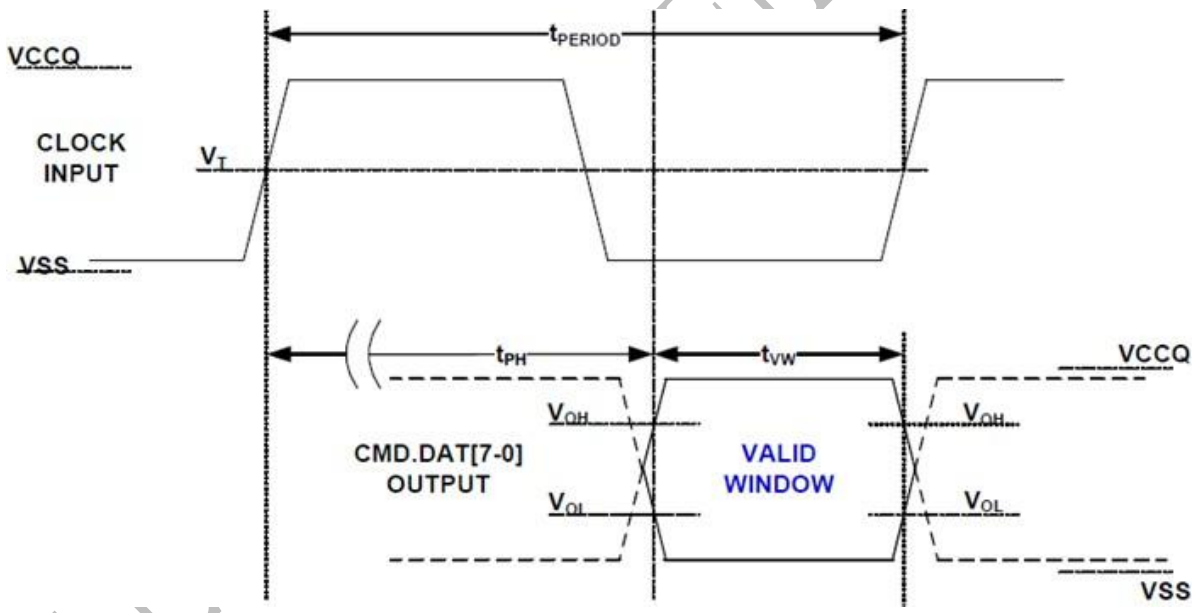


Figure 5-5.1: Timing diagram data output referenced to clock (HS200 Mode)

Table 5-5: Bus Timing – Parameters Values (HS200 mode)

Parameter	Symbol	Min.	Max.	Unit	Remark
Input MMC_CLK					
Clock cycle time	t_{PERIOD}	5	-	ns	
Clock rise time / Clock fall time	t_{TLH}/t_{THL}	-	1	ns	C_{Device} = 6 pF
Clock duty cycle	-	30	70	%	
Input MMC_CMD, MMC_DAT (referenced to MMC_CLK)					
Input set-up time	t_{ISU}	1.4	-	ns	C_{Device} ≤ 6pF
Input hold time	t_{IH}	0.8	-	ns	C_{Device} ≤ 6pF
Output MMC_CMD, MMC_DAT (referenced to MMC_CLK)					
Output delay time during data transfer	t_{PH}	0	2	UI	
Delay variation due to temperature change after tuning	Δ_{TPH}	-350 (ΔT=-20°C)	+1550 (ΔT=90°C)	ps	
Output valid data window	t_{VW}	0.575	-	UI	

(1) Unit Interval (UI) is one bit nominal time. For example, UI = 5ns at 200MHz.

5.6. Bus Timing (HS200 mode)

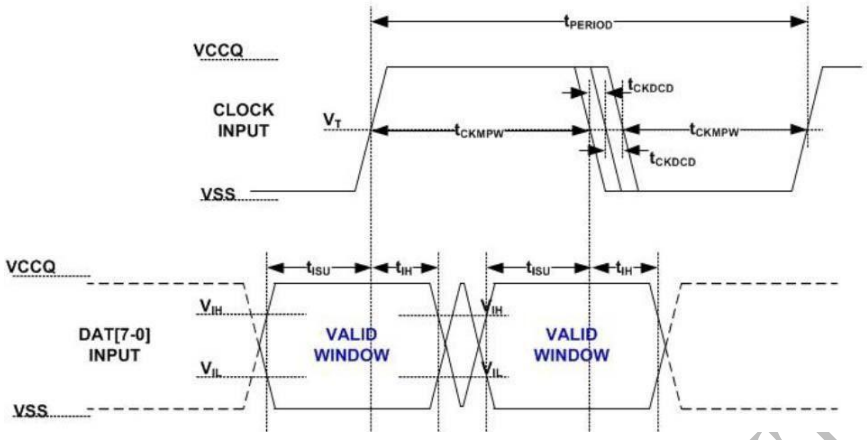


Figure 5.6: Timing diagram data input referenced to clock (HS400 mode)

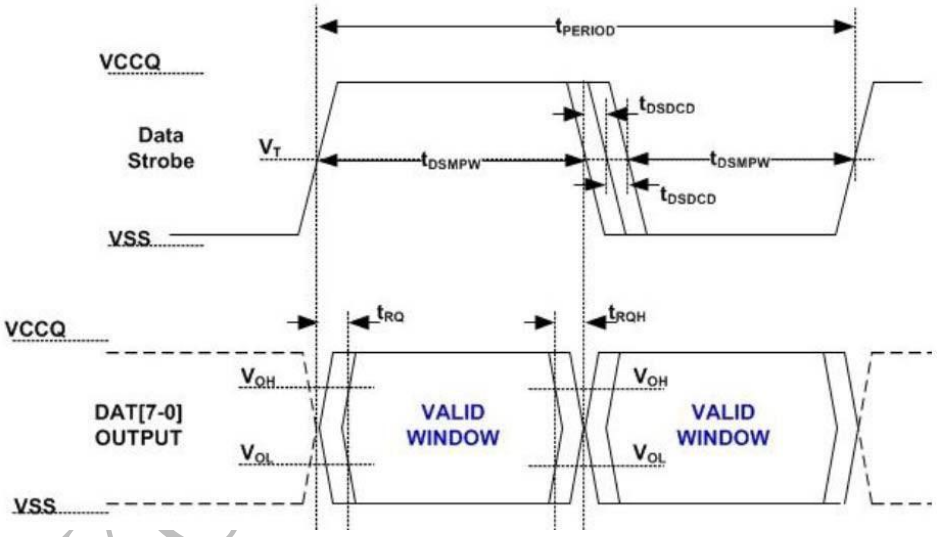


Figure5.6.1: Timing diagram data output referenced to clock (HS400 mode)

Table 5-6: Bus Timing – Parameters Values (HS400 mode)

Parameter	Symbol	Min.	Max.	Unit	Remark
Input MMC_CLK					
Clock cycle time	t_{PERIOD}	5	-	ns	
Slew rate	SR	1.125	-	V/ns	
Duty cycle distortion	t_{CKDCD}	0	0.3	ns	
Minimum pulse width	t_{CKMPW}	2.2	-	ns	
Input MMC_DAT (referenced to MMC_CLK)					
Input set-up time	t_{ISUddr}	0.4	-	ns	$C_{Device} \leq 6pF$
Input hold time	t_{IHddr}	0.4	-	ns	$C_{Device} \leq 6pF$
Slew rate	SR	1.125	-	V/ns	
Output MMC_STRB					
Clock cycle time	t_{PERIOD}	5	-	ns	
Slew rate	SR	1.125	-	V/ns	
Duty cycle distortion	t_{CKDCD}	0	0.2	ns	
Minimum pulse width	t_{CKMPW}	2	-	ns	
Read pre-amble	t_{RPRE}	0.4	-	t_{PERIOD}	
Read post-amble	t_{RPST}	0.4	-	t_{PERIOD}	
Output MMC_ DAT/ MMC_ CMD (referenced to MMC_STRB)					
Output skew	t_{RQ}/t_{RQ_CMD}	-	0.4	ns	
Output hold skew	t_{RQH}/t_{RQH_CMD}	-	0.4	ns	
Slew rate	SR	1.125	-	V/ns	

5.7. FLASH INTERFACE AC CHARACTERISTIC

Table 5-7: Flash Interface AC Characteristic

Parameter	Symbol	Min.	Max.	Unit	Remark
CLE/ALE setup time	t_{CLS}/t_{ALS}	15	-	ns	
CLE/ALE hold time	t_{CLH}/t_{ALH}	5	-	ns	
WE low pulse width	t_{WP}	11	-	ns	
WE high pulse width	t_{WH}	11	-	ns	
RE low pulse width	t_{RP}	2.25	-	ns	
RE high pulse width	t_{REH}	2.25	-	ns	
Read cycle time	t_{RC}	5	-	ns	
Write cycle time	t_{WC}	25	-	ns	
Data setup time	t_{DS}	0.28	-	ns	
Data hold time	t_{DH}	0.28	-	ns	

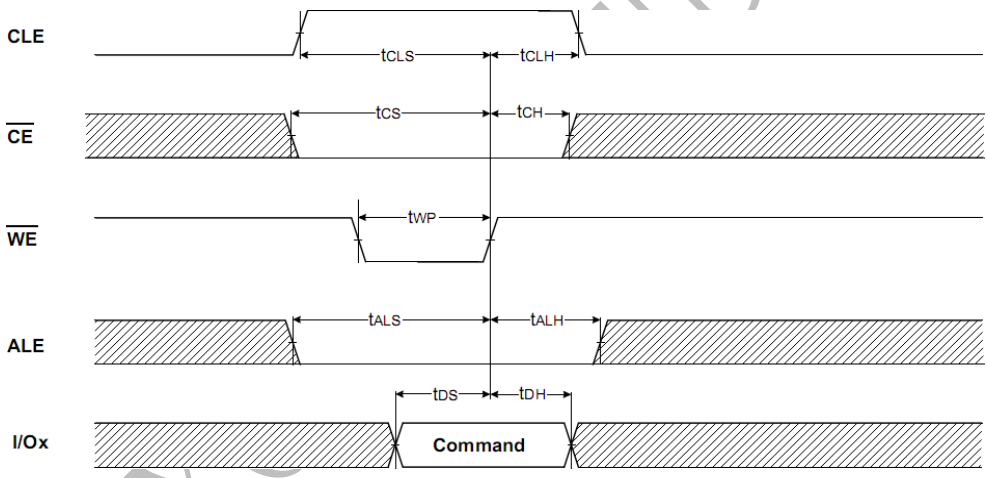


Figure 5-7.1: Command Latch Cycle

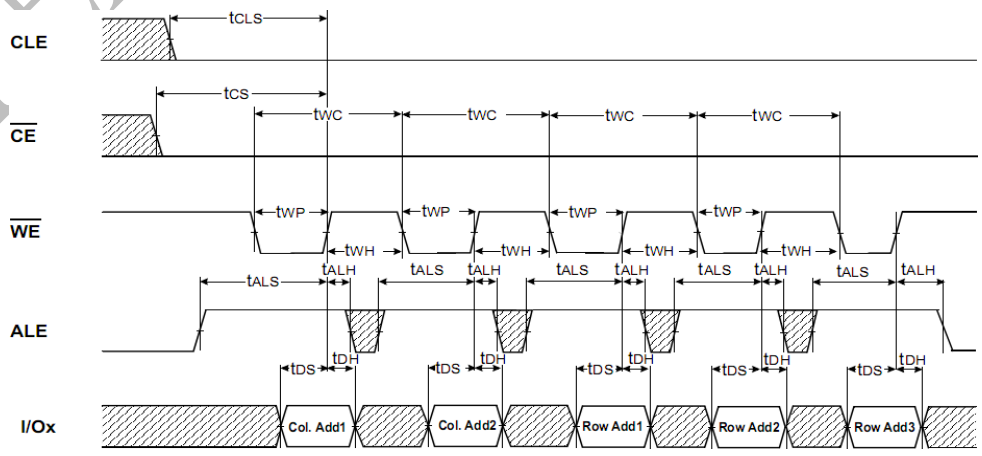


Figure 5-7.2: Address Latch Cycle

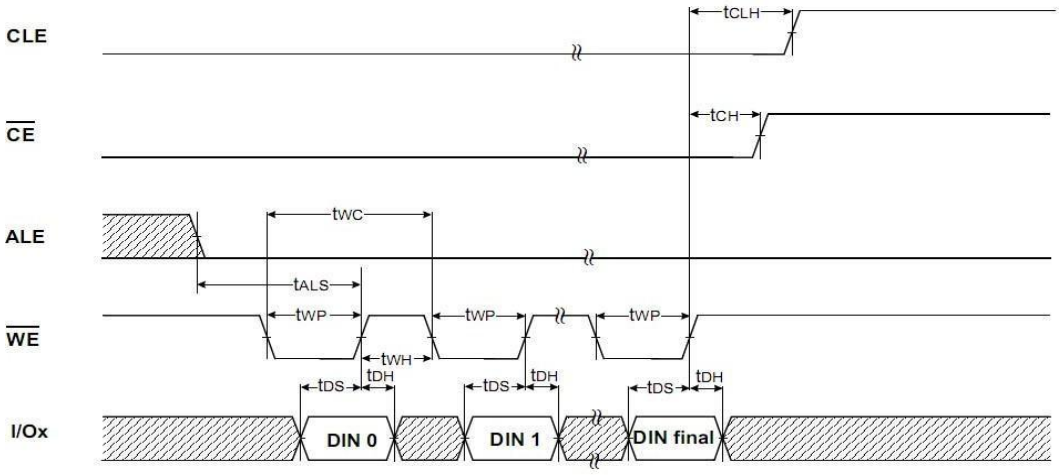


Figure 5-7.3: Input Data Latch Cycle

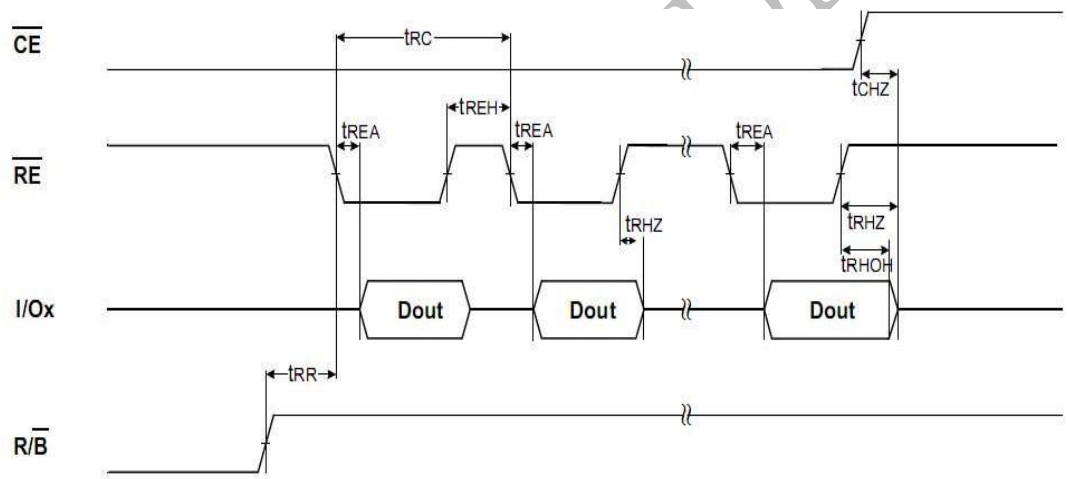
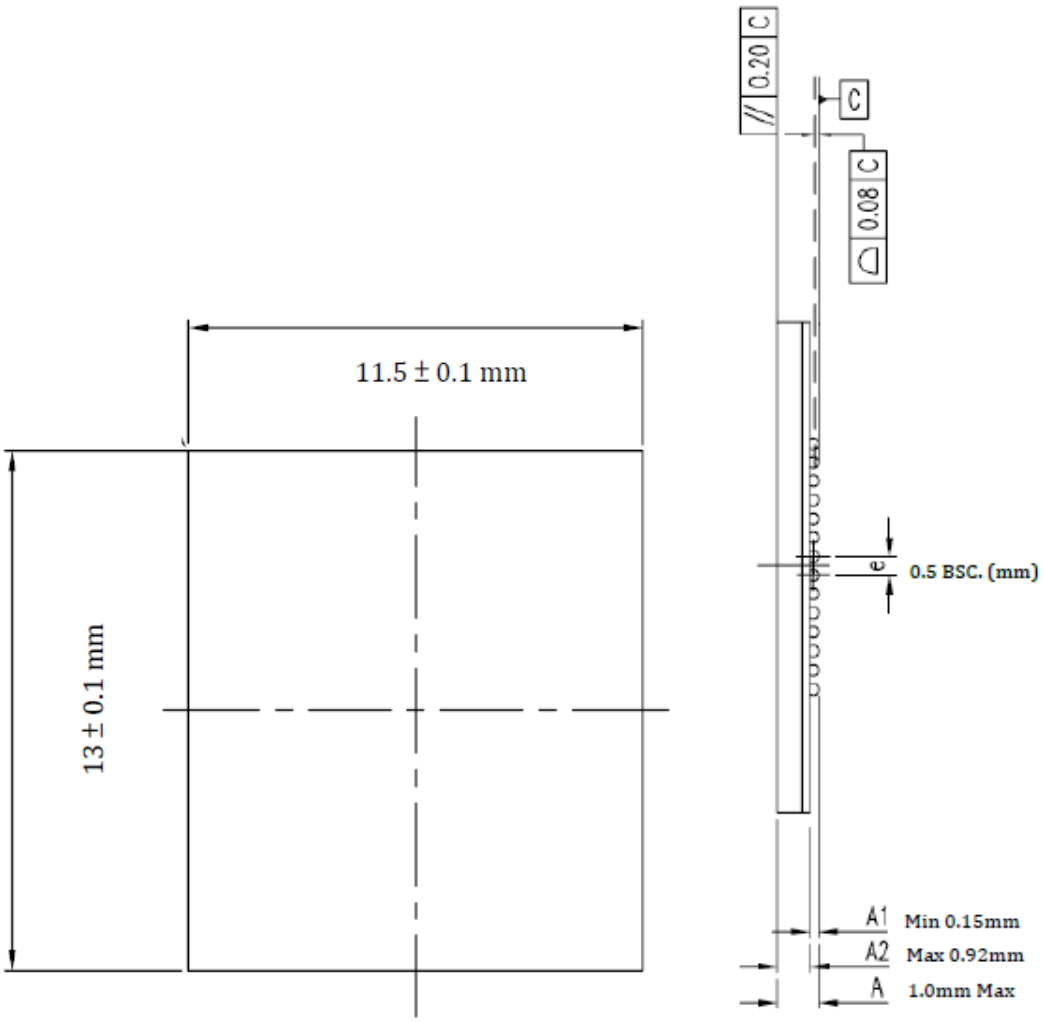
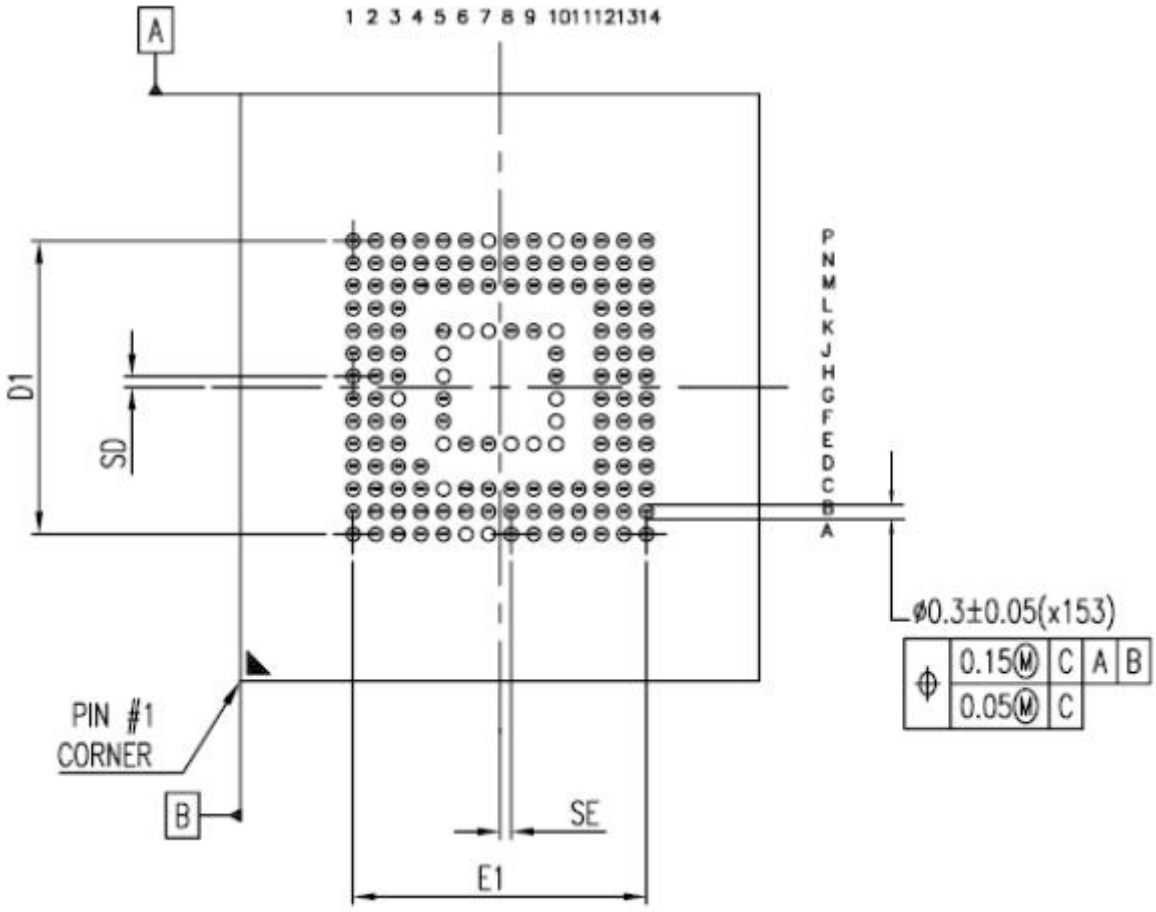


Figure 5-7.4: Sequential Out Cycle after Read (CLE=L,/WE=H,ALE=L)

6. PACKAGE

Package Size: 11.5 x 13.0 x 1.0mm





Bottom View:

N	SE (MM)	SD (MM)	E1 (MM)	D1 (MM)	JEDEC (REF)
153	0.25 BSC.	0.25 BSC.	6.50 BSC.	6.50 BSC.	MO-276 BA

7. ORDERING INFORMATION

Capacity	MPN (Gold Grade)	MPN (Diamond Grade)	Power System	Pin Configuration	Package Size
4GB	FEMC004GCG-3A40	FEMC004GCE-3A40	VCCQ: 1.8V/3.3V VCC: 3.3V	153 FBGA	11.5x13x1.0 (mm)
8GB	FEMC008GCG-3A40	FEMC008GCE-3A40			
16GB	FEMC016GCG-3A40	FEMC016GCE-3A40			

Revision History

Revision	Release Date	History
1.0	2022/01	First release
1.1	2023/01	Add ECSD
1.2	2024/06	Update Bus timing
1.3	2025/12	Update Ordering Information