Industrial eMMC 5.1 Specification

(AXO Series, 3D pSLC, 100ball)

V1.1

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1. GENERAL DESCRIPTION

1.1. Introduction

FLEXXON's AXO eMMC is fully comply with JEDEC eMMC5.1 Standard. It is combined of an embedded flash controller and standard NAND flash memory in one JEDEC standard package, 100Balls (14.0mm x 18.0mm). FLEXXON eMMC provides high performance, good reliability and advanced power management. It is suitable for small, low power electronic devices.

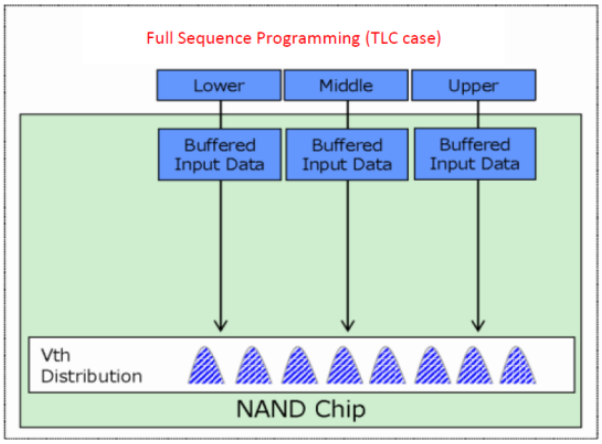
1.2. Product Overview

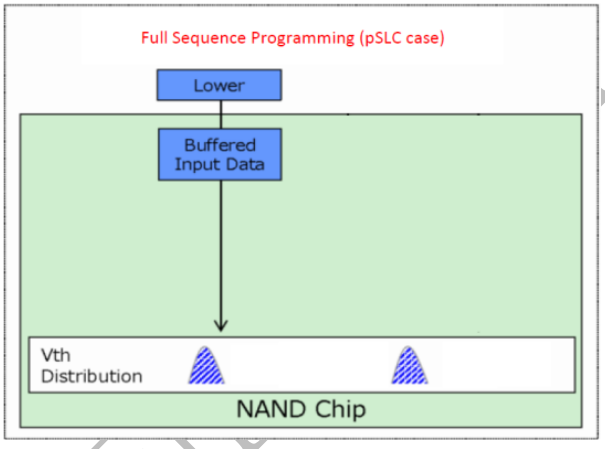
FLEXXON AXO eMMC 5.1 includes the following features:

- Compliant with eMMC Specification Ver. 5.1
- Flash Type:
  - 3D pSLC: 16GB~128GB
- Package of eMMC
  - 14.0 mm x 18.0 mm x 1.4 mm
- Temperature Range
  - Operation & Storage (Gold Grade): -25°C ~ 85°C
  - Operation & Storage (Diamond Grade): -40°C ~ 85°C
  - Operation & Storage (Automotive Grade 3): -40°C ~ 85°C
  - Operation & Storage (Automotive Grade 2): -40°C ~ 105°C
- Operating Voltage
  - VCC: 3.3V
  - VCCQ: 1.8V/3.3V
- Bus Mode
  - High-speed eMMC protocol
  - Clock frequency: 0 ~ 200MHz
- Supports three data bus widths: 1 bit (default), 4 bits, 8 bits
- Supports High Speed Mode HS400
- Supports Production State Awareness
- Supports Field Firmware Update
- RoHS compliant

1.3. 3D pSLC

3D Pseudo SLC can be considered as an extended version of 3D TLC. While 3D TLC does Full Sequence Programming into 8 Vth distribution, 3D pSLC only does Lower page programming into 2 Vth distribution. Accordingly, because only Lower pages are programmed, 3D pSLC provides better performance and endurance than 3D TLC. Moreover, 3D pSLC performs similarly with SLC, yet 3D pSLC is more cost-effective.





2. PRODUCT SPECIFICATIONS

2.1. Performance

Table 2-1 eMMC Performance

Density	Sequential Read (MB/s)	Sequential Write (MB/s)
16GB	280	120
32GB	300	200
64GB	300	200
128GB	300	200

Notes:

1. 8-bit bus width; HS400 mode; Vcc = 3.3V, V_{CCQ} = 1.8V
2. Performance may differ according to flash configuration and platform.

2.2. Power Consumption

Table 2-2 eMMC Power Consumption

Capacity	Read (mA)		Write (mA)		Standby (mA)
	V_{CCQ}	Vcc	V_{CCQ}	Vcc	
16GB	110	90	95	90	0.5
32GB	175	110	100	115	0.5
64GB	175	115	110	115	0.5
128GB	175	115	110	115	0.5

Notes:

1. 8-bit bus width; clock frequency of 200MHz DDR mode; Vcc = 3.3V, V_{CCQ} = 1.8V
2. Standby current is measured at Vcc = 3.3V, 8-bit bus width without clock frequency.

3. INTERFACE DESCRIPTION

3.1. FLEXXON eMMC I/F Ball Array

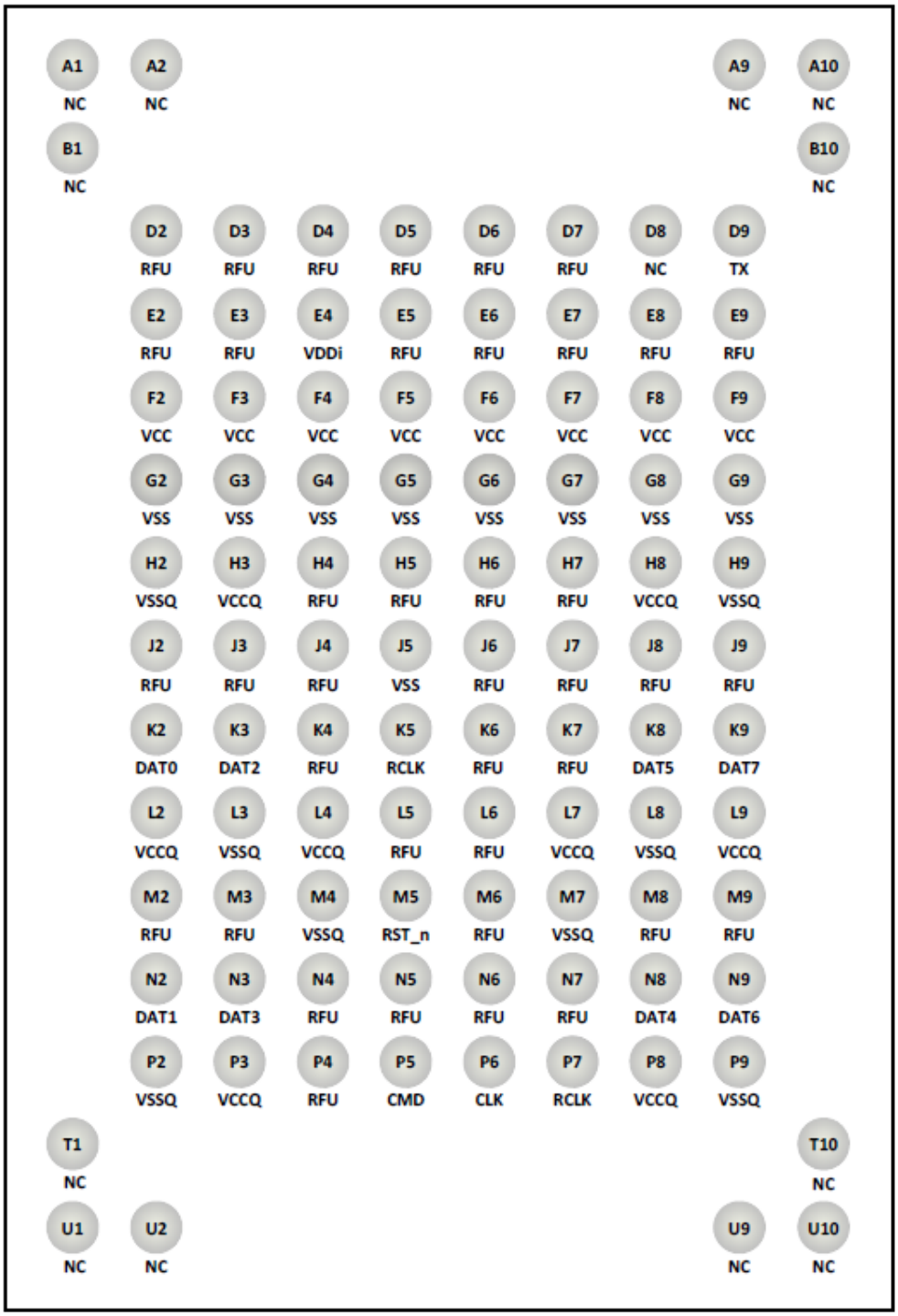


Figure 3-1 eMMC interface in 100Balls Array (Top View)

3.2. Pins and Signal Description

Table 3-1 Function Pin Assignment, 100 balls

eMMC Interface			
Ball No.	**Ball Signal**	**Type**	**Description**
K2	DAT0	I/O/PP	Data I/O: Bidirectional channel used for data transfer
N2	DAT1		
K3	DAT2		
N3	DAT3		
N8	DAT4		
K8	DAT5		
N9	DAT6		
K9	DAT7		
P5	CMD	I/O/PP	Command: A bidirectional channel used for device initialization and command transfers.
P6	CLK	Input	Clock: Each cycle directs a 1-bit transfer on the command and DAT lines
M5	RST_n	Input	Hardware Reset
F2 – F9	VCC	Supply	Supply Voltage for Core
H3, H8, L2, L4, L7, L9, P3, P8	VCCQ	Supply	Supply Voltage for I/O
G2 – G9, J5	VSS	Supply	Ground connection for Core
H2, H9, L3, L8, M4, M7, P2, P9	VSSQ	Supply	Ground connection for I/O
K5	RCLK	O/PP	Data strobe (HS400 Mode)
P7			
E4	VDDi		Internal Voltage Node A 1.0uF capacitor is required for VDDi for core power stabilization. Do not tie to supply voltage or ground.
D9	TX	Output	UART Tx Output for debug use

Note:

NC: No connect in eMMC. Left it floating.

4. EMMC REGISTERS

4.1. OCR Register

The 32-bit Operation Conditions Register (OCR) stores the VDD voltage profile of the Device and the access mode indication. The OCR register should be implemented by all Device.

Table 4-1 OCR Register Table

OCR slice	Description	Value	Width
[31]	Card power up status bit (busy)[1]		
[30:29]	Access mode	00b (byte mode) 10b (sector mode)	2
[28:24]	Reserved	0 0000b	5
[23:15]	2.7 – 3.6V	1 1111 1111b	9
[14:8]	2.0 – 2.6V	000 0000b	7
[7]	1.7 – 1.95V	1b	1
[6:0]	Reserved	000 0000b	7
Note [1]: This bit is set to Low if the Device has not finished the power up routine			

4.2. CID Register

The Card Identification (CID) register is 128 bits wide. It contains the Device identification information used during the Device identification phase. For details, refer to JEDEC Standard Specification No. JESD84-B51.

Table 4-2 CID Register Table

Name	Field	CID Slice	Value	Width
Manufacturer ID	MID	[127:120]	89h	8
Reserved	-	[119:114]	-	6
Device/BGA	CBX	[113:112]	1h	2
OEM/ Application ID	OID	[111:104]	51h	8
Product Name	PNM	[103:56]	eMMC	48
Product Revision	PRV	[55:48]	-	8
Product Serial Number	PSN	[47:16]	Random by Production	32
Manufacturing Date	MDT	[15:8]	Month, Year	8
CRC7 Checksum	CRC	[7:1]	-	7
Not used, always “1”	-	[0:0]	1h	1

4.3. CSD Register

The Device-Specific Data (CSD) register provides information on how to access the contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, etc. For details, refer to JEDEC Standard Specification No. JESD84-B51.

Table 4-3 CSD Register Table

Name	Field	Width	Type	CSD Slice	Value
CSD structure	CSD_STRUCTURE	2	R	[127:126]	3h
System specification version	SPEC_VERS	4	R	[125:122]	4h
Reserved	-	2	R	[121:120]	0h
Data read access-time 1	TAAC	8	R	[119:112]	27h
Data read access-time 2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]	1h
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]	32h
Device command classes	CCC	12	R	[95:84]	0F5h
Max. read data block length	READ_BL_LEN	4	R	[83:80]	9h
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0h
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0h
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0h
DSR implemented	DSR_IMP	1	R	[76:76]	0h
Reserved	-	2	R	[75:74]	0h
Device size	C_SIZE	12	R	[73:62]	FFFh
Max. read current @ VDD min	VDD_R_CURR_MIN	3	R	[61:59]	7h
Max. read current @ VDD max	VDD_R_CURR_MAX	3	R	[58:56]	7h
Max. write current @ VDD min	VDD_W_CURR_MIN	3	R	[55:53]	7h
Max. write current @ VDD max	VDD_W_CURR_MAX	3	R	[52:50]	7h
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	7h
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	1Fh
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	1Fh
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	64GB:0Fh 128~512GB: 1Fh
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	1h
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	0h
Write speed factor	R2W_FACTOR	3	R	[28:26]	2h
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	9h
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0h
Reserved	-	4	R	[20:17]	0h
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0h
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0h
Copy flag (OTP)	COPY	1	R/W	[14:14]	1h
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0h
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0h
File format	FILE_FORMAT	2	R/W	[11:10]	0h
ECC code	ECC	2	R/W/E	[9:8]	0h

CRC	CRC	7	R/W/E	[7:1]	-
Not used, always '1'	-	1	-	[0:0]	1h

4.4. Extended CSD Register

The Extended CSD register defines the Device properties and selected modes. It is 512 byes long. The most significant 320 bytes are the Properties segment, which defines the Device capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the Device is working in. These modes can be changed by the host by means of the SWITCH command. For details, refer to JEDEC Standard Specification No. JESD84-B51.

Name	Field	Size (Byte	CSD-slice	Value
Properties Segment				
Reserved1	–	6	[511:506]	-
Extended Security Commands Error	EXT_SECURITY_ERR	1	[505]	0h
Supported Command Sets	S_CMD_SET	1	[504]	1h
HPI features	HPI_FEATURES	1	[503]	1h
Background operations support	BKOPS_SUPPORT	1	[502]	1h
Max packed read commands	MAX_PACKED_READS	1	[501]	20h
Max packed write commands	MAX_PACKED_WRITES	1	[500]	20h
Data Tag Support	DATA_TAG_SUPPORT	1	[499]	1h
Tag Unit Size	TAG_UNIT_SIZE	1	[498]	0h
Tag Resources Size	TAG_RES_SIZE	1	[497]	0h
Context management capabilities	CONTEXT_CAPABILITIES	1	[496]	78h
Large Unit size	LARGE_UNIT_SIZE_M1	1	[495]	1h
Extended partitions attribute support	EXT_SUPPORT	1	[494]	3h
Supported modes	SUPPPORTED_MODES	1	[493]	1h
FFU Features	FFU_FEATURES	1	[492]	0h
Operation code timeout	OPERATION_CODE_TIMEOUT	1	[491]	17h
FFU Argument	FFU_ARG	1	[490:487]	FFFAFFF0h
Barrier support	BARRIER_SUPPORT	1	[486]	1h
Reserved		177	[485:309]	-
CMD Queuing Support	CMDQ_SUPPORT	1	[308]	1h
CMD Queuing Dept	CMDQ_DEPTH	1	[307]	1Fh
Reserved		1	[306]	
Number of FW sectors correctly programmed	NUMBER_OF_FW_SECTOR	4	[305:302]	0000h
Vendor proprietary health report	VENDOR_PROPRIETARY_H EALTH_REPORT	32	[301:270]	-

Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B	1	[269]	01h
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A	1	[268]	01h
Pre EOL information	PRE_EOL_INFO	1	[267]	01h
Optimal read size	OPTIMAL_READ_SIZE	1	[266]	40h
Optimal write size	OPTIMAL_WRITE_SIZE	1	[265]	40h
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SI	1	[264]	07h
Device version	DEVICE_VERSION	2	[263:262]	See Note
Firmware version	FIRMWARE_VERSION	8	[261:254]	See Note
Power class for 200MHz, DDR at	PWR_CL_DDR_200_360	1	[253]	0h
Cache size	CACHE_SIZE	4	[252:249]	0400h
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	[248]	5h
Power off notification(long) timeout	POWER_OFF_LONG_TIME	1	[247]	64h
Background operations status	BKOPS_STATUS	1	[246]	0h
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	[245:242]	0h
1st initialization time after partitioning	INI_TIMEOUT_AP	1	[241]	0Ah
Cache Flushing Policy	CACHE_FLUSH_POLICY	1	[240]	1h
Power class for 52MHz, DDR at 3.6V	PWR_CL_DDR_52_360	1	[239]	0h
Power class for 52MHz, DDR at 1.95V	PWR_CL_DDR_52_195	1	[238]	0h
Power class for 200MHz at 3.6V	PWR_CL_200_360	1	[237]	0h
Power class for 200MHz, at 1.95V	PWR_CL_200_195	1	[236]	0h
Minimum Write Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	[235]	0h
Minimum Read Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	[234]	0h
Reserved1	–	1	[233]	–
TRIM Multiplier	TRIM_MULT	1	[232]	02h
Secure Feature support	SEC_FEATURE_SUPPORT	1	[231]	55h
Secure Erase Multiplier	SEC_ERASE_MULT	1	[230]	512GB: 0x64 256GB: 0x64 128GB: 0x64 64GB: 0x32
Secure TRIM Multiplier	SEC_TRIM_MULT	1	[229]	0Ah
Boot information	BOOT_INFO	1	[228]	7h
Reserved1	–	1	[227]	–
Boot partition size	BOOT_SIZE_MULTI	1	[226]	FCh
Access size	ACC_SIZE	1	[225]	6h

High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	[224]	1h
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	[223]	2h
Reliable write sector count	REL_WR_SEC_C	1	[222]	10h
High-capacity write protect group size	HC_WP_GRP_SIZE	1	[221]	512GB: 20h 256GB: 20h 128GB: 20h 64GB: 10h
Sleep current (VCC)	S_C_VCC	1	[220]	7h
Sleep current (VCCQ)	S_C_VCCQ	1	[219]	7h
Production state awareness timeout	PRODUCTION_STATE_AWA RENESS_TIMEOUT	1	[218]	17h
Sleep/awake timeout	S_A_TIMEOUT	1	[217]	12h
Sleep Notification Timeout	SLEEP_NOTIFICATION_TIME	1	[216]	0Ch
Sector Count	SEC_COUNT	4	[215:212]	512GB: 3A400000h 256GB: 1D200000h 128GB: E900000h 64GB: 7340000h
Secure Write Protect Information	SECURE_WP_INFO	1	[211]	1h
Minimum Write Performance for 8bit	MIN_PERF_W_8_52	1	[210]	0h
Minimum Read Performance for 8bit at 52MHz	MIN_PERF_R_8_52	1	[209]	0h
Minimum Write Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	1	[208]	0h
Minimum Read Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	1	[207]	0h
Minimum Write Performance for 4bit at 26MHz	MIN_PERF_W_4_26	1	[206]	0h
Minimum Read Performance for 4bit at 26MHz	MIN_PERF_R_4_26	1	[205]	0h
Reserved1	–	1	[204]	–
Power class for 26MHz at 3.6V 1 R	PWR_CL_26_360	1	[203]	0h
Power class for 52MHz at 3.6V 1 R	PWR_CL_52_360	1	[202]	0h
Power class for 26MHz at 1.95V 1 R	PWR_CL_26_195	1	[201]	0h
Power class for 52MHz at 1.95V 1 R	PWR_CL_52_195	1	[200]	0h
Partition switching timing	PARTITION_SWITCH_TIME	1	[199]	4h
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	[198]	Ah

I/O Driver Strength	DRIVER_STRENGTH	1	[197]	1Fh
Device type	CARD_TYPE	1	[196]	57h
Reserved (note1)	–	1	[195]	–
CSD structure version			[194]	2h
Reserved (note1)	–	1	[193]	–
Extended CSD revision	EXT_CSD_REV	1	[192]	8h
Modes Segment				
Command set	CMD_SET	1	[191]	0h
Reserved (note1)	–	1	[190]	–
Command set revision	CMD_SET_REV	1	[189]	0h
Reserved (note1)	–	1	[188]	–
Power class	POWER_CLASS	1	[187]	0h
Reserved (note1)	–	1	[186]	–
High-speed interface timing	HS_TIMING	1	[185]	0h
Strobe Support	STROBE_SUPPORT	1	[184]	1h
Bus width mode	BUS_WIDTH	1	[183]	0h
Reserved (note1)	–	1	[182]	–
Erased memory content	ERASED_MEM_CONT	1	[181]	0h
Reserved (note1)	–	1	[180]	–
Partition configuration	PARTITION_CONFIG	1	[179]	0h
Boot config protection	BOOT_CONFIG_PROT	1	[178]	0h
Boot bus Conditions	BOOT_BUS_CONDITIONS	1	[177]	0h
Reserved (note1)	–	1	[176]	–
High-density erase group definition	ERASE_GROUP_DEF	1	[175]	0h
Boot write protection status registers	BOOT_WP_STATUS	1	[174]	0h
Boot area write protection register	BOOT_WP	1	[173]	0h
Reserved (note1)	–	1	[172]	–
User area write protection register	USER_WP	1	[171]	0h
Reserved (note1)	–	1	[170]	–
FW configuration	FW_CONFIG	1	[169]	0h
RPMB Size	RPMB_SIZE_MULT	1	[168]	20h
Write reliability setting register	WR_REL_SET	1	[167]	1Fh
Write reliability parameter register	WR_REL_PARAM	1	[166]	15h
Start Sanitize operation	SANITIZE_START	1	[165]	0h
Manually start background operations	BKOPS_START	1	[164]	0h
Enable background operations	BKOPS_EN	1	[163]	0h
H/W reset function	RST_n_FUNCTION	1	[162]	0h
HPI management	HPI_MGMT	1	[161]	0h
Partitioning Support	PARTITIONING_SUPPORT	1	[160]	7h
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	[159:157]	512GB: 26D5h 256GB: 136Ah 128GB: 9B5h 64GB: 99Ah

Partitions attribute	PARTITIONS_ATTRIBUTE	1	[156]	0h
Partitioning Setting	PARTITION_SETTING_	1	[155]	0h
General Purpose Partition Size	GP_SIZE_MULT 4	3	[154:152]	0h
General Purpose Partition Size	GP_SIZE_MULT3	3	[151:149]	0h
General Purpose Partition Size	GP_SIZE_MULT2	3	[148:146]	0h
General Purpose Partition Size	GP_SIZE_MULT1	3	[145:143]	0h
Enhanced User Data Area Size	ENH_SIZE_MULT	3	[142:140]	0h
Enhanced User Data Start Address	ENH_START_ADDR	4	[139:136]	0h
Reserved (note1)	–	1	[135]	–
Bad Block Management mode	SEC_BAD_BLK_MGMNT	1	[134]	0h
Production state awareness	PRODUCTION_STATE_AW A RENESS	1	[133]	0h
Package Case Temperature is	TCASE_SUPPORT	1	[132]	0h
Periodic Wake-up	PERIODIC_WAKEUP	1	[131]	0h
Program CID/CSD in DDR mode	PROGRAM_CID_CSD_DD	1	[130]	1h
Reserved (note1)	–	2	[129:128]	–
Vendor Specific Fields	VENDOR_SPECIFIC_FIELD	64	[127:64]	–
Native sector size	NATIVE_SECTOR_SIZE	1	[63]	1h
Sector size emulation	USE_NATIVE_SECTOR	1	[62]	0h
Sector size	DATA_SECTOR_SIZE	1	[61]	0h
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	[60]	0Ah
Class 6 commands control	CLASS_6_CTRL	1	[59]	0h
Number of addressed group to be	DYNCAP_NEEDED	1	[58]	0h
Exception events control	EXCEPTION_EVENTS_CTR	2	[57:56]	00h
Exception events status	EXCEPTION_EVENTS_STA	2	[55:54]	00h
Extended Partitions Attribute	EXT_PARTITIONS_ATTRIB	2	[53:52]	00h
Context configuration	CONTEXT_CONF	15	[51:37]	0h
Packed command status	PACKED_COMMAND_STA TUS	1	[36]	0h
Packed command failure index	PACKED_FAILURE_INDEX	1	[35]	0h
Power Off Notification	POWER_OFF_NOTIFICATI ON	1	[34]	0h
Control to turn the Cache ON/OFF	CACHE_CTRL	1	[33]	0h
Flushing of the cache	FLUSH_CACHE	1	[32]	0h
Mode operation codes	MODE_OPERATION_CO DE	1	[29]	0h
Reserved	-	2	[28:27]	-

FFU status	FFU_STATUS	1	[26]	0h
Pre loading data size	PRE_LOADING_DATA_SIZ	4	[25:22]	0h
Max pre loading data size	MAX_PRE_LOADING_DATA_SIZE	4	[21:18]	512GB: 136A8000h 256GB: 9B50000h 128GB: 4DA8000h 64GB: 2668000h
Product state awareness enablement	PRODUCT_STATE_AWARE NESS_ENABLEMENT	1	[17]	01h
Secure Removal Type	SECURE_REMOVAL_TYPE	1	[16]	3Bh
Command Queue Mode Enable	CMDQ_MODE_EN	1	[15]	0h
Reserved	-	15	[14:0]	-
Note1：Reserved bits should read as “0.” Note: * Changed by Firmware release note				

4.5. RCA Register

The writable 16-bit Relative Device Address (RCA) register carries the Device address assigned by the host during the Device identification. This address is used for the addressed host-Device communication after the Device identification procedure. The default value of the RCA register is 0x0001. The value 0x0000 is reserved to set all Devices into the *Stand-by State* with CMD7.

4.6. DSR Register

The 16-bit driver stage register (DSR) is described in detail in JEDEC Standard Specification, JESD84-B51 Section 7.6. It can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of Devices). The CSD register carries the information about the DSR register usage. The default value of the DSR register is 0x404.

5. ELECTRICAL CHARACTERISTICS

5.1. Power Supply

Table 5-1 eMMC power supply

Parameter	Symbol	Min	Max	Unit
Supply voltage (NAND)	Vcc	2.7	3.6	V
Supply voltage (I/O)	V_{CCQ}	2.7	3.6	V
		1.7	1.95	V
Supply Power-Up for 1.8V	tPRUL		25	ms
Supply Power-Up for 3.3V	tPRUH		35	Ms

5.2. Bus Signal Levels

Figure 5-1 Bus Signal Levels

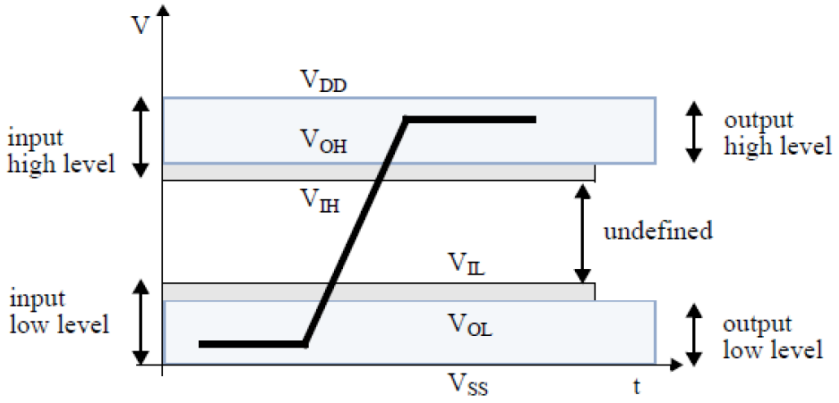
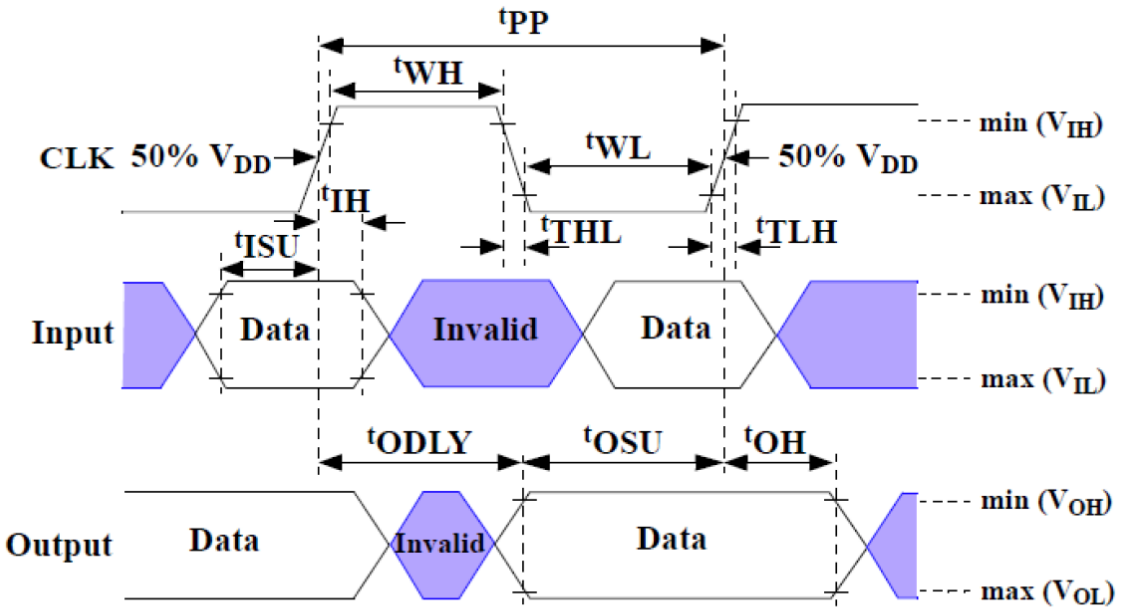


Table 5-2 Bus Signals Levels

Parameter	Symbol	Min	Max	Unit	Remark
Open-Drain Bus Signal Level					
Output High Voltage	V_{OH}	VDD – 0.2	-	V	I_{OH} = -100 uA
Output Low Voltage	V_{OL}	-	0.3	V	I_{OL} = 2 mA
Push-pull bus signal level (2.7V~3.6V)					
Output High Voltage	V_{OH}	0.75 * VCCQ	-	V	I_{OH} = -100 uA @ V_{CCQ} min
Output Low Voltage	V_{OL}	-	0.125 * VCCQ	V	I_{OL} = 100 uA @ V_{CCQ} min
Input High Voltage	V_{IH}	0.625 * VCCQ	VCCQ + 0.3	V	
Input Low Voltage	V_{IL}	VSS – 0.3	0.25 * VCCQ	V	
Push-pull bus signal level (1.7V~1.95V)					
Output High Voltage	V_{OH}	VCCQ – 0.45V	-	V	I_{OH} = -2 mA
Output Low Voltage	V_{OL}	-	0.45V	V	I_{OL} = 2 mA
Input High Voltage	V_{IH}	0.65 * VCCQ	VCCQ + 0.3	V	
Input Low Voltage	V_{IL}	V_{SS} – 0.3	0.35 * V_{DD}	V	

5.3. Bus Timing

Figure 5-2 Bus Timing in Single Data Rate Mode



Data must always be sampled on the rising edge of the clock.

Table 5-3 High Speed Device Interface Timing

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK[1]					
Clock Frequency Data Transfer Mode (PP)[2]	f_{PP}	0	52[3]	MHz	CL ≤30 pF Tolerance:+ 100 KHz
Clock Frequency Identification Mode (OD)	f_{OD}	0	400	kHz	Tolerance: +20 KHz
Clock high time	t_{WH}	6.5	-	ns	CL ≤30 pF
Clock low time	t_{WL}	6.5	-	ns	CL ≤30 pF
Clock rise time[4]	t_{TLH}	-	3	ns	CL ≤30 pF
Clock fall time	t_{THL}	-	3	ns	CL ≤30 pF
Inputs /Outputs CMD, DAT (Referenced to CLK)					
Input set-up time	t_{ISU}	3	-	ns	CL ≤30 pF
Input hold time	t_{IH}	3	-	ns	CL ≤30 pF
Output delay time during data transfer	t_{ODLY}	-	13.7	ns	CL ≤30 pF
Output hold time	t_{OH}	2.5	-	ns	CL ≤30 pF
Signal rise time[5]	t_{RISE}	-	3	ns	CL ≤30 pF
Note [1]: CLK timing is measured at 50% of VDD. Note [2]: eMMC shall support the full frequency range from 0-26Mhz, or 0-52MHz Note [3]: Device can operate as high-speed Device interface timing at 26 MHz clock frequency. Note [4]: CLK rise and fall times are measured by min (VIH) and max (VIL). Note [5]: Inputs CMD, DAT rise and fall times are measured by min (VIH) and max (VIL), and output CMD, DAT rise and fall times are measured by min (VOH) and max (VOL).					

Figure 5-3 Bus Timing in Dual Data Rate Mode

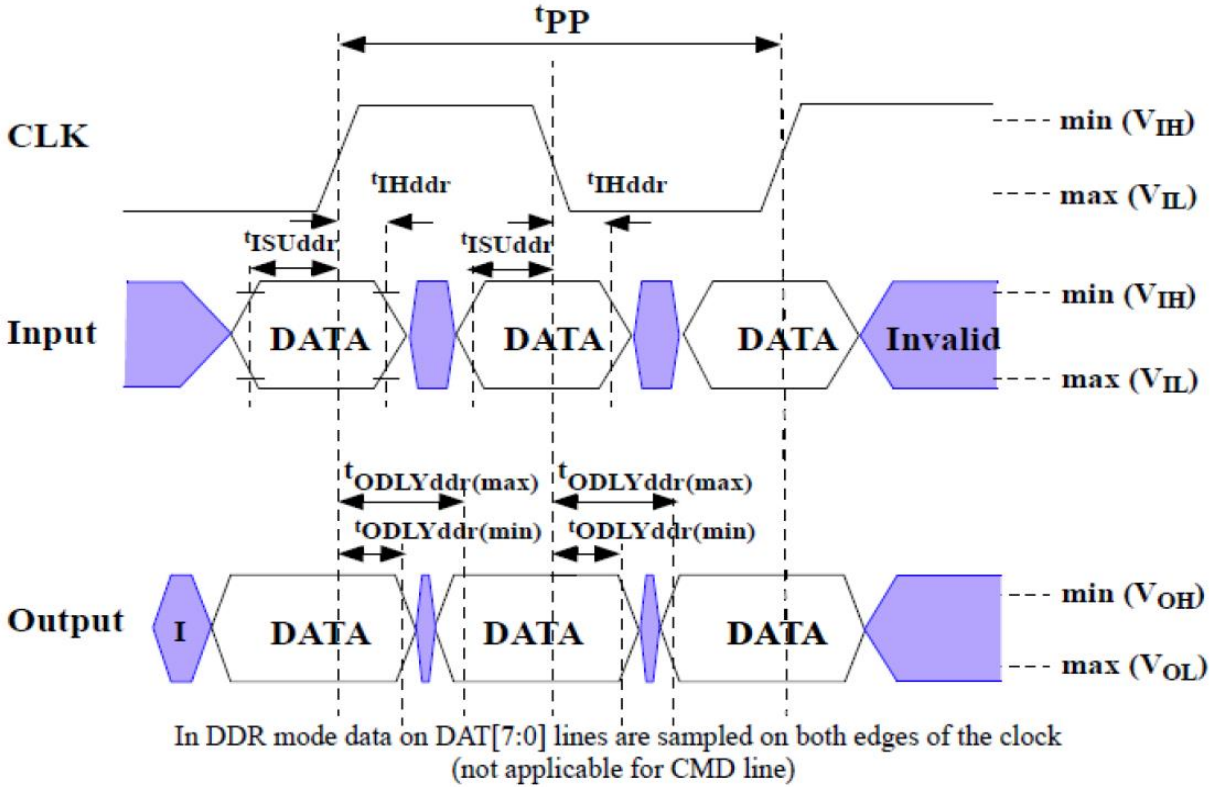
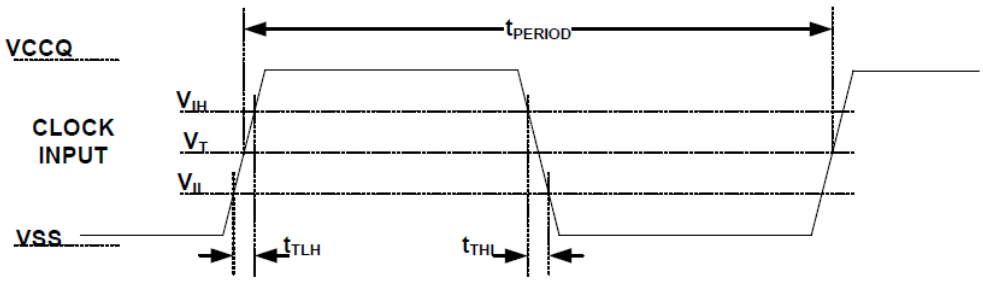


Table 5-4 Dual Data Rate Interface Timing

Parameter	Symbol	Min	Max	Unit	Remark
Input CLK[1]					
Clock Duty Cycle	-	45	55	%	Include jitter, phase noise
Input/Output DAT (Referenced to CLK-DDR Mode)					
Input set-up time	t_{ISUddr}	2.5	-	ns	CL ≤20 pF
Input hold time	t_{IHddr}	2.5	-	ns	CL ≤20 pF
Output delay time	$t_{ODLYddr}$	1.5	7	ns	CL ≤20 pF
Signal rise time (DAT0-7)[2]	t_{RISE}	-	2	ns	CL ≤20 pF
Signal fall time (DAT0-7)	t_{FALL}	-	2	ns	CL ≤20 pF
Note [1]: CLK timing is measured at 50% of VDD. Note [2]: Inputs DAT rise and fall times are measured by min (VIH) and max (VIL), and outputs DAT rise and fall times are measured by min (VOH) and max (VOL).					

Figure 5-4 HS200 Clock Signal Timing



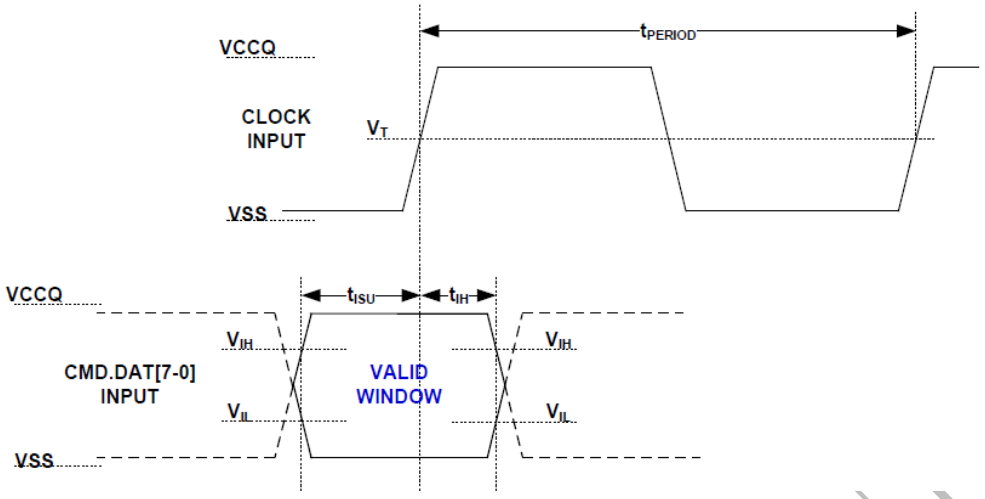
Notes:

1. V_{IH} denote V_{IH}(min.) and V_{IL} denotes V_{IL}(max.).
2. V_T=0.975V – Clock Threshold, indicates clock reference point for timing measurements.

Table 5-3 HS200 Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{PERIOD}	5	-	ns	200MHz (Max.), between rising edges
t_{TLH}, t_{THL}	-	0.2* tPERIOD	ns	tTLH, tTHL < 1ns (max.) at 200MHz, C_{DEVICE}=6pF, The absolute maximum value of tTLH, tTHL is 10ns regardless of clock frequency.
Duty Cycle	30	70	%	

Figure 5-5 HS200 Device Input Timing



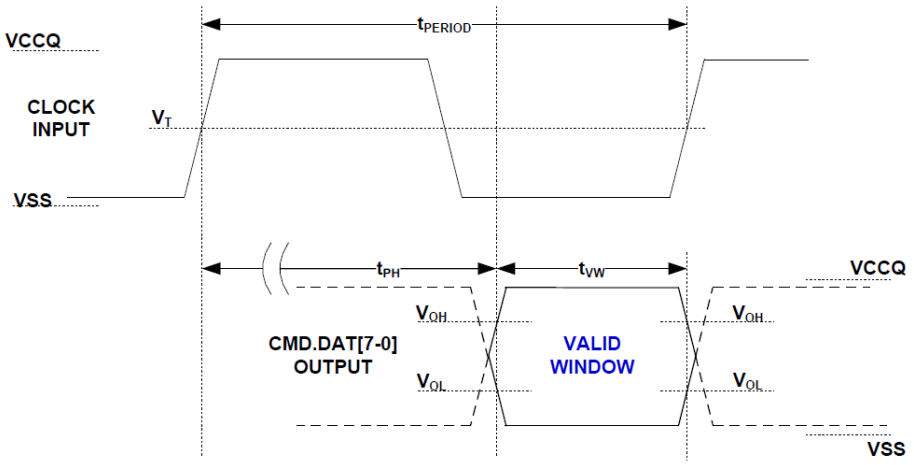
Note 1: t_{ISU} and t_{IH} are measured at V_{IL} (max) and V_{IH} (min).

Note 2: V_{IH} denote V_{IH} (min) and V_{IL} (max) denotes V_{IL} (max).

Table 5-6 HS200 Device Input Timing

Symbol	Min	Max	Unit	Remark
t_{ISU}	1.40	-	ns	C_{DEVICE} ≤6pF
t_{IH}	0.8	-	ns	C_{DEVICE} ≤6pF

Figure 5-6 HS200 Device Output Timing



NOTE V_{OH} denotes V_{OH}(min.) and V_{OL} denotes V_{OL}(max.).

Table 5-7 HS200 Device Output Timing

Symbol	Min	Max	Unit	Remark
t_{PH}	0	2	UI	Device output momentary phase from CLK input to CMD or DAT lines output. Does not include a long term temperature drift.
Δ_{TPH}	-350 (ΔT= -20°C)	+1550 (ΔT= 90°C)	ps	Delay variation due to temperature change after tuning. Total allowable shift of output valid window (TVW) from last system Tuning procedure ΔTPH is 2600ps for ΔT from -25°C to 125°C during operation.
T_{vw}	0.575	-	UI	tvw=2.88ns at 200MHz Using test circuit including skew among CMD and DAT lines created by the Device. Host path may add Signal Integrity induced noise, skews, etc. Expected TVW at Host input is larger than 0.475UI.
Note: Unit Interval (UI) is one bit nominal time. For example, UI=5ns at 200MHz.				

Figure 5-7 ΔTPH consideration

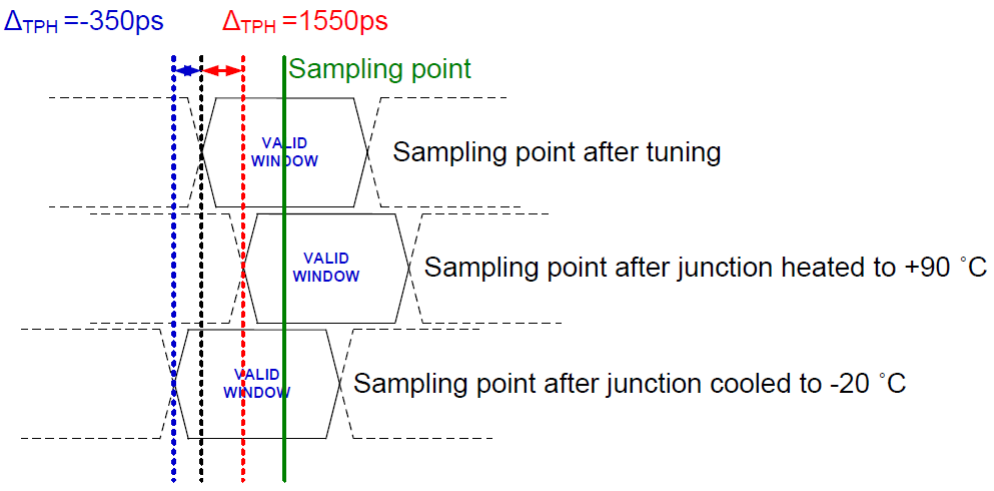


Figure 5-8 HS400 Device Input Timing

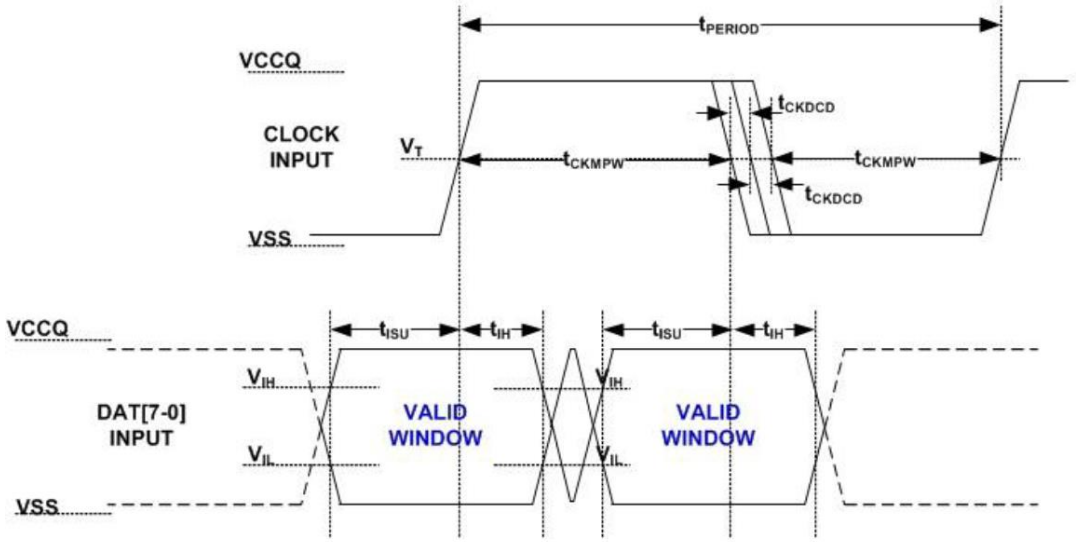


Table 5-4 HS400 Device Input Timing

Parameter	Symbol	Min	Max	Unit	Remark
Input CLK					
Cycle time data transfer mode	tPERIOD	5			200MHz (Max), between rising edges with respect to V_T.
Slew rate	SR	1.125		V/ns	With respect to V_{IH}/V_{IL}.
Duty cycle distortion	tCKDCD	0	0.3	ns	Allowable deviation from an ideal 50% duty cycle. With respect to V_T. Includes jitter, phase noise.
Minimum pulse width	tCKMPW	2.2		ns	With respect to V_T.
Input DAT (referenced to CLK)					
Input set-up time	t_{ISUddr}	0.4	-	ns	$C_{device} \leq 6pF$ with respect to V_{IH}/V_{IL}.
Input hold time	t_{IHddr}	0.4	-	ns	$C_{device} \leq 6pF$ with respect to V_{IH}/V_{IL}.
Slew rate	SR	1.125		V/ns	with respect to V_{IH}/V_{IL}.

Figure 5-9 HS400 Device Output Timing

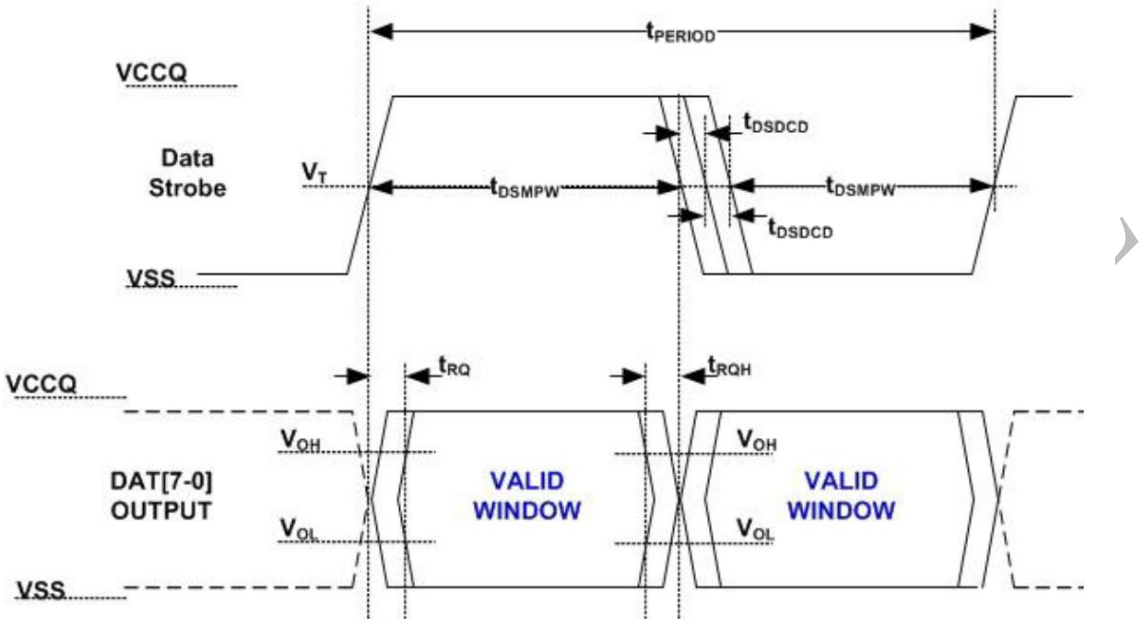


Table 5-5 HS400 Device Output Timing

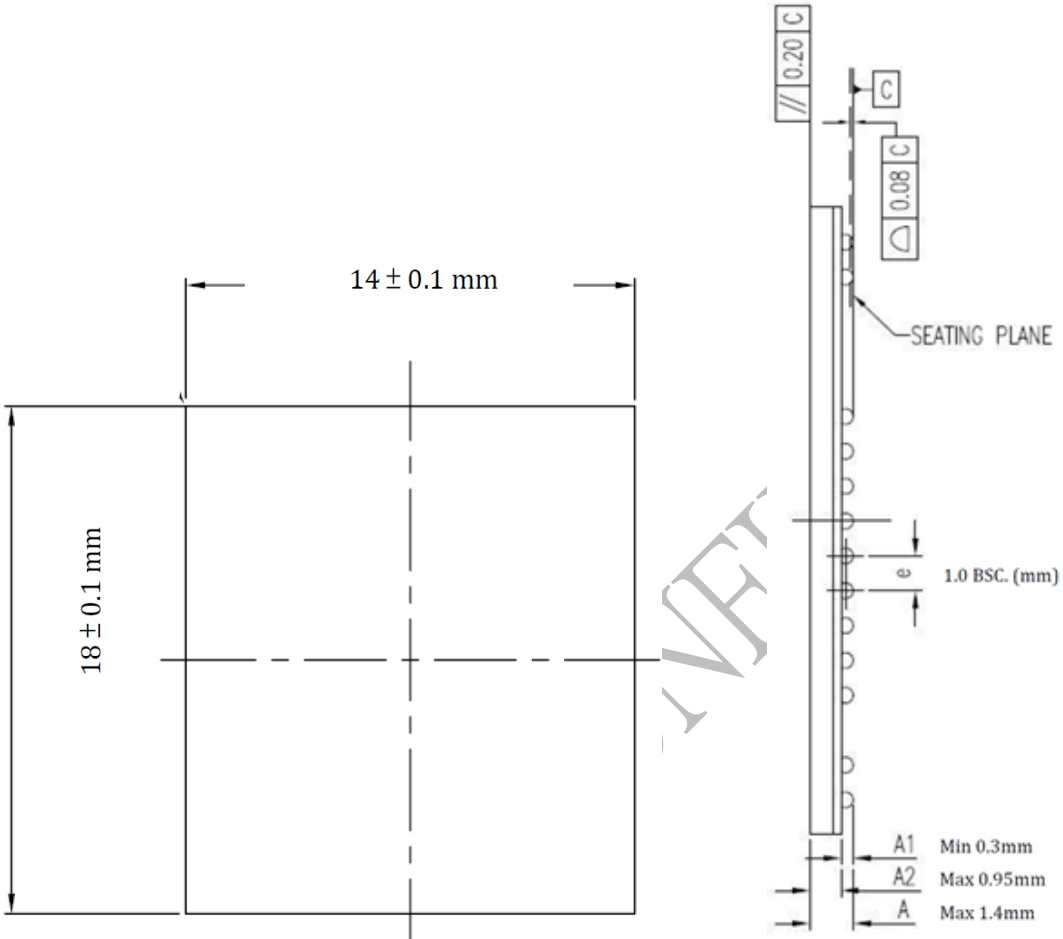
Parameter	Symbol	Min	Max	Unit	Remark
Data Strobe					
Cycle time data transfer mode	t_{PERIOD}	5			200MHz(Max), between rising edges with respect to V_T.
Slew rate	SR	1.125		V/ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Duty cycle distortion	t_{DSDCD}	0	0.2	ns	Allowable deviation from an input CLK duty cycle distortion (tCKDCD). With respect to V_T. Includes jitter, phase noise
Minimum pulse width	t_{DSMPW}	2		ns	With respect to V_T.
Read pre-amble	t_{RPRE}	0.4		t_{PERIOD}	Max value is specified by manufacture. Value up to infinite is valid
Read post-amble	t_{RPST}	0.4		t_{PERIOD}	Max value is specified by manufacture. Value up to infinite is valid
Output DAT (Referenced to Data Strobe)					
Slew rate	SR	1.125		V/ns	With respect to VOH/VOL and HS400 reference load.

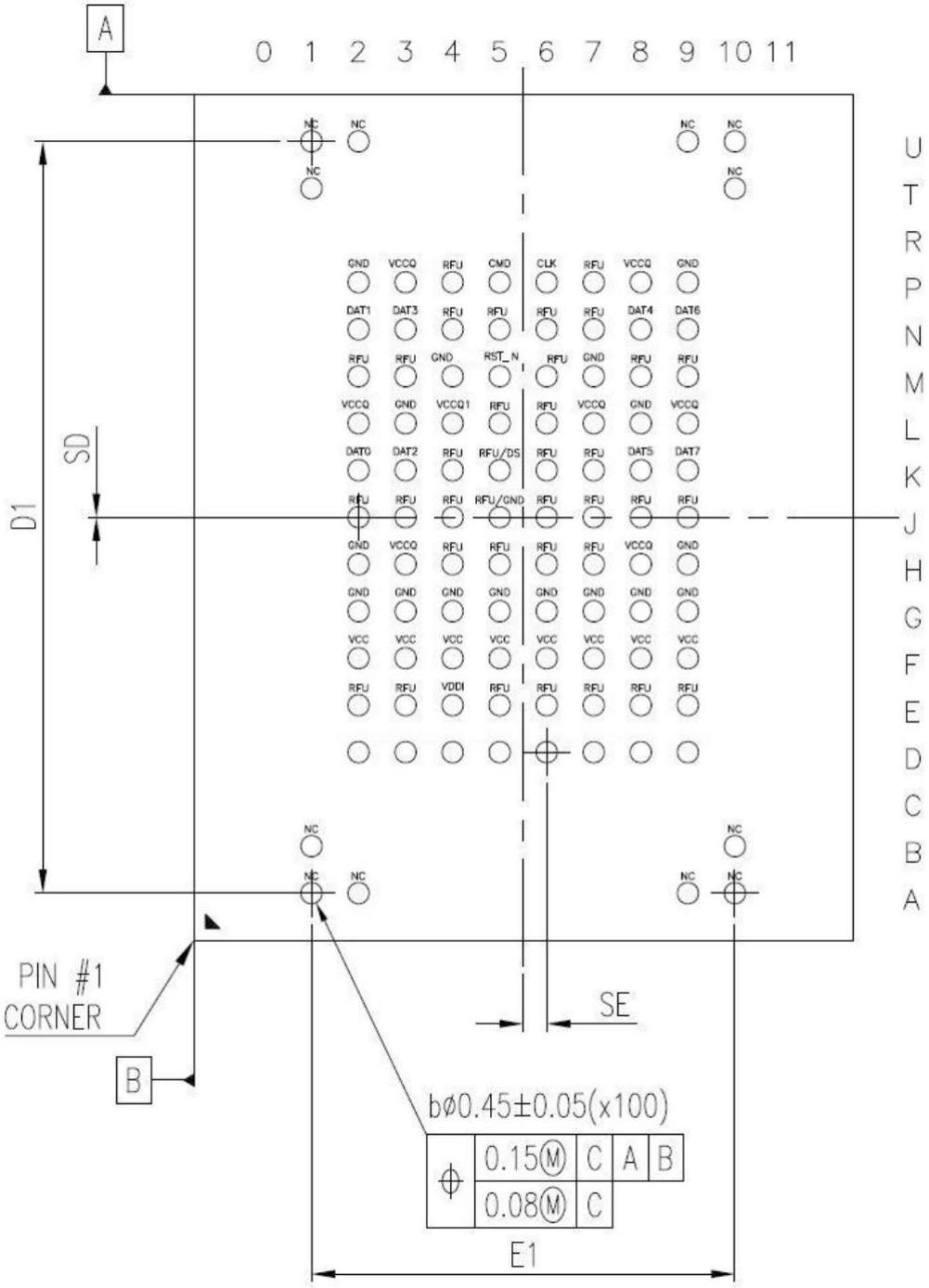
Table 5-6 HS400 Capacitance

Parameter	Symbol	Min	Type	Max	Unit
Pull-up resistance for CMD	R_{CMD}	4.7		50	Kohm
Pull-up resistance for DAT0-7	R_{DAT}	10		50	Kohm
Pull-down resistance for Data Strobe	R_{DS}	10		50	Kohm
Internal pull up resistance DAT1-DAT7	R_{int}	10		150	Kohm
Single Device capacitance	C_{device}			6	pF

6. PACKAGE

Package Size: 14.0 x 18.0 x 1.4mm





N	SE (MM)	SD (MM)	E1 (MM)	D1 (MM)	JEDEC (REF)
100	0.50 BSC.	0.00 BSC.	9.00 BSC.	16.00 BSC.	MO-276 BA

7. ORDERING INFORMATION

Capacity	MPN (Diamond Grade)	MPN (Gold Grade)	Power System	Pin Configuration	Package Size
16GB	FEMC016GCE-E530	FEMC016GCG-E530	VCCQ: 1.8V/3.3V VCC: 3.3V	100 FBGA	14x18x1.4 (mm)
32GB	FEMC032GCE-E530	FEMC032GCG-E530			
64GB	FEMC064GCE-E530	FEMC064GCG-E530			
128GB	FEMC128GCE-E530	FEMC128GCG-E530			

Capacity	MPN (Automotive Grade 2)	MPN (Automotive Grade 3)	Power System	Pin Configuration	Package Size
16GB	FEMC016GCB-E530	FEMC016GCA-E530	VCCQ: 1.8V/3.3V VCC: 3.3V	100 FBGA	14x18x1.4 (mm)
32GB	FEMC032GCB-E530	FEMC032GCA-E530			
64GB	FEMC064GCB-E530	FEMC064GCA-E530			
128GB	FEMC128GCB-E530	FEMC128GCA-E530			

Revision History

Revision	Release Date	History
1.0	2023/03	Frist Release
1.1	2023/10	Update Section 3