# Industrial eMMC 5.1 Specification

## (XTRA V Series, 3D TLC, 153ball)

**Version 2.4**



Address: 28 Genting Lane, #09-03/04/05 Platinum 28, Singapore 349585
Tel : +65-6493 5035
Fax : +65-6493 5037
Website: http://www.flexxon.com
Email: flexxon@flexxon.com

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# 1. GENERAL DESCRIPTION

## 1.1. Introduction

FLEXXON's XTRA V eMMC is fully comply with JEDEC eMMC5.1 Standard. It is combine of an embedded flash controller and 3D NAND flash memory in one JEDEC standard package, 153Balls (11.5mm x 13mm). FLEXXON eMMC provides high performance, good reliability and advanced power management. It is suitable for small, low power electronic devices.

## 1.2. Product Overview

FLEXXON XTRA V eMMC 5.1 includes the following features:

- Compliant with eMMC Specification Ver. 4.4, 4.41, 4.5, 5.0, 5.1
- Package of eMMC
  - 11.5 mm x 13 mm x 1.0 mm
- Temperature Range
  - Operation: -25°C ~ 85°C
  - Storage: -40°C ~ 85°C
- Operating Voltage
  - VCC: 3.3V
  - VCCQ: 1.8V/3.3V
- Bus Mode
  - High-speed eMMC protocol
  - Clock frequency: 0 ~ 200MHz
- Supports three data bus widths: 1 bit (default), 4 bits, 8 bits
- Supports High Speed Mode HS400
- Supports Production State Awareness
- Supports Field Firmware Update
- Supports Power Off Notification
- Support Enhanced Data Strobe
- Support Secure Write Protection
- RoHS compliant

# 2. PRODUCT SPECIFICATIONS

## 2.1. Performance

**Table 2-1 eMMC Performance**

| Density | Sequential Read (MB/s) | Sequential Write (MB/s) |
|---|---|---|
| 16GB | 315 | 195 |
| 32GB | 315 | 195 |
| 64GB | 315 | 215 |
| 128GB | 315 | 225 |
| 256GB | 315 | 240 |

Notes:

1. 8-bit bus width; HS400 mode; Vcc = 3.3V, $V_{CCQ}$ = 1.8V
2. Performance may differ according to flash configuration and platform.

## 2.2. Power Consumption

**Table 2-3 eMMC Power Consumption**

| Capacity | Read (mA) | | Write (mA) | | Standby (mA) |
|---|---|---|---|---|---|
| | $V_{CCQ}$ | Vcc | $V_{CCQ}$ | Vcc | |
| 16GB | 150 | 90 | 70 | 60 | 0.10 |
| 32GB | 160 | 90 | 70 | 60 | 0.10 |
| 64GB | 155 | 100 | 70 | 65 | 0.15 |
| 128GB | 155 | 105 | 70 | 105 | 0.15 |
| 256GB | 155 | 110 | 80 | 165 | 0.15 |

Notes:

1. 8-bit bus width; clock frequency of 200MHz DDR mode; VCC= 1.8V±5%, VCCQ=3.3V±5%
2. Standby current is measured at Vcc = 3.3V±5%, 8-bit bus width without clock frequency。

## 2.3. Partition Capacity

**Table 2-4 eMMC Partition Capacity**

| Capacity | Boot Partition 1 | Boot Partition 2 | RPMB |
|---|---|---|---|
| 16GB | 4096 KB | 4096 KB | 4096 KB |
| 32GB | 4096 KB | 4096 KB | 4096 KB |
| 64GB | 4096 KB | 4096 KB | 4096 KB |
| 128GB | 4096 KB | 4096 KB | 4096 KB |
| 256GB | 4096 KB | 4096 KB | 4096 KB |

# 3. INTERFACE DESCRIPTION

## 3.1. FLEXXON eMMC I/F Ball Array

| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 14 | NC | NC | NC | NC | NC | NC | NC | NC | NC | NC | NC | NC | NC | NC | 14 |
| 13 | NC | NC | NC | NC | NC | NC | NC | NC | NC | NC | NC | NC | NC | NC | 13 |
| 12 | NC | NC | NC | NC | NC | NC | NC | NC | NC | NC | NC | NC | NC | NC | 12 |
| 11 | NC | NC | NC | | | | | | | | | NC | NC | NC | 11 |
| 10 | NC | NC | NC | | NC | NC | NC | VSS | VCC | NC | | NC | NC | NC | 10 |
| 9 | NC | NC | NC | | NC | | | | | VCC | | NC | NC | NC | 9 |
| 8 | NC | NC | NC | | NC | | | | | VSS | | NC | NC | NC | 8 |
| 7 | NC | NC | NC | | VSS | | | | | NC | | NC | NC | NC | 7 |
| 6 | VSS | DAT7 | VCCQ | | VCC | | | | | NC | | CLK | NC | VSSQ | 6 |
| 5 | DAT2 | DAT6 | NC | | NC | VCC | VSS | DS | VSS | RST_n | | CMD | VSSQ | VCCQ | 5 |
| 4 | DAT1 | DAT5 | VSSQ | NC | | | | | | | | VCCQ | VCCQ | VSSQ | 4 |
| 3 | DAT0 | DAT4 | NC | NC | NC | NC | NC | NC | NC | NC | NC | NC | NC | VCCQ | 3 |
| 2 | NC | DAT3 | VDDi | NC | NC | NC | NC | NC | NC | NC | NC | NC | VSSQ | NC | 2 |
| 1 | NC | NC | NC | NC | NC | NC | NC | NC | NC | NC | NC | NC | NC | NC | 1 |
| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | |

**Figure 3-1 eMMC interface in 153Balls Array (Top View)**

## 3.2. Pins and Signal Description

**Table 3-1 Function Pin Assignment, 153 balls**

| eMMC Interface | | | |
|---|---|---|---|
| **Ball No.** | **Ball Signal** | **Type** | **Description** |
| A3 | DAT0 | I/O/PP | Data I/O: Bidirectional channel used for data transfer |
| A4 | DAT1 | | |
| A5 | DAT2 | | |
| B2 | DAT3 | | |
| B3 | DAT4 | | |
| B4 | DAT5 | | |
| B5 | DAT6 | | |
| B6 | DAT7 | | |
| M5 | CMD | I/O/PP | Command: A bidirectional channel used for device initialization and command transfers. |
| M6 | CLK | Input | Clock: Each cycle directs a 1-bit transfer on the command and DAT lines |
| K5 | RST_n | Input | Hardware Reset |
| E6 | VCC | Supply | Supply Voltage for Core |
| F5 | VCC | | |
| J10 | VCC | | |
| K9 | VCC | | |
| C6 | VCCQ | Supply | Supply Voltage for I/O |
| M4 | VCCQ | | |
| N4 | VCCQ | | |
| P3 | VCCQ | | |
| P5 | VCCQ | | |
| A6 | VSS | Supply | Supply Voltage ground for Core |
| E7 | VSS | | |
| G5 | VSS | | |
| H10 | VSS | | |
| J5 | VSS | | |
| K8 | VSS | | |
| C4 | VSSQ | Supply | Supply Voltage ground for I/O |
| N2 | VSSQ | | |
| N5 | VSSQ | | |
| P4 | VSSQ | | |
| P6 | VSSQ | | |
| H5 | DS | O/PP | Data strobe |
| C2 | VDDi | | Connect capacitor from VDDi to GND for stabilize internal power. |

**Note:**

NC: No connect in eMMC. Left it floating.

# 4. EMMC REGISTERS

## 4.1. OCR Register

The 32-bit Operation Conditions Register (OCR) stores the VDD voltage profile of the Device and the access mode indication. The OCR register should be implemented by all Device.

**Table 4-1 OCR Register Table**

| OCR slice | Description | Value | Width |
|---|---|---|---|
| [31] | Card power up status bit (busy)[1] | | |
| [30:29] | Access mode | 00b (byte mode)<br>10b (sector mode) | 2 |
| [28:24] | Reserved | 0 0000b | 5 |
| [23:15] | 2.7 - 3.6V | 1 1111 1111b | 9 |
| [14:8] | 2.0 - 2.6V | 000 0000b | 7 |
| [7] | 1.7 - 1.95V | 1b | 1 |
| [6:0] | Reserved | 000 0000b | 7 |
| Note [1]: This bit is set to Low if the Device has not finished the power up routine | | | |

## 4.2. CID Register

The Card Identification (CID) register is 128 bits wide. It contains the Device identification information used during the Device identification phase. For details, refer to JEDEC Standard Specification No. JESD84-B51.

**Table 4-2 CID Register Table**

| Name | Field | CID Slice | Value | Width |
|---|---|---|---|---|
| Manufacturer ID | MID | [127:120] | EBh | 8 |
| Reserved | - | [119:114] | 0h | 6 |
| Device/BGA | CBX | [113:112] | 1h | 2 |
| OEM/ Application ID | OID | [111:104] | 0Dh | 8 |
| Product Name | PNM | [103:56] | eMMC | 48 |
| Product Revision | PRV | [55:48] | 51h | 8 |
| Product Serial Number | PSN | [47:16] | Random by Production | 32 |
| Manufacturing Date | MDT | [15:8] | Month, Year | 8 |
| CRC7 Checksum | CRC | [7:1] | - | 7 |
| Not used, always “1” | - | [0:0] | 1h | 1 |

## 4.3. CSD Register

The Device-Specific Data (CSD) register provides information on how to access the contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, etc. For details, refer to JEDEC Standard Specification No. JESD84-B51.

**Table 4-3 CSD Register Table**

| Name | Field | Width | Type | CSD Slice | Value |
|---|---|---|---|---|---|
| CSD structure | CSD_STRUCTURE | 2 | R | [127:126] | 3h |
| System specification version | SPEC_VERS | 4 | R | [125:122] | 4h |
| Reserved | - | 2 | R | [121:120] | 0h |
| Data read access-time 1 | TAAC | 8 | R | [119:112] | 4Fh |
| Data read access-time 2 in CLK cycles (NSAC*100) | NSAC | 8 | R | [111:104] | 1h |
| Max. bus clock frequency | TRAN_SPEED | 8 | R | [103:96] | 32h |
| Device command classes | CCC | 12 | R | [95:84] | 8F5h |
| Max. read data block length | READ_BL_LEN | 4 | R | [83:80] | 9h |
| Partial blocks for read allowed | READ_BL_PARTIAL | 1 | R | [79:79] | 0h |
| Write block misalignment | WRITE_BLK_MISALIGN | 1 | R | [78:78] | 0h |
| Read block misalignment | READ_BLK_MISALIGN | 1 | R | [77:77] | 0h |
| DSR implemented | DSR_IMP | 1 | R | [76:76] | 0h |
| Reserved | - | 2 | R | [75:74] | 0h |
| Device size | C_SIZE | 12 | R | [73:62] | FFFh |
| Max. read current @ VDD min | VDD_R_CURR_MIN | 3 | R | [61:59] | 7h |
| Max. read current @ VDD max | VDD_R_CURR_MAX | 3 | R | [58:56] | 7h |
| Max. write current @ VDD min | VDD_W_CURR_MIN | 3 | R | [55:53] | 7h |
| Max. write current @ VDD max | VDD_W_CURR_MAX | 3 | R | [52:50] | 7h |
| Device size multiplier | C_SIZE_MULT | 3 | R | [49:47] | 7h |
| Erase group size | ERASE_GRP_SIZE | 5 | R | [46:42] | 0Fh (16GB&32GB)<br>1Fh (64GB, 128GB& 256GB) |
| Erase group size multiplier | ERASE_GRP_MULT | 5 | R | [41:37] | 1Fh |
| Write protect group size | WP_GRP_SIZE | 5 | R | [36:32] | 0Fh |
| Write protect group enable | WP_GRP_ENABLE | 1 | R | [31:31] | 1h |
| Manufacturer default ECC | DEFAULT_ECC | 2 | R | [30:29] | 0h |
| Write speed factor | R2W_FACTOR | 3 | R | [28:26] | 2h |
| Max. write data block length | WRITE_BL_LEN | 4 | R | [25:22] | 9h |
| Partial blocks for write allowed | WRITE_BL_PARTIAL | 1 | R | [21:21] | 0h |
| Reserved | - | 4 | R | [20:17] | 0h |
| Content protection application | CONTENT_PROT_APP | 1 | R | [16:16] | 0h |
| File format group | FILE_FORMAT_GRP | 1 | R/W | [15:15] | 0h |
| Copy flag (OTP) | COPY | 1 | R/W | [14:14] | 0h |

| | | | | | |
|---|---|---|---|---|---|
| Permanent write protection | PERM_WRITE_PROTEC | 1 | R/W | [13:13] | 0h |
| Temporary write protection | TMP_WRITE_PROTECT | 1 | R/W/E | [12:12] | 0h |
| File format | FILE_FORMAT | 2 | R/W | [11:10] | 0h |
| ECC code | ECC | 2 | R/W/E | [9:8] | 0h |
| CRC | CRC | 7 | R/W/E | [7:1] | 64h-(16GB&32GB)<br>2Eh -(64GB,<br>128GB& 256GB) |
| Not used, always '1' | - | 1 | - | [0:0] | 1h |

## 4.4. Extended CSD Register

The Extended CSD register defines the Device properties and selected modes. It is 512 bytes long. The most significant 320 bytes are the Properties segment, which defines the Device capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the Device is working in. These modes can be changed by the host by means of the SWITCH command. For details, refer to JEDEC Standard Specification No. JESD84-B51.

## 4.5. RCA Register

The writable 16-bit Relative Device Address (RCA) register carries the Device address assigned by the host during the Device identification. This address is used for the addressed host-Device communication after the Device identification procedure. The default value of the RCA register is 0x0001. The value 0x0000 is reserved to set all Devices into the *Stand-by State* with CMD7.

## 4.6. DSR Register

The 16-bit driver stage register (DSR) is described in detail in JEDEC Standard Specification, JESD84-B51 Section 7.6. It can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of Devices). The CSD register carries the information about the DSR register usage. The default value of the DSR register is 0x404.

# 5. ELECTRICAL CHARACTERISTICS

## 5.1. Power Supply

**Table 5-1 eMMC power supply**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage (NAND) | Vcc | 2.7 | 3.6 | V |
| Supply voltage (I/O) | $V_{CCQ}$ | 2.7 | 3.6 | V |
| | | 1.7 | 1.95 | V |
| Supply Power-Up for 1.8V | tPRUL | | 25 | ms |
| Supply Power-Up for 3.3V | tPRUH | | 35 | ms |

## 5.2. Bus Signal Levels

**Figure 5-1 Bus Signal Levels**

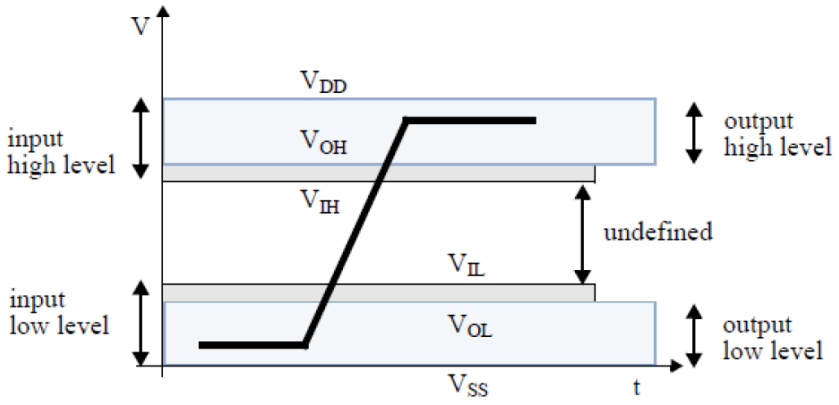
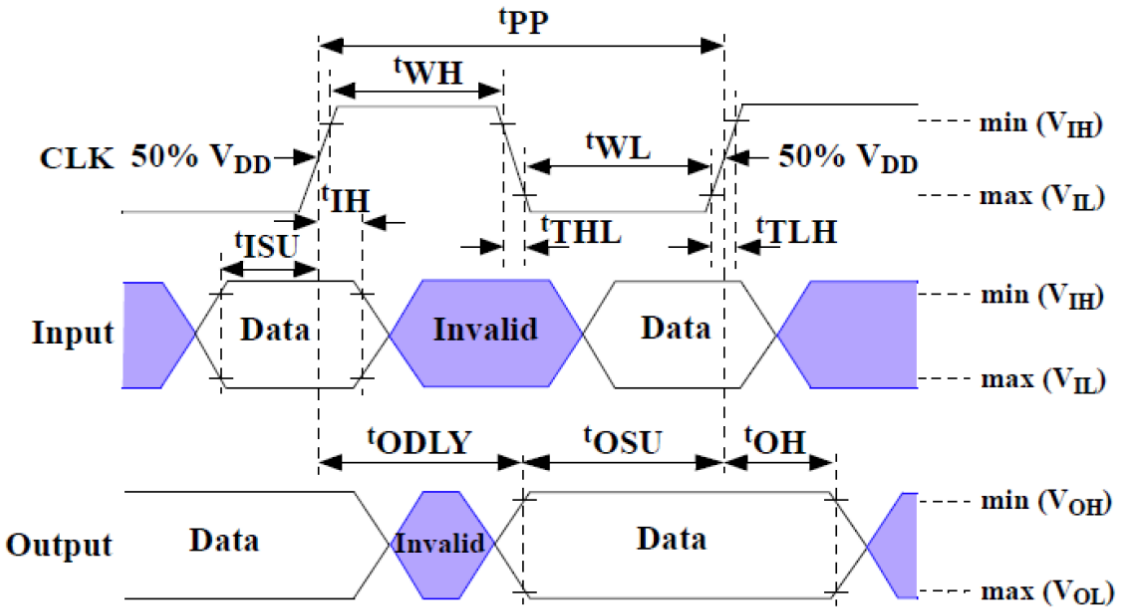



**Table 5-2 Bus Signals Levels**

| Parameter | Symbol | Min | Max | Unit | Remark |
|---|---|---|---|---|---|
| **Open-Drain Bus Signal Level** | | | | | |
| Output High Voltage | $V_{OH}$ | VDD - 0.2 | - | V | $I_{OH}$ = -100 uA |
| Output Low Voltage | $V_{OL}$ | - | 0.3 | V | $I_{OL}$ = 2 mA |
| **Push-pull bus signal level (2.7V~3.6V)** | | | | | |
| Output High Voltage | $V_{OH}$ | 0.75 * VCCQ | - | V | $I_{OH}$ = -100 uA @ $V_{CCQ}$ min |
| Output Low Voltage | $V_{OL}$ | - | 0.125 * VCCQ | V | $I_{OL}$ = 100 uA @ $V_{CCQ}$ min |
| Input High Voltage | $V_{IH}$ | 0.625 * VCCQ | VCCQ + 0.3 | V | |
| Input Low Voltage | $V_{IL}$ | VSS - 0.3 | 0.25 * VCCQ | V | |
| **Push-pull bus signal level (1.7V~1.95V)** | | | | | |
| Output High Voltage | $V_{OH}$ | VCCQ - 0.45V | - | V | $I_{OH}$ = -2 mA |
| Output Low Voltage | $V_{OL}$ | - | 0.45V | V | $I_{OL}$ = 2 mA |
| Input High Voltage | $V_{IH}$ | 0.65 * VCCQ | VCCQ + 0.3 | V | |
| Input Low Voltage | $V_{IL}$ | $V_{SS}$ - 0.3 | 0.35 * $V_{DD}$ | V | |

## 5.3. Bus Timing

**Figure 5-2 Bus Timing in Single Data Rate Mode**




Data must always be sampled on the rising edge of the clock.

**Table 5-3 Backward Compatible Device Interface Timing**

| Parameter | Symbol | Min | Max | Unit | Remark[1] |
|---|---|---|---|---|---|
| **Clock CLK[2]** | | | | | |
| Clock Frequency Data Transfer Mode (PP)[3] | $f_{PP}$ | 0 | 26 | MHz | CL ≤ 30 pF |
| Clock Frequency Identification Mode (OD) | $f_{OD}$ | 0 | 400 | kHz | |
| Clock high time | $t_{WH}$ | 10 | - | ns | CL ≤ 30 pF |
| Clock low time | $t_{WL}$ | 10 | - | ns | CL ≤ 30 pF |
| Clock rise time[4] | $t_{TLH}$ | - | 10 | ns | CL ≤ 30 pF |
| Clock fall time | $t_{THL}$ | - | 10 | ns | CL ≤ 30 pF |
| **Inputs/Outputs CMD, DAT** (Referenced to CLK) | | | | | |
| Input set-up time | $t_{ISU}$ | 3 | - | ns | CL ≤ 30 pF |
| Input hold time | $t_{IH}$ | 3 | - | ns | CL ≤ 30 pF |
| Output set-up time[5] | $t_{OSU}$ | 11.7 | - | ns | CL ≤ 30 pF |
| Output hold time[5] | $t_{OH}$ | 8.3 | - | ns | CL ≤ 30 pF |

Note [1]: The Device must always start with the backward-compatible interface timing. The timing mode can be switched to high-speed interface timing by the host sending the SWITCH command (CMD6) with the argument for high-speed interface select.
Note [2]: CLK timing is measured at 50% of VDD.
Note [3]: For compatibility with Devices that support the v4.2 standard or earlier, host should not use > 26 MHz before switching to high-speed interface timing.
Note [4]: CLK rise and fall times are measured by min (VIH) and max (VIL).
Note [5]: tOSU and tOH are defined as values from clock rising edge. However, there may be Devices or devices which utilize clock falling edge to output data in backward compatibility mode. Therefore, it is recommended for hosts either to settWL value as long as possible within the range which will not go over tCK-tOH(min) in the system or to use slow clock frequency, so that host could have data set up margin for those devices. In this case, each device which utilizes clock falling edge might show the correlation either between tWL and tOSU or between tCK and tOSU for the device in its own datasheet as a note or its' application notes.

**Table 5-4 High Speed Device Interface Timing**

| Parameter | Symbol | Min | Max | Unit | Remark |
|---|---|---|---|---|---|
| **Clock CLK**[1] | | | | | |
| Clock Frequency Data Transfer Mode (PP)[2] | $f_{PP}$ | 0 | 52[3] | MHz | CL ≤30 pF<br>Tolerance:+ 100 KHz |
| Clock Frequency Identification Mode (OD) | $f_{OD}$ | 0 | 400 | kHz | Tolerance: +20 KHz |
| Clock high time | $t_{WH}$ | 6.5 | - | ns | CL ≤30 pF |
| Clock low time | $t_{WL}$ | 6.5 | - | ns | CL ≤30 pF |
| Clock rise time[4] | $t_{TLH}$ | - | 3 | ns | CL ≤30 pF |
| Clock fall time | $t_{THL}$ | - | 3 | ns | CL ≤30 pF |
| **Inputs /Outputs CMD, DAT** (Referenced to CLK) | | | | | |
| Input set-up time | $t_{ISU}$ | 3 | - | ns | CL ≤30 pF |
| Input hold time | $t_{IH}$ | 3 | - | ns | CL ≤30 pF |
| Output delay time during data transfer | $t_{ODLY}$ | - | 13.7 | ns | CL ≤30 pF |
| Output hold time | $t_{OH}$ | 2.5 | - | ns | CL ≤30 pF |
| Signal rise time[5] | $t_{RISE}$ | - | 3 | ns | CL ≤30 pF |
| Note [1]: CLK timing is measured at 50% of VDD.<br>Note [2]: eMMC shall support the full frequency range from 0-26Mhz, or 0-52MHz<br>Note [3]: Device can operate as high-speed Device interface timing at 26 MHz clock frequency.<br>Note [4]: CLK rise and fall times are measured by min (VIH) and max (VIL).<br>Note [5]: Inputs CMD, DAT rise and fall times are measured by min (VIH) and max (VIL), and output CMD, DAT rise and fall times are measured by min (VOH) and max (VOL). | | | | | |



**Figure 5-3 Bus Timing in Dual Data Rate Mode**

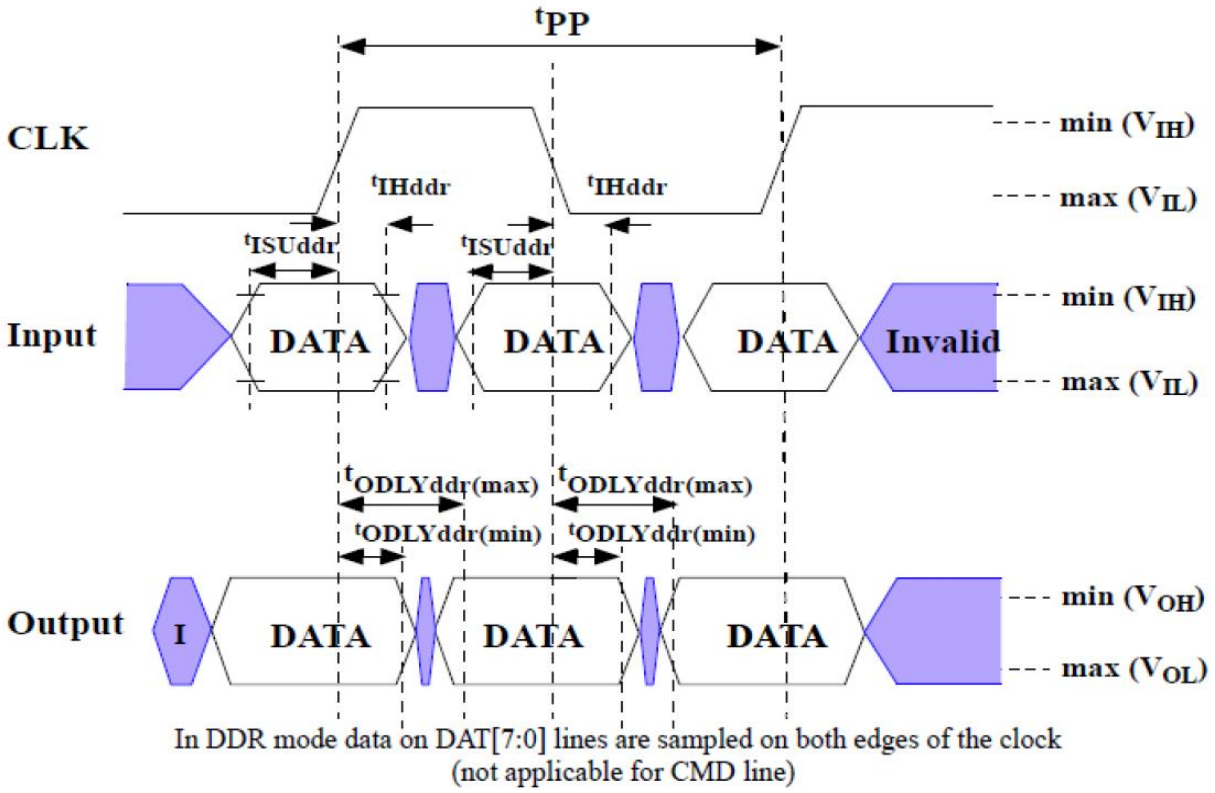
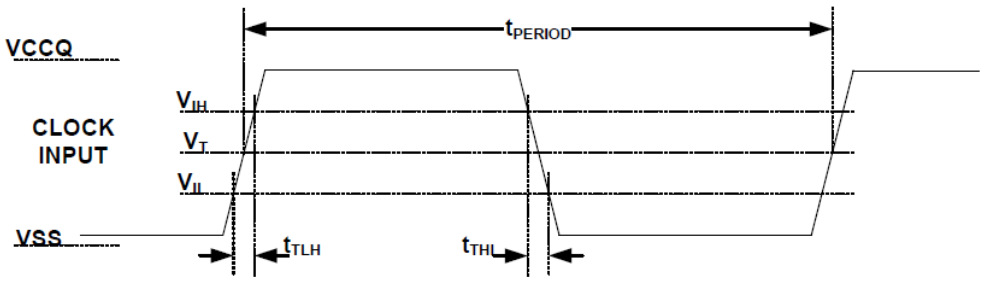


**Table 5-5 Dual Data Rate Interface Timing**

| Parameter | Symbol | Min | Max | Unit | Remark |
|---|---|---|---|---|---|
| **Input CLK**[1] | | | | | |
| Clock Duty Cycle | - | 45 | 55 | % | Include jitter, phase noise |
| **Input/Output DAT** (Referenced to CLK-DDR Mode) | | | | | |
| Input set-up time | $t_{ISUddr}$ | 2.5 | - | ns | CL ≤20 pF |
| Input hold time | $t_{IHddr}$ | 2.5 | - | ns | CL ≤20 pF |
| Output delay time | $t_{ODLYddr}$ | 1.5 | 7 | ns | CL ≤20 pF |
| Signal rise time (DAT0-7)[2] | $t_{RISE}$ | - | 2 | ns | CL ≤20 pF |
| Signal fall time (DAT0-7) | $t_{FALL}$ | - | 2 | ns | CL ≤20 pF |
| Note [1]: CLK timing is measured at 50% of VDD.<br>Note [2]: Inputs DAT rise and fall times are measured by min (VIH) and max (VIL), and outputs DAT rise and fall times are measured by min (VOH) and max (VOL). | | | | | |

**Figure 5-4 HS200 Clock Signal Timing**



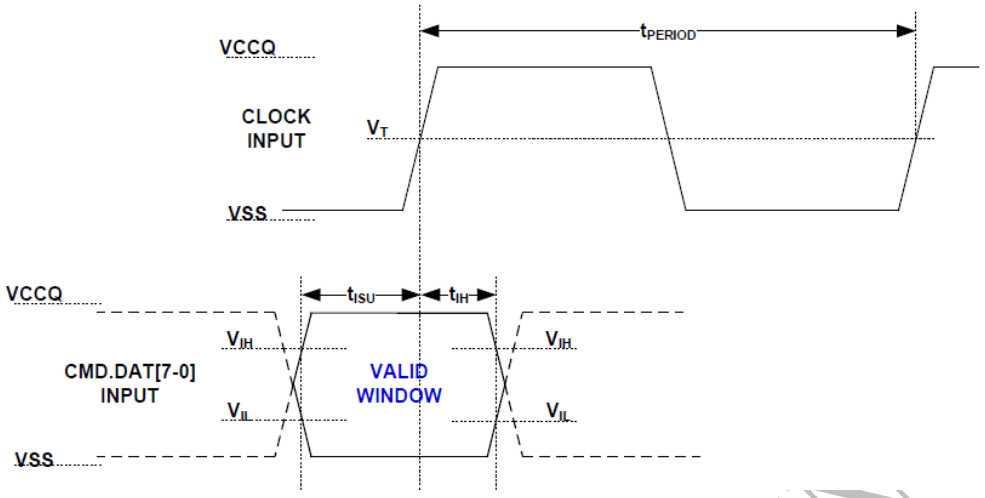

Notes:

1. $V_{IH}$ denote $V_{IH}$(min.) and $V_{IL}$ denotes $V_{IL}$(max.).
2. $V_T$=0.975V – Clock Threshold, indicates clock reference point for timing measurements.

**Table 5-6 HS200 Clock Signal Timing**

| Symbol | Min | Max | Unit | Remark |
|---|---|---|---|---|
| $t_{PERIOD}$ | 5 | - | ns | 200MHz (Max.), between rising edges |
| $t_{TLH}$, $t_{THL}$ | - | 0.2* tPERIOD | ns | tTLH, tTHL < 1ns (max.) at 200MHz, $C_{DEVICE}$=6pF, The absolute maximum value of tTLH, tTHL is 10ns regardless of clock frequency. |
| Duty Cycle | 30 | 70 | % | |

**Figure 5-5 HS200 Device Input Timing**



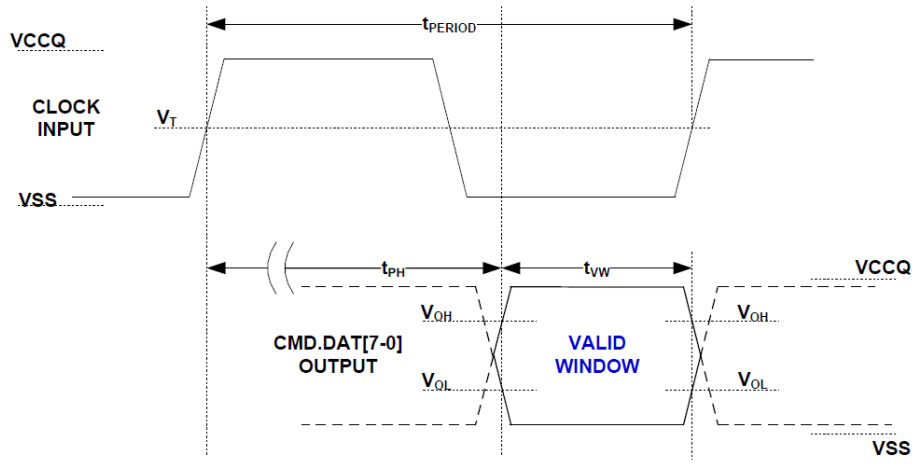

Note 1: $t_{ISU}$ and $t_{IH}$ are measured at $V_{IL}$ (max) and $V_{IH}$ (min).

Note 2: $V_{IH}$ denote $V_{IH}$ (min) and $V_{IL}$ (max) denotes $V_{IL}$ (max).

**Table 5-7 HS200 Device Input Timing**

| Symbol | Min | Max | Unit | Remark |
|---|---|---|---|---|
| $t_{ISU}$ | 1.40 | - | ns | $C_{DEVICE}$ ≤6pF |
| $t_{IH}$ | 0.8 | - | ns | $C_{DEVICE}$ ≤6pF |

**Figure 5-6 HS200 Device Output Timing**




NOTE $V_{OH}$ denotes $V_{OH}$(min.) and $V_{OL}$ denotes $V_{OL}$(max.).

**Table 5-8 HS200 Device Output Timing**

| Symbol | Min | Max | Unit | Remark |
|---|---|---|---|---|
| $t_{PH}$ | 0 | 2 | UI | Device output momentary phase from CLK input to CMD or DAT lines output.<br>Does not include a long term temperature drift. |
| $\Delta_{TPH}$ | -350<br>(ΔT= -20°C) | +1550<br>(ΔT= 90°C) | ps | Delay variation due to temperature change after tuning. Total allowable shift of output valid window (TVW) from last system Tuning procedure ΔTPH is 2600ps for ΔT from -25°C to 125°C during operation. |
| $t_{VW}$ | 0.575 | - | UI | tvw=2.88ns at 200MHz<br>Using test circuit including skew among CMD and DAT lines created by the Device.<br>Host path may add Signal Integrity induced noise, skews, etc. Expected TVW at Host input is larger than 0.475UI. |
| Note: Unit Interval (UI) is one bit nominal time. For example, UI=5ns at 200MHz. | | | | |

**Figure 5-7 ΔTPH consideration**

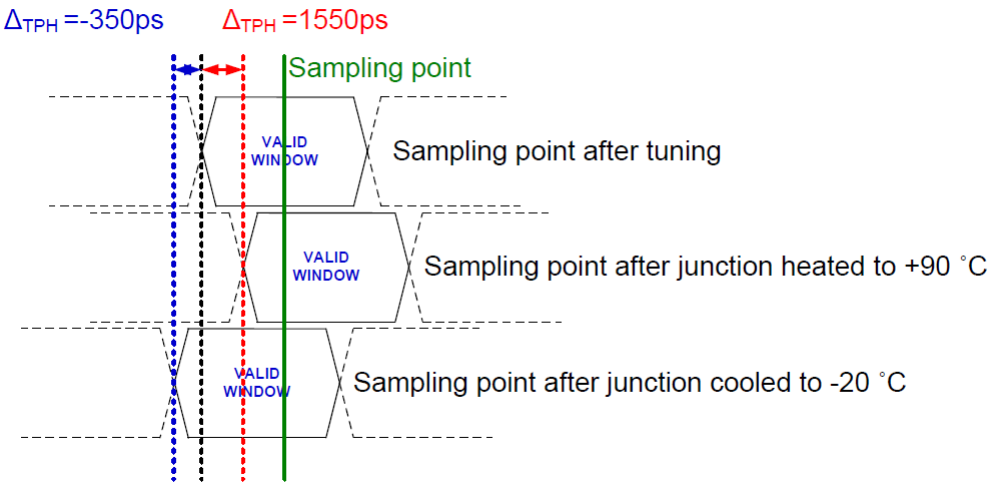


**Figure 5-8 HS400 Device Input Timing**

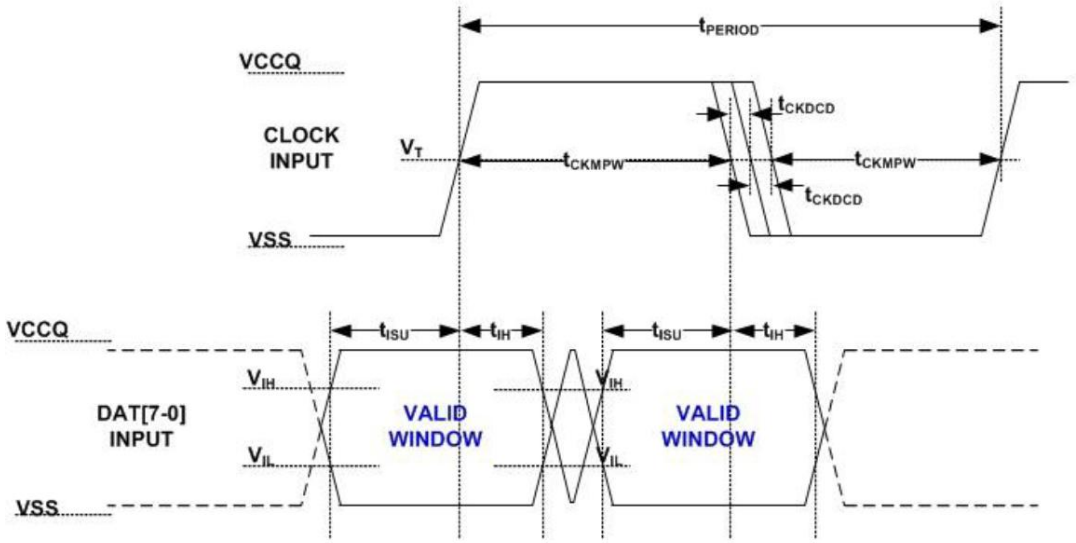



**Table 5-9 HS400 Device Input Timing**

| Parameter | Symbol | Min | Max | Unit | Remark |
|---|---|---|---|---|---|
| **Input CLK** | | | | | |
| Cycle time data transfer mode | tPERIOD | 5 | | | 200MHz (Max), between rising edges with respect to $V_T$. |
| Slew rate | SR | 1.125 | | V/ns | With respect to $V_{IH}/V_{IL}$. |
| Duty cycle distortion | tCKDCD | 0 | 0.3 | ns | Allowable deviation from an ideal 50% duty cycle. With respect to $V_T$. Includes jitter, phase noise. |
| Minimum pulse width | tCKMPW | 2.2 | | ns | With respect to $V_T$. |
| **Input DAT** (referenced to CLK) | | | | | |
| Input set-up time | $t_{ISUddr}$ | 0.4 | - | ns | $C_{Device}$ ≤ 6pF with respect to $V_{IH}/V_{IL}$. |
| Input hold time | $t_{IHddr}$ | 0.4 | - | ns | $C_{Device}$ ≤ 6pF with respect to $V_{IH}/V_{IL}$. |
| Slew rate | SR | 1.125 | | V/ns | with respect to $V_{IH}/V_{IL}$. |

**Figure 5-9 HS400 Device Output Timing**

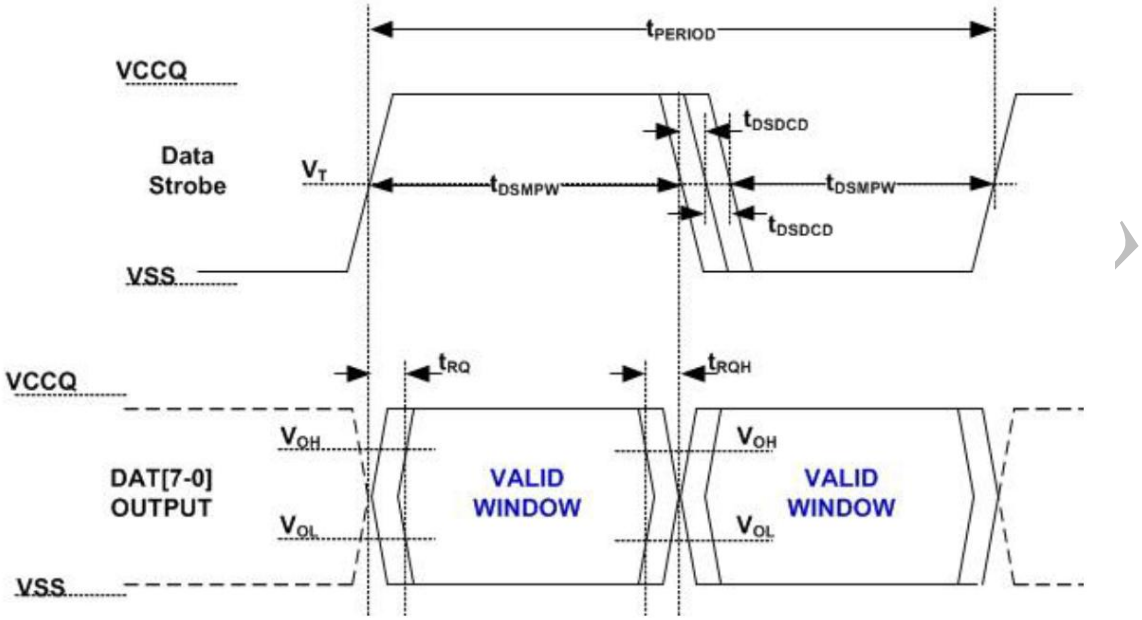



**Table 5-10 HS400 Device Output Timing**

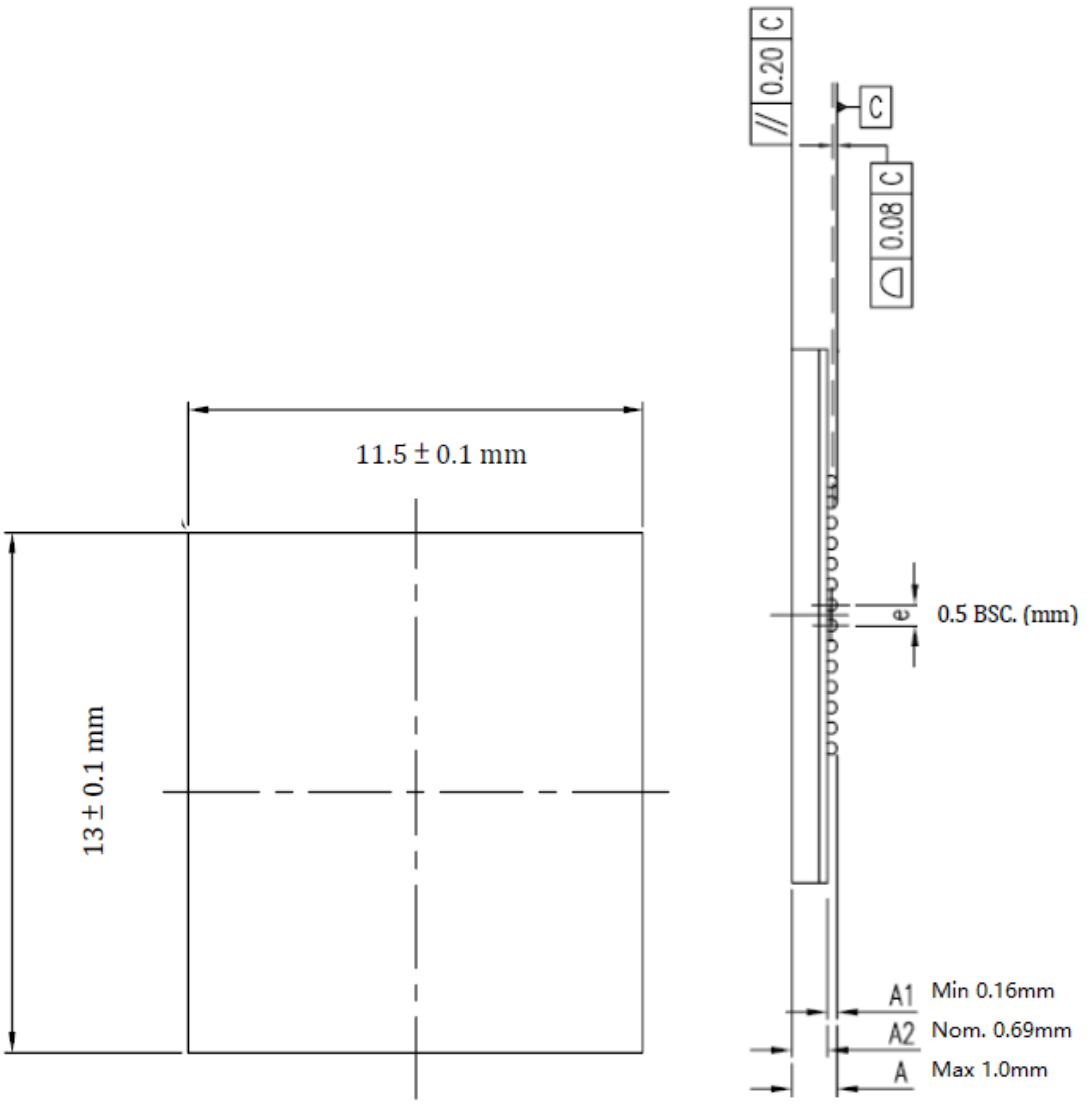
| Parameter | Symbol | Min | Max | Unit | Remark |
|---|---|---|---|---|---|
| **Data Strobe** | | | | | |
| Cycle time data transfer mode | $t_{PERIOD}$ | 5 | | | 200MHz(Max), between rising edges with respect to $V_T$. |
| Slew rate | SR | 1.125 | | V/ns | With respect to $V_{OH}$/$V_{OL}$ and HS400 reference load |
| Duty cycle distortion | $t_{DSDCD}$ | 0 | 0.2 | ns | Allowable deviation from an input CLK duty cycle distortion (tCKDCD). With respect to $V_T$. Includes jitter, phase noise |
| Minimum pulse width | $t_{DSMPW}$ | 2 | | ns | With respect to $V_T$. |
| Read pre-amble | $t_{RPRE}$ | 0.4 | | $t_{PERIOD}$ | Max value is specified by manufacture. Value up to infinite is valid |
| Read post-amble | $t_{RPST}$ | 0.4 | | $t_{PERIOD}$ | Max value is specified by manufacture. Value up to infinite is valid |
| **Output DAT** (Referenced to Data Strobe) | | | | | |
| Slew rate | SR | 1.125 | | V/ns | With respect to VOH/VOL and HS400 reference load. |

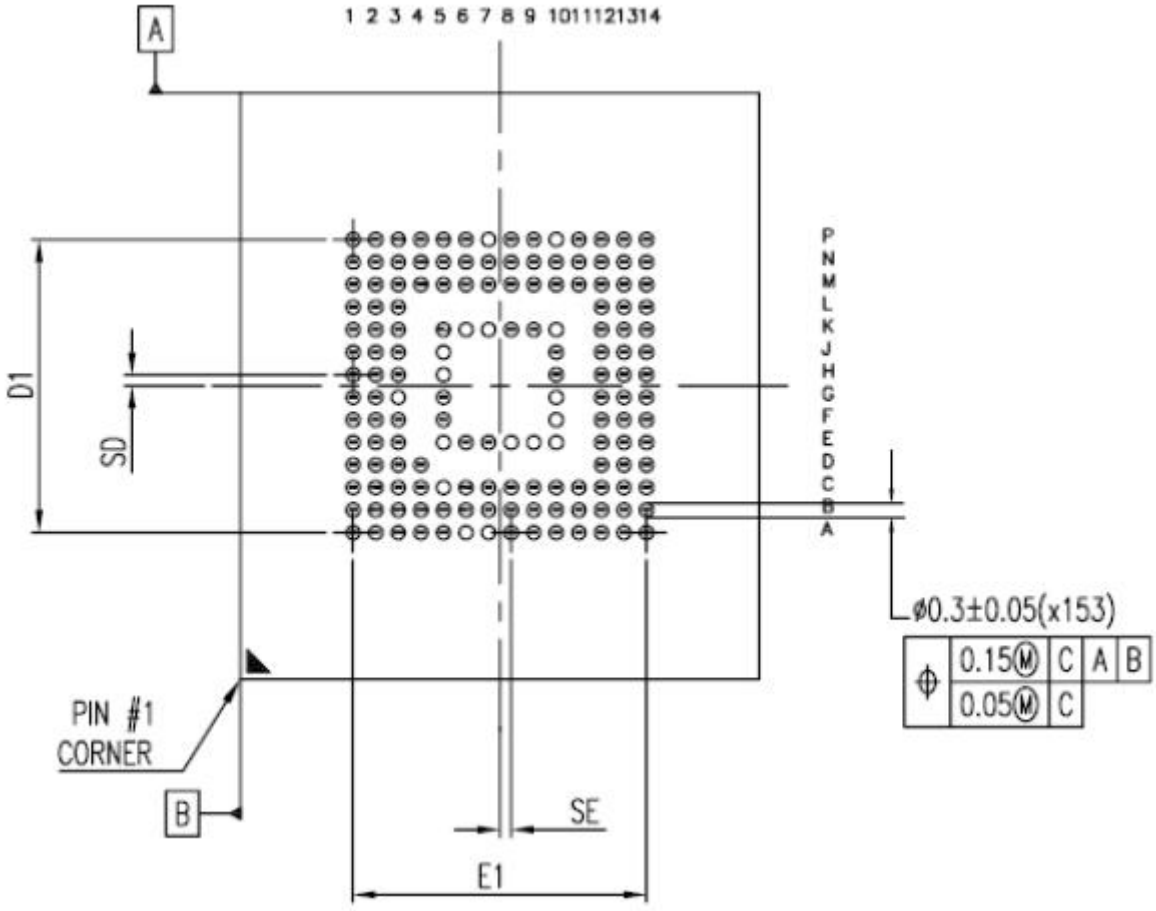
**Table 5-11 HS400 Capacitance**

| Parameter | Symbol | Min | Type | Max | Unit |
|---|---|---|---|---|---|
| Pull-up resistance for CMD | $R_{CMD}$ | 4.7 | | 50 | Kohm |
| Pull-up resistance for DAT0-7 | $R_{DAT}$ | 10 | | 50 | Kohm |
| Pull-down resistance for Data Strobe | $R_{DS}$ | 10 | | 50 | Kohm |
| Internal pull up resistance DAT1-DAT7 | $R_{int}$ | 10 | | 150 | Kohm |
| Bus signal line capacitance | CL | | | 13 | pF |
| Single Device capacitance | $C_{Device}$ | | | 6 | pF |

# 6. PACKAGE

Package Size: 11.5 x 13.0 x 1.0mm






Bottom View:

| N | SE (MM) | SD (MM) | E1 (MM) | D1 (MM) | JEDEC (REF) |
|---|---|---|---|---|---|
| 153 | 0.25 BSC. | 0.25 BSC. | 6.50 BSC. | 6.50 BSC. | MO-276 BA |

# 7. ORDERING INFORMATION

| Capacity | MPN (Gold Grade) | Power System | Pin Configuration | Package Size |
|---|---|---|---|---|
| 8GB | FEMC008GBG-T34N | VCCQ: 1.8V/3.3V<br>VCC: 3.3V | 153 FBGA | 11.5x13x1.0 (mm) |
| 16GB | FEMC016GBG-T34N | | | |
| 32GB | FEMC032GBG-T34N | | | |
| 64GB | FEMC064GBG-T34N | | | |
| 128GB | FEMC128GBG-T34N | | | |
| 256GB | FEMC256GBG-T34N | | | |

# Revision History

| Revision | Release Date | History |
|---|---|---|
| 1.0 | 2018/09 | First release |
| 1.1 | 2019/02 | Update VCCQ and performance |
| 1.2 | 2019/05 | Update VCCQ and ordering information |
| 1.3 | 2019/08 | Update Ordering Information |
| 1.4 | 2019/09 | Update Ordering Information |
| 1.5 | 2019/09 | Update Product Specification |
| 1.6 | 2019/10 | Update Product Specification |
| 1.7 | 2020/01 | Update VCCQ for Diamond Grade |
| 1.8 | 2020/03 | Update eMMC Register and ordering information |
| 1.9 | 2020/06 | Update Performance, Power consumption, Pin and signal description. |
| 2.0 | 2020/07 | Add Partition Capacity |
| 2.1 | 2020/10 | Update VCCQ in Power supply |
| 2.2 | 2021/05 | Update Ordering information |
| 2.3 | 2022/01 | Update Product Overview, Specification, and Ordering Information. |
| 2.4 | 2023/03 | Update Product Specification, CSD Register and Ordering Information. |