eSD Memory Card Specification

(pSLC, BGA100)

Version 1.0

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1. GENERAL DESCRIPTION

1.1. Introduction

FLEXXON eSD is compatible with SD Interface and JEDEC 100ball BGA. It provides high data transfer rate, high random IOPS, Power Loss Protection, and read/program disturb management etc. It is designed for high performance, good reliability and wide compatibility. It's well adapted for industrial applications.

1.2. Product Overview

- **Package**
  - 100 ball BGA package
- **Flash**
  - pSLC
- **Capacity**
  - 4GB up to 32GB
- **Support SD system specification version 3.0**
- **Support SD SPI mode**
- **Support Dynamic and Static Wear Leveling**
- **Management of Power Loss Protection**
- **Read disturbance management**
- **Temperature Range**
  - Operation (Gold): -25°C ~ 85°C
  - Operation (Diamond): -40°C ~ 85°C
  - Storage: -50°C ~ 95°C
- **SMART Function**
- **RoHS Compliant**

❖ **Bus Speed Mode**

- **Non-UHS mode**
  - Default speed mode: 3.3V signaling, frequency up to 25MHz, up to 12.5MB/sec
  - High speed mode: 3.3V signaling, frequency up to 50MHz, up to 25MB/sec
- **UHS-I mode**
  - SDR12: SDR up to 25MHz, 1.8V signaling
  - SDR25: SDR up to 50MHz, 1.8V signaling
  - SDR50: 1.8V signaling, frequency up to 100MHz, up to 50 MB/sec
  - SDR104: 1.8V signaling, frequency up to 208MHz, up to 104 MB/sec
  - DDR50: 1.8V signaling, frequency up to 50MHz, sampled on both clock edges, up to 50 MB/sec

1.3. Pseudo SLC

Pseudo SLC can be considered as an extended version of the MLC. While MLC contains both fast and slow pages, pseudo SLC only applies fast pages for programming. The concept of pseudo SLC is demonstrated in the two tables below. The first and second bits of a memory cell represent a fast and slow page respectively, as shown in the left table. Since only fast pages are programmed when applying pseudo SLC, the bits highlighted in red are used, as shown in the right table. Accordingly, because only fast pages are programmed, pseudo SLC provides better performance and endurance than MLC. Moreover, pseudo SLC performs similarly to the SLC, yet pSLC more cost effective.

MLC Flash	
1st bit (fast)	2nd bit (slow)
1	1
1	0
0	1
0	0

Pseudo SLC	
1st bit (fast)	2nd bit (slow)
1	1
1	0
0	1
0	0

2. PRODUCT SPECIFICATIONS

2.1. Performance

Table 2-1 Performance of eSD

Capacity	Sequential	
	Read (MB/s)	Write (MB/s)
4GB	95	50
8GB	95	75
16GB	95	80
32GB	95	80

NOTES:

1. The performance is obtained from TestMetrix Test (@500MB).
2. Samples are made of MLC NAND Flash.
3. Performance may vary from flash configuration and platform.

2.2. Power

Table 2-2 Power Consumption of eSD

Capacity	Read (mA)	Write (mA)	Standby (uA)
4GB	130	100	250
8GB	130	110	250
16GB	135	110	300
32GB	140	120	350

NOTES:

1. Power consumption may vary from flash configuration and platform.

3. INTERFACE DESCRIPTION

3.1. FLEXXON eSD Ball Array

	1	2	3	4	5	6	7	8	9	10	
A	NC	NC							NC	NC	A
B	NC									NC	B
C											C
D		NC	NC	NC	NC	NC	NC	NC	NC		D
E		NC	NC	NC	NC	NC	NC	NC	NC		E
F		VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC		F
G		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS		G
H		VSS	NC	NC	NC	NC	NC	NC	VSS		H
J		NC	NC	NC	NC	NC	NC	NC	NC		J
K		DAT0	DAT2	NC	NC	NC	NC	NC	NC		K
L		NC	VSS	NC	NC	NC	NC	VSS	NC		L
M		NC	NC	VSS	NC	NC	VSS	NC	NC		M
N		DAT1	DAT3	NC	NC	NC	NC	NC	NC		N
P		VSS	NC	NC	CMD	CLK	NC	NC	VSS		P
R											R
T	NC									NC	T
U	NC	NC							NC	NC	U
	1	2	3	4	5	6	7	8	9	10	

Figure 3-1 eSD interface in 100Balls Array (Top View)

3.2. FLEXXON eSD Pin Assignment

Table 3-1 eSD in SD Bus Mode Pin Assignment

eSD in SD Bus Mode			
Ball No.	**Ball Signal**	**Type**	**Description**
K3	DAT2	I/O	Data Line[Bit2]
N3	BD/DAT3	I/O	BGA Detect /Data Line[Bit3]
P5	CMD	PP	Command / Response
VCC	VCC	S	Supply Voltage
P6	CLK	I	Clock
VSS	VSS	S	Supply Voltage Ground
K2	DAT0	I/O	Data Line [Bit 0]
N2	DAT1	I/O	Data Line [Bit 1]

Notes:

1. S: power supply; I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers;
2. The extended DAT Lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used.

Table 3-2 eSD in SD Bus Mode Pin Assignment

eSD in SPI Bus Mode			
Ball No.	**Ball Signal**	**Type**	**Description**
K3	RSV		Reserved
N3	CS	I	Chip Select (neg true)
P5	DI	I	Data In
VCC	VCC	S	Supply Voltage
P6	SCLK	I	Clock
VSS	VSS	S	Supply Voltage Ground
K2	DO	O	Data Out
N2	RSV		Reserved

4. ELECTRICAL SPECIFICATIONS

4.1. Absolute Maximum Rating

Item	Symbol	Parameter	MIN	MAX	Unit
1	V_{DD}	Supply Voltage	2.7	3.6	V
2	T_a	Operating Temperature	-40	+85	℃
3	T_{st}	Storage Temperature	-50	+95	℃

4.2. DC Characteristics

4.2.1. Bus Operation Conditions for 3.3V Signaling

Table 4-1 Threshold Level for High Voltage Range

Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.6	V	
Output High Voltage	V_{OH}	0.75*V_{DD}		V	I_{OH}=-2mA V_{DD} Min
Output Low Voltage	V_{OL}		0.125*V_{DD}	V	I_{OL}=2mA V_{DD} Min
Input High Voltage	V_{IH}	0.625*V_{DD}	V_{DD}+0.3	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3	0.25*V_{DD}	V	
Power Up Time			250	ms	From 0V to V_{DD} min

Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.6	V	
Regulator Voltage	V_{DDIO}	1.7	1.95	V	Generated by V_{DD}
Output High Voltage	V_{OH}	1.4	-	V	I_{OH}=-2mA
Output Low Voltage	V_{OL}	-	0.45	V	I_{OL}=2mA
Input High Voltage	V_{IH}	1.27	2.00	V	
Input Low Voltage	V_{IL}	V_{ss}-0.3	0.58	V	

Parameter	Symbol	Min	Max.	Unit	Remarks
Input Leakage Current		-2	2	uA	DAT3 pull-up is disconnected.

Table 4-2 Peak Voltage and Leakage Current

Parameter	Symbol	Min	Max.	Unit	Remarks
Peak voltage on all lines		-0.3	V_{DD}+0.3	V	
All Inputs					
Input Leakage Current		-10	10	uA	
All Outputs					
Output Leakage Current		-10	10	uA	

4.2.2. Bus Signal Line Load

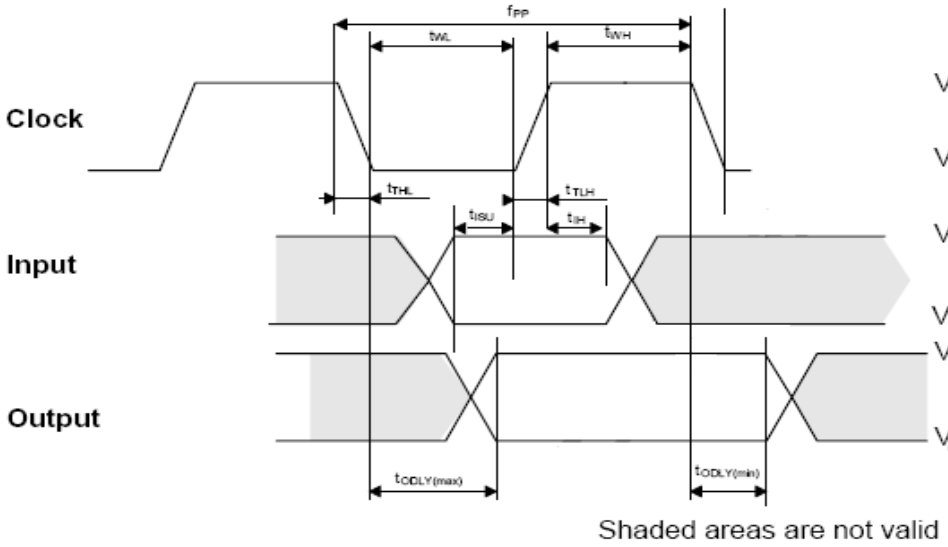
Bus Operation Conditions – Signal Line's Load

Total Bus Capacitance = C_{HOST} + C_{BUS} + N C_{BGA}

Parameter	symbol	Min	Max	Unit	Remark
Pull-up resistance	R_{CMD} R_{DAT}	10	100	kΩ	to prevent bus floating
Total bus capacitance for each signal line	C_L		40	pF	1 BGA C_{HOST}+C_{BUS} shall not exceed 30 pF
BGA Capacitance for each signal pin	C_{BGA}		10[1]	pF	
Maximum signal line inductance			16	nH	
Pull-up resistance inside BGA (pin1)	R_{DAT3}	10	90	kΩ	May be used for BGA detection
Capacity Connected to Power Line	C_C		5	uF	To prevent inrush current

4.3. AC Characteristic

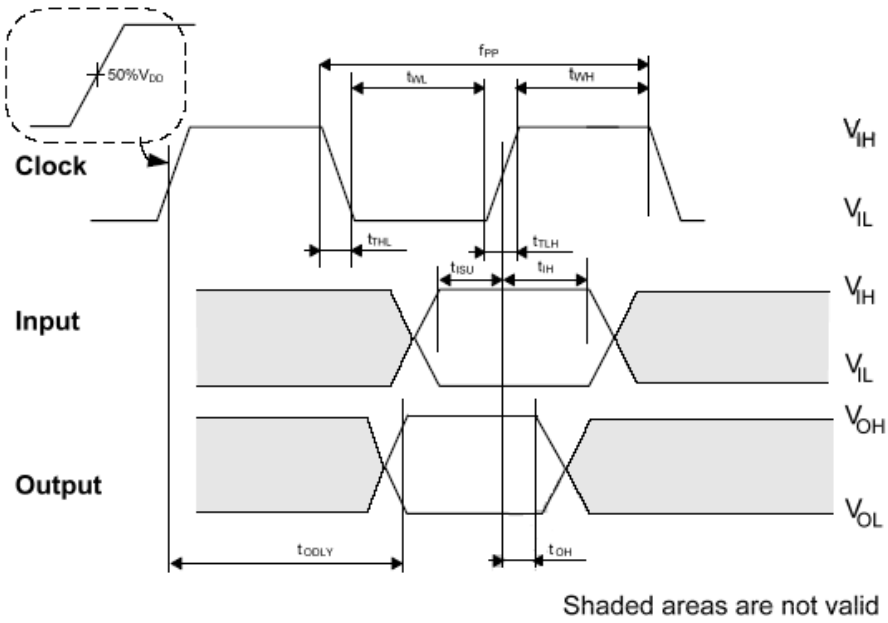
4.3.1. eSD Interface timing (Default)



Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	25	MHz	C_{BGA}≤ 10 pF (1 BGA)
Clock frequency Identification Mode	f_{OD}	0(1)/100	400	KHz	C_{BGA}≤ 10 pF (1 BGA)
Clock low time	t_{WL}	10		ns	C_{BGA}≤ 10 pF (1 BGA)
Clock high time	t_{WH}	10		ns	C_{BGA}≤ 10 pF (1 BGA)
Clock rise time	t_{TLH}		10	ns	C_{BGA}≤ 10 pF (1 BGA)
Clock fall time	t_{THL}		10	ns	C_{BGA}≤ 10 pF (1 BGA)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	C_{BGA}≤ 10 pF (1 BGA)
Input hold time	t_{IH}	5		ns	C_{BGA}≤ 10 pF (1 BGA)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	C_L≤ 40 pF (1 BGA)
Output Delay time during Identification Mode	t_{ODLY}	0	50	ns	C_L≤ 40 pF (1 BGA)

(1) 0Hz means to stop the clock. The given minimum frequency range is for cases where continues clock is required.

4.3.2. eSD Interface Timing (High-Speed Mode)

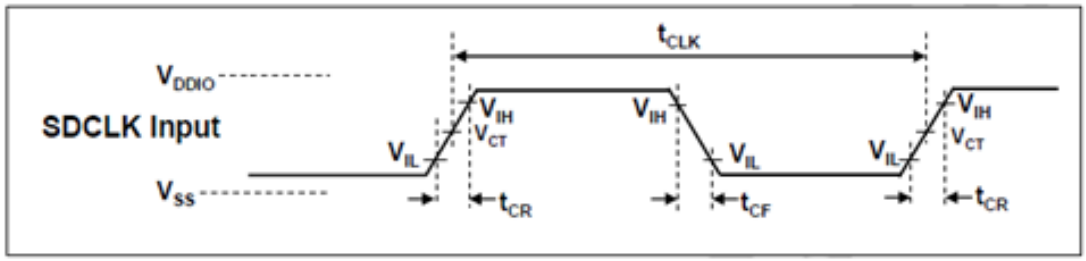


Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	50	MHz	C_{BGA} ≤ 10 pF (1 BGA)
Clock low time	t_{WL}	7		ns	C_{BGA} ≤ 10 pF (1 BGA)
Clock high time	t_{WH}	7		ns	C_{BGA} ≤ 10 pF (1 BGA)
Clock rise time	t_{TLH}		3	ns	C_{BGA} ≤ 10 pF (1 BGA)
Clock fall time	t_{THL}		3	ns	C_{BGA} ≤ 10 pF (1 BGA)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	C_{BGA} ≤ 10 pF (1 BGA)
Input hold time	t_{IH}	2		ns	C_{BGA} ≤ 10 pF (1 BGA)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}		14	ns	C_L ≤ 40 pF (1 BGA)
Output Hold time	T_{OH}	2.5		ns	C_L ≤ 15 pF (1 BGA)
Total System capacitance of each line[1]	C_L		40	pF	CL ≤ 15 pF (1 BGA)

(1) In order to satisfy severe timing, the host shall drive only one BGA.

4.3.3. eSD Interface timing (SDR12, SDR25, SDR50 and SDR104 Modes)

Input:

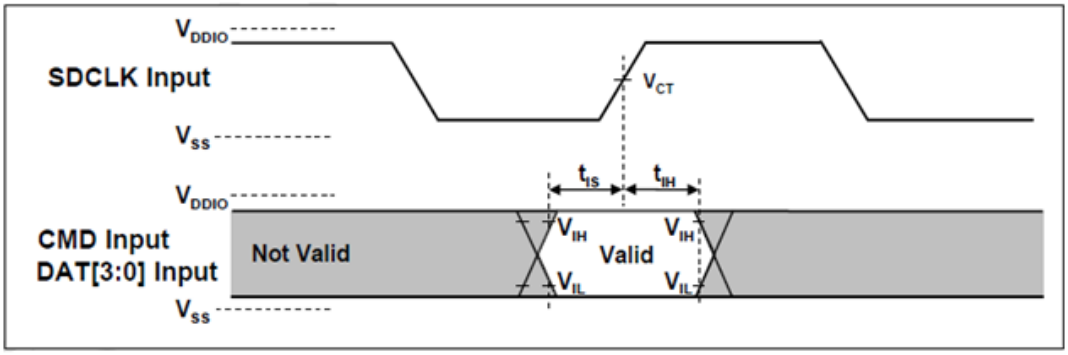


Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	4.80	-	ns	208MHz (Max.), Between rising edge, V_{CT}= 0.975V
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 0.96ns (max.) at 208MHz, C_{BGA}=10pF t_{CR}, t_{CF} < 2.00ns (max.) at 100MHz, C_{BGA}=10pF The absolute maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency
Clock Duty	30	70	%	

Clock Signal Timing

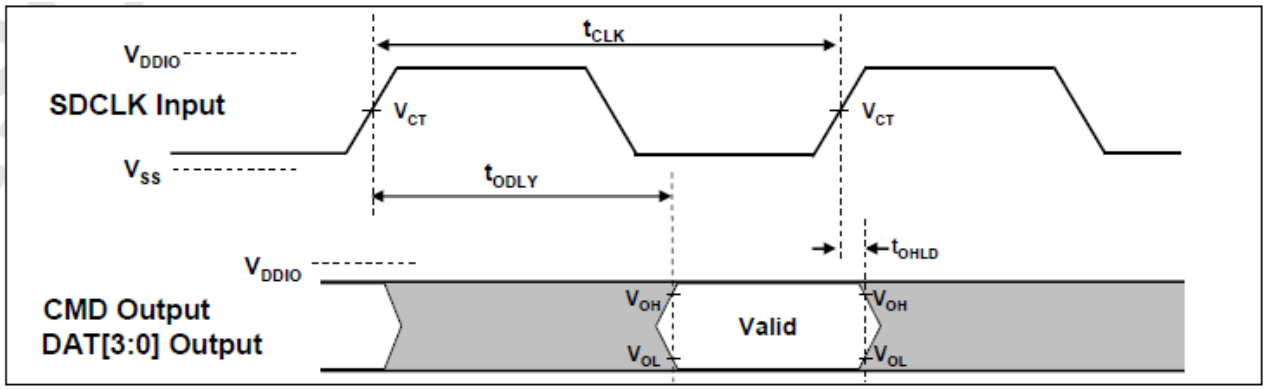
SDR50 and SDR104 Input Timing:



Card Input Timing

Symbol	Min	Max	Unit	SDR104 Mode
t_{IS}	1.40	-	ns	C_{BGA} =10pF, V_{CT}= 0.975V
t_{IH}	0.80	-	ns	C_{BGA} = 5pF, V_{CT}= 0.975V
Symbol	**Min**	**Max**	**Unit**	**SDR50 Mode**
t_{IS}	3.00	-	ns	C_{BGA} =10pF, V_{CT}= 0.975V
t_{IH}	0.80	-	ns	C_{BGA} = 5pF, V_{CT}= 0.975V

Output:

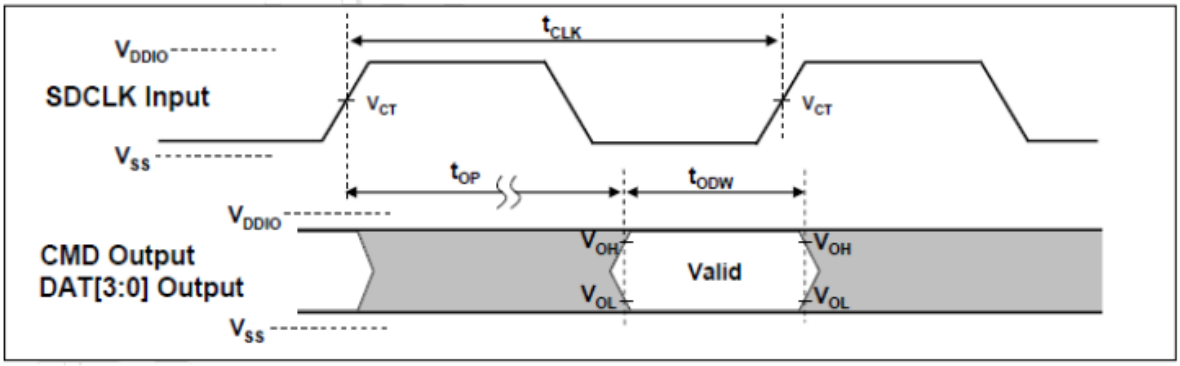


Output Timing of Fixed Data Window

Symbol	Min	Max	Unit	Remark
t_{ODLY}	-	7.5	ns	t_{CLK}>=10.0ns, C_L=30pF, using driver Type B, for SDR50
t_{ODLY}	-	14	ns	t_{CLK}>=20.0ns, C_L=40pF, using driver Type B, for SDR25 and SDR12,
T_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min.), C_L=15pF

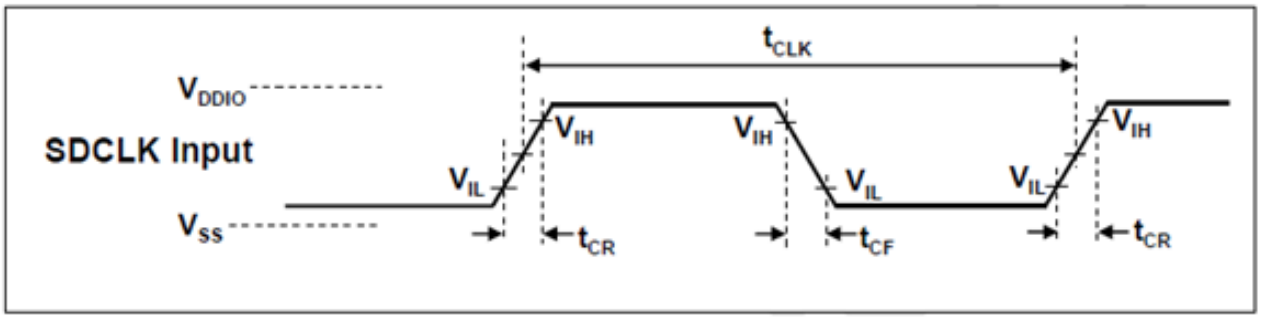
Output Timing of Fixed Data Window

Output (SDR104 Mode):



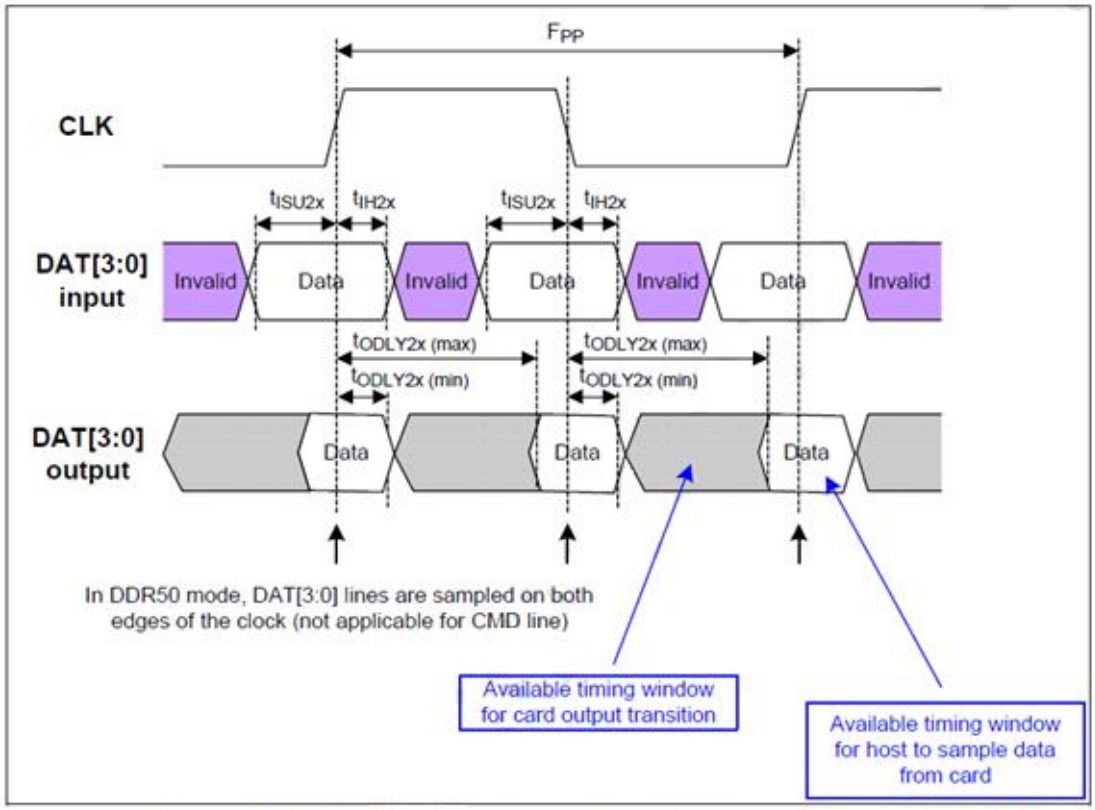
Symbol	Min	Max	Unit	Remark
t_{OP}	0	2	UI	BGA Output Phase
$\triangle t_{OP}$	-350	+1550	ps	Delay variable due to temperature change after tuning
t_{ODW}	0.60	-	UI	t_{ODW} = 2.88ns at 208MHz

4.3.4. eSD Interface timing (DDR50 Modes)



Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	4.8	-	ns	50MHz (Max.), Between rising edge
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 4.00ns (max.) at 50MHz, C_{BGA}=10pF
Clock Duty	45	55	%	



Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

Bus Timings – Parameters Values (DDR50 Mode)

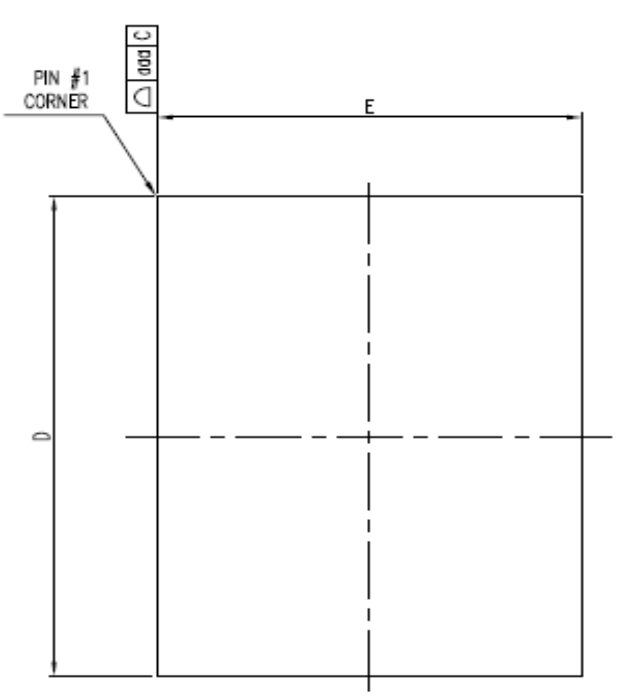
Parameter	Symbol	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input set-up time	t_{ISU}	6	-	ns	C_{BGA}≤ 10 pF (1 BGA)
Input hold time	t_{IH}	0.8	-	ns	C_{BGA}≤ 10 pF (1 BGA)
Output CMD (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode	t_{ODLY}		13.7	ns	C_L≤ 30 pF (1 BGA)
Output Hold time	T_{OH}	1.5	-	ns	C_L≥ 15 pF (1 BGA)
Inputs DAT (referenced to CLK rising and falling edges)					
Input set-up time	t_{ISU2x}	3	-	ns	C_{BGA}≤ 10 pF (1 BGA)
Input hold time	t_{IH2x}	0.8	-	ns	C_{BGA}≤ 10 pF (1 BGA)
Outputs DAT (referenced to CLK rising and falling edges)					
Output Delay time during Data Transfer Mode	t_{ODLY2x}	-	7.0	ns	C_L≤ 25 pF (1 BGA)
Output Hold time	T_{OH2x}	1.5	-	ns	C_L≥ 15 pF (1 BGA)

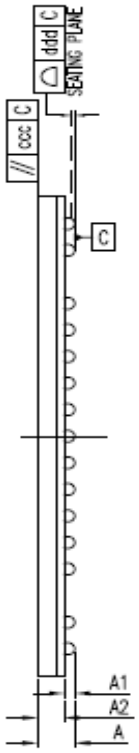
5. PACKAGE

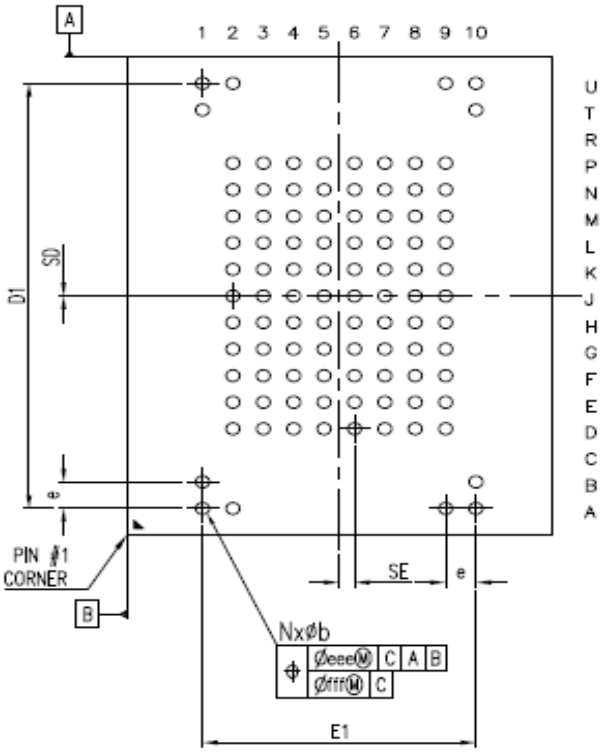
Package Size: 14.0 x 18.0 x 1.4mm

Ball Size: 0.45mm

Ball Pitch: 1.0mm







SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	1.11	1.23	1.35	0.044	0.048	0.053
A1	0.30	0.35	0.40	0.012	0.014	0.016
A2	0.81	0.88	0.95	0.032	0.035	0.037
b	0.40	0.45	0.50	0.016	0.018	0.020
D	17.90	18.00	18.10	0.705	0.709	0.713
E	13.90	14.00	14.10	0.547	0.551	0.555
e	1.00 BSC.			0.039 BSC.		
aaa	0.10					
ccc	0.20					
ddd	0.10					
eee	0.15					
fff	0.10					

N	SE (mm)	SD (mm)	E1 (mm)	D1 (mm)
100	0.50 BSC.	0.00 BSC.	9.00 BSC.	16.00 BSC.

6. ORDERING INFORMATION

Capacity	Part Number (Gold)	Part Number (Diamond)
4GB	FDME004GPG-N230	FDME004GPE-N230
8GB	FDME008GPG-N230	FDME008GPE-N230
16GB	FDME016GPG-N230	FDME016GPE-N230
32GB	FDME032GPG-N230	FDME032GPE-N230

Revision History

Revision	Release Date	Description
1.0	2020/07	First release