e.MMC™ Memory

MTFC32GANALEA-WT, MTFC64GANALAM-WT

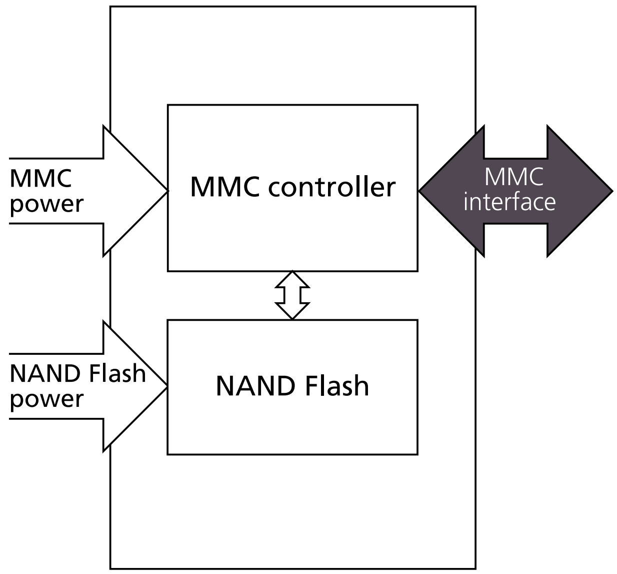
Features

- MultiMediaCard (MMC) controller and NAND Flash
- 153-ball FBGA (RoHS compliant, "green package")
- V_{CCM}: 2.70–3.60V
- V_{CCQM}: 1.70–1.95V
- Temperature ranges
  - Operating temperature: –25˚C to +85˚C[1]
  - Storage temperature: –40˚C to +85˚C

MMC-Specific Features

- JEDEC/MMC standard version 5.1-compliant (JEDEC Standard No. JESD84-B51)[2]
  - Advanced 12-signal interface
  - x1, x4, and x8 I/Os, selectable by host
  - e.MMC I/F boot frequency: 0 to 52 MHz
  - e.MMC I/F clock frequency: 0 to 200 MHz
  - HS200/HS400 modes
  - Real-time clock
  - Command classes: class 0 (basic); class 2 (block read); class 4 (block write); class 5 (erase); class 6 (write protection); class 7 (lock card)
  - Temporary, permanent and power-on write protection
  - Boot operation (high-speed boot)
  - Sleep mode
  - Replay-protected memory block (RPMB)
  - Secure erase and secure trim
  - Hardware reset signal
  - Multiple partitions with enhanced attribute
  - High-priority interrupt (HPI)
  - Background operations

Figure 1: Micron e.MMC Device



MMC-Specific Features (Continued)

  - Packed commands
  - Reliable write
  - Discard and sanitize
  - Extended partitioning
  - Command queueing
  - Context ID; Data TAG
  - Cache
  - Backward compatible with previous MMC
- ECC and block management implemented

Notes: 1. Operating temperature (T_{OPER}) is the case surface temperature on the center/top of the package.
2. The JEDEC specification is available at www.jedec.org/sites/default/files/docs/JESD84-B51.pdf.

Part Numbering Information

Micron® *e*.MMC memory devices are available in different configurations and densities.

Figure 2: e.MMC Part Numbering

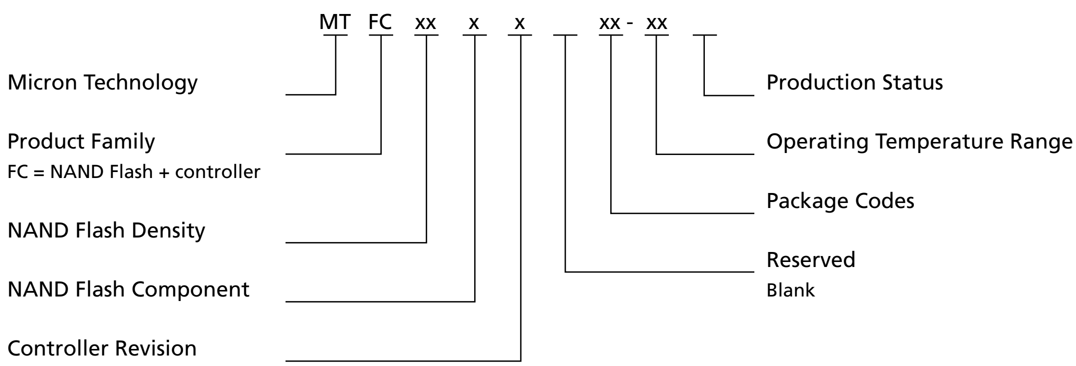


Table 1: Ordering Information

Part Number	Density	Package	Package Code	Shipping
MTFC32GANALEA-WT	32GB	153-ball WFBGA 11.5mm x 13.0mm x 0.8mm	EA	Tray
				Tape and reel
MTFC64GANALAM-WT	64GB	153-ball VFBGA 11.5mm x 13.0mm x 1.0mm	AM	Tray
				Tape and reel

Device Marking

Due to the size of the package, the Micron-standard part number is not printed on the top of the device. Instead, an abbreviated device mark consisting of a 5-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to the Micron part numbers at the FBGA Part Marking Decoder site: www.micron.com/decoder.

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e.MMC Performance and Current Consumption

Table 2: Performance

Condition[1]	Typical Values		Unit
	32GB	64GB	
Sequential write (cache on)	130	200	MB/s
Sequential read	300	300	MB/s
Random write (cache on)	10,000	10,000	IOPS
Random read	10,000	10,000	IOPS

Note: 1. Performances are measured under HS400 mode, with a bus width of 8-bit, cache on, and command queue depth = 4. Chunk size of 512KB for sequential read/write performances and chunk size of 4KB for random read/write performances.

Sequential write performance values are guaranteed as long as the device enters in an idle state longer than a ^{t}IDLE (100s) for each 1GB written.

Additional performance data, such as system performance on a specific application board, will be provided in a separate document upon customer request.

Table 3: Active Current Consumption

Condition	Typical Values (I_{CCM}/I_{CCQM})[1]		Peak Values (I_{CCM}/I_{CCQM})[2]		Unit
	32GB	64GB	32GB	64GB	
Write	30/90	30/90	305/240	425/255	mA
Read	50/200	55/210	240/280	325/280	mA

Notes:
1. Bus in ×8 I/O and HS400 modes. V_{CCM} = 3.6V and V_{CCQM} = 1.95V; T_{OPER} = 25°C. Measurements done as average RMS current consumption. I_{CCQM} in READ operation measurements with tester load disconnected.
2. Bus in ×8 I/O and HS400 modes. V_{CCM} = 3.6V and V_{CCQM} = 1.95V; T_{OPER} = 25°C. Sampling period is 200ps.

Table 4: Low Power Mode

Condition	Typical Values (I_{CCM}/I_{CCQM})[1]		Maximum Values (I_{CCM}/I_{CCQM})[2]		Unit
	32GB	64GB	32GB	64GB	
Standby	60/85	95/85	75/380	115/380	µA
Sleep	55/75	90/85	65/350	110/350	µA

Notes:
1. V_{CCM} = 3.6V and V_{CCQM} = 1.95V; T_{OPER} = 25°C. Measurements done as average current consumption. Not 100% tested.
2. V_{CCM} = 3.6V and V_{CCQM} = 1.95V; T_{OPER} in the range –25°C to +85°C. Not 100% tested.

General Description

Micron e.MMC is a communication and mass data storage device that includes a MultiMediaCard (MMC) interface, a NAND Flash component, and a controller on an advanced 12-signal bus, which is compliant with the MMC system specification. Its low cost, small size, Flash technology independence, and high data throughput make e.MMC ideal for smartphones, digital cameras, PDAs, MP3s, and other portable applications.

The nonvolatile e.MMC draws no power to maintain stored data, delivers high performance across a wide range of operating temperatures, and resists shock and vibration disruption.

Ball Assignments

Figure 3: 153-Ball (Top View, Ball Down)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	NC	NC	DAT0	DAT1	DAT2	V_{SS}	RFU	NC	NC	NC	NC	NC	NC	NC	A
B	NC	DAT3	DAT4	DAT5	DAT6	DAT7	NC	NC	NC	NC	NC	NC	NC	NC	B
C	NC	V_{DDIM}	NC	V_{SS}	NC	V_{CCQM}	NC	NC	NC	NC	NC	NC	NC	NC	C
D	NC	NC	NC	NC								NC	NC	NC	D
E	NC	NC	NC		RFU	V_{CCM}	V_{SS}	NC	VSF2	VSF3		NC	NC	NC	E
F	NC	NC	NC		V_{CCM}					VSF4		NC	NC	NC	F
G	NC	NC	NC		V_{SS}					VSF5		NC	NC	NC	G
H	NC	NC	NC		DS					V_{SS}		NC	NC	NC	H
J	NC	NC	NC		V_{SS}					V_{CCM}		NC	NC	NC	J
K	NC	NC	NC		RST_n	RFU	RFU	V_{SS}	V_{CCM}	VSF6		NC	NC	NC	K
L	NC	NC	NC									NC	NC	NC	L
M	NC	NC	NC	V_{CCQM}	CMD	CLK	NC	NC	NC	NC	NC	NC	NC	NC	M
N	NC	V_{SS}	NC	V_{CCQM}	V_{SS}	NC	NC	NC	NC	NC	NC	NC	NC	NC	N
P	NC	NC	V_{CCQM}	V_{SS}	V_{CCQM}	V_{SS}	NC	NC	NC	VSF7	NC	NC	NC	NC	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Top View (ball down)

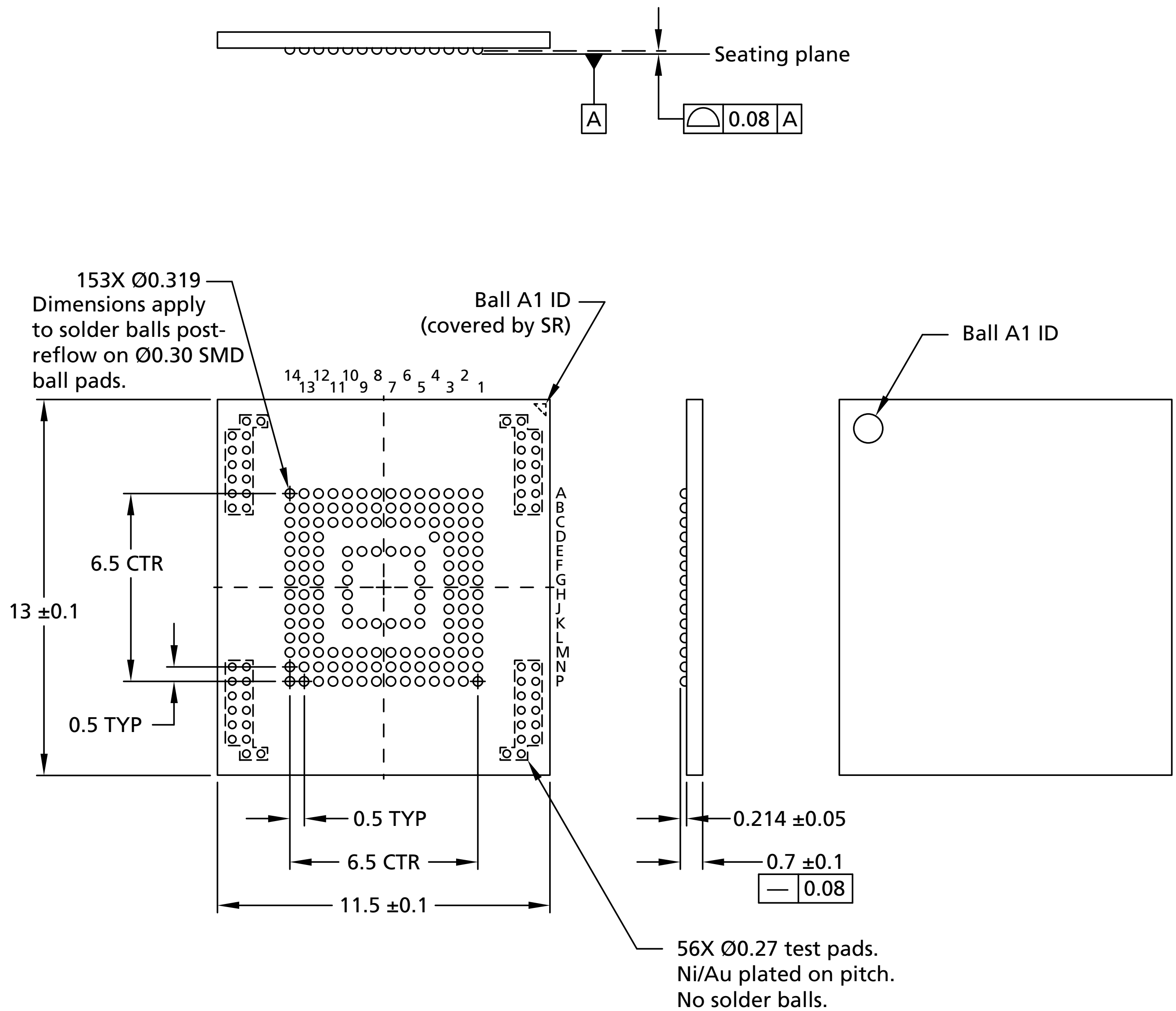
Ball Descriptions

Table 5: e.MMC Ball Descriptions

Symbol	Type	Description
CLK	Input	**Clock:** Each cycle directs a 1-bit transfer on the command and DAT lines.
CMD	Input/ output	**Command:** A bidirectional channel used for device initialization and command transfers. Command has two operating modes: 1) Open drain for initialization 2) Push-pull for fast command transfer
DAT[7:0]	Input/ output	**Data bus:** Bidirectional channel used for data transfer.
RST_n	Input	Reset
DS	Output	**Data strobe:** generated by the device and used for data output and CRC status response output in HS400 mode.
VSF[7:2]	Input/ output	**Vendor specific function:** VSF2, VSF3, VSF4, VSF5, VSF6, and VSF7 are internally connected.
V_{CCM}	Supply	**V_{CCM}:** NAND I/F I/O and NAND power supply (2.70–3.6V).
V_{CCQM}	Supply	**V_{CCQM}:** e.MMC controller core and e.MMC I/F I/O power supply (1.70–1.95V).
V_{DDIM}	–	**V_{DDIM}:** The internal regulator connection to an external decoupling capacitor (see the Capacitor and Resistance Specifications table).
V_{SS}	Supply	Shared ground.
DNU	–	**Do not use:** Must be grounded or left floating.
NC	–	**No connect:** Not internally connected.
RFU	–	Reserved for future use.

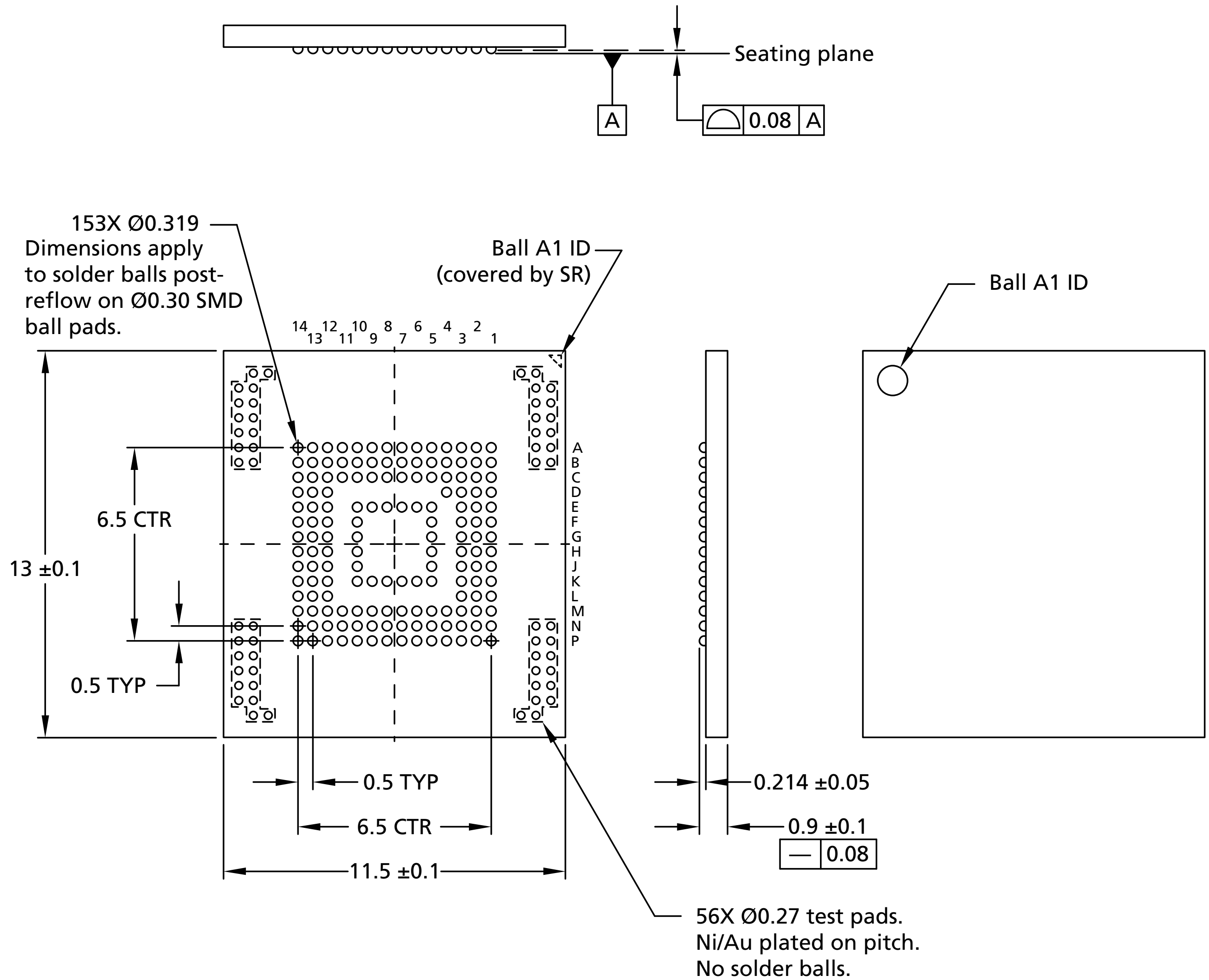
Package Dimensions

Figure 4: 153-Ball WFBGA – 11.5mm x 13.0mm x 0.8mm (Package Code: EA)



Note: 1. Dimensions are in millimeters.

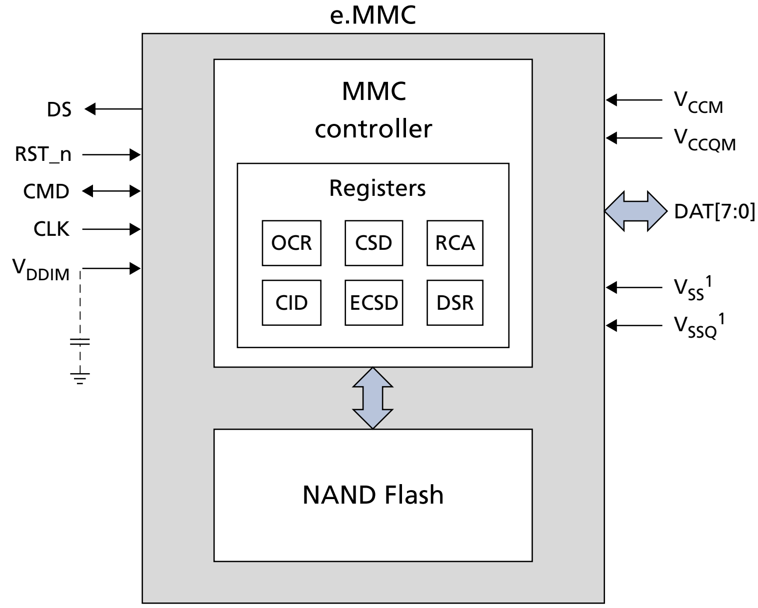
Figure 5: 153-Ball VFBGA – 11.5mm x 13.0mm x 1.0mm (Package Code: AM)



Note: 1. Dimensions are in millimeters.

Architecture

Figure 6: e.MMC Functional Block Diagram



Note: 1. V_{SS} and V_{SSQ} are internally connected.

MMC Protocol Independent of NAND Flash Technology

The MMC specification defines the communication protocol between a host and a device. The protocol is independent of the NAND Flash features included in the device. The device has an intelligent on-board controller that manages the MMC communication protocol.

The controller also handles block management functions such as logical block allocation and wear leveling. These management functions require complex algorithms and depend entirely on NAND Flash technology (generation or memory cell type).

The device handles these management functions internally, making them invisible to the host processor.

Defect and Error Management

Micron e.MMC incorporates advanced technology for defect and error management. If a defective block is identified, the device completely replaces the defective block with one of the spare blocks. This process is invisible to the host and does not affect data space allocated for the user.

The device also includes a built-in error correction code (ECC) algorithm to ensure that data integrity is maintained.

To make the best use of these advanced technologies and ensure proper data loading and storage over the life of the device, the host must exercise the following precautions:

- Check the status after WRITE, READ, and ERASE operations.
- Avoid power-down during WRITE and ERASE operations.

OCR Register

The 32-bit operation conditions register (OCR) stores the voltage profile of the card and the access mode indication. In addition, this register includes a status information bit.

Table 6: OCR Parameters

OCR Bits	OCR Value	Description
[31]	1b (ready)/0b (busy)[1]	Device power-on status bit
[30:29]	10b	Sector mode
[28:24]	0 0000b	Reserved
[23:15]	1 1111 1111b	2.7–3.6V voltage range
[14:8]	000 0000b	2.0–2.7V voltage range
[7]	1b	1.70–1.95V voltage range
[6:0]	000 0000b	Reserved

Note: 1. OCR = C0FF8080h after the device has completed power-up.

CID Register

The card identification (CID) register is 128 bits wide. It contains the device identification information used during the card identification phase as required by *e*.MMC protocol. Each device is created with a unique identification number.

Table 7: CID Register Field Parameters

Name	Field	Width	CID Bits	CID Value	
				32GB	64GB
Manufacturer ID	MID	8	[127:120]	13h	13h
Reserved	–	6	[119:114]	–	–
Card/BGA	CBX	2	[113:112]	01h	01h
OEM/application ID	OID	8	[111:104]	4Eh	4Eh
Product name	PNM	48	[103:56]	53304A333759h	53304A333859h
Product revision	PRV	8	[55:48]	1.0	1.0
Product serial number	PSN	32	[47:16]	–	–
Manufacturing date	MDT	8	[15:8]	–	–
CRC7 checksum	CRC	7	[7:1]	–	–
Not used; always 1	–	1	0	–	–

CSD Register

The card-specific data (CSD) register provides information about accessing the device contents. The CSD register defines the data format, error correction type, maximum data access time, and data transfer speed, as well as whether the DS register can be used. The programmable part of the register (entries marked with W or E in the following table) can be changed by the PROGRAM_CSD (CMD27) command.

Table 8: CSD Register Field Parameters

Name	Field	Size (Bits)	Cell Type[1]	CSD Bits	CSD Value
CSD structure	CSD_STRUCTURE	2	R	[127:126]	03h
System specification version	SPEC_VERS	4	R	[125:122]	04h
Reserved[2]	–	2	–	[121:120]	–
Data read access time 1	TAAC	8	R	[119:112]	5Fh
Data read access time 2 in CLK cycles (NSAC × 100)	NSAC	8	R	[111:104]	01h
Maximum bus clock frequency	TRAN_SPEED	8	R	[103:96]	32h
Card command classes	CCC	12	R	[95:84]	8F5h
Maximum read data block length	READ_BL_LEN	4	R	[83:80]	09h
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79]	0h
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78]	0h
Read block misalignment	READ_BLK_MISALIGN	1	R	[77]	0h
DSR implemented	DSR_IMP	1	R	[76]	1h
Reserved	–	2	–	[75:74]	–
Device size	C_SIZE	12	R	[73:62]	FFFh
Maximum read current at $V_{DD,min}$	VDD_R_CURR_MIN	3	R	[61:59]	07h
Maximum read current at $V_{DD,max}$	VDD_R_CURR_MAX	3	R	[58:56]	07h
Maximum write current at $V_{DD,min}$	VDD_W_CURR_MIN	3	R	[55:53]	07h
Maximum write current at $V_{DD,max}$	VDD_W_CURR_MAX	3	R	[52:50]	07h
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	07h
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	1Fh
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	1Fh
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	0Fh
Write protect group enable	WP_GRP_ENABLE	1	R	[31]	1h
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	00h
Write speed factor	R2W_FACTOR	3	R	[28:26]	05h
Maximum write data block length	WRITE_BL_LEN	4	R	[25:22]	09h
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21]	0h
Reserved	–	4	–	[20:17]	0h
Content protection application	CONTENT_PROT_APP	1	R	[16]	0h
File format group	FILE_FORMAT_GRP	1	R/W	[15]	0h
Copy flag (OTP)	COPY	1	R/W	[14]	0h

Table 8: CSD Register Field Parameters (Continued)

Name	Field	Size (Bits)	Cell Type[1]	CSD Bits	CSD Value
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13]	0h
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12]	0h
File format	FILE_FORMAT	2	R/W	[11:10]	00h
ECC	ECC	2	R/W/E	[9:8]	00h
CRC	CRC	7	R/W/E	[7:1]	–
Reserved	–	1	–	[0]	–

Notes:
1. R = Read-only;
R/W = One-time programmable and readable;
R/W/E = Multiple writable with value kept after a power cycle, assertion of the RST_n signal, and any CMD0 reset, and readable.
2. Reserved bits should be read as "0".

ECSD Register

The 512-byte extended card-specific data (ECSD) register defines device properties and selected modes. The most significant 320 bytes are the properties segment. This segment defines device capabilities and cannot be modified by the host. The lower 192 bytes are the modes segment. The modes segment defines the configuration in which the device is working. The host can change the properties of modes segments using the SWITCH command.

Table 9: ECSD Register Field Parameters

Name	Field	Size (Bytes)	Cell Type[2]	ECSD Bytes	ECSD Value
Properties Segment					
Reserved[3]	–	6	–	[511:506]	–
Extended security commands error	EXT_SECURITY_ERR	1	R	[505]	00h
Supported command sets	S_CMD_SET	1	R	[504]	01h
HPI features	HPI_FEATURES	1	R	[503]	01h
Background operations support	BKOPS_SUPPORT	1	R	[502]	01h
Max packed read commands	MAX_PACKED_READS	1	R	[501]	00h
Max packed write commands	MAX_PACKED_WRITES	1	R	[500]	00h
Data tag support	DATA_TAG_SUPPORT	1	R	[499]	01h
Tag unit size	TAG_UNIT_SIZE	1	R	[498]	03h
Tag resources size	TAG_RES_SIZE	1	R	[497]	00h
Context management capabilities	CONTEXT_CAPABILITIES	1	R	[496]	05h
Large unit size	LARGE_UNIT_SIZE_M1	1	R	[495]	0Bh
Extended partitions attribute support	EXT_SUPPORT	1	R	[494]	03h
Supported modes	SUPPORTED_MODES	1	R	[493]	03h
Field firmware update features	FFU_FEATURES	1	R	[492]	00h
Operation code timeout	OPERATION_CODE_TIMEOUT	1	R	[491]	00h
Field firmware update argument	FFU_ARG	4	R	[490:487]	0000FFFFh
Barrier support	BARRIER_SUPPORT	1	R	[486]	01h
Reserved	–	177	–	[485:309]	–
CMD queuing support	CMDQ_SUPPORT	1	R	[308]	01h
CMD queuing depth	CMDQ_DEPTH	1	R	[307]	1Fh
Reserved	–	1	–	[306]	–
Number of firmware sectors correctly programmed	NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	4	R	[305:302]	00000000h
Vendor proprietary health report	VENDOR_PROPRIETARY_HEALTH_REPORT	32	R	[301:270]	00h

Table 9: ECSD Register Field Parameters (Continued)

Name	Field		Size (Bytes)	Cell Type[2]	ECSD Bytes	ECSD Value
Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B		1	R	[269]	01h
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A		1	R	[268]	01h
Pre end of life information	PRE_EOL_INFO		1	R	[267]	01h
Optimal READ size	OPTIMAL_READ_SIZE		1	R	[266]	01h
Optimal WRITE size	OPTIMAL_WRITE_SIZE		1	R	[265]	08h
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE		1	R	[264]	01h
Device version	DEVICE_VERSION		2	R	[263:262]	–
Firmware version	FIRMWARE_VERSION		8	R	[261:254]	–
Power class for 200MHz, DDR at V_{CC} = 3.6V	PWR_CL_DDR_200_360		1	R	[253]	00h
Cache size	CACHE_SIZE		4	R	[252:249]	00000800h
Generic CMD6 timeout	GENERIC_CMD6_TIME		1	R	[248]	32h
Power-off notification (long) timeout	POWER_OFF_LONG_TIME		1	R	[247]	32h
Background operations status	BKOPS_STATUS		1	R	[246]	00h
Number of correctly programmed sectors	CORRECTLY_PROG_SECTORS_NUM		4	R	[245:242]	00000000h
First initialization time after partitioning	INI_TIMEOUT_AP		1	R	[241]	28h
Cache flushing policy	CACHE_FLUSH_POLICY		1	R	[240]	01h
Power class for 52 MHz, DDR at V_{CC} = 3.6V	PWR_CL_DDR_52_360		1	R	[239]	00h
Power class for 52 MHz, DDR at V_{CC} = 1.95V	PWR_CL_DDR_52_195		1	R	[238]	00h
Power class for 200 MHz, at V_{CCQ} = 1.95V, V_{CC} = 3.6V	PWR_CL_200_195		1	R	[237]	00h
Power class for 200 MHz, at V_{CCQ} = 1.3V, V_{CC} = 3.6V	PWR_CL_200_130		1	R	[236]	00h
Minimum write performance for 8-bit at 52 MHz in DDR mode	MIN_PERF_DDR_W_8_52		1	R	[235]	12h
Minimum read performance for 8-bit at 52 MHz in DDR mode	MIN_PERF_DDR_R_8_52		1	R	[234]	00h
Reserved	–		1	–	[233]	–
TRIM multiplier	TRIM_MULT	32GB	1	R	[232]	11h
		64GB				22h
Secure feature support	SEC_FEATURE_SUPPORT		1	R	[231]	55h
Secure erase multiplier	SEC_ERASE_MULT		1	R	[230]	A0h
Secure trim multiplier	SEC_TRIM_MULT		1	R	[229]	A0h

Table 9: ECSD Register Field Parameters (Continued)

Name	Field		Size (Bytes)	Cell Type[2]	ECSD Bytes	ECSD Value
Boot information	BOOT_INFO		1	R	[228]	07h
Reserved	–		1	–	[227]	–
Boot partition size	BOOT_SIZE_MULT		1	R	[226]	20h
Access size	ACC_SIZE	32GB	1	R	[225]	08h
		64GB				09h
High-capacity erase unit size	HC_ERASE_GRP_SIZE		1	R	[224]	01h
High-capacity erase timeout	ERASE_TIMEOUT_MULT	32GB	1	R	[223]	11h
		64GB				22h
Reliable write-sector count	REL_WR_SEC_C		1	R	[222]	01h
High-capacity write protect group size	HC_WP_GRP_SIZE		1	R	[221]	10h
Sleep current (V_{CC})	S_C_VCC		1	R	[220]	08h
Sleep current (V_{CCQ})	S_C_VCCQ		1	R	[219]	08h
Production state awareness timeout	PRODUCTION_STATE_AWARENESS_TIME-OUT		1	R	[218]	14h
Sleep/awake timeout	S_A_TIMEOUT		1	R	[217]	15h
Sleep notification time	SLEEP_NOTIFICATION_TIME		1	R	[216]	0Fh
Sector count	SEC_COUNT	32GB	4	R	[215:212]	03A3E000h
		64GB				0747C000h
Secure write protect information	SECURE_WP_INFO		1	R	[211]	01h
Minimum write performance for 8-bit at 52 MHz	MIN_PERF_W_8_52		1	R	[210]	0Eh
Minimum read performance for 8-bit at 52 MHz	MIN_PERF_R_8_52		1	R	[209]	08h
Minimum write performance for 8-bit at 26 MHz and 4-bit at 52 MHz	MIN_PERF_W_8_26_4_52		1	R	[208]	10h
Minimum read performance for 8-bit at 26 MHz and 4-bit at 52 MHz	MIN_PERF_R_8_26_4_52		1	R	[207]	08h
Minimum write performance for 4-bit at 26 MHz	MIN_PERF_W_4_26		1	R	[206]	12h
Minimum read performance for 4-bit at 26 MHz	MIN_PERF_R_4_26		1	R	[205]	08h
Reserved	–		1	–	[204]	–
Power class for 26 MHz at 3.6V	PWR_CL_26_360		1	R	[203]	00h
Power class for 52 MHz at 3.6V	PWR_CL_52_360		1	R	[202]	00h
Power class for 26 MHz at 1.95V	PWR_CL_26_195		1	R	[201]	00h
Power class for 52 MHz at 1.95V	PWR_CL_52_195		1	R	[200]	00h

Table 9: ECSD Register Field Parameters (Continued)

Name	Field	Size (Bytes)	Cell Type[2]	ECSD Bytes	ECSD Value
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	01h
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	FFh
I/O driver strength	DRIVER_STRENGTH	1	R	[197]	1Fh
Device type	DEVICE_TYPE	1	R	[196]	57h
Reserved	–	1	–	[195]	–
CSD structure	CSD_STRUCTURE	1	R	[194]	02h
Reserved	–	1	–	[193]	–
Extended CSD revision	EXT_CSD_REV	1	R	[192]	08h
Modes Segment					
Command set	CMD_SET	1	R/W/E_P	[191]	00h
Reserved	–	1	–	[190]	–
Command set revision	CMD_SET_REV	1	R	[189]	00h
Reserved	–	1	–	[188]	–
Power class	POWER_CLASS	1	R/W/E_P	[187]	00h
Reserved	–	1	–	[186]	–
High-speed interface timing	HS_TIMING	1	R/W/E_P	[185]	00h
Strobe support	STROBE_SUPPORT	1	R	[184]	01h
Bus width mode	BUS_WIDTH	1	W/E_P	[183]	00h
Reserved	–	1	–	[182]	–
Erased memory content	ERASED_MEM_CONT	1	R	[181]	00h
Reserved	–	1	–	[180]	–
Partition configuration	PARTITION_CONFIG	1	R/W/E, R/W/E_P	[179]	00h
Boot configuration protection	BOOT_CONFIG_PROT	1	R/W, R/W/C_P	[178]	00h
Boot bus conditions	BOOT_BUS_CONDITIONS	1	R/W/E	[177]	00h
Reserved	–	1	–	[176]	–
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E_P	[175]	00h
Boot write protection status registers	BOOT_WP_STATUS	1	R	[174]	00h
Boot area write protection register	BOOT_WP	1	R/W, R/W/C_P	[173]	00h
Reserved	–	1	–	[172]	–
User area write protection register	USER_WP	1	R/W, R/W/C_P, R/W/E_P	[171]	00h
Reserved	–	1	–	[170]	–
Firmware configuration	FW_CONFIG	1	R/W	[169]	00h

Table 9: ECSD Register Field Parameters (Continued)

Name	Field	Size (Bytes)	Cell Type[2]	ECSD Bytes	ECSD Value
RPMB size	RPMB_SIZE_MULT	1	R	[168]	20h
Write reliability setting register[4]	WR_REL_SET	1	R/W	[167]	1Fh
Write reliability parameter register	WR_REL_PARAM	1	R	[166]	15h
Start sanitize operation	SANITIZE_START	1	W/E_P	[165]	00h
Manually start background operations	BKOPS_START	1	W/E_P	[164]	00h
Enable background operations handshake	BKOPS_EN	1	R/W	[163]	02h
Hardware RESET function	RST_n_FUNCTION	1	R/W	[162]	00h
HPI management	HPI_MGMT	1	R/W/E_P	[161]	00h
Partitioning support	PARTITIONING_SUPPORT	1	R	[160]	07h
Max enhanced area size	MAX_ENH_SIZE_MULT 32GB	3	R	[159:157]	0004DAh
	MAX_ENH_SIZE_MULT 64GB				0009B4h
Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	[156]	00h
Partitioning setting	PARTITION_SETTING_COMPLETED	1	R/W	[155]	00h
General-purpose partition size	GP_SIZE_MULT_GP3	12	R/W	[154:152]	000000h
	GP_SIZE_MULT_GP2			[151:149]	000000h
	GP_SIZE_MULT_GP1			[148:146]	000000h
	GP_SIZE_MULT_GP0			[145:143]	000000h
Enhanced user data area size	ENH_SIZE_MULT	3	R/W	[142:140]	000000h
Enhanced user data start address	ENH_START_ADDR	4	R/W	[139:136]	00000000h
Reserved	–	1	–	[135]	–
Bad block management mode	SEC_BAD_BLK_MGMNT	1	R/W	[134]	00h
Production state awareness	PRODUCTION_STATE_AWARENESS	1	R/W/E	[133]	00h
Package case temperature is controlled	TCASE_SUPPORT	1	W/E_P	[132]	00h
Periodic wake-up	PERIODIC_WAKEUP	1	R/W/E	[131]	00h
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_SUPPORT	1	R	[130]	01h
Reserved	–	2	–	[129:128]	–
Vendor specific fields	VENDOR_SPECIFIC_FIELD	64	<vendor specific>	[127:64]	–
Native sector size	NATIVE_SECTOR_SIZE	1	R	[63]	00h
Sector size emulation	USE_NATIVE_SECTOR	1	R/W	[62]	00h
Sector size	DATA_SECTOR_SIZE	1	R	[61]	00h
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	R	[60]	00h

Table 9: ECSD Register Field Parameters (Continued)

Name	Field	Size (Bytes)	Cell Type[2]	ECSD Bytes	ECSD Value
Class 6 commands control	CLASS_6_CTRL	1	R/W/E_P	[59]	00h
Number of addressed group to be released	DYNCAP_NEEDED	1	R	[58]	00h
Exception events control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	[57:56]	0000h
Exception events status	EXCEPTION_EVENTS_STATUS	2	R	[55:54]	0000h
Extended partitions attribute	EXT_PARTITIONS_ATTRIBUTE	2	R/W	[53:52]	0000h
Context configuration	CONTEXT_CONF ID#15	15	R/W/E_P	[51]	00h
	CONTEXT_CONF ID#14			[50]	00h
	CONTEXT_CONF ID#13			[49]	00h
	CONTEXT_CONF ID#12			[48]	00h
	CONTEXT_CONF ID#11			[47]	00h
	CONTEXT_CONF ID#10			[46]	00h
	CONTEXT_CONF ID#9			[45]	00h
	CONTEXT_CONF ID#8			[44]	00h
	CONTEXT_CONF ID#7			[43]	00h
	CONTEXT_CONF ID#6			[42]	00h
	CONTEXT_CONF ID#5			[41]	00h
	CONTEXT_CONF ID#4			[40]	00h
	CONTEXT_CONF ID#3			[39]	00h
	CONTEXT_CONF ID#2			[38]	00h
	CONTEXT_CONF ID#1			[37]	00h
Packed command status	PACKED_COMMAND_STATUS	1	R	[36]	00h
Packed command failure index	PACKED_FAILURE_INDEX	1	R	[35]	00h
Power-off notification	POWER_OFF_NOTIFICATION	1	R/W/E_P	[34]	00h
Control to turn the cache on/off	CACHE_CTRL	1	R/W/E_P	[33]	00h
Flushing of the cache	FLUSH_CACHE	1	W/E_P	[32]	00h
Control to turn the barrier on/off	BARRIER_CTRL	1	R/W	[31]	00h
Mode configuration	MODE_CONFIG	1	R/W/E_P	[30]	00h
Mode operation codes	MODE_OPERATION_CODES	1	W/E_P	[29]	00h
Reserved	–	2	–	[28:27]	–
Field firmware update status	FFU_STATUS	1	R	[26]	00h
Pre-loading data size	PRE_LOADING_DATA_SIZE	4	R/W/E_P	[25:22]	00000000h
Maximum pre-loading data size	MAX_PRE_LOADING_DATA_SIZE 32GB	4	R	[21:18]	01342000h
	64GB				02684000h
Product state awareness enablement	PRODUCT_STATE_AWARENESS_ENABLEMENT	1	R/W/E & R	[17]	01h
Secure removal type	SECURE_REMOVAL_TYPE	1	R/W/E & R	[16]	01h

Table 9: ECSD Register Field Parameters (Continued)

Name	Field	Size (Bytes)	Cell Type[2]	ECSD Bytes	ECSD Value
Command queue mode enable	CMDQ_MODE_EN	1	R/W/E_P	[15]	00h
Reserved	–	15	–	[14:0]	–

Notes:
1. Some of the register values in this table might be subject to change. Updated values will be provided upon customer request.
2. R = Read-only;
   R/W = One-time programmable and readable;
   R/W/E = Multiple writable with the value kept after a power cycle, assertion of the RST_n signal, and any CMD0 reset, and readable;
   R/W/C_P = Writable after the value is cleared by a power cycle and assertion of the RST_n signal (the value not cleared by CMD0 reset) and readable;
   R/W/E_P = Multiple writable with the value reset after a power cycle, assertion of the RST_n signal, and any CMD0 reset, and readable;
   W/E_P = Multiple writable with the value reset after power cycle, assertion of the RST_n signal, and any CMD0 reset, and not readable
3. Reserved bits should be read as 0.
4. Micron has tested power failure under best-application knowledge conditions with positive results. Customers may request a dedicated test for their specific application condition. Micron set this register during factory test and used the one-time programming option.
5. It is recommended to issue a power-off notification when pre-programming the device.
6. EXT_CSD [235:234] and [210:205] fields values are "Don't Care."

DC Electrical Specifications – Device Power

The device current consumption for various device configurations is defined in the power class fields of the ECSD register.

V_{CCM} is used for the NAND Flash device and its interface voltage; V_{CCQM} is used for the controller and the e.MMC interface voltage.

Figure 7: Device Power Diagram

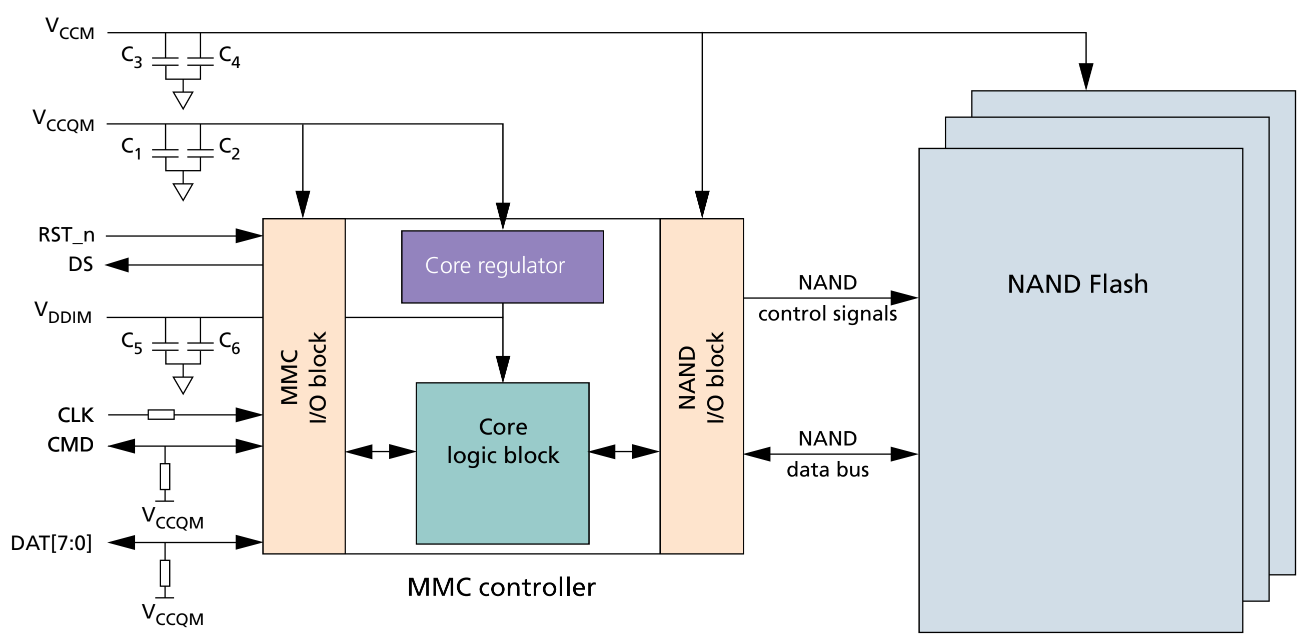


Table 10: Power Domains

Parameter	Symbol	Comments
Host interface	V_{CCQM}	Low voltage range = 1.8V (nominal)
Memory	V_{CCM}	High voltage range = 3.3V (nominal)
Internal	V_{DDIM}	The internal regulator connection to an external decoupling capacitor

Table 11: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage[1]	V_{CCM}	2.70	3.30	3.60	V
I/O supply voltage[1]	V_{CCQM}	1.70	1.80	1.95	V
Operating temperature range	T_{OPER}	–25	–	+85	°C

Note: 1. AC noise should not exceed ±3% of typical supply voltages (10 kHz to 800 MHz). The overall AC and DC noise on supply voltages should be within the minimum/maximum range specified in this table.

Table 12: Capacitor and Resistance Specifications

Parameter	Symbol	Min	Max	Typ	Units	Notes
Pull-up resistance: CMD	R_CMD	4.7	50	10	kΩ	1
Pull-up resistance: DAT[7:0]	R_DAT	10	50	50	kΩ	1
Pull-up resistance: RST_n	R_RST_n	4.7	50	50	kΩ	2
CLK/CMD/DAT[7:0] impedance		45	55	50	Ω	3
Serial resistance on CLK	SR_CLK	0	47	22	Ω	
Pull-down resistance: DS	R_DS	10	100	–	kΩ	
V_{CCQM} capacitor	C1	2.2	4.7	2.2	µF	4
	C2	0.1	0.22	0.1		
V_{CCM} capacitor	C3	2.2	4.7	2.2	µF	5
	C4	0.1	0.22	0.1		
V_{DDIM} capacitor (C_{reg})	C5	1	4.7	1	µF	6
	C6	0.1	0.1	0.1		

Notes:
1. Used to prevent bus floating.
2. If host does not use H/W RESET (RST_n), pull-up resistance is not needed on RST_n line (Extended_CSD[162] = 00h).
3. Impedance match.
4. The coupling capacitor should be connected with V_{CCQM} and V_{SSQ} as closely as possible.
5. The coupling capacitor should be connected with V_{CCM} and V_{SS} as closely as possible.
6. The coupling capacitor should be connected with V_{DDIM} and V_{SS} as closely as possible.

Revision History

Rev. D – 10/17

- Added Recommended Operating Conditions table

Rev. C – 09/17

- Updated operating temperature range
- Updated Current Consumption tables

Rev. B – 06/17

- Updated legal status to Production
- Updated notes to the Performance table
- Updated Current Consumption table
- Updated ECSD Register

Rev. A – 02/17

- Initial release

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