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Spartan 7 FPGAs Data Sheet: DC and AC Switching Characteristics (DS189)

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Spartan 7 FPGAs Data Sheet: DC and AC Switching Characteristics

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Spartan 7 FPGAs Data Sheet: DC and AC Switching Characteristics (DS189)

Spartan 7 FPGAs Data Sheet: DC and AC Switching Characteristics

	Spartan 7 FPGAs Data Sheet: DC and AC Switching Characteristics
	Product Specification

Introduction

Spartan™ 7 FPGAs are available in -2, -1, and -1L speed grades, with -2 having the highest performance. The Spartan 7 FPGAs predominantly operate at a 1.0V core voltage. The -1L devices are screened for lower maximum static power and can operate at lower core voltages for lower dynamic power than the -1 devices. The -1L devices operate only at $V_{CCINT} = V_{CCBRAM} = 0.95V$ and have the same speed specifications as the -1 speed grade.

Spartan 7 FPGA DC and AC characteristics are specified in commercial (C), industrial (I), and expanded (Q) temperature ranges. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1Q expanded speed grade device are the same as for a -1C commercial speed grade device). However, only selected speed grades and/or devices are available in each temperature range. For example, the -1L speed grade is only available in the industrial (I) temperature range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

Available device and package combinations can be found in:

- 7 Series FPGAs Overview (DS180) [Ref 1]
- XA Spartan 7 Automotive FPGA Data Sheet: Overview (DS171) [Ref 2]

This Spartan 7 FPGA data sheet, part of an overall [HTTP URL](http://docs.amd.com) documentation on the 7 series FPGAs, is available on the Xilinx website at <http://docs.amd.com>.

DC Characteristics

Table 1: Absolute Maximum Ratings(1)

Symbol	Description	Min	Max	Units
FPGA Logic				
V_{CCINT}	Internal supply voltage.	-0.5	1.1	V
V_{CCAUX}	Auxiliary supply voltage.	-0.5	2.0	V
V_{CCBRAM}	Supply voltage for the block RAM memories.	-0.5	1.1	V

Symbol	Description	Min	Max	Units
V_{CCO}	Output drivers supply voltage for HR I/O banks.	-0.5	3.6	V
V_{REF}	Input reference voltage.	-0.5	2.0	V
$V_{IN(2)(3)(4)}$	I/O input voltage.	-0.4	$V_{CCO} + 0.55$	V
	I/O input voltage (when $V_{CCO} = 3.3V$) for V_{REF} and differential I/O standards except TMD5_33.(5)	-0.4	2.625	V
V_{CCBATT}	Key memory battery backup supply.	-0.5	2.0	V

Symbol	Description	Min	Max	Units
XADC				
V_{CCADC}	XADC supply relative to GNDADC.	-0.5	2.0	V
V_{REFP}	XADC reference input relative to GNDADC.	-0.5	2.0	V
Temperature				
T_{STG}	Storage temperature (ambient).	-65	150	°C

Symbol	Description	Min	Max	Units
T_{SOL}	Maximum soldering temperature for Pb/Sn component bodies.(6)	–	+220	°C
	Maximum soldering temperature for Pb-free component bodies.(6)	–	+260	°C
T_j	Maximum junction temperature. (6)	–	+125	°C

Symbol	Description	Min	Max	Units
Notes:				
<p>1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.</p> <p>2. The lower absolute voltage specification always applies.</p> <p>3. For I/O operation, refer to the 7 Series FPGAs SelectIO Resources User Guide (UG471) [Ref 3].</p> <p>4. The maximum limit applies to DC signals. For maximum undershoot and overshoot AC specifications, see Table: VIN Maximum Allowed AC Voltage Overshoot and Undershoot for HR I/O Banks(1)(2).</p> <p>5. See Table: Differential SelectIO DC Input and Output Levels for TMD5_33 specifications.</p> <p>6. For soldering guidelines and thermal considerations, see the 7 Series FPGA Packaging and Pinout Specification (UG475) [Ref 4].</p>				

Table 2: [Recommended Operating Conditions\(1\)\(2\)](#)

Symbol	Description	Min	Typ	Max	Units
FPGA Logic					

Symbol	Description	Min	Typ	Max	Units
$V_{CCINT(3)}$	For -2 and -1 (1.0V) devices: internal supply voltage.	0.95	1.00	1.05	V
	For -1L (0.95V) devices: internal supply voltage.	0.92	0.95	0.98	V
V_{CCAUX}	Auxiliary supply voltage.	1.71	1.80	1.89	V

Symbol	Description	Min	Typ	Max	Units
V_{CCBRAM} (3)	For -2 and -1 (1.0V) devices: block RAM supply voltage.	0.95	1.00	1.05	V
	For -1L (0.95V) devices: block RAM supply voltage.	0.92	0.95	0.98	V
V_{CCO} (4)(5)	Supply voltage for HR I/O banks.	1.14	–	3.465	V

Symbol	Description	Min	Typ	Max	Units
$V_{IN(6)}$	I/O input voltage.	-0.20	-	$V_{CCO} + 0.20$	V
	I/O input voltage (when $V_{CCO} = 3.3V$) for V_{REF} and differential I/O standards except TMDS_33. (7)	-0.20	-	2.625	V
$I_{IN(8)}$	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	-	-	10	mA

Symbol	Description	Min	Typ	Max	Units
$V_{CCBATT(9)}$	Battery voltage.	1.0	–	1.89	V
XADC					
V_{CCADC}	XADC supply relative to GNDADC.	1.71	1.80	1.89	V
V_{REFP}	Externally supplied reference voltage.	1.20	1.25	1.30	V
Temperature					

Symbol	Description	Min	Typ	Max	Units
T_j	Junction temperature operating range for commercial (C) temperature devices.	0	–	85	°C
	Junction temperature operating range for industrial (I) temperature devices.	–40	–	100	°C

Symbol	Description	Min	Typ	Max	Units
	Junction temperature operating range for expanded (Q) temperature devices.	-40	-	125	°C

Symbol	Description	Min	Typ	Max	Units
Notes:					
1. All voltages are relative to ground.					
2. For the design of the power distribution system consult the 7 Series FPGAs PCB Design Guide (UG483) [Ref 5].					
3. If V_{CCINT} and V_{CCBRAM} are operating at the same voltage, V_{CCINT} and V_{CCBRAM} should be connected to the same supply.					
4. Configuration data is retained even if V_{CCO} drops to 0V.					
5. Includes V_{CCO} of 1.2V, 1.35V, 1.5V, 1.8V, 2.5V, and 3.3V at $\pm 5\%$.					
6. The lower absolute voltage specification always applies.					
7. See Table: Differential SelectIO DC Input and Output Levels for TMDS_33 specifications.					
8. A total of 200 mA per bank should not be exceeded.					
9. V_{CCBATT} is required only when using bitstream encryption. If battery is not used, connect V_{CCBATT} to either ground or V_{CCAUX} .					

Table 3: DC Characteristics Over Recommended Operating Conditions

Symbol	Description	Min	Typ (1)	Max	Units
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Symbol	Description	Min	T _{vp} (1)	Max	Units
V _{DRINT}	Data retention V _{CCINT} voltage (below which configuration data might be lost).	0.75	–	–	V
V _{DRI}	Data retention V _{CCAUX} voltage (below which configuration data might be lost).	1.5	–	–	V
I _{REF}	V _{REF} leakage current per pin.	–	–	15	μA

Symbol	Description	Min	T _{vd} (1)	Max	Units
I _L	Input or output leakage current per pin (sample-tested).	–	–	15	μA
C _{IN} (2)	Die input capacitance at the pad.	–	–	8	pF

Symbol	Description	Min	T _{vd} (1)	Max	Units
I _{RPU}	Pad pull-up (when selected) at V _{IN} = 0V, V _{CC0} = 3.3V.	90	–	330	μA
	Pad pull-up (when selected) at V _{IN} = 0V, V _{CC0} = 2.5V.	68	–	250	μA
	Pad pull-up (when selected) at V _{IN} = 0V, V _{CC0} = 1.8V.	34	–	220	μA
	Pad pull-up (when selected) at V _{IN} = 0V, V _{CC0} = 1.5V.	23	–	150	μA

Symbol	Description	Min	T _{vp} (1)	Max	Units
	Pad pull-up (when selected) at V _{IN} = 0V, V _{CC0} = 1.2V.	12	–	120	μA
I _{RPD}	Pad pull-down (when selected) at V _{IN} = 3.3V.	68	–	330	μA
I _{CCADC}	Analog supply current, analog circuits in powered up state.	–	–	25	mA
I _{BATT} (3)	Battery supply current.	–	–	150	nA

Symbol	Description	Min	T_{vd} (1)	Max	Units
$R_{IN_TERM(4)}$	Thevenin equivalent resistance of programmable input termination to $V_{CC0}/2$ (UNTUNED_SPLIT_40).	28	40	55	W
	Thevenin equivalent resistance of programmable input termination to $V_{CC0}/2$ (UNTUNED_SPLIT_50).	35	50	65	W

Symbol	Description	Min	V_D (1)	Max	Units
	Thevenin equivalent resistance of programmable input termination to $V_{CC0}/2$ (UNTUNE_D_SPLIT_60).	44	60	83	W
n	Temperature diode ideality factor.	–	1.010	–	–
r	Temperature diode series resistance.	–	2	–	W

Symbol	Description	Min	T_{vd} (1)	Max	Units
Notes:					
1. Typical values are specified at nominal voltage, 25°C.					
2. This measurement represents the die capacitance at the pad, not including the package.					
3. Maximum value specified for worst case process at 25°C.					
4. Termination resistance to a $V_{CCO}/2$ level.					

Table 4: V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HR I/O Banks(1)(2)

AC Voltage Overshoot	% of UI at – 40°C to 125°C	AC Voltage Undershoot	% of UI at – 40°C to 125°C
$V_{CCO} + 0.55$	100	-0.40	100
		-0.45	61.7
		-0.50	25.8
		-0.55	11.0

AC Voltage Overshoot	% of UI at – 40°C to 125°C	AC Voltage Undershoot	% of UI at – 40°C to 125°C
$V_{CCO} + 0.60$	46.6	–0.60	4.77
$V_{CCO} + 0.65$	21.2	–0.65	2.10
$V_{CCO} + 0.70$	9.75	–0.70	0.94
$V_{CCO} + 0.75$	4.55	–0.75	0.43
$V_{CCO} + 0.80$	2.15	–0.80	0.20
$V_{CCO} + 0.85$	1.02	–0.85	0.09
$V_{CCO} + 0.90$	0.49	–0.90	0.04
$V_{CCO} + 0.95$	0.24	–0.95	0.02

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. The peak voltage of the overshoot or undershoot, and the duration above $V_{CCO} + 0.20V$ or below $GND - 0.20V$, must not exceed the values in this table.

I _{CCIN} TQ	Quiet scen t V _{CCI} NT supp ly curre nt.	XC7 S6	36	36	36	36	36	32	mA
		XC7 S15	36	36	36	36	36	32	mA
		XC7 S25	48	48	48	48	48	43	mA
		XC7 S50	95	95	95	95	95	59	mA
		XC7 S75	148	148	148	148	148	134	mA
		XC7 S100	148	148	148	148	148	134	mA
		XA7 S6	N/A	36	N/A	36	36	N/A	mA
		XA7 S15	N/A	36	N/A	36	36	N/A	mA
		XA7 S25	N/A	48	N/A	48	48	N/A	mA

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		XA7 S50	N/A	95	N/A	95	95	N/A	mA
		XA7 S75	N/A	148	N/A	148	148	N/A	mA
		XA7 S100	N/A	148	N/A	148	148	N/A	mA

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I _{CCO} Q	Quiescent V _{CC} supply current.	XC7 S6	1	1	1	1	1	1	mA
		XC7 S15	1	1	1	1	1	1	mA
		XC7 S25	1	1	1	1	1	1	mA
		XC7 S50	1	1	1	1	1	1	mA
		XC7 S75	4	4	4	4	4	4	mA
		XC7 S100	4	4	4	4	4	4	mA
		XA7 S6	N/A	1	N/A	1	1	N/A	mA
		XA7 S15	N/A	1	N/A	1	1	N/A	mA
		XA7 S25	N/A	1	N/A	1	1	N/A	mA

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		XA7 S50	N/A	1	N/A	1	1	N/A	mA
		XA7 S75	N/A	4	N/A	4	4	N/A	mA
		XA7 S100	N/A	4	N/A	4	4	N/A	mA

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I _{CCA} UXQ	Quiet scen t V _{CC} AUX supp ly curre nt.	XC7 S6	10	10	10	10	10	10	mA
		XC7 S15	10	10	10	10	10	10	mA
		XC7 S25	13	13	13	13	13	13	mA
		XC7 S50	22	22	22	22	22	20	mA
		XC7 S75	43	43	43	43	43	43	mA
		XC7 S100	43	43	43	43	43	43	mA
		XA7 S6	N/A	10	N/A	10	10	N/A	mA
		XA7 S15	N/A	10	N/A	10	10	N/A	mA
		XA7 S25	N/A	13	N/A	13	13	N/A	mA

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		XA7 S50	N/A	22	N/A	22	22	N/A	mA
		XA7 S75	N/A	43	N/A	43	43	N/A	mA
		XA7 S100	N/A	43	N/A	43	43	N/A	mA

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I _{CCB} RAM Q	Quiet scen t V _{CC} BRA M supp ly curre nt.	XC7 S6	1	1	1	1	1	1	mA
		XC7 S15	1	1	1	1	1	1	mA
		XC7 S25	1	1	1	1	1	1	mA
		XC7 S50	2	2	2	2	2	1	mA
		XC7 S75	9	9	9	9	9	8	mA
		XC7 S100	9	9	9	9	9	8	mA
		XA7 S6	N/A	1	N/A	1	1	N/A	mA
		XA7 S15	N/A	1	N/A	1	1	N/A	mA
		XA7 S25	N/A	1	N/A	1	1	N/A	mA

		XA7 S50	N/A	2	N/A	2	2	N/A	mA
		XA7 S75	N/A	9	N/A	9	9	N/A	mA
		XA7 S100	N/A	9	N/A	9	9	N/A	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperature (T_j) with single-ended SelectIO™ resources.

2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.

3. Use the Xilinx Power Estimator spreadsheet tool [Ref 6] to estimate static power consumption for conditions other than those specified.

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT} , V_{CCBRAM} , V_{CCAUX} , and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX} and V_{CCO} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0 the following conditions apply.

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability

levels.

- The $T_{V_{CCO2}V_{CCAUX}}$ time can be allocated in any percentage between the power-on and power-off ramps.

There is no recommended sequence for supplies not discussed in this section.

Table: Power-On Current shows the minimum current, in addition to I_{CCQ} maximum, that is required by Spartan 7 devices for proper power-on and configuration. If the current minimums shown in **Table: Power-On Current** are met, the device powers on after all four supplies have passed through their power-on reset threshold voltages. The FPGA must not be configured until after V_{CCINT} is applied. Once initialized and configured, use the Xilinx Power Estimator spreadsheet tool [Ref 6] to estimate current drain on these supplies.

Table 6: **Power-On Current**

Device	$I_{CCINT} + T_{MIN}$	$I_{CCAUX} + X_{MIN}$	$I_{CCO} + MIN$	$I_{CCBR} + AMMIN$	Units
XC7S6	$I_{CCINTQ} + 120$	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 60$	mA
XC7S15	$I_{CCINTQ} + 120$	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 60$	mA
XC7S25	$I_{CCINTQ} + 120$	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 60$	mA

Device	$I_{CCINTQ} + I_{TMIN}$	$I_{CCAUXQ} + I_{XMIN}$	$I_{CCOQ} + I_{MIN}$	$I_{CCBRAMQ} + I_{AMMIN}$	Units
XC7S50	$I_{CCINTQ} + 120$	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 60$	mA
XC7S75	$I_{CCINTQ} + 300$	$I_{CCAUXQ} + 140$	$I_{CCOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 60$	mA
XC7S100	$I_{CCINTQ} + 300$	$I_{CCAUXQ} + 140$	$I_{CCOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 60$	mA
XA7S6	$I_{CCINTQ} + 120$	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 60$	mA
XA7S15	$I_{CCINTQ} + 120$	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 60$	mA
XA7S25	$I_{CCINTQ} + 120$	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 60$	mA

Device	$I_{CCINTQ} + T_{MIN}$	$I_{CCAUXQ} + X_{MIN}$	$I_{CCOQ} + MIN$	$I_{CCBRAMQ} + AMMIN$	Units
XA7S50	$I_{CCINTQ} + 120$	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 60$	mA
XA7S75	$I_{CCINTQ} + 300$	$I_{CCAUXQ} + 140$	$I_{CCOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 60$	mA
XA7S100	$I_{CCINTQ} + 300$	$I_{CCAUXQ} + 140$	$I_{CCOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 60$	mA

Table 7: Power Supply Ramp Time

Symbol	Description	Conditions	Min	Max	Units
T_{VCCINT}	Ramp time from GND to 90% of V_{CCINT} .		0.2	50	ms
T_{VCCO}	Ramp time from GND to 90% of V_{CCO} .		0.2	50	ms

Symbol	Description	Conditions	Min	Max	Units
T_{VCCAUX}	Ramp time from GND to 90% of V_{CCAUX} .		0.2	50	ms
$T_{VCCBRAM}$	Ramp time from GND to 90% of V_{CCBRAM} .		0.2	50	ms
$T_{VCCO2VCCAUX}$	Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625V$.	$T_J = 125^{\circ}C(1)$	–	300	ms
		$T_J = 100^{\circ}C(1)$	–	500	ms
		$T_J = 85^{\circ}C(1)$	–	800	ms
Notes:					
1. Based on 240,000 power cycles with a nominal V_{CCO} of 3.3V or 36,500 power cycles with a worst case V_{CCO} of 3.465V.					

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a

minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 8: SelectIO DC Input and Output Levels(1)(2)(3)

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
HSTL_I	-0.300	V_{REF} -0.100	V_{REF} +0.100	V_{CCO} +0.300	0.400	V_{CCO} -0.400	8.00	-8.00
HSTL_I_18	-0.300	V_{REF} -0.100	V_{REF} +0.100	V_{CCO} +0.300	0.400	V_{CCO} -0.400	8.00	-8.00
HSTL_II	-0.300	V_{REF} -0.100	V_{REF} +0.100	V_{CCO} +0.300	0.400	V_{CCO} -0.400	16.00	-16.00
HSTL_II_18	-0.300	V_{REF} -0.100	V_{REF} +0.100	V_{CCO} +0.300	0.400	V_{CCO} -0.400	16.00	-16.00

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HSUL _12	– 0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.10	–0.10
LVC MOS 12	– 0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVC MOS 15	– 0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	Note 5	Note 5
LVC MOS 18	– 0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 6	Note 6
LVC MOS 25	– 0.300	0.7	1.700	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 5	Note 5
LVC MOS 33	– 0.300	0.8	2.000	3.450	0.400	V_{CCO} – 0.400	Note 5	Note 5
LVTT L	– 0.300	0.8	2.000	3.450	0.400	2.400	Note 6	Note 6

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MOBILE_DDR	– 0.300	20% V_{CCO}	80% V_{CCO}	V_{CCO} + 0.300	10% V_{CCO}	90% V_{CCO}	0.10	–0.10
PCI3_3_3	– 0.400	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.500	10% V_{CCO}	90% V_{CCO}	1.50	–0.50
SSTL135	– 0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO} /2 – 0.150	V_{CCO} /2 + 0.150	13.00	– 13.00
SSTL135_R	– 0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO} /2 – 0.150	V_{CCO} /2 + 0.150	8.90	–8.90
SSTL15	– 0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO} /2 – 0.175	V_{CCO} /2 + 0.175	13.00	– 13.00
SSTL15_R	– 0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO} /2 – 0.175	V_{CCO} /2 + 0.175	8.90	–8.90
SSTL18_I	– 0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO} /2 – 0.470	V_{CCO} /2 + 0.470	8.00	–8.00

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BL VD S_ 25	0.3 00	1.2 00	1.4 25	0.1 00	–	–	–	1.2 50	–	Note 5		
MI NI _L VD S_ 25	0.3 00	1.2 00	V _C CA UX	0.2 00	0.4 00	0.6 00	1.0 00	1.2 00	1.4 00	0.3 00	0.4 50	0.6 00
PP DS _2 5	0.2 00	0.9 00	V _C CA UX	0.1 00	0.2 50	0.4 00	0.5 00	0.9 50	1.4 00	0.1 00	0.2 50	0.4 00
RS DS _2 5	0.3 00	0.9 00	1.5 00	0.1 00	0.3 50	0.6 00	1.0 00	1.2 00	1.4 00	0.1 00	0.3 50	0.6 00
TM DS _3 3	2.7 00	2.9 65	3.2 30	0.1 50	0.6 75	1.2 00	V _C CO – 0.4 05	V _C CO – 0.3 00	V _C CO – 0.1 90	0.4 00	0.6 00	0.8 00

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – Q).
3. V_{OCM} is the output common mode voltage.
4. V_{OD} is the output differential voltage (Q – Q).
5. V_{OD} for BLVDS will vary significantly depending on topology and loading.

Table 10: Complementary Differential SelectIO DC Input and Output Levels

I/O Standard	V_{ICM} (1)			V_{ID} (2)		V_{OL} (3)		V_{OH} (4)		I _{OL}	I _{O_H}
	V	V	V	V	V	V	V	m	m		
	Min	Typ	Max	Min	Max	Max	Min	A	A	Max	Min
DIFF_HS_TL_I	0.300	0.750	1.125	0.100	–	0.400	$V_{CC} - 0.400$	8.00	–	8.00	–

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DIFF _HS TL_I _18	0.30 0	0.90 0	1.42 5	0.10 0	–	0.40 0	V _{CC} 0 – 0.40 0	8.00 0	– 8.00
DIFF _HS TL_II	0.30 0	0.75 0	1.12 5	0.10 0	–	0.40 0	V _{CC} 0 – 0.40 0	16.0 0	– 16.0 0
DIFF _HS TL_II _18	0.30 0	0.90 0	1.42 5	0.10 0	–	0.40 0	V _{CC} 0 – 0.40 0	16.0 0	– 16.0 0
DIFF _HS UL_1 2	0.30 0	0.60 0	0.85 0	0.10 0	–	20% V _{CC} 0	80% V _{CC} 0	0.10 0	– 0.10 0
DIFF _MO BILE _DD R	0.30 0	0.90 0	1.42 5	0.10 0	–	10% V _{CC} 0	90% V _{CC} 0	0.10 0	– 0.10 0
DIFF _SS TL13 5	0.30 0	0.67 5	1.00 0	0.10 0	–	(V _{CC} 0/2) – 0.15 0	(V _{CC} 0/2) + 0.15 0	13.0	– 13.0

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DIFF _SS TL13 5_R	0.30 0	0.67 5	1.00 0	0.10 0	–	(V _{CC} 0/2) – 0.15 0	(V _{CC} 0/2) + 0.15 0	8.9	–8.9
DIFF _SS TL15	0.30 0	0.75 0	1.12 5	0.10 0	–	(V _{CC} 0/2) – 0.17 5	(V _{CC} 0/2) + 0.17 5	13.0	– 13.0
DIFF _SS TL15 _R	0.30 0	0.75 0	1.12 5	0.10 0	–	(V _{CC} 0/2) – 0.17 5	(V _{CC} 0/2) + 0.17 5	8.9	–8.9
DIFF _SS TL18 _I	0.30 0	0.90 0	1.42 5	0.10 0	–	(V _{CC} 0/2) – 0.47 0	(V _{CC} 0/2) + 0.47 0	8.00	– 8.00
DIFF _SS TL18 _II	0.30 0	0.90 0	1.42 5	0.10 0	–	(V _{CC} 0/2) – 0.60 0	(V _{CC} 0/2) + 0.60 0	13.4	– 13.4

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – Q).
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

LVDS DC Specifications (LVDS_25)

Table 11: LVDS_25 DC Specifications(1)

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply voltage.		2.375	2.500	2.625	V
V_{OH}	Output High voltage for Q and Q.	$R_T = 100\Omega$ across Q and Q signals.	–	–	1.675	V

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{OL}	Output Low voltage for Q and \bar{Q} .	$R_T = 100\Omega$ across Q and \bar{Q} signals.	0.700	–	–	V
V_{ODIFF}	Differential output voltage: (Q – \bar{Q}), Q = High (\bar{Q} – Q), Q = High	$R_T = 100\Omega$ across Q and \bar{Q} signals.	247	350	600	mV
V_{OCM}	Output common-mode voltage.	$R_T = 100\Omega$ across Q and \bar{Q} signals.	1.000	1.250	1.425	V

Sym bol	DC Para mete r	Cond itions	Min	Typ	Max	Units
V_{IDIFF}	Differential input voltage: (Q – Q), Q = High (Q – Q), Q = High		100	350	600	mV
V_{ICM}	Input common-mode voltage.		0.300	1.200	1.500	V
<p>Notes:</p> <p>1. Differential inputs for LVDS_25 can be placed in banks with V_{CCO} levels that are different from the required level for outputs. Consult the 7 Series FPGAs SelectIO Resources User Guide (UG471) [Ref 3] for more information.</p>						

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications from the Vivado™ Design Suite as outlined in [Table: Speed Specification Version By Device](#).

Table 12: [Speed Specification Version By Device](#)

2018.2.1	Device
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2018.2.1	Device
1.23	XC7S6, XC7S15, XC7S25, XC7S50, XC7S75, XC7S100
1.16	XA7S6, XA7S15, XA7S25, XA7S50, XA7S75, XA7S100

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows.

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Spartan 7 FPGAs.

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. [Table: Spartan 7 Device Speed Grade Designations](#) correlates the current status of each Spartan 7 device on a per speed grade basis.

Table 13: Spartan 7 Device Speed Grade Designations

Device	Speed Grade, Temperature Range, and V _{CCINT} Operating Voltage		
	Advance	Preliminary	Production
XC7S6			-2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), -1Q (1.0V), and -1LI (0.95V) ⁽¹⁾

Device	Speed Grade, Temperature Range, and V _{CCINT} Operating Voltage		
	Advance	Preliminary	Production
XC7S15			-2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), -1Q (1.0V), and -1LI (0.95V)(1)
XC7S25			-2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), -1Q (1.0V), and -1LI (0.95V)(1)
XC7S50			-2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), -1Q (1.0V), and -1LI (0.95V)(1)

Device	Speed Grade, Temperature Range, and V _{CCINT} Operating Voltage		
	Advance	Preliminary	Production
XC7S75			-2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), -1Q (1.0V), and -1LI (0.95V)(1)
XC7S100			-2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), -1Q (1.0V), and -1LI (0.95V)(1)
XA7S6			-2I (1.0V), -1I (1.0V), -1Q (1.0V)
XA7S15			-2I (1.0V), -1I (1.0V), -1Q (1.0V)

Device	Speed Grade, Temperature Range, and V_{CCINT} Operating Voltage		
	Advance	Preliminary	Production
XA7S25			-2I (1.0V), -1I (1.0V), -1Q (1.0V)
XA7S50			-2I (1.0V), -1I (1.0V), -1Q (1.0V)
XA7S75			-2I (1.0V), -1I (1.0V), -1Q (1.0V)
XA7S100			-2I (1.0V), -1I (1.0V), -1Q (1.0V)
<p>Notes:</p> <p>1. The lowest power -1LI devices, where $V_{CCINT} = 0.95V$, are listed in the Vivado Design Suite as -1IL.</p>			

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance,

Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

[Table: Spartan 7 Device Production Software and Speed Specification Release](#) lists the production released Spartan 7 device, speed grade, and the minimum corresponding supported speed specification version and software revisions. The software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 14: Spartan 7 Device Production Software and Speed Specification Release

Device	Operating Voltage, Speed Grade, and Temperature Range					
	V _{CCINT}	1.0V				0.95V
	-2C	-2I	-1C	-1I	-1Q	-1LI
XC7S6	Vivado tools 2018.2 v1.22				Vivado tools 2018.2.1 v1.23	Vivado tools 2018.2 v1.22
XC7S15	Vivado tools 2018.2 v1.22				Vivado tools 2018.2.1 v1.23	Vivado tools 2018.2 v1.22

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XC7S25	Vivado tools 2017.4 v1.20			Vivado tools 2018.1 v1.21	Vivado tools 2017.4 v1.20
XC7S50	Vivado tools 2017.2 v1.17			Vivado tools 2017.3 v1.19	Vivado tools 2017.2 v1.17
XC7S75	Vivado tools 2018.1 v1.21			Vivado tools 2018.2.1 v1.23	Vivado tools 2018.1 v1.21
XC7S100	Vivado tools 2018.1 v1.21			Vivado tools 2018.2.1 v1.23	Vivado tools 2018.1 v1.21
XA7S6	N/A	Vivado tools 2018.2.1 v1.16	N/A	Vivado tools 2018.2.1 v1.16	N/A
XA7S15	N/A	Vivado tools 2018.2.1 v1.16	N/A	Vivado tools 2018.2.1 v1.16	N/A

XA7S25	N/A	Vivado tools 2018.1 v1.15	N/A	Vivado tools 2018.1 v1.15	N/A
XA7S50	N/A	Vivado tools 2017.3 v1.12	N/A	Vivado tools 2017.3 v1.12	N/A
XA7S75	N/A	Vivado tools 2018.2.1 v1.16	N/A	Vivado tools 2018.2.1 v1.16	N/A
XA7S100	N/A	Vivado tools 2018.2.1 v1.16	N/A	Vivado tools 2018.2.1 v1.16	N/A

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Spartan 7 FPGAs. These values are subject to the same guidelines as the [AC Switching Characteristics](#).

Table 15: [Networking Applications Interface Performances](#)

Description	V _{CCINT} Operating Voltage, Speed Grade, and Temperature Range			Units
	1.0V	0.95V		
	-2C/-2I	-1C/-1I/-1Q	-1LI	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH H = 4 to 8)	680	600	600	Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH H = 4 to 14)	1250	950	950	Mb/s
SDR LVDS receiver(1)	680	600	600	Mb/s
DDR LVDS receiver(1)	1250	950	950	Mb/s

Notes:

1.LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

Table 16: Maximum Physical Interface (PHY) Rate for Memory Interface IP available with the Memory Interface Generator(1)

Memory Standard	V _{CCINT}	Operating Voltage, Speed Grade, and Temperature Range			Units
		1.0V	0.95V		
	-2C/-2I	-1C/-1I	-1Q	-1LI	
4:1 Memory Controllers					
DDR3	800(2)	667	667	667	Mb/s
DDR3L	800(2)	667	N/A	667	Mb/s
DDR2	800(2)	667	533	667	Mb/s
2:1 Memory Controllers					

DDR3	800(2)	667	667	667	Mb/s
DDR3L	800(2)	667	N/A	667	Mb/s
DDR2	800(2)	667	533	667	Mb/s
LPDDR2	667	533	400	533	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see the Zynq 7000 SoC and 7 Series Devices Memory Interface Solutions User Guide (UG586) [Ref 7].

2. The maximum PHY rate is 667 Mb/s in the FTGB196 package.

IOB Pad Input/Output/3-State

Table: IOB High Range (HR) Switching Characteristics summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- T_{IOP_I} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.

- T_{IOP_O} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

- T_{IOP_T} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HR I/O banks, the IN_TERM termination turn-on time is always faster than T_{IOP_T} when the INTERMDISABLE pin is used.

Table 17: IOB High Range (HR) Switching Characteristics

I/O Standard	T IOPI		T IOOP				T IOTP		Units		
	V CCINT Operating Voltage and Speed Grade										
	1.0V	0	1.0V	0	1.0V	0	0	0			
		.95V		.95V		.95V		.95V			
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L		
LVT TL_S4	1.34	1.41	1.41	3.93	4.18	4.18	3.96	4.20	4.20	ns	
LVT TL_S8	1.34	1.41	1.41	3.66	3.92	3.92	3.69	3.93	3.93	ns	
LVT TL_S12	1.34	1.41	1.41	3.65	3.90	3.90	3.68	3.91	3.91	ns	

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LVT TL_ S16	1.34	1.41	1.41	3.19	3.45	3.45	3.22	3.46	3.46	ns
LVT TL_ S24	1.34	1.41	1.41	3.41	3.67	3.67	3.44	3.68	3.68	ns
LVT TL_ F4	1.34	1.41	1.41	3.38	3.64	3.64	3.41	3.65	3.65	ns
LVT TL_ F8	1.34	1.41	1.41	2.87	3.12	3.12	2.90	3.13	3.13	ns
LVT TL_ F12	1.34	1.41	1.41	2.85	3.10	3.10	2.88	3.12	3.12	ns
LVT TL_ F16	1.34	1.41	1.41	2.68	2.93	2.93	2.71	2.95	2.95	ns
LVT TL_ F24	1.34	1.41	1.41	2.65	2.90	2.90	2.68	2.91	2.91	ns

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LVD S_2 5	0.81	0.88	0.88	1.41	1.67	1.67	1.44	1.68	1.68	ns
MIN I_LV DS_ 25	0.81	0.88	0.88	1.40	1.65	1.65	1.43	1.66	1.66	ns
BLV DS_ 25	0.81	0.88	0.88	1.96	2.21	2.21	1.99	2.23	2.23	ns
RS DS_ 25 (poi nt to poin t)	0.81	0.88	0.88	1.40	1.65	1.65	1.43	1.66	1.66	ns
PP DS_ 25	0.81	0.88	0.88	1.41	1.67	1.67	1.44	1.68	1.68	ns
TM DS_ 33	0.81	0.88	0.88	1.54	1.79	1.79	1.57	1.80	1.80	ns

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PCI 33_ 3	1.32	1.39	1.39	3.22	3.48	3.48	3.25	3.49	3.49	ns
HS UL_ 12_ S	0.75	0.82	0.82	1.93	2.18	2.18	1.96	2.20	2.20	ns
HS UL_ 12_ F	0.75	0.82	0.82	1.41	1.67	1.67	1.44	1.68	1.68	ns
DIF F_H SUL _12 _S	0.76	0.83	0.83	1.93	2.18	2.18	1.96	2.20	2.20	ns
DIF F_H SUL _12 _F	0.76	0.83	0.83	1.41	1.67	1.67	1.44	1.68	1.68	ns
MO BIL E_D DR_ S	0.84	0.91	0.91	1.80	2.06	2.06	1.83	2.07	2.07	ns

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MOBILE_DDR_F	0.84	0.91	0.91	1.51	1.76	1.76	1.54	1.77	1.77	ns
DIFF_MOBILE_DDR_S	0.78	0.85	0.85	1.82	2.07	2.07	1.85	2.09	2.09	ns
DIFF_MOBILE_DDR_F	0.78	0.85	0.85	1.57	1.82	1.82	1.60	1.84	1.84	ns
HSTL_I_S	0.75	0.82	0.82	1.74	1.99	1.99	1.77	2.01	2.01	ns
HSTL_II_S	0.73	0.80	0.80	1.54	1.79	1.79	1.57	1.80	1.80	ns
HSTL_I_18_S	0.75	0.82	0.82	1.41	1.67	1.67	1.44	1.68	1.68	ns

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HST L_II _18 _S	0.75	0.81	0.81	1.54	1.79	1.79	1.57	1.80	1.80	ns
DIF F_H STL _I_S	0.76	0.83	0.83	1.71	1.96	1.96	1.74	1.98	1.98	ns
DIF F_H STL _II_ S	0.76	0.83	0.83	1.63	1.88	1.88	1.66	1.90	1.90	ns
DIF F_H STL _I_1 8_S	0.79	0.86	0.86	1.51	1.76	1.76	1.54	1.77	1.77	ns
DIF F_H STL _II_ 18_ S	0.78	0.85	0.85	1.58	1.84	1.84	1.61	1.85	1.85	ns
HST L_I_ F	0.75	0.82	0.82	1.22	1.48	1.48	1.25	1.49	1.49	ns

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HST L_II _F	0.73	0.80	0.80	1.24	1.49	1.49	1.27	1.51	1.51	ns
HST L_I_ 18_ F	0.75	0.82	0.82	1.26	1.51	1.51	1.29	1.52	1.52	ns
HST L_II _18 _F	0.75	0.81	0.81	1.24	1.49	1.49	1.27	1.51	1.51	ns
DIF F_H STL _I_F	0.76	0.83	0.83	1.30	1.56	1.56	1.33	1.57	1.57	ns
DIF F_H STL _II_ F	0.76	0.83	0.83	1.33	1.59	1.59	1.36	1.60	1.60	ns
DIF F_H STL _I_1 8_F	0.79	0.86	0.86	1.33	1.59	1.59	1.36	1.60	1.60	ns

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DIF F_H STL _II_ 18_ F	0.78	0.85	0.85	1.33	1.59	1.59	1.36	1.60	1.60	ns
LVC MO S33 _S4	1.34	1.41	1.41	3.93	4.18	4.18	3.96	4.20	4.20	ns
LVC MO S33 _S8	1.34	1.41	1.41	3.65	3.90	3.90	3.68	3.91	3.91	ns
LVC MO S33 _S1 2	1.34	1.41	1.41	3.21	3.46	3.46	3.24	3.48	3.48	ns
LVC MO S33 _S1 6	1.34	1.41	1.41	3.52	3.77	3.77	3.55	3.79	3.79	ns

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LVC MO S33 _F4	1.34	1.41	1.41	3.38	3.64	3.64	3.41	3.65	3.65	ns
LVC MO S33 _F8	1.34	1.41	1.41	2.87	3.12	3.12	2.90	3.13	3.13	ns
LVC MO S33 _F1 2	1.34	1.41	1.41	2.68	2.93	2.93	2.71	2.95	2.95	ns
LVC MO S33 _F1 6	1.34	1.41	1.41	2.68	2.93	2.93	2.71	2.95	2.95	ns
LVC MO S25 _S4	1.20	1.27	1.27	3.26	3.51	3.51	3.29	3.52	3.52	ns
LVC MO S25 _S8	1.20	1.27	1.27	3.01	3.26	3.26	3.04	3.27	3.27	ns

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LVC MO S25 _S1 2	1.20	1.27	1.27	2.60	2.85	2.85	2.63	2.87	2.87	ns
LVC MO S25 _S1 6	1.20	1.27	1.27	2.94	3.20	3.20	2.97	3.21	3.21	ns
LVC MO S25 _F4	1.20	1.27	1.27	2.87	3.12	3.12	2.90	3.13	3.13	ns
LVC MO S25 _F8	1.20	1.27	1.27	2.30	2.56	2.56	2.33	2.57	2.57	ns
LVC MO S25 _F1 2	1.20	1.27	1.27	2.29	2.54	2.54	2.32	2.55	2.55	ns

Spartan 7 FPGAs Data Sheet: DC and AC Switching Characteristics (DS189)

LVC MO S25 _F1 6	1.20	1.27	1.27	2.13	2.39	2.39	2.16	2.40	2.40	ns
LVC MO S18 _S4	0.83	0.89	0.89	1.74	1.99	1.99	1.77	2.01	2.01	ns
LVC MO S18 _S8	0.83	0.89	0.89	2.30	2.56	2.56	2.33	2.57	2.57	ns
LVC MO S18 _S1 2	0.83	0.89	0.89	2.30	2.56	2.56	2.33	2.57	2.57	ns
LVC MO S18 _S1 6	0.83	0.89	0.89	1.65	1.90	1.90	1.68	1.91	1.91	ns

Spartan 7 FPGAs Data Sheet: DC and AC Switching Characteristics (DS189)

LVC MO S18 _S2 4	0.83	0.89	0.89	1.72	1.98	1.98	1.75	1.99	1.99	ns
LVC MO S18 _F4	0.83	0.89	0.89	1.57	1.82	1.82	1.60	1.84	1.84	ns
LVC MO S18 _F8	0.83	0.89	0.89	1.80	2.06	2.06	1.83	2.07	2.07	ns
LVC MO S18 _F1 2	0.83	0.89	0.89	1.80	2.06	2.06	1.83	2.07	2.07	ns
LVC MO S18 _F1 6	0.83	0.89	0.89	1.52	1.77	1.77	1.55	1.79	1.79	ns

Spartan 7 FPGAs Data Sheet: DC and AC Switching Characteristics (DS189)

LVC MO S18 _F2 4	0.83	0.89	0.89	1.46	1.71	1.71	1.49	1.73	1.73	ns
LVC MO S15 _S4	0.86	0.93	0.93	2.18	2.43	2.43	2.21	2.45	2.45	ns
LVC MO S15 _S8	0.86	0.93	0.93	2.21	2.46	2.46	2.24	2.48	2.48	ns
LVC MO S15 _S1 2	0.86	0.93	0.93	1.71	1.96	1.96	1.74	1.98	1.98	ns
LVC MO S15 _S1 6	0.86	0.93	0.93	1.71	1.96	1.96	1.74	1.98	1.98	ns
LVC MO S15 _F4	0.86	0.93	0.93	1.97	2.23	2.23	2.00	2.24	2.24	ns

Spartan 7 FPGAs Data Sheet: DC and AC Switching Characteristics (DS189)

LVC MO S15 _F8	0.86	0.93	0.93	1.72	1.98	1.98	1.75	1.99	1.99	ns
LVC MO S15 _F1 2	0.86	0.93	0.93	1.47	1.73	1.73	1.50	1.74	1.74	ns
LVC MO S15 _F1 6	0.86	0.93	0.93	1.46	1.71	1.71	1.49	1.73	1.73	ns
LVC MO S12 _S4	0.95	1.02	1.02	2.69	2.95	2.95	2.72	2.96	2.96	ns
LVC MO S12 _S8	0.95	1.02	1.02	2.21	2.46	2.46	2.24	2.48	2.48	ns
LVC MO S12 _S1 2	0.95	1.02	1.02	1.91	2.17	2.17	1.94	2.18	2.18	ns

Spartan 7 FPGAs Data Sheet: DC and AC Switching Characteristics (DS189)

LVC MO S12 _F4	0.95	1.02	1.02	2.10	2.35	2.35	2.13	2.37	2.37	ns
LVC MO S12 _F8	0.95	1.02	1.02	1.66	1.92	1.92	1.69	1.93	1.93	ns
LVC MO S12 _F1 2	0.95	1.02	1.02	1.51	1.76	1.76	1.54	1.77	1.77	ns
SST L13 5_S	0.75	0.82	0.82	1.47	1.73	1.73	1.50	1.74	1.74	ns
SST L15 _S	0.68	0.75	0.75	1.43	1.68	1.68	1.46	1.69	1.69	ns
SST L18 _I_S	0.75	0.82	0.82	1.79	2.04	2.04	1.82	2.06	2.06	ns

Spartan 7 FPGAs Data Sheet: DC and AC Switching Characteristics (DS189)

SST L18 _II_ S	0.75	0.82	0.82	1.43	1.68	1.68	1.46	1.70	1.70	ns
DIF F_S STL 135 _S	0.76	0.83	0.83	1.47	1.73	1.73	1.50	1.74	1.74	ns
DIF F_S STL 15_ S	0.76	0.83	0.83	1.43	1.68	1.68	1.46	1.69	1.69	ns
DIF F_S STL 18_I _S	0.79	0.86	0.86	1.80	2.06	2.06	1.83	2.07	2.07	ns
DIF F_S STL 18_I I_S	0.79	0.86	0.86	1.51	1.76	1.76	1.54	1.77	1.77	ns
SST L13 5_F	0.75	0.82	0.82	1.24	1.49	1.49	1.27	1.51	1.51	ns

Spartan 7 FPGAs Data Sheet: DC and AC Switching Characteristics (DS189)

SST L15 _F	0.68	0.75	0.75	1.19	1.45	1.45	1.22	1.46	1.46	ns
SST L18 _I_F	0.75	0.82	0.82	1.24	1.49	1.49	1.27	1.51	1.51	ns
SST L18 _II_ F	0.75	0.82	0.82	1.24	1.49	1.49	1.27	1.51	1.51	ns
DIF F_S STL 135 _F	0.76	0.83	0.83	1.24	1.49	1.49	1.27	1.51	1.51	ns
DIF F_S STL 15_ F	0.76	0.83	0.83	1.19	1.45	1.45	1.22	1.46	1.46	ns
DIF F_S STL 18_I _F	0.79	0.86	0.86	1.35	1.60	1.60	1.38	1.62	1.62	ns

DIF F_S STL 18_I I_F	0.79	0.86	0.86	1.33	1.59	1.59	1.36	1.60	1.60	ns
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[Table: IOB 3-state Output Switching Characteristics](#) specifies the values of T_{IOTPHZ} and $T_{IOIBUFDISABLE}$. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{IOIBUFDISABLE}$ is described as the IOB delay from IBUFDISABLE to O output. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than T_{IOTPHZ} when the INTERMDISABLE pin is used.

Table 18: [IOB 3-state Output Switching Characteristics](#)

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V	0.95V		
		-2	-1	-1L	
T_{IOTPHZ}	T input to pad high-impedance.	2.19	2.37	2.37	ns

$T_{IOIBUFDIS}$ ABLE	IBUF turn-on time from IBUFDISABLE to O output.	2.30	2.60	2.60	ns
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I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

[Table: Input Delay Measurement Methodology](#) shows the test setup parameters used for measuring input delay.

Table 19: [Input Delay Measurement Methodology](#)

Description	I/O Standard Attribute	V_L (1)	V_H (1)	V_{MEAS} (3) (5)	V_{REF} (2) (4)
LVC MOS, 1.2V	LVC MOS12	0.1	1.1	0.6	–
LVC MOS, 1.5V	LVC MOS15	0.1	1.4	0.75	–

Description	I/O Standard Attribute	V _L (1)	V _H (1)	V _{MEAS} (3) (5)	V _{REF} (2) (4)
LVC MOS, 1.8V	LVC MOS18	0.1	1.7	0.9	–
LVC MOS, 2.5V	LVC MOS25	0.1	2.4	1.25	–
LVC MOS, 3.3V	LVC MOS33	0.1	3.2	1.65	–
LVTTL, 3.3V	LVTTL	0.1	3.2	1.65	–
MOBILE_ DDR, 1.8V	MOBILE_ DDR	0.1	1.7	0.9	–
PCI33, 3.3V	PCI33_3	0.1	3.2	1.65	–

Description	I/O Standard Attribute	V_L (1)	V_H (1)	V_{MEAS} (3) (5)	V_{REF} (2) (4)
HSTL (high-speed transceiver logic), Class I, 1.2V	HSTL_I_12	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.60
HSTL, Class I & II, 1.5V	HSTL_I, HSTL_II	$V_{REF} - 0.65$	$V_{REF} + 0.65$	V_{REF}	0.75
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	$V_{REF} - 0.8$	$V_{REF} + 0.8$	V_{REF}	0.90
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.60

Description	I/O Standard Attribute	V _L (1)	V _H (1)	V _{MEAS} (3) (5)	V _{REF} (2) (4)
SSTL (stub-terminated transceiver logic), 1.2V	SSTL12	V _{REF} - 0.5	V _{REF} + 0.5	V _{REF}	0.60
SSTL, 1.35V	SSTL135, SSTL135_R	V _{REF} - 0.575	V _{REF} + 0.575	V _{REF}	0.675
SSTL, 1.5V	SSTL15, SSTL15_R	V _{REF} - 0.65	V _{REF} + 0.65	V _{REF}	0.75
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	V _{REF} - 0.8	V _{REF} + 0.8	V _{REF}	0.90
DIFF_MOBILE_DDR, 1.8V	DIFF_MOBILE_DDR	0.9 - 0.125	0.9 + 0.125	0(5)	-

Description	I/O Standard Attribute	V _L (1)	V _H (1)	V _{MEAS} (3) (5)	V _{REF} (2) (4)
DIFF_HSTL, Class I, 1.2V	DIFF_HSTL_I_12	0.6 – 0.125	0.6 + 0.125	0(5)	–
DIFF_HSTL, Class I & II, 1.5V	DIFF_HSTL_I, DIFF_HSTL_II	0.75 – 0.125	0.75 + 0.125	0(5)	–
DIFF_HSTL, Class I & II, 1.8V	DIFF_HSTL_I_18, DIFF_HSTL_II_18	0.9 – 0.125	0.9 + 0.125	0(5)	–
DIFF_HSTL, 1.2V	DIFF_HSTL_12	0.6 – 0.125	0.6 + 0.125	0(5)	–
DIFF_SSTL135/ DIFF_SSTL135_R, 1.35V	DIFF_SSTL135, DIFF_SSTL135_R	0.675 – 0.125	0.675 + 0.125	0(5)	–

Description	I/O Standard Attribute	V _L (1)	V _H (1)	V _{MEAS} (3) (5)	V _{REF} (2) (4)
DIFF_SST L15/ DIFF_SST L15_R, 1.5V	DIFF_SST L15, DIFF_SST L15_R	0.75 – 0.125	0.75 + 0.125	0(5)	–
DIFF_SST L18_I/ DIFF_SST L18_II, 1.8V	DIFF_SST L18_I, DIFF_SST L18_II	0.9 – 0.125	0.9 + 0.125	0(5)	–
LVDS_25, 2.5V	LVDS_25	1.2 – 0.125	1.2 + 0.125	0(5)	–
BLVDS_25, 2.5V	BLVDS_25	1.25 – 0.125	1.25 + 0.125	0(5)	–
MINI_LVDS_25, 2.5V	MINI_LVDS_25	1.25 – 0.125	1.25 + 0.125	0(5)	–
PPDS_25	PPDS_25	1.25 – 0.125	1.25 + 0.125	0(5)	–

Description	I/O Standard Attribute	V_L (1)	V_H (1)	V_{MEAS} (3) (5)	V_{REF} (2) (4)
RSDS_25	RSDS_25	1.25 – 0.125	1.25 + 0.125	0(5)	–
TMDS_33	TMDS_33	3 – 0.125	3 + 0.125	0(5)	–

Notes:

- Input waveform switches between V_L and V_H .
- Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
- Input voltage level from which measurement starts.
- This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in [This Figure](#).
- The value given is the differential input voltage.

Output Delay Measurements

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in [This Figure](#) and [This Figure](#).

Figure 1: Single-ended Test Setup

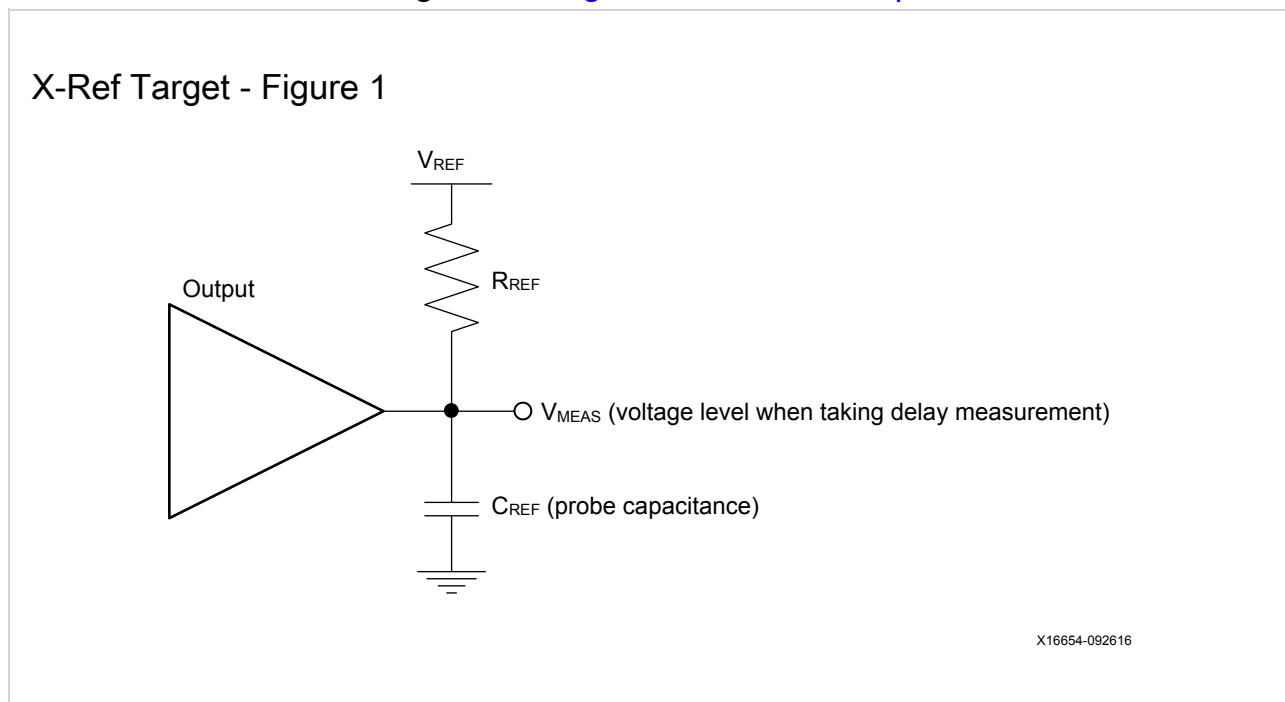
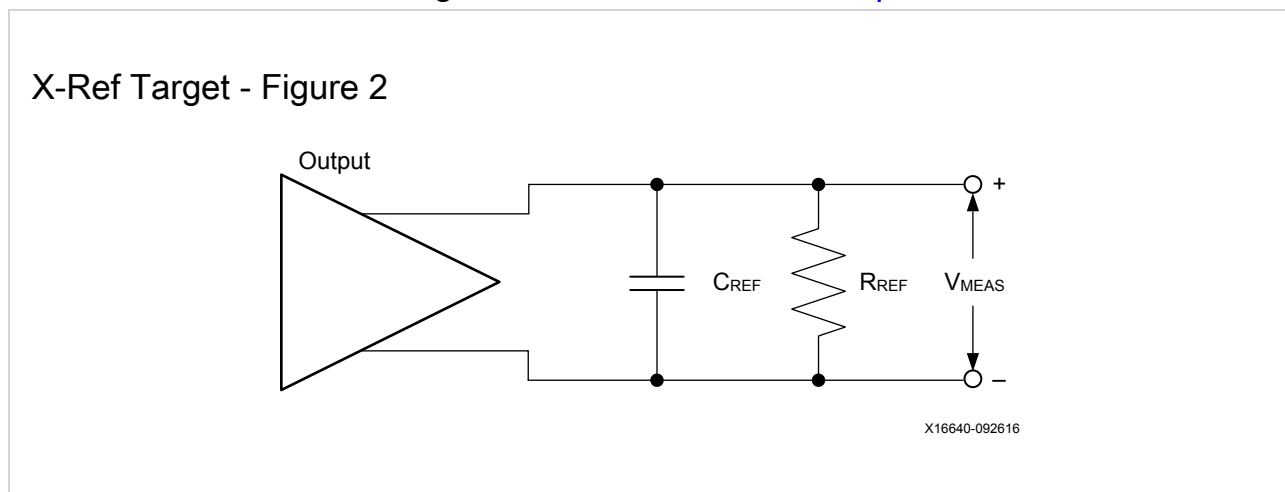


Figure 2: Differential Test Setup



Parameters V_{REF} , R_{REF} , C_{REF} , and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from [Table: Output Delay Measurement Methodology](#).
2. Record the time to V_{MEAS} .
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS} .

5. Compare the results of [step 2](#) and [step 4](#). The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 20: Output Delay Measurement Methodology

Description	I/O Standard Attribute	Resistance (Ω)	Capacitance (pF)	Measurement Voltage (V)	Reference Voltage (V)
LVCMOS, 1.2V	LVCMOS12	1M	0	0.6	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 3.3V	LVCMOS33	1M	0	1.65	0
LVTTL, 3.3V	LVTTL	1M	0	1.65	0

Description	I/O Standard Attribute	R _{REF} (Ω)	C _{REF} (pF)	V _{MEAS} (V)	V _{REF} (V)
PCI33, 3.3V	PCI33_3	25	10	1.65	0
HSTL (high-speed transceiver logic), Class I, 1.2V	HSTL_I_12	50	0	V _{REF}	0.6
HSTL, Class I, 1.5V	HSTL_I	50	0	V _{REF}	0.75
HSTL, Class II, 1.5V	HSTL_II	25	0	V _{REF}	0.75
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V _{REF}	0.9

Description	I/O Standard Attribute	R RE F (W)	C RE F (1) (pF)	V MEAS (V)	V REF (V)
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V _{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	50	0	V _{REF}	0.6
SSTL12, 1.2V	SSTL12	50	0	V _{REF}	0.6
SSTL135/SSTL135_R, 1.35V	SSTL135, SSTL135_R	50	0	V _{REF}	0.675
SSTL15/SSTL15_R, 1.5V	SSTL15, SSTL15_R	50	0	V _{REF}	0.75

Description	I/O Standard Attribute	R _{REF} (Ω)	C _{REF} (pF)	V _{MEAS} (V)	V _{REF} (V)
SSTL (stub-series terminated logic), Class I & Class II, 1.8V	SSTL18_I, SSTL18_II	50	0	V _{REF}	0.9
DIFF_MOBILE_DDR, 1.8V	DIFF_MOBILE_DDR	50	0	V _{REF}	0.9
DIFF_HSTL, Class I, 1.2V	DIFF_HSTL_I_12	50	0	V _{REF}	0.6
DIFF_HSTL, Class I & II, 1.5V	DIFF_HSTL_I, DIFF_HSTL_II	50	0	V _{REF}	0.75

Description	I/O Standard Attribute	R _{REF} (W)	C _{REF} (pF)	V _{MEAS} (V)	V _{REF} (V)
DIFF_HSTL, Class I & II, 1.8V	DIFF_HSTL_I_18, DIFF_HSTL_II_18	50	0	V _{REF}	0.9
DIFF_HSUL_12, 1.2V	DIFF_HSUL_12	50	0	V _{REF}	0.6
DIFF_SSTL135/DIFF_SSTL135_R, 1.35V	DIFF_SSTL135, DIFF_SSTL135_R	50	0	V _{REF}	0.675
DIFF_SSTL15/DIFF_SSTL15_R, 1.5V	DIFF_SSTL15, DIFF_SSTL15_R	50	0	V _{REF}	0.75
DIFF_SSTL18, Class I & II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	50	0	V _{REF}	0.9

Description	I/O Standard Attribute	R _{REF} (W)	C _{REF} (1) (pF)	V _{MEAS} (V)	V _{REF} (V)
LVDS, 2.5V	LVDS_25	100	0	0(2)	0
BLVDS (Bus LVDS), 2.5V	BLVDS_25	100	0	0(2)	0
Mini LVDS, 2.5V	MINI_LVDS_25	100	0	0(2)	0
PPDS_25	PPDS_25	100	0	0(2)	0
RSDS_25	RSDS_25	100	0	0(2)	0
TMDS_33	TMDS_33	50	0	0(2)	3.3

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.

2. The value given is the differential output voltage.

Input/Output Logic Switching Characteristics

Table 21: ILOGIC Switching Characteristics

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V	0.95V		
		-2	-1	-1L	
Setup/Hold					
T _{ICE1CK} /T _{ICKCE1}	CE1 pin setup/hold with respect to CLK.	0.54/0.02	0.76/0.02	0.76/0.02	ns
T _{ISRCK} /T _{ICKSR}	SR pin setup/hold with respect to CLK.	0.70/0.01	1.13/0.01	1.13/0.01	ns

$T_{\text{IDOCK}/T_{\text{IOCKD}}}$	D pin setup/hold with respect to CLK without delay.	0.01/0.29	0.01/0.33	0.01/0.33	ns
$T_{\text{IDOCKD}/T_{\text{IOCKDD}}}$	DDL Y pin setup/hold with respect to CLK (using IDELAY).	0.02/0.29	0.02/0.33	0.02/0.33	ns
Combinatorial					
T_{IDI}	D pin to O pin propagation delay, no delay.	0.11	0.13	0.13	ns
T_{IDID}	DDL Y pin to O pin propagation delay (using IDELAY).	0.12	0.14	0.14	ns
Sequential Delays					

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T_{IDLO}	D pin to Q1 pin using flip-flop as a latch without delay.	0.44	0.51	0.51	ns
T_{IDL0D}	DDL pin to Q1 pin using flip-flop as a latch (using IDELAY).	0.44	0.51	0.51	ns
T_{ICKQ}	CLK to Q outputs.	0.57	0.66	0.66	ns
T_{RQ_ILOGIC}	SR pin to OQ/TQ out.	1.08	1.32	1.32	ns
T_{GSRQ_ILOGIC}	Global set/reset to Q outputs.	7.60	10.51	10.51	ns
Set/Reset					

T_{RPW_ILO} GIC	Minimum pulse width, SR inputs.	0.72	0.72	0.72	ns, Min
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Table 22: OLOGIC Switching Characteristics

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V	0.95V		
		-2	-1	-1L	
Setup/Hold					
T_{ODCK}/T_{OCKD}	D1/D2 pins setup/hold with respect to CLK.	0.71/-0.11	0.84/-0.11	0.84/-0.11	ns
T_{OOCECK}/T_{OCKOCE}	OCE pin setup/hold with respect to CLK.	0.34/0.58	0.51/0.58	0.51/0.58	ns

T_{OSRCK}/T_{OCKSR}	SR pin setup/hold with respect to CLK.	0.44/0.21	0.80/0.21	0.80/0.21	ns
T_{OTCK}/T_{OCT}	T1/T2 pins setup/hold with respect to CLK.	0.73/-0.14	0.89/-0.14	0.89/-0.14	ns
T_{OTCECK}/T_{OCTCE}	TCE pin setup/hold with respect to CLK.	0.34/0.01	0.51/0.01	0.51/0.01	ns
Combinatorial					
T_{ODQ}	D1 to OQ out or T1 to TQ out.	0.96	1.16	1.16	ns
Sequential Delays					
T_{OCKQ}	CLK to OQ/TQ out.	0.49	0.56	0.56	ns

T_{RQ_OLOGIC}	SR pin to OQ/TQ out.	0.80	0.95	0.95	ns
T_{GSRQ_OLOGIC}	Global set/reset to Q outputs.	7.60	10.51	10.51	ns
Set/Reset					
T_{RPW_OLOGIC}	Minimum pulse width, SR inputs.	0.74	0.74	0.74	ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 23: ISERDES Switching Characteristics

Symbol	Description	V _{CCINT}	Operating Voltage and Speed Grade		Units
		1.0V		0.95V	
		-2	-1	-1L	

Setup/Hold for Control Lines

T_{ISCK_BI} T_{ISCK_BI} T_{ISCK_BI} T_{ISCK_BI}	BITSLIP pin setup/hold with respect to CLKDIV.	0.02/0.15	0.02/0.17	0.02/0.17	ns
T_{ISCK_CE} / T_{ISCK_CE}	CE pin setup/hold with respect to CLK (for CE1).	0.50/-0.01	0.72/-0.01	0.72/-0.01	ns
T_{ISCK_CE} 2/ T_{ISCK_CE} 2	CE pin setup/hold with respect to CLKDIV (for CE2).	-0.10/0.36	-0.10/0.40	-0.10/0.40	ns

Setup/Hold for Data Lines

T_{ISCK_D} T_{ISCK_D}	D pin setup/hold with respect to CLK.	-0.02/0.14	-0.02/0.17	-0.02/0.17	ns
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$T_{ISDCK_DDL}/$ T_{ISCKD_DDL}	DDL pin setup/hold with respect to CLK (using IDELAY). (1)	-0.02/0.14	-0.02/0.17	-0.02/0.17	ns
$T_{ISDCK_DDR}/$ T_{ISCKD_DDR}	D pin setup/hold with respect to CLK at DDR mode.	-0.02/0.14	-0.02/0.17	-0.02/0.17	ns
$T_{ISDCK_DDL_DDR}/$ $T_{ISCKD_DDL_DDR}$	D pin setup/hold with respect to CLK at DDR mode (using IDELAY). (1)	0.14/0.14	0.17/0.17	0.17/0.17	ns
Sequential Delays					

T_{ISCKO_Q}	CLKDIV to out at Q pin.	0.54	0.66	0.66	ns
Propagation Delays					
T_{ISDO_DO}	D input to DO output pin.	0.11	0.13	0.13	ns
Notes:					
1. Recorded at 0 tap value.					

Output Serializer/Deserializer Switching Characteristics

Table 24: OSERDES Switching Characteristics

Symbol	Description	V_{CCINT}	Operating Voltage and Speed Grade		Units
		1.0V		0.95V	
		-2	-1	-1L	

Setup/Hold					
T_{OSDCK_D} / T_{OSCKD_D}	D input setup/hold with respect to CLKDIV.	0.45/0.03	0.63/0.03	0.63/0.03	ns
T_{OSDCK_T} / T_{OSCKD_T}	T input setup/hold with respect to CLK.	0.73/-0.13	0.88/-0.13	0.88/-0.13	ns
T_{OSDCK_T} 2/ T_{OSCKD_T} 2	T input setup/hold with respect to CLKDIV.	0.34/-0.13	0.39/-0.13	0.39/-0.13	ns
T_{OSCK_O} CE/ T_{OSCK} C_OCE	OCE input setup/hold with respect to CLK.	0.34/0.58	0.51/0.58	0.51/0.58	ns
T_{OSCK_S}	SR (reset) input setup with respect to CLKDIV.	0.52	0.85	0.85	ns

T_{OSCK_T} $C_{E/TOSCK}$ C_{TCE}	TCE input setup/hold with respect to CLK.	0.34/0.01	0.51/0.01	0.51/0.01	ns
Sequential Delays					
T_{OSCKO_O} Q	Clock to out from CLK to OQ.	0.42	0.48	0.48	ns
T_{OSCKO_T} Q	Clock to out from CLK to TQ.	0.49	0.56	0.56	ns
Combinatorial					
T_{OSDO_TT} Q	T input to TQ out.	0.92	1.11	1.11	ns

Input/Output Delay Switching Characteristics

Table 25: [Input/Output Delay Switching Characteristics](#)

Symbol	Description	V _{CCINT}	Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
		-2		-1	-1L	
IDELAYCTRL						
T _{DLYCCO_RDY}	Reset to ready for IDELAYCTRL.	3.67	3.67	3.67		μs

F _{IDELAYCT} RL_REF	Attribute REFCLK frequency = 200.00. (1)	200.00	200.00	200.00	MHz
	Attribute REFCLK frequency = 300.00. (1)	300.00	300.00	300.00	MHz
	Attribute REFCLK frequency = 400.00. (1)	400.00	N/A	N/A	MHz
IDELAYC TRL_REF _PRECISI ON	REFCLK precision	±10	±10	±10	MHz
T _{IDELAYCT} RL_RPW	Minimum reset pulse width.	59.28	59.28	59.28	ns
IDELAY					

Spartan 7 FPGAs Data Sheet: DC and AC Switching Characteristics (DS189)

$T_{IDELAYRE}$ SOLUTION	IDELAY chain delay resolution.	$1/(32 \times 2 \times F_{REF})$	μs
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Spartan 7 FPGAs Data Sheet: DC and AC Switching Characteristics (DS189)

$T_{IDELAYPA}$ T_{JIT}	Pattern dependent period jitter in delay chain for clock pattern.(2)	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23).(3)	± 5	± 5	± 5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23).(4)	± 9	± 9	± 9	ps per tap

$T_{IDELAY_CLK_MAX}$	Maximum frequency of CLK input to IDELAY.	680.00	600.00	600.00	MHz
$T_{IDCCK_CE} / T_{IDCKC_CE}$	CE pin setup/hold with respect to C for IDELAY.	0.16/0.13	0.21/0.16	0.21/0.16	ns
$T_{IDCCK_INC} / T_{IDCKC_INC}$	INC pin setup/hold with respect to C for IDELAY.	0.14/0.18	0.16/0.22	0.16/0.22	ns
$T_{IDCCK_RST} / T_{IDCKC_RST}$	RST pin setup/hold with respect to C for IDELAY.	0.16/0.11	0.18/0.14	0.18/0.14	ns
$T_{IDDO_IDATAIN}$	Propagation delay through IDELAY.	Note 5	Note 5	Note 5	ps

Notes:

1. Average tap delay at 200 MHz = 78 ps, at 300 MHz = 52 ps, and at 400 MHz = 39 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY tap setting. See the timing report for actual values.

Table 26: IO_FIFO Switching Characteristics

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V	0.95V		
		-2	-1	-1L	
IO_FIFO Clock to Out Delays					
T _{OFFCKO_DO}	RDCLK to Q outputs.	0.60	0.68	0.68	ns

Spartan 7 FPGAs Data Sheet: DC and AC Switching Characteristics (DS189)

T_{CKO_FLAG}	Clock to IO_FIFO flags.	0.61	0.77	0.77	ns
Setup/Hold					
T_{CCK_D}/T_{CKC_D}	D inputs to WRCLK.	0.51/0.02	0.58/0.02	0.58/0.02	ns
$T_{IFFCCK_WREN}/T_{IFFCKC_WREN}$	WREN to WRCLK.	0.47/-0.01	0.53/-0.01	0.53/-0.01	ns
$T_{OFFCCK_RDEN}/T_{OFFCKC_RDEN}$	RDEN to RDCLK.	0.58/0.02	0.66/0.02	0.66/0.02	ns
Minimum Pulse Width					
$T_{PWH_IO_FIFO}$	RESET, RDCLK, WRCLK.	2.15	2.15	2.15	ns
$T_{PWL_IO_FIFO}$	RESET, RDCLK, WRCLK.	2.15	2.15	2.15	ns

Maximum Frequency					
F_{MAX}	RDCLK and WRCLK.	200.00	200.00	200.00	MHz

CLB Switching Characteristics

Table 27: CLB Switching Characteristics

Symbol	Description	V _{CCINT}	Operating Voltage and Speed Grade		Units
		1.0V		0.95V	
		-2	-1	-1L	
Combinatorial Delays					
T_{ILO}	An – Dn LUT address to A.	0.11	0.13	0.13	ns, Max

T_{ILO_2}	An – Dn LUT address to AMUX/CMUX.	0.30	0.36	0.36	ns, Max
T_{ILO_3}	An – Dn LUT address to BMUX_A.	0.46	0.55	0.55	ns, Max
T_{ITO}	An – Dn inputs to A – D Q outputs.	1.05	1.27	1.27	ns, Max
T_{AXA}	AX inputs to AMUX output.	0.69	0.84	0.84	ns, Max
T_{AXB}	AX inputs to BMUX output.	0.66	0.83	0.83	ns, Max
T_{AXC}	AX inputs to CMUX output.	0.68	0.82	0.82	ns, Max
T_{AXD}	AX inputs to DMUX output.	0.75	0.90	0.90	ns, Max

T_{BxB}	BX inputs to BMUX output.	0.57	0.69	0.69	ns, Max
T_{BxD}	BX inputs to DMUX output.	0.69	0.82	0.82	ns, Max
T_{CxC}	CX inputs to CMUX output.	0.48	0.58	0.58	ns, Max
T_{CxD}	CX inputs to DMUX output.	0.59	0.71	0.71	ns, Max
T_{DxD}	DX inputs to DMUX output.	0.58	0.70	0.70	ns, Max

Sequential Delays

T_{CKO}	Clock to AQ – DQ outputs.	0.44	0.53	0.53	ns, Max
T_{SHCKO}	Clock to AMUX – DMUX outputs.	0.53	0.66	0.66	ns, Max

Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK

T_{AS}/T_{AH}	AN – DN input to CLK on A – D flip- flops.	0.09/0.14	0.11/0.18	0.11/0.18	ns, Min
T_{DICK}/T_{CK} DI	AX – DX input to CLK on A – D flip- flops.	0.07/0.21	0.09/0.26	0.09/0.26	ns, Min
	AX – DX input through MUXs and/or carry logic to CLK on A – D flip- flops.	0.66/0.09	0.81/0.11	0.81/0.11	ns, Min
T_{CECK_CL} B/ T_{CKCE_CL} B	CE input to CLK on A – D flip- flops.	0.17/0.00	0.21/0.01	0.21/0.01	ns, Min

T_{SRCK}/T_C KSR	SR input to CLK on A – D flip-flops.	0.43/0.04	0.53/0.05	0.53/0.05	ns, Min
Set/Reset					
T_{SRMIN}	SR input minimum pulse width.	0.78	1.04	1.04	ns, Min
T_{RQ}	Delay from SR input to AQ – DQ flip-flops.	0.59	0.71	0.71	ns, Max
T_{CEO}	Delay from CE input to AQ – DQ flip-flops.	0.58	0.70	0.70	ns, Max
F_{TOG}	Toggle frequency (for export control).	1286	1098	1098	MHz

CLB Distributed RAM Switching Characteristics

(SLICEM Only)

Table 28: CLB Distributed RAM Switching Characteristics

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V	0.95V		
		-2	-1	-1L	
Sequential Delays					
T _{SHCKO}	Clock to A – B outputs.	1.09	1.32	1.32	ns, Max
T _{SHCKO_1}	Clock to AMUX – BMUX outputs.	1.53	1.86	1.86	ns, Max
Setup and Hold Times Before/After Clock CLK					
T _{DS_LRAM} / T _{DH_LRAM}	A – D inputs to CLK.	0.60/0.30	0.72/0.35	0.72/0.35	ns, Min

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T_{AS_LRAM} / T_{AH_LRAM}	Address An inputs to clock.	0.30/0.60	0.37/0.70	0.37/0.70	ns, Min
	Address An inputs through MUXs and/or carry logic to clock.	0.77/0.21	0.94/0.26	0.94/0.26	ns, Min
T_{WS_LRAM} / T_{WH_LRAM}	WE input to clock.	0.43/0.12	0.53/0.17	0.53/0.17	ns, Min
T_{CECK_LRAM} / T_{CKCE_LRAM}	CE input to CLK.	0.44/0.11	0.53/0.17	0.53/0.17	ns, Min
Clock CLK					
T_{MPW_LRAM}	Minimum pulse width.	1.13	1.25	1.25	ns, Min
T_{MCP}	Minimum clock period.	2.26	2.50	2.50	ns, Min

Notes:

1. T_{SHCKO} also represents the CLK to XMUX output. Refer to the timing report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 29: CLB Shift Register Switching Characteristics

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V	0.95V		
		-2	-1	-1L	
Sequential Delays					
T_{REG}	Clock to A – D outputs.	1.33	1.61	1.61	ns, Max
T_{REG_MUX}	Clock to AMUX – DMUX output.	1.77	2.15	2.15	ns, Max

T_{REG_M31}	Clock to DMUX output via M31 output.	1.23	1.46	1.46	ns, Max
Setup and Hold Times Before/After Clock CLK					
T_{WS_SHFR} EG/ T_{WH_SHFR} EG	WE input.	0.41/0.12	0.51/0.17	0.51/0.17	ns, Min
T_{CECK_SH} FREG/ T_{CKCE_SH} FREG	CE input to CLK.	0.42/0.11	0.52/0.17	0.52/0.17	ns, Min
T_{DS_SHFR} EG/ T_{DH_SHFR} EG	A – D inputs to CLK.	0.37/0.37	0.44/0.43	0.44/0.43	ns, Min
Clock CLK					
T_{MPW_SHF} REG	Minimum pulse width.	0.86	0.98	0.98	ns, Min

Block RAM and FIFO Switching Characteristics

Table 30: Block RAM and FIFO Switching Characteristics

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V -2	0.95V -1	0.95V -1L	
Block RAM and FIFO Clock-to-Out Delays					
T _{RCKO_DO} and T _{RCKO_DO} _REG	Clock CLK to DOUT output (without output register). (1)(2)	2.13	2.46	2.46	ns, Max
	Clock CLK to DOUT output (with output register). (3)(4)	0.74	0.89	0.89	ns, Max

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$T_{RCKO_DO_ECC}$ and $T_{RCKO_DO_ECC_REG}$	Clock CLK to DOUT output with ECC (without output register). (1)(2)	3.04	3.84	3.84	ns, Max
	Clock CLK to DOUT output with ECC (with output register). (3)(4)	0.81	0.94	0.94	ns, Max

$T_{RCKO_DO_CASCOUT}$ and $T_{RCKO_DO_CASCOUT_REG}$	Clock CLK to DOUT output with cascade (without output register). (1)	2.88	3.30	3.30	ns, Max
	Clock CLK to DOUT output with cascade (with output register). (3)	1.28	1.46	1.46	ns, Max
T_{RCKO_FLAG}	Clock CLK to FIFO flags outputs.(5)	0.87	1.05	1.05	ns, Max
$T_{RCKO_POINTER}$	Clock CLK to FIFO pointers outputs.(6)	1.02	1.15	1.15	ns, Max

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$T_{RCKO_PARITY_ECC}$	Clock CLK to ECCPARITY in ECC encode only mode.	0.85	0.94	0.94	ns, Max
$T_{RCKO_SD_BIT_ECC}$ and $T_{RCKO_SD_BIT_ECC_REG}$	Clock CLK to BITERR (without output register).	2.81	3.55	3.55	ns, Max
	Clock CLK to BITERR (with output register).	0.76	0.89	0.89	ns, Max

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T_{RCKO_RD} ADDR_ECC and T_{RCKO_RD} ADDR_ECC _REG	Clock CLK to RDADDR output with ECC (without output register).	0.88	1.07	1.07	ns, Max
	Clock CLK to RDADDR output with ECC (with output register).	0.93	1.08	1.08	ns, Max
Setup and Hold Times Before/After Clock CLK					
T_{RCCK_AD} DRA/ T_{RCKC_AD} DRA	ADDR inputs.(7)	0.49/0.33	0.57/0.36	0.57/0.36	ns, Min

$T_{RDCK_DI_WF_NC}$ / $T_{RCKD_DI_WF_NC}$	Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode.(8)	0.65/0.63	0.74/0.67	0.74/0.67	ns, Min
$T_{RDCK_DI_RF}$ / $T_{RCKD_DI_RF}$	Data input setup/hold time when block RAM is configured in READ_FIRST mode.(8)	0.22/0.34	0.25/0.41	0.25/0.41	ns, Min
$T_{RDCK_DI_ECC}$ / $T_{RCKD_DI_ECC}$	DIN inputs with block RAM ECC in standard mode.(8)	0.55/0.46	0.63/0.50	0.63/0.50	ns, Min

$T_{RDCK_DI_ECCW}$ / $T_{RCKD_DI_ECCW}$	DIN inputs with block RAM ECC encode only.(8)	1.02/0.46	1.17/0.50	1.17/0.50	ns, Min
$T_{RDCK_DI_ECC_FIFO}$ / $T_{RCKD_DI_ECC_FIFO}$	DIN inputs with FIFO ECC in standard mode.(8)	1.15/0.59	1.32/0.64	1.32/0.64	ns, Min
$T_{RCCK_INJECTBITERR}$ / $T_{RCKC_INJECTBITERR}$	Inject single/double bit error in ECC mode.	0.64/0.37	0.74/0.40	0.74/0.40	ns, Min
T_{RCCK_EN} / T_{RCKC_EN}	Block RAM enable (EN) input.	0.39/0.21	0.45/0.23	0.45/0.23	ns, Min
T_{RCCK_REGCE} / T_{RCKC_REGCE}	CE input of output register.	0.29/0.15	0.36/0.16	0.36/0.16	ns, Min

Spartan 7 FPGAs Data Sheet: DC and AC Switching Characteristics (DS189)

T_{RCCK_RS} $T_{REG}/$ T_{RCKC_RS} T_{REG}	Synchronous RSTREG input.	0.32/0.07	0.35/0.07	0.35/0.07	ns, Min
T_{RCCK_RS} $T_{RAM}/$ T_{RCKC_RS} T_{RAM}	Synchronous RSTRAM input.	0.34/0.43	0.36/0.46	0.36/0.46	ns, Min
T_{RCCK_WE} $A/T_{RCKC_}$ WEA	Write enable (WE) input (block RAM only).	0.48/0.19	0.54/0.20	0.54/0.20	ns, Min
T_{RCCK_WR} $EN/$ T_{RCKC_WR} EN	WREN FIFO inputs.	0.46/0.35	0.47/0.43	0.47/0.43	ns, Min
T_{RCCK_RD} $EN/$ T_{RCKC_RD} EN	RDEN FIFO inputs.	0.43/0.35	0.43/0.43	0.43/0.43	ns, Min
Reset Delays					

Spartan 7 FPGAs Data Sheet: DC and AC Switching Characteristics (DS189)

$T_{\text{RCO_FLAG}}$	Reset RST to FIFO flags/pointers.(9)	0.98	1.10	1.10	ns, Max
$T_{\text{RREC_RST}}/T_{\text{RREM_RST}}$	FIFO reset recovery and removal timing.(10)	2.07/-0.81	2.37/-0.81	2.37/-0.81	ns, Max
Maximum Frequency					
$F_{\text{MAX_BRAM_WF_NC}}$	Block RAM (write first and no change modes) when not in SDP RF mode.	460.83	388.20	388.20	MHz

Spartan 7 FPGAs Data Sheet: DC and AC Switching Characteristics (DS189)

$F_{MAX_BRAM_RF_PERFORMANCE}$	Block RAM (read first, performance mode) when in SDP RF mode but no address overlap between port A and port B.	460.83	388.20	388.20	MHz
$F_{MAX_BRAM_RF_DELAYED_WRITE}$	Block RAM (read first, delayed write mode) when in SDP RF mode and there is possibility of overlap between port A and port B addresses.	404.53	339.67	339.67	MHz

Spartan 7 FPGAs Data Sheet: DC and AC Switching Characteristics (DS189)

$F_{MAX_CAS_WF_NC}$	Block RAM cascade (write first, no change mode) when cascade but not in RF mode.	418.59	345.78	345.78	MHz
$F_{MAX_CAS_RF_PERFORMANCE}$	Block RAM cascade (read first, performance mode) when in cascade with RF mode and no possibility of address overlap/one port is disabled.	418.59	345.78	345.78	MHz

Spartan 7 FPGAs Data Sheet: DC and AC Switching Characteristics (DS189)

$F_{\text{MAX_CAS_RF_DELAYED_WRITE}}$	When in cascade RF mode and there is a possibility of address overlap between port A and port B.	362.19	297.35	297.35	MHz
$F_{\text{MAX_FIFO}}$	FIFO in all modes without ECC.	460.83	388.20	388.20	MHz
$F_{\text{MAX_ECC}}$	Block RAM and FIFO in ECC configuration.	365.10	297.53	297.53	MHz

Notes:

1. T_{RCKO_DOR} includes T_{RCKO_DOW} , T_{RCKO_DOPR} , and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
2. These parameters also apply to synchronous FIFO with $DO_REG = 0$.
3. T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
4. These parameters also apply to multi-rate (asynchronous) and synchronous FIFO with $DO_REG = 1$.
5. T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY} , T_{RCKO_AFULL} , T_{RCKO_EMPTY} , T_{RCKO_FULL} , T_{RCKO_RDERR} , T_{RCKO_WRERR} .
6. $T_{RCKO_POINTERS}$ includes both $T_{RCKO_RDCOUNT}$ and $T_{RCKO_WRCOUNT}$.
7. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
8. These parameters include both A and B inputs as well as the parity inputs of A and B.
9. T_{RCKO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
10. RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

DSP48E1 Switching Characteristics

Table 31: DSP48E1 Switching Characteristics

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V	0.95V		
		-2	-1	-1L	
Setup and Hold Times of Data/Control Pins to the Input Register Clock					
T _{DSPDCK_A_AREG} / T _{DSPCKD_A_AREG}	A input to A register CLK.	0.30/0.13	0.37/0.14	0.37/0.14	ns
T _{DSPDCK_B_BREG} / T _{DSPCKD_B_BREG}	B input to B register CLK.	0.38/0.16	0.45/0.18	0.45/0.18	ns
T _{DSPDCK_C_CREG} / T _{DSPCKD_C_CREG}	C input to C register CLK.	0.20/0.19	0.24/0.21	0.24/0.21	ns

$T_{\text{DSPDCK_D_DREG}}$ $T_{\text{DSPCKD_D_DREG}}$	D input to D register CLK.	0.32/0.27	0.42/0.27	0.42/0.27	ns
$T_{\text{DSPDCK_ACIN_AREG}}$ $T_{\text{DSPCKD_ACIN_AREG}}$	ACIN input to A register CLK.	0.27/0.13	0.32/0.14	0.32/0.14	ns
$T_{\text{DSPDCK_BCIN_BREG}}$ $T_{\text{DSPCKD_BCIN_BREG}}$	BCIN input to B register CLK.	0.29/0.16	0.36/0.18	0.36/0.18	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock					
$T_{\text{DSPDCK_A, B_MREG_MULT}}$ $T_{\text{DSPCKD_A, B_MREG_MULT}}$	{A, B} input to M register CLK using multiplier.	2.76/−0.01	3.29/−0.01	3.29/−0.01	ns

$T_{\text{DSPDCK}}\{A, D\}_{\text{ADREG}}$ $T_{\text{DSPCKD}}\{A, D\}_{\text{ADREG}}$	{A, D} input to AD register CLK.	1.48/–0.02	1.76/–0.02	1.76/–0.02	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock					
$T_{\text{DSPDCK}}\{A, B\}_{\text{PREG_MULT}}$ $T_{\text{DSPCKD}}\{A, B\}_{\text{PREG_MULT}}$	{A, B} input to P register CLK using multiplier.	4.60/–0.28	5.48/–0.28	5.48/–0.28	ns
$T_{\text{DSPDCK}}\{D\}_{\text{PREG_MULT}}$ $T_{\text{DSPCKD}}\{D\}_{\text{PREG_MULT}}$	D input to P register CLK using multiplier.	4.50/–0.73	5.35/–0.73	5.35/–0.73	ns

$T_{\text{DSPDCK}}\{\text{A, B}\}$ _PREG/ $T_{\text{DSPCKD}}\{\text{A, B}\}$ _PREG	A or B input to P register CLK not using multiplier.	1.98/–0.28	2.35/–0.28	2.35/–0.28	ns
$T_{\text{DSPDCK}}\text{C_PREG}/$ $T_{\text{DSPCKD}}\text{C_PREG}$	C input to P register CLK not using multiplier.	1.76/–0.26	2.10/–0.26	2.10/–0.26	ns
$T_{\text{DSPDCK}}\text{PCIN_PREG}$ / $T_{\text{DSPCKD}}\text{PCIN_PREG}$	PCIN input to P register CLK.	1.51/–0.15	1.80/–0.15	1.80/–0.15	ns
Setup and Hold Times of the CE Pins					
$T_{\text{DSPDCK}}\{\text{CEA;CEB}\}\{\text{AREG;BREG}\}$ / $T_{\text{DSPCKD}}\{\text{CEA;CEB}\}\{\text{AREG;BREG}\}$	{CEA; CEB} input to {A; B} register CLK.	0.42/0.08	0.52/0.11	0.52/0.11	ns

$T_{DSPDCK_CEC_CREG} / T_{DSPCKD_CEC_CREG}$	CEC input to C register CLK.	0.34/0.11	0.42/0.13	0.42/0.13	ns
$T_{DSPDCK_CED_DREG} / T_{DSPCKD_CED_DREG}$	CED input to D register CLK.	0.43/-0.03	0.52/-0.03	0.52/-0.03	ns
$T_{DSPDCK_CEM_MREG} / T_{DSPCKD_CEM_MREG}$	CEM input to M register CLK.	0.21/0.20	0.27/0.23	0.27/0.23	ns
$T_{DSPDCK_CEP_PREG} / T_{DSPCKD_CEP_PREG}$	CEP input to P register CLK.	0.43/0.01	0.53/0.01	0.53/0.01	ns
Setup and Hold Times of the RST Pins					

$T_{DSPDCK_}$ RSTA; RSTB}_{AR EG; BREG}/ $T_{DSPCKD_}$ RSTA; RSTB}_{AR EG; BREG}	{RSTA, RSTB} input to {A, B} register CLK.	0.46/0.13	0.55/0.15	0.55/0.15	ns
$T_{DSPDCK_}$ RSTC_CRE G/ $T_{DSPCKD_}$ RSTC_CRE G	RSTC input to C register CLK.	0.08/0.11	0.09/0.12	0.09/0.12	ns
$T_{DSPDCK_}$ RSTD_DRE G/ $T_{DSPCKD_}$ RSTD_DRE G	RSTD input to D register CLK	0.50/0.08	0.59/0.09	0.59/0.09	ns
$T_{DSPDCK_}$ RSTM_MRE G/ $T_{DSPCKD_}$ RSTM_MRE G	RSTM input to M register CLK	0.23/0.24	0.27/0.28	0.27/0.28	ns

$T_{\text{DSPDCK_RSTP_PRE}}/$ $T_{\text{DSPCKD_RSTP_PRE}}/$ G	RSTP input to P register CLK	0.30/0.01	0.35/0.01	0.35/0.01	ns
Combinatorial Delays from Input Pins to Output Pins					
$T_{\text{DSPDO_A_CARRYOUT_MULT}}$	A input to CARRYOUT output using multiplier.	4.35	5.18	5.18	ns
$T_{\text{DSPDO_D_P_MULT}}$	D input to P output using multiplier.	4.26	5.07	5.07	ns
$T_{\text{DSPDO_B_P}}$	B input to P output not using multiplier.	1.75	2.08	2.08	ns
$T_{\text{DSPDO_C_P}}$	C input to P output.	1.53	1.82	1.82	ns
Combinatorial Delays from Input Pins to Cascading Output Pins					

$T_{DSPDO_{\{A; B\}_{ACOUT; BCOUT}}}$	{A, B} input to {ACOUT, BCOUT} output.	0.63	0.74	0.74	ns
$T_{DSPDO_{\{A, B\}_{CARRYC ASCOUT_MULT}}}$	{A, B} input to CARRYC ASCOUT output using multiplier.	4.65	5.54	5.54	ns
$T_{DSPDO_{D_CARRYC ASCOUT_MULT}}$	D input to CARRYC ASCOUT output using multiplier.	4.54	5.40	5.40	ns
$T_{DSPDO_{\{A, B\}_{CARRYC ASCOUT}}}$	{A, B} input to CARRYC ASCOUT output not using multiplier.	2.03	2.41	2.41	ns
$T_{DSPDO_{C_CARRYC ASCOUT}}$	C input to CARRYC ASCOUT output.	1.81	2.15	2.15	ns

Combinatorial Delays from Cascading Input Pins to All Output Pins

$T_{\text{DSPDO_A}}$ CIN_P_MUL T	ACIN input to P output using multiplier.	4.19	5.00	5.00	ns
$T_{\text{DSPDO_A}}$ CIN_P	ACIN input to P output not using multiplier.	1.57	1.88	1.88	ns
$T_{\text{DSPDO_A}}$ CIN_ACOU	ACIN input to ACOU output.	0.44	0.53	0.53	ns
$T_{\text{DSPDO_A}}$ CIN_CARRY CASCOU_ MULT	ACIN input to CARRYC ASCOU output using multiplier.	4.47	5.33	5.33	ns

$T_{\text{DSPDO_A}}$ CIN_CARRY CASCOUT	ACIN input to CARRYC ASCOUT output not using multiplier.	1.85	2.21	2.21	ns
$T_{\text{DSPDO_P}}$ CIN_P	PCIN input to P output.	1.28	1.52	1.52	ns
$T_{\text{DSPDO_P}}$ CIN_CARRY CASCOUT	PCIN input to CARRYC ASCOUT output.	1.56	1.85	1.85	ns
Clock to Outs from Output Register Clock to Output Pins					
$T_{\text{DSPCKO_}}$ P_PREG	CLK PREG to P output.	0.37	0.44	0.44	ns
$T_{\text{DSPCKO_}}$ CARRYCAS COUT_PREG	CLK PREG to CARRYC ASCOUT output.	0.59	0.69	0.69	ns

Clock to Outs from Pipeline Register Clock to Output Pins

$T_{\text{DSPCKO_P_MREG}}$	CLK MREG to P output.	1.93	2.31	2.31	ns
$T_{\text{DSPCKO_CARRYCAS_COUT_MREG}}$	CLK MREG to CARRYC ASCOUT output.	2.21	2.64	2.64	ns
$T_{\text{DSPCKO_P_ADREG_MULT}}$	CLK ADREG to P output using multiplier.	3.10	3.69	3.69	ns
$T_{\text{DSPCKO_CARRYCAS_COUT_ADREG_MULT}}$	CLK ADREG to CARRYC ASCOUT output using multiplier.	3.38	4.02	4.02	ns
Clock to Outs from Input Register Clock to Output Pins					
$T_{\text{DSPCKO_P_AREG_MULT}}$	CLK AREG to P output using multiplier.	4.51	5.37	5.37	ns

$T_{\text{DSPCKO_P_BREG}}$	CLK BREG to P output not using multiplier.	1.87	2.22	2.22	ns
$T_{\text{DSPCKO_P_CREG}}$	CLK CREG to P output not using multiplier.	1.93	2.30	2.30	ns
$T_{\text{DSPCKO_P_DREG_MULT}}$	CLK DREG to P output using multiplier.	4.48	5.32	5.32	ns
Clock to Outs from Input Register Clock to Cascading Output Pins					
$T_{\text{DSPCKO_}\{ACOUT; BCOUT\}_\{AREG; BREG\}}$	CLK (ACOUT, BCOUT) to {A,B} register output.	0.73	0.87	0.87	ns

$T_{\text{DSPCKO_CARRYCAS_COUT_}\{A\text{REG, BREG}\}_\text{MULT}}$	CLK (AREG, BREG) to CARRYC ASCOUT output using multiplier.	4.79	5.70	5.70	ns
$T_{\text{DSPCKO_CARRYCAS_COUT_BREG}}$	CLK BREG to CARRYC ASCOUT output not using multiplier.	2.15	2.55	2.55	ns
$T_{\text{DSPCKO_CARRYCAS_COUT_DREG_MULT}}$	CLK DREG to CARRYC ASCOUT output using multiplier.	4.76	5.65	5.65	ns
$T_{\text{DSPCKO_CARRYCAS_COUT_CREG}}$	CLK CREG to CARRYC ASCOUT output.	2.21	2.63	2.63	ns
Maximum Frequency					

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F_{MAX}	With all registers used.	550.66	464.25	464.25	MHz
$F_{MAX_PAT_DET}$	With pattern detector.	465.77	392.93	392.93	MHz
$F_{MAX_MULT_NOMREG}$	Two register multiply without MREG.	305.62	257.47	257.47	MHz
$F_{MAX_MULT_NOMREG_PATDET}$	Two register multiply without MREG with pattern detect.	277.62	233.92	233.92	MHz
$F_{MAX_PRE_ADD_MULT_NOADREG}$	Without ADREG.	346.26	290.44	290.44	MHz

F_{MAX_PRE} ADD_MULT _NOADREG _PATDET	Without ADREG with pattern detect.	346.26	290.44	290.44	MHz
F_{MAX_NOP} IPELINERE G	Without pipeline registers (MREG, ADREG).	227.01	190.69	190.69	MHz
F_{MAX_NOP} IPELINERE G_PATDET	Without pipeline registers (MREG, ADREG) with pattern detect.	211.15	177.43	177.43	MHz

Clock Buffers and Networks

Table 32: Global Clock Switching Characteristics (Including BUFGCTRL)

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V	0.95V		
		-2	-1	-1L	
T _{BCCCK_CE} /T _{BCCCK_C} CE(1)	CE pins setup/hold	0.13/0.40	0.16/0.41	0.16/0.41	ns
T _{BCCCK_S} /T _{BCCCK_S} (1)	S pins setup/hold	0.13/0.40	0.16/0.41	0.16/0.41	ns
T _{BCCCKO_O} (2)	BUFGCTRL delay from I0/I1 to O.	0.09	0.10	0.10	ns
Maximum Frequency					
F _{MAX_BUF} G	Global clock tree (BUFG).	628.00	464.00	464.00	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCKC_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.

2. T_{BGCKO_O} (BUFG delay from I0 to O) values are the same as T_{BCKO_O} values.

Table 33: Input/Output Clock Switching Characteristics (BUFIO)

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V	0.95V		
		-2	-1	-1L	
T_{BIOCKO_O}	Clock to out delay from I to O.	1.26	1.54	1.54	ns
Maximum Frequency					

$F_{\text{MAX_BUFI O}}$	I/O clock tree (BUFIO).	680.00	600.00	600.00	MHz
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Table 34: Regional Clock Buffer Switching Characteristics (BUFR)

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V	0.95V		
		-2	-1	-1L	
$T_{\text{BRCKO_O}}$	Clock to out delay from I to O.	0.76	0.99	0.99	ns
$T_{\text{BRCKO_O_BYP}}$	Clock to out delay from I to O with Divide Bypass attribute set.	0.39	0.52	0.52	ns

T_{BRDO_O}	Propagation delay from CLR to O.	0.85	1.09	1.09	ns
Maximum Frequency					
F_{MAX_BUF} R(1)	Regional clock tree (BUFR).	375.00	315.00	315.00	MHz
Notes:					
1. The maximum input frequency to the BUFR is the BUFRIO F_{MAX} frequency.					

Table 35: Horizontal Clock Buffer Switching Characteristics (BUFH)

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V	0.95V		
		-2	-1	-1L	
T_{BHCKO_O}	BUFH delay from I to O.	0.11	0.13	0.13	ns

$T_{BHCKC_CE}/T_{BHCKC_CE}$	CE pin setup and hold.	0.22/0.15	0.28/0.21	0.28/0.21	ns
Maximum Frequency					
F_{MAX_BUFH}	Horizontal clock buffer (BUFH).	628.00	464.00	464.00	MHz

Table 36: Duty Cycle Distortion and Clock-Tree Skew

Symbol	Description	Device	V _{CCINT}	Operating Voltage and Speed Grade	Units
			1.0V	0.95V	
			-2	-1	-1L

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$T_{\text{DCD_CLK}}$	Global clock tree duty-cycle distortion.(1)	All	0.20	0.20	0.20	ns
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T _{CKSKE} W	Global clock tree skew.(2)	XC7S6	0.05	0.06	0.06	ns
		XC7S15	0.05	0.06	0.06	ns
		XC7S25	0.26	0.26	0.26	ns
		XC7S50	0.26	0.26	0.26	ns
		XC7S75	0.33	0.36	0.36	ns
		XC7S100	0.33	0.36	0.36	ns
		XA7S6	0.05	0.06	N/A	ns
		XA7S15	0.05	0.06	N/A	ns
		XA7S25	0.26	0.26	N/A	ns
		XA7S50	0.26	0.26	N/A	ns
		XA7S75	0.33	0.36	N/A	ns
		XA7S100	0.33	0.36	N/A	ns

T_{DCD_BUFIO}	I/O clock tree duty cycle distortion.	All	0.14	0.14	0.14	ns
$T_{BUFIOSKEW}$	I/O clock tree skew across one clock region.	All	0.03	0.03	0.03	ns
T_{DCD_UFR}	Regional clock tree duty cycle distortion.	All	0.18	0.18	0.18	ns

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the I/O flip flops. For all I/O standards, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.

2. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx timing analysis tools to evaluate clock skew specific to your application.

MMCM Switching Characteristics

Table 37: MMCM Specification

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V	0.95V		
		-2	-1	-1L	
MMCM_F ₁ NMAX	Maximum input clock frequency.	800.00	800.00	800.00	MHz
MMCM_F ₁ NMIN	Minimum input clock frequency.	10.00	10.00	10.00	MHz
MMCM_F ₁ NJITTER	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max			

MMCM_F ₁ NDUTY	Allowable input duty cycle: 10 —49 MHz.	25	25	25	%
	Allowable input duty cycle: 50 —199 MHz.	30	30	30	%
	Allowable input duty cycle: 200 —399 MHz.	35	35	35	%
	Allowable input duty cycle: 400 —499 MHz.	40	40	40	%
	Allowable input duty cycle: > 500 MHz.	45	45	45	%

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MMCM_F MIN_PSCLK	Minimum dynamic phase- shift clock frequency.	0.01	0.01	0.01	MHz
MMCM_F MAX_PSCLK	Maximum dynamic phase- shift clock frequency.	500.00	450.00	450.00	MHz
MMCM_F VCOMIN	Minimum MMCM VCO frequency.	600.00	600.00	600.00	MHz
MMCM_F VCOMAX	Maximum MMCM VCO frequency.	1440.00	1200.00	1200.00	MHz

Spartan 7 FPGAs Data Sheet: DC and AC Switching Characteristics (DS189)

MMCM_F BANDWIDTH	Low MMCM bandwidth at typical. (1)	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical. (1)	4.00	4.00	4.00	MHz
MMCM_T STATPHAS OFFSET	Static phase offset of the MMCM outputs.(2)	0.12	0.12	0.12	ns
MMCM_T OUTJITTER	MMCM output jitter.	Note 3			
MMCM_T OUTDUTY	MMCM output clock duty- cycle precision. (4)	0.20	0.20	0.20	ns

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MMCM_T _L LOCKMAX	MMCM maximum lock time.	100.00	100.00	100.00	μs
MMCM_F OUTMAX	MMCM maximum output frequency.	800.00	800.00	800.00	MHz
MMCM_F OUTMIN	MMCM minimum output frequency. (5)(6)	4.69	4.69	4.69	MHz
MMCM_T EXTFDVAR	External clock feedback variation.	< 20% of clock input period or 1 ns Max			
MMCM_R ST _{MINPUL} SE	Minimum reset pulse width.	5.00	5.00	5.00	ns
MMCM_F PFDMAX	Maximum frequency at the phase frequency detector.	500.00	450.00	450.00	MHz

MMCM_F PFDMIN	Minimum frequency at the phase frequency detector.	10.00	10.00	10.00	MHz
MMCM_T FBDELAY	Maximum delay in the feedback path.	3 ns Max or one CLKIN cycle			
MMCM Switching Characteristics Setup and Hold					
T_{MMCMDC} K_PSEN/ T_{MMCMCK} D_PSEN	Setup and hold of phase-shift enable.	1.04/0.00	1.04/0.00	1.04/0.00	ns
T_{MMCMDC} K_PSINCDE C/ T_{MMCMCK} D_PSINCDE C	Setup and hold of phase-shift increment/decrement.	1.04/0.00	1.04/0.00	1.04/0.00	ns

T_{MMCMCK} O_PSDONE	Phase shift clock-to-out of PSDONE.	0.68	0.81	0.81	ns
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK					
T_{MMCMDC} K_DADDR/ T_{MMCMCK} D_DADDR	DADDR setup/hold ·	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T_{MMCMDC} K_DI/ T_{MMCMCK} D_DI	DI setup/hold ·	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T_{MMCMDC} K_DEN/ T_{MMCMCK} D_DEN	DEN setup/hold ·	1.97/0.00	2.29/0.00	2.29/0.00	ns, Min
T_{MMCMDC} K_DWE/ T_{MMCMCK} D_DWE	DWE setup/hold ·	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T_{MMCMCK} O_DRDY	CLK to out of DRDY.	0.72	0.99	0.99	ns, Max

F_{DCK}	DCLK frequency.	200.00	200.00	200.00	MHz, Max
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Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard [Ref 8].
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.
6. When `CLKOUT4_CASCADE = TRUE`, $MMCM_{F_{OUTMIN}}$ is 0.036 MHz.

PLL Switching Characteristics

Table 38: PLL Specification

Symbol	Description	V _{CCINT}	Operating Voltage and Speed Grade		Units
			1.0V	0.95V	
		-2	-1	-1L	

Spartan 7 FPGAs Data Sheet: DC and AC Switching Characteristics (DS189)

PLL_F _{INM} AX	Maximum input clock frequency.	800.00	800.00	800.00	MHz
PLL_F _{INM} N	Minimum input clock frequency.	19.00	19.00	19.00	MHz
PLL_F _{INJ} ITTER	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max			

Spartan 7 FPGAs Data Sheet: DC and AC Switching Characteristics (DS189)

PLL_F _{IND} UTY	Allowable input duty cycle: 19—49 MHz.	25	25	25	%
	Allowable input duty cycle: 50—199 MHz.	30	30	30	%
	Allowable input duty cycle: 200—399 MHz.	35	35	35	%
	Allowable input duty cycle: 400—499 MHz.	40	40	40	%
	Allowable input duty cycle: >500 MHz.	45	45	45	%
PLL_F _{VCO} MIN	Minimum PLL VCO frequency.	800.00	800.00	800.00	MHz

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PLL_F _{VCO} MAX	Maximum PLL VCO frequency.	1866.00	1600.00	1600.00	MHz
PLL_F _{BAN} DWIDTH	Low PLL bandwidth at typical.	1.00	1.00	1.00	MHz
	High PLL bandwidth at typical. (1)	4.00	4.00	4.00	MHz
PLL_T _{STA} TPHAOFFS ET	Static phase offset of the PLL outputs.(2)	0.12	0.12	0.12	ns
PLL_T _{OUT} JITTER	PLL output jitter.	Note 3			
PLL_T _{OUT} DUTY	PLL output clock duty-cycle precision. (4)	0.20	0.20	0.20	ns

Spartan 7 FPGAs Data Sheet: DC and AC Switching Characteristics (DS189)

PLL_T _{LOC} KMAX	PLL maximum lock time.	100.00	100.00	100.00	μs
PLL_F _{OUT} MAX	PLL maximum output frequency.	800.00	800.00	800.00	MHz
PLL_F _{OUT} MIN	PLL minimum output frequency. (5)	6.25	6.25	6.25	MHz
PLL_T _{EXT} FDVAR	External clock feedback variation.	< 20% of clock input period or 1 ns Max			
PLL_RST MINPULSE	Minimum reset pulse width.	5.00	5.00	5.00	ns
PLL_F _{PFD} MAX	Maximum frequency at the phase frequency detector.	500.00	450.00	450.00	MHz

PLL_F _{PFD} MIN	Minimum frequency at the phase frequency detector.	19.00	19.00	19.00	MHz
PLL_T _{FBD} ELAY	Maximum delay in the feedback path.	3 ns Max or one CLKIN cycle			
Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK					
T _{PLLDCK_} DADDR/ T _{PLLCKD_} DADDR	Setup and hold of D address.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T _{PLLDCK_} DI/ T _{PLLCKD_} DI	Setup and hold of D input.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T _{PLLDCK_} DEN/ T _{PLLCKD_} DEN	Setup and hold of D enable.	1.97/0.00	2.29/0.00	2.29/0.00	ns, Min

$T_{\text{PLLCKD_DWE}}$	Setup and hold of D write enable.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
$T_{\text{PLLCKO_DRDY}}$	CLK to out of DRDY.	0.72	0.99	0.99	ns, Max
F_{DCK}	DCLK frequency.	200.00	200.00	200.00	MHz, Max

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard [Ref 8].
4. Includes global clock buffer.
5. Calculated as $F_{\text{VCO}}/128$ assuming output duty cycle is 50%.

Device Pin-to-Pin Output Parameter Guidelines

Table 39: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)(1)

Symbol	Description	Device	V _{CCINT}	Operating Voltage and Speed Grade	Units
			1.0V	0.95V	
			-2	-1	-1L

SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, without MMCM/PLL.

T _{ICKOF}	Clock-capable clock input and OUTFFF at pins/banks closest to the BUFGs without MMCM/PLL (near clock region). (2)	XC7S6	5.55	6.50	6.50	ns
		XC7S15	5.55	6.50	6.50	ns
		XC7S25	5.55	6.44	6.44	ns
		XC7S50	5.71	6.62	6.62	ns
		XC7S75	5.73	6.71	6.71	ns
		XC7S100	5.73	6.71	6.71	ns
		XA7S6	5.55	6.50	N/A	ns
		XA7S15	5.55	6.50	N/A	ns
		XA7S25	5.55	6.44	N/A	ns
		XA7S50	5.71	6.62	N/A	ns
		XA7S75	5.73	6.71	N/A	ns
		XA7S100	5.73	6.71	N/A	ns

Notes:

1. [This table](#) lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

2. [Refer to the](#) Die Level Bank Numbering Overview section of the 7 Series FPGA Packaging and Pinout Specification (UG475) [\[Ref 4\]](#).

Table 40: [Clock-Capable Clock Input to Output Delay Without MMCM/PLL \(Far Clock Region\)\(1\)](#)

Symbol	Description	Device	V _{CCINT}	Operating Voltage and Speed Grade	Units
			1.0V	0.95V	
			-2	-1	-1L

SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, without MMCM/PLL.

T _{ICKOFF} AR	Clock-capable clock input and OUTF _{FF} at pins/banks farthest from the BUFGs without MMCM/PLL (far clock region). (2)	XC7S6	5.55	6.50	6.50	ns
		XC7S15	5.55	6.50	6.50	ns
		XC7S25	5.55	6.44	6.44	ns
		XC7S50	5.71	6.62	6.62	ns
		XC7S75	6.01	7.02	7.02	ns
		XC7S100	6.01	7.02	7.02	ns
		XA7S6	5.55	6.50	N/A	ns
		XA7S15	5.55	6.50	N/A	ns
		XA7S25	5.55	6.44	N/A	ns
		XA7S50	5.71	6.62	N/A	ns
		XA7S75	6.01	7.02	N/A	ns
		XA7S100	6.01	7.02	N/A	ns

Notes:

1. [This table](#) lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

2. [Refer to the](#) Die Level Bank Numbering Overview section of the 7 Series FPGA Packaging and Pinout Specification (UG475) [\[Ref 4\]](#).

Table 41: [Clock-Capable Clock Input to Output Delay With MMCM\(1\)](#)

Symbol	Description	Device	V _{CCINT}	Operating Voltage and Speed Grade	Units
			1.0V	0.95V	
			-2	-1	-1L

SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with MMCM.

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T _{ICKO} FM MCMCC	Clock-capable clock input and OUTF _F with MMCM. (2)	XC7S6	1.03	1.03	1.03	ns
		XC7S15	1.03	1.03	1.03	ns
		XC7S25	1.00	1.00	1.00	ns
		XC7S50	1.00	1.00	1.00	ns
		XC7S75	1.00	1.00	1.00	ns
		XC7S100	1.00	1.00	1.00	ns
		XA7S6	1.03	1.03	N/A	ns
		XA7S15	1.03	1.03	N/A	ns
		XA7S25	1.00	1.00	N/A	ns
		XA7S50	1.00	1.00	N/A	ns
		XA7S75	1.00	1.00	N/A	ns
		XA7S100	1.00	1.00	N/A	ns

Notes:

1. [This table](#) lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

2. [MMCM output jitter](#) is already included in the timing calculation.

Table 42: [Clock-Capable Clock Input to Output Delay With PLL\(1\)](#)

Symbol	Description	Device	V _{CCINT}	Operating Voltage and Speed Grade		Units
			1.0V		0.95V	
			-2	-1	-1L	

SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with PLL.

Spartan 7 FPGAs Data Sheet: DC and AC Switching Characteristics (DS189)

T _{ICKOFF} LLCC	Clock-capable clock input and OUTFF with PLL.(2)	XC7S6	0.85	0.85	0.85	ns
		XC7S15	0.85	0.85	0.85	ns
		XC7S25	0.83	0.83	0.83	ns
		XC7S50	0.83	0.83	0.83	ns
		XC7S75	0.83	0.83	0.83	ns
		XC7S100	0.83	0.83	0.83	ns
		XA7S6	0.85	0.85	N/A	ns
		XA7S15	0.85	0.85	N/A	ns
		XA7S25	0.83	0.83	N/A	ns
		XA7S50	0.83	0.83	N/A	ns
		XA7S75	0.83	0.83	N/A	ns
		XA7S100	0.83	0.83	N/A	ns

Notes:

1. [This table](#) lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

2. [PLL output jitter is already included in the timing calculation.](#)

Table 43: Pin-to-Pin, Clock-to-Out using BUFIO

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V	0.95V		
		-2	-1	-1L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with BUFIO.					
T _{ICKOFCS}	Clock to out of I/O clock.	5.61	6.64	6.64	ns

Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 44: Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks

Symbol	Description	Device	V _{CCINT}	Operating Voltage and Speed Grade	Units
			1.0V	0.95V	
			-2	-1	-1L

Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1)

Spartan 7 FPGAs Data Sheet: DC and AC Switching Characteristics (DS189)

$T_{PSFD}/$ T_{PHFD}	Full delay (legacy delay or default delay) global clock input and IFF(2) without MMCM/ PLL with ZHOLD_ DELAY on HR I/O banks.	XC7S6	2.76/– 0.40	3.17/– 0.40	3.17/– 0.40	ns
		XC7S15	2.76/– 0.40	3.17/– 0.40	3.17/– 0.40	ns
		XC7S25	2.67/– 0.37	3.12/– 0.37	3.12/– 0.37	ns
		XC7S50	2.66/– 0.28	3.11/– 0.28	3.11/– 0.28	ns
		XC7S75	2.91/– 0.33	3.36/– 0.33	3.36/– 0.33	ns
		XC7S100	2.91/– 0.33	3.36/– 0.33	3.36/– 0.33	ns
		XA7S6	2.76/– 0.40	3.17/– 0.40	N/A	ns
		XA7S15	2.76/– 0.40	3.17/– 0.40	N/A	ns
		XA7S25	2.67/– 0.37	3.12/– 0.37	N/A	ns

		XA7S50	2.66/ 0.28	3.11/ 0.28	N/A	ns
		XA7S75	2.91/ 0.33	3.36/ 0.33	N/A	ns
		XA7S10 0	2.91/ 0.33	3.36/ 0.33	N/A	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.

2. IFF = Input flip-flop or latch.

Table 45: Clock-Capable Clock Input Setup and Hold With MMCM

Symbol	Description	Device	V _{CCINT}	Operating Voltage and Speed Grade	Units
			1.0V	0.95V	
			-2	-1	-1L

Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15
Standard.(1)(2)

Spartan 7 FPGAs Data Sheet: DC and AC Switching Characteristics (DS189)

T_{PSMMC} MCC/ T_{PHMMC} MCC	No delay clock- capable clock input and IFF(3) with MMCM.	XC7S6	2.73/- 0.59	3.27/- 0.59	3.27/- 0.59	ns
		XC7S15	2.73/- 0.59	3.27/- 0.59	3.27/- 0.59	ns
		XC7S25	2.69/- 0.61	3.21/- 0.61	3.21/- 0.61	ns
		XC7S50	2.81/- 0.62	3.35/- 0.62	3.35/- 0.62	ns
		XC7S75	2.81/- 0.62	3.36/- 0.62	3.36/- 0.62	ns
		XC7S100	2.81/- 0.62	3.36/- 0.62	3.36/- 0.62	ns
		XA7S6	2.73/- 0.59	3.27/- 0.59	N/A	ns
		XA7S15	2.73/- 0.59	3.27/- 0.59	N/A	ns
		XA7S25	2.69/- 0.61	3.21/- 0.61	N/A	ns

		XA7S50	2.81/– 0.62	3.35/– 0.62	N/A	ns
		XA7S75	2.81/– 0.62	3.36/– 0.62	N/A	ns
		XA7S10 0	2.81/– 0.62	3.36/– 0.62	N/A	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.

2. Use [IBIS to determine any duty-cycle distortion incurred using various standards.](#)

3. IFF = [Input flip-flop or latch.](#)

Table 46: [Clock-Capable Clock Input Setup and Hold With PLL](#)

Symbol	Description	Device	V _{CCINT}	Operating Voltage and Speed Grade	Units
			1.0V	0.95V	
			-2	-1	-1L

Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard.(1)(2)

Spartan 7 FPGAs Data Sheet: DC and AC Switching Characteristics (DS189)

$T_{PSPLLCC}$ $T_{PHPLLCC}$	No delay clock-capable clock input and IFF(3) with PLL.	XC7S6	3.07/- 0.17	3.69/- 0.17	3.69/- 0.17	ns
		XC7S15	3.07/- 0.17	3.69/- 0.17	3.69/- 0.17	ns
		XC7S25	3.04/- 0.19	3.64/- 0.19	3.64/- 0.19	ns
		XC7S50	3.15/- 0.19	3.77/- 0.19	3.77/- 0.19	ns
		XC7S75	3.15/- 0.19	3.78/- 0.19	3.78/- 0.19	ns
		XC7S100	3.15/- 0.19	3.78/- 0.19	3.78/- 0.19	ns
		XA7S6	3.07/- 0.17	3.69/- 0.17	N/A	ns
		XA7S15	3.07/- 0.17	3.69/- 0.17	N/A	ns
		XA7S25	3.04/- 0.19	3.64/- 0.19	N/A	ns

		XA7S50	3.15/– 0.19	3.77/– 0.19	N/A	ns
		XA7S75	3.15/– 0.19	3.78/– 0.19	N/A	ns
		XA7S10 0	3.15/– 0.19	3.78/– 0.19	N/A	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.

2. Use [IBIS to determine any duty-cycle distortion incurred using various standards](#).

3. IFF = [Input flip-flop or latch](#).

Table 47: Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V	0.95V		
		-2	-1	-1L	
Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard.					
T _{PSCS} /T _P HCS	Setup and hold of I/O clock.	-0.38/1.46	-0.38/1.73	-0.38/1.76	ns

Table 48: Sample Window

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V	0.95V		
		-2	-1	-1L	

T_{SAMP}	Sampling error at receiver pins.(1)	0.64	0.70	0.70	ns
$T_{\text{SAMP_BU FIO}}$	Sampling error at receiver pins using BUFIO.(2)	0.40	0.46	0.46	ns

Notes:

1. This parameter indicates the total sampling error of the Spartan 7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:

- CLK0 MMCM jitter
- MMCM accuracy (phase offset)
- MMCM phase shift resolution

These measurements do not include package or clock tree skew.

2. This parameter indicates the total sampling error of the Spartan 7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for Spartan 7 FPGA clock transmitter and receiver data-valid windows.

Table 49: Package Skew(1)

Symbol	Description	Device	Package	Value	Units
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Symbol	Description	Device	Package	Value	Units
T _{PKGSKEW}	Package skew.(2)	XC7S6	CPGA196	44	ps
			CSGA225	83	ps
			FTGB196	65	ps
		XC7S15	CPGA196	44	ps
			CSGA225	83	ps
			FTGB196	65	ps
		XC7S25	CSGA225	93	ps
			CSGA324	62	ps
			FTGB196	83	ps

Symbol	Description	Device	Package	Value	Units
		XC7S50	CSGA324	80	ps
			FGGA484	110	ps
			FTGB196	103	ps
		XC7S75	FGGA484	117	ps
			FGGA676	110	ps
		XC7S100	FGGA484	117	ps
			FGGA676	110	ps
		XA7S6	CPGA196	44	ps
			CSGA225	83	ps
		XA7S15	CPGA196	44	ps
			CSGA225	83	ps

Symbol	Description	Device	Package	Value	Units
		XA7S25	CSGA225	93	ps
			CSGA324	62	ps
		XA7S50	CSGA324	80	ps
			FGGA484	110	ps
		XA7S75	FGGA484	117	ps
			FGGA676	110	ps
		XC7S100	FGGA484	117	ps
			FGGA676	110	ps

Notes:

1. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

2. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.

XADC Specifications

The 7 Series FPGAs Overview (DS180) [Ref 1] and XA Spartan 7 Automotive FPGA Data Sheet: Overview (DS171) [Ref 2] list the devices that contain a 7 series XADC dual 12-Bit 1 MSPS analog-to-digital converter.

Table 50: XADC Specifications

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
$V_{CCADC} = 1.8V \pm 5\%$, $V_{REFP} = 1.25V$, $V_{REFN} = 0V$, $ADCCLK = 26\text{ MHz}$, $-55^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$. Typical values at $T_j = +40^{\circ}\text{C}$.						
ADC Accuracy(1)						
Resolution			12	–	–	Bits

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Integral nonlinearity(2)	INL	–40°C ≤ T _j ≤ 100°C	–	–	±2	LSBs
		–55°C ≤ T _j < –40°C; 100°C < T _j ≤ 125°C	–	–	±3	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic.	–	–	±1	LSBs

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Offset error	Unipolar	$-40^{\circ}\text{C} \leq T_j \leq 100^{\circ}\text{C}$	–	–	± 8	LSBs
		$-55^{\circ}\text{C} \leq T_j < -40^{\circ}\text{C}; 100^{\circ}\text{C} < T_j \leq 125^{\circ}\text{C}$	–	–	± 12	LSBs
	Bipolar	$-55^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$	–	–	± 4	LSBs
Gain error			–	–	± 0.5	%
Offset matching			–	–	4	LSBs
Gain matching			–	–	0.3	%
Sample rate			–	–	1	MS/s

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Signal to noise ratio(2)	SNR	$F_{\text{SAMPLE}} = 500$ KS/s, $F_{\text{IN}} = 20$ kHz	60	–	–	dB
RMS code noise		External 1.25V reference.	–	–	2	LSBs
		On-chip reference.	–	3	–	LSBs
Total harmonic distortion(2)	THD	$F_{\text{SAMPLE}} = 500$ KS/s, $F_{\text{IN}} = 20$ kHz	70	–	–	dB
Analog Inputs(3)						

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
ADC input ranges		Unipolar operation.	0	–	1	V
		Bipolar operation.	–0.5	–	+0.5	V
		Unipolar common mode range (FS input).	0	–	+0.5	V
		Bipolar common mode range (FS input).	+0.5	–	+0.6	V

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Maximum external channel input ranges		Adjacent analog channels set within these ranges should not corrupt measurements on adjacent channels.	-0.1	-	V_{CCADC}	V
Full-resolution bandwidth	FRBW	Auxiliary channel full resolution bandwidth.	250	-	-	kHz
On-chip Sensors						

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Temperature sensor error		-40°C ≤ T _j ≤ 100°C	-	-	±4	°C
		-55°C ≤ T _j < -40°C; 100°C < T _j ≤ 125°C	-	-	±6	°C
Supply sensor error		-40°C ≤ T _j ≤ 100°C	-	-	±1	%
		-55°C ≤ T _j < -40°C; 100°C < T _j ≤ 125°C	-	-	±2	%
Conversion Rate(4)						

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Conversion time: continuous	t_{CONV}	Number of ADCCLK cycles.	26	–	32	Cycles
Conversion time: event	t_{CONV}	Number of CLK cycles.	–	–	21	Cycles
DRP clock frequency	DCLK	DRP clock frequency.	8	–	250	MHz
ADC clock frequency	ADCCLK	Derived from DCLK.	1	–	26	MHz
DCLK duty cycle			40	–	60	%
XADC Reference(5)						

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
External reference	V_{REFP}	Externally supplied reference voltage.	1.20	1.25	1.30	V
On-chip reference		Ground V_{REFP} pin to AGND, $-40^{\circ}\text{C} \leq T_j \leq 100^{\circ}\text{C}$	1.2375	1.25	1.2625	V
		Ground V_{REFP} pin to AGND, $-55^{\circ}\text{C} \leq T_j < -40^{\circ}\text{C}$; $100^{\circ}\text{C} < T_j \leq 125^{\circ}\text{C}$	1.225	1.25	1.275	V

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
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Notes:

1. Offset and gain errors are removed by enabling the XADC automatic gain calibration feature. The values are specified for when this feature is enabled.

2. Only specified for bitstream option `XADCEnhancedLinearity = ON`.

3. For a detailed description, see the ADC chapter in the 7 Series FPGAs and Zynq 7000 SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide (UG480) [Ref 9].

4. For a detailed description, see the Timing chapter in the 7 Series FPGAs and Zynq 7000 SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide (UG480) [Ref 9].

5. Any variation in the reference voltage from the nominal $V_{REFP} = 1.25V$ and $V_{REFN} = 0V$ will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by $\pm 4\%$ is permitted.

Configuration Switching Characteristics

Table 51: Configuration Switching Characteristics

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V	0.95V		
		-2	-1	-1L	
Power-up Timing Characteristics					
T _{PL} (1)	Program latency.	5.00	5.00	5.00	ms, Max
T _{POR} (2)	Power-on reset (50 ms ramp rate time).	10/50	10/50	10/50	ms, Min/Max
	Power-on reset (1 ms ramp rate time).	10/35	10/35	10/35	ms, Min/Max
T _{PROGRAM}	Program pulse width.	250.00	250.00	250.00	ns, Min

CCLK Output (Master Mode)					
T_{ICCK}	Master CCLK output delay.	150.00	150.00	150.00	ns, Min
T_{MCCKL}	Master CCLK clock Low time duty cycle.	40/60	40/60	40/60	%, Min/Max
T_{MCCKH}	Master CCLK clock High time duty cycle.	40/60	40/60	40/60	%, Min/Max
F_{MCCK}	Master CCLK frequency.	100.00	100.00	100.00	MHz, Max
	Master CCLK frequency for AES encrypted x16.(2)	50.00	50.00	50.00	MHz, Max

Spartan 7 FPGAs Data Sheet: DC and AC Switching Characteristics (DS189)

$F_{\text{MCCK_START}}$	Master CCLK frequency at start of configuration.	3.00	3.00	3.00	MHz, Typ
F_{MCCKTOL}	Frequency tolerance, master mode with respect to nominal CCLK.	± 50	± 50	± 50	%, Max
CCLK Input (Slave Modes)					
T_{SCCKL}	Slave CCLK clock minimum Low time.	2.50	2.50	2.50	ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time.	2.50	2.50	2.50	ns, Min
F_{SCCK}	Slave CCLK frequency.	100.00	100.00	100.00	MHz, Max

EMCCLK Input (Master Mode)					
T_{EMCCKL}	External master CCLK Low time.	2.50	2.50	2.50	ns, Min
T_{EMCCKH}	External master CCLK High time.	2.50	2.50	2.50	ns, Min
F_{EMCCK}	External master CCLK frequency.	100.00	100.00	100.00	MHz, Max
Internal Configuration Access Port					
F_{ICAPCK}	Internal configuration access port (ICAPE2) clock frequency.	100.00	100.00	100.00	MHz, Max
Master/Slave Serial Mode Programming Switching					

$T_{DCCK}/$ T_{CCKD}	D_{IN} setup/hold .	4.00/0.00	4.00/0.00	4.00/0.00	ns, Min
T_{CCO}	D_{OUT} clock to out.	8.00	8.00	8.00	ns, Max
SelectMAP Mode Programming Switching					
$T_{SMDCCK}/$ T_{SMCCKD}	$D[31:00]$ setup/hold .	4.00/0.00	4.00/0.00	4.00/0.00	ns, Min
$T_{SMCSCCK}$ / $T_{SMCCKCS}$	CSI_B setup/hold .	4.00/0.00	4.00/0.00	4.00/0.00	ns, Min
$T_{SMWCCK}/$ T_{SMCCKW}	$RDWR_B$ setup/hold .	10.00/0.00	10.00/0.00	10.00/0.00	ns, Min
T_{SMCKCS} o	CSO_B clock to out (330 W pull-up resistor required).	7.00	7.00	7.00	ns, Max

T_{SMCO}	D[31:00] clock to out in readback.	8.00	8.00	8.00	ns, Max
F_{RBCK}	Readback frequency.	100.00	100.00	100.00	MHz, Max
Boundary-Scan Port Timing Specifications					
$T_{TAPTCK}/$ T_{TCKTAP}	TMS and TDI setup/hold .	3.00/2.00	3.00/2.00	3.00/2.00	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output.	7.00	7.00	7.00	ns, Max
F_{TCK}	TCK frequency.	66.00	66.00	66.00	MHz, Max
SPI Flash Master Mode Programming Switching					
$T_{SPIDCC}/$ T_{SPICCD}	D[03:00] setup/hold .	3.00/0.00	3.00/0.00	3.00/0.00	ns, Min

Spartan 7 FPGAs Data Sheet: DC and AC Switching Characteristics (DS189)

T_{SPICCM}	MOSI clock to out.	8.00	8.00	8.00	ns, Max
T_{SPICFC}	FCS_B clock to out.	8.00	8.00	8.00	ns, Max
STARTUPE2 Ports					
$T_{USRCCLK}$ O	STARTUP E2 USRCCLK O input to CCLK output.	0.50/6.70	0.50/7.50	0.50/7.50	ns, Min/Max
$F_{CFGMCLK}$	STARTUP E2 CFGMCLK output frequency.	65.00	65.00	65.00	MHz, Typ
$F_{CFGMCLK}$ TOL	STARTUP E2 CFGMCLK output frequency tolerance.	±50	±50	±50	%, Max

Device DNA Access Port

F_{DNACK}	DNA access port (DNA_PORT).	100.00	100.00	100.00	MHz, Max
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Notes:

1. To support longer delays in configuration, use the design solutions described in the 7 Series FPGA Configuration User Guide (UG470) [Ref 10].

2. See the 7 Series FPGAs Overview (DS180) [Ref 1] and XA Spartan 7 Automotive FPGA Data Sheet: Overview (DS171) [Ref 2] for a list of devices that support bitstream encryption.

eFUSE Programming Conditions

Table: eFUSE Programming Conditions(1) lists the programming conditions specifically for eFUSE. For more information, see the 7 Series FPGA Configuration User Guide (UG470) [Ref 10].

Table 52: eFUSE Programming Conditions(1)

Symbol	Description	Min	Typ	Max	Units
I_{FS}	V_{CCAUX} supply current	–	–	115	mA
T_{j}	Temperature range	15	–	125	°C

Symbol	Description	Min	Typ	Max	Units
Notes:					
1. The FPGA must not be configured during eFUSE programming.					

References

1. 7 Series FPGAs Overview ([DS180](#))
2. XA Spartan 7 Automotive FPGA Data Sheet: Overview ([DS171](#))
3. 7 Series FPGAs SelectIO Resources User Guide ([UG471](#))
4. 7 Series FPGA Packaging and Pinout Specification ([UG475](#))
5. 7 Series FPGAs PCB Design Guide ([UG483](#))
6. Xilinx Power Estimator spreadsheet tool ([XPE](#))
7. Zynq 7000 SoC and 7 Series Devices Memory Interface Solutions User Guide ([UG586](#))
8. [See the Clocking Wizard](#) in Vivado software.
9. 7 Series FPGAs and Zynq 7000 SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide ([UG480](#))
10. 7 Series FPGA Configuration User Guide ([UG470](#))

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
10/18/2024	1.11	In Table: Maximum Physical Interface (PHY) Rate for Memory Interface IP available with the Memory Interface Generator(1) , updated rate for DDR3L in -1Q (1.0V) to N/A.
10/31/2022	1.10	In Table: Maximum Physical Interface (PHY) Rate for Memory Interface IP available with the Memory Interface Generator(1) , split -1Q speed grade into its own column.
03/13/2019	1.9	Removed FTGB196 package from XA7S6, XA7S15, XA7S25, and XA7S50 devices in Table: Package Skew(1) .

Date	Version	Description of Revisions
09/28/2018	1.8	Removed description of -1Q speed grade only being available in XA Spartan-7 FPGAs from second paragraph of Introduction .
07/31/2018	1.7	In Table: Speed Specification Version By Device , updated Vivado tools version to 2018.2.1. In Table: Spartan 7 Device Speed Grade Designations , moved all speed grades for all devices to Production. In Table: Spartan 7 Device Production Software and Speed Specification Release , added Vivado tools version for XC7S6, XC7S15, XC7S75, XC7S100, XA7S6, XA7S15, XA7S75, and XA7S100.

Date	Version	Description of Revisions
06/18/2018	1.6	<p>In Table: Speed Specification Version By Device, updated Vivado tools version to 2018.2.</p> <p>In Table: Spartan 7 Device Speed Grade Designations, moved all speed grades except -1Q (1.0V) for XC7S6 and XC7S15 to Production. In Table: Spartan 7 Device Production Software and Speed Specification Release, added Vivado tools version for XC7S6 and XC7S15.</p>

Date	Version	Description of Revisions
04/04/2018	1.5	<p>Added XA7S6, XA7S15, XA7S25, XA7S75, and XA7S100 devices throughout. In Table: Typical Quiescent Supply Current(1)(2)(3), updated typical quiescent supply current values for XC7S25 and XC7S50 devices, and added values for XC7S6, XC7S15, XC7S75, and XC7S100 devices. In Table: Power-On Current, updated table title and $I_{CCINTMIN}$ and $I_{CCAUXMIN}$ for XC7S75 and XC7S100 devices. In Table: Spartan 7 Device Speed Grade Designations, moved all speed grades for XC7S6 and XC7S15 to Preliminary, moved -1LI (0.95V) speed grade for XC7S25 to Production, and moved all speed grades except -1Q (1.0V) for XC7S75 and XC7S100 from Preliminary to Production. In Table:</p>

Date	Version	Description of Revisions
		<p>Spartan 7 Device Production Software and Speed Specification Release, added Vivado tools version for XC7S25, XC7S75, and XC7S100. In Table: Duty Cycle Distortion and Clock-Tree Skew, Table: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)(1), Table: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)(1), Table: Clock-Capable Clock Input to Output Delay With MMCM(1), Table: Clock-Capable Clock Input to Output Delay With PLL(1), Table: Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks, Table: Clock-Capable Clock Input Setup and Hold With MMCM, and Table: Clock-Capable Clock Input Setup and Hold</p>

Date	Version	Description of Revisions
		<p>With PLL, changed parameter value for XA7S50 to N/A. In Table: Package Skew(1), added package skew values for XC7S6 and XC7S15 devices.</p>

Date	Version	Description of Revisions
12/22/2017	1.4	<p>In Table: Speed Specification Version By Device, updated Vivado tools version to 2017.4.</p> <p>In Table: Spartan 7 Device Speed Grade Designations, moved all speed grades for XC7S75 and XC7S100 from Advance to Preliminary and all speed grades except -1LI (0.95V) for XC7S25 from Advance to Production. In Table: Spartan 7 Device Production Software and Speed Specification Release, added Vivado tools version for XC7S25. Added Note 2 to Table: Maximum Physical Interface (PHY) Rate for Memory Interface IP available with the Memory Interface Generator(1).</p> <p>In Table: Package Skew(1), added package skew values for XC7S25 device in CSGA324 package and XC7S75 and XC7S100</p>

Date	Version	Description of Revisions
		devices in FGGA676 package.

Date	Version	Description of Revisions
11/20/2017	1.3	<p>Added XA7S50 device throughout. Updated description of offered temperature ranges in second paragraph of Introduction. Added row for junction temperature (T_j) at expanded (Q) temperature to Table: Recommended Operating Conditions(1)(2). Added -1Q (1.0V) speed grade to Table: Typical Quiescent Supply Current(1)(2)(3), and Table: Spartan 7 Device Speed Grade Designations to Table: Maximum Physical Interface (PHY) Rate for Memory Interface IP available with the Memory Interface Generator(1). In Table: Speed Specification Version By Device, updated Vivado tools version to 2017.3. In Table: Package Skew(1), added package skew values for XC7S25, XC7S50, XC7S75, and XC7S100</p>

Date	Version	Description of Revisions
		devices in CSGA225, FTGB196, and FGGA484 packages. Added XA Spartan 7 Automotive FPGA Data Sheet: Overview (DS171) to References .

Date	Version	Description of Revisions
06/20/2017	1.2	<p>Updated paragraph before Table: Power-On Current. In Table: Speed Specification Version By Device, updated Vivado tools version to 2017.2. In Table: Spartan 7 Device Speed Grade Designations, moved all speed grades for XC7S50 from Preliminary to Production and updated Note 1. In Table: Spartan 7 Device Production Software and Speed Specification Release, added Vivado tools version for XC7S50. In Table: Package Skew(1), added package skew value for XC7S50 device in FGGA484 package.</p>

Date	Version	Description of Revisions
04/07/2017	1.1	<p>Added 1.35V to Note 5 in Table: Recommended Operating Conditions(1) (2). In Table: Speed Specification Version By Device, updated Vivado tools version to 2016.4. In Table: Spartan 7 Device Speed Grade Designations, moved all speed grades for XC7S50 from Advance to Preliminary. Removed SFI-4.1 and SPI-4.2 from descriptions of SDR LVDS receiver and DDR LVDS receiver, respectively, in Table: Networking Applications Interface Performances. In Table: Input/Output Delay Switching Characteristics, changed $T_{IDELAYRESOLUTION}$ units from ps to μs. Removed BUFMR from Note 1 in Table: Regional Clock Buffer Switching Characteristics (BUFR). In Table: Package Skew(1), replaced</p>

Date	Version	Description of Revisions
		TQGA144 with FTGB196 for XC7S6, XC7S15, and XC7S25 devices, added FTGB196 package for XC7S50 device, and added package skew value for XC7S50 device in CSGA324 package.
09/27/2016	1.0	Initial Xilinx release.

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