IGLOO 2 FPGA Product Brief

Introduction (Ask a Question)

Microchip IGLOO® 2 FPGAs integrate the fourth-generation Flash-based FPGA fabric and high-performance communication interfaces on a single chip. The IGLOO 2 family is the industry's lowest power, most reliable and highest security programmable logic solution. This next generation IGLOO 2 architecture offers up to 3.6X gate count implemented with the 4-input Look-Up Table (LUT) fabric with carry chains, giving 2X performance and includes multiple embedded memory options and math blocks for Digital Signal Processing (DSP). High-speed serial interfaces include PCI Express (PCIe), 10 Gbps Attachment Unit Interface (XAUI)/XGMII Extended Sublayer (XGXS) plus native Serialization/Deserialization (SerDes) communication, while Double Data Rate 2 (DDR2)/DDR3 memory controllers provide high-speed memory interfaces.

Features (Ask a Question)

The following features are supported by the IGLOO 2 family devices.

- High-performance FPGA
  - Efficient 4-input LUTs with carry chains for high-performance and low power
  - Up to 236 blocks of dual-port 18 kb SRAM (Large SRAM) with 400 MHz synchronous performance (512 × 36, 512 × 32, 1 kb × 18, 1 kb × 16, 2 kb × 9, 2 kb × 8, 4 kb × 4, 8 kb × 2 or 16 kb × 1)
  - Up to 240 blocks of three-port 1 kb SRAM with 2 read ports and 1 write port (micro SRAM)
  - High-performance DSP

    Up to 240 fast math blocks with 18 × 18 signed multiplication, 17 × 17 unsigned multiplication and 44-bit accumulator
- High-speed Serial Interfaces

  Up to 16 SerDes lanes are available and each of them has the following characteristics:
  - XGMII Extended Sublayer (XGXS)/10 Gbps Attachment Unit Interface (XAUI) extension (to implement a 10 Gbps (10 Gigabit Media Independent Interface (XGMII)) Ethernet Embedded Physical Interface (PHY) interface)
  - Native EPCS SerDes interface facilitates implementation of serial rapid IO in fabric or an SGMII interface to a soft Ethernet MAC
  - PCIe endpoint controller
  - ×1, ×2 and ×4 lane PCI express core
  - Up to 2 kbps maximum payload size
  - 64/32-bit Advanced eXtensible Interface (AXI)/Advanced High-performance Bus (AHB) Host and Client interfaces to the application layer
- High-speed Memory Interfaces
  - Up to two high-speed DDRx memory controllers
    - High-Performance Memory Subsystem (HPMS) Double Data Rate (DDR) (DDR2/3 controller in HPMS (MDDR)) and fabric DDR (DDR2/3 Controller in FPGA Fabric (FDDR)) controllers
    - Supports LPDDR/DDR2/DDR3
    - Maximum 333 MHz clock rate

        - Single Error Correct Double Error Detect (SECDED) enable/disable feature
        - Supports various DRAM bus width modes, ×8, ×9, ×16, ×18, ×32 and ×36
        - Supports command reordering to optimize memory efficiency
        - Supports data reordering, returning critical word first for each command
    - SDRAM support through a soft SDRAM memory controller.
- High-performance Memory Subsystem
    - 64 KB embedded SRAM (eSRAM)
    - Up to 512 KB embedded Non Volatile Memory (eNVM)
    - One Serial Peripheral Interface (SPI)/Communication Block (COMM_BLK)
    - DDR bridge (2 port data R/W buffering bridge to DDR memory) with 64-bit AXI interface
    - Non-blocking, multilayer AHB bus matrix allowing multi-master scheme supporting 5 hosts and 7 clients
    - Two AHB/Advanced Peripheral Bus (APB) interfaces to FPGA fabric (host/client capable)
    - Two DMA controllers to offload data transactions
        - 8-channel Peripheral DMA (PDMA) for data transfer between HPMS peripherals and memory
    - High-Performance DMA (HPDMA) for data transfer between eSRAM and DDR memories
- Clocking Resources
    - Clock sources
        - High precision 32 kHz to 20 MHz main crystal oscillator
        - 1 MHz embedded RC oscillator
        - 50 MHz embedded RC oscillator
    - Up to eight Clock Conditioning Circuits (CCCs) with up to eight integrated analog Phase-Locked Loops (PLLs):
        - Output clock with eight output phases and 45° phase difference (multiply/divide and delay capabilities)
    - Frequency: Input 1 MHz to 200 MHz, output 20 MHz to 400 MHz
- Operating Voltage and I/Os
    - 1.2V core voltage
    - Mulch-standard user I/Os (MSIO/MSIOD)
        - LVTTL/LVCMOS 3.3V (MSIO only)
        - LVCMOS 1.2V, 1.5V, 1.8V and 2.5V
        - DDR (SSTL2_1and SSTL2_2)
        - LVDS, MLVDS, Mini-LVDS and RSDS differential standards
        - PCI
        - LVPECL (receiver only)
    - DDRI/Os (DDRIO)
        - DDR, DDR2, DDR3, LPDDR, SSTL2, SSTL18 and HSTL
        - LVCMOS 1.2V, 1.5V, 1.8V and 2.5V
    - Market leading number of user I/Os with 5G SerDes
- Security
    - Design security features (available on all devices)

      The following list provides the design security features:

        - Intellectual Property (IP) protection through unique security features and use models new to the PLD industry
        - Encrypted user key and bit stream loading, enabling programming in less-trusted locations
        - Supply-chain assurance device certificate
        - Enhanced anti-tamper features
        - Zeroization
    - Data security features (available on premium devices)

      The following list provides the data security features:
        - Non-deterministic random bit generator (NRBG)
        - User cryptographic services (Advanced Encryption Standard (AES)-256, Secure Hashing Algorithm (SHA)-256 and Elliptical Curve Cryptography (ECC) engine)
        - User Physically Unclonable Function (PUF) key enrollment and regeneration
        - CRI pass-through Differential Power Analysis (DPA) patent portfolio license
        - Hardware firewalls Protecting Microcontroller Subsystem (HPMS) memories
- Reliability
    - Single Event Upset (SEU)-Immune
        - Zero FIT FPGA configuration cells
    - Junction temperature
        - 125 °C—Military Temperature
        - 100 °C—Industrial Temperature
        - 85 °C—Commercial Temperature
    - SECDED protection on the following
        - Embedded memories (eSRAMs)
        - PCIe buffer
        - DDR memory controllers with optional SECDED modes
    - Buffers implemented with SEU resistant latches on the following
        - DDR bridges (HPMS, MDDR and FDDR)
        - SPIFIFO
        - NVM integrity check at power-up and on-demand
        - No external configuration memory required—instant-on, retains configuration when turned off
- Low Power
    - Low static and dynamic power
        - Flash*Freeze (F*F) mode for fabric
    - Power as low as 13 mW/Gbps per lane for SerDes devices
    - Up to 25% lower total power than competing devices

Table of Contents

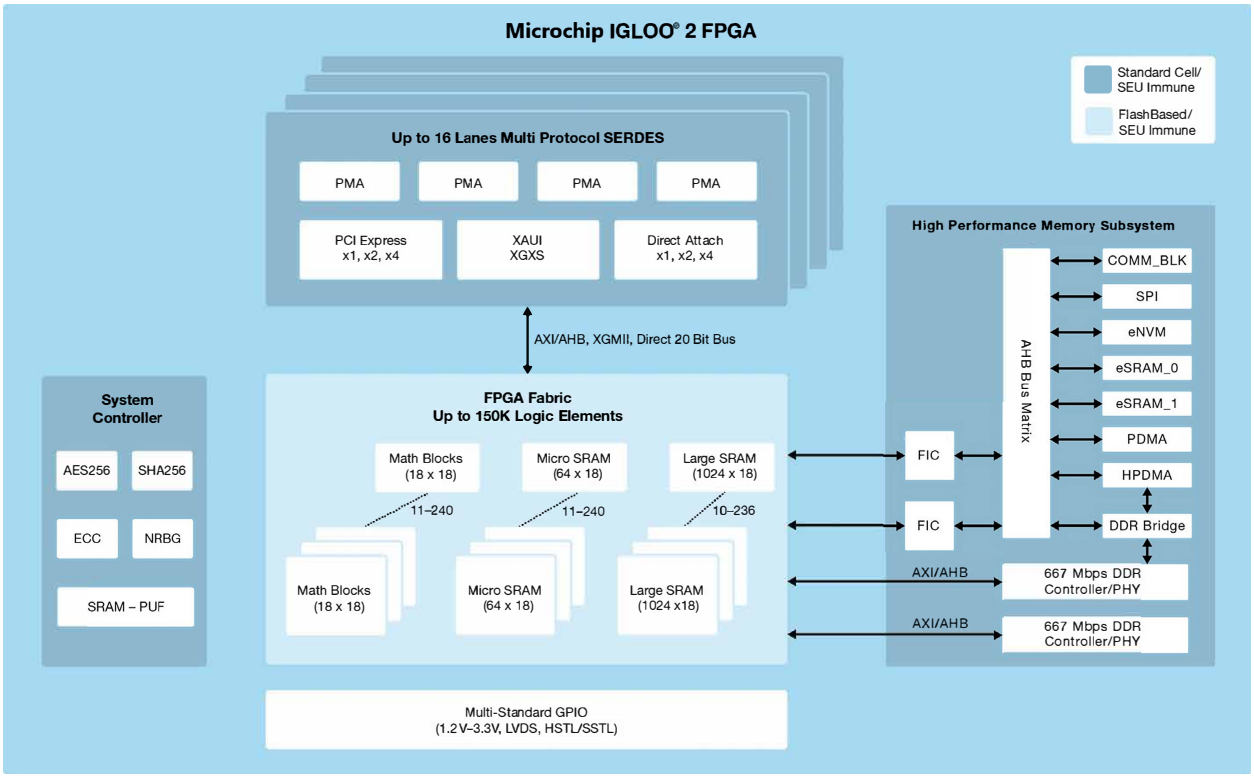
1. IGLOO 2 FPGAs Overview (Ask a Question)

The following sections describe the key features and block diagram of the IGLOO 2 FPGA.

1.1. Block Diagram (Ask a Question)

The following figure shows the various blocks available in IGLOO 2 FPGA.

Figure 1-1. IGLOO 2 FPGA Block Diagram



The following table lists the features supported by devices in the IGLOO 2 FPGA family.

Table 1-1. IGLOO® 2 FPGA Product Family

Peripherals	Features [1, 2]	M2GL005 (S)	M2GL010 (S/T/TS)	M2GL025 (T/TS)	M2GL050 (T/TS)	M2GL060 (T/TS)	M2GL090 (T/TS)	M2GL150 (T/TS)
Logic/DSP	Maximum Logic Elements (4LUT + DFF)[3]	6,060	12,084	27,696	56,340	56,520	86,184	146,124
	Math Blocks (18 × 18)	11	22	34	72	72	84	240
	PLLs and CCCs	2	2	6	6	6	6	8
	SPI/HPDMA/ PDMA	1 each	1 each	1 each	1 each	1 each	1 each	1 each
	Fabric Interface Controllers	1	1	1	2	1	1	2
	Data Security	AES256, SHA256 and RNG	AES256, SHA256 and RNG	AES256, SHA256 and RNG	AES256, SHA256 and RNG	AES256, SHA256, RNG, ECC and PUF	AES256, SHA256, RNG, ECC and PUF	AES256, SHA256, RNG, ECC and PUF
Memory	eNVM (KB)	128	256	256	256	256	512	512
	LSRAM18K Blocks	10	21	31	69	69	109	236
	µSRAM 1K Blocks	11	22	34	72	72	112	240
	eSRAM (KB)	64	64	64	64	64	64	64
	Total RAM (Kbit)	703	912	1104	1826	1826	2586	5000
High Speed	DDR Controllers	1 × 18	1 × 18	1 × 18	2 × 36	1 × 18	1 × 18	2 × 36
	SerDes Lanes (T)	0	4	4	8	4	4	16
	PCIe End Points	0	1	1	2	2	2	4
User I/Os	MSIO (3.3V)	119	123	157	139	279	309	292
	MSIOD (2.5V)	28	40	40	62	40	40	106
	DDRIO (2.5V)	66	70	70	176	76	76	176
	Total User I/O	209	233	267	377	395	425	574
Grades	Commercial(C), Industrial (I), Military (M) and Automotive (T1/T2)	C,I, T1 and T2	C,I, M, T1 and T2	C,I, M, T1 and T2	C,I, M,T1 and T2	C,I, M, T1 and T2	C,I, M, T1 andT2	C,I and M

Notes:

1. Feature availability is package dependent.
2. Data security features are only available in S and TS devices.
3. Total logic might vary based on utilization of DSP and memories in your design. See UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide for more information about DSP and memories.

1.2. I/Os Per Package (Ask a Question)

The following table provides the packaging options for IGLOO 2 devices.

Table 1-2. Packaging Options

Package Options[1]	Pitch (mm)	Length × Width (mm)
FCSG325[2]	0.5	11 × 11
VF(G)256[2,3]	0.8	14 × 14
FCSG536[2]	0.5	16 × 16
VF(G)400[2, 3]	0.8	17 × 17
FCV(G)484[2, 3]	0.8	19 × 19
TQ(G)144[2, 4]	0.5	20 × 20
FG(G)484[2, 5]	1.0	23 × 23
VFG784	0.8	23 × 23
FG(G)676[2, 3]	1.0	27 × 27
FG(G)896[2]	1.0	31 × 31
FC(G)1152[2]	1.0	35 × 35

Notes:

1. All the mentioned packages are available with lead and lead free. Package VFG784 is available only in lead-free.
2. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.
3. Automotive T2 grade devices are available in the VF(G)256, VF(G)400, FG(G)484 and FG(G)676 packages.
4. The TQ(G)144 package is available in T2 grade by the end of February 2017.
5. Automotive T1grade devices are available in the FG(G)484 package.

The following table provides the I/O details for IGLOO 2 devices.

Table 1-3. I/Os per Package

Devices		M2GL005 (S)	M2GL010 (T/TS)[1,2]	M2GL025 (T/TS)[1]	M2GL050 (T/TS)[1]	M2GL060 (T/TS)[1]	M2GL090 (T/TS)[1,3,4]	M2GL150 (T/TS)[5]
FCSG325	I/Os	—	—	**180**	**200**	**200**	180	—
	Lanes	—	—	**2**	**2**	**2**	4	—
VFG256	I/Os	161	**138**	**138**	—	—	—	—
	Lanes	—	**2**	**2**	—	—	—	—
FCSG536	I/Os	—	—	—	—	—	—	293
	Lanes	—	—	—	—	—	—	4
VFG400	I/Os	**171**	**195**	**207**	**207**	**207**	—	—
	Lanes	—	**4**	**4**	**4**	**4**	—	—
FCV(G)484	I/Os	—	—	—	—	—	—	248
	Lanes	—	—	—	—	—	—	4
TQ(G)144	I/Os	84	84	—	—	—	—	—
	Lanes	—	—	—	—	—	—	—
FG(G)484	I/Os	**209**	**233**	**267**	**267**	**267**	**267**	—
	Lanes	—	**4**	**4**	**4**	**4**	**4**	—
FG(G)676	I/Os	—	—	—	—	**387**	**425**	—
	Lanes	—	—	—	—	**4**	**4**	—
VFG784	I/Os	—	—	—	—	395	—	—
	Lanes	—	—	—	—	4	—	—

Table 1-3. I/Os per Package (continued)

Devices		M2GL005 (S)	M2GL010 (T/TS)[1,2]	M2GL025 (T/TS)[1]	M2GL050 (T/TS)[1]	M2GL060 (T/TS)[1]	M2GL090 (T/TS)[1,3,4]	M2GL150 (T/TS)[5]
FG(G)896	I/Os	—	—	—	377	—	—	—
	Lanes	—	—	—	8	—	—	—
FC(G)1152	I/Os	—	—	—	—	—	—	574
	Lanes	—	—	—	—	—	—	16

Notes:

1. Mil Temperature 010/025/050/060/090 devices are only available in the FG(G)484 package.
2. M2GL010(S) device is only available in TQ(G)144 package. M2GL010 (T/TS) devices are not available in TQ(G)144 package.
3. 090FCS(G)325 is 11x13.5 pkg dimension.
4. The M2GL090 (T/TS) device in the FCSG325 package is available with an ordering code of XZ48. The XZ48 ordering code pre-configures the device for Auto Update mode. Minimum Order quantities apply, contact your local Microchip sales office for details.
5. Mil Temperature 150 devices are only available in the FC(G)1152 package.
   - Highlighted cells indicate that the device packages have vertical migration capability.

The following table lists the features per device and its package combination.

Table 1-4. Features per Device/Package Combination

Package	Devices	MDDR	FDDR	Crystal Oscillators	5G SerDes Lanes[1]	PCIe Endpoints	MSIO (3.3V max.)[2]	MSIOD (2.5 max.)[3]	DDRIO (2.5V max.)	Total User I/Os
TQ(G)144[4]	M2GL005 (S)	—	—	1	—	—	52	9	23	84
	M2GL010 (S)	—	—	1	—	—	50	11	23	84
VFG256[4]	M2GL005 (S)	—	—	1	—	—	119	12	30	161
	M2GL010 (T/TS)	×18[5]	—	1	2	1	66	8	64	138
	M2GL025 (T/TS)	×18[5]	—	1	2	1	66	8	64	138
FCSG325[4]	M2GL025 (T/TS)	×18[5]	—	1	2	1	94	22	64	180
	M2GL050 (T/TS)	×18[5]	—	1	2	1	90	22	88	200
	M2GL060 (T/TS)	×18[5]	—	1	4	2	114	22	64	200
	M2GL090 (T/TS)	×18[5]	—	1	4	2	104	12	64	180
VFG400[4]	M2GL005(S)	×18[5]	—	1	—	—	79	28	64	171
	M2GL010 (T/TS)	×18[5]	—	1	4	1	99	32	64	195
	M2GL025 (T/TS)	×18[5]	—	1	4	1	111	32	64	207
	M2GL050 (T/TS)	×18[5]	—	1	4	1	87	32	88	207
	M2GL060 (T/TS)	×18[5]	—	1	4	2	111	32	64	207
FCV(G)484[4]	M2GL150 (T/TS)	×18[5]	×18[5]	1	4	4[7]	91	34	123	248
FG(G)484[4]	M2GL005 (S)	×18[5]	—	1	—	—	115	28	66	209
	M2GL010 (T/TS)	×18[5]	—	1	4	1	123	40	70	233
	M2GL025 (T/TS)	×18[5]	—	1	4	1	157	40	70	267
	M2GL050 (T/TS)	×18[6]	—	1	4	1	105	40	122	267
	M2GL060 (T/TS)	×18[5]	—	1	4	2	157	40	70	267
	M2GL090 (T/TS)	×18[5]	—	1	4	2	157	40	70	267
FC(G)536[4]	M2GL150 (T/TS)	×18[5]	×18[5]	1	4	4[7]	151	16	126	293
FG(G)676[4]	M2GL060 (T/TS)	×18[5]	—	1	4	2	271	40	76	387
	M2GL090 (T/TS)	×18[5]	—	1	4	2	309	40	76	425

Table 1-4. Features per Device/Package Combination (continued)

Package	Devices	MDDR	FDDR	Crystal Oscillators	5G SerDes Lanes[1]	PCIe Endpoints	MSIO (3.3V max.) [2]	MSIOD (2.5 max.)[3]	DDRIO (2.5V max.)	Total User I/Os
VFG784	M2GL060 (T/TS)	×18[5]	—	1	4	2	279	40	76	395
FG(G)896 [4,8]	M2GL050 (T/TS)	×36[9]	×36[9]	1	8	2	139	62	176	377
FC(G)1152[4]	M2GL150 (T/TS)	×36[10]	×36[10]	1	16	4	292	106	176	574

Notes:

1. Maximum SerDes rate for military temperature devices is 3.125 bps.
2. Number of differential MSIO is number of MSIOs/2 for even and number of MSIOs and 1/2 for odd.
3. Number of differential MSIOD is number of MSIODs/2 for even and number of MSIODs and 1/2 for odd.
4. All the packages mentioned above are available with lead and lead free. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.
5. DDR supports ×18, ×16, ×9 and ×8 modes
6. DDR supports ×18 and ×16 modes
7. 4 PCIe Gen1/Gen2 endpoints ×1 lane configuration.
8. DDR3 is non-compliant. Call technical support for details.
9. DDR supports ×36, ×32, ×18 and ×16 modes.
10. DDR supports ×36, ×32, ×18, ×16, ×9 and ×8 modes.
    - SerDes is not available in Automotive T1 grade.

The following table lists the programming interfaces that are available in IGLOO 2 FPGA.

Table 1-5. Programming Interfaces

Package	Devices	JTAG	SPI_0	Flash_GOLDEN_N	System Controller SPI Port
TQ(G)144[1]	M2GL005 (S)	Yes	Yes	No	No
	M2GL010 (S)	Yes	Yes	No	No
VFG256[1]	M2GL005 (S)	Yes	Yes	Yes	Yes
	M2GL010 (T/TS)	Yes	Yes	Yes	No
	M2GL025 (T/TS)	Yes	Yes	Yes	No
FCSG325[1]	M2GL025 (T/TS)	Yes	Yes	No	No
	M2GL050 (T/TS)	Yes	Yes	No	No
	M2GL060 (T/TS)	Yes	Yes	No	No
	M2GL090 (T/TS)	Yes	Yes	No	No
VFG400[1]	M2GL005 (S)	Yes	Yes	Yes	Yes
	M2GL010 (T/TS)	Yes	Yes	Yes	Yes
	M2GL025 (T/TS)	Yes	Yes	Yes	Yes
	M2GL050 (T/TS)	Yes	Yes	Yes	Yes
	M2GL060 (T/TS)	Yes	Yes	Yes	Yes
FCV(G)484[1]	M2GL150 (T/TS)	Yes	Yes	Yes	Yes
FG(G)484[1]	M2GL005 (S)	Yes	Yes	Yes	Yes
	M2GL010 (T/TS)	Yes	Yes	Yes	Yes
	M2GL025(T/TS)	Yes	Yes	Yes	Yes
	M2GL050 (T/TS)	Yes	Yes	Yes	Yes
	M2GL060 (T/TS)	Yes	Yes	Yes	Yes
	M2GL090(T/TS)	Yes	Yes	Yes	Yes
FCSG536[1]	M2GL150 (T/TS)	Yes	Yes	Yes	Yes
FG(G)676[1]	M2GL060(T/TS)	Yes	Yes	Yes	Yes
	M2GL090(T/TS)	Yes	Yes	Yes	Yes
VFG784	M2GL060 (T/TS)	Yes	Yes	Yes	Yes
FG(G)896[1]	M2GL050 (T/TS)	Yes	Yes	Yes	Yes
FC(G)1152[1]	M2GL150 (T/TS)	Yes	Yes	Yes	Yes

Note:

1. All the mentioned packages are available with lead and lead free. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.

The following table lists the chip resources needed for programming modes.

Table 1-6. Chip Resources Needed for Programming Modes

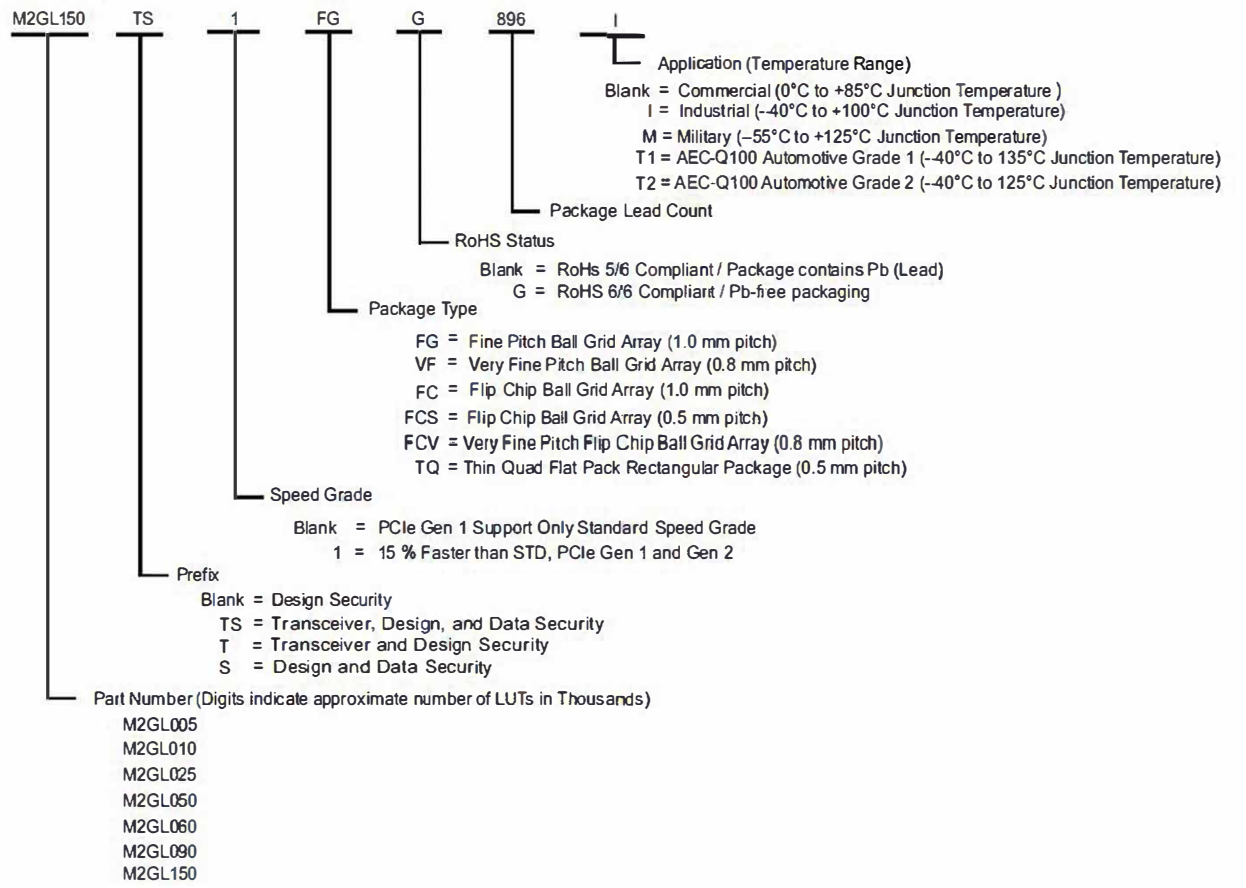
Programming Mode	JTAG	SPI_0	Flash_GOLDEN_N	System Controller SPI Port
External FlashPro4/5	Yes	No	No	No
External uP–TAG Client	Yes	No	No	No
External uP–SPI Client	No	No	No	Yes
Auto Programming	No	Yes	Yes	No
2-Step IAP	No	Yes	No	No
Programming Recovery	No	Yes	No	No

1.3. Ordering Information (Ask a Question)

The M2GL150 device is taken as an example and explains the various parts and their purposes.

The following figure shows the IGLOO 2 Ordering Information.

Figure 1-2. IGLOO 2 Ordering Information



Notes:

- M2GL005 devices are not available with transceivers or in the military temperature grade.
- Automotive grade devices are available with S/TS.

1.3.1. IGLOO 2 Commercial and Industrial Temperature Grade Devices (Ask a Question)

The following table lists the IGLOO 2 commercial and industrial temperature grade devices.

Table 1-7. IGLOO 2 Devices without Data Security (All Speed Grades, C and I Temperature)[1]

M2GL	FCS(G)325	VF(G)256	FCS(G)536	VF(G)400	FCV(G)484	TQ(G)144	FG(G)484	FG(G)676	VFG784	FG(G)896	FC(G)1152
005	—	—	—	—	—	—	—	—	—	—	—
010	—	T	—	T	—	—	T	—	—	—	—
025	T	T	—	T	—	—	T	—	—	—	—
050	T	—	—	T	—	—	T	—	—	T	—
060	T	—	—	T	—	—	T	T	T	—	—
090	T	—	—	—	—	—	T	T	—	—	—
150	—	—	T	—	T	—	—	—	—	—	T

Notes:

1. All the packages mentioned in the preceding table are available with lead and lead free. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.

- T indicates that the devices are available with Transceiver. For example, ordering code: M2GL025T-FCSG325.
- Highlighted cells indicate that the devices are available without Transceiver. For example, ordering code: M2GL025-FCSG325.

The following table lists IGLOO 2 data security devices.

Table 1-8. IGLOO 2 Data Security S Devices (All Speed Grades, C and I Temperature)[1]

M2GL	FCS(G)325	VF(G)256	FCS(G)536	VF(G)400	FCV(G)484	TQ(G)144	FG(G)484	FG(G)676	VFG784	FG(G)896	FC(G)1152
005	—	S	—	S	—	S	—	—	—	—	—
010	—	TS	—	TS	—	S	TS	—	—	—	—
025	TS	TS	—	TS	—	—	TS	—	—	—	—
050	TS	—	—	TS	—	—	TS	—	—	TS	—
060	TS	—	—	TS	—	—	TS	TS	TS	—	—
090	TS	—	—	—	—	—	TS	TS	—	—	—
150	—	—	TS	—	TS	—	—	—	—	—	TS

Notes:

1. All the packages mentioned in the preceding table are available with lead and lead free. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.

- S indicates that the devices are available with Data Security. For example, M2GL005S-VFG400
- TS indicates that the devices are available with Transceiver and Data Security. Example ordering code: M2GL025TS-FCSG325.

1.3.2. IGLOO 2 Military Temperature Grade Devices (Ask a Question)

The following list contains the IGLOO 2 military temperature devices:

- M2GL010 (T/TS)-1FG(G)484M
- M2GL025 (T/TS)-1FG(G)484M
- M2GL050 (T/TS)-1FG(G)484M
- M2GL060 (T/TS)-1FG(G)484M
- M2GL090 (T/TS)-1FG(G)484M

- M2GL150 (T/TS)-1FC(G)1152M
- M2GL150 (T/TS)-1FCV484M

Notes:

- Gold Wire bonds are available for the FG484 package by appending X399 to the part number when ordering. For example, M2GL090 (T/TS)-1FG484MX399.
- All the mentioned packages are available with lead and lead free. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.

1.4. IGLOO 2 Device Status (Ask a Question)

See the DS0128: IGLOO2 and SmartFusion2 Datasheet for device status.

1.5. IGLOO 2 Datasheet and Pin Descriptions (Ask a Question)

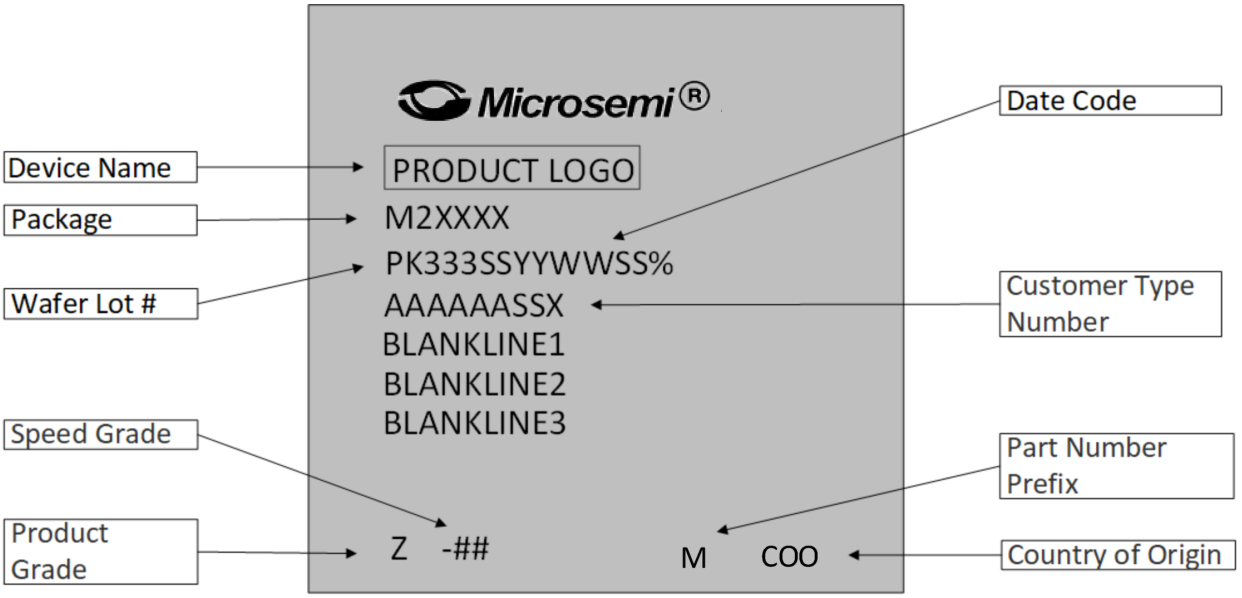
For datasheet and pin descriptions, see the following publications:

- DS0128: IGLOO2 and SmartFusion2 Datasheet
- DS0124: IGLOO2 Pin Descriptions Datasheet
- DS0138: IGLOO2 Automotive Grade 1 Datasheet
- DS0134: SmartFusion2 and IGLOO2 Automotive Grade 2 Datasheet
- PB0135: Automotive Grade 2 IGLOO2 FPGAs Product Brief

1.6. Marking Specification Details (Ask a Question)

Microchip normally topside marks the full ordering part number on each device. The following figure shows the details for each character code present on Microchip's IGLOO 2 FPGA devices.

Figure 1-3. Character Codes



1.6.1. Description (Ask a Question)

The following list provides the description of character codes:

- Device Name (M2XXXX)
  M2GL is used for IGLOO 2 Devices, for example: M2GL050TS
- Package (PK###): Available Package
  - PK: Package code[1]
    - FG(G): Fine Pitch BGA, 1.00 mm pitch
    - FC(G): Flip Chip Fine Pitch BGA with Metal LID on top, 1.00 mm pitch
    - FCV(G): Flip Chip Very Fine Pitch BGA with Metal LID on top, 0.8 mm pitch
    - FCS(G): Flip Chip Ultra Fine Pitch BGA with Metal LID on top, 0.5 mm pitch
    - VF(G): Very Fine Pitch BGA, 0.8 mm pitch
    - TQ(G): Ultra Fine Pitch Thin Quad Flat Pack Package, 0.5 mm pitch
  - ###: Number of Pins: Can be three or four digits. For example, 144, 256, or 1152.
- Wafer Lot (AAAAAASSX): Microchip wafer lot number
  - AAAAAA: Wafer lot number
  - SS: Two blank spaces
  - X: One digit die revision code
- Speed Grade (-###): Speed Binning Number
  - Blank: Standard speed grade
  - –1: –1 Speed grade
- Product grade (Z): Product Grade
  The following list provides the product grades:
  - Blank/C: Commercial
  - ES: Engineering Samples
  - I: Industrial
  - M: Military Temperature
  - PP: Pre-Production
  - T1: AEC-Q100 Automotive Grade 1
  - T2: AEC-Q100 Automotive Grade 2
- Date Code (YYWWSS%): Assembly Date Code
  - YY: Last two digits for seal year
  - WW: Work week the part was sealed
  - SS: Two blank spaces
  - %: Can be digital number or character for new product
- Customer Type Number: As specified on the lot traveler
  - GW: Gold Wire bond
- Part number Prefix: Part number prefix
  The following list describes different part number prefixes:
  - Blank: Design Security
  - T: Transceivers and Design Security
  - S: Design and Data Security
  - TS: Transceiver, Design, and Data Security

- Country of Origin (CCD): Assembly house country location
  - Country name: Country Code
  - China: CHN
  - Hong Kong: HKG
  - Japan: JPN
  - Korea,South: KOR
  - Philippines: PHL
  - Taiwan: TWN
  - Singapore: SGP
  - United States: USA
  - Malaysia: MYS

Note:

1. All the mentioned packages are available with lead and lead free. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.

2. IGLOO 2 Device Family Overview (Ask a Question)

Microchip's IGLOO 2 FPGAs integrate the fourth generation flash-based FPGA fabric and high-performance communication interfaces on a single chip. The IGLOO 2 family is the industry's lowest power, highest reliability, and most secured programmable logic solution. This next generation IGLOO 2 architecture offers up to 3.6X gate count, implemented with the 4-input LUT fabric with carry chains, giving 2X performance, and includes multiple embedded memory options and math blocks for DSP. High-speed serial interfaces enable PCIe, XAUI/XGXS plus native SerDes communication while DDR2/DDR3 memory controllers provide high-speed memory interfaces.

2.1. Reliability (Ask a Question)

IGLOO 2 Flash-based fabric has zero FIT configuration rate due to its SEU immunity, which is critical in reliability applications. The Flash fabric also has the advantage that no external configuration memory is required, making the device instant-on; it retains configuration when powered off. To complement this unique FPGA capability, IGLOO2 devices add reliability to many other aspects of the device. SECDED protection is implemented on the embedded SRAM (eSRAM), and is optional on the DDR memory controllers. This means that if a one-bit error is detected, it is corrected automatically. If more than one-bit errors are detected, they are not corrected. SECDED error signals are brought to the FPGA fabric to allow the user to monitor the status of these protected internal memories. Other areas of the architecture are implemented with latches, which are more resistant to SEUs. Therefore, no correction is needed in DDR bridges such as HPMS, MDDR, and FDDR, SPI, and PCIe FIFOs.

2.2. Highest Security Devices (Ask a Question)

Building further on the intrinsic security benefits of Flash nonvolatile memory technology, the IGLOO 2 family incorporates essentially all the legacy security features that made the original SmartFusion®, Fusion®, IGLOO®, and ProASIC® 3 third-generation Flash FPGAs the gold standard for secure devices in the PLD industry. In addition, the fourth-generation Flash-based SmartFusion 2 and IGLOO 2 FPGAs add many unique designs and data security features and use models new to the PLD industry.

2.2.1. Design Security vs. Data Security (Ask a Question)

When classifying security attributes of PLDs, a useful distinction is made between design security and data security.

2.2.2. Design Security (Ask a Question)

Design security helps protecting the intent of the owner of the design, such as keeping the design and associated bitstream keys confidential, preventing design changes (for example, insertion of Trojan Horses), and controlling the number of copies made throughout the device life cycle. Design security may also be known as IP protection. It is one aspect of anti-tamper (AT) protection. Design security applies to the device from initial production, includes any updates such as in-the-field upgrades, and can include decommissioning of the device at the end of its life, if desired. Good design security is a prerequisite for good data security.

The following table lists the main design security features supported in IGLOO 2.

Table 2-1. Design Security Features

Features (all devices)	M2GL005, M2GL010, M2GL025, and M2GL050	M2GL060, M2GL090, and M2GL150
FlashLock® passcode security (256-bit)	Available	Available
Flexible security settings using Flash lock-bits	Available	Available
Encrypted/authenticated design key loading	Available	Available
Symmetric key design security (256-bit)	Available	Available

Table 2-1. Design Security Features (continued)

Features (all devices)	M2GL005, M2GL010, M2GL025, and M2GL050	M2GL060, M2GL090, and M2GL150
Design key verification protocol	Available	Available
Encrypted/authenticated configuration loading	Available	Available
Certificate-of-Conformance (C-of-C)	Available	Available
Back-tracking prevention (also known as Versioning)	Available	Available
Device certificate(s) (anti-counterfeiting)	Available	Available
Support for configuration variations	Available	Available
Fabric NVM and eNVM integrity tests	Available	Available
Information services (S/N, Cert., USERCODE, and others)	Available	Available
Tamper detection	Available	Available
Tamper response (includes Zeroization)	Available	Available
ECC public key design security (384-bit)	—	Available
Hardware intrinsic design key (SRAM-PUF)	—	Available

2.2.3. Data Security (Ask a Question)

Data security protects the information that IGLOO 2 FPGA stores, processes, or communicates with the end application. If, for example, the configured design allows implementing the key management and encryption portion of a secure military radio, data security is entailed in encrypting and authenticating the radio traffic, and protecting the associated application-level cryptographic keys. Data security is closely related to the terms Information Assurance (IA) and information security. All IGLOO 2 devices incorporate enhanced design security, making them the most secure programmable logic devices ever made. Select IGLOO 2 models also include an advanced set of on-chip data security features that helps designing the most secure information assurance applications easier and better than ever before.

The following table lists the data security features of IGLOO 2.

Table 2-2. Data Security Features

Features (S Devices)	M2GL005S, M2GL010S, M2GL010TS, M2GL025TS, and M2GL050TS	M2GL060TS, M2GL090TS,and M2GL150TS
CRI pass-through DPA patent license	Available	Available
Hardware firewalls protecting access to memories	Available	Available
Non-deterministic random bit generator service	Available	Available
AES-128/256service (ECB, OFB, CTR, and CBC modes)	Available	Available
SHA-256service	Available	Available
HMAC-SHA-256service	Available	Available
Key tree service	Available	Available
PUF emulation (Pseudo-PUF)	Available	—
PUF emulation (SRAM-PUF)	—	Available
ECC point-multiplication service	—	Available
ECC point-addition service	—	Available
User SRAM-PUF enrollment service	—	Available
User SRAM-PUF activation code export service	—	Available
SRAM-PUF intrinsic key gen. and enrollment service	—	Available

Table 2-2. Data Security Features (continued)

Features (S Devices)	M2GL005S, M2GL010S, M2GL010TS, M2GL025TS, and M2GL050TS	M2GL060TS, M2GL090TS,and M2GL150TS
SRAM-PUF key import and enrollment service	—	Available
SRAM-PUF key regeneration service	—	Available

2.3. Low Power (Ask a Question)

Microchip's Flash-based FPGA fabric results in extremely low-power design implementation with static power as low as 7.5 mW (for 6,060 LE device). Flash*Freeze (F*F) technology provides an ultra-low power static mode, also known as Flash*Freeze mode, for IGLOO 2 devices, with power less than 11 mW for the largest device, which contains 146124 LEs. Flash*Freeze mode entry retains all SRAMs and register information, and the exit from Flash*Freeze mode achieves rapid recovery to active mode.

2.4. High-Performance FPGA Fabric (Ask a Question)

Built on 65 nm process technology, the IGLOO 2 FPGA fabric is composed of a logic module, a large SRAM (LSARM), an mSRAM, and a math block. The logic module is the basic logic element.

A logic module has the following advanced features:

- A fully permutable 4-input LUT optimized for lowest power
- A dedicated carry chain based on carry look-ahead technique
- A separate flip-flop which can be used independently from the LUT

The 4-input LUT is configured either to implement any 4-input combinatorial function or to implement an arithmetic function where the LUT output is XORed with carry input to generate the sum output.

2.4.1. Dual-Port Large SRAM (Ask a Question)

Large SRAM (LSRAM) (RAM1K×18) is targeted for storing large memory for use with various operations. Each LSRAM block can store up to 18,432 bits. Each RAM1K×18 block contains Port A and Port B. The LSRAM is synchronous for both read and write operations. Operations are triggered on the rising edge of the clock. The data output ports of the LSRAM have pipeline registers, which have control signals that are independent of the SRAM's control signals.

2.4.2. Three-Port Micro SRAM (Ask a Question)

µSRAM (RAM64×18) is the second type of SRAM, which is embedded in the IGLOO 2 FPGA fabric devices. The µSRAM block is approximately 1 KB (1152 bits). The µSRAM blocks are primarily targeted for building embedded FIFOs that can be used by any embedded fabric hosts. RAM64×18 µSRAM is a 3-port SRAM; Port A and Port B are used for read operations and Port C is used for write operations. The two read ports are independent of each other and can perform read operations in both synchronous and asynchronous modes. The write port is always synchronous.

2.4.3. Math Blocks for DSP Applications (Ask a Question)

The fundamental building block in any digital signal processing algorithm is the Multiply Accumulate (MACC) function. The IGLOO 2 device implements a custom 18 × 18 MACC block for efficient implementation of complex DSP algorithms such as Finite Impulse Response (FIR) filters, Infinite Impulse Response (IIR) filters, and Fast Fourier Transform (FFT) for filtering and image processing applications.

Each math block has the following capabilities:

- Supports18 × 18 signed multiplications natively (A[17:0] × B[17:0])
- Supports dot product; the multiplier computes:

  - $(A[8:0] \times B[17:9] + A[17:9] \times B[8:0]) \times 2^9$
- Built-in addition, subtraction, and accumulation units to combine multiplication results efficiently

In addition to the basic MACC function, DSP algorithms typically need small amounts of RAM for coefficients and larger RAMs for data storage. IGLOO 2 micro RAMs are ideally suited to serve the needs of coefficient storage while the large RAMs are used for data storage.

2.5. High-Performance Memory Subsystem (Ask a Question)

The High-Performance Memory Subsystem (HPMS) embeds two separate 32 KB SRAM blocks that have optional SECDED capabilities (32 KB with SECDED enabled, 40 KB with SECDED disabled), up to two separate 256 KB eNVM (Flash) blocks, and two separate DMA controllers for fast DMA user logic offloading. The HPMS provides multiple interfacing options to the FPGA fabric to facilitate tight integration between the HPMS and user logic in the fabric.

2.5.1. DDR Bridge (Ask a Question)

The DDR bridge is a data bridge between two AHB bus hosts and a single AXI bus client. The DDR bridge accumulates AHB writes into write combining buffers prior to bursting out to the external DDR memory. The DDR bridge also includes read combining buffers, allowing AHB hosts to efficiently read data from the external DDR memory from a local buffer. The DDR bridge optimizes reads and writes from multiple hosts to a single external DDR memory. Data coherency rules between the hosts and the external DDR memory are implemented in hardware. The DDR bridge contains two write combining buffers and two read buffers. All buffers within the DDR bridge are implemented with SEU tolerant latches and are not subject to SEUs that SRAM exhibits. IGLOO2 devices implement three DDR bridges in the HPMS, FDDR, and MDDR subsystems.

2.5.2. AHB Bus Matrix (Ask a Question)

The AHB bus matrix (ABM) is a non-blocking AHB-Lite multi-layer switch, supporting four Host interfaces and eight Client interfaces. The switch decodes access is attempted by hosts to various clients, according to the memory map and security configurations. When multiple hosts attempt to access a particular client simultaneously, an arbiter associated with that client decides which host gains access, according to a configurable set of arbitration rules. These rules can be configured by the user to provide different usage patterns to each client. For example, many consecutive access opportunities to the client can be allocated to one particular host, to increase the likelihood of the same type of accesses (all reads or all writes), which makes more efficient usage of the bandwidth to the client.

2.5.3. Fabric Interface Controller (Ask a Question)

The Fabric Interface Controller (FIC) block provides the HPMS Master (MM) and Fabric Master (FM) interfaces between the HPMS and the FPGA fabric. Each of these interfaces can be configured to operate as AHB-Lite or APB3. Depending on device density, there are up to two FIC blocks present in the HPMS (FIC_0 and FIC_1).

2.5.4. Embedded SRAM (Ask a Question)

The HPMS contains two blocks of 32 KB eSRAM, giving a total of 64 KB. Having the eSRAM arranged as two separate blocks allows the user to take advantage of the parallelism that exists in the HPMS.

The eSRAM is designed for SECDED protection. When SECDED is disabled, the SRAM used to store SECDED data may be reused as an extra 16 KB of eSRAM.

2.5.5. Embedded NVM (Ask a Question)

The HPMS contains up to 512 KB of eNVM, which is 64 bits wide.

2.5.6. DMA Engines (Ask a Question)

High-performance DMA and peripheral DMA engines are present in the HPMS.

2.5.7. APB Configuration Bus (Ask a Question)

On every IGLOO2 device memory, an APB configuration bus is present to allow the user to initialize the SerDes ASIC blocks, the fabric DDR memory controller, and user instantiated peripherals in the FPGA fabric

2.5.8. Peripherals (Ask a Question)

Alarge number of communications and general-purpose peripherals are implemented in the HPMS.

2.5.8.1. Communication Block (Ask a Question)

COMM_BLK provides an UART-like communications channel between the HPMS and the system controller. System services are initiated through the COMM_BLK. System services, such as Enter Flash*Freeze mode are initiated through the COMM_BLK.

2.5.8.2. Serial Peripheral Interface (Ask a Question)

The SPI controller is compliant with the Motorola SPI, Texas Instruments synchronous serial, and National Semiconductor MICROWIRE™ formats. In addition, the SPI supports interfacing to large SPI flash and EEPROM devices by way of the Client protocol engine. The SPI controller supports both Host and Client modes of operations.

The SPI controller embeds two 4 × 32 (depth × width) FIFOs for receive (RX) and transmit (TX). These FIFOs are accessible through RX data and TX data registers. Writing to the TX data register causes the data to be written to the transmit FIFO. This is emptied by the transmit logic. Similarly, reading from the RX data register causes data to be read from the receive FIFO.

2.6. Clock Sources: On-Chip Oscillators, PLLs, and CCCs (Ask a Question)

IGLOO 2 devices have two on-chip RC oscillators—a 1 MHz RC oscillator and a 50 MHz RC oscillator —and the main crystal oscillator (32 KHz–20 MHz). These are available to the user for generating clocks to the on-chip resources and the logic built on the FPGA fabric array. These oscillators can be used in conjunction with the integrated user PLLs and FAB_CCCs to generate clocks of varying frequency and phase. In addition to being available to the user, these oscillators are also used by the system controller, Power-on Reset circuitry, and HPMS during the Flash*Freeze mode.

IGLOO 2 devices have up to eight fabric CCC (FAB_CCC) blocks and a dedicated PLL associated with each CCC to provide flexible clocking to the FPGA fabric portion of the device. The user has the freedom to use any of the eight PLLs and CCCs to generate the fabric clocks and the internal HPMS clock from the base fabric clock (CLK_BASE). There is also a dedicated CCC block for the HPMS (HPMS_CCC) and an associated PLL (MPLL) for HPMS clocking and de-skewing the CLK_BASE clock. Fabric Alignment Clock Controller (FACC), part of the HPMS CCC, is responsible for generating various aligned clocks required by the HPMS for correct operation of the HPMS blocks and synchronous communication with the user logic in the FPGA fabric.

2.7. High-Speed Serial Interfaces (Ask a Question)

This section discusses about high-speed serial interfaces.

Up to 16 SerDes lanes are available and each of them has the following characteristics:

- XGMII Extended Sublayer (XGXS)/10 Gbps Attachment Unit Interface (XAUI) extension (to implement a 10 Gbps (10 Gigabit Media Independent Interface (XGMII)) Ethernet Embedded Physical Interface (PHY) interface)
- Native EPCS SerDes interface facilitates implementation of serial rapid IO in fabric or an SGMII interface to a soft Ethernet MAC
- PCIe endpoint controller
- ×1, ×2 and ×4 lane PCI express core
- Up to 2 kbps maximum payload size
- 64/32-bit Advanced eXtensible Interface (AXI)/Advanced High-performance Bus (AHB) Host and Client interfaces to the application layer

2.7.1. SerDes Interface (Ask a Question)

IGLOO 2 FPGA has up to four 5 Gbps SerDes transceivers, each supports the following features:

- Four SerDes/PCS lanes
- The native EPCS SerDes interface facilitates implementation of serial rapid IO (SRIO) in fabric or a SGMII interface for a soft Ethernet MAC. In EPCS modes, the maximum SerDes rate is 3.2 Gbps.

2.7.2. PCI Express (Ask a Question)

PCIe is a high speed, packet-based, point-to-point, low pin count, and serial inter connectbus. The IGLOO 2 family has two hard high-speed serial interface blocks. Each SerDes block contains a PCIe system block. The PCIe system is connected to the SerDes block. The following list provides the main supported features:

- Supports ×1, ×2, and ×4 lane configuration
- Endpoint configuration only
- PCI express base specification revision 2.0
- 2.5 Gbps and 5.0 Gbps compliant
- Embedded receive (2 KB), transmit (1 KB) and retry (1 KB) buffer dual-port RAM implementation
- Up to 2 KB maximum payload size
- 64-bitAXI or 32-bit/64-bit AHBL Host and Client interface to the application layer
- 32-bitAPB interface to access configuration and status registers of PCIe system
- Up to 3 x 64 bit base address registers
- 1 Virtual Channel (VC)

2.7.3. XAUI/XGXS Extension (Ask a Question)

The XAUI/XGXS extension allows the user to implement a 10 Gbps (XGMII) Ethernet PHY interface by connecting the XGMII fabric interface through an appropriate soft IP block in the fabric.

2.8. High-Speed Memory Interfaces: DDRx Memory Controllers (Ask a Question)

There are up to two DDR subsystems, MDDR (HPMS DDR), and FDDR (fabric DDR) present in IGLOO 2 devices. Each subsystem consists of a DDR controller, PHY, and a wrapper. The MDDR has an interface to/from the HPMS and fabric, and FDDR provides an interface to/from the fabric.

The following list contains the main features supported by the FDDR and MDDR:

- Supports LPDDR, DDR2, and DDR3 memories
- Simplified DDR command interface to standard AMBA AXI/AHB interface
- Up to 667 Mbps (333 MHz double data-rate) performance
- Supports 1, 2, or 4 ranks of memory
- Supports different DRAM bus width modes: ×8, ×9, ×16, ×18, ×32, and ×36
- Supports DRAM burst length of 2, 4, or 8 in full bus-width mode; supports DRAM burst length of 2, 4, 8, or 16 in Half bus-Width mode
- Supports memory densities up to 4 GB
- Supports a maximum of eight memory banks
- SECDED enable/disable feature
- PHY
- Read and write buffers in fully associative CAMs, configurable in powers of 2, up to 64 reads plus 64 writes
- Supports dynamically changing clock frequency while in self-refresh

- Supports command reordering to optimize memory efficiency
- Supports data reordering, returning critical word first for each command

2.8.1. MDDR Subsystem (Ask a Question)

The MDDR subsystem has two interfaces to the DDR: An AXI 64-bit bus from the DDR bridge within the HPMS and a multiplexed interface from the FPGA fabric, which can be configured as either a single AXI 64-bit bus or two 32-bit AHB-Lite buses. There is also a 16-bit APB configuration bus, which is used to initialize most of the internal registers within the MDDR subsystem after reset. This APB configuration bus is mastered by a host in the FPGA fabric. Support for 3.3V single data-rate DRAMs (SDRAM) can be obtained by instantiating a soft AHB or AXI SDRAM memory controller in the FPGA fabric and connecting I/O ports to 3.3V MSIO.

2.8.2. FDDR Subsystem (Ask a Question)

The FDDR subsystem has one interface to the DDR. This is a multiplexed interface from the FPGA fabric, which can be configured as either a single AXI 64-bit bus or two 32-bit AHB-Lite buses. There is also a 16-bit APB configuration bus, which is used to initialize the majority of the internal registers within the FDDR subsystem after reset. This APB configuration bus can be mastered by a host in the FPGA fabric.

2.9. IGLOO 2 Development Tools (Ask a Question)

2.9.1. Design Software (Ask a Question)

Microchip's Libero® SoC is a comprehensive software tool set to design applications using the IGLOO 2 device. Libero SoC manages the entire design flow from design entry, synthesis and simulation, place and route, timing, and power analysis, with the enhanced integration of the embedded design flow.

System designers can leverage the easy-to-use Libero SoC that includes the following features:

- System Builder for creation of system level architecture
- Synthesis,DSP, and debug support from Synopsys
- Simulation from Mentor Graphics
- Push-button design flow with power analysis and timing analysis
- Smart Debug for access to non-invasive probes within the IGLOO 2 devices See the LiberoSoC web page for more information.

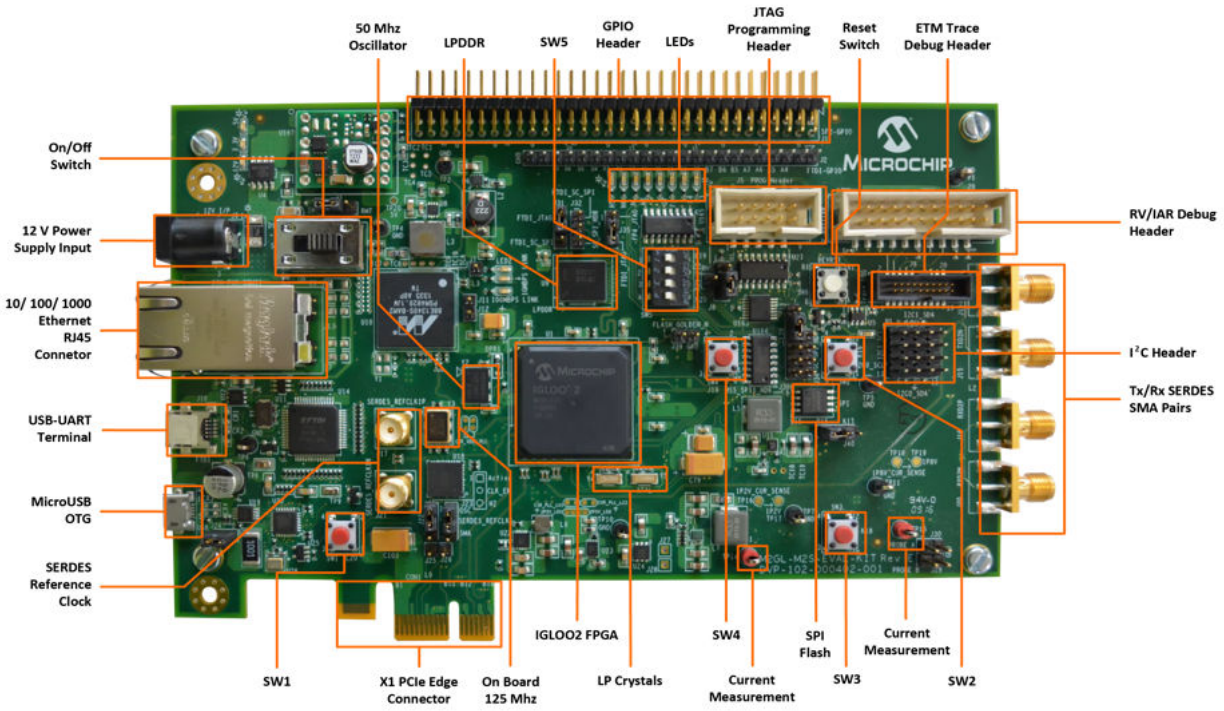
2.9.2. Design Hardware (Ask a Question)

Microchip's IGLOO2 evaluation kit (M2GL-EVAL-KIT) is a low-cost platform to evaluate various features offered by IGLOO2 devices.

The kit includes a M2GL010T-1FGG484 device. The board includes an RJ45 interface to 10/100/1000 Ethernet, 512 Mb of LPDDR, 64 Mb SPI Flash, USB-UART connections as well as I^2C, SPI, and GPIO headers. The kit includes a 12V power supply but can also be powered through the PCIe edge connector. The kit also includes a FlashPro4 JTAG programmer for programming and debugging.

The following figure shows the board image of the IGLOO2 evaluation kit.

Figure 2-1. IGLOO2 Evaluation Kit



2.9.3. IP Cores (Ask a Question)

Microchip offers many soft peripherals that can be placed in the FPGA fabric of the device. These include Core429, Core1553, CoreJESD204BRX/TX, CoreFRI, CoreFFT, and many other DirectCores. See the IPCores web page for more information.

3. Revision History (Ask a Question)

Revision	Date	Description
C	July 2025	Following is the summary of changes made in this revision: • Updated Figure 1-2 by replacing M2GL050 with M2GL150. • Updated Marking Specification Details by replacing Microchip logo with Microsemi logo.
B	03/2024	Following is the summary of changes made in this revision: • Updated Microsemi links with Microchip links • Updated the units of Total RAM (from KB to Kbit) in Table 1-1
A	06/2022	Following is the summary of changes made in this revision: • Document is updated as per Microchip publishing format • Replaced 51700121 with DS50003316A • As per Microchip terminology updates, replaced Slave with Client and Master with Host throughout the document • Updated User I/Os values (M2GL060 (T/TS): MSIO (3.3V and Total User I/O) in Table 1-1 • Added VFG784 package option details to Table 1-2 • Added VFG784 device details to Table 1-3. • Added VFG784 package details to Table 1-4 • Added VFG784 package details to Table 1-5 • Added VFG784 values to Table 1-7 • Added VFG784 values to Table 1-8 • Updated Figure 2-1
15.0	—	Information about M2GL150 FCV484M was added. See IGLOO2 Military Temperature Grade Devices.
14.0	—	Name change from native SerDes interface to native EPCS SerDes interface in the High-Speed Serial Interfaces in revision 14.0.
13.0	—	The following is a summary of changes made in revision 13.0: Updated Table 1 and Table 2 for grade 1 and 2 entries (SAR 80231). Updated the IGLOO2 Ordering Information image for grade 1 and 2 entries (SAR 80231). Added the grade 1 and grade 2 references in IGLOO2 Datasheet and Pin Descriptions (SAR 80231). Added grade 1 and 2 entries in Description, page 14 (SAR 80231).
12.0	—	The following is a summary of changes made in revision 12.0: Footnotes were inserted in Table 4 as required. (SAR 66079, SAR 77444, and SAR 73335)
11.0	—	The following is a summary of changes made in revision 11.0: Updated Table 1 (SAR 71995). Updated Marking Specification Details (SAR 71995). Updated Low Power (SAR 71995).
10.0	—	The following is a summary of changes made in revision 9.0: Updated Table 4 (SAR 69876). Added Table 6, Table 7, and Table 8 (SAR 69876). Updated Marking Specification Details (SAR 69876).

Revision History (continued)

Revision	Date	Description
9.0	—	The following is a summary of changes made in revision 9.0: Updated Table 1, Table 3, Table 4, Table 5, and Table 9. Removed all instances of and references to M2GL100. VQ144 is replaced with TQ144 (SAR 62858). Updated Table 9, page 16 and Table 10. Updated IGLOO2 Ordering Information. Added IGLOO2 Development Tools.
8.0	—	Updated Device Packages 005-VF256 and 150-FCS536 in Table 4–Table 5 in revision 8.0.
7.0	—	Table 2, Table 4, and Table 5, were updated in revision 7.0.
6.0	—	The following is a summary of changes made in revision 6.0: Table 1 to Table 5 and IGLOO2 Ordering Information were update with Military device data. The Marking Specification Details, page 13 and the Programming Interfaces, page 9 were added.
5.0	—	The following is a summary of changes made in revision 5.0: Tables 3-6 were combined into Table 5. Fabric Interface Controller features were added to IGLOO2 FPGA Product Family. Packages VQ144 and FCV484 were added to Table 3, page 7 and Table 5.
4.0	—	The following is a summary of changes made in revision 4.0: The Data Security Features section, table and the Device Status table were removed. Figure 1 was updated.
3.0	—	The following is a summary of changes made in revision 3.0: • Packages FCS325 and VF256 were added to I/Os Per Package. • IGLOO2 Ordering Information was updated.
2.0	—	The following was a summary of changes that were made in revision 2.0: • LSRAM x32/36 widths added. Table 1, page 6 table note added referring to updates in Table 5– Table 7. • IGLOO2 Ordering Information was updated. Part Numbers (tables 7 and 8) were removed. • IGLOO2 Device Status was updated. • M2GL090-FG676 and M2GL005-VF400 package pinouts finalized.
1.0	—	This was the initial release of this document.

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