Data Sheet

ADM3056E

5.7 kV rms, Signal Isolated CAN FD Transceiver

FEATURES

- 5.7 kV rms (8000 V peak) signal isolated CAN transceiver
- 1.7 V to 5.5 V supply range for V_{DD1}
- 4.5 V to 5.5 V supply range for V_{DD2}
- ISO 11898-2:2016 compliant CAN FD
- Data rates up to 12 Mbps for CAN FD
- Low loop propagation delay of 150 ns maximum
- Extended common-mode range of ±25 V
- Bus fault protection (CANH, CANL) of ±40 V
- Low power standby supporting remote wake request
- Extra isolated signal for control (for example, termination switches)
- Slope control for reduced EMI
- Safety and regulatory approvals
  - DIN EN IEC 60747-17 (VDE 0884-17)
    - V_{IORM} = 849 V peak
  - UL 1577
    - V_{ISO} = 5700 V rms for 1 minute
  - IEC/EN/CSA 62368-1
  - IEC/CSA 60601-1
  - IEC/CSA 61010-1
  - CQC GB4943.1
- 8.3 mm creepage/clearance with 16-lead SOIC package
- High common-mode transient immunity: ≥75 kV/µs
- Industrial temperature range: −40°C to +125°C

APPLICATIONS

- CANOpen, DeviceNet, and other CAN bus implementations
- Solar inverters and battery management
- Motor and process control
- Industrial automation
- Transport and infrastructure

FUNCTIONAL BLOCK DIAGRAM

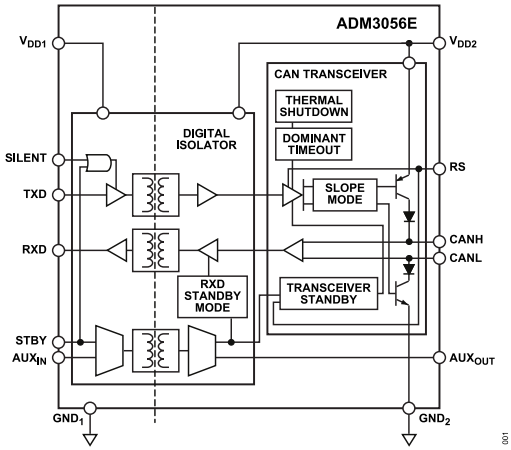

Figure 1.

GENERAL DESCRIPTION

The ADM3056E is a 5.7 kV rms isolated controller area network (CAN) physical layer transceiver. The ADM3056E fully meets the CAN flexible data rate (CAN FD) CAN FD ISO 11898-2:2016 requirements and is further capable of supporting data rates as high as 12 Mbps.

The device employs Analog Devices, Inc., *i*Coupler® technology to combine a highly robust 3-channel isolator and a CAN transceiver into a single SOIC, surface-mount package. The ADM3056E provides galvanic isolation between the CAN controller and physical layer bus.

Safety and regulatory approvals for 5.7 kV rms isolation voltage, 849 V peak working insulation voltage, 12.8 kV surge, and 8.3 mm creepage and clearance, ensure that the ADM3056E meets isolation requirements for high voltage applications.

Low propagation delays through the isolation support longer bus cables. Slope control mode is available for the standard CAN at low data rates. Standby mode can minimize power consumption when the bus is idle, or if the node goes offline. Silent mode allows the TXD input to be ignored for listen only functionality.

Dominant timeout functionality protects against bus lock up in a fault condition, and current limiting and thermal shutdown features protect against output short circuits. The device is fully specified over the −40°C to +125°C industrial temperature range and is available in a 16-lead, increased creepage, wide-body SOIC package.

Rev. B

DOCUMENT FEEDBACK
TECHNICAL SUPPORT

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REVISION HISTORY

9/2025—Rev. A to Rev. B

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12/2018—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

All voltages are relative to their respective ground. 1.7 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, −40°C ≤ ambient temperature (T_A) ≤ +125°C, and STBY is low, unless otherwise noted. Typical specifications are at V_{DD1} = V_{DD2} = 5 V and T_A = 25°C, unless otherwise noted.

Table 1. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT						
Bus Side	I_{DD2}					
Standby Mode				3.5	mA	STBY high, AUX_{IN} low, load resistance (R_L) = 60 Ω
Recessive State (or Silent)			9	10	mA	TXD and/or SILENT high, R_L = 60 Ω
Dominant State			63	75	mA	Fault condition, see the Theory of Operation section, R_L = 60 Ω
70% Dominant/30% Recessive						Worst case, see the Theory of Operation section, R_L = 60 Ω
1 Mbps			50	58	mA	
5 Mbps			53	60	mA	
12 Mbps			58	65	mA	
Logic Side *i*Coupler Current	I_{DD1}					
Normal Mode				5	mA	TXD high, low, or switching; AUX_{IN} low
Standby Mode			1.6	2	mA	STBY high
DRIVER						
Differential Outputs						See Figure 21
Recessive State, Normal Mode						TXD high, termination resistor (R_L) and common-mode filter capacitor (C_F) open
CANH, CANL Voltage	V_{CANL}, V_{CANH}	2.0		3.0	V	
Differential Output Voltage	V_{OD}	−500		+50	mV	
Dominant State, Normal Mode						TXD and SILENT low, C_F open
CANH Voltage	V_{CANH}	2.75		4.5	V	50 Ω ≤ R_L ≤ 65 Ω
CANL Voltage	V_{CANL}	0.5		2.0	V	50 Ω ≤ R_L ≤ 65 Ω
Differential Output Voltage	V_{OD}	1.5		3.0	V	50 Ω ≤ R_L ≤ 65 Ω
		1.4		3.3	V	45 Ω ≤ R_L ≤ 70 Ω
		1.5		5.0	V	R_L = 2240 Ω
Standby Mode						STBY high, R_L and C_F open
CANH, CANL Voltage	V_{CANL}, V_{CANH}	−0.1		+0.1	V	
Differential Output Voltage	V_{OD}	−200		+200	mV	
Output Symmetry (V_{DD2} − V_{CANH} − V_{CANL})	V_{SYM}	−0.55		+0.55	V	R_L = 60 Ω, C_F = 4.7 nF, RS low
Short-Circuit Current	$\|I_{SC}\|$					R_L open
Absolute						
CANH				115	mA	V_{CANH} = −3 V
CANL				115	mA	V_{CANL} = 18 V
Steady State						
CANH				115	mA	V_{CANH} = −24 V
CANL				115	mA	V_{CANL} = 24 V
Logic Inputs (TXD, SILENT, STBY, AUX_{IN})						
Input Voltage						
High	V_{IH}	0.65 × V_{DD1}			V	
Low	V_{IL}			0.35 × V_{DD1}	V	
Capacitance	C_{IN}		4.0		pF	Logic input pin to GND_1
Complementary Metal-Oxide Semiconductor (CMOS) Logic Input Currents	$\|I_{IH}\|$, $\|I_{IL}\|$			10	µA	Input high or low

SPECIFICATIONS

Table 1. Electrical Characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
RECEIVER						
Differential Inputs						
Differential Input Voltage Range	V_{ID}					See Figure 22, RXD capacitance (C_{RXD}) open, −25 V < V_{CANL}, and V_{CANH} < +25 V
Recessive		−1.0		+0.5	V	
		−1.0		+0.4	V	STBY high
Dominant		0.9		5.0	V	
		1.15		5.0	V	STBY high
Input Voltage Hysteresis	V_{HYS}		150		mV	
Unpowered Input Leakage Current	$\|I_{IN\ (OFF)}\|$			10	µA	V_{CANH}, V_{CANL} = 5 V, V_{DD2} = 0 V
CANH, CANL Input Resistance	R_{INH}, R_{INL}	6		25	kΩ	
Differential Input Resistance	R_{DIFF}	20		100	kΩ	
Input Resistance Matching	m_R	−0.03		+0.03		$m_R = 2 \times (R_{INH} - R_{INL})/(R_{INH} + R_{INL})$
CANH, CANL Input Capacitance	C_{INH}, C_{INL}		35		pF	
Differential Input Capacitance	C_{DIFF}		12		pF	
Logic Outputs (RXD, AUX_{OUT})						
Output Voltage						
Logic Low	V_{OL}		0.2	0.4	V	Output current (I_{OUT}) = 2 mA
Logic High	V_{OH}					I_{OUT} = −2 mA
RXD		V_{DD1} − 0.2			V	
AUX_{OUT}		2.4			V	
Short-Circuit Current	I_{OS}					Output voltage (V_{OUT}) = GND_1 or V_{DD1}
RXD		7		85	mA	
COMMON-MODE TRANSIENT IMMUNITY[1]						Common-mode voltage (V_{CM}) ≥ 1 kV, transient magnitude ≥ 800 V
Input High, Recessive	$\|CM_H\|$	75	100		kV/µs	AUX_{IN} high, TXD high, or CANH, CANL recessive
Input Low, Dominant	$\|CM_L\|$	75	100		kV/µs	AUX_{IN} low, TXD low, or CANH, CANL dominant
SLOPE CONTROL						
Input Voltage for Standby Mode	V_{STB}	4.0			V	
Current for Slope Control Mode	I_{SLOPE}			−240	µA	RS voltage (V_{RS}) = 0 V
Slope Control Mode Voltage	V_{SLOPE}	2.1			V	RS current (I_{RS}) = 10 µA
Input Voltage for High Speed Mode	V_{HS}			1	V	

[1] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining AUX_{OUT} ≥ 2.4 V, CANH, CANL recessive, or RXD ≥ V_{DD1} − 0.2 V. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining AUX_{OUT} ≤ 0.4 V, CANH, CANL dominant, or RXD ≤ 0.4 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

SPECIFICATIONS

TIMING SPECIFICATIONS

All voltages are relative to their respective ground. 1.7 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, −40°C ≤ T_A ≤ +125°C, and STBY low, unless otherwise noted. Typical specifications are at V_{DD1} = V_{DD2} = 5 V and T_A = 25°C, unless otherwise noted.

Table 2. Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DRIVER						SILENT low, see Figure 2 TXD pin bit time (t_{BIT_TXD}) = 200 ns, see Figure 23 RS pin pull-down resistance (R_{SLOPE}) = 0 Ω R_L = 60 Ω, C_L = 100 pF
Maximum Data Rate		12			Mbps	
Propagation Delay from TXD to Bus (Recessive to Dominant)	t_{TXD_DOM}		35	60	ns	
Propagation Delay from TXD to Bus (Dominant to Recessive)	t_{TXD_REC}		46	70	ns	
Transmit Dominant Timeout	t_{DT}	1175			µs	TXD low, see Figure 5
RECEIVER						SILENT low, see Figure 2 and Figure 23 R_L = 60 Ω, C_L = 100 pF C_{RXD} = 15 pF
Falling Edge Loop Propagation Delay (TXD to RXD)	t_{LOOP_FALL}					
Full Speed Mode				150	ns	R_{SLOPE} = 0 Ω, t_{BIT_TXD} = 200 ns
Slope Control Mode				300	ns	R_{SLOPE} = 47 kΩ, t_{BIT_TXD} = 1 µs
Rising Edge Loop Propagation Delay (TXD to RXD)	t_{LOOP_RISE}					
Full Speed Mode				150	ns	R_{SLOPE} = 0 Ω, t_{BIT_TXD} = 200 ns
Slope Control Mode				300	ns	R_{SLOPE} = 47 kΩ, t_{BIT_TXD} = 1 µs
Loop Delay Symmetry (Minimum Recessive Bit Width)	t_{BIT_RXD}					
2 Mbps		450		550	ns	t_{BIT_TXD} = 500 ns
5 Mbps		160		220	ns	t_{BIT_TXD} = 200 ns
8 Mbps		85		140	ns	t_{BIT_TXD} = 125 ns
12 Mbps		50		91.6	ns	t_{BIT_TXD} = 83.3 ns
CANH, CANL SLEW RATE	|SR|		7		V/µs	R_{SLOPE} = 47 kΩ
STANDBY						
Minimum Pulse Width Detected (Receiver Filter Time)	t_{FILTER}	1		5	µs	STBY high, see Figure 4
Wake-Up Pattern Detection Reset Time	t_{WUPR}	1175		4000	µs	STBY high, see Figure 4
Normal Mode to Standby Mode Time	t_{STBY_ON}			25	µs	Not shown in timing figures
Standby Mode to Normal Mode Time	t_{STBY_OFF}			25	µs	Time until RXD valid, not shown in timing figures
AUXILIARY SIGNAL						
Maximum Switching Rate	f_{AUX}	20			kHz	
AUX_{IN} to AUX_{OUT} Propagation Delay	t_{AUX}			25	µs	Not shown in timing figures
SILENT MODE						
Normal Mode to Silent Mode Time	t_{SILENT_ON}		40	100	ns	TXD low, R_{SLOPE} = 0 Ω, see Figure 3
Silent Mode to Normal Mode Time	t_{SILENT_OFF}		50	100	ns	TXD low, R_{SLOPE} = 0 Ω, see Figure 3

SPECIFICATIONS

Timing Diagrams

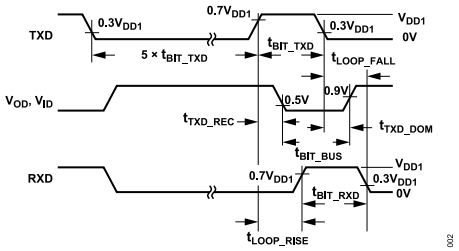


Figure 2. Driver/Receiver Timing Diagram

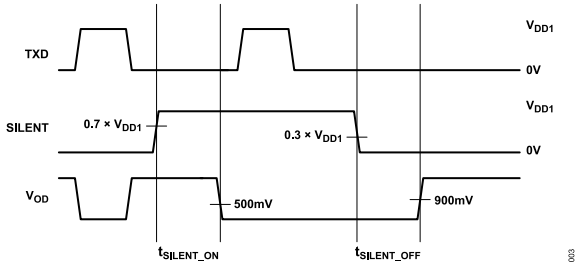


Figure 3. Silent Mode Timing Diagram

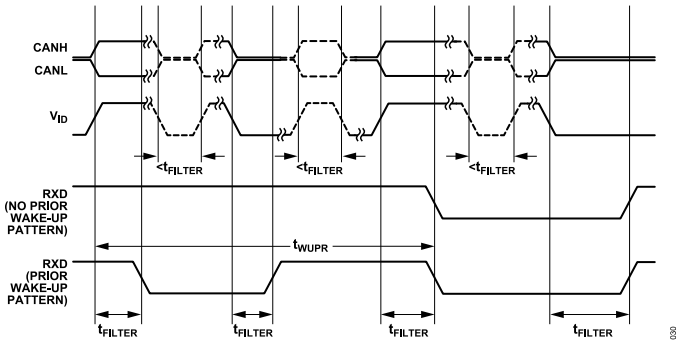


Figure 4. Wake-Up Pattern Detection and Filtered RXD in Standby Timing Diagram

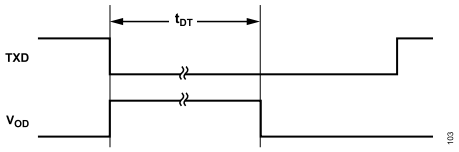


Figure 5. Dominant Timeout

SPECIFICATIONS

INSULATION SPECIFICATIONS

The ADM3056E is suitable for "safe electrical insulation" only within the safety limiting ratings. Compliance with the safety limiting ratings shall be ensured by means of suitable protective circuits.

Table 3. ADM3056E 16-Lead Increased Creepage SOIC [SOIC_IC] (RI-16-2) Insulation Characteristics

Parameter	Symbol	Value	Unit	Test Conditions/Comments
GENERAL				
Minimum External Clearance Distance	CLR	8.3	mm	Measured from input terminals to output terminals, shortest distance through air per IEC 60664-1
Minimum External Creepage Distance	CRP	8.3	mm	Measured from input terminals to output terminals, shortest distance along body per IEC 60664-1
Distance Through Insulation	DTI	29	µm	Minimum internal
Comparative Tracking Index	CTI	>600	V	Per IEC 60112
Material Group		I		Per IEC 60664-1
Overvoltage Category per IEC 60664-1		I to IV		Rated mains voltage ≤ 150V rms
		I to IV		Rated mains voltage ≤ 300V rms
		I to IV		Rated mains voltage ≤ 600V rms
SAFETY LIMITING VALUES				
Maximum Ambient Safety Temperature	T_S	150	°C	
Maximum Total Power Dissipation	P_{TOT}	1.73	W	T_A ≤ 25°C , $P_{TOT} = P_{SI} = P_{SO}$
Derating Above Ambient (T_A)		13.84	mW/°C	T_A > 25°C, see Figure 6
Junction-to-Air Thermal Impedance	θ_{JA}	72	°C/W	See the Thermal Characteristics section
IEC 60747-17 (REINFORCED INSULATION)				
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	849	V peak	
Maximum Isolation Working Voltage	V_{IOWM}	600	V rms	AC voltage, end of life test, f = 60 Hz
		849	V peak	DC voltage
Maximum Transient Isolation Voltage	V_{IOTM}	8000	V peak	$V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production)
Maximum Impulse Voltage	V_{IMP}	8000	V peak	Surge voltage in air, waveform per IEC 61000-4-5
Maximum Surge Isolation Voltage	V_{IOSM}	12800	V peak	$V_{TEST} \geq 1.3 \times V_{IMP}$ minimum 10 kV (type test), tested in oil, waveform per IEC 61000-4-5
Apparent Charge	q_{pd}	≤5	pC	Method a (sample test), $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s
				Method b1 (100% production), $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s, $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s
Resistance (Input to Output)[1]	R_{IO}	$>10^{12}$	Ω	T_A = 25°C, V_{TEST} = 500 V dc, t = 60 s
	R_{IO_S}	$>10^{9}$	Ω	$T_A = T_S$, V_{TEST} = 500 V dc, t = 60 s
Capacitance (Input to Output)[1]	C_{IO}	1.5	pF	f_{TEST} = 1 MHz
Climatic Category		40/125/21		
Pollution Degree		2		Per IEC 60664-1
UL 1577				
Maximum Withstanding Isolation Voltage	V_{ISO}	5700	V rms	$V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)

[1] Device measured as a 2-terminal device with Pin 1 to Pin 4 connected and Pin 5 to Pin 8 connected.

SPECIFICATIONS

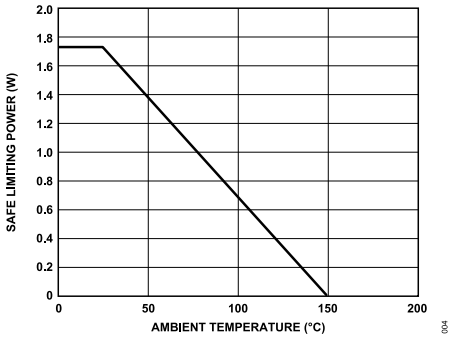


Figure 6. Thermal Derating Curve for 16-Lead Increased Creepage SOIC [SOIC_IC] (RI-16-2), Dependence of Safety Limiting Power with Ambient Temperature per IEC 60747-17

REGULATORY INFORMATION

The ADM3056E has been approved by the organizations listed in Table 4. Copies of the relevant certificates are available at Safety and Regulatory Certifications for Digital Isolation.

Table 4. ADM3056E, 16-Lead Increased Creepage SOIC [SOIC_IC] (RI-16-2) Package Certifications

Regulatory Agency	Safety Standard/Rating	File or Certificate Number
UL	UL 1577 component recognition program Single protection, 5700 V rms isolation voltage	File E214100
CSA[1]	CSA C22.2 No. 14-18 CSA/EN/IEC 62368-1 Basic insulation at 830 V rms Reinforced insulation at 415 V rms CSA/IEC 60601-1 1 MOPP at 519 V rms (pending) 2 MOPP at 261 V rms CSA/IEC 61010-1 Basic insulation at 600 V rms Reinforced insulation at 300 V rms	File 205078
VDE	DIN EN IEC 60747-17 (VDE 0884-17) Reinforced insulation at 849 V peak	Certificate 40051926
CQC	GB 4943.1 Basic insulation at 830 V rms Reinforced insulation at 415 V rms	Certificate CQC19001229587

[1] Working voltages are quoted for Pollution Degree 2, Material Group III and Overvoltage Category II except where otherwise specified. The ADM3056E case material has been evaluated by CSA as Material Group I.

ABSOLUTE MAXIMUM RATINGS

Pin voltages with respect to the GND_X on same side, unless otherwise stated.

Table 5.

Parameter	Rating
V_{DD1}, V_{DD2}	−0.5 V to +6 V
Logic Side Input/Output (TXD, RXD, AUX_{IN}, SILENT, STBY)	−0.5 V to V_{DD1} + 0.5 V
CANH, CANL	−40 V to +40 V
AUX_{OUT}, RS	−0.5 V to V_{DD2} + 0.5 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J Maximum)	150°C
Moisture Sensitivity Level (MSL)	3

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Thermal resistance and characterization parameter values specified in Table 6 are defined and calculated based on the JEDEC JESD51 standards. For more details on their definition and usage, see JEDEC JESD51-12 and the Thermal Analysis section.

Table 6. Package Thermal Data

Package Type	θ_{JA}	θ_{JB}	Ψ_{JB}	Ψ_{JT}	Unit
RI-16-2[1]	72	51	53	7.8	°C/W

[1] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with no vias and still air.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

International Electrotechnical Commission (IEC) electromagnetic compatibility: Part 4-2 (IEC) per IEC 61000-4-2.

ESD Ratings for ADM3056E

Table 7. ADM3056E, 16-Lead SOIC_IC

ESD Model	Withstand Threshold (V)	Class
HBM[1]	±4 kV	3A
IEC[2]	±8 kV (contact discharge) to GND_2	Level 4
	±15 kV (air discharge) to GND_2	Level 4
	±8 kV (contact, across isolation barrier) to GND_1	Level 4

[1] All pins, 1.5 kΩ, 100 pF.

[2] The CANH and CANL pins only.

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

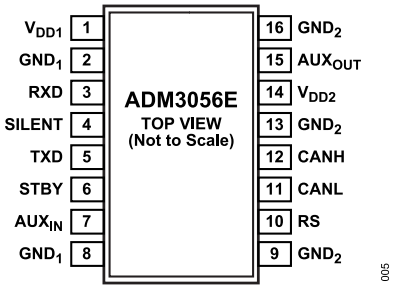


Figure 7. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Power Supply, Logic Side, 1.7 V to 5.5 V. This pin requires 0.1 µF and 0.01 µF decoupling capacitors.
2, 8	GND_1	Ground, Logic Side.
3	RXD	Receiver Output Data.
4	SILENT	Silent Mode Select. Active with input high. Bring this input low or leave the pin unconnected (internal pull-down) for normal mode.
5	TXD	Transmitter Input Data. This pin has a weak internal pull-up resistor to V_{DD1}.
6	STBY	Standby Mode Select. Active with input high. Bring this input low or leave the pin unconnected (internal pull-down) for normal mode.
7	AUX_{IN}	Auxiliary Channel Input. This pin sets the AUX_{OUT} output.
9, 13, 16	GND_2	Ground, Bus Side.
10	RS	Slope Control Pin. Short this pin to ground for full speed operation or use a weak pull-down (for example, 47 kΩ) for slope control mode. An input high signal places the CAN transceiver in standby.
11	CANL	CAN Low Input/Output.
12	CANH	CAN High Input/Output.
14	V_{DD2}	Power Supply, Bus Side, 4.5 V to 5.5 V. This pin requires 0.1 µF and 0.01 µF decoupling capacitors.
15	AUX_{OUT}	Isolated Auxiliary Channel Output per Auxiliary Input in Normal Mode. The state of AUX_{OUT} is latched when STBY is high. By default, AUX_{OUT} is low at startup or when V_{DD1} is unpowered.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

OPERATIONAL TRUTH TABLE

Table 9. Truth Table

Power		Inputs[1, 2]						Outputs		
V_{DD1}	V_{DD2}	TXD	SILENT	STBY	AUX_{IN}	RS	Mode	RXD	AUX_{OUT}	CANH/CANL
On	On	Low	Low	Low	Low	Low/pull-down	Normal/slope mode	Low	Low	Dominant[3]
On	On	Low	Low	Low	High	Low/pull-down	Normal/slope mode	Low	High	Dominant[3]
On	On	High	Low	Low	Low	Low/pull-down	Normal/slope mode	High/per bus	Low	Recessive/set by bus
On	On	High	Low	Low	High	Low/pull-down	Normal/slope mode	High/per bus	High	Recessive/set by bus
On	On	X	High	Low	Low	X	Listen only	High/per bus	Low	Recessive/set by bus
On	On	X	High	Low	High	X	Listen only	High/per bus	High	Recessive/set by bus
On	On	X	X	High	X	X	Standby[4]	High/WUP[5]/filtered	Last state	High-Z, biased to GND_2/set by bus
On	On	X	X	X	Low	High	Standby[4]	High/WUP[5]/filtered	Low	High-Z, based to GND_2/set by bus
On	On	X	X	X	High	High	Standby[4]	High/WUP[5]/filtered	High	High-Z, biased to GND_2/set by bus
Off	On	Z	Z	Z	Z	Low/pull-down	Normal/slope mode	Indeterminate	Low	Recessive/set by bus
On	Off	X	X	X	X	X	Transceiver off	High	Indeterminate	High-Z

1 Z means high impedance within one diode drop of ground.

2 X means don't care.

3 Limited by t_{DT}.

4 RS can only set the transceiver to standby mode. It does not control the digital isolator.

5 WUP means remote wake-up pattern.

TYPICAL PERFORMANCE CHARACTERISTICS

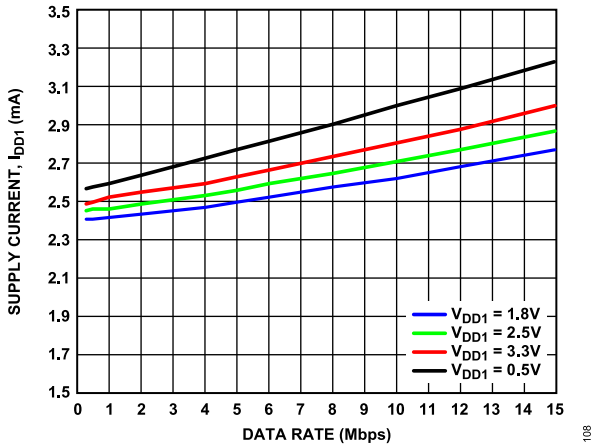


Figure 8. Supply Current, I_{DD1} vs. Data Rate, AUX_{IN} Low

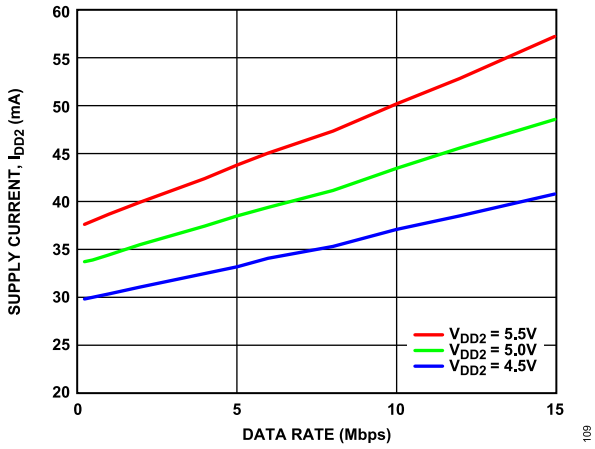


Figure 9. Supply Current, I_{DD2} vs. Data Rate

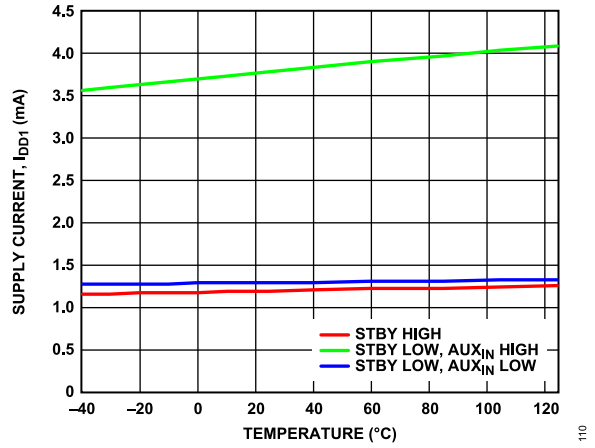


Figure 10. Supply Current, I_{DD1} vs. Temperature (Inputs Idle, V_{DD1} = 5 V)

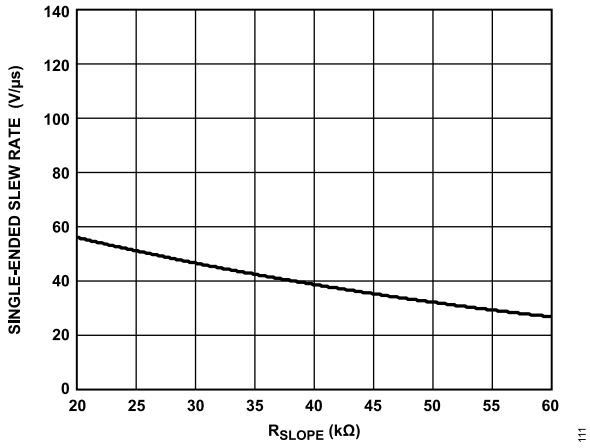


Figure 11. Single-Ended Slew Rate vs. R_{SLOPE}

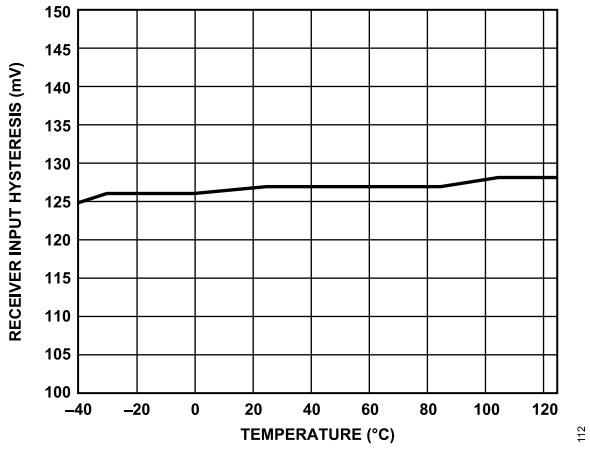


Figure 12. Receiver Input Hysteresis vs. Temperature

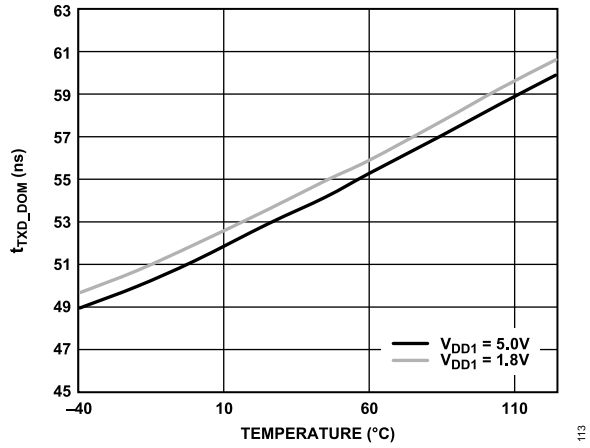


Figure 13. t_{TXD_DOM} vs. Temperature (R_{SLOPE} = 0 Ω)

TYPICAL PERFORMANCE CHARACTERISTICS

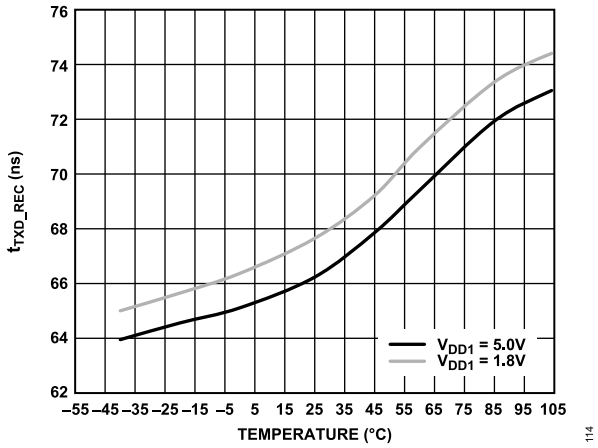


Figure 14. t_{TXD_REC} vs. Temperature (R_{SLOPE} = 0 Ω)

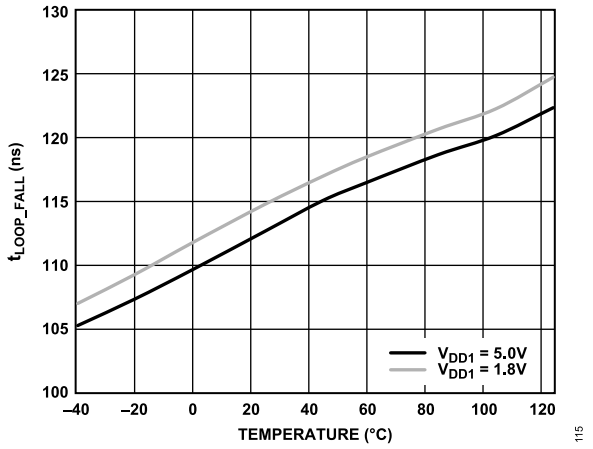


Figure 15. t_{LOOP_FALL} vs. Temperature (R_{SLOPE} = 0 Ω)

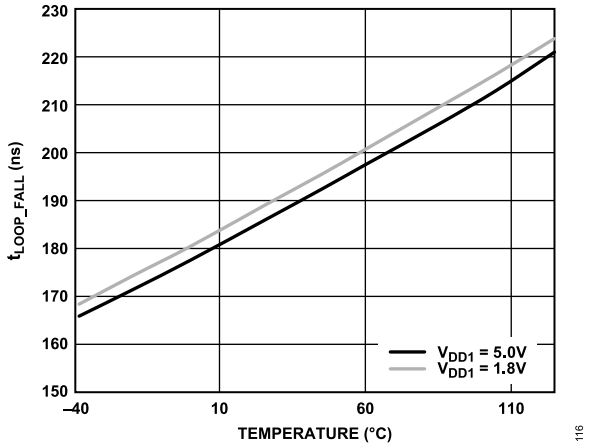


Figure 16. t_{LOOP_FALL} vs. Temperature (R_{SLOPE} = 47 kΩ)

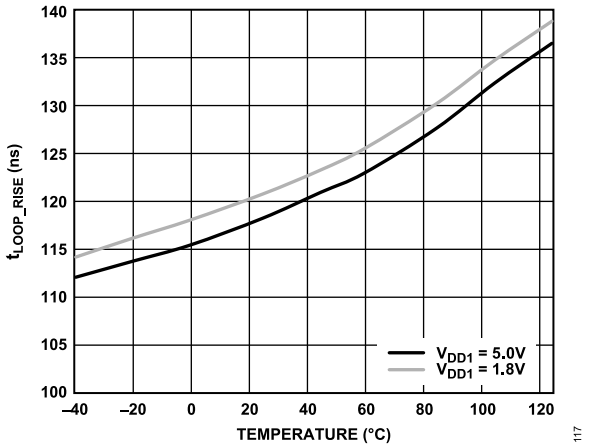


Figure 17. t_{LOOP_RISE} vs. Temperature (R_{SLOPE} = 0 Ω)

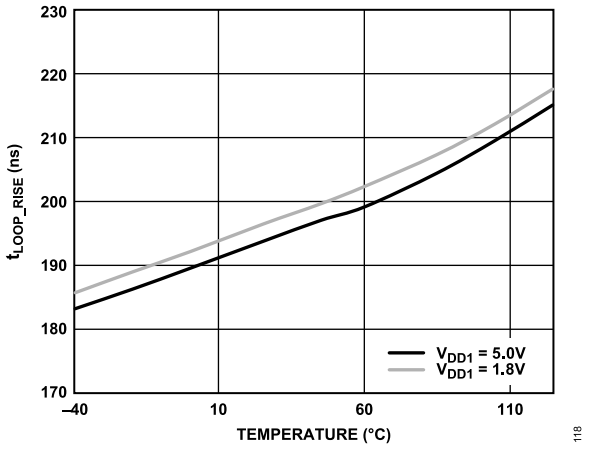


Figure 18. t_{LOOP_RISE} vs. Temperature (R_{SLOPE} = 47 kΩ)

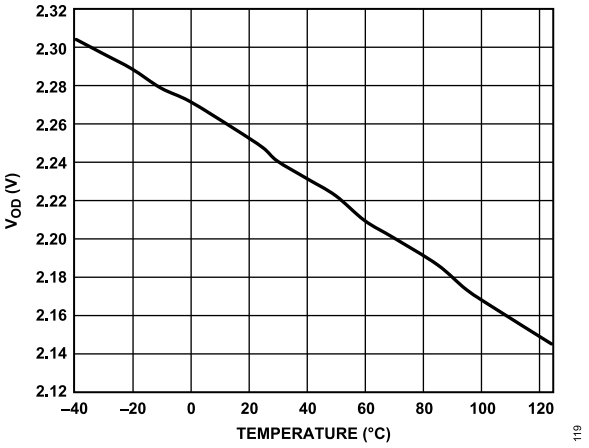


Figure 19. V_{OD} vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

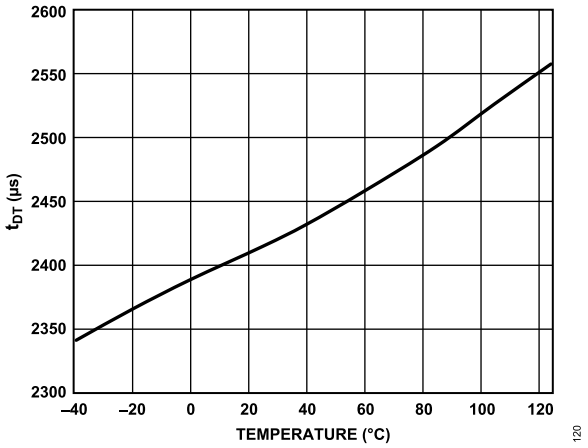


Figure 20. t_{DT} vs. Temperature

TEST CIRCUITS

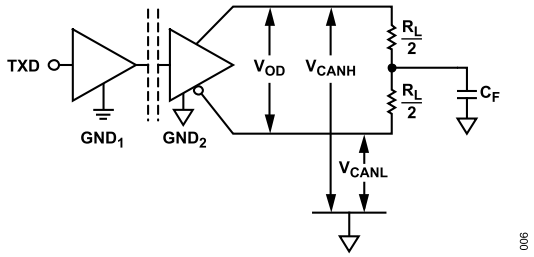


Figure 21. Driver Voltage Measurement

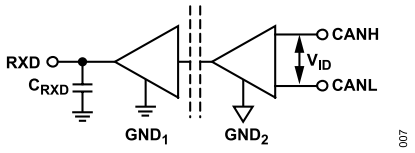
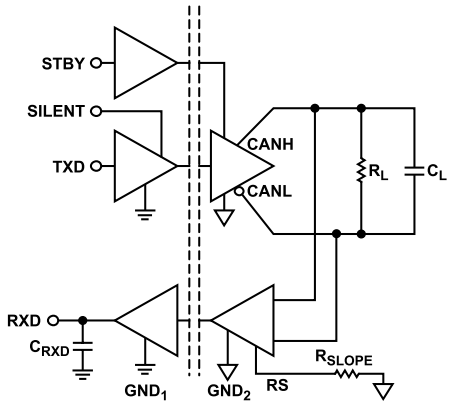


Figure 22. Receiver Voltage Measurement



NOTES
1. 1% TOLERANCE FOR ALL RESISTORS AND CAPACITORS.

008

Figure 23. Switching Characteristics Measurements

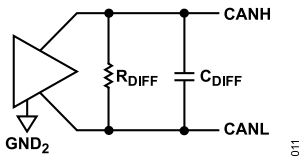


Figure 24. R_{DIFF} and C_{DIFF} Measured in Recessive State, Bus Disconnected

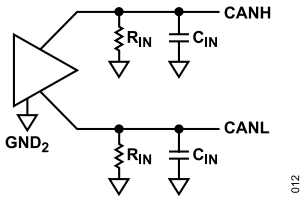


Figure 25. R_{IN} and C_{IN} Measured in Recessive State, Bus Disconnected

TERMINOLOGY

I_{DD1}

I_{DD1} is the current drawn by the V_{DD1} pin. This pin powers the logic side iCoupler digital isolator.

I_{DD2}

I_{DD2} is the current drawn by the V_{DD2} pin. This pin powers the bus side iCoupler digital isolator and transceiver.

V_{OD} and V_{ID}

V_{OD} and V_{ID} are the differential voltages from the transmitter or at the receiver on the CANH and CANL pins.

t_{TXD_DOM}

t_{TXD_DOM} is the propagation delay from a low signal on TXD to transition the bus to a dominant state. See Figure 2 for level definitions.

t_{TXD_REC}

t_{TXD_REC} is the propagation delay from a high signal on TXD to transition the bus to a recessive state. See Figure 2 for level definitions.

t_{LOOP_FALL}

t_{LOOP_FALL} is the propagation delay from a low signal on TXD to the bus dominant and transitions low on the RXD. See Figure 2 for level definitions.

t_{LOOP_RISE}

t_{LOOP_RISE} is the propagation delay from a high signal on TXD to the bus recessive and transitions high on the RXD. See Figure 2 for level definitions.

t_{BIT_TXD}

t_{BIT_TXD} is the bit time on the TXD pin as transmitted by the CAN controller. See Figure 2 for level definitions.

t_{BIT_BUS}

t_{BIT_BUS} is the bit time as transmitted by the transceiver to the bus. When compared with a given t_{BIT_TXD}, a measure of bit symmetry from the TXD digital isolation channel and CAN transceiver can be determined. See Figure 2 for level definitions.

t_{BIT_RXD}

t_{BIT_RXD} is the bit time on the RXD output pin, which can be compared with t_{BIT_TXD} for a round trip measure of pulse width distortion through the TXD digital isolation channel, the CAN transceiver, and back through the RXD isolation channel. See Figure 2 for level definitions.

Wake-Up Pattern

The wake-up pattern is the remote transmitted pattern required to trigger the low speed data transmission by the CAN transceiver while in standby mode. The pattern does not take the transceiver out of standby mode, and its effect on the transceiver times out. See Figure 4 for additional information.

THEORY OF OPERATION

CAN TRANSCEIVER OPERATION

The ADM3056E facilitates galvanically isolated communication between a CAN controller and the CAN bus. The CAN controller and the ADM3056E communicate with standard 1.8 V, 2.5 V, 3.3 V, or 5.0 V CMOS levels.

The CAN bus has two states: dominant and recessive. The recessive state is present on the bus when the differential voltage between CANH and CANL is less than 0.5 V. In the recessive state, the CANH and CANL pins are set to high impedance and are loosely biased to a single-ended voltage of 2.5 V. A dominant state is present on the bus when the differential voltage between CANH and CANL is greater than 1.5 V. The transceiver transmits a dominant state by driving the single-ended voltage of the CANH pin to 3.5 V and the CANL pin to 1.5 V. The recessive and dominant states correspond to CMOS high on the RXD pin and CMOS low on the TXD pin, respectively.

A dominant state from another node overwrites a recessive state on the bus. A CAN frame can be set for higher priority by using a longer string of dominant bits to gain control of the CAN bus during the arbitration phase. While transmitting, a CAN transceiver also reads back the state of the bus. When a CAN controller receives a dominant state while transmitting a recessive state during arbitration, the CAN controller surrenders the bus to the node still transmitting the dominant state. The node that gains control during the arbitration phase reads back only its own transmission. This interaction between recessive and dominant states allows competing nodes to negotiate for control of the bus while avoiding contention between nodes.

Industrial applications can have long cable runs. These long runs can have differences in local earth potential. Different sources may also power nodes. The ADM3056E transceiver has a ±25 V common-mode range (CMR) that exceeds the ISO 11898-2:2016 requirement and further increases the tolerance to ground variation.

See the AN-1123 Application Note for additional information on CAN.

SIGNAL ISOLATION

The ADM3056E device provides galvanic signal isolation implemented on the logic side of the interface. The RXD and TXD isolation channels transmit with an on off keying (OOK) architecture on *i*Coupler digital isolation technology.

The low propagation delay isolation, quick transceiver conversion speeds, and integrated form factor are critical for longer cable lengths and higher data speeds and reducing the total solution board space. The ADM3056E isolated transceiver reduces solution board space while increasing data transfer rates over discrete solutions.

The V_{DD1} supply pin powers the logic side signal isolation. The voltage on this pin scales the digital interface logic from 1.7 V to 5.5 V, depending on the supply voltage to the V_{DD1} pin. The V_{DD2} supply pin powers the bus side digital isolator and CAN transceiver and must be supplied with a nominal 5 V supply.

STANDBY MODE

The STBY pin engages a reduced power standby mode that modifies the operation of both the CAN transceiver and digital isolation channels. Standby mode disables the TXD signal isolation channel and sets the transmitter output to a high impedance state loosely biased to GND_2. While in standby mode, the receiver filters bus data and responds only after the remote wake-up sequence is received.

When entering or exiting standby mode, the TXD input must be kept high and the RXD output must be ignored for the full t_{STBY_ON} and t_{STBY_OFF} times.

REMOTE WAKE UP

The ADM3056E responds to the remote wake-up sequence as defined in ISO 11898-2:2016. When the CAN transceiver is presented with the defined slow speed, high to low to high sequence within the low wake-up pattern detection reset time (t_{WUPR}), low speed data transmission is allowed.

Receipt of the remote wake-up pattern does not bring the ADM3056E out of standby mode. The ADM3056E STBY pin must be brought low externally to exit standby mode. After the ADM3056E receives the remote wake-up pattern, the transceiver continues to receive low speed data until standby mode is exited.

SILENT MODE

Asserting the SILENT pin disables the TXD digital isolation channel. Any inputs to the TXD pin are ignored in this mode, and the transceiver presents a recessive bus state. The operation of the RXD channel is unaffected. The RXD channel continues to output data received from the internal CAN transceiver monitoring the bus.

Silent mode is useful when paired with a CAN controller using automatic baud rate detection. A CAN controller must be set to the same data rate as all attached nodes. The CAN controller produces an error frame and ties up the bus with a dominant state when the received data rate is different from expected. Other CAN nodes then echo this error frame. While in silent mode, the error frames produced by the CAN controller are kept from interrupting bus traffic, and the controller can continue listening to bus traffic.

RS

The RS pin sets the transceiver in one of three different modes of operation: high speed, slope control, or standby. This pin cannot be left floating.

For high speed mode, connect the RS pin directly to GND_2. Ensure that the transition time of the CAN bus signals is as short as possible to allow higher speed signaling. A shielded cable is recommended to avoid electromagnetic interference (EMI) problems in high speed mode.

THEORY OF OPERATION

Slope control mode allows the use of unshielded twisted pair wires or parallel pair wires as bus lines. Slow the signal rise and fall transition times to reduce EMI and ringing in slope control mode. Adjust the rise and fall slopes by adding a resistor (R_{SLOPE}) connected from RS to GND_2. The slope is proportional to the current output at the RS pin.

The RS pin can also set the CAN transceiver to standby mode, which occurs when the pin is driven to a voltage above V_{STB}. In standby mode, high speed data is filtered, and the CANH and CANL lines are biased to GND_2.

The RS pin can only set the CAN transceiver to standby mode. The state of the RS pin does not modify the operation of digital isolation channels or the auxiliary channel.

AUXILIARY CHANNEL

The auxiliary channel is available for low speed data transmission at up to 20 kHz (or 40 kbps nonreturn-to-zero format) when STBY is not asserted. The data rate limit of the channel allows the data channel to be shared by the STBY signal.

In standby mode, or when STBY is driven high, the operation of the channel is modified to share the multiplexed signal path with the STBY signal (see Figure 1). The AUX_{OUT} pin remains latched in the state when STBY is asserted. Periodic pulses (<25 µs wide) are sent to indicate that the logic side is powered and remains in standby mode.

In applications where AUX_{OUT} may be shorted to GND_2 or V_{DD2}, add a series resistance to the output channel.

INTEGRATED AND CERTIFIED IEC EMC SOLUTION

Typically, designers must add protection against harsh operating environments while also making the device as small as possible. To reduce board space and the design effort needed to meet the system level ESD standards, the ADM3056E has robust protection circuitry on chip for the CANH and CANL pins.

FAULT PROTECTION

High voltage miswire events commonly occur when the system power supply is connected directly to the CANH and the CANL bus lines during assembly. Supplies may also be shorted by accidental damage to the fieldbus cables while the system is operating. Accounting for inductive kickback and switching effects, the ADM3056E isolated transceiver CAN bus lines are protected against these miswire or shorting events in systems with up to nominal 24 V supplies. The CANH and CANL signal lines can withstand a continuous supply short with respect to GND_2 or between the CAN bus lines without damage. This level of protection applies when the device is either powered or unpowered.

FAIL-SAFE FEATURES

In cases where the TXD input pin is allowed to float, to prevent bus traffic interruption, the TXD input channel has an internal pull-up to the V_{DD1} pin. The pull-up holds the transceiver in the recessive state.

The ADM3056E features a dominant timeout (t_{DT} in Table 2). A TXD line shorted to ground or malfunctioning CAN controller are examples of how a single node can indefinitely prevent further bus traffic. The dominant timeout limits how long the transceiver can transmit in the dominant state. When the TXD pin is presented with a logic high, normal TXD functionality is restored.

The t_{DT} minimum also inherently creates a minimum data rate. Under normal operation, the CAN protocol allows five consecutive bits of the same polarity before stuffing a bit of the opposite polarity into the transmitting bit sequence. When an error is detected, the CAN controller purposely violates the bit stuffing rules by producing six consecutive dominant bits. At any given data rate, the CAN controller must transmit as many as 11 consecutive dominant bits to effectively limit the ADM3056E minimum data rate to 9600 bps.

THERMAL SHUTDOWN

The ADM3056E contains thermal shutdown circuitry that protects the device from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature under this condition and disables the driver outputs. The circuitry disables the driver outputs when the die temperature reaches 175°C. When the die has cooled, the drivers are enabled again.

APPLICATIONS INFORMATION

RADIATED EMISSIONS AND PCB LAYOUT

The ADM3056E isolated CAN transceiver is designed to pass EN55022 Class B by 6 dB on a simple 2-layer PCB design. Stitching capacitance or surface-mount technology (SMT) safety capacitors are not required to meet this emissions level.

PCB LAYOUT

The ADM3056E digital isolator requires no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 26). Bypass capacitors are most conveniently connected between Pin 1 and Pin 2 for V_{DD1} and between Pin 15 and Pin 16 for V_{DD2}. The recommended bypass capacitor value is between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin must not exceed 10 mm. Bypassing between Pin 1 and Pin 8 and between Pin 9 and Pin 16 must also be considered, unless the ground pair on each package side is connected close to the package.

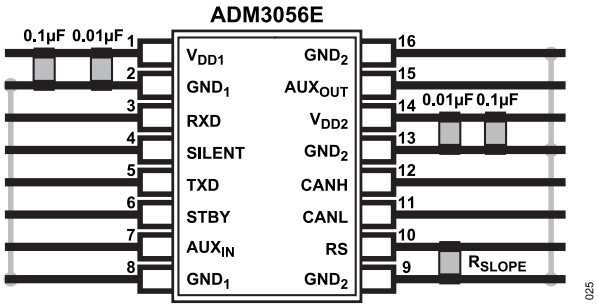


Figure 26. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, design the board layout such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this coupling can cause voltage differentials between pins exceeding the absolute maximum ratings of the device, thereby leading to latch-up or permanent damage.

Note that the total lead length between the ends of the low equivalent series resistance (ESR) capacitor and the input power supply pin must not exceed 2 mm. Installing the bypass capacitor with traces more than 2 mm in length may result in data corruption.

THERMAL ANALYSIS

The ADM3056E consists of three internal die attached to a split lead frame with two die attach pads. For the purposes of thermal analysis, the die are treated as a single thermal unit, with the highest junction temperature reflected in the thermal parameter values from Table 6. The thermal parameter values are based on thermal simulations with the devices mounted on a JEDEC standard, 4-layer board with fine width traces and still air. Under normal operating conditions, the ADM3056E can operate at full load across the full temperature range without derating the output current.

θ_{JA} and θ_{JB} are mainly used to compare the thermal performance of the package of the device with other semiconductor packages when all test conditions listed are similar. θ_{JA} and θ_{JB} can be used for first order approximation of the junction temperature in the system environment.

If an accurate thermal measurement of the board temperature near the device under test or directly on the package top surface operating in the system environment is available along with the corresponding device power dissipation, then using Ψ_{JB} or Ψ_{JT} is a more appropriate way to estimate the junction temperature in the system environment. Use Ψ_{JB} when the temperature measurement point is on the board or Ψ_{JT} when it is on the package top. The junction temperature is estimated using the following equation:

$$T_J = \psi_{Jx} \times P_d + T_x \quad (1)$$

where

P_d is the dissipated power.

T_x is the measured temperature at location *x* and *x* is either *B* for the PCB or *T* for the package top.

The temperature measurement point for θ_{JB} and Ψ_{JB} is between Pin 5 and Pin 6 on the outer edge of the pin footprint. The temperature measurement point for Ψ_{JT} is at the center of the top side of the package.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation as well as on the materials and material interfaces. Analog Devices conducts an extensive set of evaluations to determine the lifetime of the insulation structure within the ADM3056E as per IEC 60747-17.

SURFACE TRACKING

Surface tracking is addressed in electrical safety standards by setting a minimum surface creepage based on the working voltage, the environmental conditions, and the properties of the insulation material. Safety agencies perform characterization testing on the surface insulation of components that allows the components to be categorized in different material groups. Lower material group ratings are more resistant to surface tracking and, therefore, can provide adequate lifetime with smaller creepage. The minimum creepage for a given working voltage and material group is in each system level standard and is based on the total rms voltage across the isolation, pollution degree, and material group.

The material group and creepage for the ADM3056E isolator are listed in Table 3 for the 16-lead SOIC with increased creepage package.

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
RI-16-2	SOIC_IC	16-Lead Standard Small Outline Package with Increased Creepage

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADM3056EBRIZ	−40°C to +125°C	16-Lead Standard Small Outline Package with Increased Creepage [SOIC_IC]	Tube, 37	RI-16-2
ADM3056EBRIZ-RL	−40°C to +125°C	16-Lead Standard Small Outline Package with Increased Creepage [SOIC_IC]	Reel, 1000	RI-16-2

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
EVAL-ADM3056EEBZ	ADM3056E Evaluation Board

[1] Z = RoHS Compliant Part.

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