

# SC18IS606

## I<sup>2</sup>C-Bus to SPI Bridge

Rev. 1.1 — 27 May 2026

Product data sheet



## 1 General description

---

SC18IS606 is designed to serve as an interface between a standard Inter-Integrated Circuit bus (I<sup>2</sup>C-bus) of a microcontroller and a Serial Peripheral Interface (SPI) bus. This allows the microcontroller to communicate directly with SPI devices through its I<sup>2</sup>C-bus. SC18IS606 operates as an I<sup>2</sup>C-bus target-transmitter or target-receiver and an SPI controller. SC18IS606 controls all the SPI bus-specific sequences, protocol, and timing. SC18IS606 has its own internal oscillator, and it supports three SPI chip select outputs that can be configured as General-Purpose Input/Output (GPIO) when not used as SPI Chip Select (CS).

SC18IS606 is a functional replacement for SC18IS602B except for:

- New pinout
- Three instead of four chip selects; no quasi-bidirectional mode
- Lower operating supply voltage level (1.71 V vs 2.4 V)
- Data buffer increased to 1024 bytes vs 200 bytes
- Temperature range of -40 °C to +105 °C vs -40 °C to +85 °C
- The device is rotated 180 degrees in the tape pocket; pin 1 is now in Quadrant 1



## 2 Features and benefits

---

- I<sup>2</sup>C-bus target interface operating up to 400 kHz
- SPI controller operating up to 1.8 Mbit/s
- 1024-byte data buffer
- Up to three targets select outputs
- Up to three programmable I/O pins
- Operating supply voltage: 1.71 V to 3.6 V
- Low power mode
- Internal oscillator
- Active LOW interrupt output
- Electrostatic Discharge (ESD) protection exceeds 2000 V Human Body Model (HBM) per JESD22-A114
- Latch-up testing is done to JEDEC Standard JESD78 that exceeds 100 mA
- Available in 16-pin TSSOP

### 3 Applications

---

- Converting I<sup>2</sup>C-bus to SPI
- Adding additional SPI bus controllers to an existing system

## 4 Ordering information

[Table 1](#) describes the ordering information of SC18IS606.

**Table 1. Ordering information**

Type number	Topside marking	Package		
		Name	Description	Version
SC18IS606PW	18IS606	TSSOP16	Plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

### 4.1 Ordering options

[Table 2](#) describes the ordering options of SC18IS606.

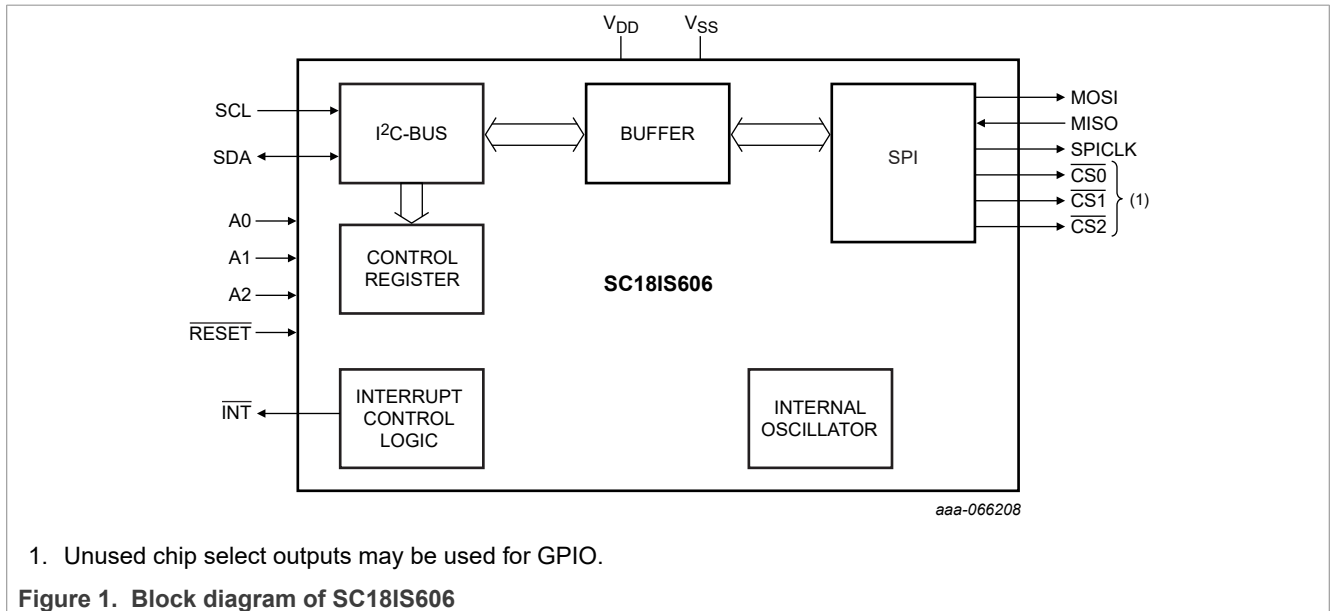
**Table 2. Ordering options**

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
SC18IS606PW	SC18IS606PWJ	TSSOP16	REEL 13" Q1 *STANDARD MARK SMD <sup>[1]</sup>	2500	T <sub>amb</sub> = -40 °C to +105 °C

[1] Find packing information at [www.nxp.com/docs/en/packing/SOT403-1\\_118.pdf](http://www.nxp.com/docs/en/packing/SOT403-1_118.pdf).

## 5 Block diagram

Figure 1 shows the block diagram of SC18IS606.



## 6 Pinning information

This section provides the pin configuration and pin description of the SC18IS606.

### 6.1 Pinning

Figure 2 shows the pin configuration of SC18IS606.

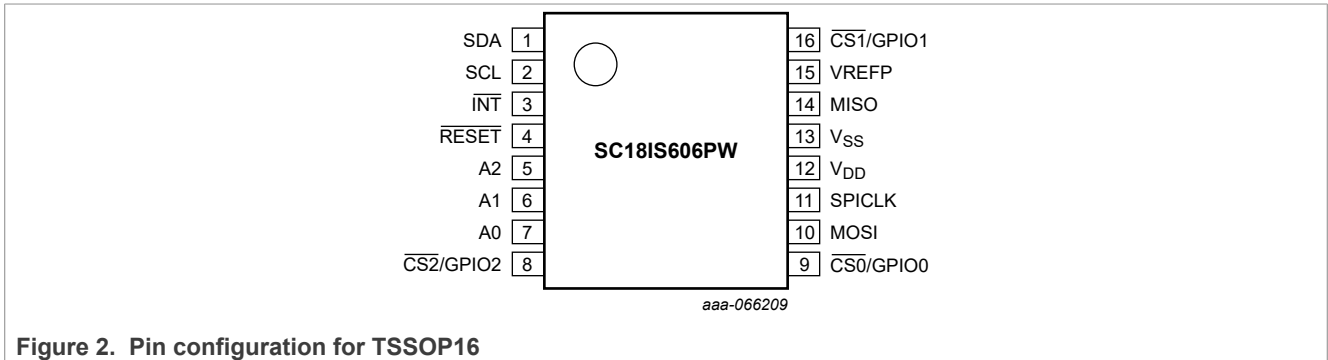


Figure 2. Pin configuration for TSSOP16

### 6.2 Pin description

Table 3 provides detailed description of various pins on SC18IS606.

Table 3. Pin description

Symbol	Pin	Type	Description
CS0/GPIO0	9	I/O	SPI chip select output 0 (active LOW) or GPIO 0
CS1/GPIO1	16	I/O	SPI chip select output 1 (active LOW) or GPIO 1
RESET	4	I	Reset input (active LOW)
V <sub>SS</sub>	13	-	Ground supply
CITO	14	I	Controller In, target Out
COTI	10	O	Controller Out, target In
SDA	1	I/O	I <sup>2</sup> C-bus data
SCL	2	I	I <sup>2</sup> C-bus clock
INT	3	O	Interrupt output (active LOW). This pin is an open-drain pin, which must be pulled HIGH with a resistor and must not be held LOW at power on or reset
CS2/GPIO2	8	I/O	SPI chip select output 2 (active LOW) or GPIO 2
SPICLK	11	O	SPI clock
V <sub>DD</sub>	12	-	Supply voltage
VREFP	15	-	Must connect to V <sub>DD</sub>
A0	7	I	Address input 0
A1	6	I	Address input 1
A2	5	I	Address input 2

## 7 Functional description

SC18IS606 acts as a bridge between an I<sup>2</sup>C-bus and an SPI interface. It allows an I<sup>2</sup>C-bus controller device to communicate with any SPI-enabled device.

### 7.1 I<sup>2</sup>C-bus interface

The I<sup>2</sup>C-bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus, and it has the following features:

- Bidirectional data transfer between controllers and targets
- Multi-controller bus (no central controller)
- Arbitration between simultaneously transmitting controllers without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- The I<sup>2</sup>C-bus can be used for test and diagnostic purposes

A typical I<sup>2</sup>C-bus configuration is shown in [Figure 3](#) (refer to NXP Semiconductors [UM10204](#), I<sup>2</sup>C-bus specification and user manual).

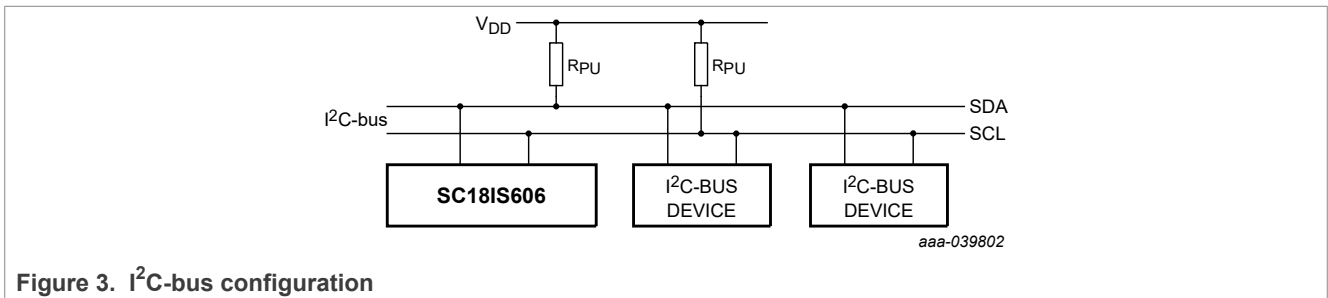


Figure 3. I<sup>2</sup>C-bus configuration

SC18IS606 device provides a byte-oriented I<sup>2</sup>C-bus interface that supports data transfers up to 400 kHz. When the I<sup>2</sup>C-bus controller is reading data from SC18IS606, the device is a target-transmitter. SC18IS606 is a target-receiver when the I<sup>2</sup>C-bus controller is sending data. At no time does SC18IS606 act as an I<sup>2</sup>C-bus controller, however, it can hold the SCL line LOW between bytes to complete its internal processes (for example, clock stretching).

#### 7.1.1 Addressing

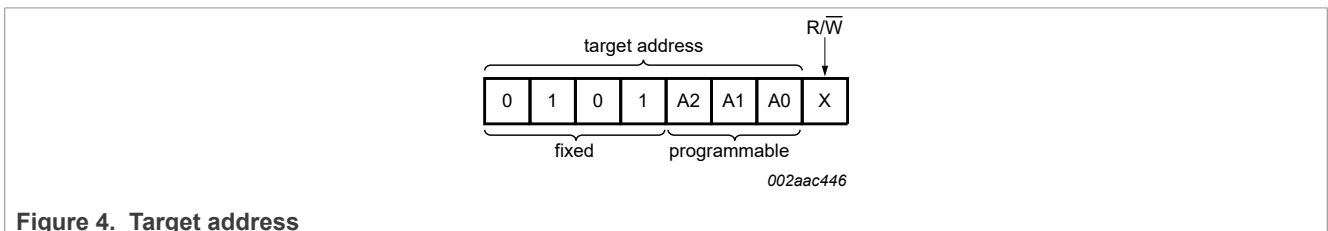


Figure 4. Target address

The first seven bits of the first byte sent after a START condition defines the target address of the device being accessed on the bus. The eighth bit determines the direction of the message. A '0' in the least significant position of the first byte means that the controller writes information to a selected target. A '1' in this position means that the controller reads information from the target. When an address is sent, each device in a system compares the first seven bits after the START condition with its address. If they match, the device considers itself addressed by the controller as a target-receiver or target-transmitter, depending on the R/W bit.

A target address of SC18IS606 consists of a fixed and a programmable part. The programmable part of the target address enables the maximum number of such devices to be connected to the I<sup>2</sup>C-bus. Since SC18IS606

has three programmable address bits (defined by the A2, A1, and A0 pins), it is possible to have eight of these devices on the same bus.

The state of the A2, A1, and A0 pins are latched at reset. Changes made after reset do not alter the address.

When SC18IS606 is busy after the address byte is transmitted, it will not acknowledge its address.

### 7.1.2 Write to a data buffer

All communications to or from SC18IS606 occur through the data buffer. The data buffer is 1024 bytes deep. A message begins with SC18IS606 address, followed by the Function ID. Depending upon the Function ID, zero to 1024 data bytes can follow.

SC18IS606 places the data received into a buffer and continue loading the buffer until a STOP condition is received. After the STOP condition is detected, further communications are not acknowledged until the function designated by the Function ID has been completed.

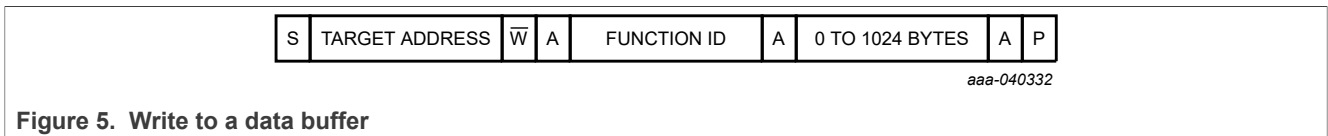


Figure 5. Write to a data buffer

### 7.1.3 SPI read and write - Function ID 01h to 0x7h

Data in the buffer is sent to the SPI port if the Function ID is 01h to 0x7h. The Function ID contains the Chip Select (CS) to be used for the transmission on the SPI port. There are three target selects that can be used, with each CS being selected by one of the bits in the Function ID. There is no restriction on the number or combination of CSs that can be enabled for an SPI message. If more than one CS<sub>n</sub> pin is enabled at one time, the user must be aware of possible contention on the data outputs of the SPI target devices.

Table 4. Function ID 01h to 0x7h

7	6	5	4	3	2	1	0
0	0	0	0	0	CS2	CS1	CS0

The data on the SPI port contains the same information as the I<sup>2</sup>C-bus data, but without the target address and Function ID. For example, if the message shown in Figure 6 is transmitted on the I<sup>2</sup>C-bus, the SPI bus sends the message shown in Figure 7.

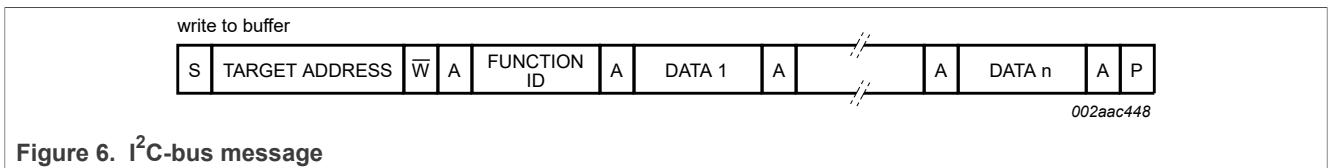


Figure 6. I<sup>2</sup>C-bus message

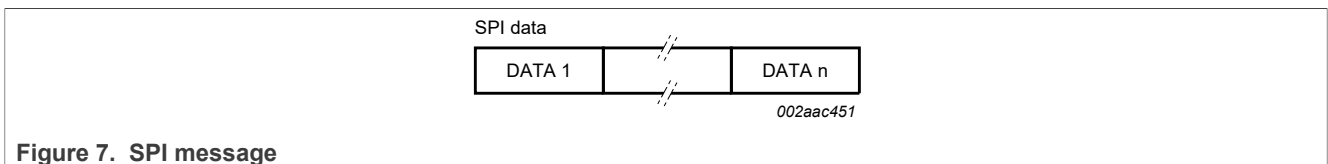


Figure 7. SPI message

SC18IS606 counts the number of data bytes sent to the I<sup>2</sup>C-bus port and automatically sends this same number of bytes to the SPI bus. As the data is transmitted from the COT1 pin, it is also read from the CITO pin and saved in the data buffer. Therefore, the old data in the buffer is overwritten. The data in the buffer can then be read back.

If the data from the SPI bus must be returned to the I<sup>2</sup>C-bus controller, the process must be completed by reading the data buffer. [Section 8](#) gives an example of an SPI read.

7.1.4 Read from buffer

A read from the data buffer requires no Function ID. The target address with the R/W bit set to a '1' causes SC18IS606 to send the buffer contents to the I<sup>2</sup>C-bus controller. The buffer contents are not modified during the read process.

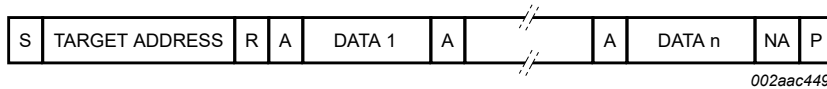


Figure 8. Read from buffer

A typical write and read from an SPI Electrically Erasable Programmable Read-Only Memory (EEPROM) is shown in [Section 8](#).

After a read, the interrupt line is cleared.

7.1.5 Configure SPI Interface - Function ID F0h

The SPI hardware operating mode, data direction, and frequency can be changed by sending a **Configure SPI Interface** command to the I<sup>2</sup>C-bus.

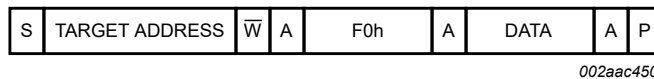


Figure 9. Configure SPI Interface

After SC18IS606 address is transmitted on the bus, the Configure SPI Interface Function ID (F0h) is sent followed by a byte, which defines the SPI communications.

The Clock Phase bit (CPHA) allows the user to set the edges for sampling and changing data. The Clock Polarity bit (CPOL) allows the user to set the clock polarity. [Figure 18](#) and [Figure 19](#) show the different settings of Clock Phase bit.

Table 5. Configure SPI Interface (F0h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	X	X	ORDER	X	MODE1	MODE0	F1	F0
Reset	X	X	0	X	0	0	0	0

Table 6. Configure SPI Interface (F0h) bit description

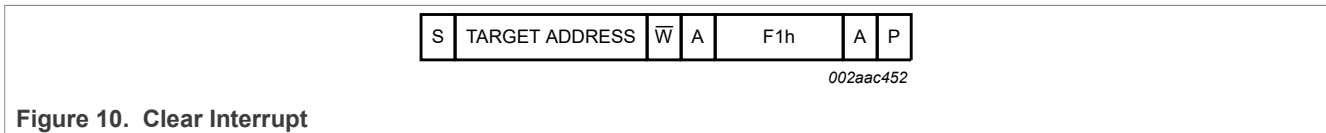
Bit	Symbol	Description
7:6	-	Reserved
5	ORDER	When logic 0, the MSB of the data word is transmitted first. If logic 1, the Least Significant Bit (LSB) of the data word is transmitted first.
4	-	Reserved
3:2	MODE1:MODE0	Mode selection 00 - SPICLK LOW when idle; data clocked in on leading edge (CPOL = 0, CPHA = 0) 01 - SPICLK LOW when idle; data clocked in on trailing edge (CPOL = 0, CPHA = 1)

Table 6. Configure SPI Interface (F0h) bit description...continued

Bit	Symbol	Description
		10 - SPICLK HIGH when idle; data clocked in on trailing edge (CPOL = 1, CPHA = 0) 11 - SPICLK HIGH when idle; data clocked in on leading edge (CPOL = 1, CPHA = 1)
1:0	F1:F0	SPI clock rate 00 - 1875 kHz 01 - 455 kHz 10 - 115 kHz 11 - 58 kHz

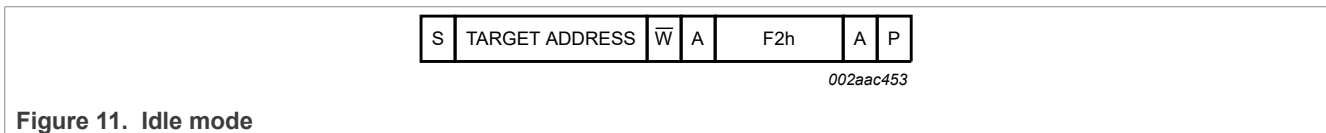
7.1.6 Clear Interrupt - Function ID F1h

SC18IS606 generates an interrupt after completing any SPI transmission. This interrupt can be cleared ( $\overline{INT}$  pin HIGH) by sending a **Clear Interrupt** command. It is not necessary to clear the interrupt; when polling the device, this function can be ignored.



7.1.7 Idle mode - Function ID F2h

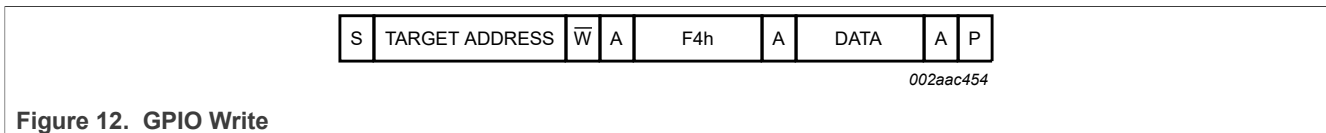
A low-power mode can be entered by sending the **Idle Mode** command.



The Idle mode is exited when its I<sup>2</sup>C-bus address is detected.

7.1.8 GPIO Write - Function ID F4h

The state of the pins defined as GPIO can be changed using the Port Write function.



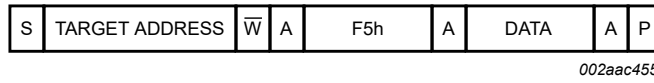
The data byte following the F4h command determines the state of CS2, CS1, and CS0, if they are configured as GPIO. If these pins are used as SPI target selects or if they are GPIO, the Port Enable function defines.

Table 7. GPIO Write (F0h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	X	X	X	X	X	CS2	CS1	CS0
Reset	X	X	X	X	X	0	0	0

7.1.9 GPIO Read - Function ID F5h

The state of the pins defined as GPIO can be read into SC18IS606 data buffer using the GPIO Read function.



002aac455

Figure 13. GPIO Read

**Note:** This function does not return the value of the GPIO. To receive the GPIO contents, a one-byte Read Buffer command would be required. The value of the Read Buffer command returns the following byte.

Table 8. GPIO Read (F5h) bit allocation

7	6	5	4	3	2	1	0
X	X	X	X	X	CS2	CS1	CS0

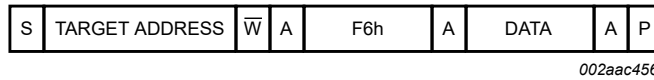
Data for pins not defined as GPIO are undefined.

A GPIO Read is always performed to update the GPIO data in the buffer. The buffer is undefined after the GPIO data is read back from the buffer. Therefore, reading data from the GPIO always requires a two-message sequence (GPIO Read, followed by Read Buffer).

7.1.10 GPIO Enable - Function ID F6h

At reset, the chip select pins ( $\overline{CS0}$ ,  $\overline{CS1}$ , and  $\overline{CS2}$ ) are configured to be used as chip select outputs. If these pins are not required for the SPI functions, they can be used as GPIO after they are enabled as GPIO. Any combination of pins can be configured to function as GPIO or chip selects.

After the GPIO Enable function is sent, the ports defined as GPIO are configured as input-only.



002aac456

Figure 14. GPIO Enable

The data byte following the F6h command byte determines which pins can be used as GPIO. A logic 1 enables the pin as a GPIO, while a logic 0 disables GPIO control.

Table 9. GPIO Enable (F6h) bit allocation

7	6	5	4	3	2	1	0
X	X	X	X	X	CS2	CS1	CS0

**7.1.11 GPIO Configuration - Function ID F7h**

The pins defined as GPIO can be configured by software to one of three types on a pin-by-pin basis. These are: push-pull, open-drain, and input-only.

Two bits select the output type for each port pin.

**Table 10. GPIO Configuration (F7h) bit allocation**

7	6	5	4	3	2	1	0
X	X	CS2.1	CS2.0	CS1.1	CS1.0	CS0.1	CS0.0

**Table 11. GPIO Configuration (F7h) bit description**

Bit	Symbol	Description	
7	X		
6	X		
5	CS2.1	CS2[1:0] = 00: input-only (high-impedance) CS2[1:0] = 01: push-pull CS2[1:0] = 10: input-only (high-impedance) CS2[1:0] = 11: open-drain	
4	CS2.0		
3	CS1.1		CS1[1:0] = 00: input-only (high-impedance) CS1[1:0] = 01: push-pull CS1[1:0] = 10: input-only (high-impedance) CS1[1:0] = 11: open-drain
2	CS1.0		
1	CS0.1	CS0[1:0] = 00: input-only (high-impedance) CS0[1:0] = 01: push-pull CS0[1:0] = 10: input-only (high-impedance) CS0[1:0] = 11: open-drain	
0	CS0.0		

The  $\overline{CS}_n$  pins defined as GPIO, for example CS0.0 and CS0.1, can be configured by software to one of three types. These are: push-pull, open-drain, and input-only. Two configuration bits in the GPIO Configuration register for each pin select the type for each pin. A pin has a Schmitt-triggered input that also has a glitch suppression circuit.

**7.1.11.1 Open-drain output configuration**

The open-drain output configuration turns off all pull-ups and only drives the pulldown transistor of the pin when the port latch contains a logic 0. To be used as a logic output, a pin configured in this manner must have an external pullup, typically a resistor tied to V<sub>DD</sub>.

The open-drain pin configuration is shown in [Figure 15](#).

An open-drain pin has a Schmitt-triggered input that also has a glitch suppression circuit.

The device uses a pseudo open-drain mode. The pin cannot be pulled up above V<sub>DD</sub>. The pins are not 5 V tolerant when V<sub>DD</sub> is grounded.

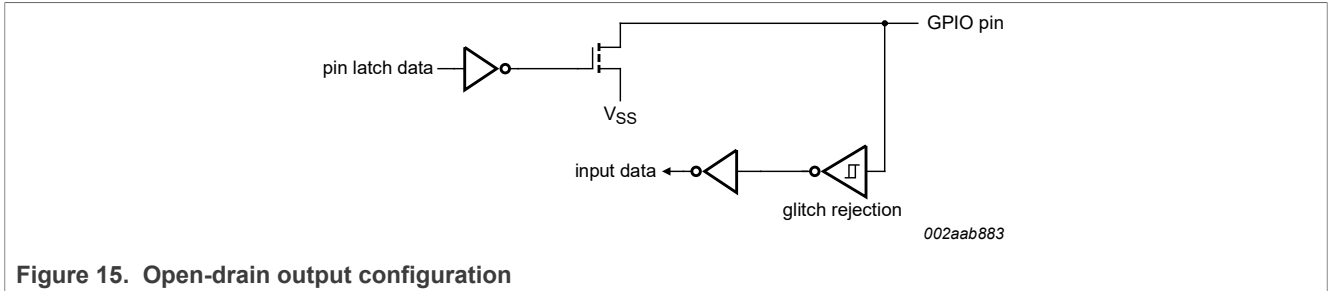


Figure 15. Open-drain output configuration

### 7.1.11.2 Input-only configuration

The input-only pin configuration is shown in [Figure 16](#). It is a Schmitt-triggered input that also has a glitch suppression circuit.

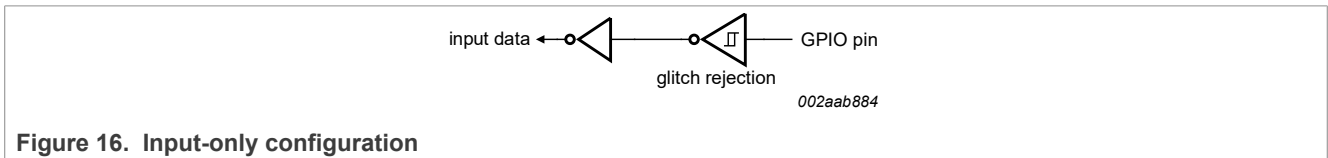


Figure 16. Input-only configuration

### 7.1.11.3 Push-pull output configuration

The push-pull output configuration has the same pulldown structure as the open-drain but provides a continuous strong pullup when the port latch contains a logic 1. The push-pull mode can be used when source current is needed from a pin output.

The push-pull pin configuration is shown in [Figure 17](#).

A push-pull pin has a Schmitt-triggered input that also has a glitch suppression circuit.

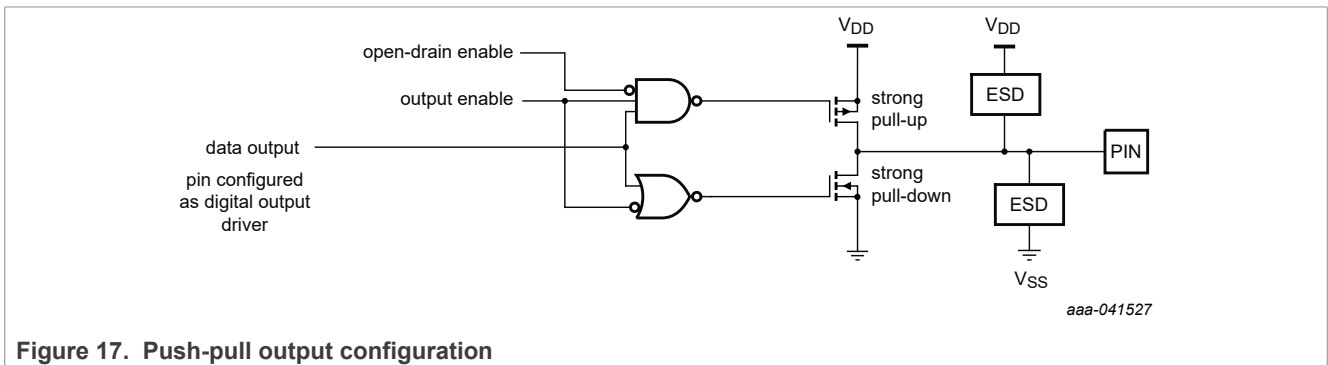


Figure 17. Push-pull output configuration

### 7.1.12 Read Version: Function ID FEh

This function commands the SC18IS606 to place version information into the read buffer. Once this command is issued, a null terminated string is placed in the read buffer. The string contains the part number and a version string "SC18IS606 1.0.0".

The total length is 16 bytes including a 00h null terminator. Values in the Read buffer past the null terminator remain from a previous operation. The example above yields these hex values in the first 16 locations in the read buffer: 0x53 0x43 0x31 0x38 0x49 0x53 0x36 0x30 0x36 0x20 0x31 0x2e 0x30 0x2e 0x30 0x00

## 7.2 SPI interface

The SPI interface can support Mode 0 through Mode 3 of the SPI specification and can operate up to 1.8 Mbit/s. The SPI interface uses at least four pins: SPICLK, COTI, CITO, and  $\overline{CSn}$ .

$\overline{CSn}$  are the chip select pins. In a typical configuration, an SPI controller selects one SPI device as the current target.

There are actually three  $\overline{CSn}$  pins ( $\overline{CS0}$ ,  $\overline{CS1}$ , and  $\overline{CS2}$ ) to allow SC18IS606 to communicate with multiple SPI devices.

SC18IS606 generates the SPICLK (SPI clock) signal to send and receive data. The SCLK, COTI, and CITO are typically tied together between two or more SPI devices. Data flows from SC18IS606 (controller) to target on the COTI pin (pin 10) and the data flows from target to SC18IS606 (controller) on the CITO pin (pin 14).

## 8 I<sup>2</sup>C-bus to SPI communications example

The following example describes a typical sequence of events required to read the contents of an SPI-based EEPROM. This example assumes that SC18IS606 is configured to respond to address 50h. A START condition is shown as 'ST', while a STOP condition is 'SP'. The data is presented in hexadecimal format.

This sequence is not included in the testing, as there is no EEPROM on the bridge board, but it must work as written. A script for reading SPI Flash was tested, however.

1. The first message is used to configure the SPI port for mode and frequency.

```
ST,50,F0,02,SP SPI frequency 115 kHz using Mode 0
```

2. An SPI EEPROM first requires that a Write Enable command be sent before data can be written.

```
ST,50,04,06,SP EEPROM write enable using CS2, assuming the Write Enable is 06h
```

3. Clear the interrupt. This is not required if using a polling method rather than interrupts.

```
ST,50,F1,SP Clear interrupt
```

4. Write the 8 data bytes. The first byte (Function ID) tells SC18IS606, which chip select output to use. This example uses CS2 (shown as 04h). The first byte sent to the EEPROM is normally 02h for the EEPROM write command. The next one or two bytes represent the subaddress in the EEPROM. In this example, a two-byte subaddress is used. Bytes 00 and 30 would cause the EEPROM to write to subaddress 0030h. The next eight bytes are the eight data bytes that are written to subaddresses 0030h through 0037h.

```
ST,50,04,02,00,30,01,02,03,04,05,06,07,08,SP Write 8 bytes using CS2
```

5. When an interrupt occurs, do a Clear Interrupt or wait until SC18IS606 responds to its I<sup>2</sup>C-bus address.

```
ST,50,F1,SP Clear interrupt
```

6. Read the eight bytes from the EEPROM. Note that a command is written, even though a read from the SPI port is performed. The Function ID is again 04h, indicating that CS2 is used. The EEPROM requires a 03h for a read, followed by the subaddress to be read. The same data previously written is read back, so the subaddress is 0030h. To read back eight bytes, eight bytes of FFh are sent to tell SC18IS606 to send eight more bytes on COTI. While it is sending these eight data bytes, it is also reading the CITO pin and saving the data in the buffer.

```
ST,50,04,03,00,30,FF,FF,FF,FF,FF,FF,FF,FF,SP Read 8 bytes using CS2
```

7. The interrupt can be cleared, if needed.

```
ST,50,F1,SP Clear interrupt
```

8. Read back the data buffer. Note that it is necessary to read back 11 data bytes since the first three bytes sent on the SPI port are the read code (03h) and the two subaddress bytes.

```
ST,50,00,00,00,01,02,03,04,05,06,07,08,SP Read the data buffer
```

It can be seen that on the I<sup>2</sup>C-bus the first four bytes do not contain the data from the SPI bus. The first byte is SC18IS606 address, followed by three dummy data bytes. These dummy data bytes correspond to the three bytes sent to the EEPROM before it actually places data on the bus (command 03h, subaddress 0030h).

## 9 Limiting values

Table 12 describes the limiting values for SC18IS606.

**Table 12. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).<sup>[1][2]</sup>

Symbol	Parameter	Conditions	Note	Min	Max	Unit
V <sub>DD</sub>	Supply voltage			-0.5	+4.6	V
T <sub>amb(bias)</sub>	Bias ambient temperature	Operating		-55	+150	°C
T <sub>stg</sub>	Storage temperature			-65	+150	°C
V <sub>I</sub>	Input voltage	5 V tolerant I/O pins; V <sub>DD</sub> ≥ 1.71 V	[3] [4]	-0.5	+5.4	V
		3 V tolerant I/O - all pins	[5]	-0.5	+3.6	V
I <sub>OH(I/O)</sub>	HIGH-level output current per input/output pin			-	8	mA
I <sub>OL(I/O)</sub>	LOW-level output current per input/output pin			-	20	mA
I <sub>I/O(tot)(max)</sub>	Maximum total I/O current			-	120	mA
P <sub>tot/pack</sub>	Total power dissipation per package		[6]	-	1.5	W

[1] This product includes circuitry designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

[2] Parameters are valid over the operating temperature range unless otherwise specified. All voltages are with respect to V<sub>SS</sub> unless otherwise noted.

[3] Applies to all 5 V tolerant I/O pins except the 3 V tolerant pin CITO.

[4] Including the voltage on outputs in 3-state mode.

[5] V<sub>DD</sub> is present or not present.

[6] Based on package heat transfer, not device power consumption.

## 10 Static characteristics

Table 13 describes the static characteristics for SC18IS606.

**Table 13. Static characteristics**

$V_{DD} = 1.71\text{ V to }3.6\text{ V}$ ;  $T_{amb} = -40\text{ °C to }+105\text{ °C}$ , unless otherwise specified

Symbol	Parameter	Conditions	Note	Min	Typ <sup>[1]</sup>	Max	Unit
$V_{DD}$	Supply voltage			1.71		3.6	V
$I_{DD(oper)}$	Operating supply current	$V_{DD} = 3.3\text{ V}$		-	2.1	4.0	mA
$I_{DD(idle)}$	Idle mode supply current	$V_{DD} = 3.3\text{ V}$		-	1.3	3.4	mA
$V_{th(HL)}$	HIGH-LOW threshold voltage	Schmitt trigger input		$0.22V_{DD}$	$0.4V_{DD}$	-	V
$V_{th(LH)}$	LOW-HIGH threshold voltage	Schmitt trigger input		-	$0.6V_{DD}$	$0.7V_{DD}$	V
$V_{hys}$	Hysteresis voltage			-	$0.2V_{DD}$	-	V
$V_{OL}$	LOW-level output voltage	All pins					
		$I_{OL} = 4\text{ mA}$ ; $2.5\text{ V} \leq V_{DD} \leq 3.6\text{ V}$		-		0.5	V
		$I_{OL} = 3\text{ mA}$ ; $1.71\text{ V} \leq V_{DD} \leq 2.5\text{ V}$		-		0.5	V
$V_{OH}$	HIGH-level output voltage	All pins					
		$I_{OH} = 4\text{ mA}$ ; $2.5\text{ V} \leq V_{DD} \leq 3.6\text{ V}$		$V_{DD} - 0.4$	-	-	V
		$I_{OH} = 3\text{ mA}$ ; $1.71\text{ V} \leq V_{DD} \leq 2.5\text{ V}$		$V_{DD} - 0.5$	-	-	V
$C_{ig}$	Input capacitance at the gate		[2]	-	-	15	pF
$I_{IL}$	LOW-level input current	Logical 0; $V_I = 0.4\text{ V}$		-	-	-80	μA
$I_{LI}$	Input leakage current	All ports; $V_I = V_{IL}$ or $V_{IH}$	[3]	-	-	±10	μA
$I_{THL}$	HIGH-LOW transition current	All ports; logical 1-to-0; $V_I = 2.0\text{ V}$ at $V_{DD} = 3.6\text{ V}$		-30	-	-450	μA
$I_{pu}$	Pull-up current	$V_I = 0\text{ V}$ ;	[4]				μA
		$2.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}$		10	50	90	μA
		$1.71\text{ V} \leq V_{DD} \leq 2.0\text{ V}$		7	50	85	μA
		$V_{DD} < V_I < 5\text{ V}$		0	0	0	μA

[1] Typical ratings are not guaranteed. The values listed are at room temperature, 3 V.

[2] Pin capacitance is characterized but not tested.

[3] Measured with pins in high-impedance mode.

[4] Pullup current measured across the weak pullup resistor

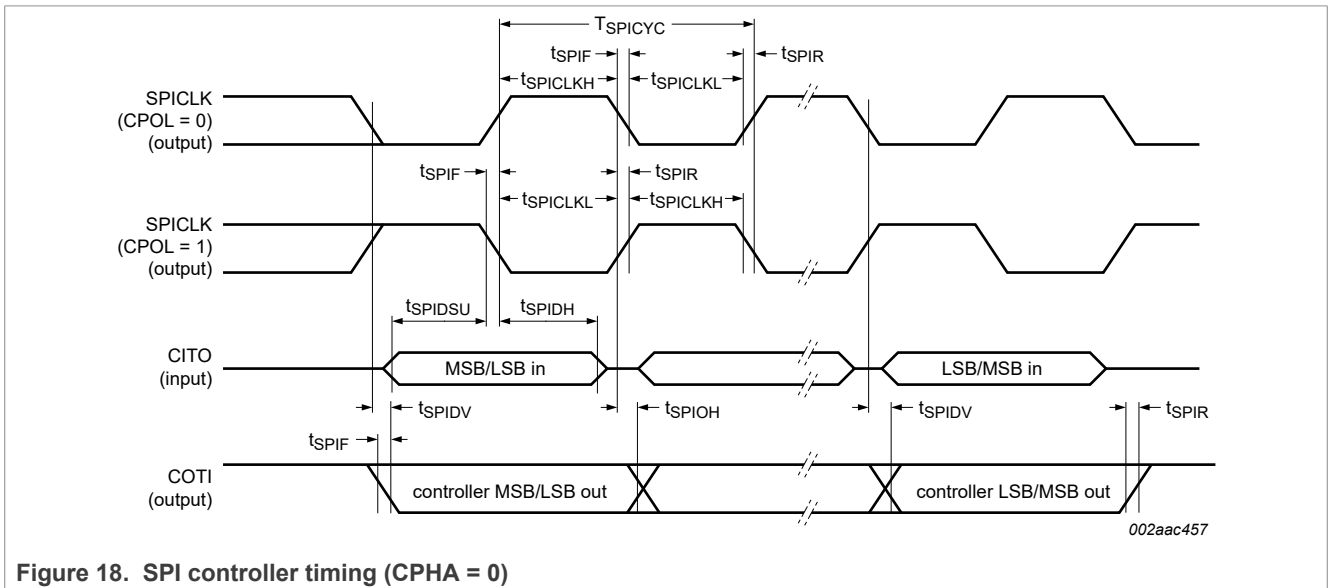
### 11 Dynamic characteristics

Table 14 describes the dynamic characteristics for SC18IS606.

Table 14. Dynamic characteristics

$V_{DD} = 1.71\text{ V to }3.6\text{ V}$ ;  $T_{amb} = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$ , unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Glitch filter</b>						
$t_{gr}$	Glitch rejection time	RESET pin	-	-	20	ns
$t_{sa}$	Signal acceptance time	RESET pin	125	-	-	ns
		Any pin except RESET	50	-	-	ns
<b>SPI controller interface</b>						
$f_{SPI}$	SPI operating frequency	1.875 MHz	-	-	1.875	MHz
$T_{SPICYC}$	SPI cycle time	1.875 MHz	533	-	-	ns
$t_{DS}$	Data set-up time		10	-	-	ns
$t_{DH}$	Data hold time		7	-	-	ns
$t_{V(Q)}$	Data output valid time		-	-	2	ns



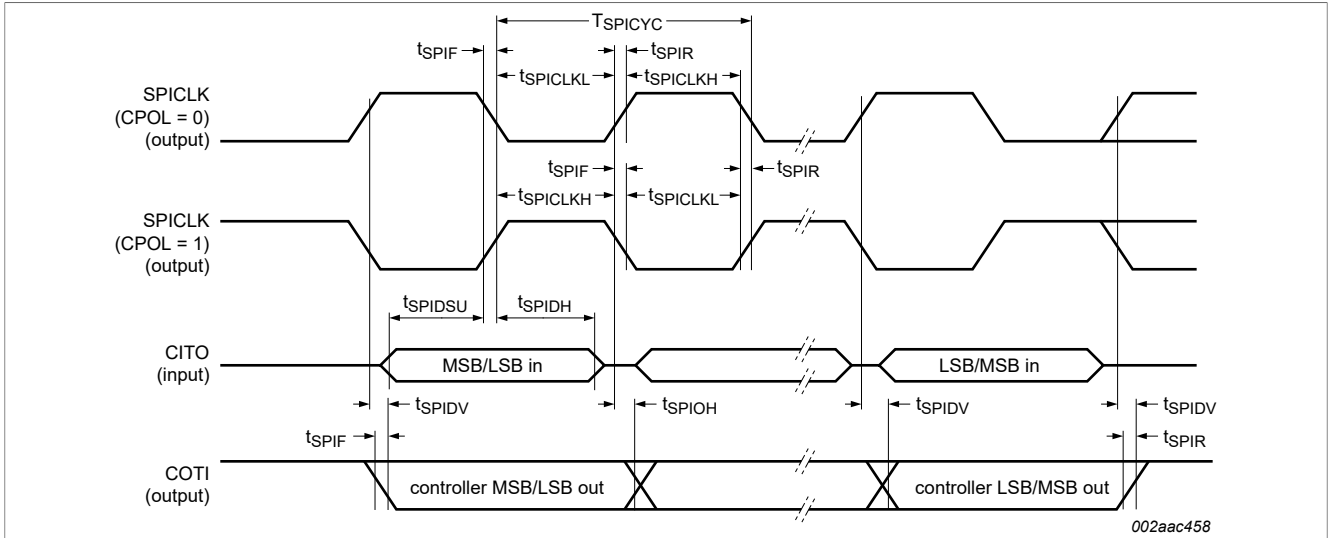


Figure 19. SPI controller timing (CPHA = 1)

## 12 Package outline

Figure 20 shows the package outline for the SC18IS606.

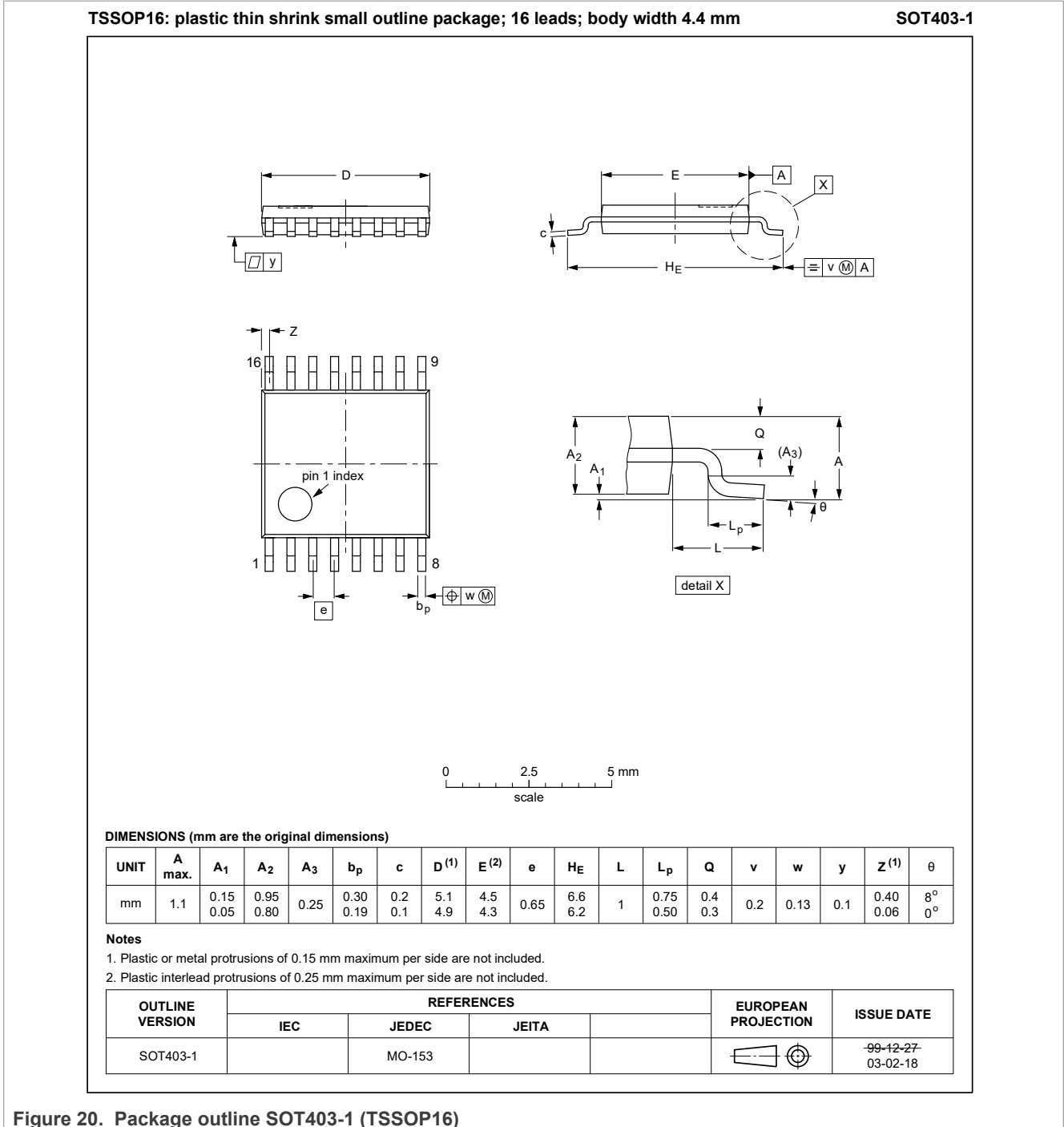
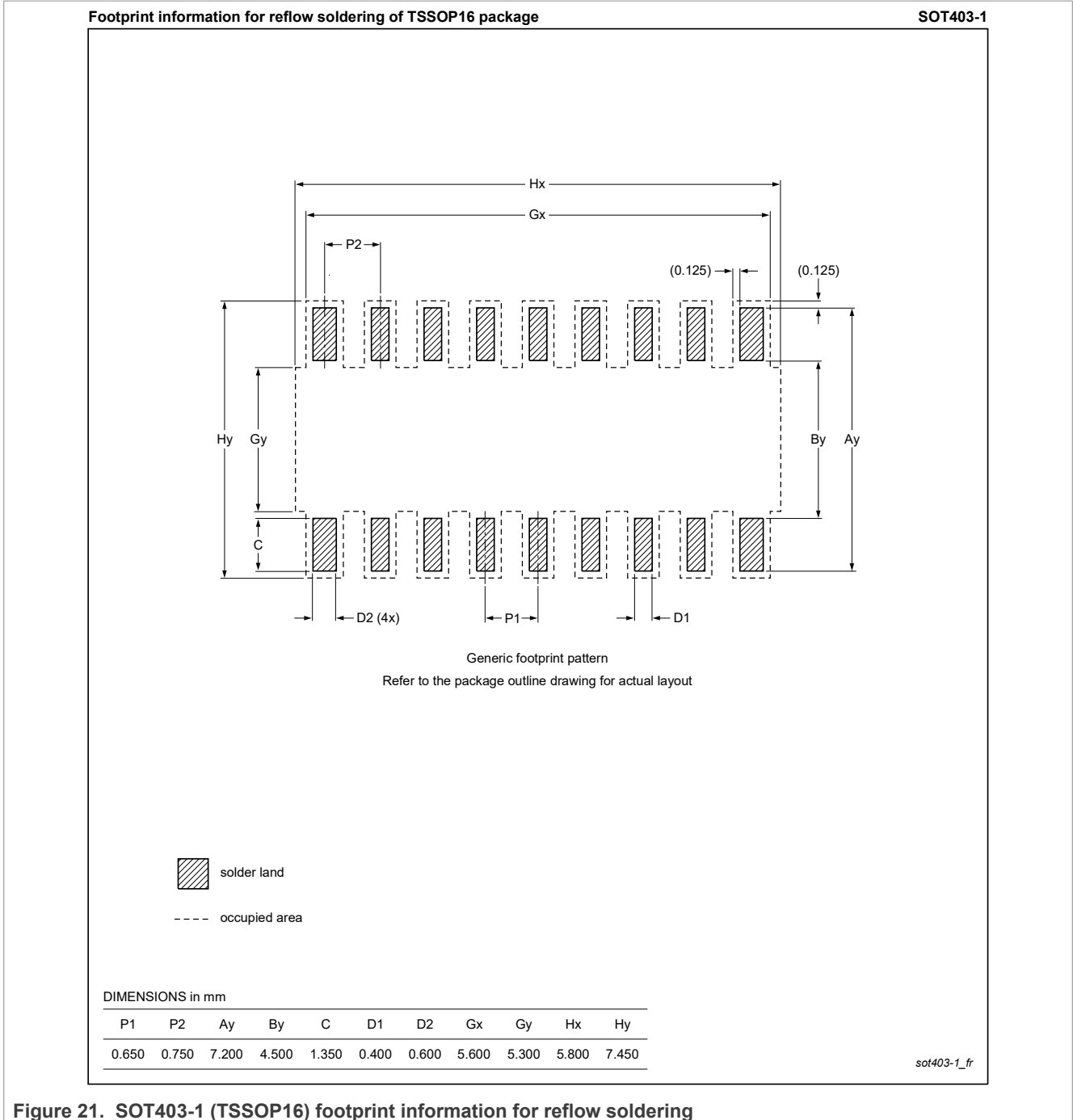


Figure 20. Package outline SOT403-1 (TSSOP16)

### 13 Printed Circuit Board (PCB) layout

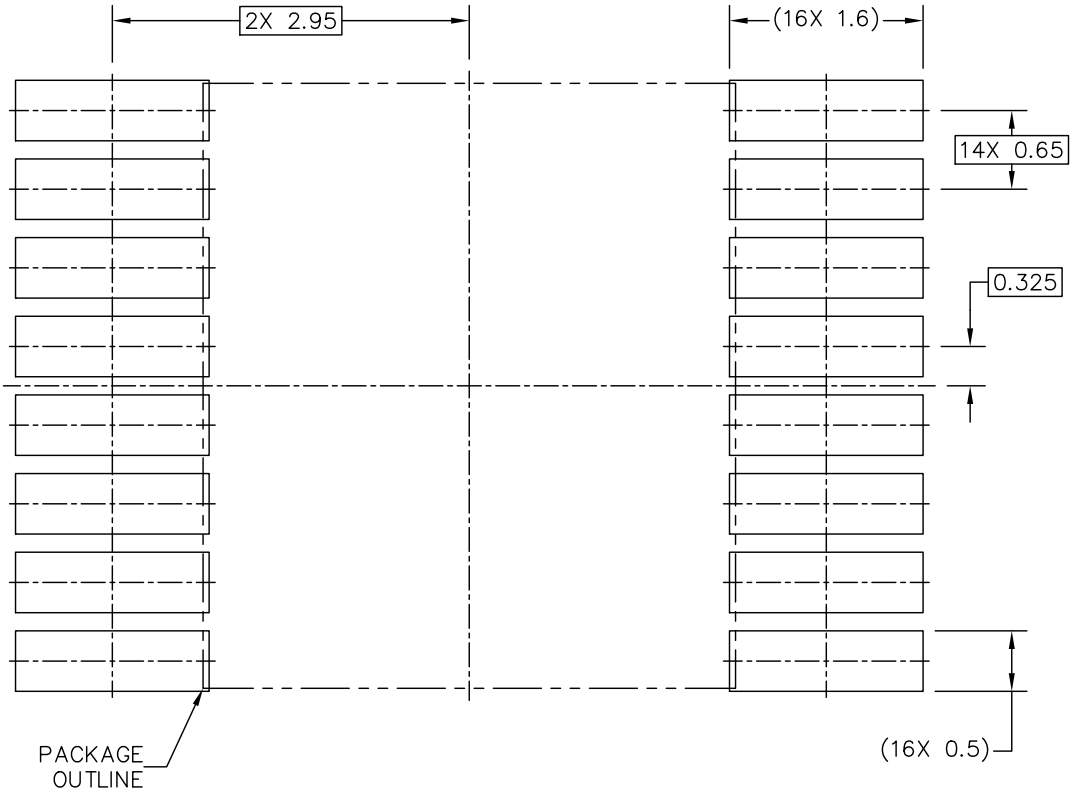
This section shows the PCB layout for the SC18IS606.



**Figure 21. SOT403-1 (TSSOP16) footprint information for reflow soldering**

PDSO-G-16 I/O  
4.4 X 5 X 1.1 PKG, 0.65 PITCH

SOT403-1



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. ALL RIGHTS RESERVED

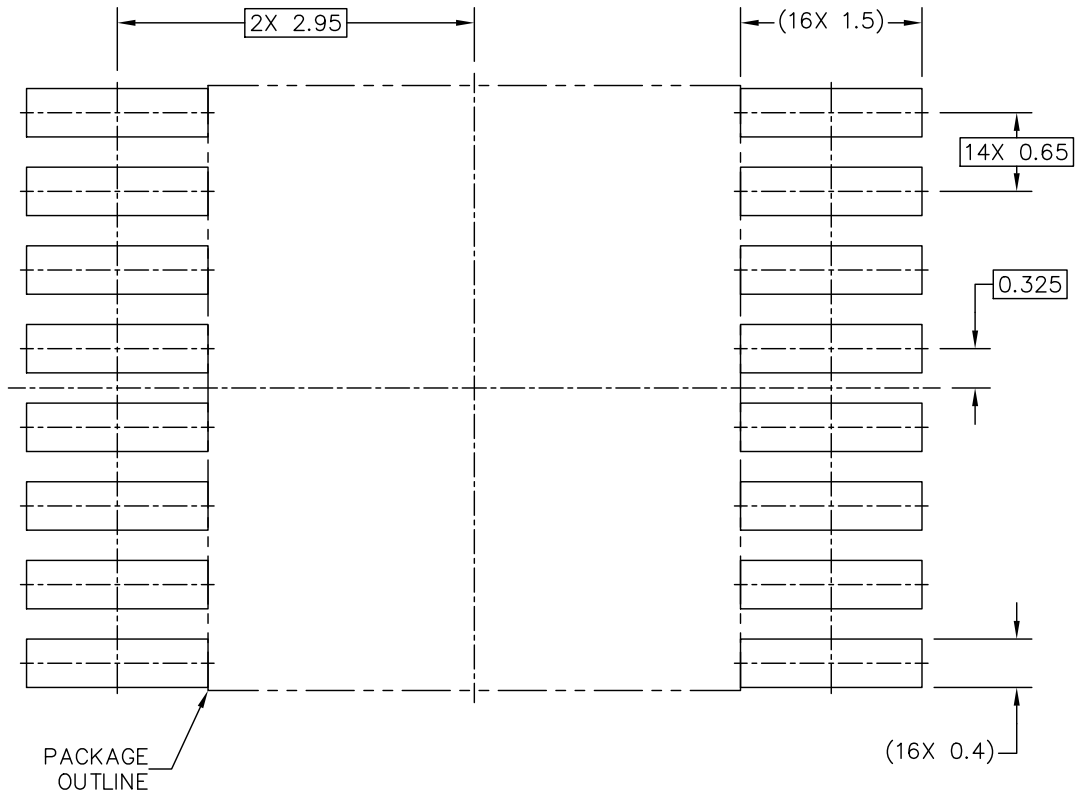
DATE: 28 NOV 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: MO-153	DRAWING NUMBER:	REVISION:	PAGE:
--	---------------------	-----------------	-----------	-------

Figure 22. SOT403-1 (TSSOP16) solder mask opening pattern

PDSO-G-16 I/O  
4.4 X 5 X 1.1 PKG, 0.65 PITCH

SOT403-1



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. ALL RIGHTS RESERVED

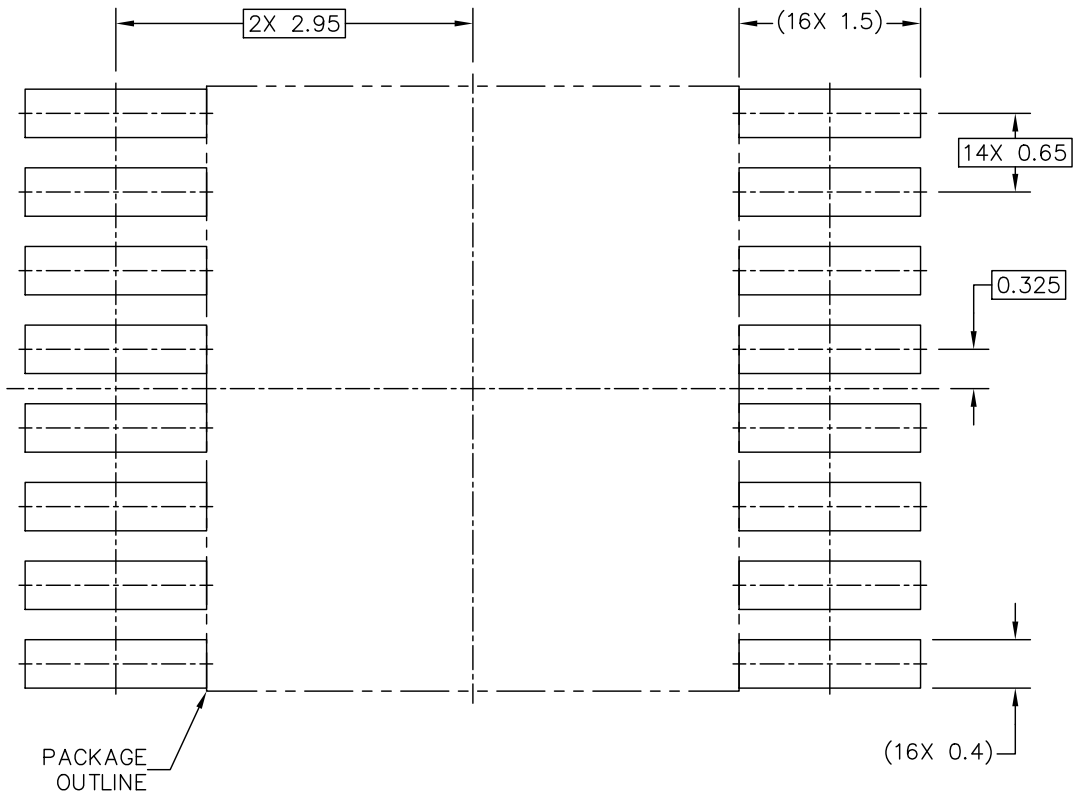
DATE: 28 NOV 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: MO-153	DRAWING NUMBER:	REVISION:	PAGE:
--	---------------------	-----------------	-----------	-------

Figure 23. SOT403-1 (TSSOP16) I/O pads and solderable area

PDSO-G-16 I/O  
4.4 X 5 X 1.1 PKG, 0.65 PITCH

SOT403-1



RECOMMENDED STENCIL THICKNESS 0.125 OR 0.150

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. ALL RIGHTS RESERVED

DATE: 28 NOV 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: MO-153	DRAWING NUMBER:	REVISION:	PAGE:
--	---------------------	-----------------	-----------	-------

Figure 24. SOT403-1 (TSSOP16) Solder paste stencil

## 14 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note AN10365 “Surface mount reflow soldering description”.

### 14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

### 14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 25](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board

- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 15](#) and [Table 16](#)

Table 15. SnPb eutectic process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 16. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 25](#).

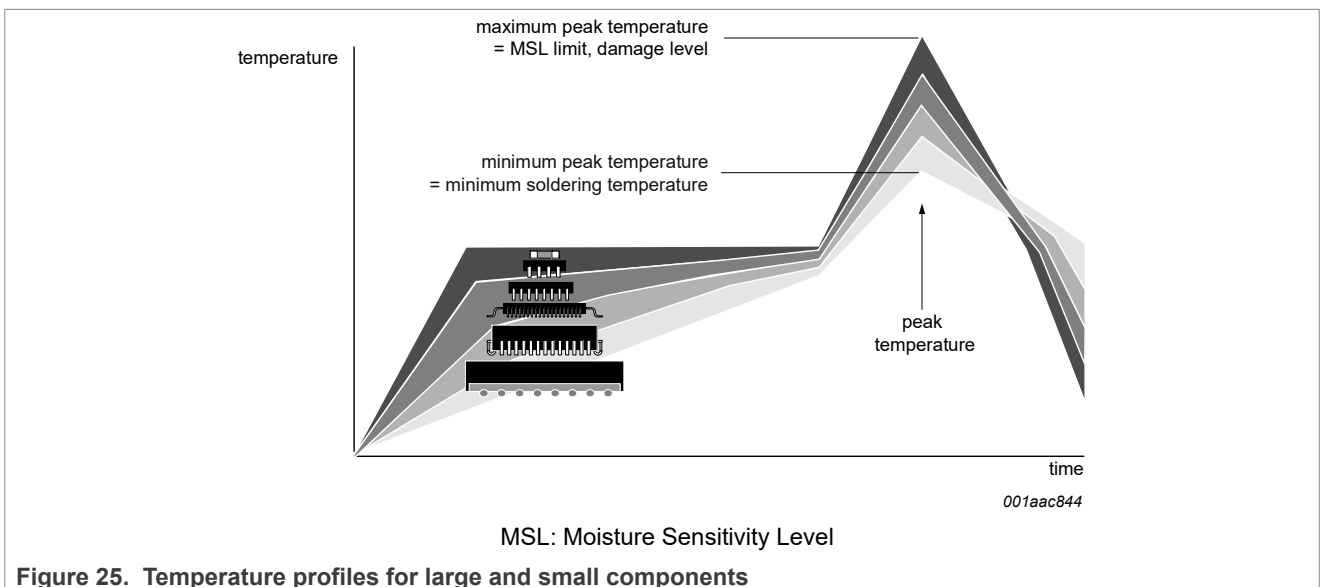


Figure 25. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

## 15 Acronyms

[Table 17](#) lists the acronyms used in this document.

**Table 17. Acronyms**

Acronym	Description
COTI	Controller Output Target Input
CPU	Central Processing Unit
CITO	Controller Input Target Output
CS	Chip Select
EEPROM	Electrically Erasable Programmable Read-Only Memory
ESD	Electrostatic Discharge
GPIO	General-Purpose Input/Output
HBM	Human Body Model
I/O	Input/Output
I <sup>2</sup> C-bus	Inter-Integrated Circuit bus
LSB	Least Significant Bit
MM	Machine Model
MSB	Most Significant Bit
PCB	Printed Circuit Board
SCL	Serial Clock
SDA	Serial Data
SMD	Surface Mounted Device
SPI	Serial Peripheral Interface

## 16 Revision history

[Table 18](#) summarizes revisions to this document.

**Table 18. Revision history**

Document ID	Release date	Description
SC18IS606 v.1.1	27 May 2026	Updated as per CIN# 2026050021: <ul style="list-style-type: none"><li>• Removed IDD(tpd) parameter related information in <a href="#">Section 10</a>.</li><li>• Minor editorial changes</li></ul>
SC18IS606 v.1.0	15 September 2021	Initial public release

## Legal information

### Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <https://www.nxp.com>.

### Definitions

**Draft** — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <https://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Quick reference data** — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Suitability for use in non-automotive qualified products** — Unless this document expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

**HTML publications** — An HTML version, if available, of this document is provided as a courtesy. Definitive information is contained in the applicable document in PDF format. If there is a discrepancy between the HTML document and the PDF document, the PDF document has priority.

**Translations** — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

**Security** — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at [PSIRT@nxp.com](mailto:PSIRT@nxp.com)) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

**NXP B.V.** — NXP B.V. is not an operating company and it does not distribute or sell products.

## Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

**NXP** — wordmark and logo are trademarks of NXP B.V.

**I2C-bus** — logo is a trademark of NXP B.V.

## Tables

Tab. 1.	Ordering information .....	4	Tab. 10.	GPIO Configuration (F7h) bit allocation .....	12
Tab. 2.	Ordering options .....	4	Tab. 11.	GPIO Configuration (F7h) bit description .....	12
Tab. 3.	Pin description .....	6	Tab. 12.	Limiting values .....	16
Tab. 4.	Function ID 01h to 0x7h .....	8	Tab. 13.	Static characteristics .....	17
Tab. 5.	Configure SPI Interface (F0h) bit allocation .....	9	Tab. 14.	Dynamic characteristics .....	18
Tab. 6.	Configure SPI Interface (F0h) bit description .....	9	Tab. 15.	SnPb eutectic process (from J-STD-020D) .....	26
Tab. 7.	GPIO Write (F0h) bit allocation .....	10	Tab. 16.	Lead-free process (from J-STD-020D) .....	26
Tab. 8.	GPIO Read (F5h) bit allocation .....	11	Tab. 17.	Acronyms .....	27
Tab. 9.	GPIO Enable (F6h) bit allocation .....	11	Tab. 18.	Revision history .....	28

**Figures**

Fig. 1.	Block diagram of SC18IS606 .....	5	Fig. 16.	Input-only configuration .....	13
Fig. 2.	Pin configuration for TSSOP16 .....	6	Fig. 17.	Push-pull output configuration .....	13
Fig. 3.	I2C-bus configuration .....	7	Fig. 18.	SPI controller timing (CPHA = 0) .....	18
Fig. 4.	Target address .....	7	Fig. 19.	SPI controller timing (CPHA = 1) .....	19
Fig. 5.	Write to a data buffer .....	8	Fig. 20.	Package outline SOT403-1 (TSSOP16) .....	20
Fig. 6.	I2C-bus message .....	8	Fig. 21.	SOT403-1 (TSSOP16) footprint information for reflow soldering .....	21
Fig. 7.	SPI message .....	8	Fig. 22.	SOT403-1 (TSSOP16) solder mask opening pattern .....	22
Fig. 8.	Read from buffer .....	9	Fig. 23.	SOT403-1 (TSSOP16) I/O pads and solderable area .....	23
Fig. 9.	Configure SPI Interface .....	9	Fig. 24.	SOT403-1 (TSSOP16) Solder paste stencil ....	24
Fig. 10.	Clear Interrupt .....	10	Fig. 25.	Temperature profiles for large and small components .....	26
Fig. 11.	Idle mode .....	10			
Fig. 12.	GPIO Write .....	10			
Fig. 13.	GPIO Read .....	11			
Fig. 14.	GPIO Enable .....	11			
Fig. 15.	Open-drain output configuration .....	13			

## Contents

<b>1</b>	<b>General description</b> .....	<b>1</b>
<b>2</b>	<b>Features and benefits</b> .....	<b>2</b>
<b>3</b>	<b>Applications</b> .....	<b>3</b>
<b>4</b>	<b>Ordering information</b> .....	<b>4</b>
4.1	Ordering options .....	4
<b>5</b>	<b>Block diagram</b> .....	<b>5</b>
<b>6</b>	<b>Pinning information</b> .....	<b>6</b>
6.1	Pinning .....	6
6.2	Pin description .....	6
<b>7</b>	<b>Functional description</b> .....	<b>7</b>
7.1	I <sup>2</sup> C-bus interface .....	7
7.1.1	Addressing .....	7
7.1.2	Write to a data buffer .....	8
7.1.3	SPI read and write - Function ID 01h to 0x7h .....	8
7.1.4	Read from buffer .....	9
7.1.5	Configure SPI Interface - Function ID F0h .....	9
7.1.6	Clear Interrupt - Function ID F1h .....	10
7.1.7	Idle mode - Function ID F2h .....	10
7.1.8	GPIO Write - Function ID F4h .....	10
7.1.9	GPIO Read - Function ID F5h .....	10
7.1.10	GPIO Enable - Function ID F6h .....	11
7.1.11	GPIO Configuration - Function ID F7h .....	12
7.1.11.1	Open-drain output configuration .....	12
7.1.11.2	Input-only configuration .....	13
7.1.11.3	Push-pull output configuration .....	13
7.1.12	Read Version: Function ID FEh .....	13
7.2	SPI interface .....	14
<b>8</b>	<b>I<sup>2</sup>C-bus to SPI communications example</b> ....	<b>15</b>
<b>9</b>	<b>Limiting values</b> .....	<b>16</b>
<b>10</b>	<b>Static characteristics</b> .....	<b>17</b>
<b>11</b>	<b>Dynamic characteristics</b> .....	<b>18</b>
<b>12</b>	<b>Package outline</b> .....	<b>20</b>
<b>13</b>	<b>Printed Circuit Board (PCB) layout</b> .....	<b>21</b>
<b>14</b>	<b>Soldering of SMD packages</b> .....	<b>25</b>
14.1	Introduction to soldering .....	
14.2	Wave and reflow soldering .....	
14.3	Wave soldering .....	
14.4	Reflow soldering .....	
<b>15</b>	<b>Acronyms</b> .....	<b>27</b>
<b>16</b>	<b>Revision history</b> .....	<b>28</b>
	<b>Legal information</b> .....	<b>29</b>

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.